Application Report
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Using the TPS55340 as a SEPIC Converter

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ABSTRACT

Applications may require a DC/DC converter to provide a regulated output voltage between the minimum and maximum input voltage. A single buck or boost cannot supply the required output. However, a boost converter integrated circuit (IC) can be configured to drive a single-ended, primary-inductor converter (SEPIC) power stage and provide a regulated output voltage between the input voltage extremes. This application report goes through a detailed design procedure based on the TPS55340 data sheet including component selection and layout considerations. Lastly, considerations for improvements and advantages of a SEPIC design are covered.

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1 Brief Overview of an Ideal SEPIC Power Stage

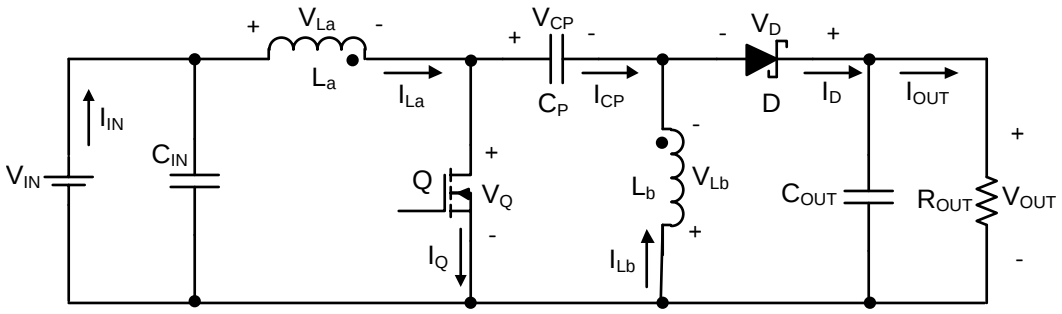

Figure 1. SEPIC Power Stage

The SEPIC topology fits in applications where the system requires a regulated output voltage from an input varying from above to below the output voltage. This is very useful when a regulated output is required from a low-cost unregulated power supply. Figure 1 shows the topology of a basic SEPIC Power Stage.

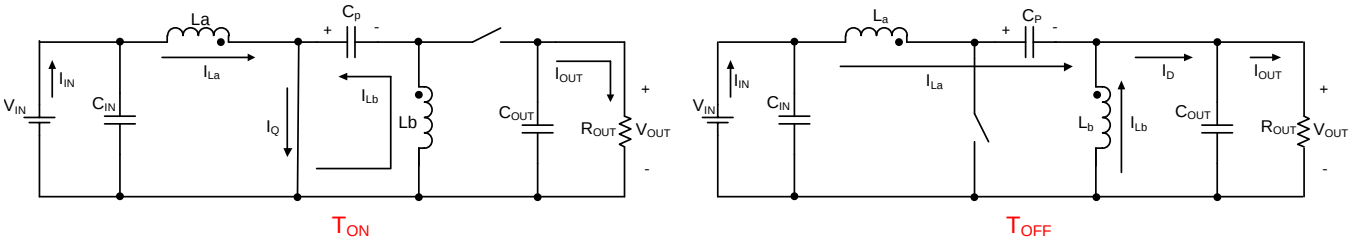

Figure 2. SEPIC Equivalent Circuit During Switch On Time and Off Time

Figure 2 details the SEPIC during the on time and off time of the switch and Figure 3 shows the current and voltage waveforms. During the on time, energy is stored in La from V_{IN}. The positive side of C_P is held to ground with the internal switch. When using a coupled inductor the one-to-one turns ratio pulls the negative side of C_P to $-V_{IN}$. The voltage across both inductors is equal to V_{IN}. The output diode is reverse biased and the output load current is supplied by the output capacitor.

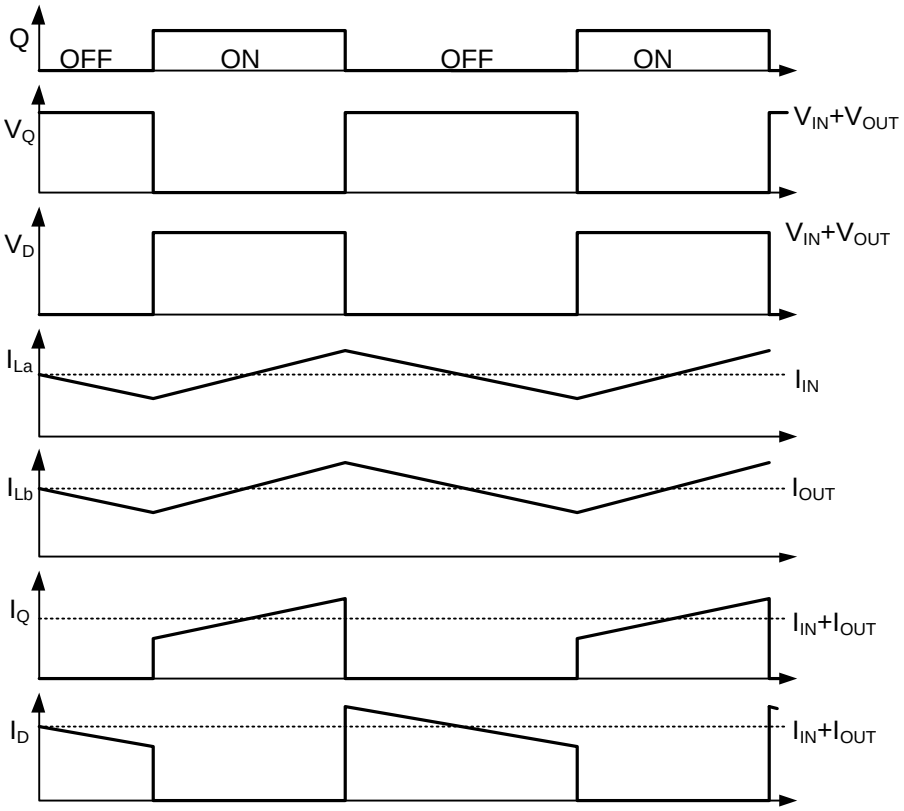

Figure 3. Voltage and Current Waveforms in a SEPIC

During the off time, C_P is recharged through La from V_{IN}. C_{OUT} is recharged from both the currents in Lb and through C_P from La. With the output diode conducting, the voltage across Lb is clamped to V_{OUT}. Through the one-to-one ratio of a coupled inductor, the voltage across the switch is equal to the sum of V_{IN} and V_{OUT}. The voltage across both La and Lb is $-V_{OUT}$.

As can be seen, this topology requires two inductors. However, using one coupled inductor can reduce cost and PCB area. This is allowed because the voltage across each individual inductor is equal during both the on time and off time of the switch. A major advantage of using a coupled inductor is the current ripple is shared between the two windings, thus decreasing the inductance required to meet a desired ripple in half. Also, most inductor vendors have a wide variety of off-the-shelf coupled inductors available and are typically lower in cost than two single inductors. The equations given in the following design assume a coupled inductor is used although a two inductor design is possible.

Lastly, using a boost converter, like the TPS55340, is also advantageous. When compared to a boost controller, the component count and PCB area is reduced because the switching MOSFET is internal to the IC. Additionally, not having to choose an external switching MOSFET reduces the complexity of the design.

2 Calculations and Component Selection

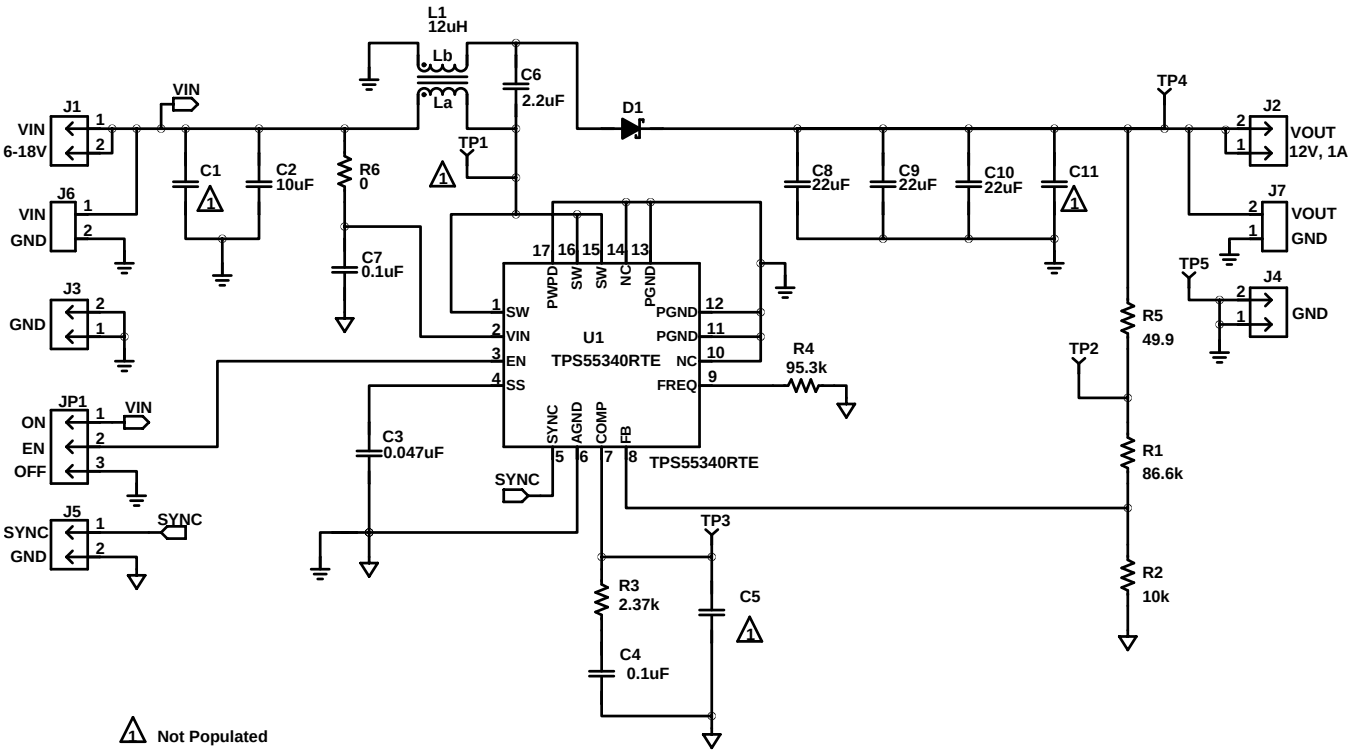

Figure 4. TPS55340EVM-147 Schematic

Table 1. Reference Design Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Voltage Range, V_{IN}		6	12	18	V
Switching Frequency, f_{SW}			500		kHz
OUTPUT CHARACTERISTICS					
Output Voltage, V_{OUT}			12		V
Output Current, I_{OUT}		0		1	A
Output Voltage Ripple, V_{RIPPLE}	V_{IN} = 6 V, I_{OUT} = 1 A		60		mVpp
Conservative Efficiency Estimate, η_{EST}	V_{IN} = 6 V, I_{OUT} = 1 A	85%			
Load Step, ΔI_{TRAN}			500		mA
Transient V_{OUT} Deviation, ΔV_{TRAN}			480		mV

The following calculations are done with the aid of the excel spreadsheet located in the product folder and by referring to Figure 4 for the schematic.

2.1 Switching Frequency (R4)

As with any switching regulator, choosing the switching frequency is one of the main tradeoffs to consider when creating a design. Lower switching frequencies are generally used for higher efficiency with relatively larger external component size. A higher switching frequency, on the other hand, results in smaller component size with relatively lower efficiency. This design uses 500 kHz in the middle of the TPS55340 operating range. The resistance to set this frequency is calculated with Equation 1 from the product data sheet and the nearest standard value is used. For 500-kHz switching frequency, the calculated resistance is 94.5 kΩ. The nearest standard value used is 95.3 kΩ.

$$R_{FREQ}(k\Omega) = 57500 \times f_{SW}(kHz)^{-1.03} \quad (1)$$

2.2 Duty-Cycle Calculations

For further calculations, the minimum and maximum duty cycles are first estimated in continuous conduction mode (CCM). This is done using Equation 2. Limitations are placed on the duty cycle based first on the TPS55340 maximum duty cycle minimum of 89%. The minimum duty cycle at which the device begins pulse skipping (D_{PS}) can be calculated based on the chosen switching frequency and the minimum controllable on time of the part (77 ns typical) with Equation 3. Typical applications will only see pulse skipping at very light loads while operating in discontinuous conduction mode (DCM). The operation in this mode is the same as shown and described in the datasheet for a boost converter design example.

$$D=\frac{V_{OUT}+V_D}{V_{OUT}+V_D+V_{IN}} \quad (2)$$

$$D_{PS}=T_{ON}min\times f_{SW} \quad (3)$$

V_D is the forward voltage drop of the rectifying diode, estimated at 0.5 V. The typical pulse skipping duty cycle in the example design is 4%. With the minimum input voltage V_{IN}min = 6 V, the maximum duty cycle is, Dmax = 0.68. Similarly, with the maximum input voltage V_{IN}max = 18 V, the minimum duty cycle is, Dmin = 0.41.

The regulator enters DCM when the sum of the currents in the two inductors ramp to zero at the end of each switching cycle. The critical current when the device operates in DCM can be calculated with Equation 4. While operating in this mode, in addition to the input and output voltage, the duty cycle is a function of the load current, inductance and switching frequency. The duty cycle can be estimated with Equation 5.

$$I_{OUT}crit=\frac{V_{IN}^2\times(V_{OUT}+V_D)}{2\times f_{SW}\times L\times(V_{OUT}+V_D+V_{IN})^2} \quad (4)$$

$$D_{DCM}=\frac{\sqrt{2\times L\times(V_{OUT}+V_D)\times I_{OUT}\times f_{SW}}}{V_{IN}} \quad (5)$$

2.3 Maximum Output Current

To determine your maximum output current, a few design parameters must first be decided on. For stable power supply operation and to minimize EMI, the inductor is chosen to keep the inductor ripple current (ΔI_L) a fraction of the DC current in La. The DC current in La is equal to the maximum DC input current (I_{IN}DC). The fraction is represented by the coefficient K_{IND} and is typically 0.2 to 0.4. Similar to other switching regulators, by choosing a higher K_{IND} the recommended inductance is lower. This increases the current ripple and a smaller inductor package is possible for a given saturation current. The higher current ripple typically leads to higher EMI, a lower maximum output current, larger output capacitance for a desired output ripple and a faster transient performance. The opposite is true for lower K_{IND}. The recommended inductance is higher, decreasing the current ripple and increasing the inductor package size. The lower current ripple typically reduces EMI, increases the maximum output current, reduces the needed output capacitance, and slows the transient response. The tradeoffs must be made based on the system level goals of the design.

The maximum input current is first calculated with Equation 6, using a conservative estimated full load efficiency, η_{EST} = 85% and V_{IN}min = 6 V. Equation 7 then calculates the desired peak-to-peak current ripple.

$$I_{IN}DC=\frac{V_{OUT}\times I_{OUT}}{\eta_{EST}\times V_{IN}min} \quad (6)$$

$$\Delta I_L=I_{IN}DC\times K_{IND} \quad (7)$$

I_{IN}DC is estimated at 2.35 A and with K_{IND} = 0.3, the desired ripple current is 706 mA. Based on this, the maximum output current (I_{OUT}max) can be calculated with Equation 8. This equation assumes a coupled inductor will be used and the TPS55340's minimum peak current limit (I_{LIM}) of 5.25 A.

$$I_{OUT}max=\frac{(I_{LIM}-\Delta I_L)}{\left(\frac{V_{OUT}}{V_{IN}min\times\eta_{EST}}+1\right)} \quad (8)$$

With the desired current ripple, the estimated maximum output current is 1.20 A. As can be seen in the equations, the maximum output current depends on the efficiency of the design and the inductor chosen. After choosing an inductor and with further evaluation of the full load efficiency, the design may be able to support higher maximum output currents.

2.4 Inductor (L1)

Based on the targeted ΔI_L, the minimum inductance (L) is calculated with Equation 9. The maximum input voltage and its corresponding duty cycle are used because this is when the current ripple in a SEPIC is the maximum. Again, the equation assumes a coupled inductor is used reducing the required inductance by half.

$$L \geq \frac{V_{IN} \times D}{2 \times f_{SW} \times \Delta I_L} \tag{9}$$

For this design, a recommended minimum L of 10.5 µH is calculated and the nearest standard value of 12 µH is chosen. With a 12 µH inductor, by rearranging Equation 9, ΔI_L is calculated to 615 mA at V_{IN}max and 338 mA at V_{IN}min. At this point you can choose to reevaluate the maximum output current with the chosen inductance. Using Equation 8, the maximum output current has increased to 1.47 A. The peak current and RMS current must then be calculated to ensure the inductor is properly rated. In a coupled inductor the total peak current is the sum of the peak current in each winding. Equation 10 calculates the peak current.

$$I_L\text{peak} = I_{La}\text{peak} + I_{Lb}\text{peak} = \left(I_{IN}\text{max} + \frac{\Delta I_L}{2}\right) + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \tag{10}$$

For this design, the peak current is estimated to be 3.69 A. It is recommended that the saturation current of the inductor be 20% higher than the peak current or greater than the peak current limit of the IC. This leaves margin for transient conditions when the peak inductor current may increase above the steady state value. Using the peak current limit of the IC is the most conservative criteria and ensures the inductor doesn't become saturated during an over current fault condition. This design uses the 6.6 A typical current limit for the minimum saturation current rating.

Equation 11 and Equation 12 calculate the RMS current in each winding. Equation 13 and Equation 14 take these currents and converts them to the ratings (I_{RMS}one and I_{RMS}both) typically shown on the data sheets of coupled inductors. I_{RMS}one represents only one winding conducting and I_{RMS}both represents both windings conducting equally. The ratings are typically given for a 40°C temperature rise.

$$I_{La}\text{RMS} \approx I_{IN}\text{DC} \tag{11}$$

$$I_{Lb}\text{RMS} \approx I_{OUT} \tag{12}$$

$$I_{RMS}\text{one} = \sqrt{\left(I_{La}\text{RMS}\right)^2 + \left(I_{Lb}\text{RMS}\right)^2} \tag{13}$$

$$I_{RMS}\text{both} = \sqrt{\frac{\left(I_{RMS}\text{one}\right)^2}{2}} \tag{14}$$

The equivalent RMS values calculated for the inductor are I_{RMS}one = 2.56 A and I_{RMS}both = 1.81 A. Based on the saturation current rating and RMS current calculation, 4 families of coupled inductors are within or near the specifications. These are shown in Table 2. For this design the MSD1260-123 is used. It should be noted, choosing an inductor with a lower DCR can improve the efficiency of the design. If both windings of the chosen inductor have equal DCR, the conduction losses can be calculated with Equation 15. The estimated conduction loss in the inductor at full load for this design is 484 mW with the minimum input voltage.

$$P_L = \left(\left(I_{La}\text{RMS}\right)^2 + \left(I_{Lb}\text{RMS}\right)^2\right) \times \text{DCR} \tag{15}$$

Table 2. Example Catalogue Coupled Inductors

Vendor	Part Number	L (µH)	I_{RMS}both (A)	I_{RMS}one (A)	I_{SAT} (A)	DCR (mΩ)
CoilCraft	MSD1260-123	12	2.21	3.12	6.86	74
Wurth Elektronic	744870100	10	2.7		7	44
Bourns	SRF1260-10	10	2.67	5.35	7.17	49.2
Cooper	DRQ125-100-R	10	2.67	5.35	7.17	37.8

2.5 Output Capacitor (C8-C10)

The output capacitor is chosen based on the maximum output voltage ripple and minimum output voltage variation from load transients. A typical output voltage ripple (V_{RIPPLE}) specification is 0.5% of the nominal output voltage but this value is typically decided on at a system level. Based on the specification of 60-mVpp output ripple, Equation 16 is used to calculate the minimum output capacitance.

$$C_{OUT} \geq \frac{Dmax \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \tag{16}$$

The minimum output capacitance to meet this specification is 22.5 µF. This assumes a ceramic output capacitor is used with negligible ESR. If non ceramic capacitors are used it will contribute to additional voltage ripple. Equation 17 calculates the total ripple and Equation 18 calculates the maximum ESR to meet the voltage ripple specification. It is important to note, the ripple in the ESR is not in phase with the ripple from the output capacitance and Equation 18 under estimates the maximum ESR. In reality higher ESR may be possible with testing or simulation of the circuit.

$$V_{RIPPLE} = \frac{Dmax \times I_{OUT}}{f_{SW} \times C_{OUT}} + ESR_{COUT} \times \left(I_{La}peak + I_{Lb}peak\right) \tag{17}$$

$$ESR_{COUT} \leq \frac{V_{RIPPLE} - \frac{Dmax \times I_{OUT}}{f_{SW} \times C_{OUT}}}{\left(I_{La}peak + I_{Lb}peak\right)} \tag{18}$$

The minimum capacitance to meet the load transient response specification from Table 1 is calculated with Equation 19. The specification of the design is a maximum 4% output voltage change (480 mV) with a 50% max load step transient (500 mA).

$$C_{OUT} \geq \frac{\Delta I_{TRAN}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \tag{19}$$

With an estimated loop bandwidth or crossover frequency (f_{BW}) of 6 kHz, the minimum capacitance is 27.6 µF. The largest value calculated between Equation 16 and Equation 19 should be used to decide the minimum output capacitance. In this design, it is 27.6 µF from the transient specification.

If non ceramics are used or the output capacitors are specified an RMS current rating, Equation 20 calculates the RMS current. This is calculated at 1.44 A for this design.

$$I_{COUT}RMS = I_{OUT}\sqrt{\frac{Dmax}{(1\text{-}Dmax)}} \tag{20}$$

The output capacitors selected are 3 x 22-µF, 25-V X7R 1210 ceramic capacitors. When using ceramic capacitors it is important to account for derating due to DC bias. With a 12-V output voltage, the estimated capacitance is 46% the nominal value giving a derated capacitance of 30.4 µF.

2.6 AC Capacitor (C6)

It is recommended to choose the AC capacitor (C_P) so the ripple voltage ΔV_{CP} is no more than 5% of the maximum V_{CP}DC equal to V_{IN}max. Equation 21 calculates the minimum capacitance.

$$C_P \geq \frac{I_{OUT} \times Dmax}{0.05 \times V_{IN}max \times f_{SW}} \tag{21}$$

The minimum capacitance is calculated to be 1.5 µF and due to derating, the next highest standard value of 2.2 µF is used. This capacitor must be rated for the maximum input voltage and capacitance derating due to DC bias should be considered. The capacitor must also be rated for the RMS current (I_{CP}RMS). This is calculated as 1.63 A using Equation 22. The capacitor selected is a 2.2-µF, 50-V X7R 1206 ceramic capacitor.

$$I_{CP}RMS = I_{IN}DC \times \sqrt{\frac{(1-Dmax)}{Dmax}} \quad (22)$$

2.7 Input Capacitor (C2)

A 10-µF ceramic input capacitor is chosen based on the minimum recommended value of 4.7 µF for the TPS55340 and must be of quality X5R or X7R. This design also places an additional 0.1-µF capacitor (C7) close to the V_{IN} pin for extra decoupling and is optional. Equation 23 calculates the input voltage ripple ($V_{INRIPPLE}$) and Equation 24 calculates the RMS current if a rating is given. With an estimated derated capacitance of 6 µF, they are calculated to be 39.9 mV and 0.098 A respectively.

$$V_{INRIPPLE} = \frac{\Delta I_L}{4 \times f_{SW} \times C_{IN}} + I_{IN}DC \times ESR_{CIN} \quad (23)$$

$$I_{CIN}RMS = \frac{\Delta I_L}{\sqrt{12}} \quad (24)$$

2.8 Rectifying Diode (D1)

Similar to a boost converter, the average current through the diode is equal to the output current. The rectifying diode must be chosen to handle the output current and voltage at the switching node. At least 20% margin is recommended for the diode's average current rating. A conservative design will use the maximum output current with V_{IN}max with the typical current limit to choose the current rating. Equation 8 with V_{IN}max gives an output over current limit of 2.60 A. Equation 25 calculates the minimum breakdown voltage (V_{BR}) of the diode to be 30.5 V, assuming V_D is 0.5 V.

$$V_{BR} = V_{OUT} + V_{IN}max + V_D \quad (25)$$

The diode's package must be rated for the power dissipation. The power is calculated using Equation 26 to be 0.5 W with a 1-A output.

$$P_D = I_{OUT} \times V_D \quad (26)$$

Based on these criteria, Diodes Inc. B340B is chosen. This is a 40-V, 3-A diode in an SMB package.

2.9 MOSFET Ratings

The IC's internal MOSFET must also be able to handle the rated voltages and currents. As seen in Figure 3, the voltage at SW is the sum of V_{OUT} and V_{IN}. Similarly the peak current is equal to the sum of the input current, output current and peak to peak ripple current. Equation 27 calculates the voltage, Equation 28 calculates the current and Equation 29 calculates the RMS current.

$$V_Q = V_{OUT} + V_{IN}max \quad (27)$$

$$I_Q peak = I_{OUT} + I_{IN}DC + \Delta I_L \quad (28)$$

$$I_Q RMS = \frac{I_{IN}DC}{\sqrt{Dmax}} \quad (29)$$

In this design the voltage stress of the MOSFET is 30 V and the peak current is 3.69 A. During initial testing it is recommended to allow a 5-10% tolerance on the voltage rating to account for ringing on the SW node. Using effective layout techniques limits the ringing on the SW node. The ringing can be further reduced by using an external snubber which can be selected with the method presented in SLVA255

2.10 Feedback Resistors (R1,R2)

The feedback resistors are chosen the same as when the TPS55340 is in a boost topology. The bottom resistor (R2) is fixed at the recommended 10 kΩ to minimize noise and current through the feedback divider. The top resistor (R1) is then calculated with Equation 30 using the TPS55340's voltage reference (V_{REF}) of 1.229 V. R1 is calculated to 87.6 kΩ and the nearest standard value of 86.6 kΩ is chosen.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{30}$$

2.11 Soft Start Capacitor (C3)

The data sheet's recommended 0.047-µF soft start capacitor is used. If the soft start time needs to be longer to reduce voltage overshoot on the output during startup or to reduce inrush current, increase this capacitance.

2.12 Compensating the Control Loop (R3,C4,C5)

Deriving a mathematical model of the SEPIC converter is extremely complicated. The easiest and fastest method to design the compensation is to use a SPICE model or measured data. For this design, a Venable gain/phase analyzer is used to measure the power stage to choose the compensation components. A stable design provides a valid measurement. Initially, a large compensation capacitor (1 µF) and small compensation resistor (1 kΩ) are used to roll off the control loop at a low frequency.

When choosing your target crossover frequency there are two criteria you must meet. It is recommended to crossover at less than one third the lowest frequency right half plane zero (RHPZ) and there must be sufficient phase at the targeted crossover. RHPZ is calculated with Equation 31.The RHPZ is at the lowest frequency with the minimum input voltage and maximum output current. Therefore the compensation design is done at this operating point. The RHPZ is calculated at 36.7 kHz and the crossover frequency must be less than 12.2 kHz.

$$f_{RHPZ} = \frac{\frac{V_{OUT}}{I_{OUT}}}{2\pi \times L \times \left(\frac{D}{(1-D)} \right)^2} \tag{31}$$

The second criterion of sufficient phase is determined by your targeted phase margin. Based on a 60° recommended phase margin and assuming the compensation will have the maximum 180° phase, the control to output phase must be no less than -120°. As can be seen in Figure 5, the power stage phase is approximately -120° at 7 kHz and is used as the targeted bandwidth.

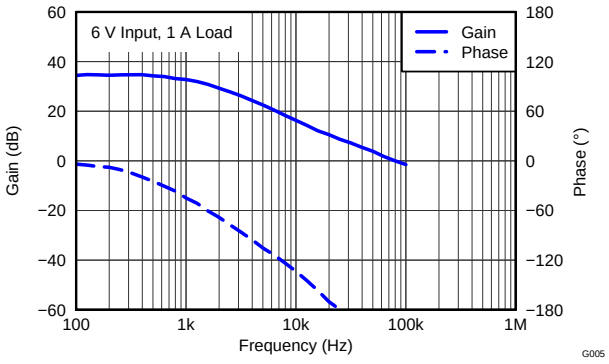

Figure 5. Measured Power-Stage Gain and Phase

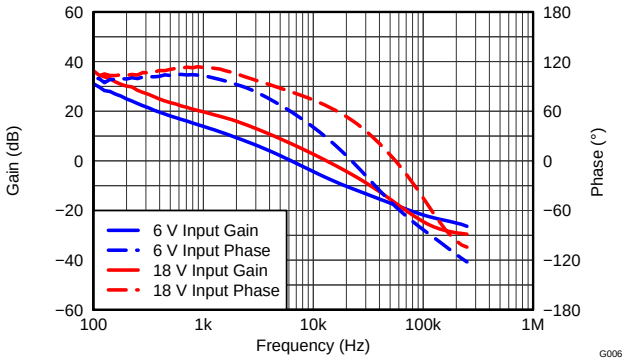

Figure 6. Measured Overall-Loop Gain and Phase

The compensation components must be chosen so the compensation gain is the inverse of the power stage gain at the desired bandwidth. The targeted compensation gain (K_{COMP}) is -19.50 dB. The value of R3 calculated with Equation 32, is 2.37 kΩ which is a standard value. The maximum value of Gea is used to ensure stability over IC variations and typical circuits will have a bandwidth lower than the targeted 7 kHz.

$$R3=\frac{10^{\left(\frac{K_{COMP}(f_{BW})}{20dB}\right)}}{Gea\times\frac{R1}{(R1+R2)}} \quad (32)$$

The compensation zero is typically set between 1/5 and 1/10 of f_{BW} to maximize phase at the crossover frequency. This design places the zero at 1/10 x f_{BW}. C4 is calculated with Equation 33 as 0.096 µF and the nearest standard value, 0.1 µF, is used.

$$C4=\frac{1}{2\pi\times R3\times\frac{f_{BW}}{10}} \quad (33)$$

C5, typically not needed with ceramic output capacitors, is used to add a high frequency pole to attenuate any high frequency noise. It is recommended to place this pole at 10 x f_{BW} or greater. Equation 34 calculates the capacitance based on the target pole frequency. If non ceramic output capacitors with higher ESR are used, this pole should be placed at the ESR zero from the output capacitors. Equation 35 calculates the value of C5 needed to add a pole at the ESR zero frequency. If C5 is not used, it can be modeled as 10 pF from stray board capacitance.

$$C5=\frac{1}{2\pi\times R3\times f_P} \quad (34)$$

$$C5=\frac{C_{OUT}\times ESR_{COUT}}{R3} \quad (35)$$

If more phase margin is needed to increase f_{BW} closer to the maximum frequency recommendation based on the RHPZ, add an additional zero by placing a feed-forward capacitor (C_{FF}) in parallel with the top feedback resistor, R1. A recommended location for this zero is somewhere greater than the target bandwidth frequency. The maximum recommended value of C_{FF} is calculated with Equation 36. Using C_{FF} also adds a pole in the compensation at a frequency higher than the added zero.

$$C_{FF}\le\frac{1}{2\pi\times R1\times f_{BW}\times\sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (36)$$

The overall loop response with the selected compensation components is shown in Figure 6. At full load with a 6-V input, the measured bandwidth is 6.3 kHz with 59.3° phase margin.

3 Layout Considerations

As for all switching power supplies, especially those operating at high frequencies with high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. This is done as follows:

- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling.
- In a SEPIC design there is an additional switching node at the connection between C_P, D1 and L1 and this area should also be minimized.
- The high current path including the switch, C6, Schottky diode and output capacitor contains nanosecond rise and fall times and should be kept as short as possible.
- The input capacitor needs not only to be close to the V_{IN} pin, but also to the AGND pin to reduce IC supply ripple.
- It is recommended the external components connected to the internal analog control circuitry use a separate ground (AGND) tied to the switching ground (PGND) at only one point. This includes components connected to FREQ, SS, COMP, SYNC and FB.

The TPS55340 comes in a thermally enhanced QFN package. This package includes a thermal pad improving the thermal capabilities. Use thermal vias directly under the TPS55340, providing a path from the exposed thermal pad to ground.

4 Test Results, Layout, and Bill of Materials

Full test results, layout, and bill of materials for this design are found in the TPS55340EVM-147 User's Guide, SLVU742

5 Improvements and Advantages

5.1 Inductor Current Ripple

After designing, building and then testing a SEPIC regulator, you may notice the current ripple waveforms in the coupled windings appear to be closer a sinusoidal waveform and not the ideal saw tooth waveform shown in Figure 7. This is caused by the combination of two properties in a real design. The voltage ripple on C_P across the leakage inductance (L_{LK}) of the coupled inductor. The change in voltage across an inductor induces extra current ripple. In many cases the added current ripple can be very high, contributing to the ripple waveform seen. The additional circulating current also increases power loss reducing efficiency. The effects of the circulating currents are the most visible when operating at the maximum output current where current in the windings is highest.

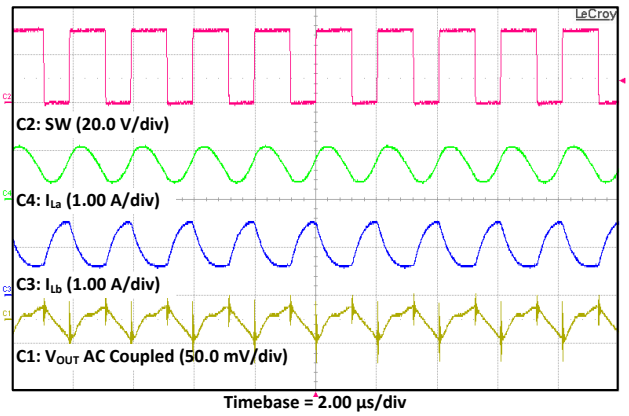

Figure 7. Current Ripple With 2.2µF C_P

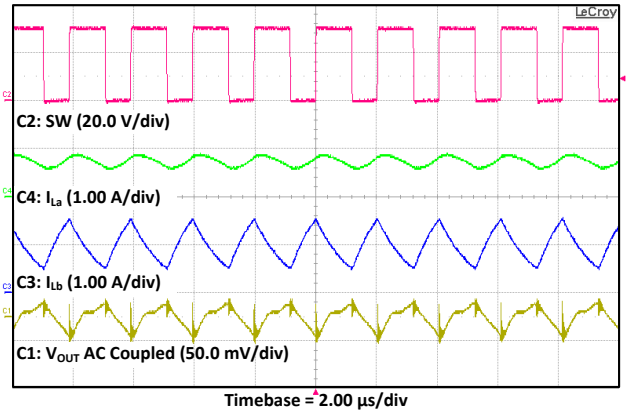

Figure 8. Current Ripple With 20 µF C_P

Based on the source of the extra ripple current, there are two ways to reduce it. Either increase the capacitance of C_P or increase the primary leakage inductance. Adding capacitance has its tradeoffs of increased size and cost. Increasing the leakage inductance may require the use of a custom magnetic component. The decision of how to remove the ripple is up to the designer. Equation 37 and Equation 38 calculate a recommended value for the leakage inductance or C_P capacitance respectively to limit the ripple. Both equations place the induced current ripple of the leakage inductance approximately equal to the magnetizing current ripple ΔI_L. In these calculations it is important to use the estimated derated capacitance for C_P.

$$L_{LK} \geq \frac{I_{OUT} \times L \times D}{C_P \times V_{IN} \times f_{SW}} \quad (37)$$

$$C_P \geq \frac{I_{OUT} \times L \times D}{L_{LK} \times V_{IN} \times f_{SW}} \quad (38)$$

As an example, C_P was increased to reduce the leakage current ripple. The typical primary leakage inductance given for the MSD1260-123ML is 0.28 µH. Using Equation 37 with the minimum input voltage, 9.7 µF of effective capacitance is needed. Two 10-µF, 25-V 1210 X5R ceramic capacitors are used with an approximate derated capacitance of 10.8 µF with the maximum input voltage. Figure 8 shows the new current ripple and illustrates the ripple-current waveform has improved but it can be further improved getting closer to the ideal. Figure 9 compares the efficiency up to the calculated maximum output current with the new capacitor. This shows an increase of up to 1% efficiency at max load.

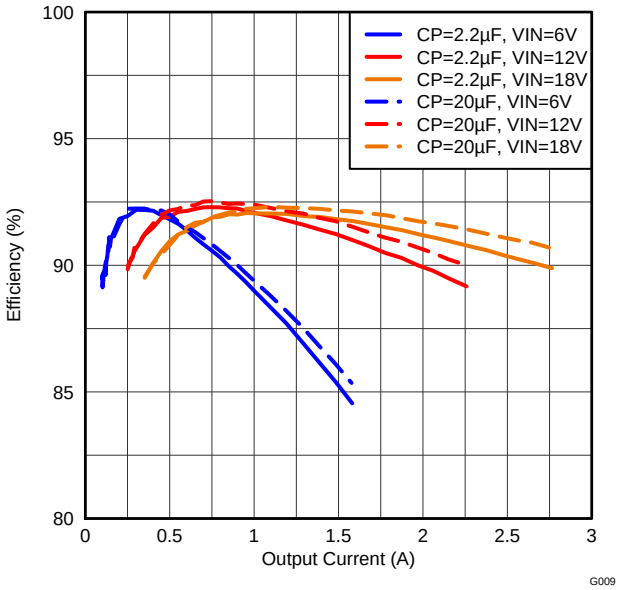

Figure 9. CCM Efficiency Using 2.2 µF and 20 µF C_P

5.2 Comparison of a SEPIC to a Flyback

To show the similarity between a SEPIC and flyback topology, by removing the switching capacitor, C_P, the design is quickly converted into a flyback converter. If needed, this can be used for a quick analysis of the difference between the two topologies. There are two advantages to a SEPIC design. First, the input current is continuous, reducing RMS current stress on the input capacitor. Secondly, the addition of C_P clamps the voltage overshoot and ripple at SW caused by the primary leakage inductance, reducing the stress in the internal MOSFET. This reduces the need for an external RCD clamp and/or RC snubber. A fair and thorough evaluation of the tradeoffs between the two is done in Reference 4. A SEPIC solution is used in isolated applications with the circuit shown in Figure 10.

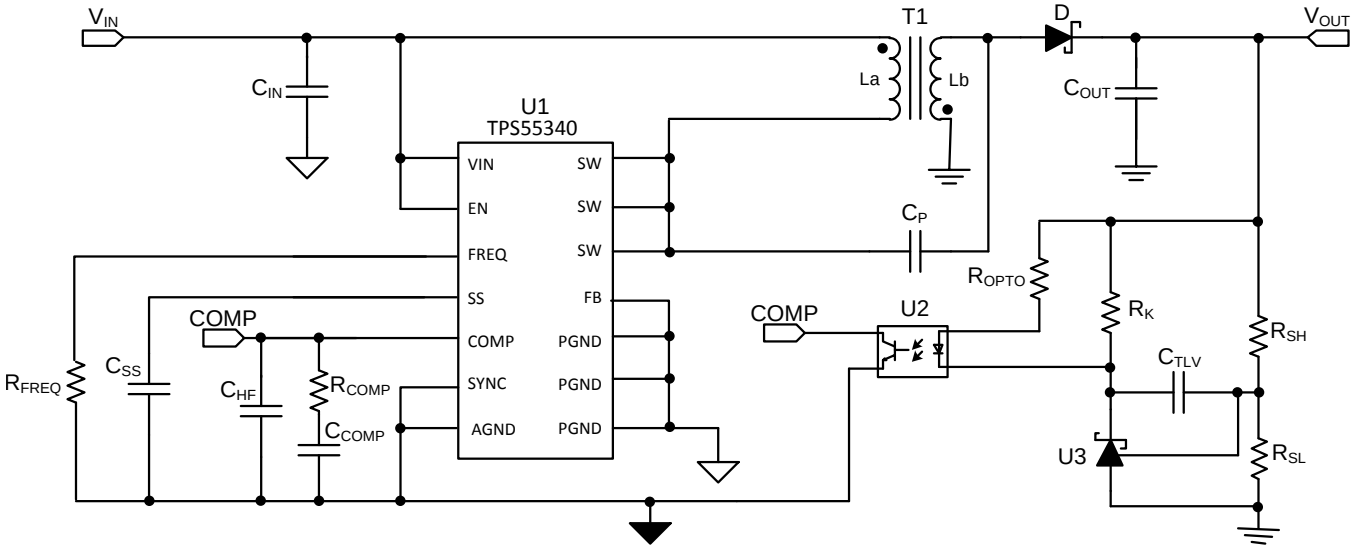

Figure 10. Isolated SEPIC

6 Conclusion

A SEPIC design is a simple, non-isolated option to regulate an output voltage between the minimum and maximum input voltage. Complete test data for this SEPIC design is found in the TPS55340EVM-147 User's Guide (SLVU742). Adding isolation to a SEPIC design in place of an isolated flyback, in certain applications, reduces the stresses on components; namely the input capacitors and the internal MOSFET.

7 References

1. *TPS55340 Data Sheet, Integrated 5-A 40-V Boost/SEPIC/Flyback Regulator* (SLVSBD4)
2. Jeff Falin, *Designing DC/DC converters based on SEPIC Topology* (SLYT309)
3. John Betten, *SEPIC Converter Benefits from Leakage Inductance* http://www.powerpulse.net/techPaper.php?paperID=153
4. John Betten and Robert Kollman, *Guess what: underutilized SEPIC outperforms the flyback topology* http://www.eetimes.com/design/power-management-design/4009575/Guess-what-underutilized-SEPIC-outperforms-the-flyback-topology

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