Application Report
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TPS54xx0-Q1 and TPS57xx0-Q1 Pin Open and Short Test Results

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ABSTRACT

This application note provides Pin Open and Short Test Results for the device pins of the TPS54xx0-Q1 and TPS57xx0-Q1 family of step-down SWIFT™ DC-DC converters. The TPS54xx0-Q1 and TPS57xx0-Q1 family of power devices consists of high-input-voltage step-down regulators that provide a variety of current options.

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1 Introduction

The TPS54xx0-Q1 and TPS57xx0-Q1 family of power devices consists of high-input-voltage, step-down regulators that provide a variety of current options. These devices have integrated high-side MOSFETs and employ current-mode control to provide simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no load, regulated output-supply current to 138 µA or less. Using the enable pin, shutdown supply current is reduced to 1.5 µA or less.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin (EN). The output-voltage start-up ramp is controlled by the slow-start pin (SS/TR) that can also be configured for sequencing and tracking. An open-drain power-good signal indicates the output is within 92% to 109% of the nominal voltage. A wide switching frequency allows for efficiency and external component size to be optimized. Frequency foldback and thermal shutdown protects the device during an overload condition.

The TPS54xx0-Q1 and TPS57xx0-Q1 devices are available in 10-pin thermally enhanced MSOP PowerPAD™ packages (DGQ) and 10-pin SON packages (DRC).

Table 1 lists the devices included in the TPS54xx0-Q1 and TPS57xx0-Q1 family of step-down SWIFT DC-DC converters.

Table 1. Summary of TPS54xx0-Q1 and TPS57xx0-Q1 Family of Step-Down SWIFT DC-DC Converters

DEVICE	INPUT VOLTAGE		OUTPUT CURRENT	PACKAGE OPTIONS
	MIN	MAX		
TPS54140-Q1	3.5 V	42 V	1.5 A	MSOP - DGQ SON - DRC
TPS54160-Q1	3.5 V	60 V	1.5 A	MSOP - DGQ SON - DRC
TPS57140-Q1	3.5 V	42 V	1.5 A	MSOP - DGQ SON - DRC
TPS57160-Q1	3.5 V	60 V	1.5 A	MSOP - DGQ SON - DRC
TPS54240-Q1	3.5 V	42 V	2.5 A	MSOP - DGQ SON - DRC
TPS54260-Q1	3.5 V	60 V	2.5 A	MSOP - DGQ SON - DRC
TPS54040-Q1	3.5 V	42 V	0.5 A	MSOP - DGQ SON - DRC
TPS54060-Q1	3.5 V	60 V	0.5 A	MSOP - DGQ SON - DRC
TPS57040-Q1	3.5 V	42 V	0.5 A	MSOP - DGQ SON - DRC
TPS57060-Q1	3.5 V	60 V	0.5 A	MSOP - DGQ SON - DRC

2 Test Results

This application note provides test results for the device pins of the TPS54xx0-Q1 and TPS57xx0-Q1 family of step-down SWIFT DC-DC converters. The failure conditions covered in this document include typical failure scenarios, such as short-circuit to GND, short-circuit to supply, short-circuit to a neighboring pin, or if the pin is left open. This application note also details how these conditions affect the device. The first effect considered is whether the condition damages the pin in question or the device itself. The second effect considered is whether the device is functional under the condition. Lastly, the analysis includes a comments section that discusses how the particular condition affects the device operation.

NOTE: Values in green indicate normal device operation. Values in red indicate damage to the device.

Table 2. Analysis for Pin Short-Circuit to GND

PIN		SHORT TO GND		
NUMBER	NAME	DAMAGE	FUNCTIONALITY	COMMENTS
1	BOOT	**Yes**	No	Damage the VIN to BOOT path
2	VIN	No	No	No output voltage because the device is off. **No Output**
3	EN	No	No	No output voltage because the device is disabled. **No Output**
4	SS/TR	No	No	No output voltage because the device is disabled. **No Output**
5	RT/CLK	No	No	Very high switching frequency
6	PWRGD	No	**Yes**	Output voltage is present, but communication about status of output voltage is lost. **Normal Operation**
7	VSENSE	**Yes**	No	Max duty cycle so device connected to output can be damaged and pass transistor may be damaged from excessive heat.
8	COMP	No	No	Duty cycle is 0. **No Output**
9	GND	No	**Yes**	Appropriate connection. **Normal Operation**
10	PH	**Yes**	No	Device is protected from overcurrent, but pass transistor may be damaged due to excessive heat. **No Output**

Table 3. Analysis for Pin Left Open

PIN		OPEN		
NUMBER	NAME	DAMAGE	FUNCTIONALITY	COMMENTS
1	BOOT	No	No	No output voltage because Boot capacitor is not charged so pass transistor is always off. **No Output**
2	VIN	**Yes**	No	No output voltage because device is always off. Potential for damage from static. **No Output**
3	EN	No	**Yes**	Output voltage overshoot at power ON and input inrush current. **Normal Operation**
4	SS/TR	No	**Yes**	Output voltage overshoot at power ON and input inrush current. **Normal Operation**
5	RT/CLK	No	No	Very low switching frequency
6	PWRGD	No	**Yes**	Output voltage is present, but communication about status of output voltage is lost. **Normal Operation**
7	VSENSE	**Yes**	No	No predicted duty cycle and potential of damage from static. **Unregulated Output**
8	COMP	No	No	Potential for unstable output due to lack of compensation. **Unstable operation**
9	GND	No	No	No output voltage because device is off. **No Output**
10	PH	No	No	No output voltage because PH pin is disconnected from output LC filter. **No Output**

Table 4. Analysis for Pin Short-Circuit to Supply Voltage

PIN		SHORT TO SUPPLY		
NUMBER	NAME	DAMAGE	FUNCTIONALITY	COMMENTS
1	BOOT	Yes	No	Damage the internal BOOT-PH ESD cell and potential damage to bond wire of PH pin depending on the voltage. **Massive Destruction**
2	VIN	No	Yes	Appropriate Connection. **Normal Operation**
3	EN	Yes	No	**Violation of absolute maximum voltage rating on EN pin if supply voltage greater than 5 V**
4	SS/TR	Yes	No	**Violation of absolute maximum voltage rating on SS/TR pin if supply voltage greater than 3 V**
5	RT/CLK	Yes	No	**Violation of absolute maximum voltage rating on RT/CLK pin if supply voltage greater than 3.6 V**
6	PWRGD	Yes	No	**Violation of absolute maximum voltage rating on PWRGD pin if supply voltage greater than 6 V**
7	VSENSE	Yes	No	**Violation of absolute maximum voltage rating on VSENSE pin if supply voltage greater than 3 V**
8	COMP	Yes	No	**Violation of absolute maximum voltage rating on COMP pin if supply voltage greater than 3 V**
9	GND	No	No	Supply shorted to GND. **No Operation**
10	PH	Yes	No	**Potential damage to device connected to output due to short between supply and PH.**

Table 5. Analysis for Pin Short-Circuit to Neighboring Pin

PIN		SHORT TO NEIGHBORING PIN		
NUMBER	NAME	DAMAGE	FUNCTIONALITY	COMMENTS[1]
1	BOOT	Yes	No	(1-2) Damage the internal BOOT-PH ESD cell and potential damage to bond wire of PH pin depending on the voltage. **Massive Destruction**
2	VIN	Yes	No	(2-3) **Violation of absolute maximum voltage rating on EN pin if supply voltage greater than 5 V**
3	EN	No	Yes	(3-4) SS/TR functionality will be altered which could result in faster start-up time than desired.
4	SS/TR	No	No	(4-5) Switching frequency is corrupted and SS/TR functionality is lost.
5	RT/CLK	N/A	N/A	(5-6) N/A as pins are on opposite sides of the package
6	PWRGD	No	No	(6-7) PWRGD pin is low at power-up, so VSENSE is driven low and stays low. **No switching and output voltage is 0 V.**
7	VSENSE	No	No	(7-8) Error amplifier output connected to VSENSE will cause the output to become unregulated upon any change in load. **Unregulated output**
8	COMP	No	No	(8-9) Duty cycle is 0. **No Output**
9	GND	Yes	No	(9-10) Device is protected from over current but pass transistor may be damaged from heat
10	PH	N/A	N/A	(10-1) N/A as pins are on opposite sides of the package

(1) The numbers in parentheses indicate the two pins that are being considered.

Revision History

Changes from A Revision (November 2013) to B Revision **Page**

- Changed document title and Pin FMEA to test results throughout document 1
- Deleted Pin FMEA from table titles 3
- Changed Table 5 title to Neighboring Pin 4

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2013) to A Revision **Page**

- Added note to Pin FMEA section to identify meaning of colors used in the tables 3

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