Application Report

How Single Pulse Mode in Boost Converter Saves the Output Capacitor

ABSTRACT

The power-save mode is a common feature for most DC-DC converters, which saves power and improve the efficiency at light load condition. There are many control schemes to control the behaviors in power save mode.

The majority of power save mode control schemes introduce a high output ripple because most of the internal circuits are disabled under light load, including the error amplifier. Only a low power voltage reference and voltage comparator are active which monitors the output voltage. The device starts switching once the output voltage drops below the target threshold. Such control schemes are not friendly to some noise sensitive sub-systems. Otherwise, more capacitors should be added to keep the output quiet.

In this application, a single pulse mode power save mode is introduced which achieves very low output ripple and can support small output capacitors. TI's new TPS613221A low quiescent-current boost converter is used as the example.

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Trademarks

1 Traditional Power-Save Mode Control Scheme

The traditional power-save mode use a low power voltage comparator to enable and disable the control loop under light load. When the output voltage reaches the target value, all the internal blocks will be disabled except the voltage comparator and reference voltage. It is fundamentally a burst-mode-control topology. In systems whose output load is at the boundary of power save mode and normal PWM mode, the device can turn on and off the control loop a number of times. To minimize the probability of the device switch between these two modes, a high hysteresis is added. Then DC output voltage is higher than the nominal value in such kind of control schemes. Typically, the DC voltage in power save mode is 0.5% to 3% higher than the nominal value. Take the TPS61021A as the example, Figure 1-1 is the typical operation behaviors of TPS61021A at light load.

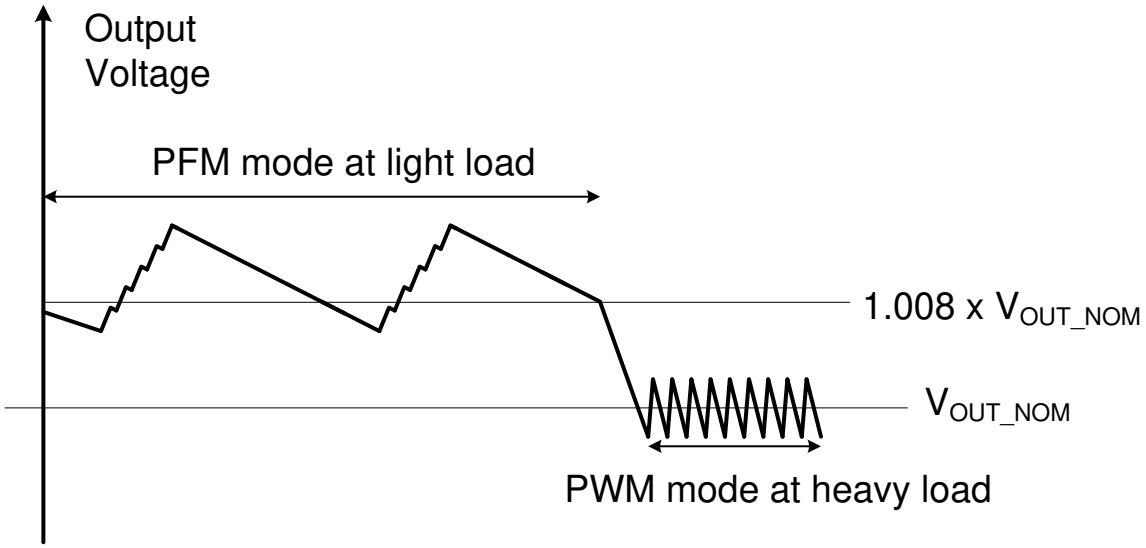

Figure 1-1. Traditional Power Save Mode Control Scheme

When the output load decreases, the error amplifier output is clamped at a certain level. Then the output voltage increases and the devices enters power save mode. During the switching period, the control loop is active and continue to output switching signals until the output voltage hits the PFM reference voltage (0.8% percent higher than the nominal voltage). Then the control loop commands the device stopping switching but actually the device will continue to switch for some cycles because of the internal comparator delay. After that, the device stops switching finally. During the non-switching period, the load is supplied by the output capacitor and the output voltage declines. When the FB voltage drops below the PFM reference voltage, the device starts switching again to ramp up the output voltage after some delay time of the comparator,.

This control scheme is very simple and effective, but it introduces high output ripple because of the multiple switching pulses in one power save mode cycle.

2 Single Pulse Power Save Mode Control Scheme

The TPS61322xx is a low quiescent, high efficiency synchronous boost converter family based on hysteretic current control topology. The TPS61322xx is designed for systems which need a constant on and quiet power rail. The input source can be one cell alkaline battery, CR2032, and lithium battery. Figure 2-1 shows the typical application schematic of TPS61322xx.

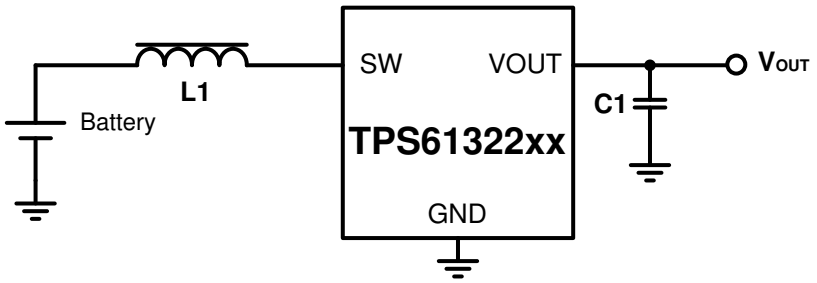

Figure 2-1. Single Pulse Control Scheme

The TPS61322xx uses single pulse power save mode and keeps the output voltage the same over all the load range. The typical control scheme is shown in Figure 2-2

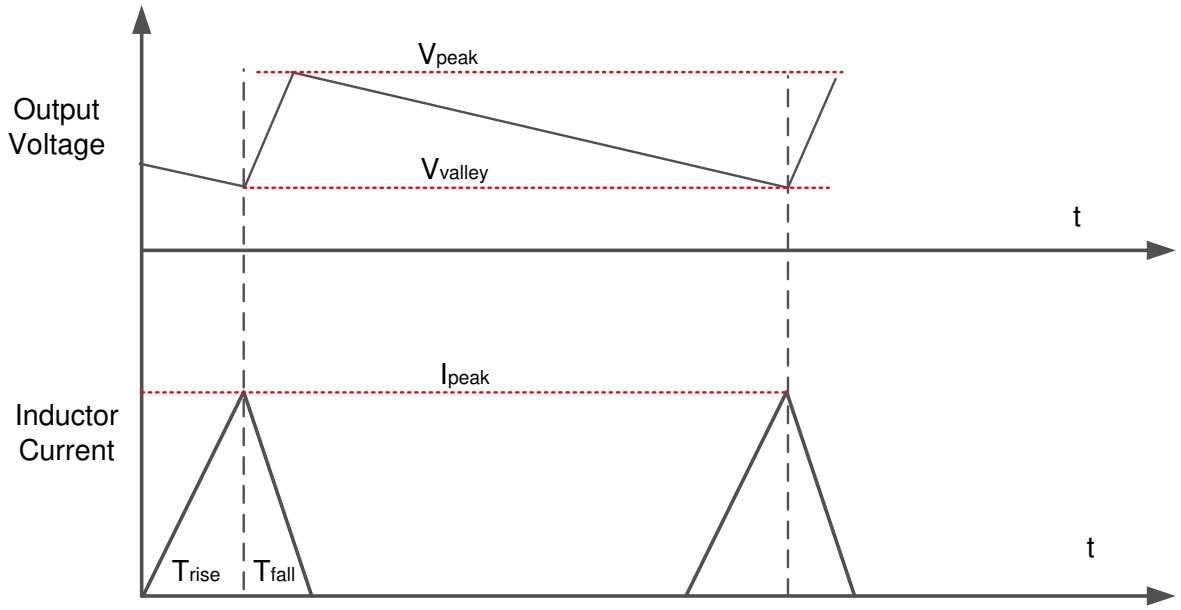

Figure 2-2. Single Pulse Control Scheme

There are 3 operation subintervals for TPS61322xx at light load: on-phase, off-phase and stop-phase. During on-phase, the low-side MOSFET is ON and high-side MOFET is OFF, the input source charges the inductor and the subsystem is powered by the output capacitor. The inductor current ramps up until triggers the hysteresis current I_{hys}, then the on-phase ends and the off-phases starts. During off-phase, the low-side MOSFET is OFF and high-side MOSFET is ON. The inductor charges the output capacitor and powers the sub-system at the same time. The inductor current ramps down until trigger zero current, then the stop-phase starts. During stop-phase, both low-side and high-side MOSFET are OFF and all the energy is from the output capacitor. The internal control loop is always active and regulate the stop-phase time.

This control scheme helps reduce the output capacitor significantly because only one current pulse is output in each power save mode cycle.

3 Output Ripple Calculation

The TPS613221A, a 3.3-V version from TPS61322xx family is used as the example.

To simplify the calculation, there is no load at the output of TPS613221A, and the efficiency is 100%. All the input energy on the inductor will be discharged to the output capacitor. From the power balance point, the energy discharged to the output capacitor is shown in Equation 1:

$$V_{IN} \times I_{IN} \times T = \frac{1}{2} \times C \times ({V_{peak}}^2 - {V_{valley}}^2) = C \times V_{OUT} \times \Delta V \tag{1}$$

where

$$\Delta V = V_{peak} - V_{valley}$$

$$I_{IN} = \frac{1}{2} \times I_{peak}$$

The peak inductor current at light load is calculated according to the Equation 2:

$$I_{peak} = I_{hys} + \frac{V_{IN}}{L} \times t_{delay} \tag{2}$$

where

- L is the power inductor inductance
- I_{hys} is 80 mA typically
- t_{delay} is 120 ns typically

The inductor current pulse period is calculated according to Equation 2:

$$T = T_{rise} + T_{fall} \tag{3}$$

where

$$T_{fall} = \frac{I_{peak}}{V_{OUT} - V_{IN}} \times L$$

$$T_{rise} = \frac{I_{hys}}{V_{IN}} \times L + t_{delay}$$

Finally, the output ripple will be a little higher because of the ESR in the output capacitor, which can be calculated as follow:

$$V_{Ripple} = \Delta V + ESR \times I_{peak} \tag{4}$$

where

- ESR is the equivalent series resistance of the output capacitor.

When the input voltage is 1.8 V, the peak inductor current will be 200 mA according to the previous equations. The output ripple is 7.6 mV (ΔV = 6 mV, ESR × I_{peak} is 1.6 mV) when using a 10-µF output capacitor with 8-mΩ ESR.

4 Bench Result

Different output capacitors are used to verify the single pulse power-save mode.

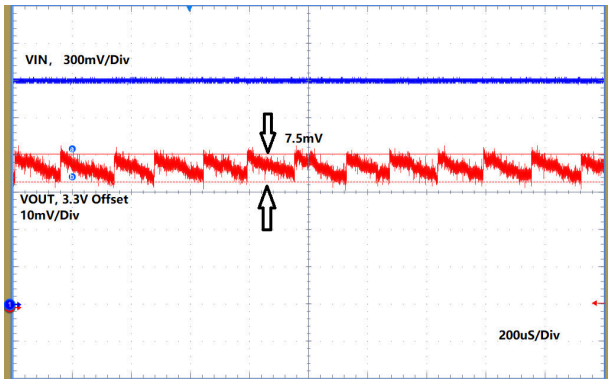

Figure 4-1. V_{IN} = 1.8 V, C_{OUT} = 10 µF

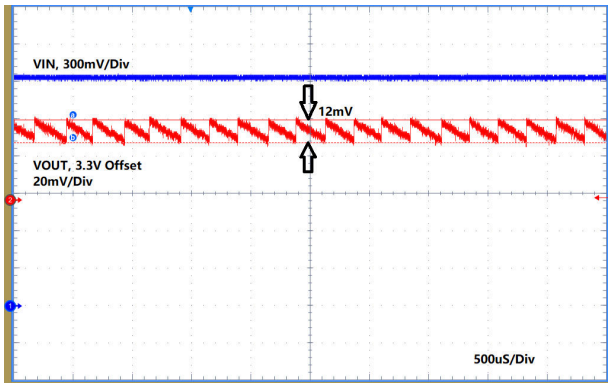

Figure 4-2. V_{IN} = 1.8 V, C_{OUT} = 4.7 µF

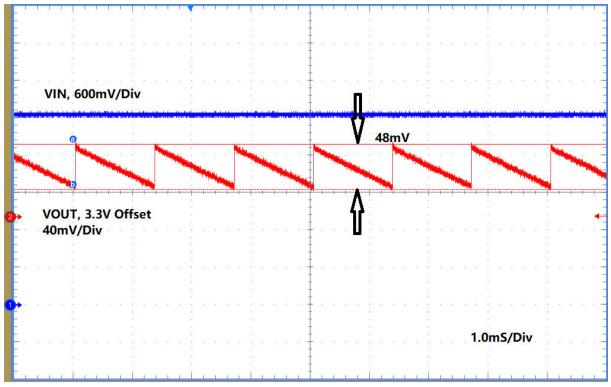

Figure 4-3. V_{IN} = 3 V, C_{OUT} = 10 µF

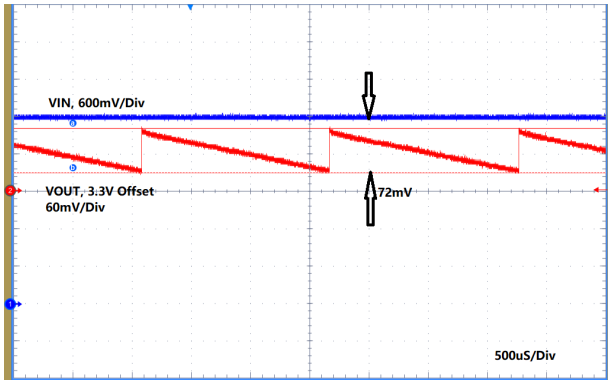

Figure 4-4. V_{IN} = 3 V, C_{OUT} = 4.7 µF

Table 4-1. Output Ripple

VIN	LOAD	C1 = 4.7 µF	C1 = 10 µF
3 V	100 µA	71.58	48.52
	1 mA	71.58	48.52
	10 mA	29.79	18.26
1.8 V	100 µA	12.26	7.53
	1 mA	11.86	7.53
	10 mA	20.26	11.33
0.9 V	100 µA	7.86	7.53
	1 mA	7.86	7.53
	10 mA	46.92	23.46

From the typical application curves and the output ripple values listed in the table, the output ripple of TPS613221A is 7.5 mV and 48.5 mV when the output capacitor is 10 µF (The actual output capacitance is 7 µF under 3.3-V bias voltage). While it increases to 12 mV and 72 mV if the output capacitor is modified to 4.7 µF (the actual capacitance is 3.6 µF under 3.3-V bias voltage)

As the comparison, the traditional power save mode introduces more than 0.8% × V_{OUT} output ripple. It is much higher than the single-pulse, power-save-mode control method if the TPS61021A has all the same output capacitance, inductance and internal comparator delay time as that of TPS613221A. Another one or two pulses will be introduced even the output voltage triggers the 1.008 × V_{OUT} threshold. That means the output ripple can reaches 34 mV or more when the output voltage is 10uF. This becomes even worse when the input voltage is 3

V because a single pulse introduces 48-mV output ripple. That means for some cycles, the output ripple can be as high as 83 mV.

5 Conclusion

Various sub-systems, such as the ADC, which is sensitive to the power rail ripple, require a small output ripple from the DC/DC converters. The single pulse mode helps keep the output ripple small and not increase the output capacitors at the same time. This control schemes overcome many issues caused by noise, give rise to a robust system performance.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2018) to Revision A (July 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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