Application Report
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How to Pass MFi VBUS Spec with USB Charger TPS2583x-Q1 and TPS2584x-Q1

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ABSTRACT

The TPS2583x-Q1 and TPS2584x-Q1 is the USB Type-C charging controller which is widely used in the automotive USB charging application. In such an application, there usually is a long cable or PCB trace between the charging controller and the USB port. It causes a voltage drop along with the load current increase. The TPS2583X-Q1 and TPS2584x-Q1 have the cable compensation that can solve this problem with a max 1.8 V voltage compensation on the USB port, but MFi has a maximum voltage restriction on the USB voltage, thus the design cannot compensate too much to the VBUS.

This application report introduces the implementation of cable compensation design for MFi certification. It also has a calculation tool that can be used to determine the RSNS, RSET, and RIMON with a given condition for a desired VBUS accuracy design.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. Cable droop compensation linearly increases the voltage at the CSN/OUT pin of the TPS2583x-Q1 as load current increases with the objective of maintaining the USB port voltage at 5 V, regardless of load conditions. Most portable devices charge at maximum current when 5 V is present at the USB connector. For the MFi requirement, it needs the non-Lightning accessories to support a minimum of a 4.97 V output voltage at 2.1 A load. Table 1 shows the USB charger output voltage regulation pass/fail criteria from MFi.

Table 1. Power Supply Voltage Outputs for non-Lightning Accessories

SUPPLY RATING	MINIMUM OUTPUT	MAXIMUM OUTPUT
1 A	4.90 V	5.25 V
2.1 A delivering up to 1.0 A	4.90 V	5.25 V
2.1 A delivering 1.0 to 2.1 A	4.97 V	5.25 V
2.4 A delivering 1.0 to 2.4 A	4.97 V	5.25 V

Through Table 1, you can see that the VBUS voltage range is very tight, especially for the 2.4 A power delivering design. In the automotive USB car charger application, you encounter several resistor drops with a remote USB connector location. Figure 1 gives an example of the charging path resistance.

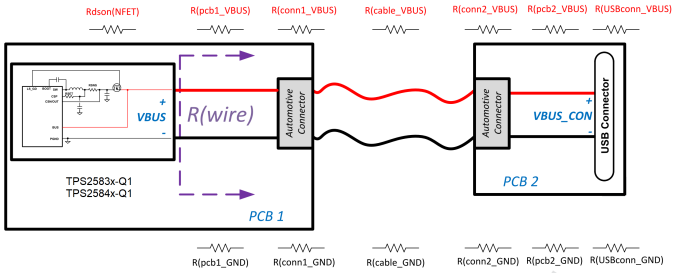

Figure 1. USB Resistances

The TPS2583x-Q1 and TPS2584x-Q1 can detect the load current and increase the voltage at the CSN/OUT pin to compensate for the IR drop in the charging path. To pass the MFi certification, the max cable compensation voltage at 2.4 A must be designed carefully because the variation from the compensation circuit must be taken into account when estimating the USB connector side or far-end VBUS accuracy.

In general, the far-end USB voltage accuracy is determined by DC/DC output voltage regulation accuracy, variation from the external components which compose the cable compensation circuit, variation from the wire or charging path resistances, and the cable compensation circuit inherent accuracy. For the TPS2583x-Q1 and TPS2584x-Q1, the DC/DC voltage regulation accuracy is ±1%. For MFi VBUS accuracy estimation, you can assume the wire resistance is constant since the MFi certification is under 25°C environment. Section 2 introduces the cable compensation theory and deduces the equation for cable compensation voltage design.

2 Cable Compensation Circuit

Figure 2 shows the cable compensation internal circuit.

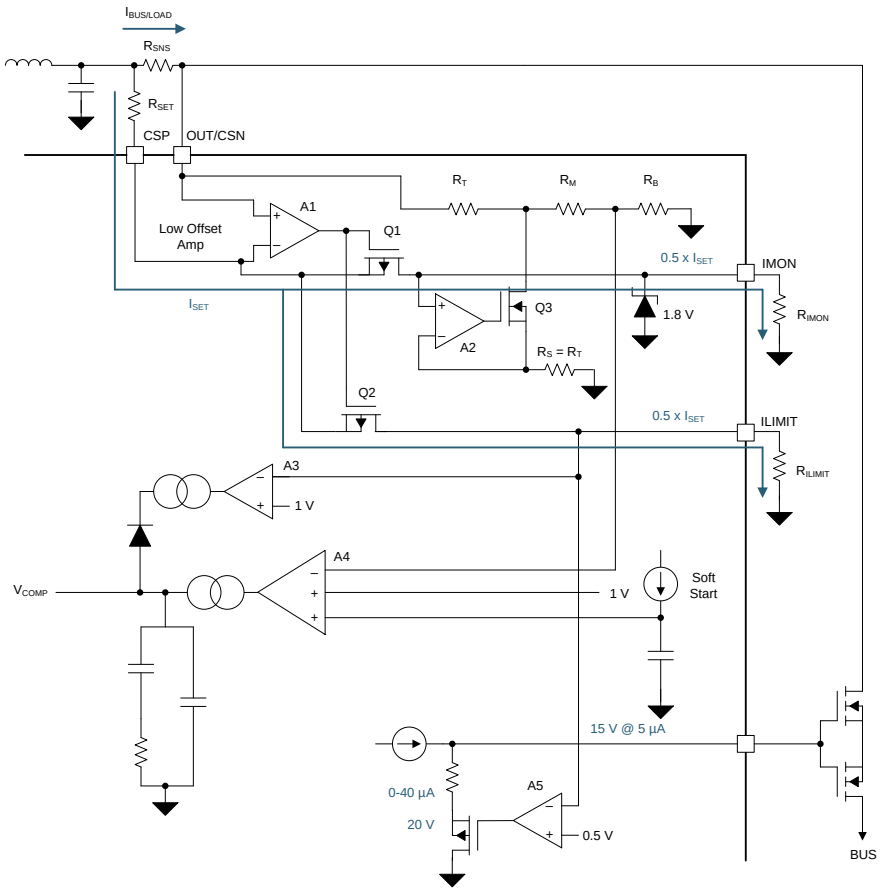

Figure 2. Cable Compensation Circuit

The I_{LOAD} passes the R_{SNS} and causes a voltage drop across the sense resistor, according to the op amp fundamental characteristic. The voltage across the R_{SET} is equal to the voltage drop on the R_{SNS}. The current that passes the R_{SET} can be calculated by Equation 1:

$$ISET = RSNS \times ILOAD / RSET \quad (1)$$

Choose an RSET value to produce an ISET current between 75 µA to 180 µA at the desired IOUT(MAX). Limit the ISET current below 200 µA to avoid saturating the internal amplifier circuit. The recommended voltage across RSNS should approach 50 mV at max load. The current mirror halves the ISET current. RIMON in conjunction with the 0.5 × ISET current produces a voltage on the IMON pin which is proportional to the load current flowing in RSNS. The voltage on the IMON can be calculated by Equation 2:

$$VIMON = (ISET / 2) \times RIMON = RSNS \times ILOAD \times RIMON / (2 \times RSET) \quad (2)$$

The op amp A2 non-inverting input connects to the IMON pin internally. According to the op amp fundamental characteristic, the A2 inverting input voltage is the same as the non-inverting input, so the voltage applied on the Rs is VIMON. This voltage forces a current flow into the Q3, and this current is in proportion to the IMON pin voltage. Since some current flows into the Q3, the voltage on the FB resistor RB decreases, then the op amp A4 tries to increase the DC/DC output voltage to compensate this voltage drop. OUT/CSN voltage is increased until the voltage on the feedback resistor is back to its previous value, which near 1 V. Since the internal resistor R_S is equal to the resistor R_T, the voltage increment on the OUT/CSN pin is the same as the IMON pin voltage, so the cable compensation voltage as Equation 3:

$$VCOMP = RSNS \times ILOAD \times RIMON / (2 \times RSET) \quad (3)$$

RIMON can be deduced by Equation 4:

$$RIMON = VCOMP \times 2 \times RSET / (ILOAD \times RSNS) \quad (4)$$

The previous equation indicates that the cable compensation voltage error is related to the external components RSNS, RIMON, and RSET. Besides the resistor variation, you still need to consider the error from the cable compensation circuit, including the op amp gain error, offset error, and others. Table 2 shows the cable compensation circuit error from the TPS2583x-Q1 datasheet.

Table 2. Cable Compensation Circuit Accuracy

CABLE COMPENSATION VOLTAGE						
V_{IMON}	Cable compensation voltage	(V_{CSP} - V_{CSN}) = 46 mV, R_{SET}= 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ	0.935	1	1.065	V
V_{IMON}	Cable compensation voltage	(V_{CSP} - V_{CSN}) = 26 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ	0.435	0.5	0.565	V

According to Table 2, the error from the compensation circuit is ±6.5% when the voltage across the RSNS is 46 mV, and the error enlarges to ±13% if the voltage across the RSNS drop to 23 mV. TI recommends choosing the larger RSNS, which has an approximate 50 mV voltage drop under desired maximum output current.

3 VBUS Accuracy Estimation for MFi Certification

As described in Section 1, the far-end VBUS accuracy can be estimated by Equation 5 and Equation 6:

$$(VBUS\_min - VBUS\_typ) / VBUS\_typ \quad (5)$$

and

$$(VBUS\_max - VBUS\_typ) / VBUS\_typ \quad (6)$$

The VBUS_min, VBUS_typ, and VBUS_max can be calculated from Equation 7, Equation 8, and Equation 9:

$$VBUS\_typ = VOUT\_typ + VCOMP\_typ - VDROP\_typ \quad (7)$$
$$VBUS\_min = VOUT\_min + VCOMP\_min - VDROP\_max \quad (8)$$
$$VBUS\_max = VOUT\_max + VCOMP\_max - VDROP\_min \quad (9)$$

To pass the MFi VBUS spec, the design needs to guarantee the VBUS_min is above 4.97 V and the VBUS_max is below 5.25 V under the 2.4 A load.

For VOUT_min and VOUT_max, it can be calculated with the DC/DC nominal output voltage and regulation accuracy VOUT_acc, as Equation 10 and Equation 11:

$$VOUT\_min = VOUT\_typ \times (1 - VOUT\_acc) \quad (10)$$

$$VOUT\_max = VOUT\_typ \times (1 + VOUT\_acc) \quad (11)$$

For the VCOMP_min and VCOMP_max, you need to consider the external resistor variations and the cable compensation circuit accuracy VIMON_acc as previously discussed. The minimum and maximum value can be calculated by Equation 12 and Equation 13:

$$VCOMP\_min = RSNS\_min \times ILOAD\_min \times RIMON\_min / 2 \times RSET\_max \times (1 - VIMON\_acc) \quad (12)$$

$$VCOMP\_max = RSNS\_max \times ILOAD\_max \times RIMON\_max / 2 \times RSET\_min \times (1 + VIMON\_acc) \quad (13)$$

The voltage drop across the wire under 2.4 A testing load can be calculated by Equation 14 and Equation 15:

$$VDROP\_min = ILOAD\_min \times Rtrace\_min \quad (14)$$

$$VDROP\_max = ILOAD\_max \times Rtrace\_max \quad (15)$$

4 Design Example

To start a design, the first step is to determine the resistence between the TPS2583x-Q1 CSN/OUT and USB connector. The USB connector is the far-end, while CSN/OUT is the near-end. The resistences Rtrace between the chip and USB connector include the RSNS, MOSFET RDSON, wire, and PCB routing resistence. The following equations take 200 mΩ as an example.

1. VDROP_typ = ILOAD_typ × Rtrace_typ = 2.4 A × 200 mΩ = 480 mV
   In the TPS2583x-Q1 and TPS2584x-Q1 cable compensation calculation tool, it can choose the trace resistance variation by choosing the minimum and maximum ambient temperature.
2. Assume Rtrace is constant since the MFi certification testing is under 25°C. Also assume ILOAD is stable and has no variation, that is ILOAD_min = ILOAD_max = ILOAD_typ = 2.4 A, so VDROP_max = VDROP_min = VDROP_typ = 480 mV.
3. Choose RSNS = 15 mΩ since RSNS is the current sense resistor. The recommended voltage across RSNS under current limit should be approximately 50 mV. Assume the desired current limit is 3.3 A for a 3 A Type-C charging port design, so RSNS = 50 mV / 3.3 A ≈ 15 mΩ.
4. Choose RSET = 300 Ω since RSET determines the input current to the transconductance amplifier and current mirror, and the recommended ISET current is 70 µA ~180 µA at the desired maximum IBUS.
5. VCOMP = VDROP = 480 mV since the compensation voltage is equal to the voltage drop which cause by cable resistences Rtrace.
6. RIMON = VCOMP × 2 × RSET / (RSNS × ILOAD) = 480 mV × 2 × 300 Ω / (15 mΩ × 2.4 A) = 8 KΩ
7. Assume the resistor accuracy is ±1%, that is RSNS_min/max = 15 mΩ × (1 ± 1%), RIMON_min/max = 8 KΩ × (1 ± 1%), and RSET = 300 Ω × (1 ± 1%).
8. VCOMP_min = 15 mΩ × 99% × 2.4A × 8 KΩ × 99% / (2 × 300 Ω × 101%) × 93.5% ≈ 435.5 mV.
   Choose VIMON_acc = ±6.5% according to the Equation 14.
   VCOMP_max = 15 mΩ × 101% × 2.4 A × 8 KΩ × 101% / (2 × 300 Ω × 99%) × 106.5% ≈ 526.74 mV
9. VBUS_min = 5.1V × 99% + 435.5 mV - 480 mV ≈ 5.005 V
   VBUS_max = 5.1 V × 101% + 526.74 mV - 480 mV ≈ 5.198 V

Since the VBUS minimum and maximum voltage drop into the 4.97 V to 5.25 V range, this design meets the MFi VBUS spec. Figure 3 shows the TPS2583x-Q1 CSN/OUT pin voltage and the USB connector side VBUS. The VBUS keeps flat along with the load current increase, and falls into the MFi spec limits.

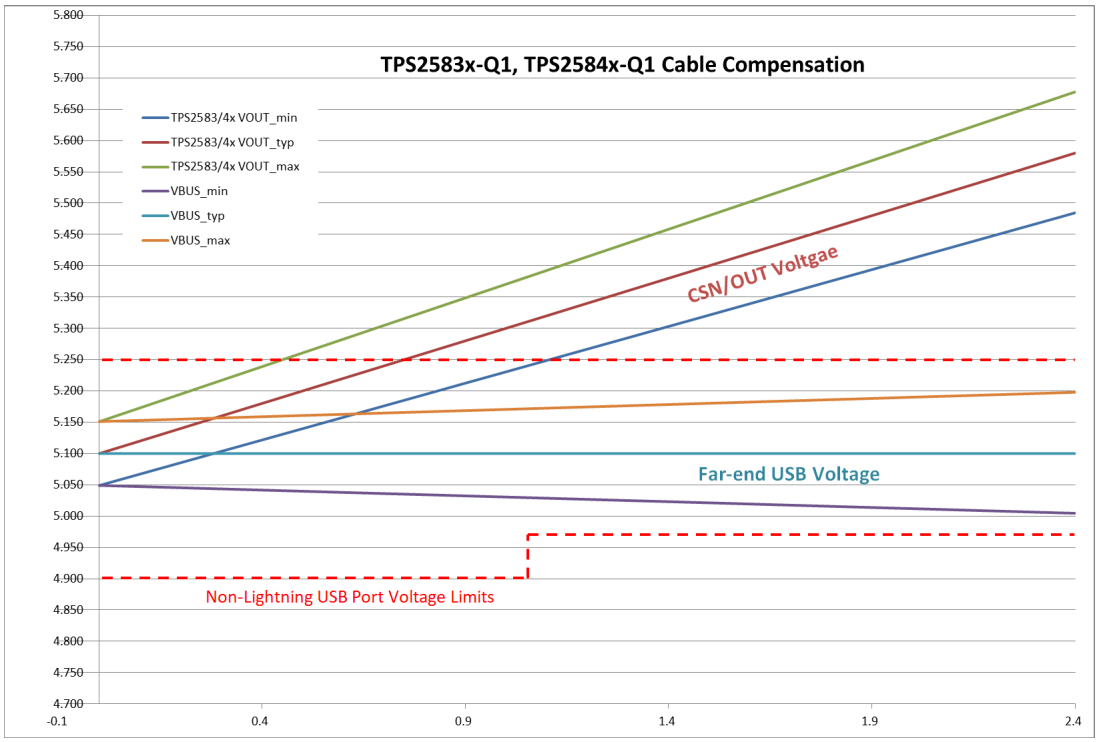

Figure 3. TPS2583x-Q1 Far-end USB Voltage

5 Summary

Cable compensation was introduced to satisfy the market requirement of USB2.0 and USB3.0 compliance VBUS voltage at USB connector side. For MFi certification, it has stricter requirements on the connector side USB voltage. Using the cable compensation function with a more careful design, the TPS2583x-Q1 and TPS2584x-Q1 can meet the MFi VBUS spec. This application report introduces where the variation of the USB port voltage comes from and analyzes its accuracy, which helps estimate the whether the design is compliant with the MFi VBUS requirement.

6 References

- *TPS2583x-Q1, USB Type-C and BC1.2 5-V 3.5-A Output, 36-V Input Synchronous Step-Down DC/DC Regulator with Cable Compensation Datasheet*
- TPS2583x and TPS2584x Far-end VBUS accuracy calculation with cable compensation

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