Functional Safety Information

TPS4H160-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS4H160-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

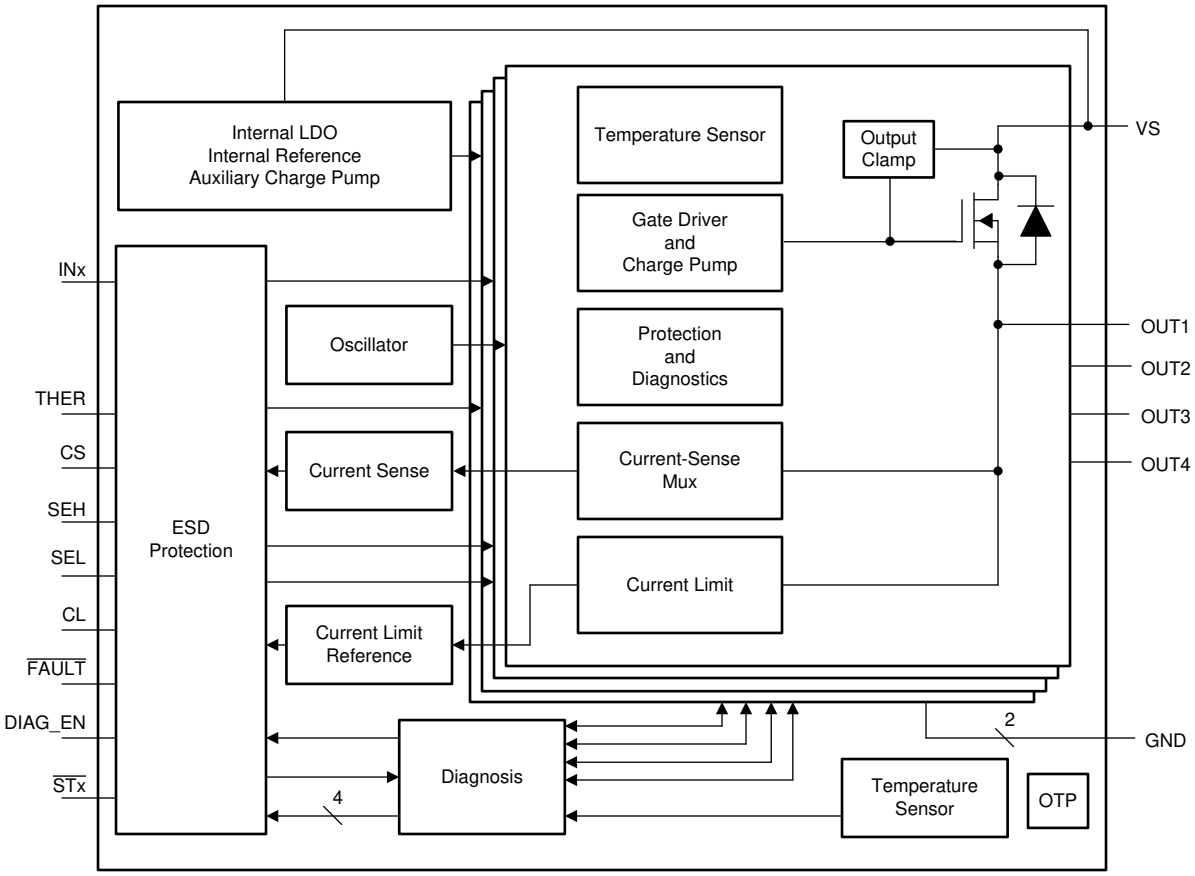

Figure 1-1. Functional Block Diagram

TPS4H160-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS4H160-Q1 based on an industry-wide used reliability standard:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	25
Die FIT Rate	6
Package FIT Rate	19

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS4H160-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT1,2,3,4 open (HiZ)	20%
OUT1,2,3,4 stuck on (VS)	10%
OUT1,2,3,4 not in specification voltage or timing	45%
Diagnostics not in specification	10%
Protection functions fails to trip	10%
Pin to pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS4H160-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS4H160-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS4H160-Q1 data sheet.

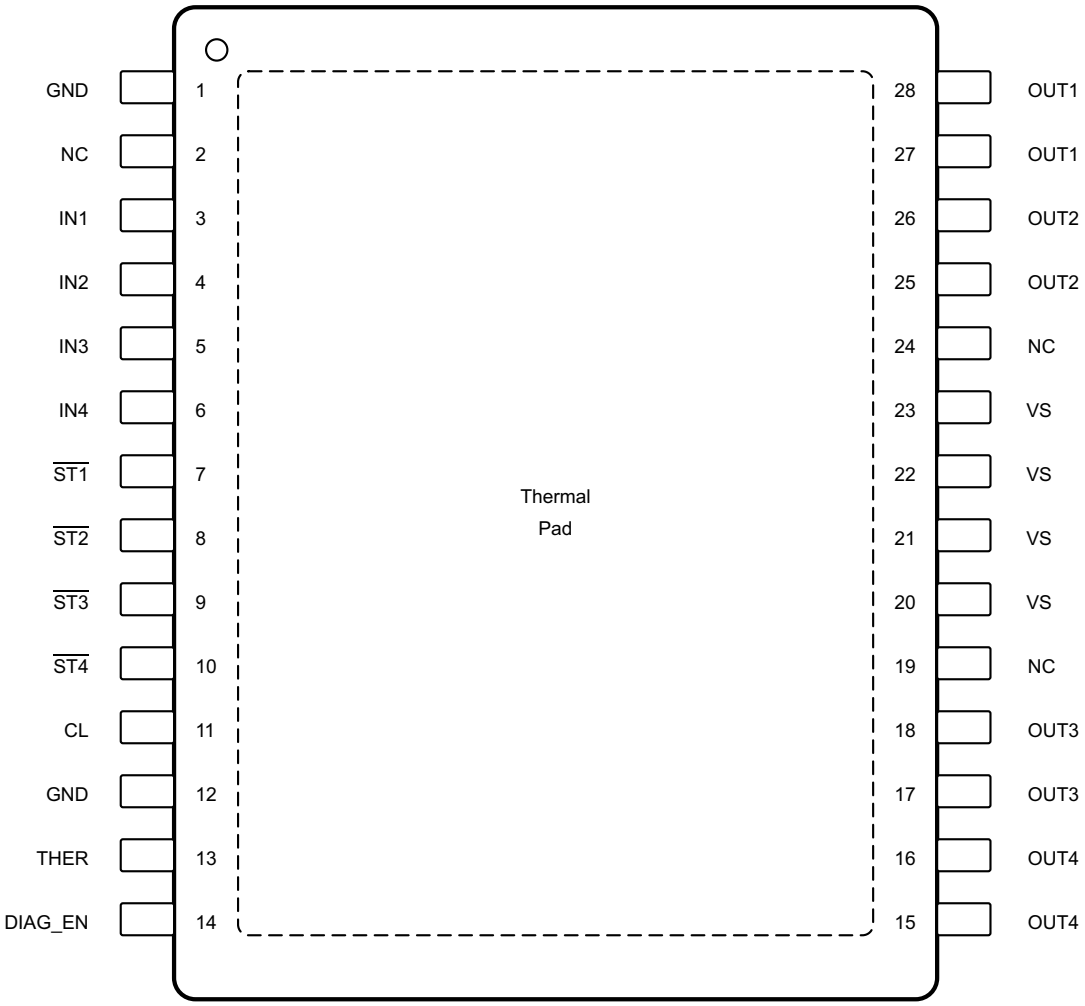

Figure 4-1. Pin Diagram (Version A)

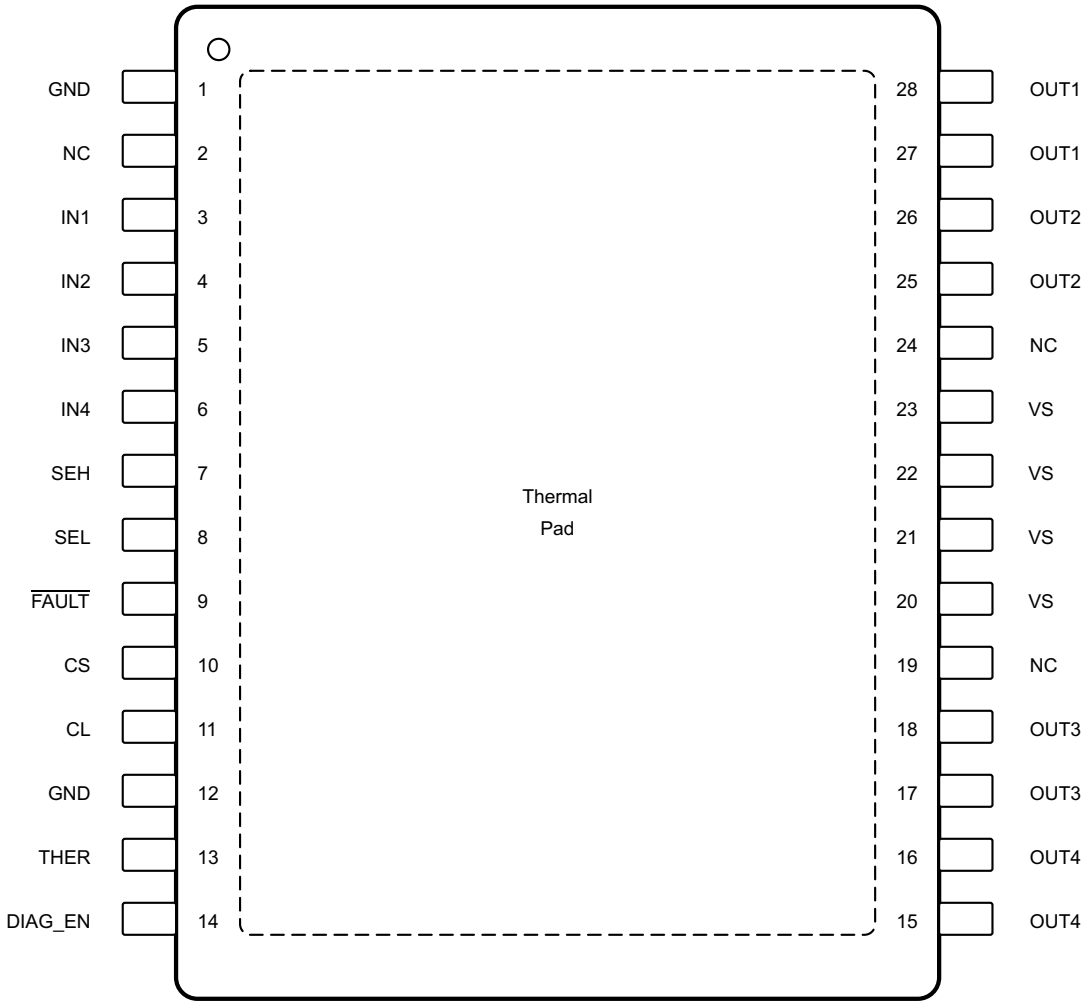

Figure 4-2. Pin Diagram (Version B)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follows data sheet recommendation for operating conditions, external components selection and PCB layout.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1, 12	Resistor/diode network will be bypassed if present.	B
NC	2, 19, 24	No effect.	D
INx	3, 4, 5, 6	Shutdown of corresponding channel.	B
$\overline{\text{STx}}$	7, 8, 9, 10	Version A only. Status being reported may be erroneous.	B
SEH	7	Version B only. If DIAG_EN is high then only channel 3 or 4's (depending on SEL) sense current output will be on SNS pin.	B
SEL	8	Version B only. If DIAG_EN is high then only channel 1 or 2's (depending on SEH) sense current output will be on SNS pin.	B
$\overline{\text{FAULT}}$	9	Version B only. Status being reported may be erroneous.	
CS	10	Version B only. Sense current not valid from CS pin.	B
CL	11	Device will default to internal current limit.	C
THER	13	Device will default to "auto-retry" mode when encountering thermal fault.	B
DIAG_EN	14	Diagnostics will be disabled.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUTx	15,16,17, 18, 25, 26, 27, 28	Current limit of device will engage.	B
VS	20, 21, 22, 23	Device will have no input supply and therefore not function.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1, 12	Loss of ground detection engages and device shuts off.	B
NC	2, 19, 24	No effect.	D
INx	3, 4, 5, 6	Corresponding channel will be shutdown and INx will be pulled down internally.	B
$\overline{\text{STx}}$	7, 8, 9, 10	Version A only. $\overline{\text{STx}}$ pin cannot pull high and diagnostics cannot be reported.	B
SEH	7	Version B only. Pulled low internally, however wrong SNS current potentially reported on CS if DIAG_EN is high.	B
SEL	8	Version B only. If DIAG_EN is high then only channel 1 or 2's (depending on SEH) sense current output will be on SNS pin.	B
$\overline{\text{FAULT}}$	9	Version B only. Fault signal not reported.	B
CS	10	Version B only. Correct sense current cannot be read.	B
CL	11	Device will default to internal current limit.	C
THER	13	Internally pulled down. Device will default to "auto-retry" mode when encountering thermal fault.	B
DIAG_EN	14	Internally pulled down. Diagnostics will be disabled.	B
OUTx	15, 16, 17, 18, 25, 26, 27, 28	No effect. If configured, open load detection will trigger.	B
VS	20, 21, 22, 23	Device will have no input supply and therefore not function.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	NC	No effect.	D
NC	2	IN1	No effect.	D
IN1	3	IN2	IN1 signal will affect IN2 signal and vice versa.	B
IN2	4	IN3	IN2 signal will affect IN3 signal and vice versa.	B
IN3	5	IN4	IN3 signal will affect IN4 signal and vice versa.	B
IN4	6	ST1	Version A only. If ST1 is high then channel 4 will be on.	B
IN4	6	SEH	Version B only. IN4 signal will affect SEH and vice versa.	B
$\overline{\text{ST1}}$	7	$\overline{\text{ST2}}$	Version A only. Fault reporting of channel 1 and channel 2 may be erroneous.	B
SEH	7	SEL	Version B only. SEH signal will affect SEL and vice versa. If DIAG_EN is high only channel 1 or 4 can be read at SNS.	B
$\overline{\text{ST2}}$	8	$\overline{\text{ST3}}$	Version A only. Fault reporting of channel 2 and channel 3 may be erroneous.	B
SEL	8	$\overline{\text{FAULT}}$	Version B only. If $\overline{\text{FAULT}}$ high and DIAG_EN high, only channel 2 or channel 4 can be read at SNS.	B
$\overline{\text{ST3}}$	9	$\overline{\text{ST4}}$	Version A only. Fault reporting of channel 3 and channel 4 may be erroneous.	B
$\overline{\text{FAULT}}$	9	CS	Version B only. Fault reporting and current sense reporting will be erroneous.	B
$\overline{\text{ST4}}$	10	CL	Version A only. $\overline{\text{ST4}}$ voltage could cause erroneous current limit to be set on device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
CS	10	CL	Version B only. Voltage level on CS could cause erroneous current limit to be set on device.	B
CL	11	GND	Device will default to internal current limit.	C
GND	12	THER	Device will be in "auto-retry" mode when encountering a thermal fault.	B
THER	13	DIAG_EN	THER signal will affect DIAG_EN signal and vice versa.	B
OUT4	15	OUT4	No effect	D
OUT4	16	OUT3	Output of channel 4 will be tied to output of channel 3.	B
OUT3	17	OUT3	No effect.	D
OUT3	18	NC	No effect.	D
NC	19	VS	No effect.	D
VS	20	VS	No effect.	D
VS	23	NC	No effect.	D
NC	24	OUT2	No effect.	D
OUT2	25	OUT2	No effect.	D
OUT2	26	OUT1	Output of channel 2 will be tied to output of channel 1.	B
OUT1	27	OUT1	No effect.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (VS)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1, 12	Supply power will be bypassed and device will not turn on.	B
NC	2, 19, 24	No effect.	D
INx	3, 4, 5, 6	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
$\overline{\text{STx}}$	7, 8, 9, 10	Version A only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
SEH	7	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
SEL	8	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
$\overline{\text{FAULT}}$	9	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
CS	10	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
CL	11	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
THER	13	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
DIAG_EN	14	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell.	A
OUTx	15, 16, 17, 18, 25, 26, 27, 28	Output will be pulled to supply voltage. Short-to-battery detection will be triggered if configured.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2021) to Revision B (June 2021)	Page
• Updated Failure Mode Distribution to "10%" in "Protection functions fails to trip" row	4

Changes from Revision * (January 2020) to Revision A (May 2021)	Page
• Updated to current TI format	2

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