Functional Safety Information

TPS7B770x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS7B770x-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

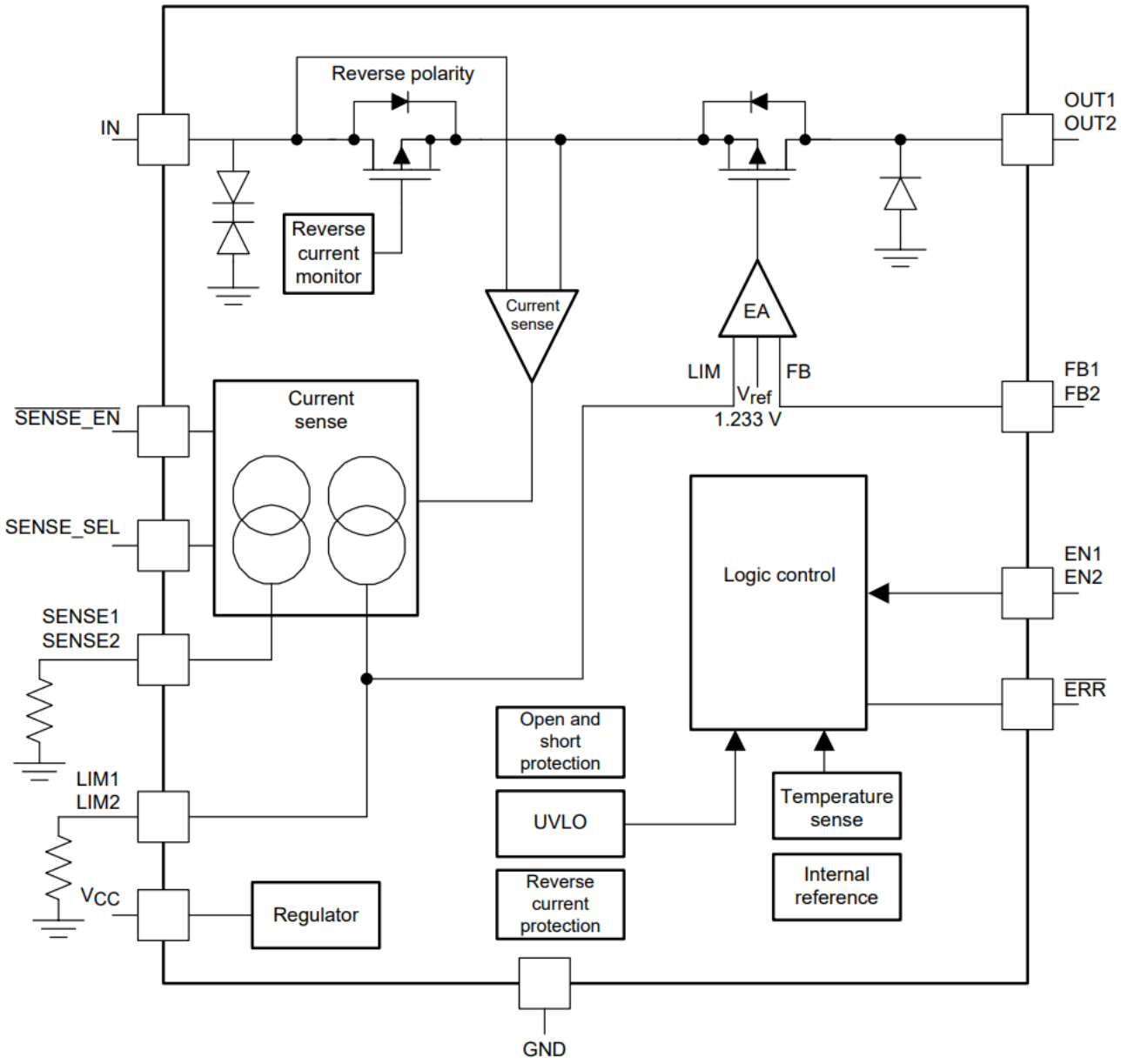

Figure 1-1. Functional Block Diagram

The TPS7B770x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7B770x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 and Table 2-3 provide FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 and Table 2-4 provide FIT rates based on the Siemens Norm SN 29500-2

2.1 Single-Channel FIT Rate

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	7
Package FIT rate	10

The failure rate and mission profile information in Table 2-1comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 750mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed ≤ 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-1 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 Dual-Channel Package FIT Rate

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	6
Package FIT rate	10

The failure rate and mission profile information in Table 2-3comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 750mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed ≤ 50V supply	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B770x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output (output low)	50
Output high (following input)	10
Output not in specification	35
Short circuit, any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B770x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 and Figure 4-2 show the TPS7B770x-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B770x-Q1 data sheet.

4.1 Single-Channel Package

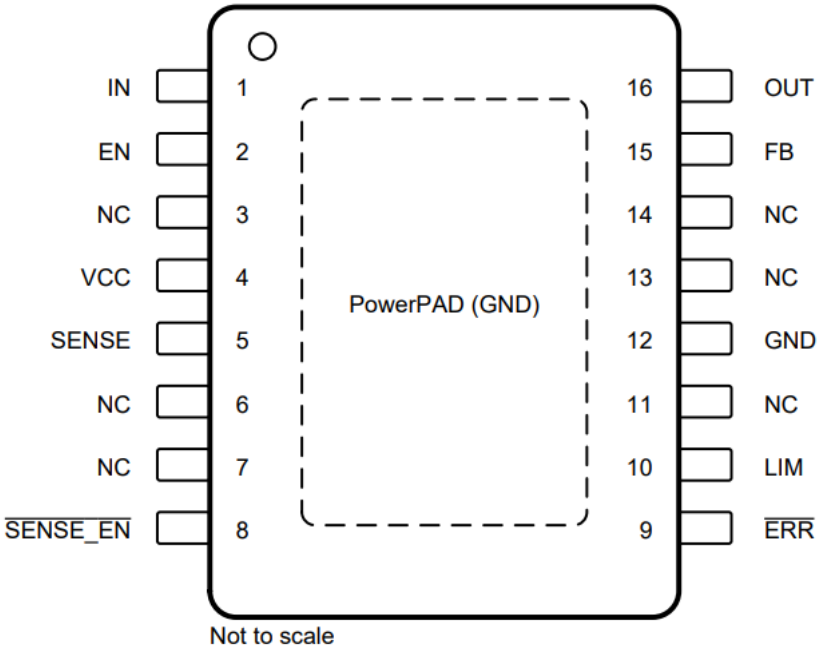

Figure 4-1. Single-Channel, TPS7B7701-Q1 PWP Package, 16-Pin HTSSOP With PowerPAD™ Integrated Circuit Package (Top View)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No input to the device. The output is off.	B
EN	2	No input to the device. The output is off.	B
NC	3	No effect, normal operation	D
VCC	4	Device cannot turn on.	B
SENSE	5	No use of current sense functionality	B
NC	6	No effect, normal operation.	D
NC	7	No effect, normal operation.	D
SENSE_EN	8	Sense functionality enabled.	B
ERR	9	Device falsely reports error signal.	B
LIM	10	Current limit is set to default.	B
NC	11	No effect, normal operation.	D
GND	12	No effect, normal operation.	D
NC	13	No effect, normal operation.	D
NC	14	No effect, normal operation.	D
FB	15	Device acts as a switch.	B
OUT	16	Regulation is not possible; the device operates at current limit. The device can cylce in and out of thermal shutdown.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No input, the output is at ground.	B
EN	2	Device not enabled, the output is at ground.	B
NC	3	No effect, normal operation.	D
VCC	4	Device still operates, but internal regulator output VCC oscillates, and so output noise is increased, and noise on the SENSEx, ILIMx pins also increases	C
SENSE	5	No change in device function; no access to SENSE outputs.	B
NC	6	No effect, normal operation.	D
NC	7	No effect, normal operation.	D
SENSE_EN	8	SENSE_EN is always active (low) (there is an internal pulldown resistor)	B
ERR	9	No access to error signal.	B
LIM	10	When LIMx is open, OUTx does not turn on.	B
NC	11	No effect, normal operation.	D
GND	12	There is no current loop for internal biasing, so the device cannot function.	B
NC	13	No effect, normal operation.	D
NC	14	No effect, normal operation.	D
FB	15	The error amplifier input is not connected. The output voltage is indeterminate.	B
OUT	16	The load is not powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN (Pin 2)	Device is always powered.	D
EN	2	NC (Pin 3)	No effect. Normal operation.	D
NC	3	NC (Pin 4)	No effect. Normal operation.	D
VCC	4	Sense (Pin 5)	Internal circuitry has less headroom and performance degrades.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SENSE	5	NC (Pin 6)	No effect. Normal operation.	D
NC	6	NC (Pin 7)	No effect. Normal operation.	D
NC	7	Sense_EN (Pin 8)	No effect. Normal operation.	D
ERR	9	Lim (Pin 10)	If ERR is pulled high, no effect. If ERR is pulled low, current limit increases.	B
LIM	10	NC (Pin 11)	No effect. Normal operation.	D
NC	11	GND (Pin 12)	No effect. Normal operation.	D
GND	12	NC (Pin 13)	No effect. Normal operation.	D
NC	13	NC (Pin 14)	No effect. Normal operation.	D
NC	14	FB (Pin 15)	No effect. Normal operation.	D
FB	15	Out (Pin 16)	Output voltage is equal to the internal reference voltage. If OUT is forced to greater than 7V, FB can be damaged.	B/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect, normal operation.	D
EN	2	Device is always enabled.	B
NC	3	No effect, normal operation.	D
VCC	4	IN is greater than 6V, VCC can be damaged. IN is less that 6V, Output can be out of regulation. SENSE outputs incorrect.	A/B
SENSE	5	If IN is greater than VCC + 0.3V, SENSE can be damaged. If IN is less than VCC + 0.3V, lose sense functionality.	A/B
NC	6	No effect, normal operation.	D
NC	7	No effect, normal operation.	D
SENSE_EN	8	If IN is greater than 7V, SENSE_EN can be damaged. If IN is less than 7V, sense functionality is always disabled.	A/B
ERR	9	If IN is greater than 7V, ERR can be damaged. If IN is less than 7V, loss of error functionality.	A/B
LIM	10	If IN is greater than 7V, LIM can be damaged. If IN is less than 7V, VOUTx does not come up	A/B
NC	11	No effect, normal operation.	D
GND	12	Supply is shorted to GND, no output voltage.	B
NC	13	No effect, normal operation.	D
NC	14	No effect, normal operation.	D
FB	15	If supply is greater than 7V, the maximum rating for FB is violated and can damage the device. If supply is less than 7V, the output is approximately 0V.	B
OUT	16	Regulation not possible. $V_{out} = V_{in}$.	B

4.2 Dual-Channel Package

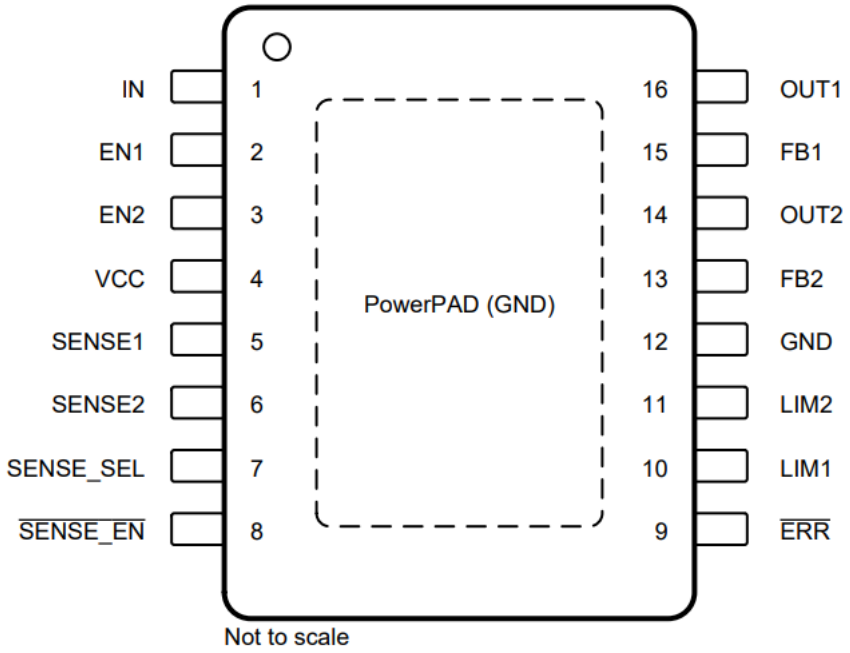

Figure 4-2. Dual-Channel, TPS7B7702-Q1 PWP Package, 16-Pin HTSSOP With PowerPAD™ Integrated Circuit Package (Top View)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No input to the device. The output is off.	B
EN1	2	No input to the device. The OUTx is off.	B
EN2	3	No input to the device. The OUTx is off.	B
VCC	4	Device cannot turn on.	B
SENSE1	5	No use of current sense functionality for OUTx	B
SENSE2	6	No use of current sense functionality for OUTx	B
SENSE_SEL	7	If $\overline{\text{SENSE\_EN}}$ is low, SENSE1 and SENSE2 are enabled. Otherwise, outputs are high impedance.	B
$\overline{\text{SENSE\_EN}}$	8	Sense functionality enabled.	B
ERR	9	Device falsely reports error signal.	B
LIM1	10	Current limit for OUTx is set to default.	B
LIM2	11	Current limit for OUTx is set to default.	B
GND	12	No effect, normal operation.	D
FB2	13	Device acts as a switch	B
OUT2	14	Regulation is not possible; the device operates at current limit. OUTx can cycle in and out of thermal shutdown.	B
FB1	15	Device acts as a switch.	B
OUT1	16	Regulation is not possible; the device operates at current limit. OUTx can cycle in and out of thermal shutdown.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No input, the output is at ground.	B
EN1	2	Device not enabled, the OUTx is at ground.	B
EN2	3	Device not enabled, the OUTx is at ground.	B
VCC	4	Device still operates, but internal regulator output VCC oscillates, and so output noise is increased, and noise on the SENSEx, ILIMx pins also increases.	C
SENSE1	5	No change in device function; no access to SENSEx outputs.	B
SENSE2	6	No change in device function; no access to SENSEx outputs.	B
SENSE_SEL	7	Current channel monitoring status is unknown.	B
$\overline{\text{SENSE\_EN}}$	8	SENSE_EN is always active (low) (there is an internal pulldown resistor).	B
ERR	9	No access to error signal.	B
LIM1	10	When LIMx is open, OUTx does not turn on.	B
LIM2	11	When LIMx is open, OUTx does not turn on.	B
GND	12	There is no current loop for internal biasing, so the device cannot function.	B
FB2	13	The error amplifier input is not connected. The output voltage is indeterminate.	B
OUT2	14	The load is not powered.	B
FB1	15	The error amplifier input is not connected. The output voltage is indeterminate.	B
OUT1	16	The load is not powered.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN1	Device is always powered.	D
EN1	2	EN2	There is no discrete control over OUTx outputs	B
EN2	3	VCC	If EN is greater than 6V, VCC can be damaged. If EN is less that 6V, Output can be out of regulation, SENSE outputs incorrect.	A/B
VCC	4	SENSE1	Internal circuitry has less headroom and performance degrades	C
SENSE1	5	SENSE2	Current reading is incorrect.	B
SENSE2	6	SENSE_SEL	Current reading is incorrect. Damage to SENSE_SEL pin in possible.	A/B
SENSE_SEL	7	$\overline{\text{SENSE\_EN}}$	Multiplexing capabilities are limited to both SENSEx signals being on or high impedance	B
$\overline{\text{SENSE\_EN}}$	8	ERR	If ERR is pulled high, SENSEx channels are both high impedance. If ERR is pulled low, SENSE_SEL multiplexes between outputs.	B
ERR	9	LIM1	If ERR is pulled high, no effect. If ERR is pulled low, current limit increases.	B
LIM1	10	LIM2	If LIMx is pulled high, no effect. If LIMx is pulled low, current limit for OUTx is set to default.	B
LIM2	11	GND	Current limit for OUTx is set to default.	B
GND	12	FB2	OUTx acts as a switch.	B
FB2	13	OUT2	OUTx voltage is equal to the internal reference voltage. If OUTx is forced to greater than 7V, FB can be damaged.	B/A
OUT2	14	FB1	OUTx voltage is equal to the internal reference voltage. If OUTx is forced to greater than 7V, FB can be damaged.	B/A
FB1	15	OUT1	OUTx voltage is equal to the internal reference voltage. If OUTx is forced to greater than 7V, FB can be damaged.	B/A
OUT1	16	IN	Regulation not possible. $V_{out} = V_{in}$	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect, normal operation.	D
EN1	2	Device is always enabled.	B
EN2	3	Device is always enabled.	B
VCC	4	If IN is greater than 6V, VCC can be damaged. If IN is less that 6V, Output can be out of regulation. SENSE outputs incorrect.	A/B
SENSE1	5	If IN is greater than VCC + 0.3V, SENSE can be damaged. If IN is less than VCC + 0.3V, lose sense functionality.	A/B
SENSE2	6	If IN is greater than VCC + 0.3V, SENSE can be damaged. If IN is less than VCC + 0.3V, lose sense functionality.	A/B
SENSE_SEL	7	If $\overline{\text{SENSE\_EN}}$ is low, SENSE1 is active and SENSE2 is high impedance. Otherwise, both are high impedance.	B
$\overline{\text{SENSE\_EN}}$	8	If IN is greater than 7V, $\overline{\text{SENSE\_EN}}$ can be damaged. If IN is less than 7V, sense functionality is always disabled.	A/B
ERR	9	If IN is greater than 7V, ERR can be damaged. If IN is less than 7V, loss of error functionality.	A/B
LIM1	10	If IN is greater than 7V, LIMx can be damaged. If IN is less than 7V, VOUTx does not come up	A/B
LIM2	11	If IN is greater than 7V, LIMx can be damaged. If IN is less than 7V, VOUTx does not come up.	A/B
GND	12	Supply is shorted to GND, no output voltage. Damage to upstream supply is possible.	B
FB2	13	If supply is greater than 7V, the maximum rating for FBx is violated and can damage the device. If supply is less than 7V, the output is approximately 0V.	A/B
OUT2	14	Regulation not possible. $V_{out} = V_{in}$.	B
FB1	15	If supply is greater than 7V, the maximum rating for FBx is violated and can damage the device. If supply is less than 7V, the output is approximately 0V.	A/B
OUT1	16	Regulation not possible. $V_{out} = V_{in}$.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (August 2024)	Page
• Updated document to current TI format	2
• Added Pin FMA to the document	6

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