Application Report
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An Accurate Approach for Calculating the Efficiency of a Synchronous Buck Converter Using the MOSFET Plateau Voltage

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ABSTRACT

This application note shows how to calculate the power loss for a synchronous buck converter. It discusses the theory calculation for switch losses, inductor losses, input and output capacitor ESR losses, and other losses, as well as their effect to the efficiency of a synchronous buck converter. Additionally, this article introduces a method to estimate the MOSFET plateau (Vpl) voltage for different drain to source currents. With the more accurate MOSFET plateau voltage, highly-accurate efficiency calculations can be made.

Contents

List of Figures

List of Tables

1 Overview

TI buck switching solutions include power modules, converters (regulators) and controllers. With integrated FETs and inductor, power modules simplify your power supply design process and get you to market faster. With an integrated FET or FETs and external inductor, converters provide a good balance of integration and flexibility. Controllers with external FETs and inductors provide the most design flexibility for high-power applications. This flexibility allows customers to choose FETs and diode maximizing efficiency at a particular load level. Buck switching regulators are also divided into synchronous buck and non-synchronous. The difference is that synchronous regulators integrate low side switch to replace the external diode in non-synchronous, which helps improve efficiency.

Customers will estimate the efficiency of the buck converter when they choose a controller IC. For either space constrained applications or higher power designs where ambient temperature are high, accurately efficiency calculations are necessary. Several losses in buck converter must be calculated to estimate the efficiency and losses.

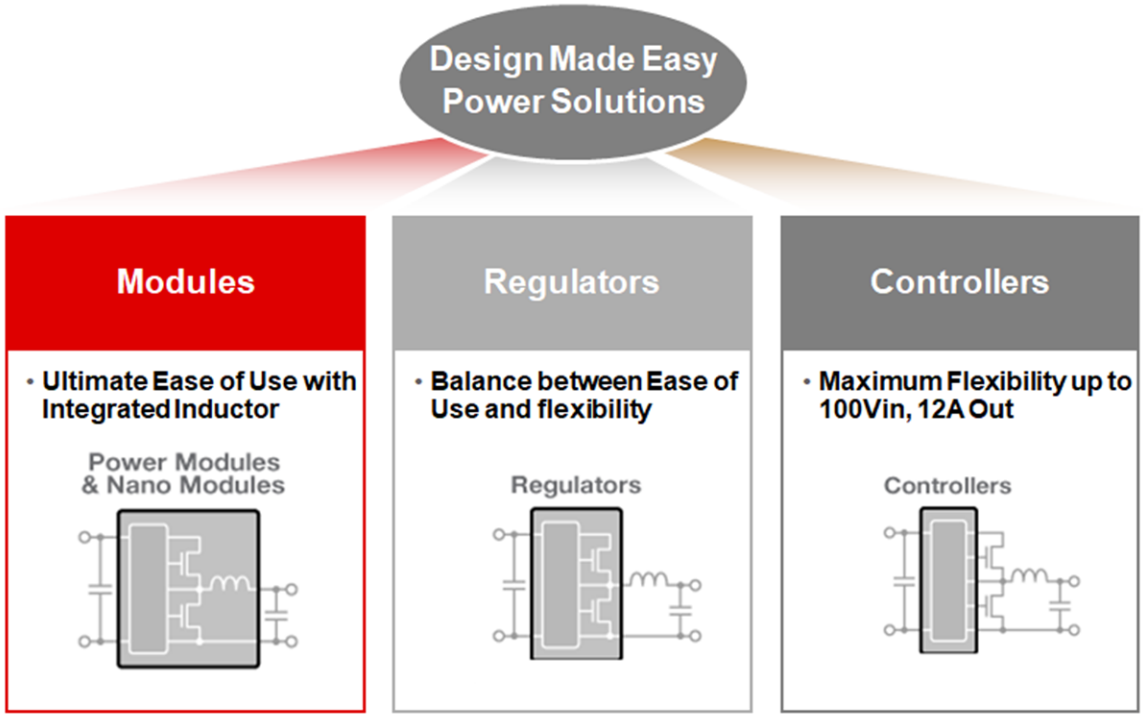

Figure 1. TI Buck Switching Solutions

2 Power Losses Calculation for Synchronous Buck Converter

Figure 2 shows the power losses of synchronous buck converter, including the switching losses, the inductor losses, the capacitor losses and other losses. The efficiency calculation is shown in Equation 1 and Equation 2.This section shows how to calculate these power losses.

$$P_{total\_loss} = P_{switches} + P_{inductor} + P_{capacitors} + P_{other} \quad (1)$$

$$\eta = \frac{V_o I_o}{V_o I_o + P_{total\_loss}} \times 100\% \quad (2)$$

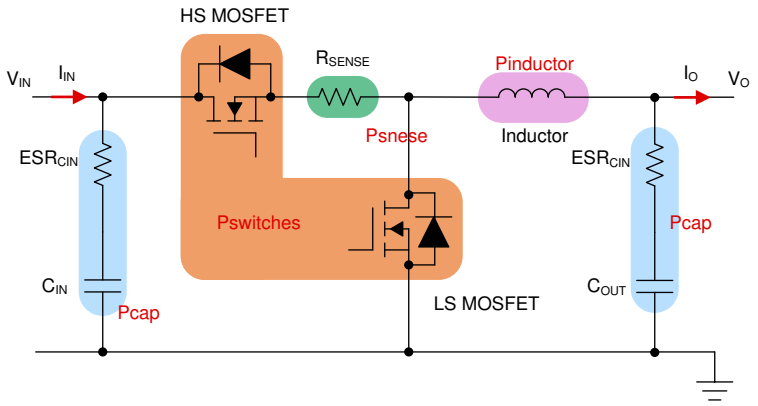

Figure 2. Power Losses of Synchronous Buck Converter

2.1 Switching Losses Calculation

There are two MOSFETs in synchronous buck converter, the High side (HS) MOSFET and the Low side (LS) MOSFET. The MOSFETs losses are composed of several parts: switching loss, conduction loss, gate drive loss, output capacitance loss, and LS MOSFET body-diode loss. These losses are analyzed in the following sections.

2.1.1 Switching Loss Calculation

Figure 3 illustrates the MOSFETs turn on and turn off transition. It can be divided into five parts:

Time t_0: the MOSFET turns off, V_{GS} is zero;

Time t_1: V_{GS} reaches V_{TH};

Time $_2$: V_{GS}reaches V_{PL}, MOSFET begins turn on, I_{DS} is increased from zero to I_O;

Time t_3: V_{GS} states in V_{PL}, MOSFET keeps turning on, I_{DS} is I_O, V_{DS} is reduced from V_{IN} to zero;

Time t_4: V_{GS} keeps increased, MOSFET fully turns on;

During the transition (Time t_2 and Time t_3), the I_{DS} and V_{DS} are not zero, so the switching loss is caused when MOSFET turns on and turns off. Equation 3 shows the switching loss calculation.

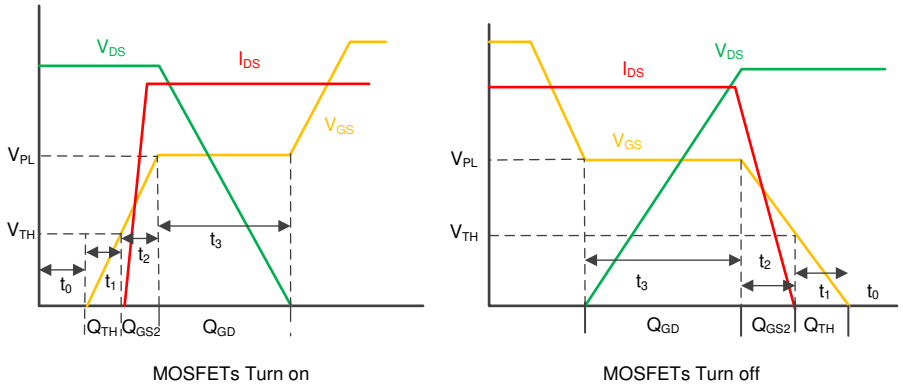

Figure 3. MOSFET Switch Transition

$$P_{switching} = \frac{V_{in}}{2}\left(I_o - \frac{\Delta i_{Lpp}}{2}\right) \times f_{sw} \times t_r + \frac{V_{in}}{2}\left(I_o + \frac{\Delta i_{Lpp}}{2}\right) \times f_{sw} \times t_{off} \quad (3)$$

Δi_{Lpp} is the ripple current in the inductor. t_r is the switching time when MOSFET turns on, t_{off} is switching time when MOSFET turns off. f_{sw} is the switching frequency.

$$\Delta i_{Lpp} = \frac{V_{in} - V_o}{L} \frac{V_o}{V_{in}} \frac{1}{f_{sw}} \tag{4}$$

$$t_r = t_1 + t_2 = \left(\frac{Q_{gs2}}{V_{dr} - 0.5 \times \left(V_{pl} + V_{gs(th)} \right)} + \frac{Q_{gd}}{V_{dr} - V_{pl}} \right) (R_g + R_{drive}) \tag{5}$$

$$t_{off} = t_3 + t_4 = \left(\frac{Q_{gs2}}{V_{dr} - 0.5 \times \left(V_{pl} + V_{gs(th)} \right)} + \frac{Q_{gd}}{V_{pl}} \right) \times (R_g + R_{drive}) \tag{6}$$

Use Equation 3 to calculate the HS MOSFET switching loss in a synchronous buck converter. Since the LS MOSFET can achieve Zero Voltage Switching (ZVS) turn on and Zero Current Switching (ZCS) turn off, the switching loss of LS MOSFET can be neglected.

2.1.2 Conduction Loss Calculation

The conduction loss is determined by the on-resistances of the MOSFETs and the transistor RMS current. Considering the temperature dependency of on-resistances δ and the inductor ripple current, specifically, the conduction loss for HS FET and the LS FET can be calculated by using Equation 7 and Equation 8, respectively:

$$P_{HS\_conduction} = R_{HS\_ds\_on} (1 + \delta) \times I_o^2 \times D \times \left(1 + \frac{1}{12} \left(\frac{\Delta i_{Lpp}}{I_o} \right)^2 \right) \tag{7}$$

$$P_{LS\_conduction} = R_{LS\_ds\_on} (1 + \delta) \times I_o^2 \times (1 - D) \times \left(1 + \frac{1}{12} \left(\frac{\Delta i_{Lpp}}{I_o} \right)^2 \right) \tag{8}$$

2.1.3 Gate Drive Loss Calculation

The gate drive loss of the MOSFETs is caused by the energy required to charge and discharge the MOSFET gate, as Figure 4shows. It can be calculated by using Equation 9, Qg is the total gate charge. The gate drive loss is frequency dependent and also a function of the gate capacitance of the MOSFET. The higher switching frequency, the higher the gate-drive loss is. This contributes to the efficiency reducing as the switching frequency goes up. Normally, larger MOSFETs with lower $R_{DS(on)}$ provide lower conduction loss at the cost of higher gate capacitances, which results in higher gate-drive losses.

$$P_{gate\_drive} = Q_g \times V_{drive} \times f_{sw} \tag{9}$$

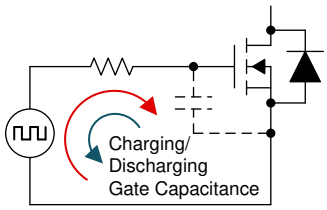

Figure 4. Gate Drive Loss of MOSFET

2.1.4 Other Losses

Output capacitance loss is another part of the MOSFET power losses, which is induced by output capacitance charge/discharge. The Coss loss for HS and LS FETs can be calculated in Equation 10 and Equation 11.

$$P_{HS\_Coss} = \frac{1}{2} Q_{oss1} \times V_{in} \times f_{sw} \tag{10}$$

$$P_{LS\_Coss} = \frac{1}{2} Q_{oss2} \times V_{in} \times f_{sw} \tag{11}$$

Qoss1 and Qoss2 are the output charge of HS and LS MOSFETs respectively. In a synchronous buck converter, the low-side MOSFET switching loss is negligible as it is switched at zero voltage, current just commutates from the channel to the body diode or vice versa during the transition dead-times. So the body diode loss is another part of loss of LS MOSFET. It is composed of body diode reverse recovery loss and body diode conduction loss, which can be calculated using Equation 12 and Equation 13, respectively.

$$P_{DRR} = V_{in} \times Q_{RR} \times f_s \tag{12}$$

$$P_{dead} = V_F \left(I_o - \frac{\Delta i_{Lpp}}{2} \right) \times t_{dr} \times f_s + V_F \left(I_o + \frac{\Delta i_{Lpp}}{2} \right) \times t_{df} \times f_s \tag{13}$$

Qrr is the reverse recovery charge of body diode, V_F is the diode forward voltage and the t_{dr} and t_{df} are the dead times at the turn off and turn on intervals.

2.2 Inductor Losses Calculation

The inductor loss is composed of two parts: winding loss and the core loss. Winding loss of inductor caused by the inductor series resistance ESR_L, it can be calculated by using Equation 14. Core loss is related to core material, operating frequency, output current and current ripple in the inductor, as show in Equation 15.

$$P_{L\_winding} = ESR_L \times {I_{out}}^2 \times \left(1 + \frac{1}{12} \left(\frac{\Delta i_{Lpp}}{I_o} \right)^2 \right) \tag{14}$$

$$P_{L\_core} = K_1 \times {f_s}^{\alpha} \left(K_2 \Delta i_{Lpp} \right)^{\beta} \tag{15}$$

K1, K2, α, β depend on the core material, operating frequency and operating temperature.

2.3 Input and Output Capacitor Losses Calculation

Normally ESR of the input and output capacitors also cause power loss of a buck converter. Usually the ceramic capacitors typically have very small ESR and the electrolytic capacitors typically have larger ESR. The input capacitors and output capacitors loss can be calculated using Equation 16 and Equation 17 respectively.

$$P_{Cin\_Loss} = ESR_{Cin} \times {I_{out}}^2 \times D \times (1 - D) \tag{16}$$

$$P_{Cout\_Loss} = ESR_{Cout} \times \frac{1}{12} \times {\Delta i_{Lpp}}^2 \tag{17}$$

2.4 Other Losses

The sense resistor and the control IC also cause power loss in buck converters. Typically their losses are very small so that it will have little influence on efficiency. When the sense resistor is series with the HS MOSFET, the loss caused by sense resistor can be calculated using Equation 18. The control IC loss is calculated using Equation 19 The I_μ is the quiescent current of a control IC.

$$P_{sense} = R_{sense} \times {I_{out}}^2 \times D \times \left(1 + \frac{1}{12} {\Delta i_{Lpp}}^2 \right) \tag{18}$$

$$P_{IC} = V_{in} \times I_\mu \tag{19}$$

3 MOSFETs' Vpl and Vgs(th) Estimation

3.1 Theory for Vpl and Vgs(th) Estimation

As discussed in Section 2.1, the HS MOSFETs carry the inductor current during the PWM on-time and typically incurs most of the switching loss. It is therefore imperative to balance the conduction and switching loss when choosing a high-side MOSFET. Equation 3 shows how to calculate the switching loss. To make accurate predictions in efficiency calculations, accurate switching times for tr and toff should be determined. Accurate switching times are dependent on the accuracy of Qgs2 and Qgd as well as Vgs(th) and Vpl of the MOSFET. These parameters can be found in the MOSFET data sheet.

However the data sheet will specify Vgs(th) and Vpl values in its characteristic table, the values are only tested with specific drain-source currents. The Vgs(th) and Vpl will change as drain-source current change. This section will introduce how to estimate the Vgs(th) and Vpl of a MOSFET by using the output characteristic curves.

Figure 5 shows a typical MOSFETs turn on waveform. The process of MOSFETs turn on can be divided into four stages.

Time between t0 – t1: time required to bring the gate voltage from zero to Vgs(th) .

Time between t1 - t2: the gate voltage has reached Vgs(th) and drain current begins to flow.

Time between t2 – t3: t2 the drain to source voltage starts to fall. Only $_{CMiller}$ is charged, Vgs = Vpl.

Time between t3 – t4: gate voltage rises form the plateau up to its final drive voltage, Vgs > Vpl.

Figure 6 shows the output characteristic curves of MOSFET. There are four sections in this curve. The yellow block shows the Figure 5, interval t2 – t3 is corresponded to the yellow block in Figure 6, the saturation zone of output characteristic curve. In the saturation zone (vgs > $V_{gs(th)}$, vds > vgs – $V_{gs(th)}$), the MOSFETs satisfied and the drain current can be calculated using Equation 20.

$$i_D = K_n(v_{gs} - V_{gs(th)})^2 \quad (20)$$

i_D is the drain to source current, Kn is the conductance constant, The conductance constant Kn is a physical parameter of MOSFET and is related to the length and width of the channel of the MOSFET, the electron mobility in the inversion layer, and the unit area of the gate (between substrate) oxide.

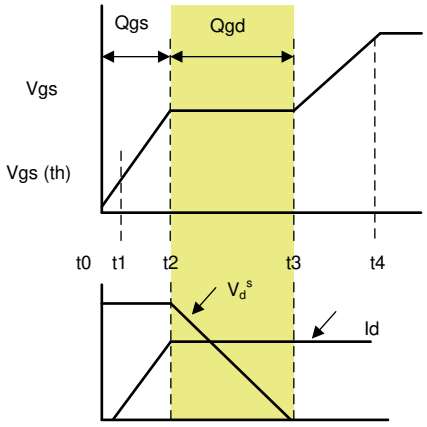

Figure 5. MOSFET Turn on Waveform

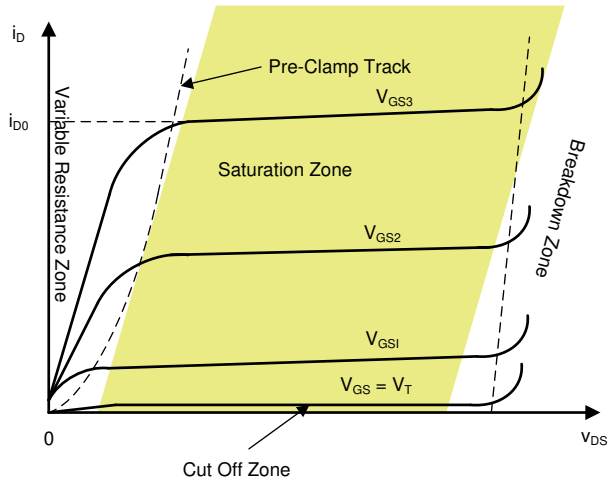

Figure 6. Output Characteristic Curves

Figure 7 is the output characteristic curves given in a MOSFET data sheet. Read from two curves the Id and Vgs and use Equation 21 populating I_{D1}, I_{D2}, Vgs1 and Vgs2 to calculate. Vgs(th) and Kn can be calculated by using Equation 22 and Equation 23, respectively. Finally the Vpl is calculated using Equation 24, populating with the calculated Vgs(th) and specified Ids. The Vpl is estimated in different drain to source current.

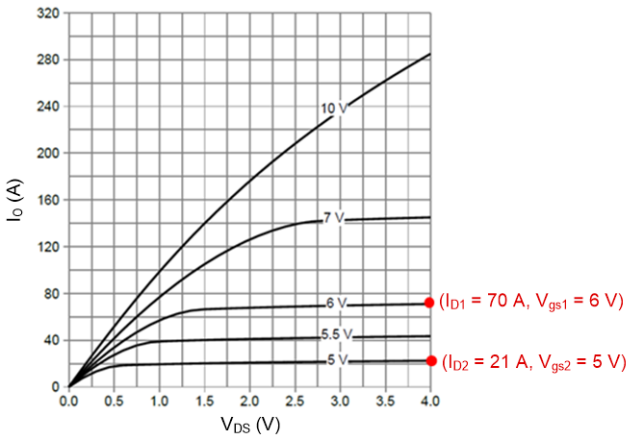

Figure 7. Output Characteristics Curve

$$\begin{cases} i_{D1} = K_n (v_{gs1} - V_{gs(th)})^2 \\ i_{D2} = K_n (v_{gs2} - V_{gs(th)})^2 \end{cases} \quad (21)$$

$$V_{gs(th)} = \frac{v_{gs2} \times \sqrt{\frac{i_{D1}}{i_{D2}}} - v_{gs1}}{\sqrt{\frac{i_{D1}}{i_{D2}}} - 1} \quad (22)$$

$$K_n = \frac{i_{D1}}{(V_{gs1} - V_{gs(th)})^2} \quad (23)$$

$$V_{pl} = \sqrt{\frac{i_D}{K_n}} - V_{gs(th)} \quad (24)$$

According Equation 22 through Equation 24, design the calculator shows in Table 1. We can easily calculate the Kn and Vgs(th) by inputting Id and Vgs which obtained from the output characteristic curves of MOSFET data sheet. Using special Ids, we can calculate Vpl correspondingly. For example, using MOSFET BSC117N08NS5, Ids = 10 A, calculates Vpl = 4.58 V correspondingly.

Table 1. Vpl Calculator

Calculate of Vplateau		
Input: The Specification from MOSFET data sheet		
Vgs1	6	From: Typ. output characteristics (Vds-Ids)
ds1	70	From: Typ. output characteristics (Vds-Ids)
Vgs2	5	From: Typ. output characteristics (Vds-Ids)
Ids2	21	From: Typ. output characteristics (Vds-Ids)
Ids	10	Ids In work condition
The Calculate Output		
Kn	13.51	Conductance constant
Vgsth	3.72	Threshold voltage
Vplateau	4.58	In the condition of Ids

3.2 Vpl Calculation Examples

To verify the calculated value for Vpl, consider the MOSFETs BSC117N08NS5 and BSC037N08NS5 as examples.

Figure 8 shows the Vgs waveforms and resulting Vpl for 10 A and 20 A of Ids current using. Table 2 shows the calculated.

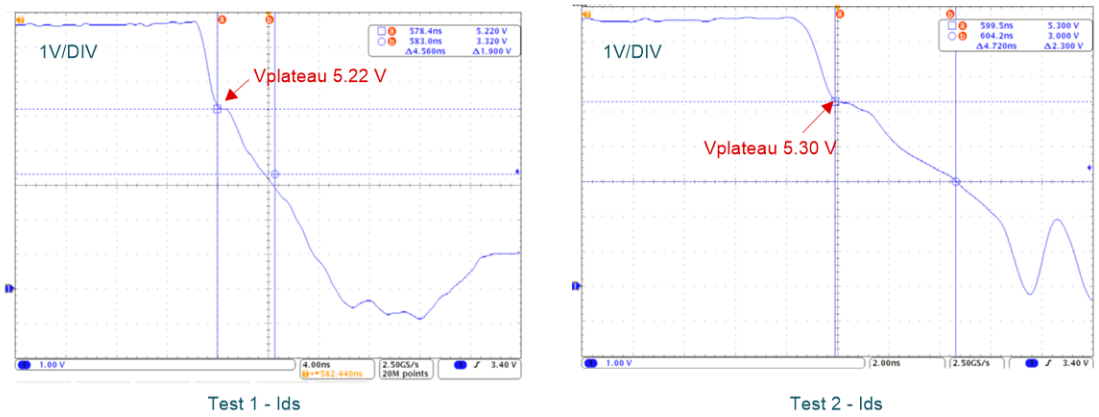

Figure 8. Vgs Waveforms of BSC117N08NS5

Table 2. Vpl Results Comparison

BSC117N08NS5		
Vplateau	Test	Calculate (Vpl)
Ids = 10 A	5.22 V	4.58 V
Ids = 20 A	5.30 V	4.94 V

Figure 9 show the Vgs waveform of BSC037N08NS5 with drain current 3 A. The waveform shows Vpl = 4.0 V, while the calculated result is 3.91 V.

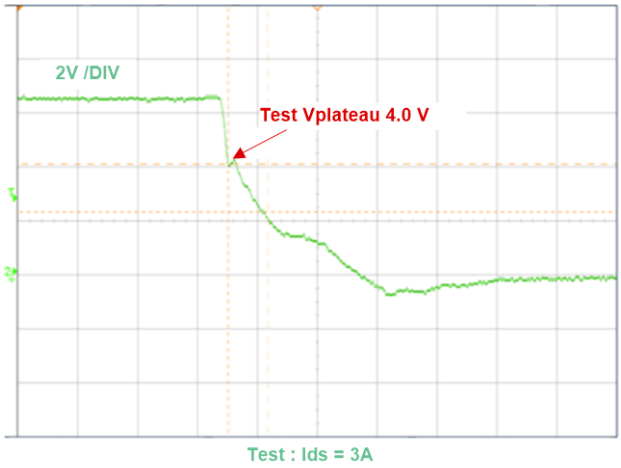

Figure 9. Vgs Waveforms of BSC037N08NS5

From the comparison of these two groups, the test and calculated results are consistent and the errors of them less than 1 V is achieved. As current Id changes, Vpl also changes.

4 Power Losses Calculation and Efficiency Estimation

To verify the accuracy of the calculations for the power loss and to estimate the efficiency, two examples are given in this report. Figure 10 shows the schematic of the LM5145 test board.

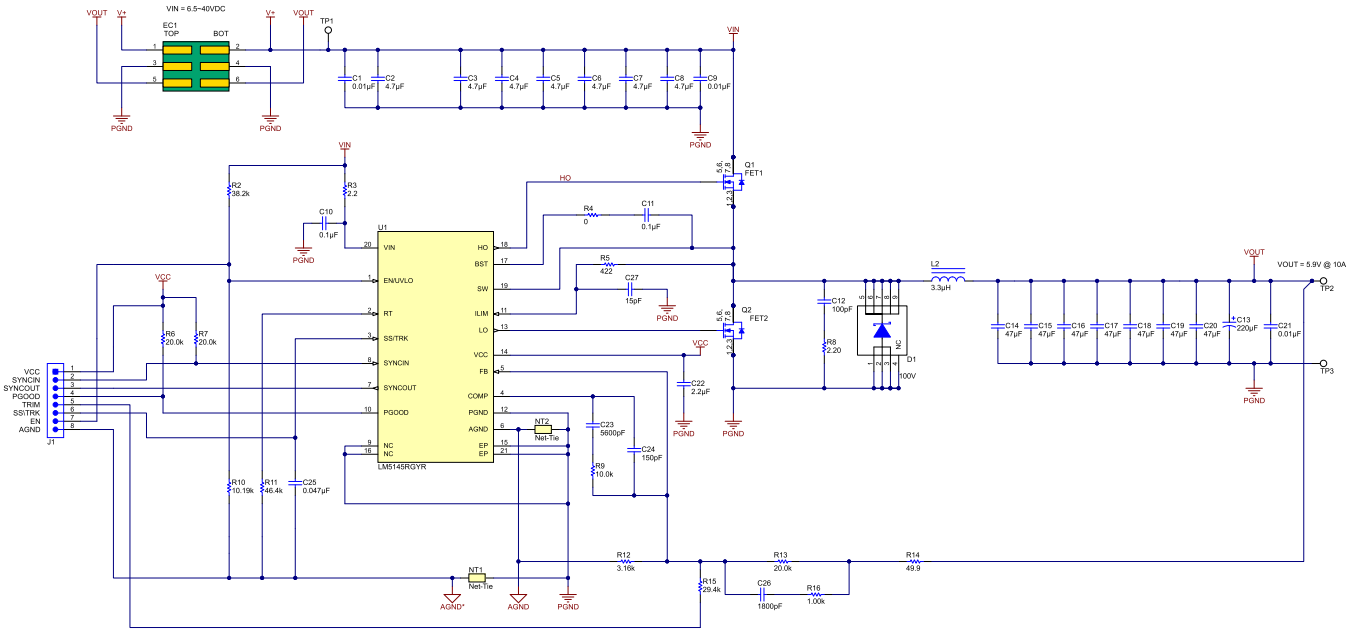

Figure 10. Schematic LM5145

By choosing different HS FET1 switch Q1, there are two group test results.

Table 3. Test Groups

	Q1	Q2
Test condition 1	BSC117N08NS5	BSC037N08NS5
Test condition 2	BSC037N08NS5	BSC037N08NS5

Refer to Section 3.1, the Vpl and Vgs(th) are 4.58 V and 3.72 V, respectively, for BSC117N08NS5 when the Ids is 10 A. Refer to the Section 2, calculate the power losses step by step. Table 4, Table 5 and Table 6 list the calculated power losses results with different V_{IN}.

Table 4. Power Losses Calculation Results (V_{IN} = 6.5 V)

Condition: V_{IN} = 6.5 V, V_{OUT} = 5.9 V, I_{OUT} = 10 A, f = 230 kHz, L = 3.3 µH						
	HS-MOSFET	LS-MOSFET	Inductor	Capacitors	Other	Total
Power Loss	2.51 W	0.32 W	0.38 W	0.02 W	0.38 W	3.61 W
Percent	69.5%	8.8%	10.5%	0.6%	10.5%	100%

V_{IN} = 6.5 V, the efficiency of calculated is 94.2%, the test efficiency is 94.0%.

Table 5. Power losses Calculation Results (V_{IN} = 25 V)

Condition: V_{IN} = 25 V, V_{OUT} = 5.9 V, I_{OUT} = 10 A, f = 230 kHz, L = 3.3 µH						
	HS-MOSFET	LS-MOSFET	Inductor	Capacitors	Other	Total
Power Loss	1.07 W	1.16 W	0.98 W	0.03 W	0.17 W	3.41 W
Percent	31.4%	34.0%	28.7%	0.9%	5.0%	100%

V_{IN} = 25 V, the efficiency of calculated is 94.5%, the test efficiency is 94.7%.

Table 6. Power Losses Calculation Results (V_{IN} = 35 V)

Condition: V_{IN} = 35 V, V_{OUT} = 5.9 V, I_{OUT} = 10 A, f = 230 kHz, L = 3.3 µH						
	HS-MOSFET	LS-MOSFET	Inductor	Capacitors	Other	Total
Power Loss	1.05 W	1.38 W	1.13 W	0.03 W	0.19 W	3.78 W
Percent	27.7%	36.5%	29.9%	0.8%	5.0%	100%

V_{IN} = 35 V, the efficiency of calculated is 93.9%, the test efficiency is 93.5%.

From Table 4, Table 5 and Table 6,the main power losses of a synchronous buck converter are the switch loss and the inductor loss, which are more than 90%. Besides, with the different V_{IN}, the switch loss and inductor loss also different. The V_{IN} increases, then duty cycle decreases, the switching loss increases and conduction loss decreases. So the HS MOSFETS is in a trade-off between switching loss and conduction loss. The V_{IN} increases, both the LS MOSFET and the inductor losses increase. The inductor losses are as the significant loss in wide V_{IN} applications.

Figure 11, Figure 12 and Figure 13 show the efficiency comparison between estimation and bench test using different input voltages. The curves show efficiency between calculate and test with currents from 5 A to 10 A. From the curves, the efficiency errors are all less than 2%. This shows the accuracy of the calculated of power losses.

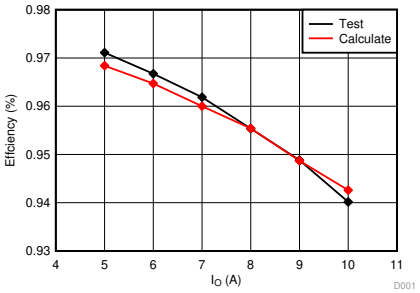

Figure 11. Efficiency Comparison (V_{IN} = 6.5 V)

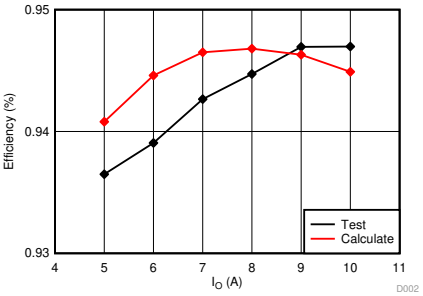

Figure 12. Efficiency Comparison (V_{IN} = 25 V)

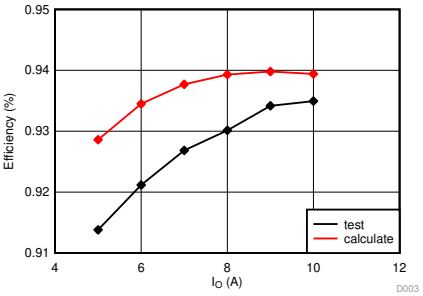

Figure 13. Efficiency Comparison (V_{IN} = 35 V)

In test condition 2, both the HS switch and LS switch Q2 are using BSC037N08NS5.

Figure 14, Figure 15, and Figure 16 show the efficiency comparison between estimation and bench test using different input voltages. The curves show that the efficiency errors between the calculation and test are less than 2%.

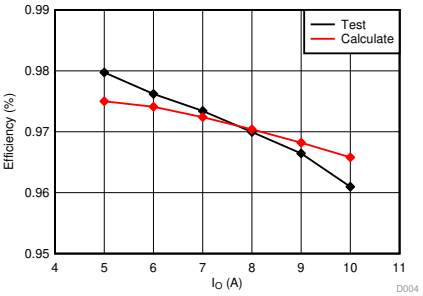

Figure 14. Efficiency Comparison (V_{IN} = 6.5 V)

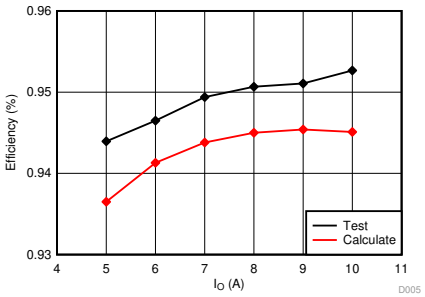

Figure 15. Efficiency Comparison (V_{IN} = 25 V)

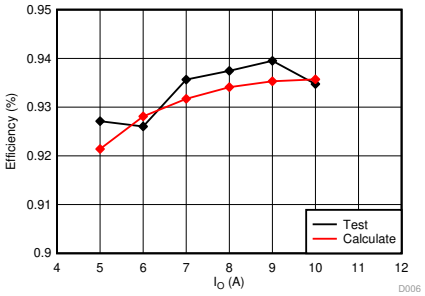

Figure 16. Efficiency Comparison (V_{IN} = 35 V)

5 Summary

This application note summarizes the calculation of the power losses for the synchronous buck converter. The method of evaluating Vpl voltage from the output characteristic curve of MOSFET is introduced, which is helpful to improve the accuracy of the switching loss. Finally, it is proved through experiments that the loss estimation method introduced in this paper has improved accuracy in calculating efficiency with the errors being less than 2%. Moreover, the test results show that most of power losses of the synchronous converter come from the switches losses and inductor losses. When the input voltage increases, the losses of the inductor are significant and cannot be ignored.

6 References

1. Texas Instruments, *Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converter Application Report*
2. Texas Instruments, LM5145EVM-HD-20A High Density Evaluation Module User's Guide

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