Application Note

Powering the i.MX 8M Plus With TPS65219

Power Management IC (PMIC)

ABSTRACT

This application note discusses the TPS65219 Power Management IC (PMIC) full feature-set powering the i.MX 8M Plus processor and principal peripherals. The power delivery network (PDN) described in this document can be used as a guide for integrating the TPS65219 Power Management IC (PMIC) into industrial applications powering the NXP™ i.MX 8M Processor. Example power maps are provided to assist the design process. For any questions or technical support, use the Power Management E2E design support forum.

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Trademarks

1 Introduction

This application note provides a reference power design for the i.MX 8M Plus processor, as well as memory and external peripherals in the system. Powering this type of processor demands requirements such as sufficient current headroom, tight transient requirements, and a number of rails that can be fully controlled for power up and power down sequencing. The TPS65219 is a cost and space optimized design developed by Texas Instruments. This Power Management IC (PMIC) has flexible analog and digital resources that can be configured to supply a variety of processors and SoCs with different power requirements. Factory programmed orderable part numbers (OPNs) come with default non-Volatile Memory (NVM) settings to support specific use cases. Alternatively, the TPS65219 PMIC has a user programmable version that comes with all rails disabled by default and allows customers to program a custom NVM settings for specific output voltages, sequence, etc. When needed, the TPS65219 PMIC can be combined with other PMIC for a multi PMIC design or with external discrete ICs. The TPS65219 GPIOs can be configured to control the enable/disable of external ICs that are part of the power design.

The i.MX 8M Plus™ processor requires a power design that can supply the following main domains: VDD_ARM (for Quad-A53), VDD_SOC (for SoC logic, DRAM controller, GPU, and VPU controllers), NVCC_3V3 (for 3.3V IO), NVCC_1V8 (for 1.8 V IO), NVCC_DRAM (DRAM IO), VDDA (1.8 V analog) and NVCC_SNVS (1.8 V for SNVS/RTC IO). Depending on the application requirements, there might be additional supplies needed, for example NVCC_SD2 (supply for SDHC2 interface). This application note describes a multi-PMIC design using TPS65219+LP8733 PMICs to power i.MX 8M Plus and DDR4. For LPDDR4, TPS65219 is combined with a discrete Buck.

Note

The end user is responsible for validating the NVM settings for proper system use including any safety impact. This document does not provide information about the electrical characteristics, or the functionality of the device. For this information and the full register map, refer to the corresponding device data sheet. In the event of any inconsistency between any user's guide, application note, or other referenced material, the data sheet specification is the definitive source.

2 Power Delivery Networks (PDNs)

This section details how the TPS65219*0C* and LP8733*4F* power resources are connected to the processor voltage domains and peripherals. All the i.MX 8M Plus power domains except VDD_SOC are supplied by the primary PMIC (TPS65219). The secondary PMIC (LP8733) can be replaced with an external 0.85V Buck regulator if preferred. Some of the external peripherals like uSD card and Ethernet PHY are optional and might not be needed for the end product. These peripherals are included in the PDN as an example. The reference PDN has a 3.3 V input supply and uses an external 3.3 V power-switch to connects the 3.3 V pre-regulator to the processor 3.3 V IO voltage domain. All the PMIC rails, except the ones configured as load-switch or bypass, can be supplied by either 5 V or 3.3 V.

Note

TPS65219*0C* is a factory programmed device and TPS65219*05* is the user-programmable version.

2.1 TPS652190C Power Rails Configuration

- The three Buck converters (Buck1, Buck2, Buck3) supports dynamic voltage scaling and are used to supply the VDD_ARM, NVCC_DRAM and NVCC_1.8V (1.8V IO) respectively. Buck2 is configured as 1.2V when using DDR4 and 1.1V when using LPDDR4.
- LDO1 is configured as bypass to supply the SD card interface. The output voltage of this LDO is set by the VSEL_SD digital pin. An external pull-down resistor on VSEL_SD sets output voltage to 3.3 V initially. After the power-up sequence, the processor can set VSEL_SD high to select 1.8 V level as needed for high-speed card operation per SD specification. This bypass configuration allows control of the LDO1 voltage from 3.3V to 1.8V without the need to establish I2C communication. The bypass configuration on LDO1 requires connecting the input supply pin (PVIN_LDO1) to 3.3V.
- LDO2 is configured as load-switch and used to supply the uSD card socket. Since this rail is configured as a switch, it requires 3.3 V input supply to output 3.3 V.

- LDO3 is configured as a standard LDO with 1.8 V output voltage and it is used to supply NVCC_SNVS for applications that do not use the SNVS low power mode. This rail is enabled first in the power-up sequence.
- LDO4 is a low noise LDO used to supply the 1.8 V analog domain.

Note

For a detailed description of the default TPS652190C register settings, refer to the Technical Reference Manual SLVUCV3

2.2 LP87334F Power Rails Configuration

- Buck1 and Buck2 are configured in multi-phase to support higher current required for VDD_SOC. This PMIC rail supplies SoC logic, DRAM controller, GPU, and VPU controllers (VDD_SOC, VDD_VPU, VDD_GPU, VDD_DRAM).
- LDO1 and LDO2 are used for peripherals. They are configured to output 2.5V and can be used to supply the VPP rail of the DDR4 memory and the 2.5V rail of the Ethernet PHY.

Note

For a detailed description of the default TPS652190C register settings, refer to the Technical Reference Manual SNVU881

Table 2-1. Power Delivery Networks (PDNs)

PMIC	Memory Type	Power Delivery Network (PDN)
TPS65219*0C* + LP8733*4F*	DDR4	Section 2.3
TPS65219*xx* + 0.85V discrete Buck	LPDDR4	Section 2.4
TPS65219*05* user-programmable PMIC	Any	Section 5

2.3 Powering i.MX 8M Plus and DDR4

This section shows the TPS652190C and LP87334F powering the i.MX 8M Plus, LPDDR4 and peripherals.

Note

Refer to Section 3 to learn more about how this PDN can be modified to support SNVS low power mode.

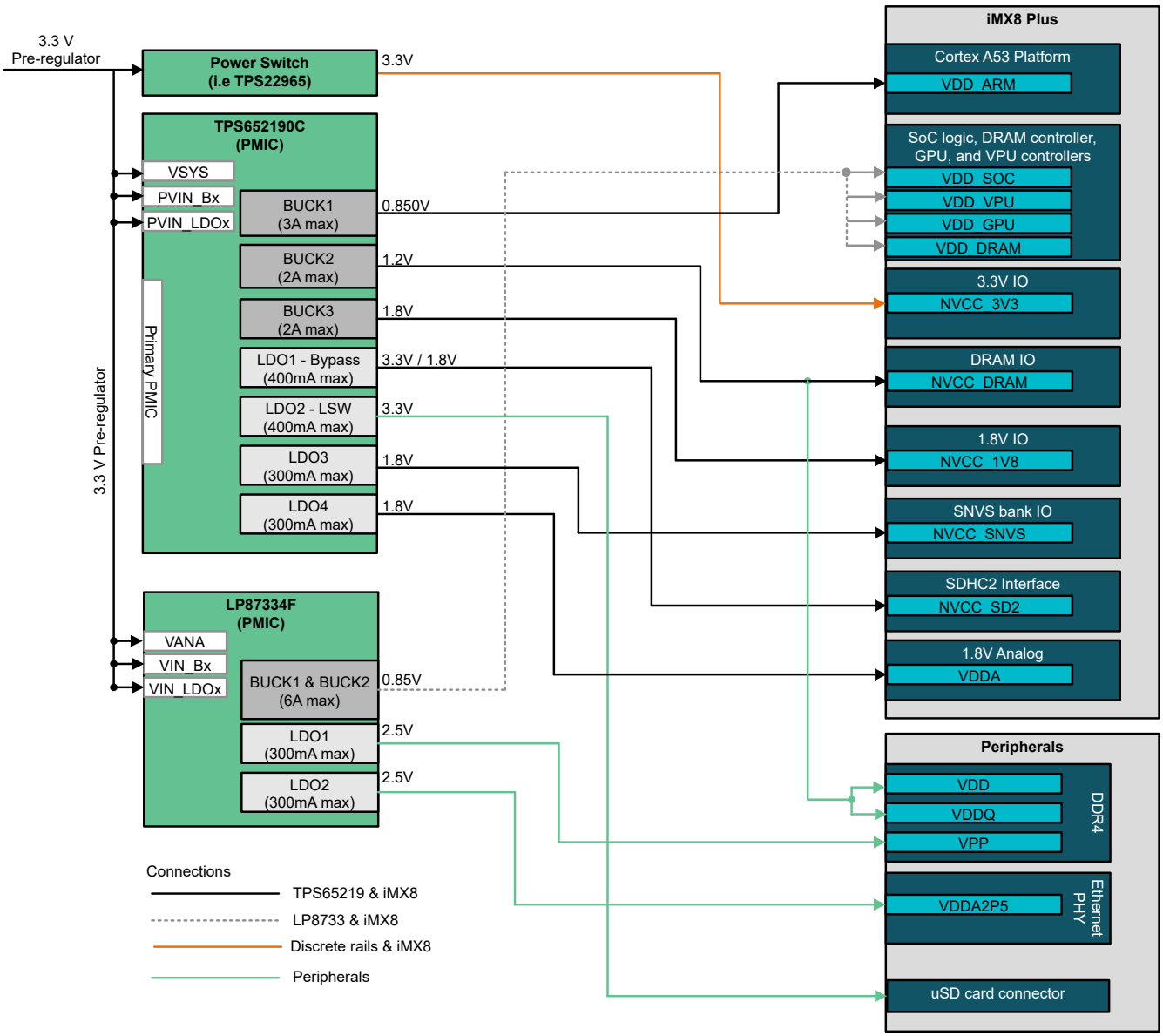

Figure 2-1. TPS652190C Powering i.MX 8M Plus and DDR4

2.4 Powering i.MX 8M Plus and LDDR4

This section shows an example of how the TPS6521905 PMIC and 0.85 V discrete power switch can power the i.MX 8M Plus, DDR4 and peripherals. TPS6521905 is a user-programmable PMIC that comes with all the rails disabled by default and can be customized to meet the requirements of different use cases.

Note

Refer to Section 3 to learn more about how this PDN can be modified to support SNVS low power mode.

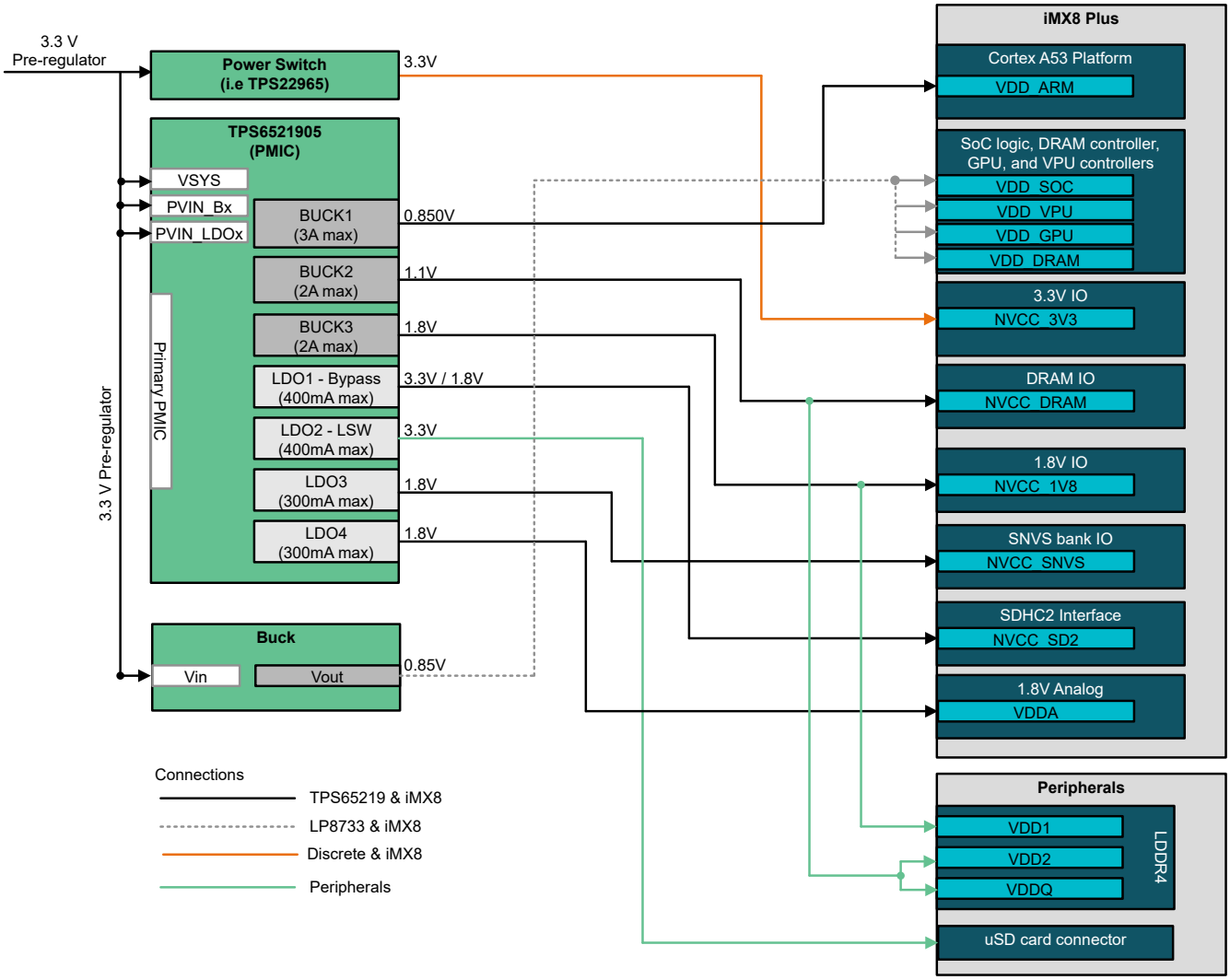

Figure 2-2. Powering i.MX 8M Plus and LPDDR4

2.5 PMICs Digital Configuration

This section describes the configuration of the TPS652190C and LP87334F digital pins.

Table 2-2. TPS652190C Digital Pins

	Pin Name	Function	Polarity/Operation
Inputs	VSEL_SD	Sets LDO1 output voltage	Low: LDO1 = 3.3V (requires PVIN_LDO1=3.3V) High: LDO1 = 1.8V
	MODE/STBY	Selects switching mode	Low: Bucks operate in auto-PFM High: Bucks operate in forced-PWM
	MODE/RESET	COLD reset	High: normal operation Falling edge: COLD reset
	EN/PB/VSENSE	PMIC enable	Low: PMIC OFF (Initilize State) High: PMIC ON
Outputs (open-drain)	nRSTOUT	Reset output (open-drain)	Goes high at the end of the PMIC power-up sequence. Can be used to drive POR_B
	nINT	Reset output	High: normal operation Low: interrupt fault detected
	GPIO	Enables secondary PMIC (LP87334F)	Enabled by default, part of the PMIC sequence. Refer to power-up/power-down timing diagram.
	GPO1	General purpose output	Enabled by default, part of the PMIC sequence. Refer to power-up/power-down timing diagram.
	GPO2	Enables external 3.3V power switch	Enabled by default, part of the PMIC sequence. Refer to power-up/power-down timing diagram.
I2C	SCL	I2C clock	NA
	SDA	I2C data	NA

Table 2-3. LP87334F Digital Pins

	Pin Name	Function	Polarity/Operation
Inputs	EN	PMIC enable pin	Low: PMIC OFF High: PMIC ON
Outputs (open-drain)	PGOOD	configured in continuous mode	see section "7.3.8.1.2 PGOOD Pin Continuous Mode" in LP8733 data sheet
	GPO	general-purpose digital output	Enabled by default, part of the PMIC sequence. Refer to power-up/power-down timing diagram.
	nINT	interrupt output	High: normal operation Low: interrupt fault detected
	CLKIN/GPO2	general-purpose digital output	Enabled by default, part of the PMIC sequence. Refer to power-up/power-down timing diagram.
I2C	SCL	I2C clock	NA
	SDA	I2C data	NA

2.6 Power-Up Sequence

This section shows the power-up sequence. The primary TPS65219 PMIC uses the GPIOs to enable the secondary PMIC and external discrete components.

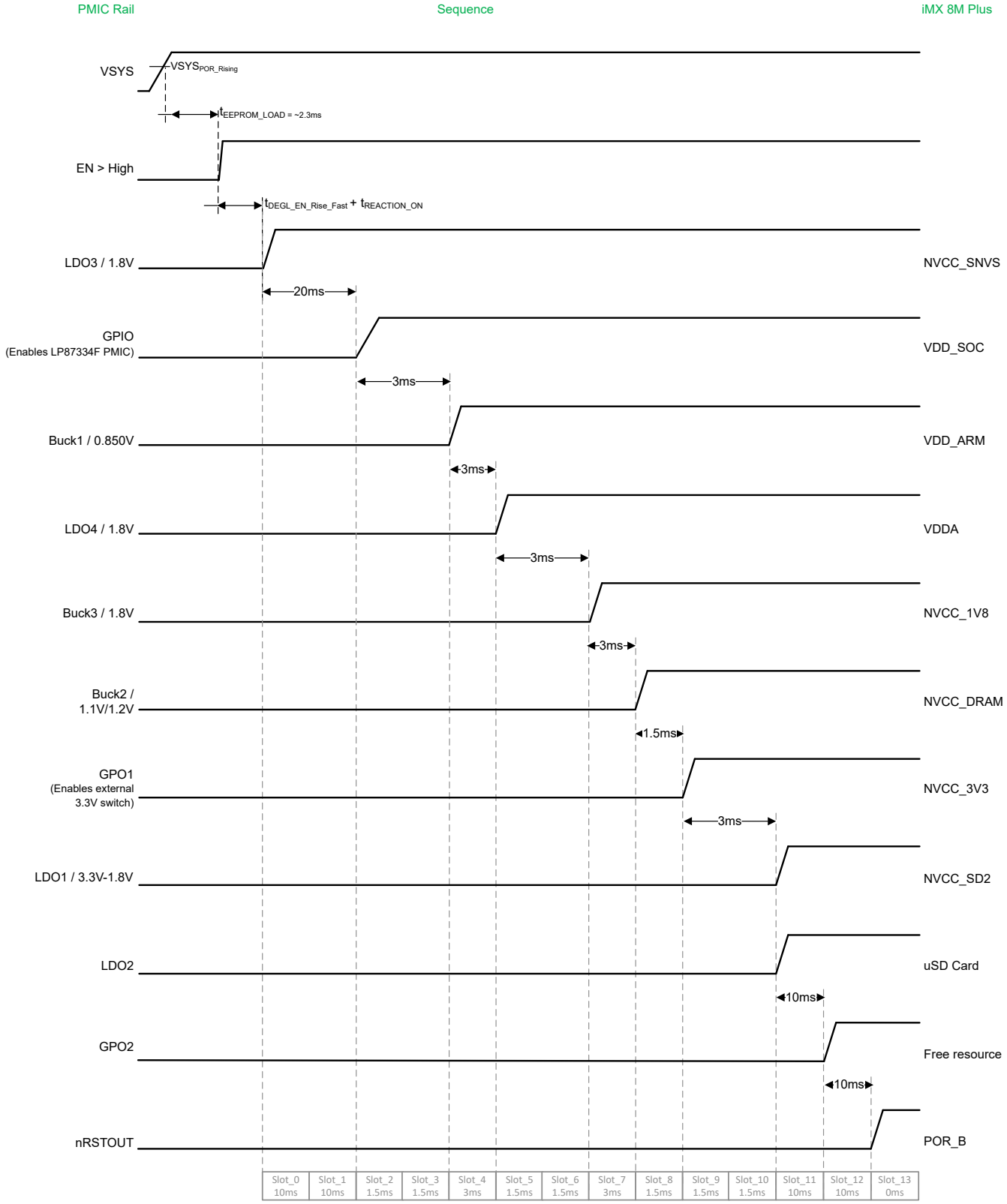

Figure 2-3. Power-Up Sequence

2.7 Power-Down Sequence

This section shows the power-down sequence which can be triggered by software (I2C_OFF_REQ) or hardware (by pulling the EN pin low).

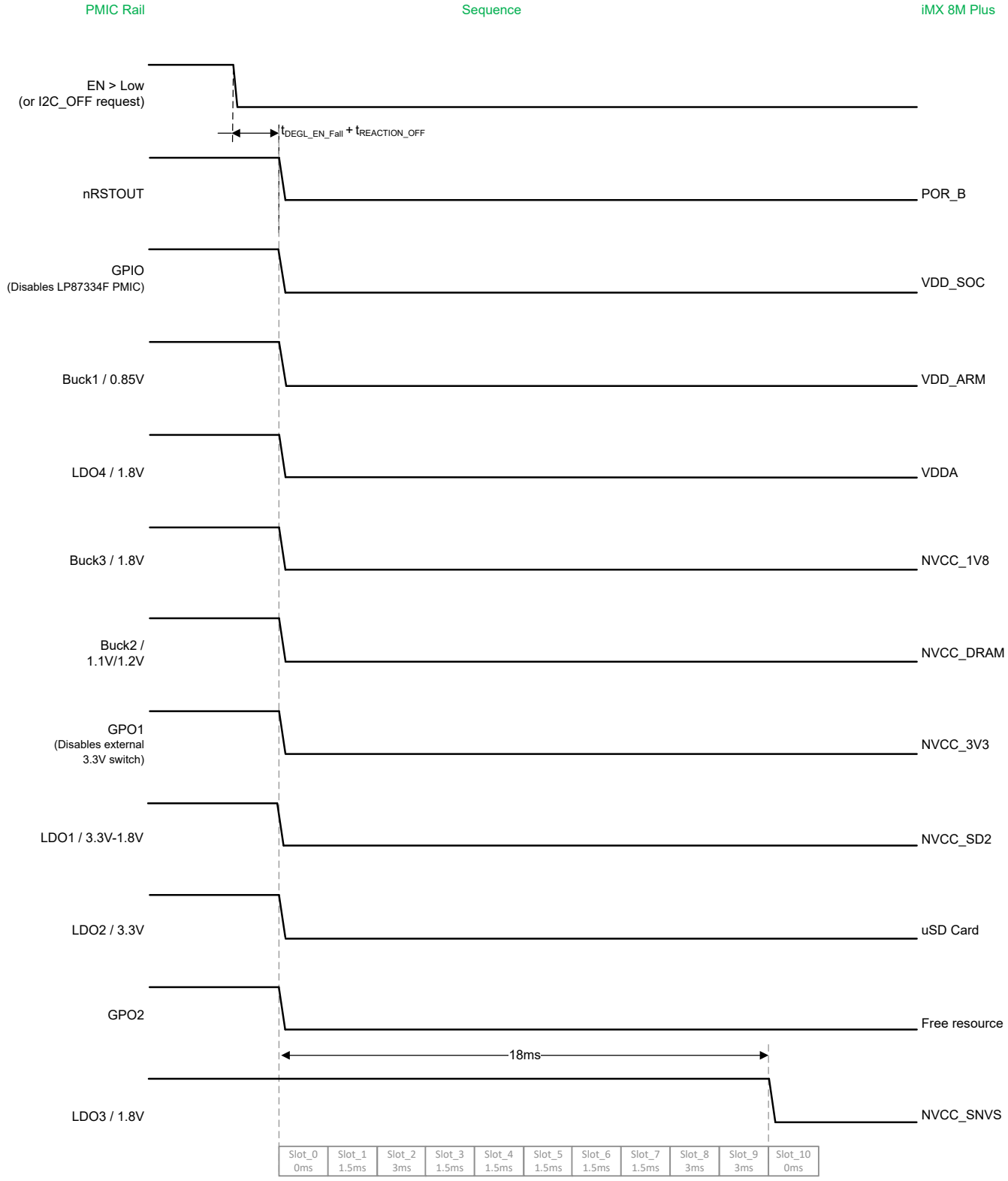

Figure 2-4. Power-Down Sequence

3 Supporting i.MX 8M Plus Low Power Modes

i.MX 8M Plus supports multiple Low Power Modes but not all them affects the PMIC power supplies. This means, some of the low power mode s requires all the PMIC rails to either stay ON or OFF. For example, in RUN Mode and IDLE, all the PMIC rails can stay ON. In OFF Mode, all PMIC rails are turned OFF.

However the SUSPEND and SNVS Modes require specific rails to stay ON while keeping the remaining PMIC rails OFF. These low power modes are optional and not used in some applications. Here are some guidelines to support the low power modes when needed:

Suspend Mode

- In this mode, all the clocks are off and unnecessary power supplies are off. Buck1 which supplies the VDD_ARM can be turned OFF by software (I2C write to register field BUCK1_EN) or by hardware (only supported when the PMIC MODE/STBY pin is configured as STBY and the Standby state is configured to turn off Buck1).

SNVS Mode

This mode is also called the RTC mode and only the SNVS domain remains on to keep RTC and SNVS operating.

- Option 1: re-configuring the MODE/STBY pin from *MODE* only to *MODE&STBY* and configuring the Standby state to keep LDO3 ON and the remaining rails OFF. This allows to use the MODE/STBY pin to turn-OFF all PMIC rails except LDO3 to support SNVS Mode. In this scenario, the SNVS mode can be triggered from Active state (after the PMIC finishes the default power-up sequence).
- Option 2: Using an external always ON LDO with power-good that can supply the NVCC_SNVS domain and enable the TPS65219 PMIC. In this use case, LDO3 becomes a free 300mA power resource.

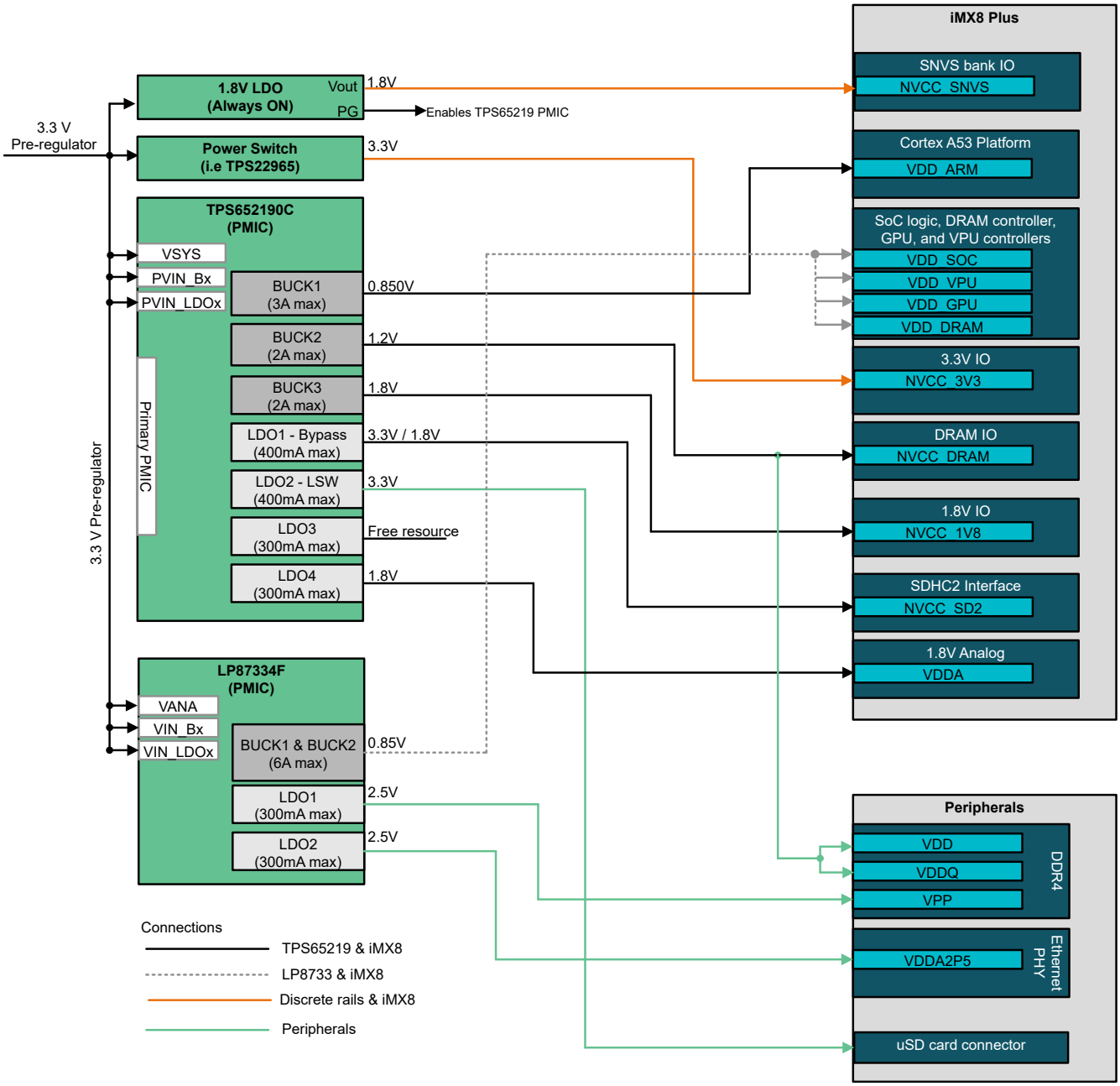

Figure 3-1. Powering i.MX 8M Plus and DDR4 - Supports SNVS Low Power Mode

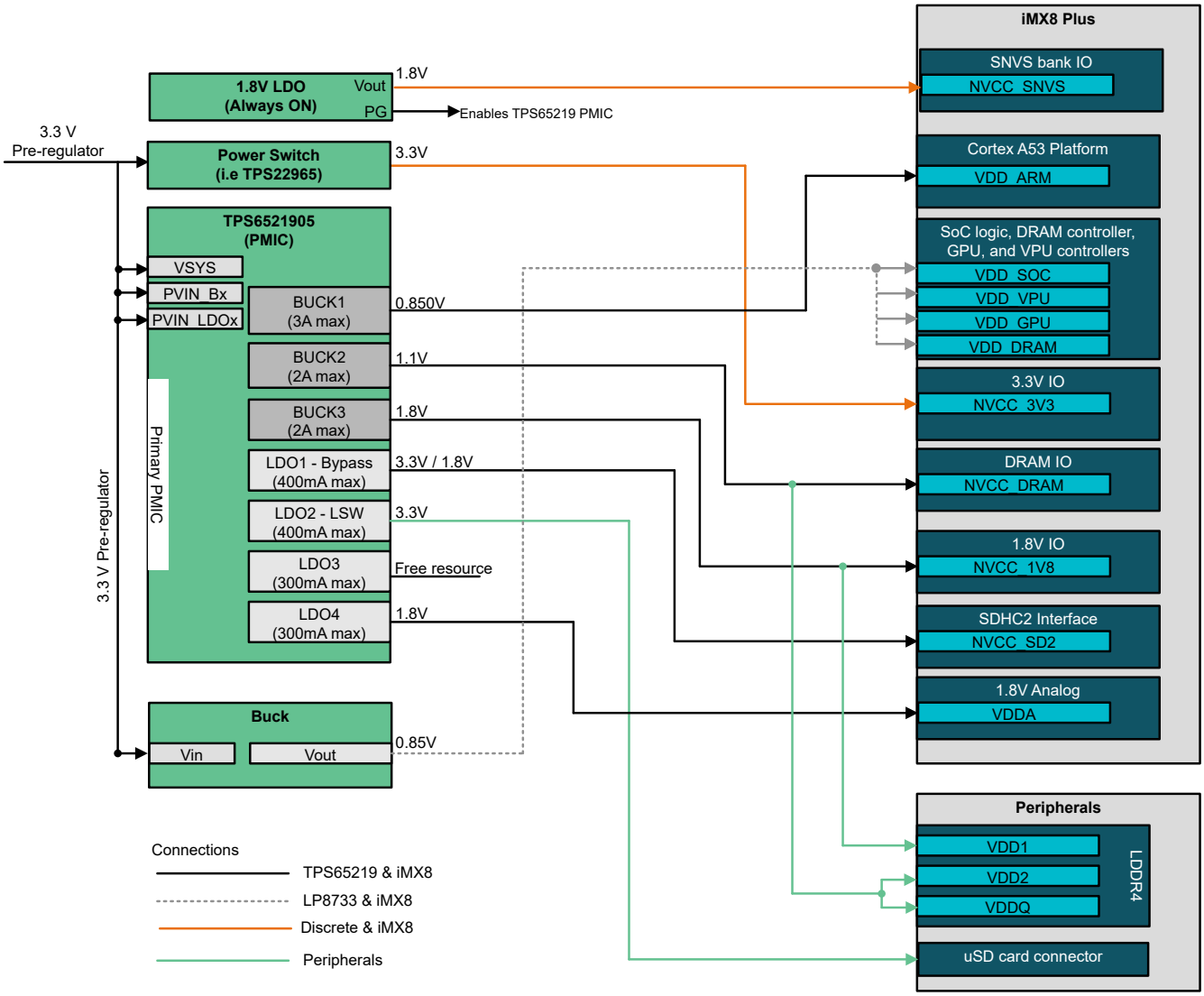

Figure 3-2. Powering i.MX 8M Plus and LDDR4 - Supports SNVS Low Power Mode

4 PMIC Schematic Example

Figure 4-1 shows an example schematic for the minimum required components of the two PMIC solution. This schematic does not include the external discrete that supplies the 3.3V IO. The second PMIC (LP8733) is optional and can be replaced with a discrete Buck when using LPDDR4.

The required output capacitance of the Buck converters in the TPS65219 PMIC is defined based on the configured switching mode and bandwidth. The TPS65219**0C** NVM is configured for quasi-fixed frequency and high bandwidth which requires a minimum of 30uF local output capacitance. 47uF output capacitance per Buck is typically used. Table 4-1 shows the minimum local capacitance and maximum total capacitance for each configuration setting.

Note

The POR_B pin of the i.MX 8M Plus can be driven with an AND gate of the TPS65219_nRSTOUT and the LP8733_PGOOD.

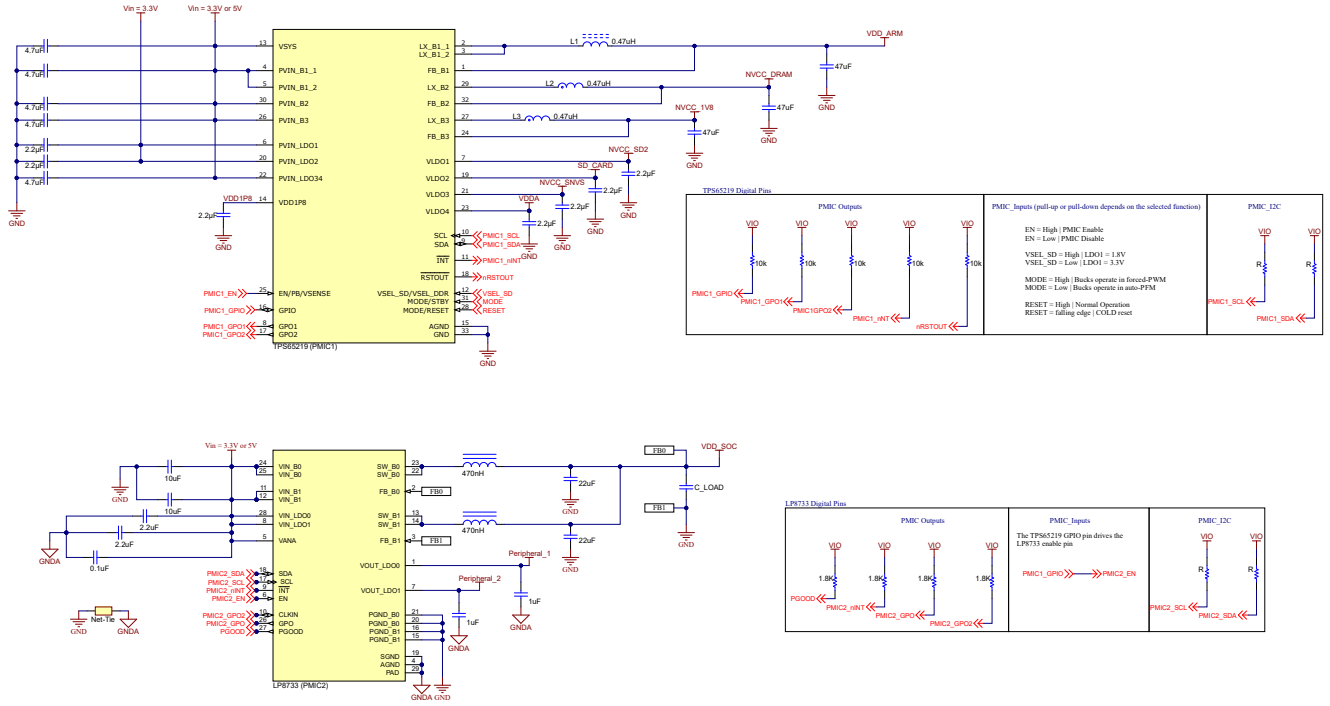

Figure 4-1. Example PMIC Schematic

Table 4-1. TPS65219 Buck output capacitance

Switching Mode Selection	Bandwidth Selection	Spec parameter	Capacitance	
Register Field: BUCK_FF_ENABLE	**Register fields: BUCK1_BW_SEL, BUCK2_BW_SEL, BUCK3_BW_SEL**		**Min (local capacitance)**	**Max (local + point of load)**
Quasi-fixed frequency (auto-PFM or forced-PWM)	Low Bandwidth	COUT	10 uF	75 uF
	High Bandwidth	COUT_HIGH_BW	30 uF	220 uF

Note

For more information about the external component requirements refer to the device data sheet.

5 TPS6521905 User-Programmable Version

Figure 5-1 shows the supply options that are available. If none of the available pre-configured orderable part numbers (OPNs) meet the application requirements or minor changes to the default register settings are needed, a custom NVM is required. For high volume opportunities, TI creates a new orderable part number with custom NVM settings. For low volume opportunities, TI's customers can use the resources listed in Table 5-1 to program the PMIC NVM memory in a production line or through third party programming service. To assist with the PMIC programming, TI facilitates a configuration file with the custom NVM settings that can easily be loaded into the PMIC NVM.

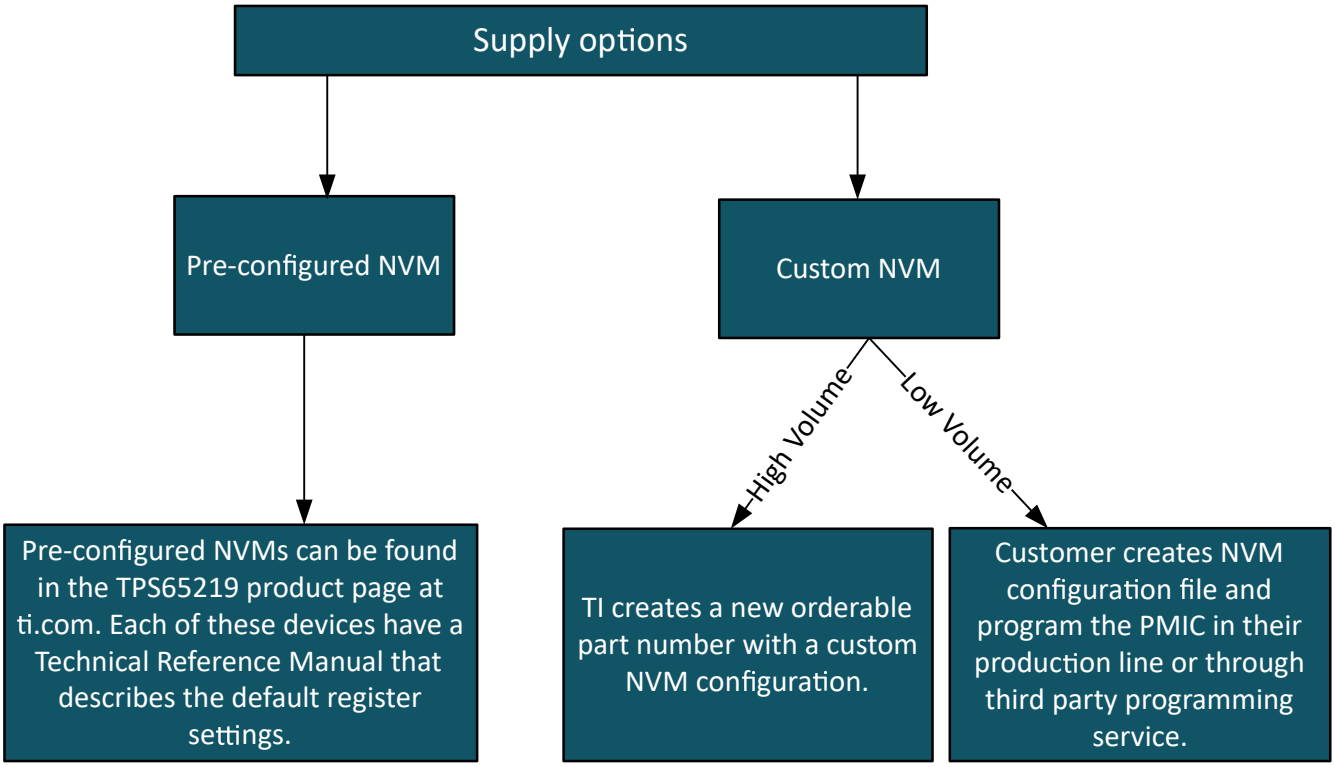

Figure 5-1. Supply Options

Table 5-1. TPS6521905 Programming Resources

Resource	Link
Programming Guide	TPS65219 Non-Volatile Memory (NVM) Programming Guide
Graphical User Interface (GUI)	TPS65219 graphical user interface
Socketed EVM	TPS65219 non-volatile memory (NVM) programming board
TPS6521905 product page	User-programmable power management IC (PMIC) with three step-down DC/DC converters and four LDOs

6 Summary

This application note described an example of how the TPS65219 PMIC resources can be configured to meet the power/sequence requirements of the iMX 8M Plus processor and principal peripherals. For any PMIC questions or technical support, use the Power Management E2E design support forum.

7 References

- Texas Instruments, *TPS65219 Integrated Power Management IC for ARM® Cortex—A53 Processors and FPGAs*
- NXP Semiconductors, *i.MX 8M Plus Applications Processor Data Sheet for Industrial Products*

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