Application Note

Improving Thermal Performance for Integrated FET Drivers

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ABSTRACT

When designing systems with integrated FET drivers, thermal performance can be a major consideration if users need the BLDC driver to operate with the most efficiency. At the most basic level, driving significant amounts of current from an integrated FET driver can only be possible if the device settings and parameters are optimized. This application note presents lab data showing how several of the customizable parameters on Texas Instruments' DRV8316 and DRV8317 affect the thermal performance of the devices.

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Trademarks

1 Introduction

Some of Texas Instruments' integrated FET motor drivers include thermal calculators that can be found on TI.com. These can be used to predict thermal performance based on system parameters, but lab data can provide additional context for the information presented by the data sheet and calculator. This application note provides real-world data explaining how settings such as PWM frequency, slew rate, and electrical characteristics affect the total power loss during operation. This document also profiles how the DRV8317 heats up over time during operation. Lastly, this application note contains design recommendations to assist in creating products with improved thermal performance.

Throughout this application note, two devices are the subject of the lab tests:

- **DRV8317**
  The DRV8317 has a small footprint and thermal characteristics that make the DRV8317 a smart design choice for low voltage and small form factor applications. The integrated features further reduce board size and bill of materials cost, making design easier.
- **DRV8316**
  The DRV8316 is similar to DRV8317, but the DRV8316 has higher power output capabilities and can include an integrated buck regulator.

2 Power Loss and Performance Expectations

First, the power loss equations that can be used to simulate thermal performance are detailed. There are several parameters which contribute to the thermal dissipation of an integrated FET driver. The most influential factor is the internal $R_{ds(on)}$ of the device, which represents the drain to source resistance of an internal FET. When driving high current, the average power loss due to this resistance (referred to as conduction loss) is the primary contributor to the total power loss. Each of the types of loss is explained below for both trapezoidal and FOC control.

Conduction Loss

$$P_{con} = 2 \times I^2_{pk(trap)} \times R_{ds,\,(on)(TA)} \quad (1)$$

$$P_{con} = 3 \times I^2_{rms(foc)} \times R_{ds,\,(on)(TA)} \quad (2)$$

$R_{ds(on)}$ is also temperature-variant. For example, $R_{ds(on)}$ increases as the temperature of the driver increases, and contributes to more power loss until a point of saturation. This is why the thermal data shown in the next section was taken several minutes after the driver reached the desired output current. In addition to conduction loss, switching loss and body diode loss can contribute to the total power loss of the device. Switching loss refers to the loss due to slewing as the FET turns on or off, while body diode loss refers to the loss due to current flowing through the FET's body diode during dead time. These are calculated using the following equations:

Switching Loss

$$P_{sw} = I_{pk(trap)} \times V_{pk(trap)} \times t_{rise/fall} \times f_{PWM} \quad (3)$$

$$P_{sw} = 3 \times I_{RMS(FOC)} \times V_{pk(FOC)} \times t_{rise/fall} \times f_{PWM} \quad (4)$$

Body Diode Loss

$$P_{diode} = 3 \times I_{pk(trap)} \times V_{f(diode)} \times t_{deadtime} \times f_{PWM} \quad (5)$$

$$P_{diode} = 6 \times I_{RMS(FOC)} \times V_{f(diode)} \times t_{deadtime} \times f_{PWM} \quad (6)$$

These power losses depend on other parameters such as slew rate and PWM frequency, which is discussed later in the lab data. More information on each of these equations can be found in the *Thermal considerations for integrated MOSFET drivers* video, which explains all of the power loss sources in systems using integrated FET drivers.

Before looking at the data, some predictions can be made about the performance of the DRV8316 and DRV8317. Since the DRV8316 has a lower $R_{ds(on)}$ value, the expectation is that DRV8316 to have an overall cooler temperature at the same output level when compared with the DRV8317. Additionally, based on the previous equations, see the following:

- Higher slew rate means that t_{rise} or t_{fall} decreases, which means the device can experience less power loss and run cooler than at a lower slew rate.
- Higher PWM frequency increases switching and diode losses since the FETs switch more often per second (and thus must go through the power loss-intensive Miller zone more often), causing the device to run hotter than at a lower PWM frequency.
- The FOC commutation algorithm is the most efficient method of commutating a BLDC motor, so the FOC needs to produce better thermal performance than trapezoidal control, which is the least efficient algorithm.

However, there are potential drawbacks to each of these settings, which is explained more in a later section.

Lastly, each device is rated to operate in a range of junction temperatures. Due to the nature of PCB design, the junction temperature is difficult to measure. The lab data presented in this application note refers to the package temperature. These two values can differ due to a variety of factors, such as the thermal resistances, ambient temperature, and available area for the heat to conduct into different media and eventually into the ambient environment. Detailed testing and analysis is required to correlate the two values, but for more information, please refer to the following application note: *Semiconductor and IC Package Thermal Metrics* . This resource is also listed in some data sheets next to the Thermal Information section.

Based on these predictions and the theory discussed previously, users need to consider real-world lab data produced using the DRV8316 and DRV8317 EVMs.

3 Lab Data and Analysis

3.1 Current Output, $R_{ds(on)}$, and PWM Frequency

The first data set shows how both output current and PWM frequency affect the temperature of the device package. These measurements were made using the DRV8317 and the following parameters: the supply voltage was set to 17.4V, the slew rate was set to a maximum value of 200V/µs, the motor was characterized while unloaded, and the measurements were made within 10-60 seconds of the device achieving the output current. Note that the internal linear regulator of the DRV8317 contributes to the power loss of the device, and this output was consistent between tests.

Table 3-1. DRV8317 Results: PWM Frequency and Output Current

PWM Frequency (kHz)	Output Current RMS (A)	Package Temperature (°C)
20	2.99	112.6
30	3.02	130.6
40	3.00	140
50	2.99	151.9
20	3.45	149.6
30	3.3	141
40	3.24	151.9
50	3.13	157

Table 3-1 shows the effects of both increasing PWM frequency and current in action. First, while holding the PWM frequency constant and comparing the package temperature with respect to the two different output current RMS values, the data show that a higher current output can significantly increase the temperature of the device. This is expected, as the conduction loss dominates at high current output, and is determined by the $R_{ds(on)}$ of the device. Second, while holding the output current RMS constant and comparing the package temperature with respect to increasing PWM frequency, the data show that high PWM frequency can also significantly increase the temperature of the device. This is expected from the switching and diode losses as discussed in the previous section.

Note that these data also show the device reaching towards the absolute maximum temperature threshold. While this threshold is typically 160 degrees Celsius according to the data sheet, device variation means that the threshold can be as low as 145 degrees Celsius or as high as 175 degrees Celsius. This can cause reliability issues across many devices when operating at these high current outputs. Thus, in practice, PWM frequency limits the amount of current which can be produced by the driver without causing permanent damage.

3.2 Slew Rate and Device

The slew rate of the voltage switching on the output phases of the device can also affect the contribution of switching losses to the overall power loss of the system. The expectation is that, given a constant current output and PWM frequency, a faster slew rate reduces the switching loss, and the device runs at a cooler temperature than with a slower slew rate. This is shown in Table 3-2. Note that voltage is roughly 17.414 to 17.416V in all tests, the motor was characterized while loaded, and the package temperature was measured 2 minutes after the target output current of around 3A RMS was achieved.

Table 3-2. DRV8316 Results: Fixed PWM While Increasing Slew Rate

PWM Frequency (kHz)	Output Current RMS (A)	Slew Rate (V/µs)	Package Temperature (°C, DRV8316)
20	3.00	25	108
20	2.95	50	82.4
20	2.98	125	68.6
20	2.95	200	66.2

Table 3-3. DRV8317 Results: Fixed PWM While Increasing Slew Rate

PWM Frequency (kHz)	Output Current RMS (A)	Slew Rate (V/µs)	Package Temperature (°C, DRV8317)
20	1.98	25	112.3
20	1.98	50	85.5
20	1.98	125	70.4
20	1.98	200	65.5

Sensorless Field Oriented Control (FOC) was used to drive the motor during the above experiment. As expected, the temperature of the device package decreased as the slew rate increased. However, while an even higher slew rate can be expected to further decrease the switching losses, designers must also keep in mind that other issues can occur. High slew rates can cause unwanted half-bridge shoot-through events through dV/dt coupling, as well as poor EMI performance through node ringing during switching. All of these drawbacks must also be considered when choosing the right slew rate for the application.

Additionally, see how the DRV8316 performs compared to the DRV8317. The DRV8316 has a lower $R_{ds(on)}$ value than the DRV8317, so we expect the DRV8316 to have lower conduction loss. Although the above experiment shows the DRV8316 running at around 3A RMS while the DRV8317 runs at about 2A RMS, the DRV8316 is cooler at each slew rate except 200V/µs (although the difference can be attributed to measurement error). Despite the significant difference in current output, the driver with the smaller $R_{ds(on)}$ ran cooler than the alternative, which shows how much conduction loss contributes to the overall temperature of the device. Note, however, that these two devices are meant for different applications. When comparing the thermal performance between two devices, designers need to consider motor drivers with similar operating power and recommended end uses. The DRV8316 is designed to be used in slightly higher-power applications than the 8317 for this reason.

3.3 Temporal Thermal Analysis

Lastly, the driver heats up over time. Based on the amount of time the application can require the motor driver to output high current, the temperature of the device changes. This affects different parameters of the device, especially the $R_{ds(on)}$ resistance. This resistance increases with higher temperatures, which increases the conduction power loss of the device. This continues until the resistance increase and device temperature saturates. Once the device disables the output, the temperature decreases rapidly. Figure 3-1 profiles the temperature over time. Any deviations in the trend are due to a variety of factors, such as measurement error or changes in motor parameters that can make the system more or less efficient.

Note

For this experiment, the DRV8317 was used with a 17.414V supply, 20kHz PWM frequency, 2.5A RMS output, and 200V/µs slew rate. The package temperature over time is plotted in Figure 3-1.

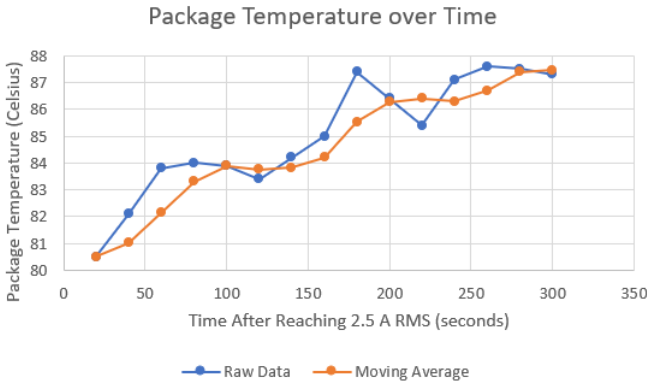

Figure 3-1. Package Temperature Over Time

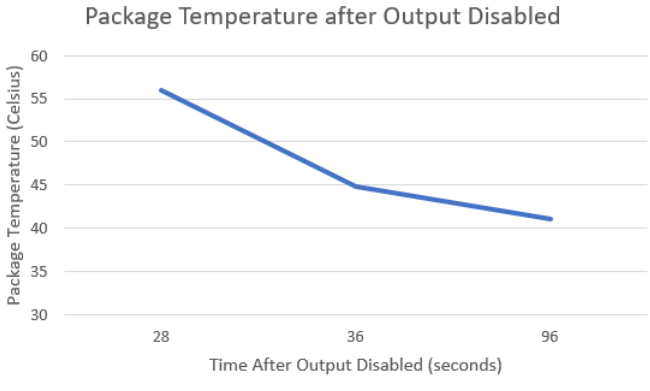

Figure 3-2. Package Temperature After Output Disabled

The device cools off rapidly due in part to the thermal dissipation through the connected copper planes. Since the output is disabled, the dominating conduction power loss is no longer a major contributor to the total power loss, and so the temperature cools quickly.

3.4 PCB Design

Images captured during this testing also show how heat dissipated across the PCB during device operation. As seen in the figures below, the part of the device package closest to the motor outputs (at the top of the package) was the hottest, which corresponds with the internal drain-to-source resistance of the phase half-bridge MOSFETs. Additionally, from the images observe the thermal gradient across the device package and the PCB. The largest gradient occurs between the device and the board. This is because the thermal pad on the bottom of the device is the primary route for thermal dissipation. As a result, TI recommends that thermally efficient board designs maximize the copper area connected to the thermal ground pad of the device. Although the thermal camera only reveals the heat dissipation on the surface of the board, the image shows the importance of effective PCB design for thermal performance. When comparing the thermal images with the layout design shown in the figure below, after the device package, the next area of the board with the highest temperature is to the bottom and to the left of the device. This region corresponds with most of the traces going from the driver to the rest of the circuit. These traces are very thin and are not surrounded by copper, which means there is not much area for heat to dissipate from the driver into the board and from the board into the environment. Meanwhile, the coolest areas of the board are to the top and right of the device package. These regions correspond with the phase outputs, VM supply, and ground, all of which consist of large copper planes. These planes allow heat to dissipate quickly across a large area.

Since most heat dissipates through the ground planes, note the importance of having a large, unimpeded area of ground copper on all layers directly under the device package. Traces reduce the area over which the heat can flow. This can be seen in the thermal images where heat builds up over the area with traces rather than flowing into the cooler copper planes. Thus, this data shows the effectiveness of large copper planes in action, as shown in Figure 3-3.

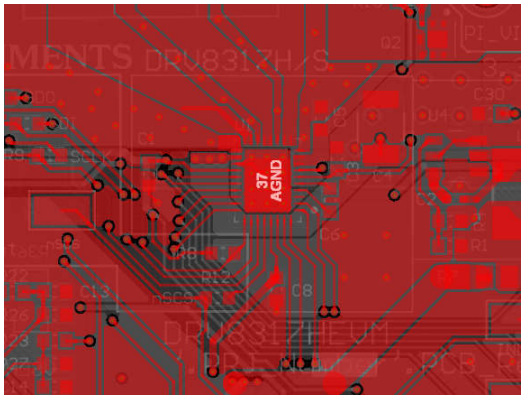

Figure 3-3. DRV8317HEVM Layout

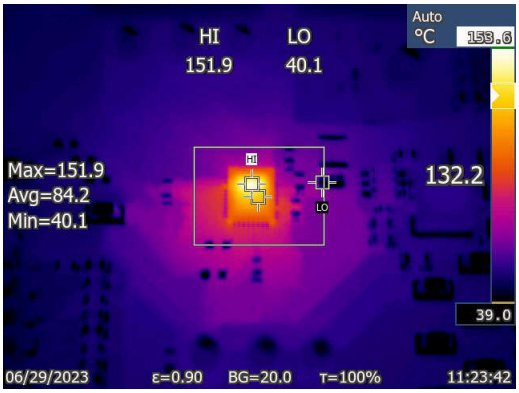

Figure 3-4. Thermal Image of DRV8317 at 50kHz PWM Frequency and 2.99A RMS

4 Thermal Design Recommendations

Based on the data provided in the previous section, this application note presents several recommendations for designers needing to maximize the thermal performance and efficiency of the integrated FET driver. First, within groups of equivalent power-level motor drivers, the integrated FET driver with the lowest $R_{ds(on)}$ value reduces conduction losses, which dominate total power loss at high current outputs. Second, to facilitate current output near the maximum of the device, TI recommends using a reasonable switching frequency based on the motor type with the highest slew rate possible that does not introduce EMI issues. Lastly, based on the diode loss equations, use as small a dead time as possible that still prevents cross-conduction events. These settings can reduce the overall temperature of the device at a given current, meaning the device can be able to reach higher current output before triggering an overtemperature shutoff (note that these devices are still limited by an overcurrent threshold). However, some systems can be susceptible to EMI due to ringing nodes caused by high slew rates, so designers must always be aware of the tradeoffs to create a robust system. Although not presented in this application note, current output from internal voltage regulators can also generate heat through added power loss. To reduce this power loss, avoid drawing significant current from these regulators in the rest of the circuit. Lowering the voltage input to these regulators can also reduce power loss by decreasing the voltage drop that needs to be made for the regulated output; however, split power supplies is not an available feature in every device. Refer to the data sheet for more information. Users can also refer to another application note on layout best practices.

Additionally, a thermally-optimized PCB design can significantly help with heat dissipation. The ground pad on the bottom of the device package needs to be connected to as much unimpeded copper as possible on several layers. Using simulated calculations from the available integrated FET driver thermal calculators available on ti.com, a small area of copper on a two-layer PCB results in a higher junction temperature than a large copper area on a four-layer PCB. The copper area needs to extend around the device as much as possible, with very few interruptions from routed traces, vias, or other components. Thermal vias must be used to stitch ground planes on one layer to another, and the vias need to be used extensively on the ground pad of the device footprint.

Another strategy for increasing the size of the copper ground plane around the device is to unify PGND and AGND into one solid ground plane, rather than attaching separate planes through a net tie. Users need to make sure that large current return paths do not cross directly under the device in the layout. However, this can create noise in the current sense amplifiers (if the current sense amplifiers are integrated in the driver, such as in the DRV8316 and DRV8317) and cause possible inefficiencies in sensorless commutation algorithms that use current monitoring. Finally, the copper connections between the motor driver and each phase output port needs to be as wide as possible, both to accommodate the large amounts of current and to provide additional routes for thermal dissipation.

Lastly, when testing the system's thermal performance, remember to keep these considerations in mind while working with integrated FET drivers:

- High PWM frequencies result not only in higher switching losses, but also reduced settling time for the CSA output. This can introduce noise into the current sense measurements, which can cause a false software current limit shutoff or inefficiencies in sensorless commutation.
- Noise on the output current can also affect maximum measurements made with an oscilloscope. An easier way to measure current output in the lab is to use the RMS value.
- To observe high current output from the driver, the motor needs to be loaded. This is due to the current being proportional to the torque provided by the motor.
- Make sure the voltage supply requirements of the motor are within the same range as the motor driver's recommended operating conditions. Operation outside of these ratings can cause damage to the device or inefficiencies that generate heat in the device package.
- When evaluating motor drivers for the application, a great place to start is by using one of Texas Instruments' evaluation boards and available GUIs. The DRV8316EVM and DRV8317EVM, along with the respective sensorless FOC GUIs, were used for testing for this application note. Please see the product page of each motor driver for more information.

5 Summary

Integrated FET drivers provide significant features and power capabilities within a small form factor, and the drivers can reduce PCB cost and complexity. At the same time, the integrated nature of the devices requires designers to consider the thermal performance of the system so that the drivers can provide more efficient performance. This application note explained various sources of power loss for integrated FET motor drivers, presented data captured in lab experiments, and provided recommendations based on that data. For more information on Texas Instruments integrated FET driver portfolio, refer to *Brushless DC (BLDC) motor drivers* . More content on thermal performance is available through videos and other design guides on ti.com.

6 References

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* , application note.
- Texas Instruments, *Thermal considerations for integrated MOSFET drivers* , video.
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* , application note.

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