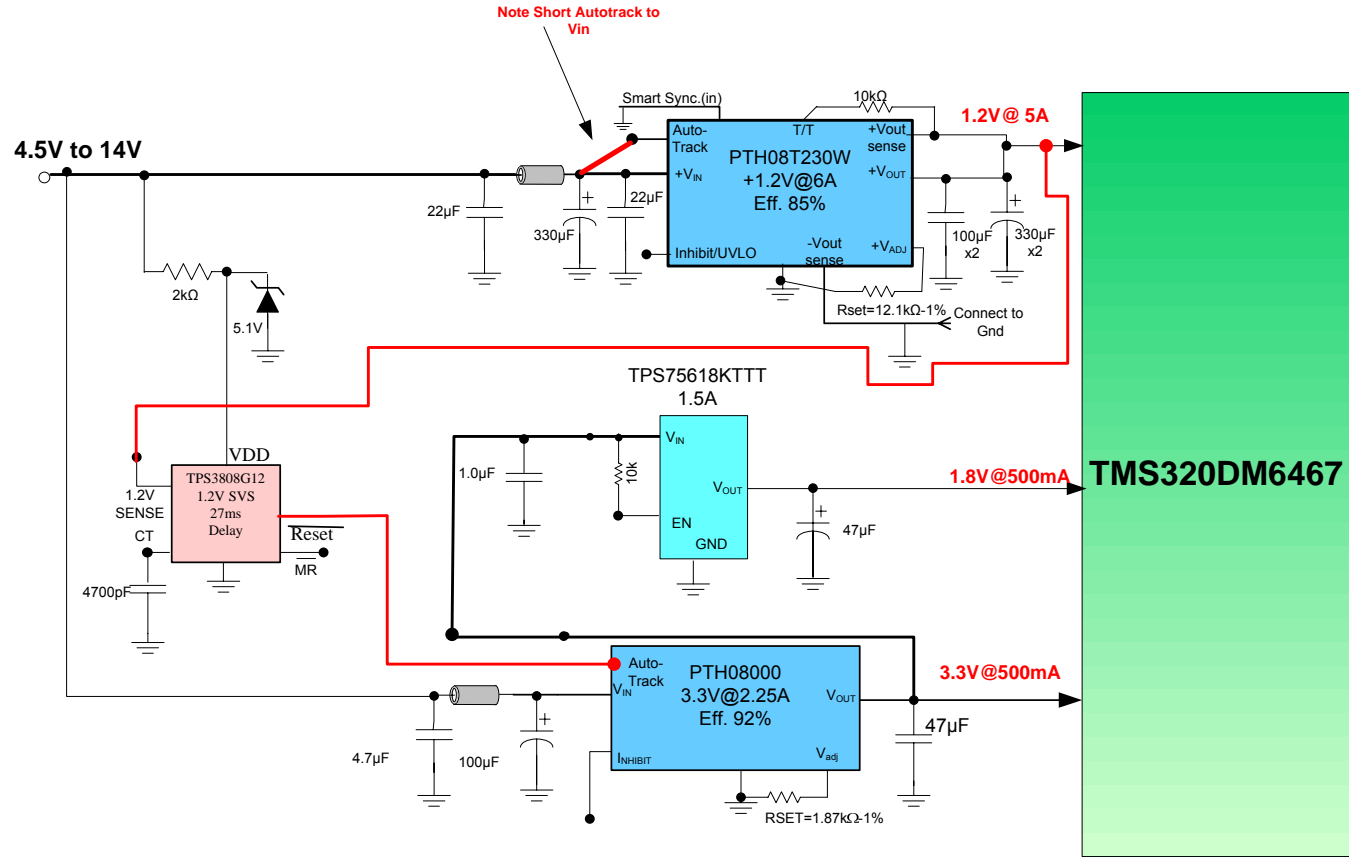


TMS320DM6467 Reference design



The DM6467 includes one core supply (CV_{DD}), and two I/O supplies— DV_{DD33} and DV_{DDR2} . To ensure proper device operation, a specific power-up sequence **must** be followed. Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start/Enable features. For more information on TI power supplies and their features, visit www.ti.com/processorpower.

Here is a summary of the power sequencing requirements:

- The power ramp order **must** be CV_{DD} before DV_{DDR2} , and DV_{DDR2} before DV_{DD33} —meaning during power up, the voltage at the DV_{DDR2} rail should never exceed the voltage at the CV_{DD} rail. Similarly, the voltage at the DV_{DD33} rail should never exceed the voltage at the DV_{DDR2} rail.
- From the time that power ramp begins, all power supplies (CV_{DD} , DV_{DDR2} , DV_{DD33}) **must** be stable within 200 ms. The term "stable" means reaching the recommended operating condition (see [Section 5.2, Recommended Operating Conditions](#) table).

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