

# High Performance Synchronous Buck EVM Using the TPS53114

## User's Guide



Literature Number: SLVU310

April 2009



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# High Performance Synchronous Buck EVM Using the TPS53114

## 1 Description

This user's guide contains background information for the TPS53114 as well as support document for the TPS53114EVM evaluation module. Also including the performance specifications, schematic and the bill of materials for the TPS53114EVM.

The TPS53114 is a single, adaptive on-time D-CAP2™ Mode synchronous buck controller. The part enables system designers to cost effectively complete the suite of various end equipments power bus regulators with a low external component count and low standby consumption. The main control loop for the TPS53114 uses the D-CAP2™ Mode which provides a very fast transient response with no external component. The TPS53114 also has a proprietary circuit that enables the device to adapt not only low equivalent series resistance (ESR) output capacitors such as POSCAP/SP-CAP, but also ceramic capacitors using the selectable CER pin. The part provides a convenient and efficient operation with conversion voltages from 4.5 V to 24 V and output voltages from 0.76 V to 5.5 V.

TPS53114 evaluation module is a high efficiency, single synchronous buck converter providing 1.05 V at 4 A from 5-V to 22-V input. This user's guide describes the TPS53114 EVM performance.

## 2 Electrical Performance

**Table 1. Electrical Performance**

SPECIFICATIONS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range ( $V_{IN}$ )		5	12	22	V
CH1	Output voltage			1.05		V
	Operating frequency	$V_{IN} = 12\text{ V}$ , $I_{out1} = 1\text{ A}$ , FSEL = L/H		350/700		kHz
	Output current range		0		4	A
	Over current limit	$V_{IN} = 12\text{ V}$		5		A
	Output ripple voltage	$V_{IN} = 12\text{ V}$ , $I_{out1} = 4\text{ A}$			12.8/10	mVp-p

### 3 Schematic

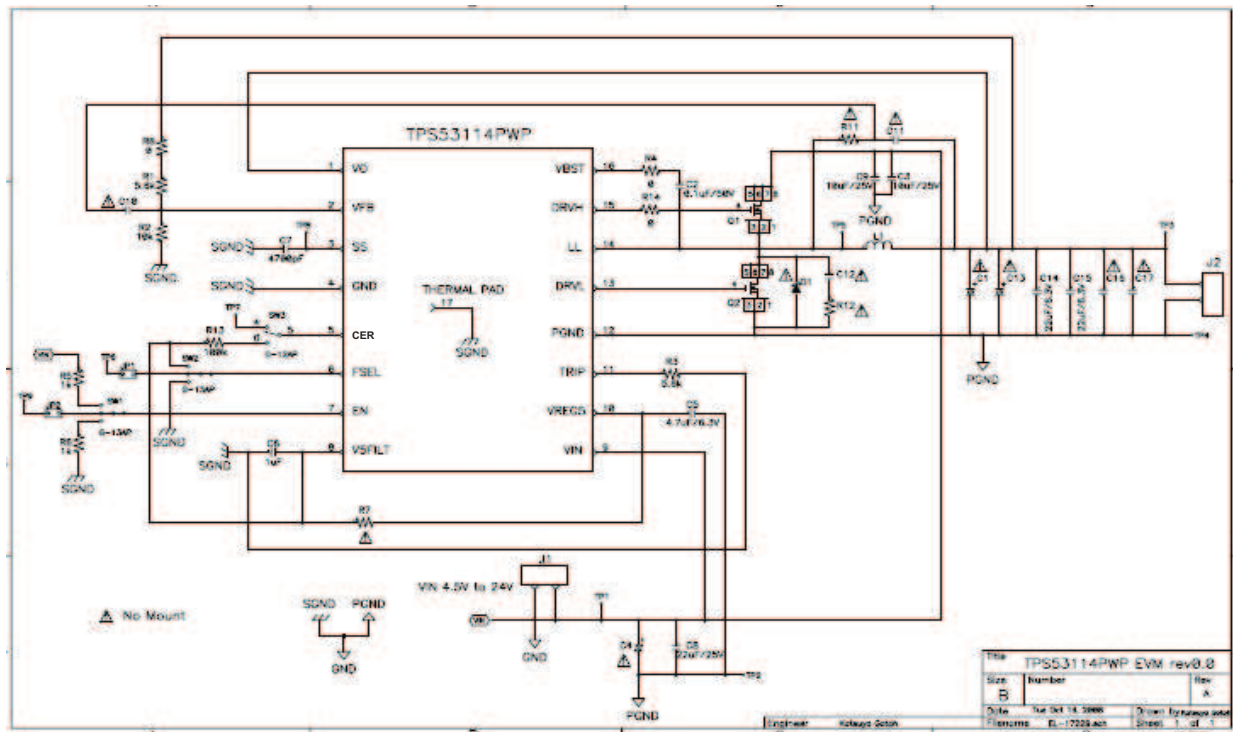


Figure 1. TPS53114 EVM Schematic Diagram

### 4 Test Setup and Results

This section describes how to properly connect, setup and use the TPS53114EVM. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, startup and switching frequency.

## 4.1 Test Setup

Connect test equipment and TPS53114 EVM board as shown in Figure 2.

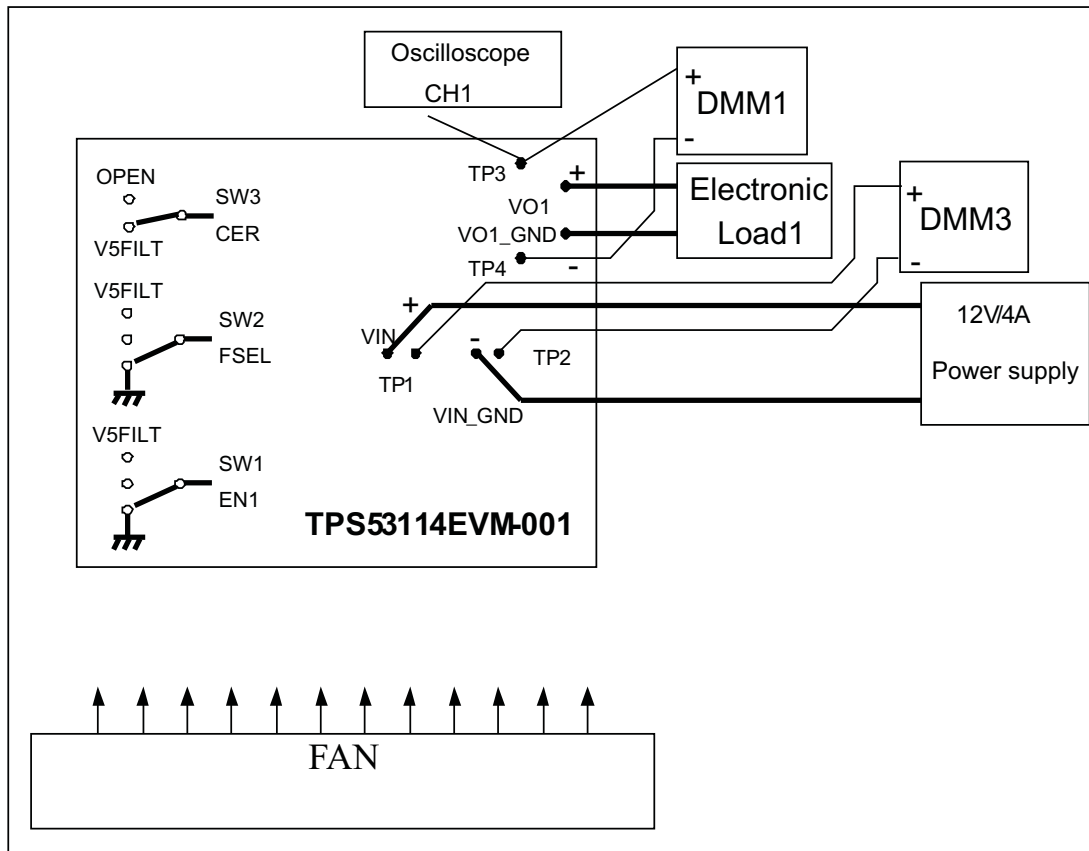
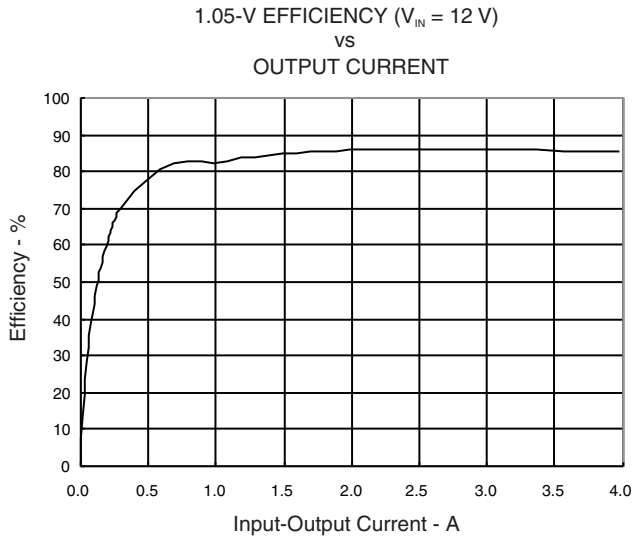


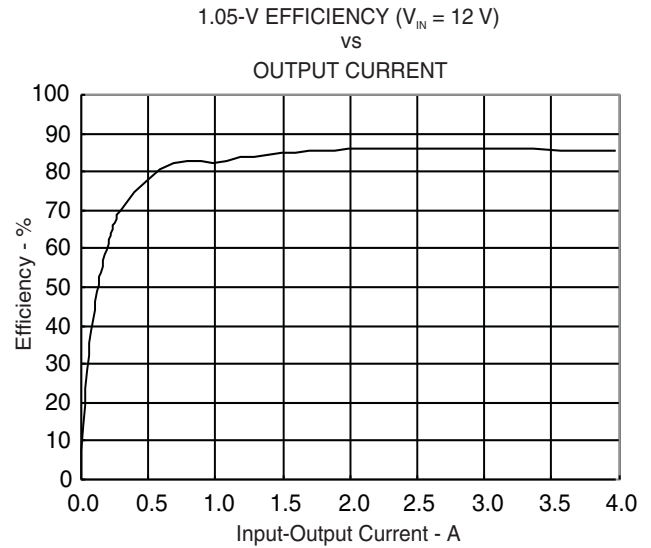
Figure 2. Equipment Setup for TPS53114 EVM Board

## 4.2 Test Procedure

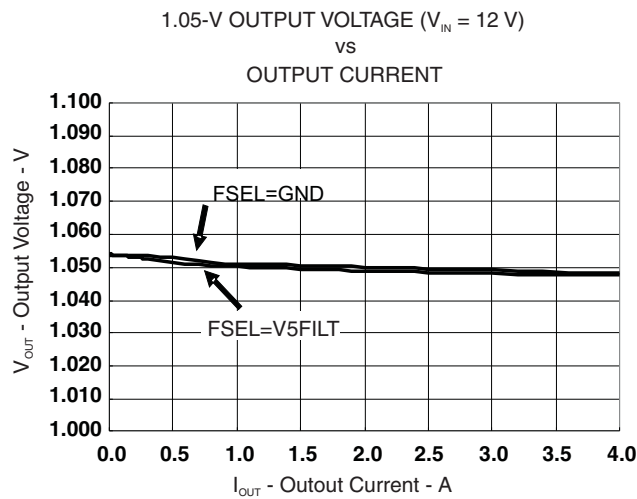
1. Make sure the switch SW1 (EN) is in "OFF" position.
2. Make sure the switch SW2 (FSEL) is in "LOW" position for switching frequency 350 kHz or in "HIGH" position for switching frequency 700 kHz.
3. Make sure the switch SW3 is in OPEN position for ceramic output capacitor use or in V5FILT position for low equivalent series resistance (ESR) output capacitors such as POSCAP/PS-CAP.
4. Apply appropriate  $V_{IN}$  voltage to VIN and VIN\_GND terminals.
5. Turn on SW1 (EN), CH-output will start up.



**Figure 3. Efficiency (FSEL = GND, 350 kHz Selection)**



**Figure 4. Efficiency (FSEL = V5FILT, 700 kHz Selection)**



**Figure 5. Load Regulation (350 kHz Selection at FSEL = GND, 700 kHz Selection at FSEL = V5FILT )**



### 4.3 Line Regulation

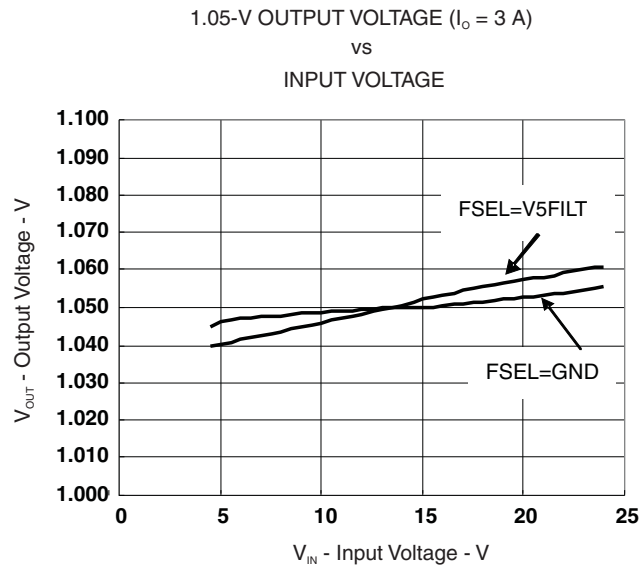


Figure 6. Line Regulation (350 kHz Selection at FSEL = GND, 700 kHz Selection at FSEL = V5FILT)

### 4.4 Load Transient Response

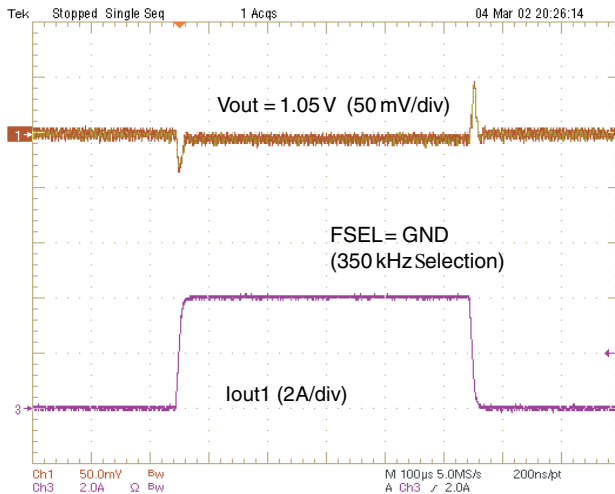


Figure 7. Transient Response (FSEL = GND, 350 kHz Selection)

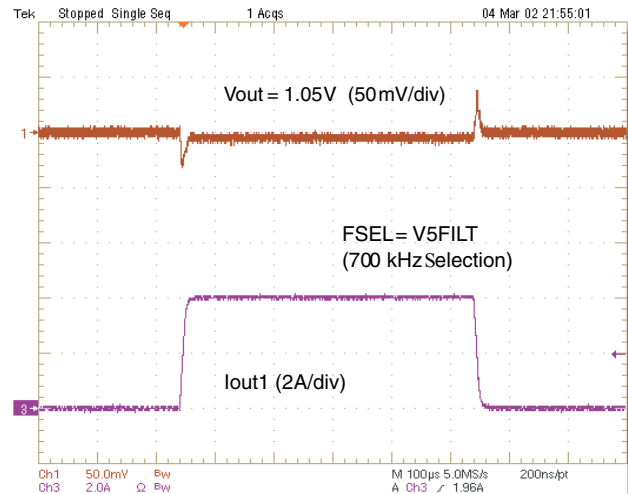
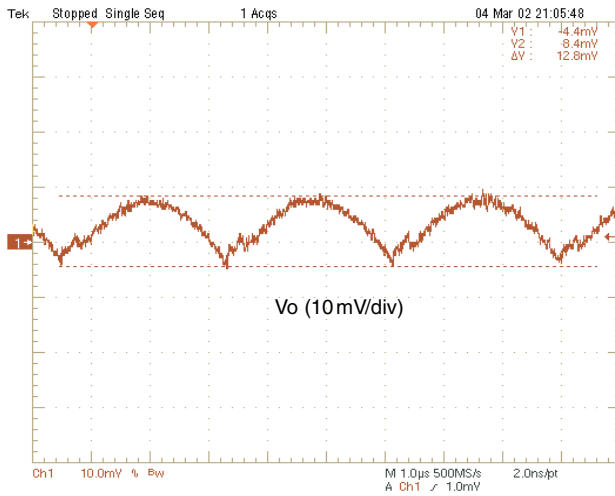


Figure 8. Transient Response (FSEL = V5FILT, 700 kHz Selection)

### 4.5 Output Voltage Ripple

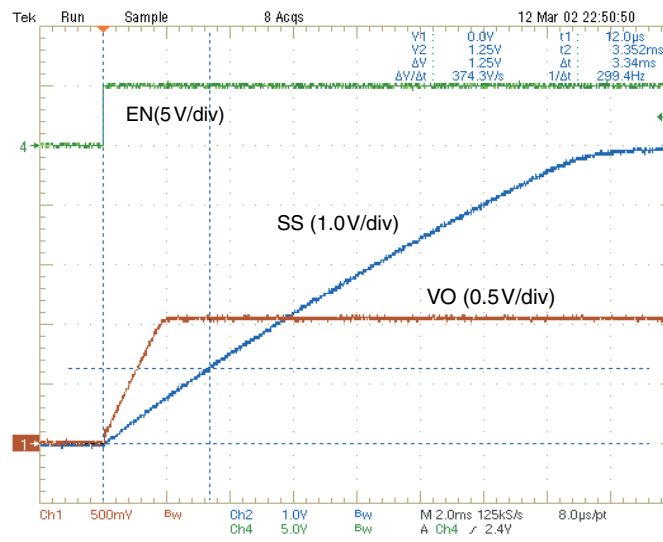


**Figure 9. Ripple Voltage**  
(FSEL = GND, 350 kHz Selection)



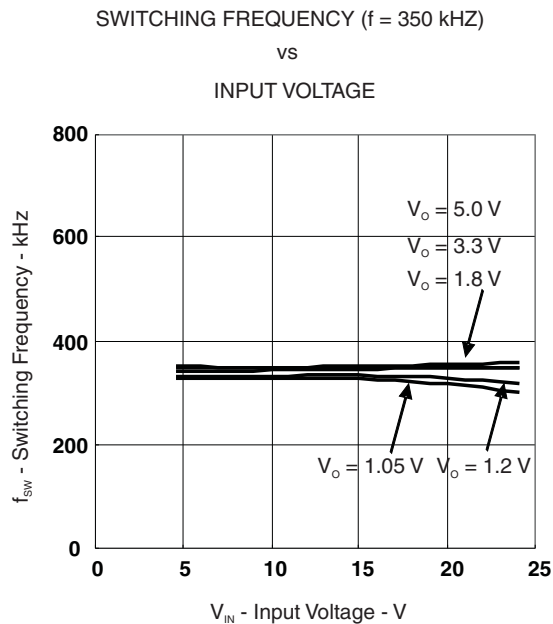
**Figure 10. Ripple Voltage**  
(FSEL = V5FILT, 700 kHz Selection)

### 4.6 Startup Performance

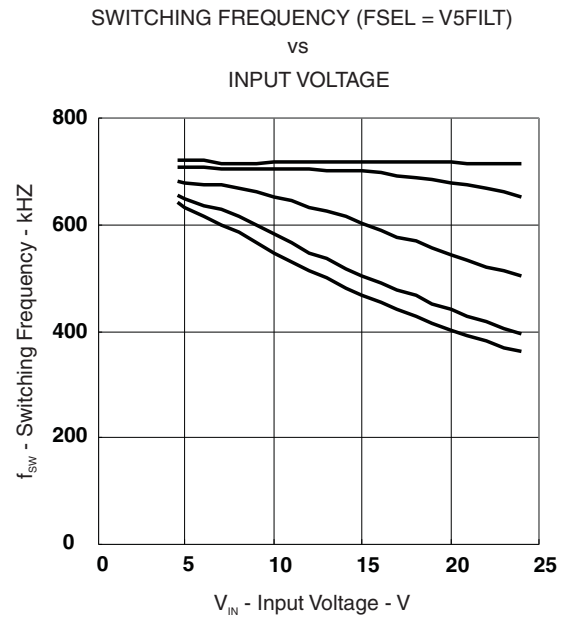


**Figure 11. 1.05-V Startup Waveforms**

### 4.7 Switching Frequency

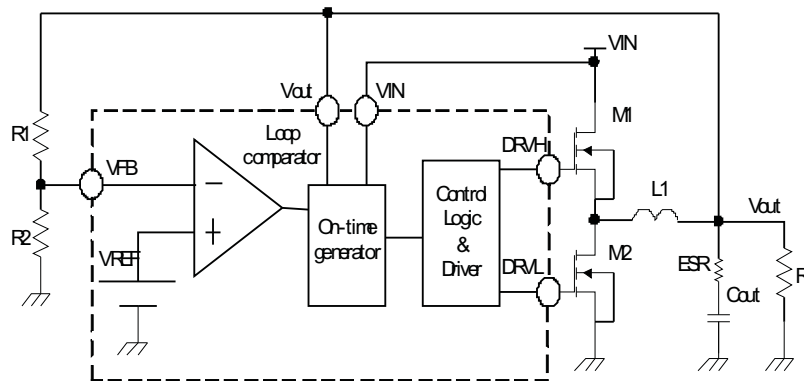


**Figure 12. Switching Frequency (FSEL = GND, 350 kHz Selection)**



**Figure 13. Switching Frequency (FSEL = V5FILT, 700 kHz Selection)**

## 5 Selection of Each External Components



**Figure 14. D-CAP™ Mode Block Diagram**

### 5.1 Output Voltage Setup

$$V_o = V_{REF} \times (1 + R1/R2) + V_{FB(ripple)} / 2 \times (1 + R1/R2) \tag{1}$$

Example:

In case of  $R1 = 3.6 \text{ k}\Omega$ ,  $R2 = 10 \text{ k}\Omega$ ,  $V_{FB(ripple)} = 10 \text{ mV}$  and  $FSEL = GND$  (350 kHz selection)  
 $V_o = 0.765 \times (1 + 3.6 \text{ k}/10 \text{ k}) + 0.01/2 \times (1 + 3.6 \text{ k}/10 \text{ k}) = 1.057 \text{ V}$

## 5.2 Softstart Time Setup

$$T_{SS} = C_{SS} \times V_{REF} / 2 \mu A \quad (2)$$

Example:

In case of  $C_{SS} = 4700 \text{ pF}$  and  $F_{SEL} = V5FILT$  ( $V_{REF} = 0.758 \text{ V}$  at 700 kHz selection)

$$T_{SS} = 4700 \text{ pF} \times 0.758 / 2 \mu A = 1.78 \text{ ms} \quad (T_{SS} = \text{softstart time, } C_{SS} = \text{cap for softstart})$$

## 5.3 Over Current Limit Setup

$$I_{ocl} = I_{(trip)} \times R_{(trip)} / R_{ds(on)} \quad (3)$$

Where:

- $I_{OCL}$  = Current limit setting value
- $R_{(trip)}$  = Resistor trip pin
- $R_{ds(on)}$  = Low side FET  $R_{ds(on)}$

Example:

In case of  $R_{(trip)} = 5.6 \text{ k}\Omega$ ,  $R_{ds(on)} = 10 \text{ m}\Omega$

$$I_{ocl} = 10 \mu A \times 5.6 \text{ k}\Omega / 0.01 \Omega = 5.6 \text{ A}$$

Where:

- $I_{ocl} = I_{load(dc)} + I_{out(ripple)}/2$

## 5.4 Coil Selection

Select coil to keep inductor ripple current 1/4~1/2 of load(max).

$$L = 1 / (I_{ind(ripple)} \times f_{SW}) \times (V_{IN(max)} - V_{OUT}) \times V_{OUT} / V_{IN(max)} \quad (4)$$

Example:

In case of  $I_{ind(ripple)} = \text{inductor ripple current} = 1 \text{ Ap-p}$ ,  $f_{SW} = \text{switching frequency} = 350 \text{ kHz}$ ,

$$V_{IN(max)} = 15 \text{ V}, V_{OUT} = 1.2 \text{ V}$$

$$L = 1 / (1 \text{ A} \times 350 \text{ kHz}) \times (15 \text{ V} - 1.2 \text{ V}) \times 1.2 \text{ V} / 15 \text{ V} = 3.15 \mu\text{H} \approx 3.3 \mu\text{H}$$

## 5.5 $V_{O(ripple)}$ Calculation for Use of Ceramic Output Capacitor

$$\begin{aligned} V_{O(ripple)} &= (1/2 \times (1/2 \times T_{CYC} \times 1/2 \times I_{ind(ripple)}) / (1/2 \times T_{CYC}) \times 1/2 \times T_{CYC} / C_{OUT} \\ &= (1/4 \times I_{ind(ripple)} \times 1/2 \times T_{CYC}) / C_{OUT} \\ &= (1/8 \times I_{ind(ripple)} \times T_{CYC}) / C_{OUT} \end{aligned} \quad (5)$$

Equation 5 neglects ESR and ESL.

Example:

In case of  $T_{CYC} = 1 / f_{SW} = 1 / 350 \text{ kHz} = 2.8 \mu\text{s}$ ,  $I_{ind(ripple)} = 1 \text{ Ap-p}$ ,  $C_{OUT} = 22 \mu\text{F} \times 2$

$$V_{O(ripple)} = (1/8 \times 1 \text{ Ap-p} \times 2.8 \mu\text{s}) / 44 \mu\text{F} = 8 \text{ mVp-p}$$

## 5.6 Overshoot in Load Transition

$$\Delta V_{OS} = 1/2 \times \Delta I_{load} \times (L/V_O) \times \Delta I_{load} / C_{OUT} \quad (6)$$

Example:

In case of  $\Delta V_{OS} = \text{overshoot voltage on } V_O$ ,  $\Delta I_{load} = \text{load current} = 3 \text{ A}$ ,  $L = 1.5 \mu\text{H}$ ,  $C_{OUT} = 22 \mu\text{F} \times 3$ ,  $V_O = 1.2 \text{ V}$

$$\Delta V_{OS} = 1/2 \times 3 \text{ A} \times (1.5 \mu\text{H} / 1.2 \text{ V}) \times 3 \text{ A} / 66 \mu\text{F} = 85 \text{ mV}$$

### 5.7 Undershoot in Load Transition

$$\Delta V_{US} = 1/2 \times \Delta I_{load} \times L/K \times \Delta I_{load} / C_{OUT}$$

Equation 7 calculation by critical inductance theory which includes consideration of the influence of min off time.

(7)

$$K = ((V_{IN} - V_O) - T_{min(off)}/T_{on} \times V_{OUT}) \times (T_{on}/(T_{on}+T_{min(off)}))$$

(8)

Example:

$\Delta V_{US}$  : undershoot voltage on  $V_O$ ,  $\Delta I_{LOAD}$  : Load current = 3 A,  $L = 1.5 \mu\text{H}$ ,  $C_{OUT} = 22 \mu\text{F} \times 3$ ,  
 $V_O = 1.2 \text{ V}$ ,  $V_{IN} = 12 \text{ V}$ ,  $T_{min(off)} = 285 \text{ ns}$  (FSEL = GND, 350 kHz selection)

$T_{on} = V_{OUT}/V_{IN} \times 1/f_{SW} = 1.2 \text{ V}/12 \text{ V} \times 1/350 \text{ kHz}$ ,  $K = ((12 \text{ V}-1.2 \text{ V}) - 0.285 \mu\text{s}/0.285 \mu\text{s} \times 1.2 \text{ V} \times (0.285 \mu\text{s} / (0.285 \mu\text{s} + 0.285 \mu\text{s})) = 10.2 \text{ V}$

$\Delta V_{US} = 1/2 \times 3 \text{ A} \times 1.5 \mu\text{H} / (10.2 \text{ V}) \times 3 \text{ A} / 66 \mu\text{F} = 10 \text{ mV}$

## 6 EVM Assembly Drawing and PCB Layout

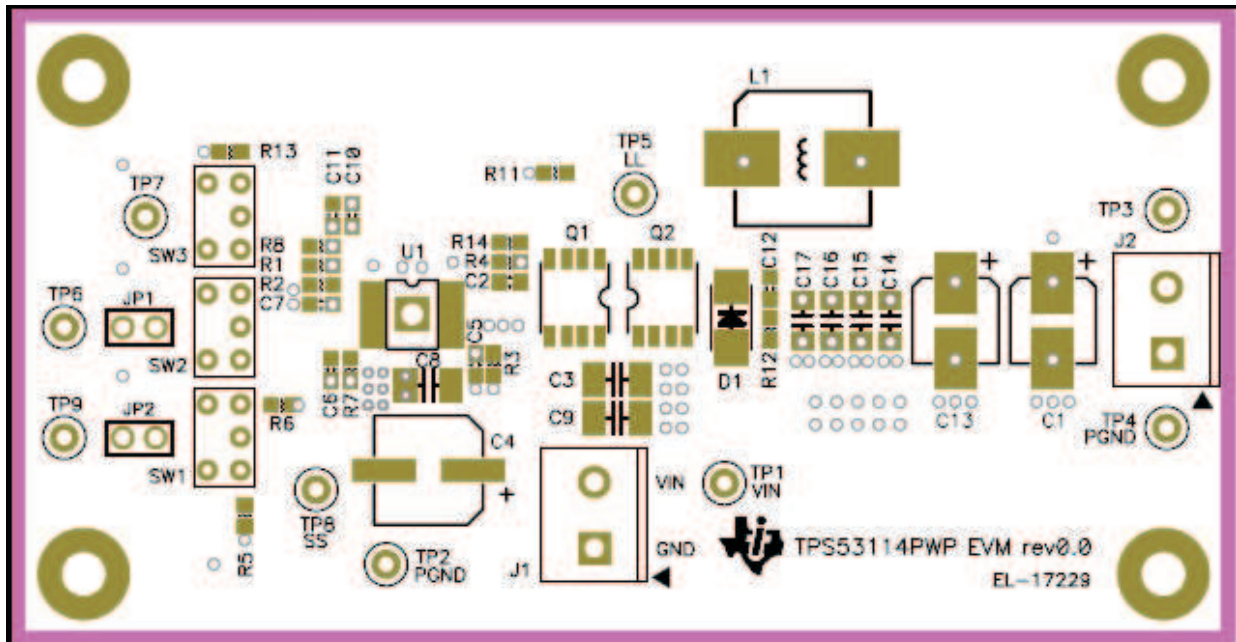


Figure 15. Top Assembly

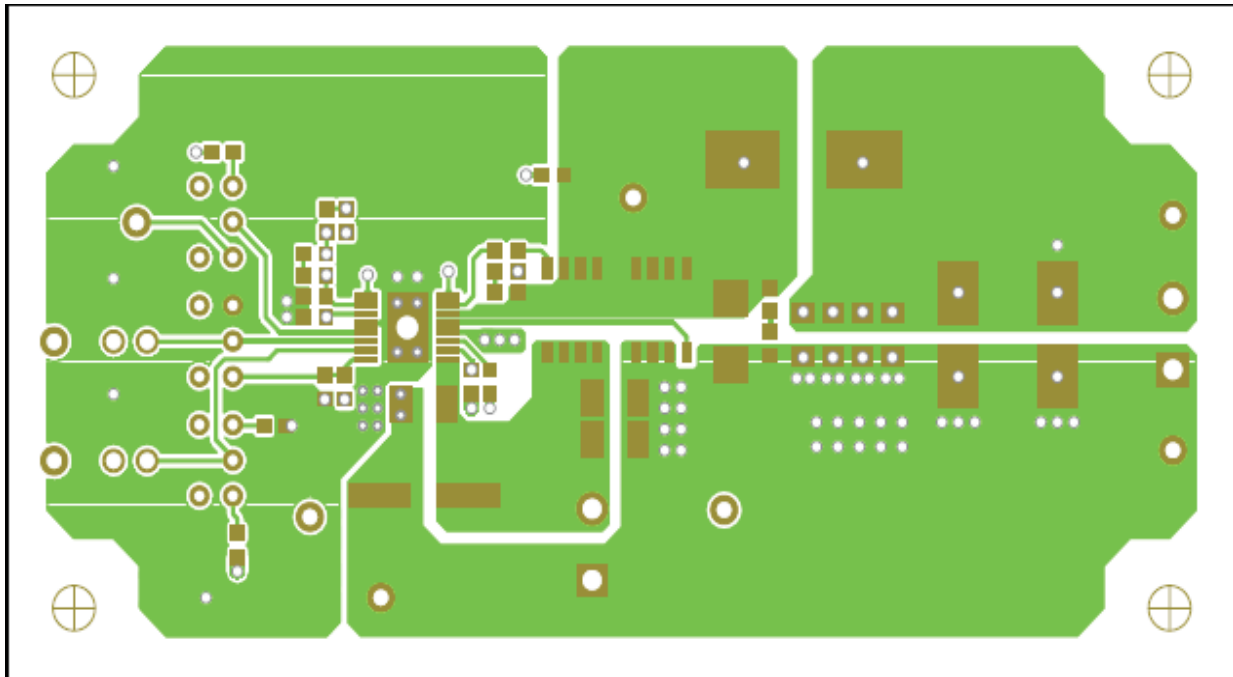


Figure 16. Top Layer

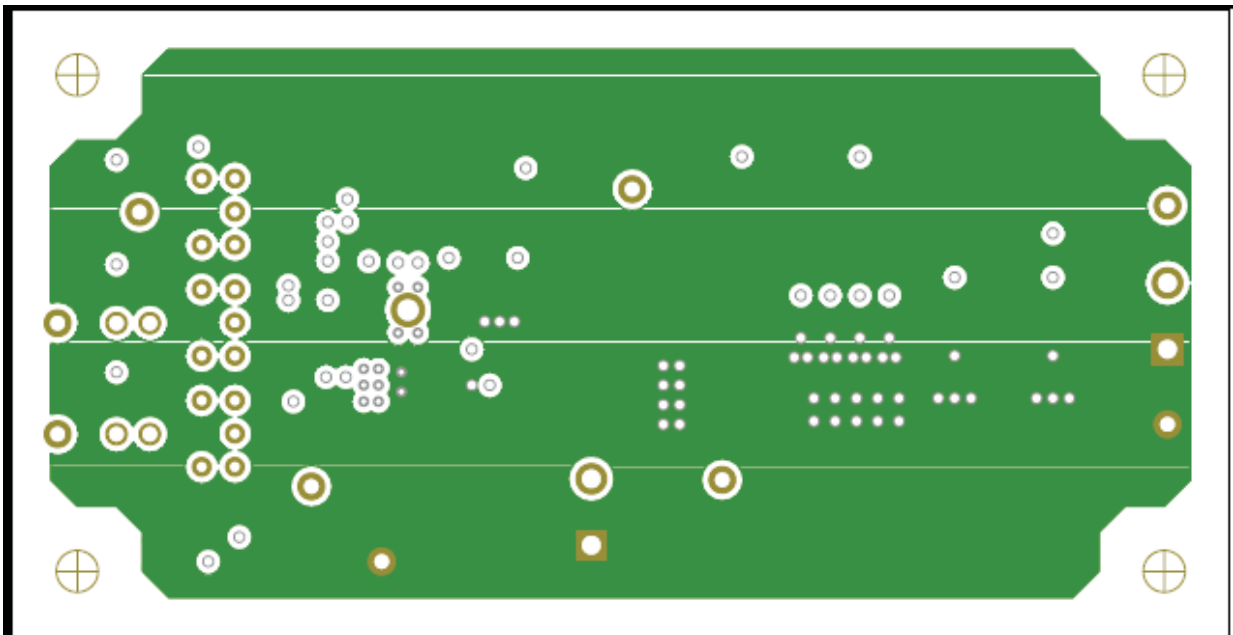


Figure 17. Inner Layer 1

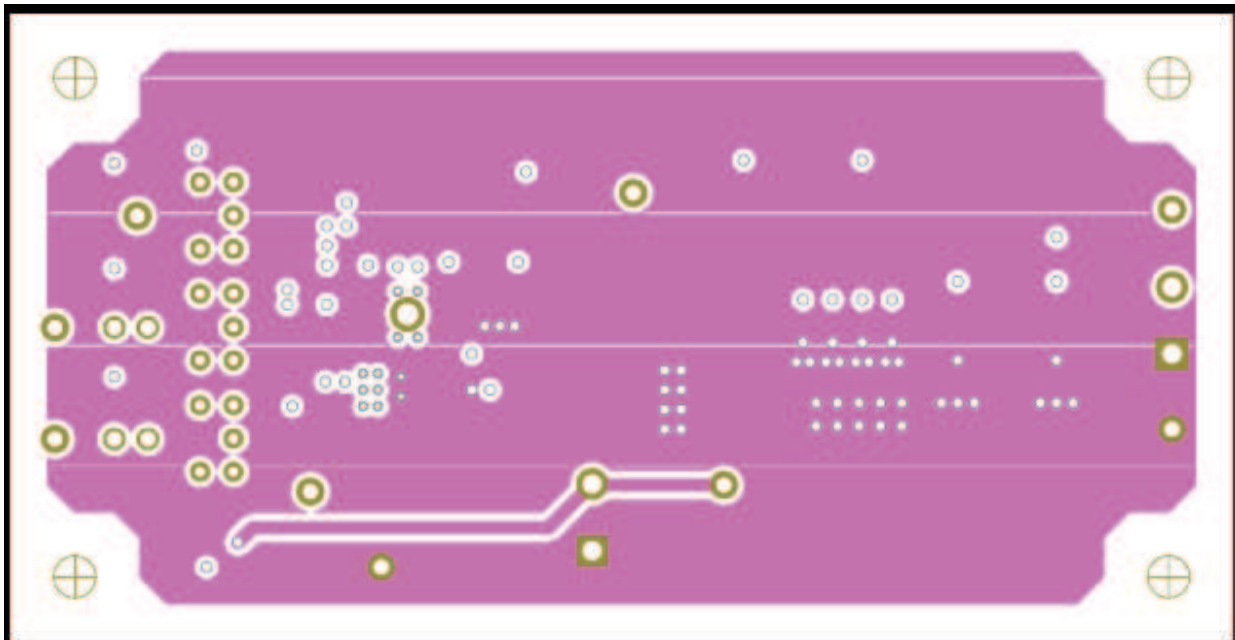


Figure 18. Inner Layer 2

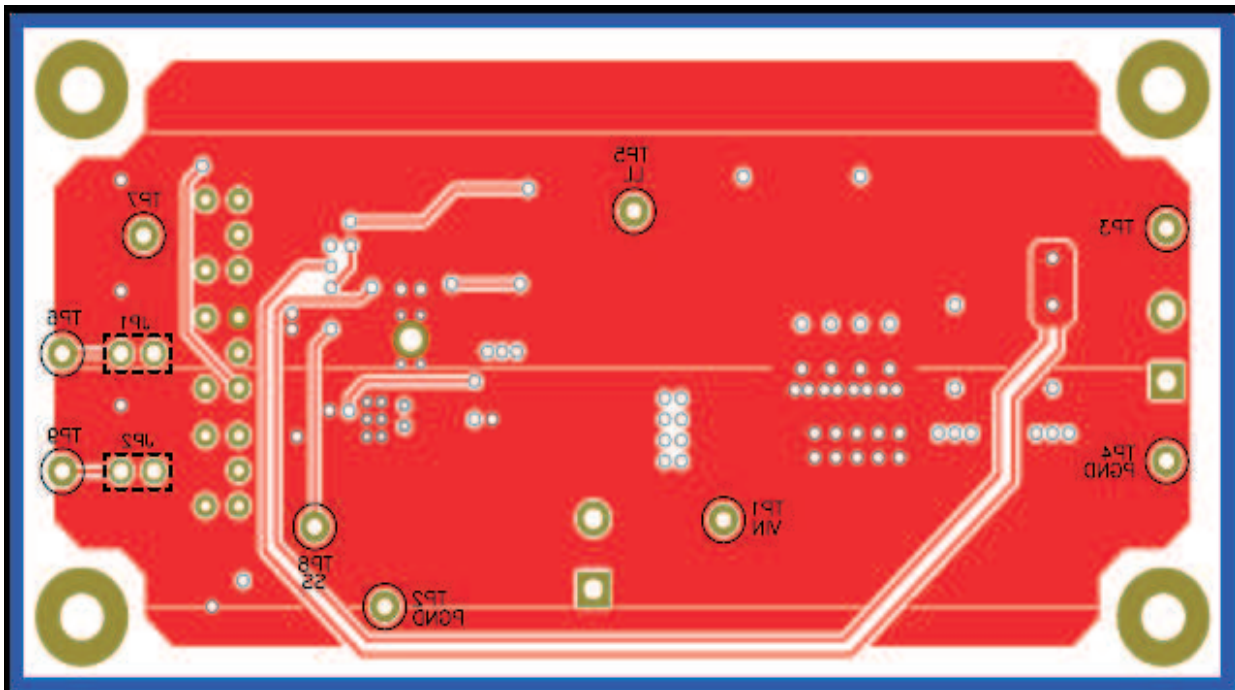


Figure 19. Bottom Layer

## 7 List of Materials

**Table 2. List of Materials**

Reference Designator	QTY	Description	Size	Mfr	Part Number
PCB	1	TPS53114PWP EVM rev 0.0			
U1	1	IC, dual synchronous step-down controller for low voltage power rails	HTSSOP16	TI	TPS53114PWP
L1	1	Inductor, 1.5 $\mu$ H, 11.0 A, 9.7 m $\Omega$	6.5 x 7.1 mm	TDK	SPM6530T-1R5M100
Q1	1	MOSFET, N-ch, 30 V, 9.3 A, 13.8 m $\Omega$	SO8	FAIRCHILD	FDS8878
Q2	1	MOSFET, N-ch, 30 V, 14 A, 8.6 m $\Omega$	SO8	FAIRCHILD	FDS8690
C1	0	Capacitor, NPCAP, 330 $\mu$ F, 4.0 V, 15 m $\Omega$ , 20% (no mount)	6.6 x 7.2 mm	NIPPON CHEMI-CON	APXE4R0ARA331M
C13	0	Capacitor, OS-CON (no mount)	0.260 sq inch	Sanyo	Any
C14, C15, C16, C17	0	Capacitor, ceramic, 22 $\mu$ F, 6.3 V, 20%, -55~85°C	1206	TDK	C3216X5R0J226M
C2	1	Capacitor, ceramic, 0.1 $\mu$ F, 50 V, 10%	0603	TDK	C1608X5R1H104K
C3, C9	2	Capacitor, ceramic, 10 $\mu$ F, 25 V, 10%, -55~125°C	1210	TDK	C3225X7R1E106K
C4	0	Capacitor (Electrolytic)	8.3 x 8.3 mm	Panasonic	EEVFKxyyyF
C5	1	Capacitor, ceramic, 4.7 $\mu$ F, 6.3 V, 10%	0603	TDK	C1608X5R0J475K
C6	1	Capacitor, ceramic, 1 $\mu$ F, 25 V, 10%	0603	Panasonic	ECJ-1VB1E105K
C7	1	Capacitor, ceramic, 4700 pF, 50 V, 10%	0603	TDK	C1608X7R1H472K
C8	1	Capacitor, ceramic, 22 $\mu$ F, 25 V, 10%, -55~85°C	1210	Murata	GRM32ER61E226KE15L
C10	1	Capacitor, ceramic (no mount)	0603	std	std
C11	1	Capacitor, ceramic (no mount)	0603	std	std
C12	1	Capacitor, ceramic (no mount)	0603	std	std
R1	1	Resistor, Chip, 3.3 k $\Omega$ , 1/10 W, 1%	0603	ROHM	MCR03EZPFX3301
R2	1	Resistor, Chip, 10 k $\Omega$ , 1/10 W, 1%	0603	ROHM	MCR03EZPFX1002
R3	1	Resistor, Chip, 4.3 k $\Omega$ , 1/10 W, 1%	0603	ROHM	MCR03EZPFX4301
R4, R14	2	Resistor, Chip, 0 $\Omega$ , 1/10 W, 5%	0603	ROHM	MCR03EZPJ000
R5, R6	2	Resistor, Chip, 1 k $\Omega$ , 1/10 W, 1%	0603	ROHM	MCR03EZPFX1001
R7, R11, R12	3	Resistor, (no mount)	0603	Std	Std
R8	1	Resistor, Chip, 330 $\Omega$ , 1/10 W, 1%	0603	ROHM	MCR03EZPFX3300
R13	1	Resistor, Chip, 100 k $\Omega$ , 1/10 W, 1%	0603	ROHM	MCR03EZPFX1003
D1	0	Diode, Schottky, 1 A, 30 V (no mount)	SMA	Any	Any
SW1	1	ON-OFF-ON mini toggle switch		Nikkai	G-13AP
SW2	1	ON-OFF-ON mini toggle switch		Nikkai	G-13AP
SW3	1	ON-OFF mini toggle switch		Nikkai	G-12AP
J1, J2	3	Terminal block, 2 pin, 15 A, 5.1 mm	0.40 x 0.35 inch	Phoenix Contact	MKDSN1.5/2-5.08
TP1	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP2	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP3	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP4	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP5	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP6	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP7	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G



**Table 2. List of Materials (continued)**

Reference Designator	QTY	Description	Size	Mfr	Part Number
TP8	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G
TP9	1	Test Point, yellow, thru hole	0.125 x 0.125 inch	MAC8	LC-2-G

## 8 References

1. TPS53114 datasheet, Single Synchronous Step-Down Controller for Low Voltage Power Rails ([SLVS887](#))

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

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