

# **TPS65283EVM-646 and TPS65283-1EVM-646 3.5-A, 2.5-A Regulator and Power Switch Evaluation Module**

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This document presents the information required to power the TPS65283 and TPS65283-1 power-management integrated circuits (PMIC) as well as the support documentation including schematic, printed-circuit board (PCB) layout, and bill of materials (BOM). Throughout the remainder of this document, the abbreviations *EVM*, *TPS65283/-1EVM-646*, and *evaluation module* refer to both the TPS65283EVM-646 and TPS65283-1EVM-646. Also throughout this user guide, the abbreviation *TPS65283/-1* refers to both the TPS65283 and TPS65283-1 ICs.

## Contents

1	Background .....	2
2	TPS65283/-1EVM-646 Schematic .....	3
3	Board Layout .....	4
4	Bench Test Setup Conditions .....	6
	4.1 Header Description and Jumper Placement .....	6
	4.2 Jumpers and Switches .....	6
	4.3 Test Points and Placement .....	7
5	Power-Up Procedure .....	7
6	Test Results .....	7
7	Bill of Materials .....	8

## List of Figures

1	TPS65283/-1EVM-646 Schematic .....	3
2	Component Placement (Top Layer) .....	4
3	Top Layer .....	5
4	Middle (Second) Layer Solid Copper Ground .....	5
5	Middle (Third) Layer .....	5
6	Bottom Layer .....	5
7	Headers Description and Jumper Placement .....	6

## List of Tables

1	Input Voltage and Output Current Summary .....	2
2	Jumpers and Switches .....	6
3	Test Points and Placement .....	7
4	Bill of Materials .....	8

## 1 Background

The TPS65283/-1 PMICs are designed to provide 3.5-A and 2.5-A continuous outputs with an operational range of 4.5 V to 18 V and an internal switching frequency of 500 kHz, with automatic pulse-frequency modulation (PFM) and pulse-width modulation (PWM) operation. The devices also feature two power distribution switches.

As there are many possible options to set the converters, [Table 1](#) presents the performance specification summary for the EVM.

**Table 1. Input Voltage and Output Current Summary**

EVM	Test Conditions	Output Current Range
TPS65283EVM TPS65283-1EVM	VIN = 4.5 V to 18 V Fsw = 500 kHz	Buck1, 1.2 V, 3.5 A Buck2, 5 V, 2.5 A (25°C ambient)
	SW_IN = 5 V	SW_OUT = 5 V ISW_OUT = 1.2 A

This evaluation module is designed to provide access to the features of the TPS65283. Some modifications can be made to this module to test performance at different input and output voltages, current and frequency operation. Please contact TI Field Applications Group for advice on these matters.

## 2 TPS65283/-1EVM-646 Schematic

Figure 1 illustrates the EVM schematic. The resistor and capacitor values have been chosen according to the guidelines presented on the TPS65283, TPS65283-1 specification. Note that for the purpose of gains-phase measurements, R15 and R16 (0 Ω on the EVM) need to be replaced by suitable low value resistors as per the network analyzer setup required. Test points connections are provided on either end of the resistors to allow for easy measurement.

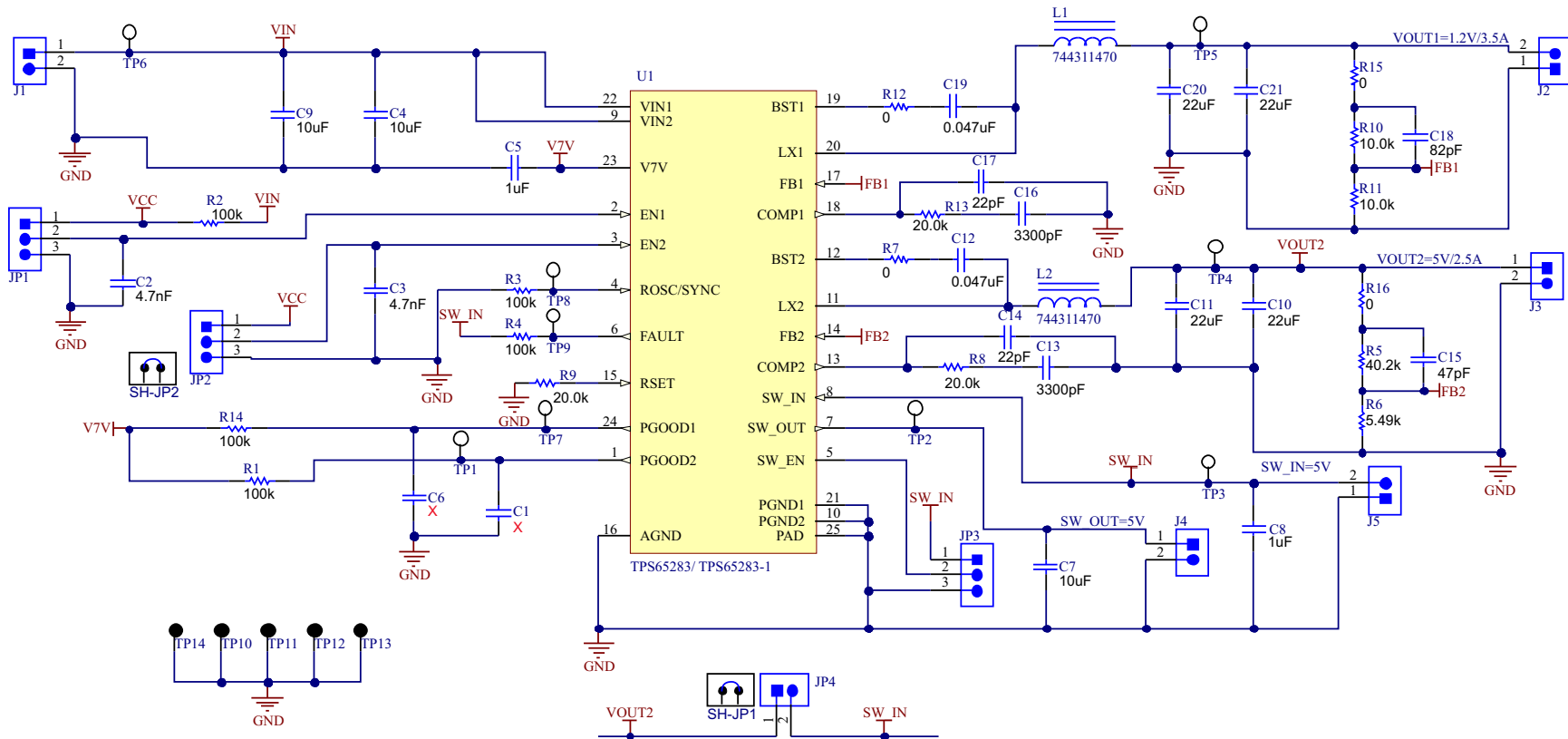


Figure 1. TPS65283/-1EVM-646 Schematic

### 3 Board Layout

Figure 2 through Figure 6 show the PCB board layouts.

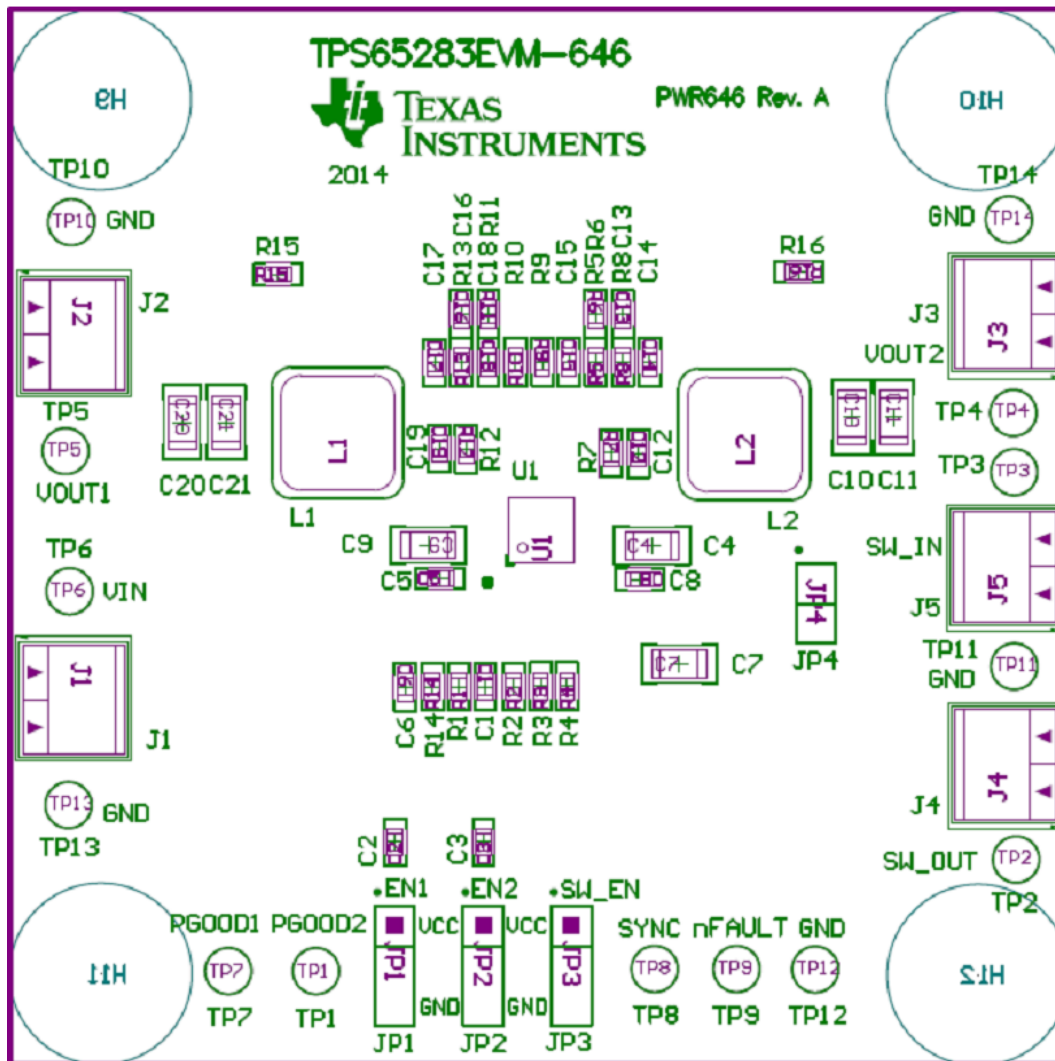
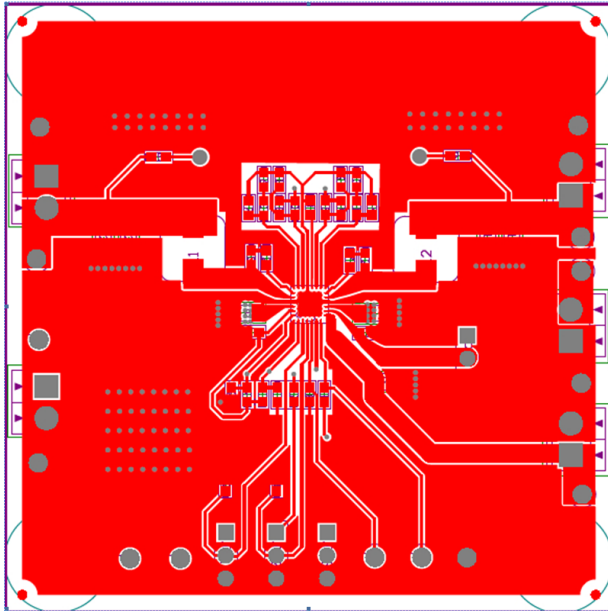
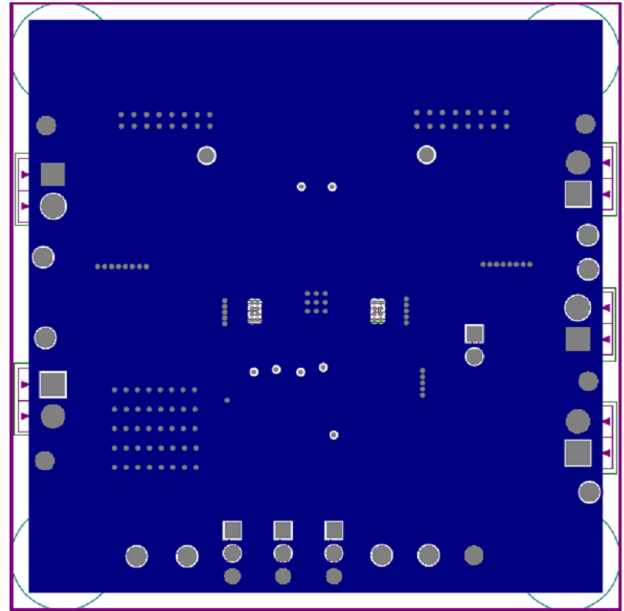


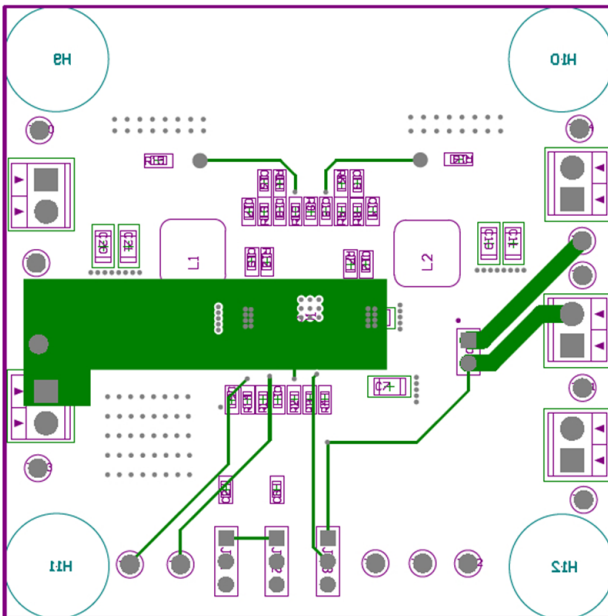
Figure 2. Component Placement (Top Layer)



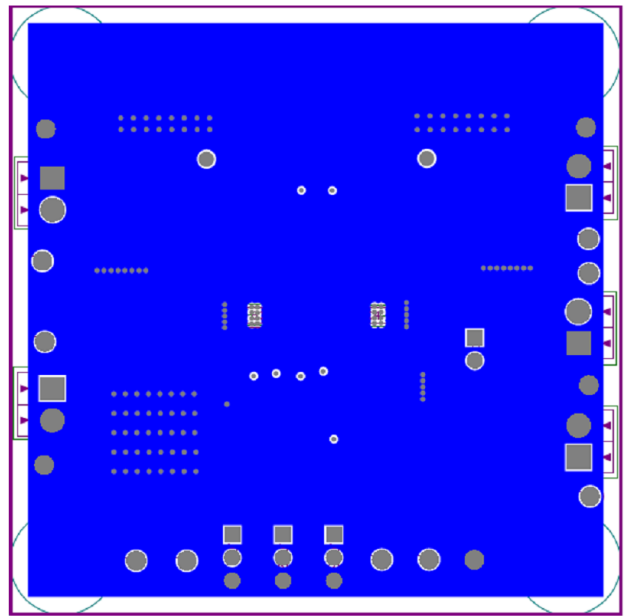
**Figure 3. Top Layer**



**Figure 4. Middle (Second) Layer Solid Copper Ground**



**Figure 5. Middle (Third) Layer**



**Figure 6. Bottom Layer**

## 4 Bench Test Setup Conditions

### 4.1 Header Description and Jumper Placement

Figure 7 illustrates header and jumper placement on the EVM.

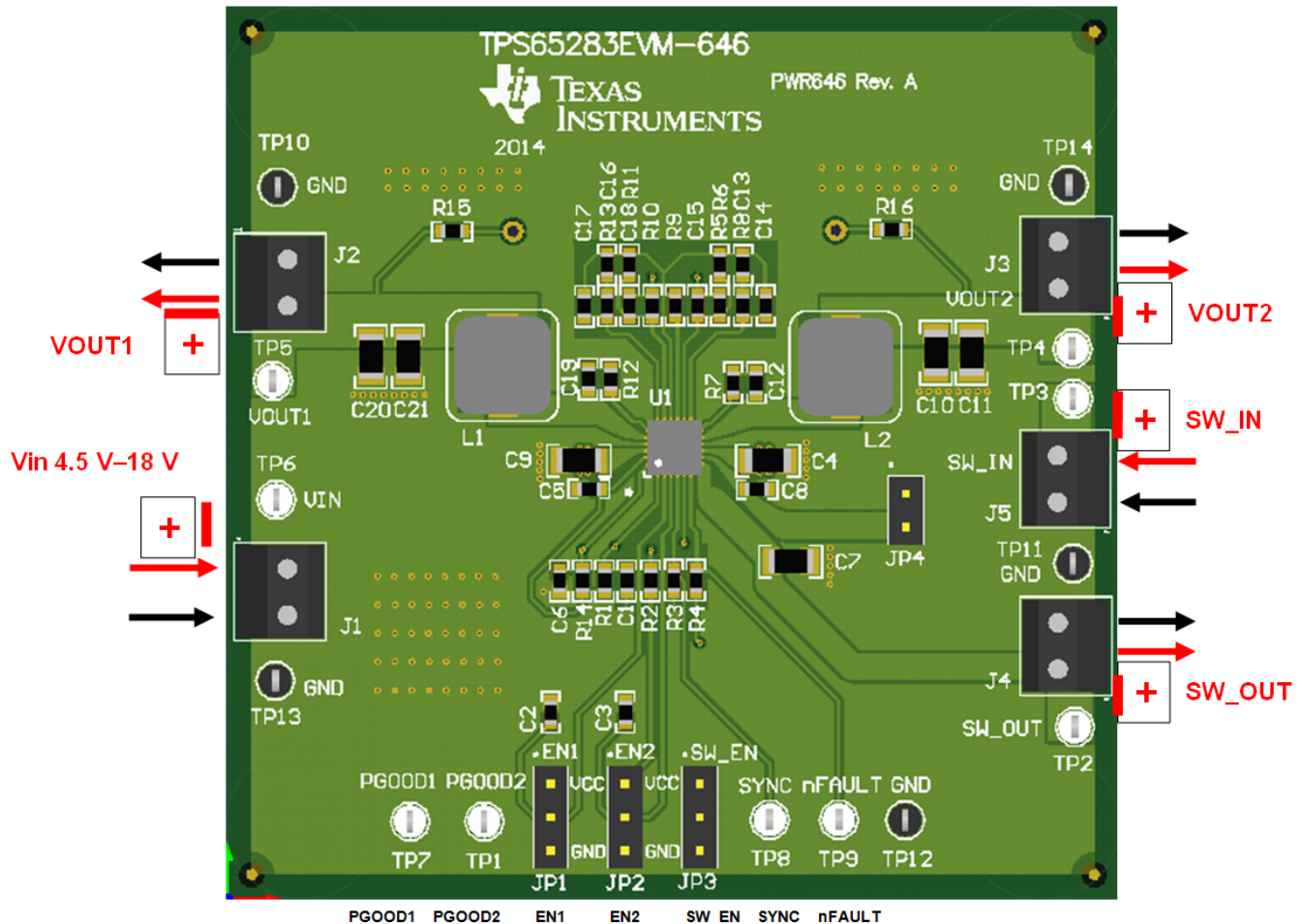


Figure 7. Headers Description and Jumper Placement

### 4.2 Jumpers and Switches

Table 2 lists the EVM jumpers and switches.

Table 2. Jumpers and Switches

#	Function	LOC	Placement	Comment
JP1	BUCK1 enable (EN)	W	For immediate start-up fit jumper to VCC For sequencing do not fit jumper To disable converter fit jumper to GND	Fit according to test requirement
JP2	BUCK2 enable (EN)	W	For immediate start-up fit jumper to VCC For sequencing do not fit jumper To disable converter fit jumper to GND	Fit according to test requirement
JP3	Switch enable (EN_SW)	W	For automatic start-up fit jumper to SW_IN To disable SWITCH fit jumper to GND	Fit according to test requirement
JP4	Vout2 to SW_IN	W	SW_IN pull to Vout2	Fit according to test requirement

### 4.3 Test Points and Placement

Buck converter outputs are white and have a label for easy location. Close to any of these test points there are black ground test points to allow for DVM measurement or to use a metal exposed scope probe to reduce common mode noise measurements. All test points are described in [Table 3](#).

**Table 3. Test Points and Placement**

TP	Name	Signal	Color	Comment
TP1	PGOOD2	Power good signal indicator for Buck2	White	
TP2	SW_OUT	Power switch output	White	
TP3	SW_IN	Power switch input	White	
TP4	VOUT2	Output voltage Buck2	White	
TP5	VOUT1	Output voltage Buck1	White	
TP6	VIN	VIN	White	
TP7	PGOOD1	Power good signal indicator for Buck1	White	
TP8	SYNC	Clock synchronization	White	
TP9	nFAULT	Power switch nFAULT signal indicator	White	
TP10	GND	GND	Black	
TP11	GND	GND	Black	
TP12	GND	GND	Black	
TP13	GND	GND	Black	
TP14	GND	GND	Black	

## 5 Power-Up Procedure

Use the following steps to power-up the EVM:

1. Define which converters are enabled or disabled by connecting jumpers to JP1 and JP2 accordingly, or by wiring external drive signals to the ENx headers
2. Define the strategy to enable the USB switches either with jumpers or external drive signals to the SW\_EN pins
3. Connect loads to the output connectors
4. Apply a DC voltage to header J1. Polarity is marked on the silk-screen.
5. To power the USB switches, apply a DC voltage to J5. Enable the switches with JP3. Check the outputs.

## 6 Test Results

For the specific test result, such as power up, power down, transient, efficiency, and load regulation, please refer to the TPS65283/-1 ([SLVSCL3](#)) data sheet's application curves. All the data and waveforms are tested based on this EVM board.

## 7 Bill of Materials

Table 4 lists the BOM for this EVM.

**Table 4. Bill of Materials**

Qty	Designator	Value	Footprint	Description	Comment
0	C1, C6	4700pF	0603	CAP, CERM, 4700pF, 25V, +/-5%, C0G/NP0, 0603	DNI
2	C2, C3	4700pF	0603	CAP, CERM, 4700pF, 25V, +/-5%, C0G/NP0, 0603	
2	C4, C9	10uF	1206	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1206	
2	C5, C8	1uF	0603	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	
1	C7	10uF	1206	CAP, CERM, 10uF, 10V, +/-20%, X5R, 1206	
4	C10, C11, C20, C21	22uF	1206	CAP, CERM, 22uF, 16V, +/-20%, X5R, 1206	
2	C12, C19	0.047uF	0603	CAP, CERM, 0.047uF, 50V, +/-10%, X7R, 0603	
2	C13, C16	3300pF	0603	CAP, CERM, 3300pF, 50V, +/-5%, C0G/NP0, 0603	
2	C14, C17	22pF	0603	CAP, CERM, 22pF, 50V, +/-5%, C0G/NP0, 0603	
1	C15	47pF	0603	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603	
1	C18	82pF	0603	CAP, CERM, 82pF, 50V, +/-5%, C0G/NP0, 0603	
4	H9, H10, H11, H12		Transparent Bumpon	Bumpon, Hemisphere, 0.44 X 0.20, Clear	
5	J1, J2, J3, J4, J5		7.0x8.2x6.5mm	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	
3	JP1, JP2, JP3		3x1 Header	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	
1	JP4		2x1 Header	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	
2	L1, L2	4.7uH	WE-HC4	Inductor, Shielded Drum Core, Superflux, 4.7uH, 6A, 0.02 ohm, SMD	
5	R1, R2, R3, R4, R14	100k	0603	RES, 100k ohm, 1%, 0.1W, 0603	
1	R5	40.2k	0603	RES, 40.2k ohm, 1%, 0.1W, 0603	
1	R6	5.49k	0603	RES, 5.49k ohm, 1%, 0.1W, 0603	
4	R7, R12, R15, R16	0	0603	RES, 0 ohm, 5%, 0.1W, 0603	
3	R8, R9, R13	20k	0603	RES, 20.0k ohm, 1%, 0.1W, 0603	
2	R10, R11	10k	0603	RES, 10.0k ohm, 1%, 0.1W, 0603	
4	SH-JP1, SH-JP2, SH-JP3, SH-JP4	1x2	Shunt	Shunt, 100mil, Gold plated, Black	
9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	White	White Miniature Testpoint	Test Point, Miniature, White, TH	
5	TP10, TP11, TP12, TP13, TP14	Black	Black Miniature Testpoint	Test Point, Miniature, Black, TH	
1	U1		QFN-24	4.5 V to 18 V Input Voltage, Maximum 3.5A/2.5A Current, Synchronous Dual Buck Converter with Power Distribution Switch, RGE0024B	



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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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