User's Guide

TPS3760EVM User's Guide

ABSTRACT

This user's guide describes the operational use of the TPS3760EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS3760/TPS3760-Q1, a low-power, wide input voltage, overvoltage or undervoltage monitor. Included in this user's guide are setup instructions, a schematic diagram, printed-circuit board (PCB) layout drawings, and a bill of materials for the EVM.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The TPS3760EVM helps design engineers to evaluate the operation and performance of the TPS3760/ TPS3760-Q1 family of overvoltage and undervoltage monitors for possible use in their own circuit applications. This particular EVM configuration contains the TPS3760A012DYYR, an undervoltage supervisor designed to monitor an adjustable rail. The family of TPS3760/TPS3760-Q1 provides variable thresholds from 2.7 V to 65V and hysteresis options from 2% to 13% in a small 14-pin SOT-23 package with both open-drain output and push-pull outputs. The TPS3760/TPS3760-Q1 family includes adjustable capacitor pins for tying capacitors to adjust delays on both the rising and falling edges of the RESET outputs. Separately available SENSE input pins allow the redundancy sought by safety-critical and high-reliability systems. Lastly, the device provides an optional manual reset that allows a hard reset and a latch feature for certain desired applications. Section 2 provides schematics, a BOM, and layout information on the board. Section 3 describes the connectors, jumpers, and test points for the device. Section 4 describes the setup and operation of the EVM.

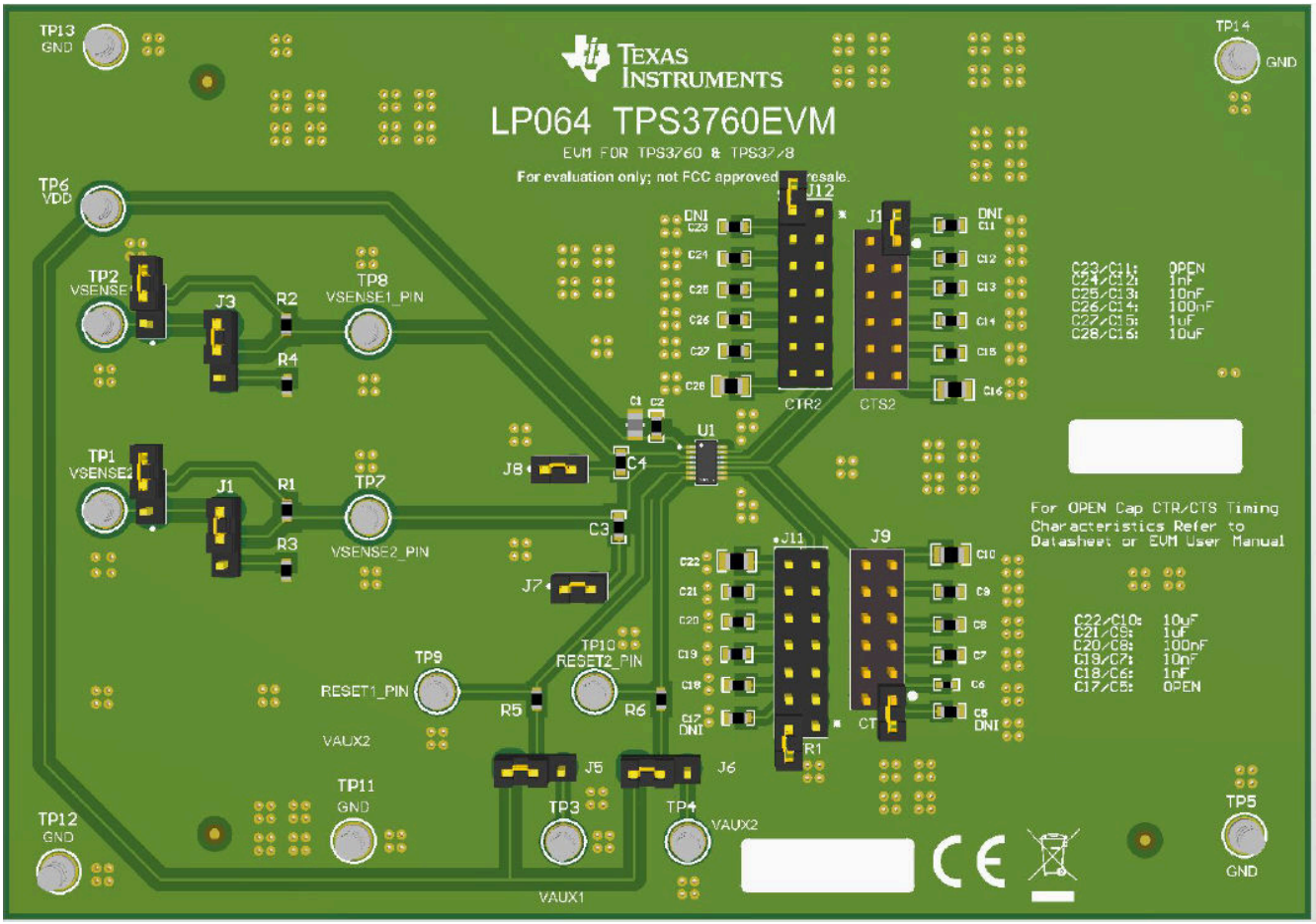

Figure 1-1. TPS3760EVM Board - Top

1.1 Related Documentation

TPS3760 (65 V & 2uA) Over and Undervoltage Detector with Delay Function, SNVS420.

Please see the TPS3760 data sheet for more detailed specifications, pin descriptions, applications, and other information related to the device. This user guide provides information related to using the EVM.

2 Schematics, Bill of Materials, and Layout

This section provides a detailed description of the TPS3760EVM schematic, bill of materials (BOM), and layout.

2.1 TPS3760EVM Schematic

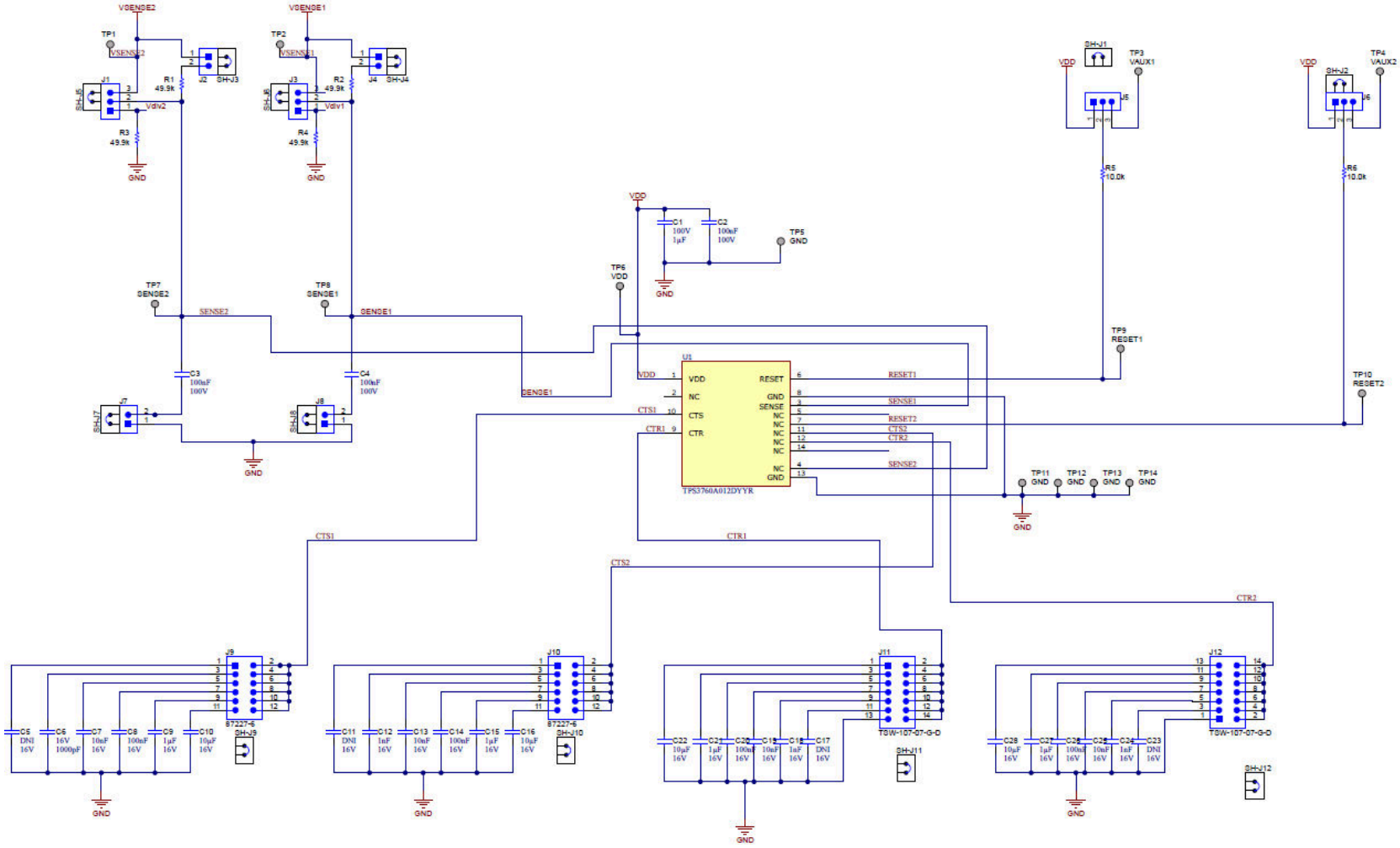

Figure 2-1. TPS3760EVM Schematic

2.2 TPS3760EVM Bill of Materials

Table 2-1. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		LP064	Any
C1	1	1uF	CAP, CERM, 1 µF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	805	08051C105K4Z2A	AVX
C2, C3, C4	3	0.1uF	CAP, CERM, 1000 pF, 16 V, +/- 10%, X7R, 0603	603	HMK107B7104MAHT	Taiyo Yuden
C5(DNI), C11(DNI), C12, C17(DNI), C18, C23(DNI), C24	3	1000pF	CAP, CERM, 1000 pF, 16 V, +/- 10%, X7R, 0603	603	885012206034	Wurth Elektronik
C6	1	1000pF	CAP, CERM, 1000 pF, 16 V, +/- 10%, X7R, 0402	402	GRM155R71C102KA01D	MuRata
C7	1	0.01uF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	603	C0603C103K4RACTU	Kemet
C8	1	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	603	EMK107B7104KA-T	Taiyo Yuden
C9, C15, C21, C27	4	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	603	EMK107B7105KA-T	Taiyo Yuden
C10, C16, C22, C28	4	10uF	CAP, CERM, 10 µF, 16 V,+/- 10%, X7R, 0805	805	CL21B106KOQNNNG	Samsung
C13, C19, C25	3	0.01uF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	603	885012206040	Wurth Elektronik
C14, C20, C26	3	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	603	885012206046	Wurth Elektronik
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J3, J5, J6	4		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J2, J4, J7, J8	4		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J9, J10	2		Header, 100mil, 6x2, Gold, TH	Header, 6x2, 100mil, Gold	87227-6	TE Connectivity
J11, J12	2		Header, 100mil, 7x2, Gold, TH	7x2 Header	TSW-107-07-G-D	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R2, R3, R4	4	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	603	RC0603FR-0749K9L	Yageo
R5, R6	2	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12	12	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14	14		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone
U1	1		High Voltage Supervisor with Programmable Sense and Reset Delay Function for Automotive	SOT-23-THIN-14	TPS3760A012DYYR	Texas Instruments

2.3 Layout and Component Placement

Figure 2-2 and Figure 2-3 are the top overlay and bottom overlay of the printed circuit board (PCB) and shows the component placement on the EVM. Figure 2-4 shows the top layout, Figure 2-5 and Figure 2-6 show the top and bottom layers, and Figure 2-7 and Figure 2-8 show the top and bottom solder masks of the EVM.

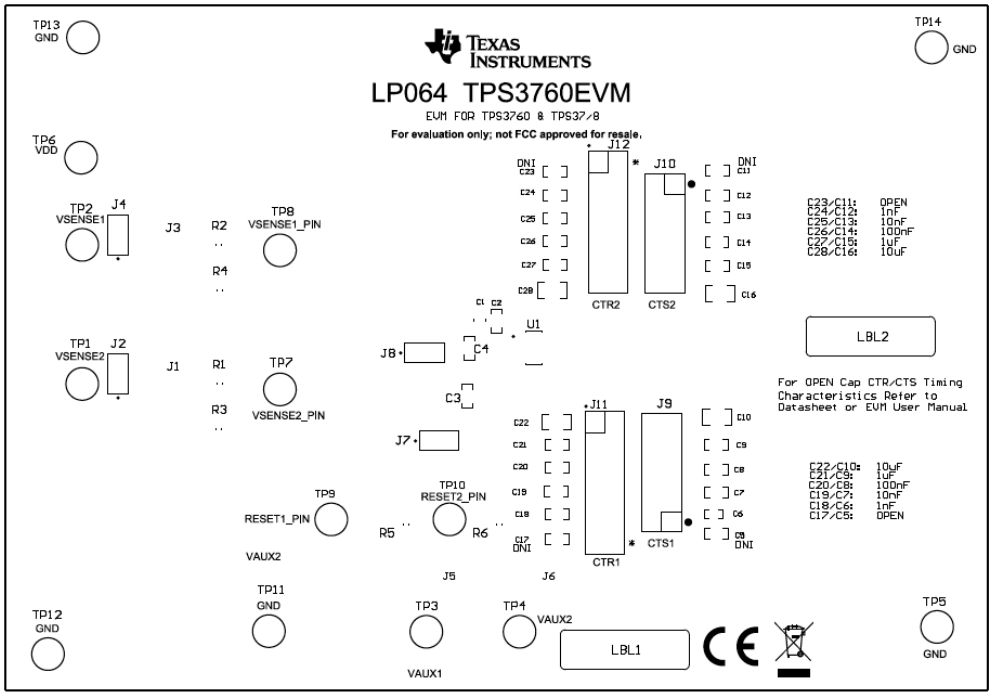

Figure 2-2. Component Placement - Top Overlay

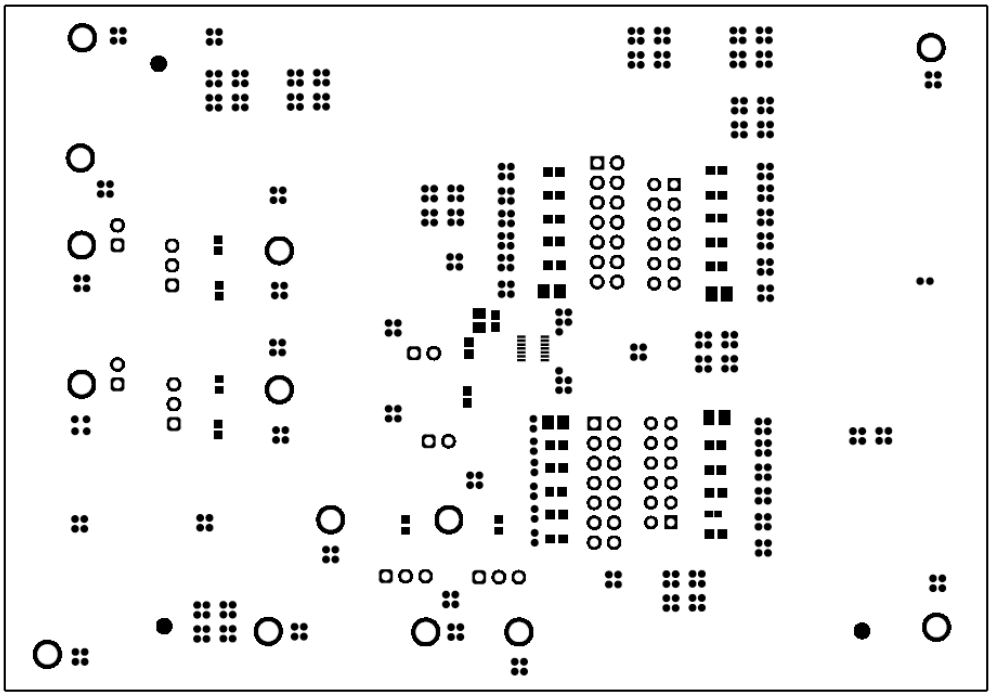

Figure 2-3. Component Placement - Bottom Overlay

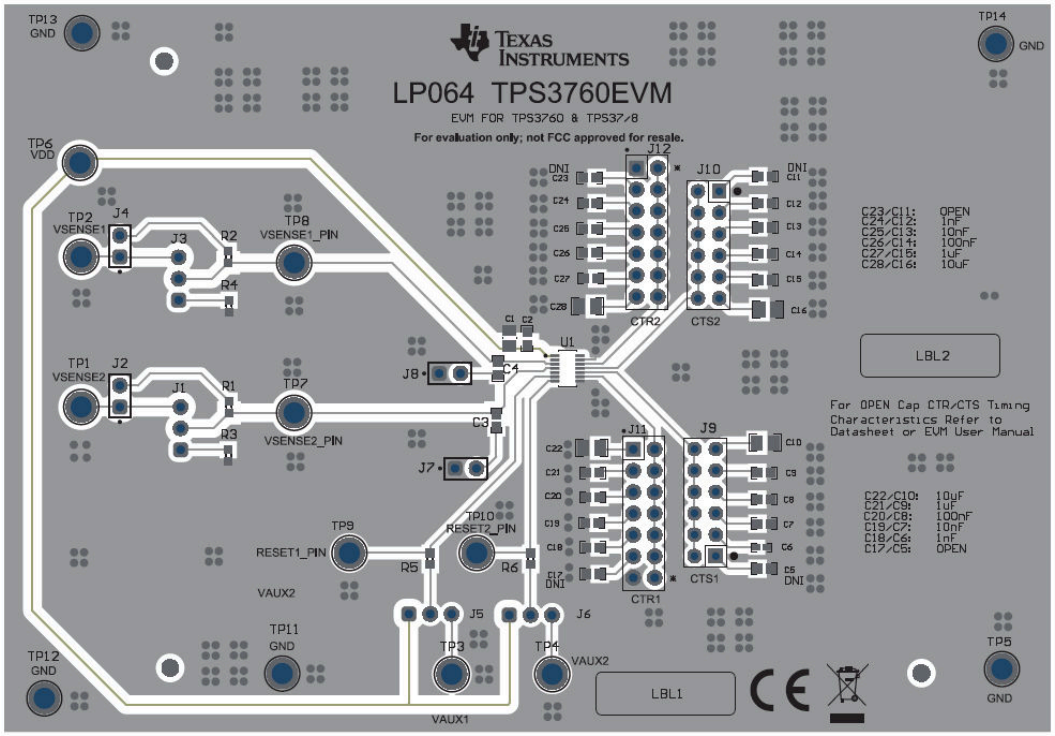

Figure 2-4. Layout - Top

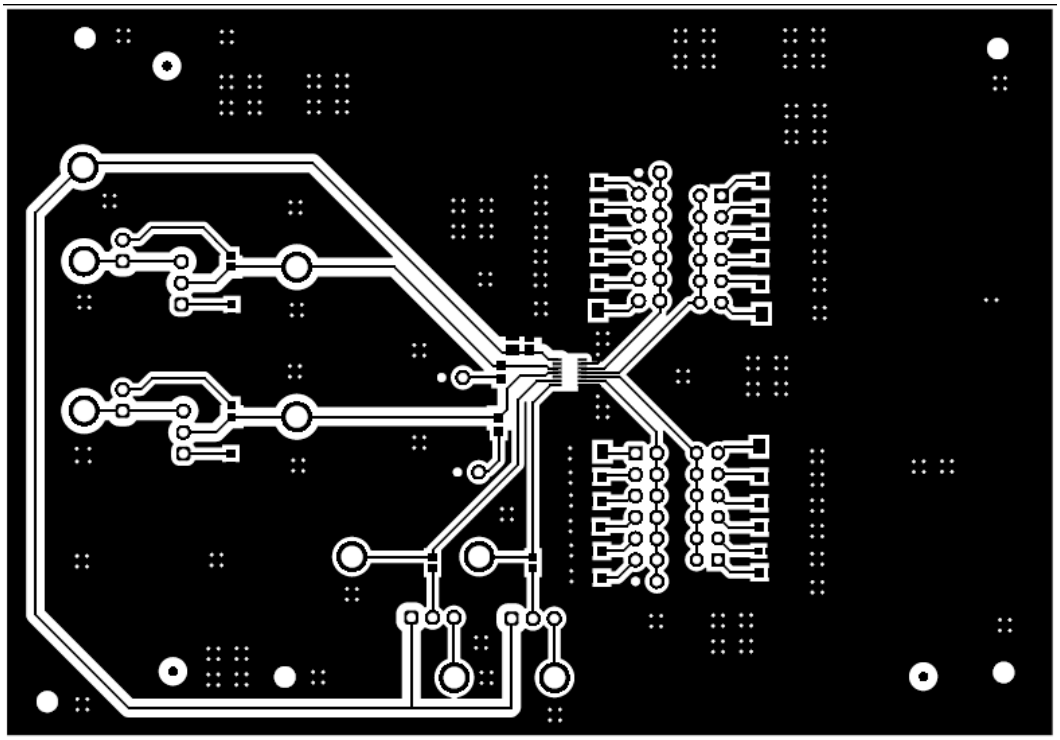

Figure 2-5. Top Layer

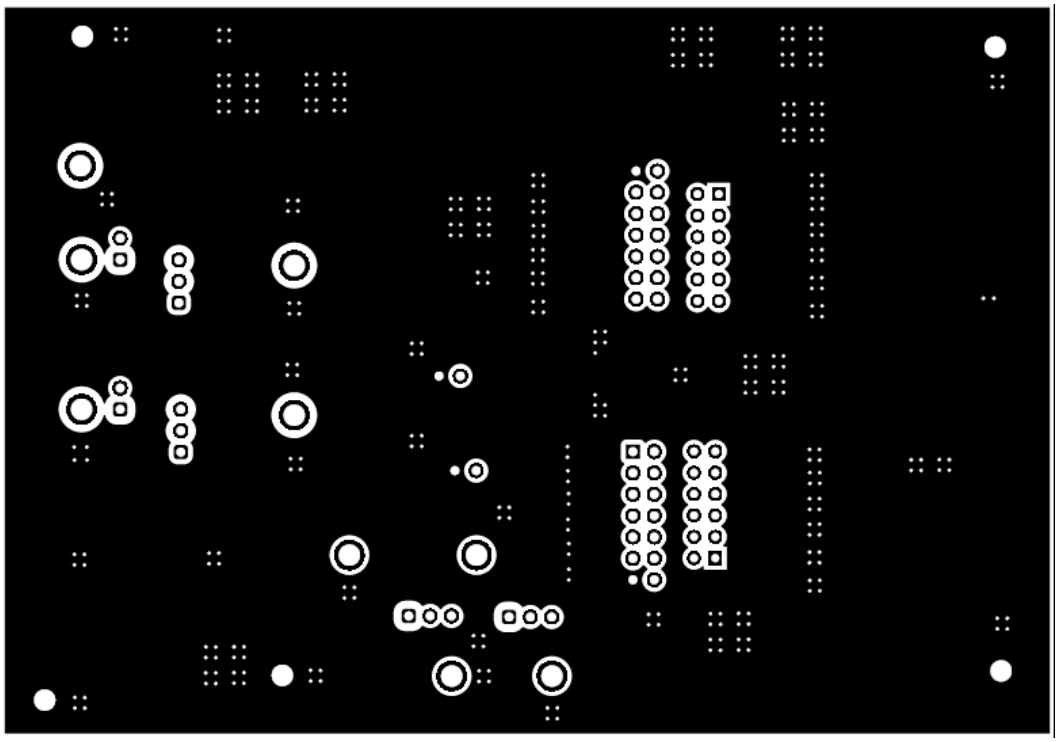

Figure 2-6. Bottom Layer

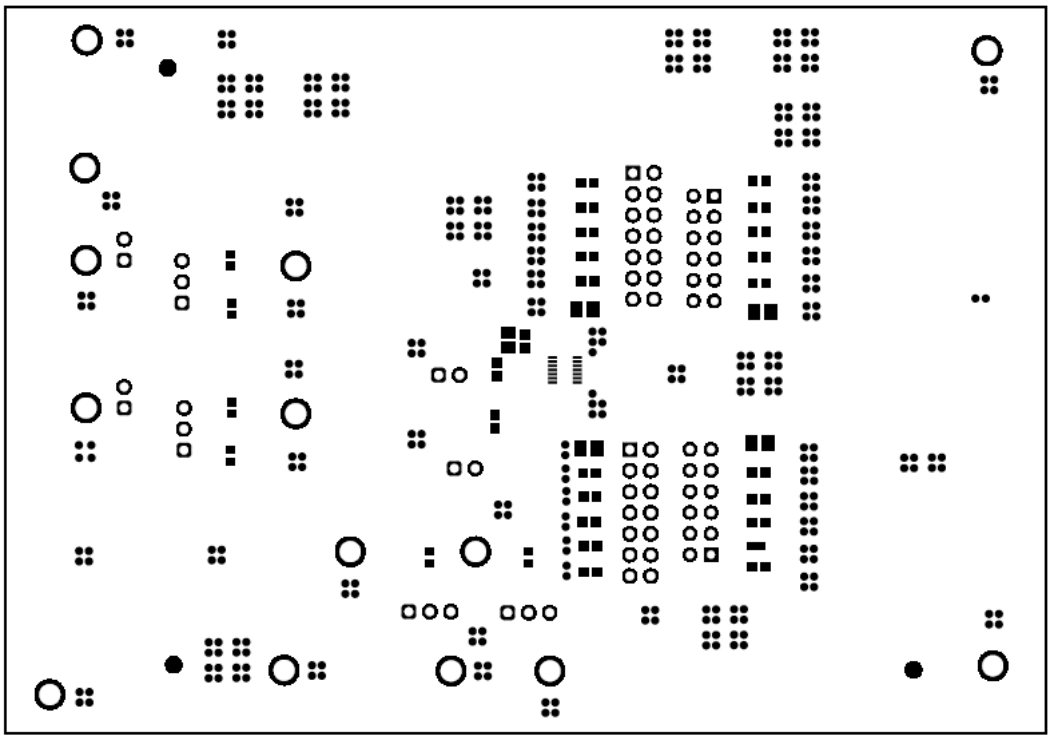

Figure 2-7. Top Solder Mask

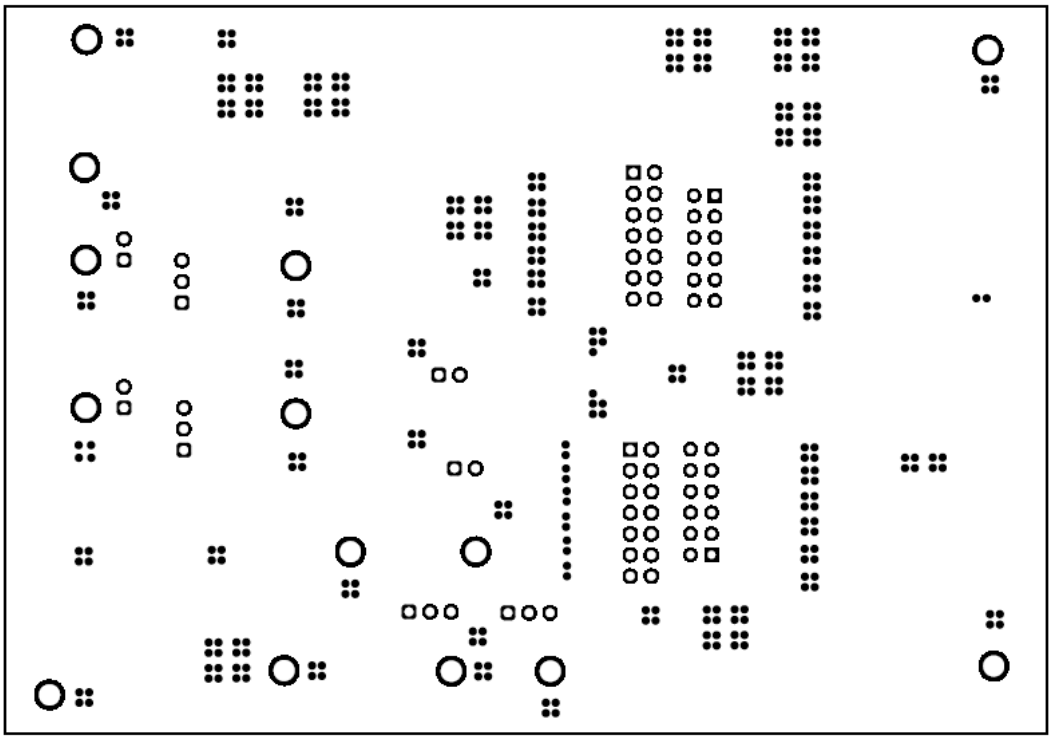

Figure 2-8. Bottom Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 3-1. Test Points

Test Point Number	Test Point Silkscreen Label	Function	Description
TP1	VSENSE2	Connects to the input of SENSE2 with optional divider.	Allows user to apply desired voltage to SENSE2 pin.
TP2	VSENSE1	Connects to the input of SENSE1 with optional divider.	Allows user to apply desired voltage to SENSE1 pin.
TP3	VAUX1	Connects to RESET1 pin.	Allows user to optionally add an external pull up rail for the RESET1 output.
TP4	VAUX2	Connects to RESET2 pin.	Allows user to optionally add an external pull up rail for the RESET1 output.
TP5	GND	Connects to ground.	Allows user to use ground connections from multiple points.
TP6	VDD	Connects to VDD pin.	Allows user to connect to the VDD pin of the device.
TP7	VSENSE2_PIN	Connects to the input of SENSE2 directly.	Allows user to connect directly to the SENSE2 pin of the device.
TP8	VSENSE1_PIN	Connects to the input of SENSE1 directly.	Allows user to connect directly to the SENSE1 pin of the device.
TP9	RESET1_PIN	Connects to the RESET1 pin.	Allows user to measure the RESET1 output voltage.
TP10	RESET2_PIN	Connects to the RESET2 pin.	Allows user to measure the RESET2 output voltage.
TP11	GND	Connects to ground.	Allows user to use ground connections from multiple points.
TP12	GND	Connects to ground.	Allows user to use ground connections from multiple points.
TP13	GND	Connects to ground.	Allows user to use ground connections from multiple points.
TP14	GND	Connects to ground.	Allows user to use ground connections from multiple points.

3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TPS3760EVM. As ordered, the EVM will have twelve jumpers installed.

Table 3-2. Jumpers

Jumper	Default Connection	Description
J1	Closed on top 2 pins	Selectable jumper to pick between halving voltage divider connection and direct VDD connection to SENSE2 (bottom 2 pins = voltage divider; top 2 pins: SENSE2 = VDD)
J2	Open	SENSE2 voltage divider jumper. Connects VDD to a halving voltage divider which feeds into SENSE2 if populated. (R_1 = R_2 = 49.9kΩ)
J3	Closed on top 2 pins	Selectable jumper to pick between halving voltage divider connection and direct VDD connection to SENSE1 (bottom 2 pins = voltage divider; top 2 pins: SENSE1 = VDD)
J4	Open	SENSE1 voltage divider jumper. Connects VDD to a halving voltage divider which feeds into SENSE1 if populated. (R_1 = R_2 = 49.9kΩ)
J5	Closed on left to middle pins	Pullup jumper to connect RESET1 via a 10.0kΩ resistor to VDD (disconnect for push-pull configuration devices or connect from middle to right to pullup to different voltages)
J6	Closed on left to middle pins	Pullup jumper to connect RESET2 via a 10.0kΩ resistor to VDD (disconnect for push-pull configuration devices or connect from middle to right to pullup to different voltages)
J7	Closed	Jumper to add a 100nF capacitor to the SENSE2 input.
J8	Closed	Jumper to add a 100nF capacitor to the SENSE1 input.
J9	Open	Selectable jumper to pick between 6 options for terminating CTS1. Capacitor sizes are marked on board and are the following, from bottom to top: DNI (solder custom capacitor here if desired), 1nF, 10nF, 100nF, 1uF, 10uF.
J10	Open	Selectable jumper to pick between 6 options for terminating CTS2. Capacitor sizes are marked on board and are the following, from top to bottom: DNI (solder custom capacitor here if desired), 1nF, 10nF, 100nF, 1uF, 10uF.
J11	Open	Selectable jumper to pick between 7 options for terminating CTR1/MR pin. Capacitor sizes are marked on board and are the following, from bottom to top: Open (Connect to GND to test MR functionality, DNI (solder custom capacitor here if desired), 1nF, 10nF, 100nF, 1uF, 10uF.
J12	Open	Selectable jumper to pick between 7 options for terminating CTR2/MR pin. Capacitor sizes are marked on board and are the following, from top to bottom: Open (Connect to GND to test MR functionality, DNI (solder custom capacitor here if desired), 1nF, 10nF, 100nF, 1uF, 10uF.

4 EVM Setup and Operation

This section describes the functionality and operation of the TPS3760EVM. The user should read the TPS3760 datasheet for electrical characteristics of the device.

4.1 Input Power (VDD)

The VDD supply is connected through the TP6 test point on board. TP6 is connected to the VDD pin of the TPS3760 device and TP5 is connected to the board common GND. The supply voltage range is 2.7V to 65V and a 0.1µF decoupling capacitor is recommended at the input for reducing noise that can propagate through the device (included on the EVM board at C2). Table 4-1 details the nominal supply voltage and typical input decoupling capacitor.

Table 4-1. Nominal Supply Parameters

Device	Nominal Supply Voltage (V)	Typical Decoupling Capacitor at Input
TPS3760, TPS3760-Q1	2.7V to 65V	0.1 µF

4.2 SENSE1/SENSE2 Inputs

The SENSE1 and SENSE2 inputs allow for any voltage rails to be monitored divided down through resistors. The default option of the TPS3760EVM is populated with a TPS3760A012DYYR device, which has an adjustable 0.8V threshold. The resistors R2 and R4 (both 49.9kΩ) control the voltage divider for the TPS3760 SENSE pin by using the SENSE1 input.These 0603 resistors can be replaced with any values to form a voltage divider that can then divide down to trip at the 0.8V threshold. This behavior and instructions on selecting these resistors can be found described in the TPS3760 datasheet in the 'Adjustable Voltage Thresholds' section. To use the voltage divider located on-board, make sure to populate a jumper on J4, and a jumper on the bottom two pins of J3 for SENSE1. To monitor VDD directly on either SENSE1 or SENSE2 populate a jumper on J4 and on the bottom two pins on J3 for for SENSE1, and populate a jumper on J2, and the bottom two pins on J1 for SENSE2 . The adjustable delays on the sense inputs can be found detailed in Section 4.5.

Also, note that the default option for this board is the TPS3760A012DYYR, which is a single channel device. TPS3760 does not include a SENSE2 input. SENSE2 and RESET2 signal path should follow the datasheet pinout configuration from the TPS3760 datasheet. The SENSE2 and RESET2 pins are for TPS37 & TPS38 family of devices which have dual channels.

4.3 RESET1/RESET2 Outputs

The RESET1 and RESET2 outputs on the device represent the effect of the voltage monitoring after operating on the inputs SENSE1 and SENSE2, respectively. The device on the TPS3760EVM is the TPS3760A012DYYR, which represents an undervoltage active-low open-drain output on RESET1 and is a single channel device. If using the EVM with another part in the TPS3760-Q1/TPS3760 family, adjustments need to be made to the default configuration to the EVM. For parts that use a push-pull topology instead of open-drain, you should depopulate the jumpers on J5 (pull-up to VDD for RESET1) or J6 (pull-up to VDD for RESET2). Additionally, if you want to use a different sized pull-up resistor on the reset pullups, either 10.0kΩ resistor at R2 or R3 can be replaced with another 0603 resistor. The RESET1 and RESET2 outputs can be pulled up to any voltage within the operating range by populating J5 on the middle and right pins for RESET1 and populating J6 on the middle and right pins for RESET2 and connecting a voltage to TP3 for RESET1 and a voltage to TP4 for RESET2.

4.4 Capacitor Time Delay Reset/$\overline{\text{MR}}$

The TPS3760 and TPS3760-Q1 family of devices contain two adjustable reset time delay pins that control the time with which the reset pins de-assert after they reach their valid condition. These pins also serve a dual purpose and act as a manual reset ($\overline{\text{MR}}$) when connected to logic ground. The user can adjust the configuration of these pins via the jumpers located at J11 and J12. Header J11 serves as the selectable option for CTR1/$\overline{\text{MR}}$ and header J12 serves as the selectable option for CTR2/$\overline{\text{MR}}$. Position DNI of the header (indicated by a DNI) connects the pin to a unstuffed 0603 capacitor pad for the user to solder on a capacitor of choice. The capacitor values for these jumpers are labeled on the board and are also listed in the jumper description section, and are as follows: for J11, from top to bottom, 10uF, 1uF, 100nF, 10nF, 1nF, DNI for a user specified value, and OPEN to be tied to GND for MR testing. For J12, from bottom to top, 10uF, 1uF, 100nF, 10nF, 1nF, DNI for a user specified

value, and OPEN to be tied to GND for MR testing. Please see the adjustable Reset Time Delay Configuration on the TPS3760-Q1 datasheet for more detailed information on user programming.

4.5 Capacitor Time Delay Sense/$\overline{\text{MR}}$

The TPS3760 and TPS3760-Q1 family of devices contain two adjustable sense time delay pins that control the time with which the reset pins assert after they reach their invalid condition. The user can adjust the configuration of these pins via the jumpers located at J9 and J10. Header J9 serves as the selectable option for CTS1 and header J10 serves as the selectable option for CTS2. The values of capacitors are labeled on the board and also in the jumper description section. For J9, they are, from bottom to top, DNI (for user defined capacitance), 1nF, 10nF, 100nF, 1uF, and 10uF. For J10, they are, from top to bottom, DNI (for user defined capacitance), 1nF, 10nF, 100nF, 1uF, and 10uF. Please see the Time Delay Configuration section on the TPS3760-Q1 datasheet for more detailed information on user programming.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265