User's Guide

TPS36Q1EVM Voltage Supervisor User Guide

ABSTRACT

This user's guide describes the TPS36Q1EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing and top and bottom board layouts.

Table of Contents

List of Figures

List of Tables

1 Trademarks

All trademarks are the property of their respective owners.

2 Introduction

The TPS36Q1EVM is an evaluation module (EVM) for the TPS3435-Q1, TPS3436-Q1, TPS35-Q1, and TPS36-Q1 voltage supervisors. These families are automotive-grade devices with support for undervoltage supervisor and watchdog functionality. Please see Table 2-1 for specific functions supported by each family. The TPS36Q1EVM is shipped pre-installed with the TPS3436CCCBGDDFRQ1 device, but can be used with any TPS3435-Q1, TPS3436-Q1, TPS35-Q1, or TPS36-Q1 device variant. The TPS3435-Q1, TPS3436-Q1, TPS35-Q1, and TPS36-Q1 families offer multiple pinout options. The TPS36Q1EVM offers connections to all input and output pins supported by various pinouts. Test points are provided to give the user access to an extra ground connection if needed for oscilloscope or multimeter measurements.

Table 2-1. Voltage Supervisors

	VOLTAGE SUPERVISION	WATCHDOG
TPS3435-Q1	None	Timeout
TPS3436-Q1	None	Window
TPS35-Q1	Undervoltage	Timeout
TPS36-Q1	Undervoltage	Window

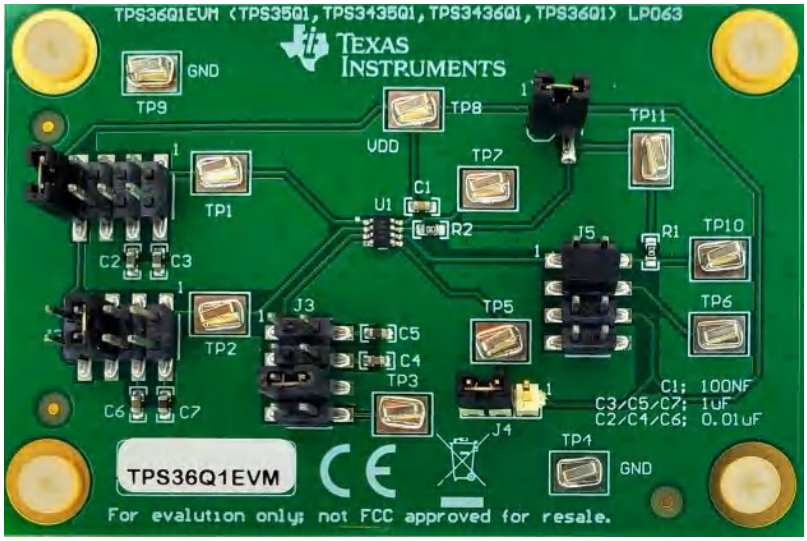

Figure 2-1. TPS36Q1EVM Board Top

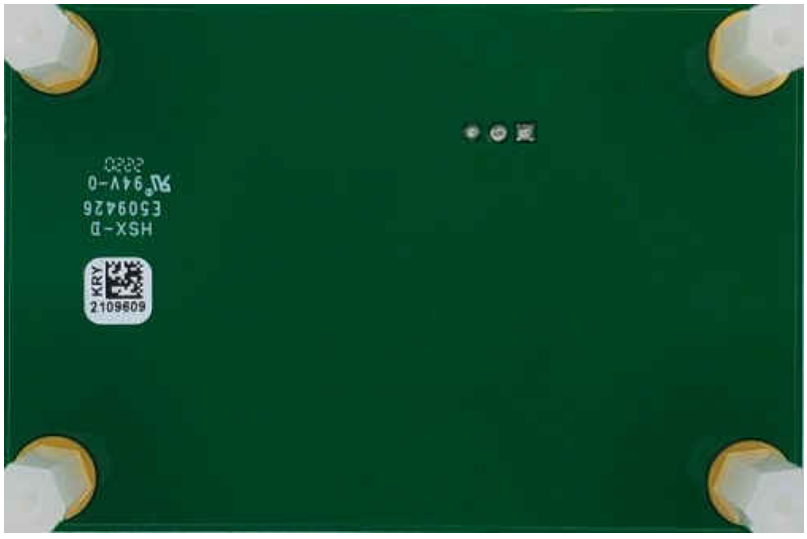

Figure 2-2. TPS36Q1EVM Board Bottom

2.1 Related Documentation

TPS3435-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet

TPS3436-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet

TPS35-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet

TPS36-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet

3 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TPS36Q1EVM schematic, bill of materials (BOM), and layout.

3.1 TPS36Q1EVM Schematic

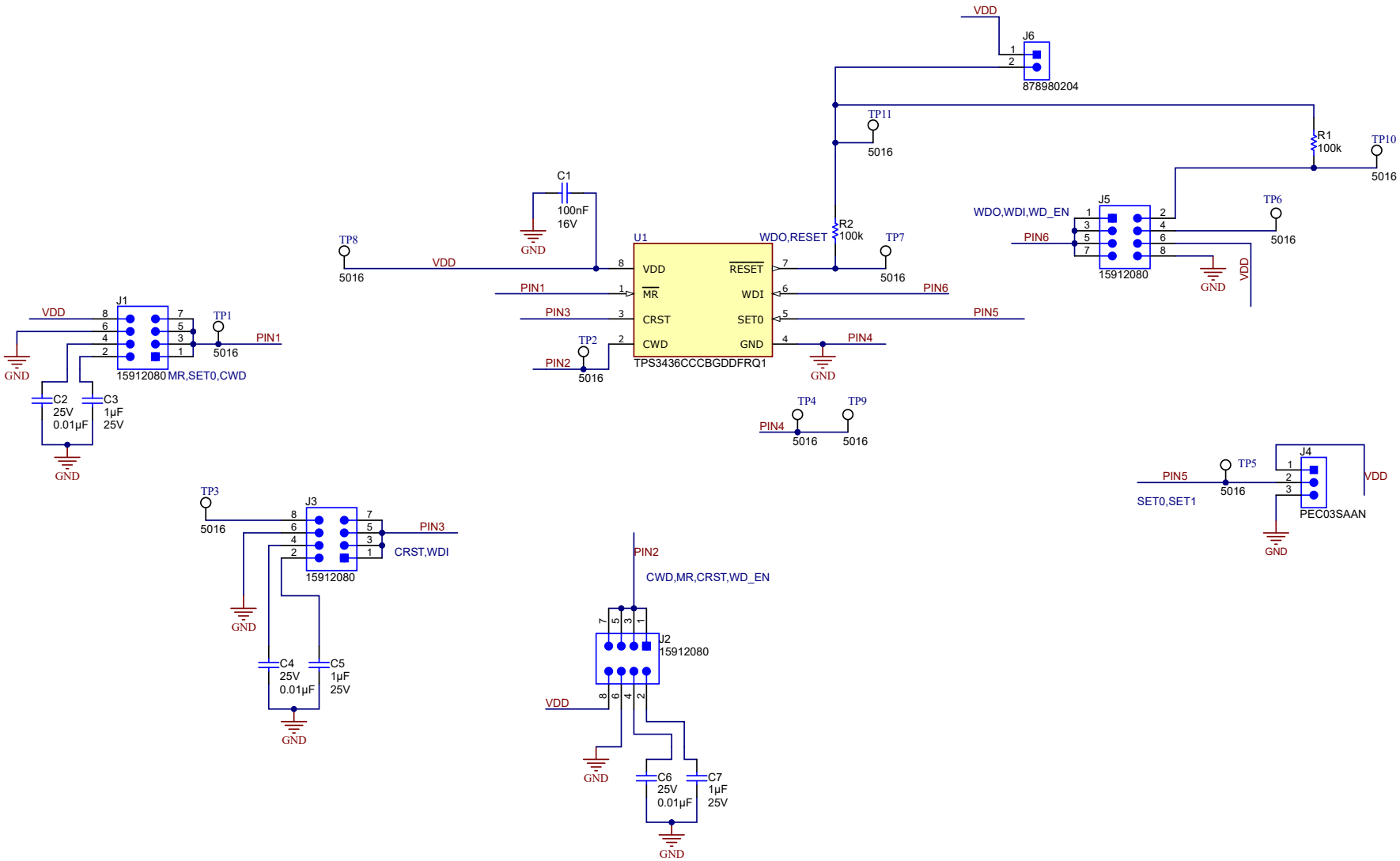

Figure 3-1. TPS36Q1EVM Schematic

3.2 TPS36Q1EVM Bill of Materials

Table 3-1. BOM

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		LP064	Any
C1	1	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 5%, X7R, 0603	0603	C0603C104J4RACTU	Kemet
C2	3	0.01 µF	CAP, CERM, 0.01 uF, 25 V, ± 1%, C0G/NP0, 0603	0603	C0603C103F3GACTU	Kemet
C3	3	0.01 µF	CAP, CERM, 1 µF, 25 V, ± 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips Panhead	7	NY PMS 440 0025 PH	B&F Fastner Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Keystone_1902C	1902C	Keystone
J1, J2, J3, J5	4		Header, 2.54 mm, 4x2, Tin, SMT	Molex_0015912080	15912080	Molex
J4	1		Header, 100mil, 3x1, Tin, TH	CONN_PEC03SAAN	PEC03SAAN	Sullins Connector Solutions
J6	1		Header, 2.54 mm, 2x1, Gold, R/A, SMT	Molex_87898-0204	878980204	Molex
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Label_650x200	THT-14-423-10	Brady
R1, R2	2	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	11		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone Electronics
U1	1		Automotive Nano IQ Precision Watchdog Timer SOT-23-8	DDF0008A-MFG	TPS3436CCCBGDDFRQ1	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial10-30	N/A	N/A

3.3 Layout and Component Placement

Figure 3-2 and Figure 3-3 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 3-4 and Figure 3-5 show the top and bottom layouts, Figure 3-6 and Figure 3-7 show the top and bottom layers, and Figure 3-8 shows the top solder mask of the EVM.

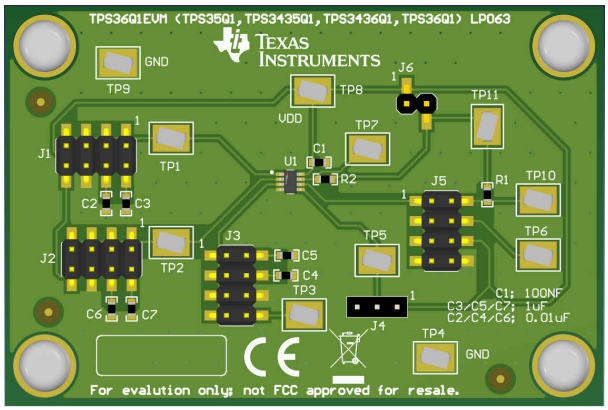

Figure 3-2. Component Placement—Top Assembly

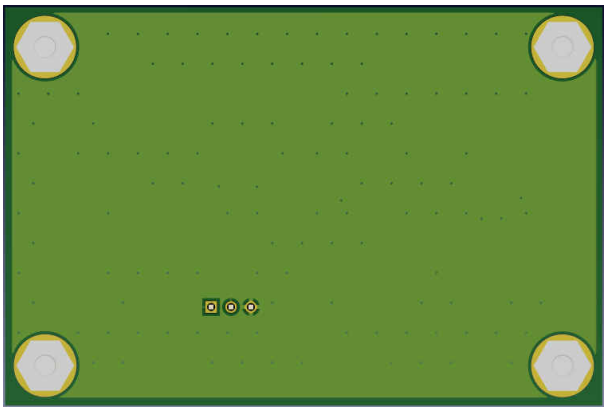

Figure 3-3. Component Placement—Bottom Assembly

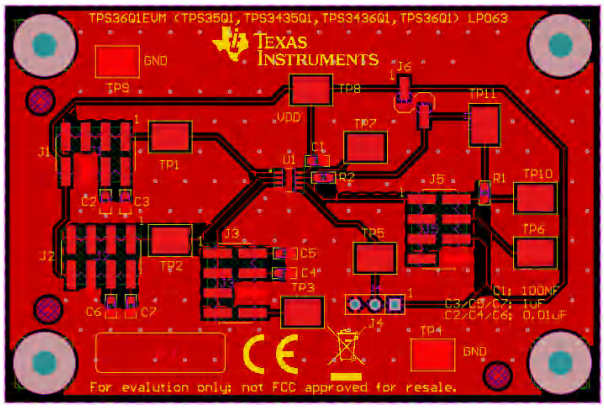

Figure 3-4. Layout—Top

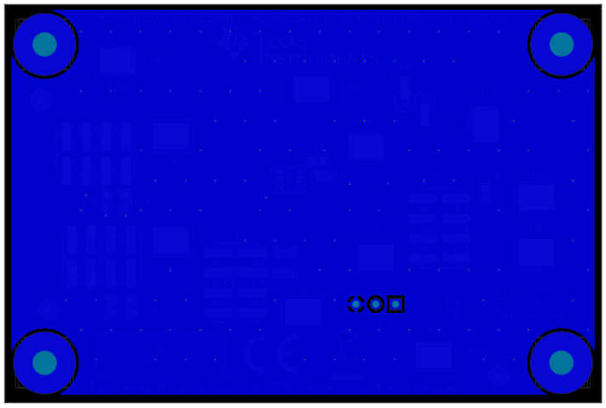

Figure 3-5. Layout—Bottom

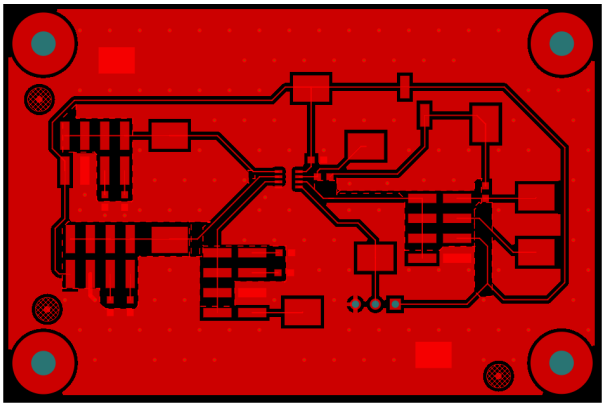

Figure 3-6. Top Layer

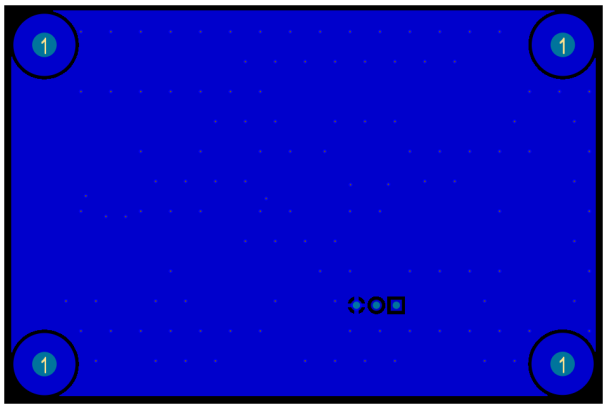

Figure 3-7. Bottom Layer

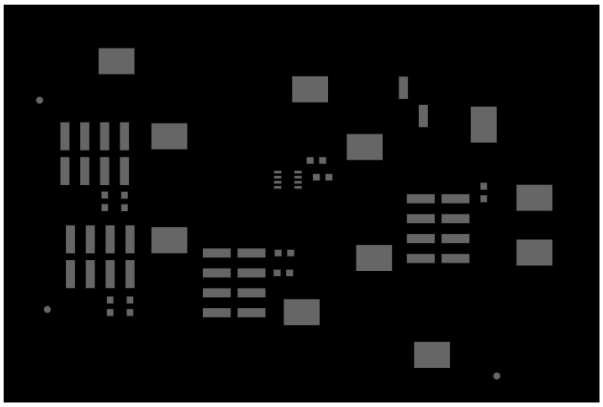

Figure 3-8. Top Solder Mask

4 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM.

4.1 EVM Jumpers

Tables 4-1, 4-2, 4-3, and 4-4 list the default jumper connections and functional descriptions for each device configuration. Each pinout configuration detailed in this section applies to all TPS3435-Q1, TPS3436-Q1, TPS35-Q1, and TPS36-Q1 device families. Please note that for pinouts A, B and C, Pin 7 refers to $\overline{\text{RESET}}$ for the TPS35-Q1 and TPS36-Q1 devices and $\overline{\text{WDO}}$ for the TPS3435-Q1 and TPS3436-Q1 devices.

Table 4-1. Pinout A Onboard Jumpers

PIN NUMBER / NAME	JUMPER CONNECTION	DEFAULT CONNECTION	DESCRIPTION
Pin 1 / $\overline{\text{MR}}$	J1	Closed (pin 7, pin 8)	Jumper J1 configures the $\overline{\text{MR}}$ pin. Connect a shunt jumper to pins 7-8 of jumper J1 to enable the device (logic high) or to pins 5-6 to disable the device (logic low).
Pin 2 / CWD	J2	Closed (pin 1, pin 2)	Jumper J2 configures the CWD pin. Connect a shunt jumper to pins 7-8 to connect to V_{DD}, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.8 CWD and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.
Pin 3 / CRST	J3	Closed (pin 1, pin 2)	Jumper J3 configures the CRST pin. Connect a shunt jumper to pins 7-8 to connect to V_{DD}, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.7 CRST and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.
Pin 5 / SET0	J4	Closed (pin 2, pin 3)	Jumper J4 configures the SET0 pin. Connect a shunt jumper to pins 1-2 of jumper J3 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 6 / WDI	J5	Closed (pin 3, pin 4)	Jumper J5 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for $\overline{\text{RESET}}$/$\overline{\text{WDO}}$ to not assert.
Pin 7 / $\overline{\text{RESET}}$ / $\overline{\text{WDO}}$	J6	Closed (pin 1, pin 2)	Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the $\overline{\text{RESET}}$ output high. Disconnect pins 1-2 if using a push-pull variant.

Table 4-2. Pinout B Onboard Jumpers

PIN NUMBER / NAME	JUMPER CONNECTION	DEFAULT CONNECTION	DESCRIPTION
Pin 1 / SET0	J1	Closed (pin 5, pin 6)	Jumper J1 configures the SET0 pin. Connect a shunt jumper to pins 5-6 of jumper J1 to input a logic high or to pins 7-8 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 2 / CWD	J2	Closed (pin 1, pin 2)	Jumper J2 configures the CWD pin. Connect a shunt jumper to pins 7-8 to connect to V_{DD}, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.8 CWD and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.
Pin 3 / CRST	J3	Closed (pin 1, pin 2)	Jumper J3 configures the CRST pin. Connect a shunt jumper to pins 7-8 to connect to V_{DD}, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.7 CRST and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.
Pin 5 / SET1	J4	Closed (pin 2, pin 3)	Jumper J4 configures the SET1 pin. Connect a shunt jumper to pins 1-2 of jumper J4 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 6 / WDI	J5	Closed (pin 3, pin 4)	Jumper J5 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for $\overline{\text{RESET}}$/$\overline{\text{WDO}}$ to not assert.
Pin 7 / $\overline{\text{RESET}}$ / $\overline{\text{WDO}}$	J6	Closed (pin 1, pin 2)	Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the $\overline{\text{RESET}}$ output high. Disconnect pins 1-2 if using a push-pull variant.

Table 4-3. Pinout C Onboard Jumpers

PIN NUMBER / NAME	JUMPER CONNECTION	DEFAULT CONNECTION	DESCRIPTION
Pin 1 / SET0	J1	Closed (pin 5, pin 6)	Jumper J1 configures the SET0 pin. Connect a shunt jumper to pins 5-6 of jumper J1 to input a logic high or to pins 7-8 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 2 / $\overline{\text{MR}}$	J2	Closed (pin 7, pin 8)	Jumper J2 configures the $\overline{\text{MR}}$ pin. Connect a shunt jumper to pins 5-6 of jumper J2 to input a logic low or to pins 7-8 to input a logic high.
Pin 3 / WDI	J3	Closed (pin 7, pin 8)	Jumper J3 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for $\overline{\text{RESET}}$/$\overline{\text{WDO}}$ to not assert.
Pin 5 / SET1	J4	Closed (pin 2, pin 3)	Jumper J4 configures the SET1 pin. Connect a shunt jumper to pins 1-2 of jumper J4 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 6 / WD-EN	J5	Closed (pin 5, pin 6)	Jumper J5 configures the WD-EN pin. Connect a shunt jumper to pins 5-6 of jumper J5 to enable the watchdog timer (logic high) and pins 7-8 to disable the watchdog timer (logic low).
Pin 7 / $\overline{\text{RESET}}$ / $\overline{\text{WDO}}$	J6	Closed (pin 1, pin 2)	Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the $\overline{\text{RESET}}$ output high. Disconnect pins 1-2 if using a push-pull variant.

Table 4-4. Pinout D Onboard Jumpers (TPS35-Q1/TPS36-Q1 Only)

PIN NUMBER / NAME	JUMPER CONNECTION	DEFAULT CONNECTION	DESCRIPTION
Pin 1 / SET0	J1	Closed (pin 5, pin 6)	Jumper J1 configures the SET0 pin. Connect a shunt jumper to pins 5-6 of jumper J1 to input a logic high or to pins 7-8 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 2 / WD-EN	J2	Closed (pin 7, pin 8)	Jumper J2 configures the WD-EN pin. Connect a shunt jumper to pins 5-6 of jumper J5 to enable the watchdog timer (logic high) and pins 7-8 to disable the watchdog timer (logic low).
Pin 3 / WDI	J3	Closed (pin 7, pin 8)	Jumper J3 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for $\overline{\text{RESET}}$/$\overline{\text{WDO}}$ to not assert.
Pin 5 / SET1	J4	Closed (pin 2, pin 3)	Jumper J4 configures the SET1 pin. Connect a shunt jumper to pins 1-2 of jumper J4 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.
Pin 6 / $\overline{\text{WDO}}$	J5	Closed (pin 3, pin 4)	Jumper J5 configures the $\overline{\text{WDO}}$ pin. Connect a shunt jumper to pins 1-2 if using an open-drain variant to activate pull-up resistor R1 and pull the $\overline{\text{WDO}}$ output high. Connect pins 3-4 if using a push-pull variant.
Pin 7 / $\overline{\text{RESET}}$	J6	Closed (pin 1, pin 2)	Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the $\overline{\text{RESET}}$ output high. Disconnect pins 1-2 if using a push-pull variant.

4.2 EVM Test Points

Test points are placed throughout the board and are used to verify pin functionality. Each device configuration option letter has different pinouts, so each test point can serve different purposes depending on the chosen IC. For example, test point 1 (TP1) is used to monitor pin 1, but the functionality of pin 1 varies between $\overline{\text{MR}}$, SET0, and CWD as seen in Figure 4-1. Jumpers can be used with shunt jumpers to connect two pins together in order to serve multiple testing purposes. For example, connecting pins 7-8 of jumper J1 connects pin 1 to V_{DD}, a logic high, and connecting pins 5-6 of jumper J1 connects pin 1 to GND, a logic low. Pins can also be connected to delay capacitors via the jumpers, and these connections can be used to adjust programmable timeout periods.

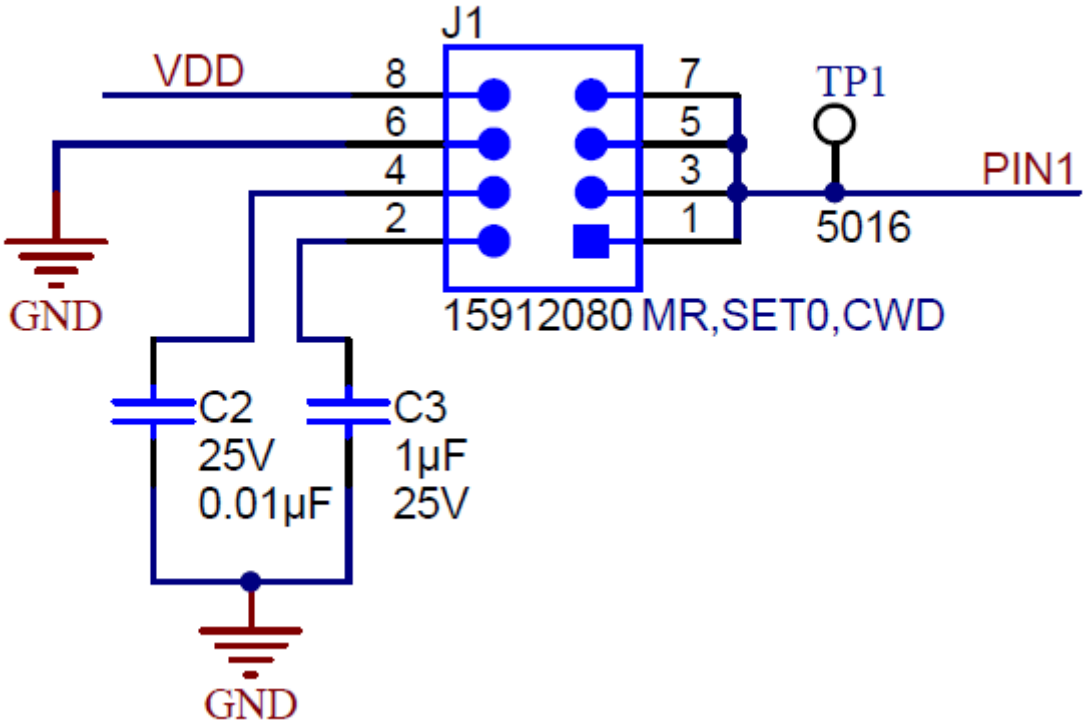

Figure 4-1. Schematic Closeup

5 EVM Setup and Operation

This section describes the functionality and operation of the TPS36Q1EVM. Even though this EVM comes with the TPS3436CCCBGDDFRQ1 variant, this section will cover the EVM utilization with the TPS36-Q1, TPS35-Q1, and TPS3435-Q1 installed on the board. All timing based parameters of this device are located in the respective device's datasheet.

5.1 Input Power (V_{DD})

The input voltage (V_{DD}) is connected through TP8 on the board. The input voltage range is 1.04V to 6.0 V. The TPS35-Q1 and the TPS36-Q1 families offer voltage supervision on the V_{DD} pin and supervisor output on the $\overline{RESET}$ pin. The voltage threshold of the supervisor is dependent on the specific device used. Please refer to the datasheet for additional details.

5.2 $\overline{RESET}$

For the TPS35-Q1 and TPS36-Q1 options A, B, and C, the $\overline{RESET}$ pin will assert on either V_{DD} going below the supervisor threshold, the $\overline{MR}$ pin being pulled low, or the watchdog detecting a fault. To access the $\overline{RESET}$ output, a probe can be attached to TP7. For pinout option D devices, supervisor faults are mapped to the $\overline{RESET}$ pin and watchdog faults are mapped to the $\overline{WDO}$ pin.

Please note that if using a push-pull output variant, the shunt jumper on J6 must be removed as a pull-up is not needed.

5.3 Manual Reset ($\overline{MR}$)

Pinout options A and C support $\overline{MR}$ functionality. The Manual Reset ($\overline{MR}$) can be utilized by either J2 (option C) or J1 (option A) headers. By installing a shunt jumper on pins 5-6 of J1 or J2, the $\overline{MR}$ pin is connected to ground. Moving the shunt jumper to pins 7-8 will connect the $\overline{MR}$ pin to V_{DD}. For the TPS35-Q1 and TPS36-Q1 devices, pulling the $\overline{MR}$ pin LOW will assert the $\overline{RESET}$ signal and deassert the $\overline{WDO}$ signal. For the TPS3435-Q1 and TPS3436-Q1 devices, pulling the $\overline{MR}$ pin LOW will assert the $\overline{WDO}$ signal. Pulling the MR pin HIGH will return the $\overline{RESET}$ and $\overline{WDO}$ outputs to their deasserted states after the t_D time delay.

5.4 SET0 and SET1

The function of the SETx pins will vary based on the device used in the EVM. Please refer to the device data sheet for the functionality. Drive SETx pins to logic 1 (connect to V_{DD}) or logic 0 (connect to GND) as per the device pinout and functionality requirements. Refer to Tables 4-1, 4-2, 4-3, and 4-4 for suggested jumper connections.

5.5 Watchdog Enable (WD_EN)

The WD_EN pin is only available in option C and D devices. This pin is used to ENABLE (logic 1) or disable (logic 0) the watchdog functionality of the device. To utilize this pin, configure J5, for option C devices, or J2 for option D devices. Refer to Table 4-3 and Table 4-4 for suggested jumper connections.

5.6 Watchdog Input (WDI)

WDI is a falling edge triggered watchdog input. TPS35-Q1 and TPS3435-Q1 devices support timeout watchdog monitor operation, while the TPS36-Q1 and TPS3436-Q1 devices support window watchdog monitor operation. Refer respective data sheet for timing related requirements. Refer to Tables 4-1, 4-2, 4-3, and 4-4 for suggested jumper connections.

5.7 Watchdog Output ($\overline{WDO}$)

The $\overline{WDO}$ output is asserted in the event of a watchdog error. For TPS35-Q1 and TPS36-Q1 devices, the $\overline{WDO}$ pin is offered in pinout option D. For TPS3435-Q1 and TPS3436-Q1 devices, the $\overline{WDO}$ pin is offered in options A, B, and C. Refer to Tables 4-1, 4-2, 4-3, and 4-4 for suggested jumper connections.

5.8 CRST

A capacitor between the CRST pin and GND sets the output assert time t_D. The TPS36Q1EVM offers two pre-installed options: 0.01µF and 1µF. These capacitors correspond to 49.5ms and 4.95s t_D time delays, respectively. Refer to Table 4-1 and Table 4-2 for suggested jumper settings. If other timing option is needed,

the capacitor may be replaced. Refer to the respective device data sheet to determine the capacitor value for required timing.

5.9 CWD

A capacitor between the CWD pin and GND sets the watchdog timeout period t_{WD} for TPS35-Q1 and TPS3435-Q1 devices or the watchdog close window period t_{WC} for TPS36-Q1 and TPS3436-Q1 devices. The TPS36Q1EVM offers two pre-installed options: 0.01µF and 1µ. These capacitors correspond to 49.5ms and 4.95s t_{WD} time delays for the TPS35-Q1 and TPS3435-Q1 devices, respectively. The t_{WD} values are determined by the SET0 and SET1 pins; please refer to Table 5-1 for a list of the values and the data sheet for the t_{WD} calculation. Refer to Table 4-1 and Table 4-2 for suggested jumper settings. If other timing option is needed, the capacitor can be replaced. Refer to the respective device data sheet to determine the capacitor value for required timing.

Table 5-1. Typical t_{WC} Values for TPS36-Q1 and TPS3436-Q1

SET0	SET1	0.01µF	1µF
0	0	0.792s	79.2s
0	1	0.396s	39.6s
1	0	Disabled/"00" if using Pinouts C or D	
1	1	0.099s	9.9s

6 EVM Performance Results

The following measurements are taken using the TPS3436CCCBGDDFRQ1 with SET0=0 and SET1=0.

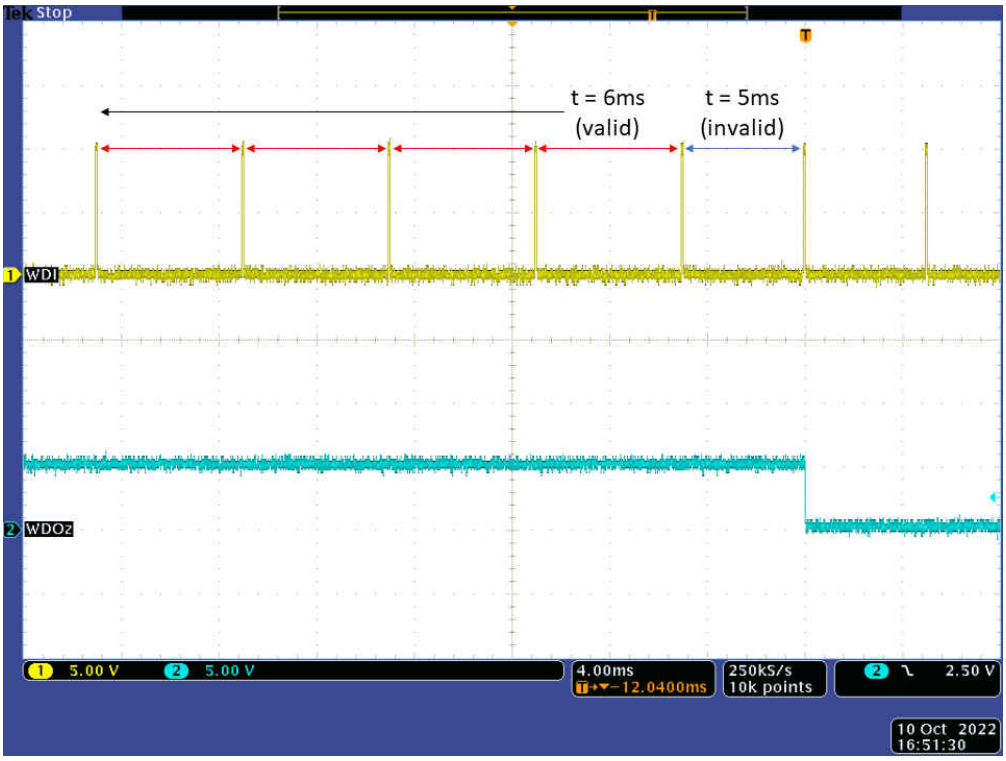

Figure 6-1. Early Fault

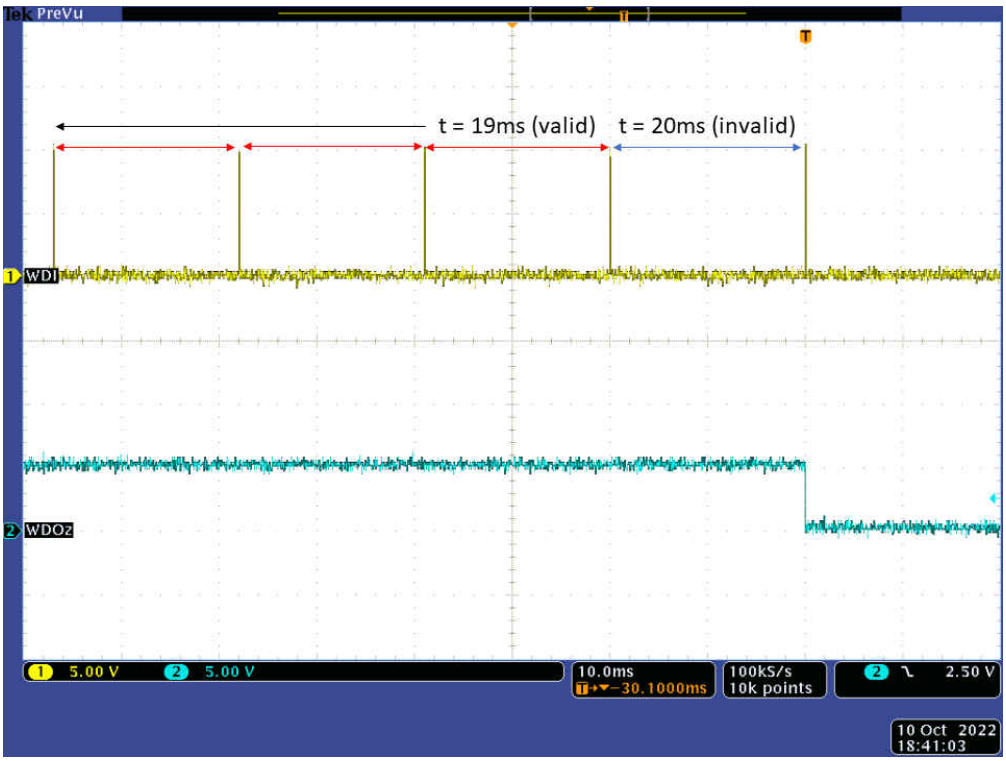

Figure 6-2. Late Fault

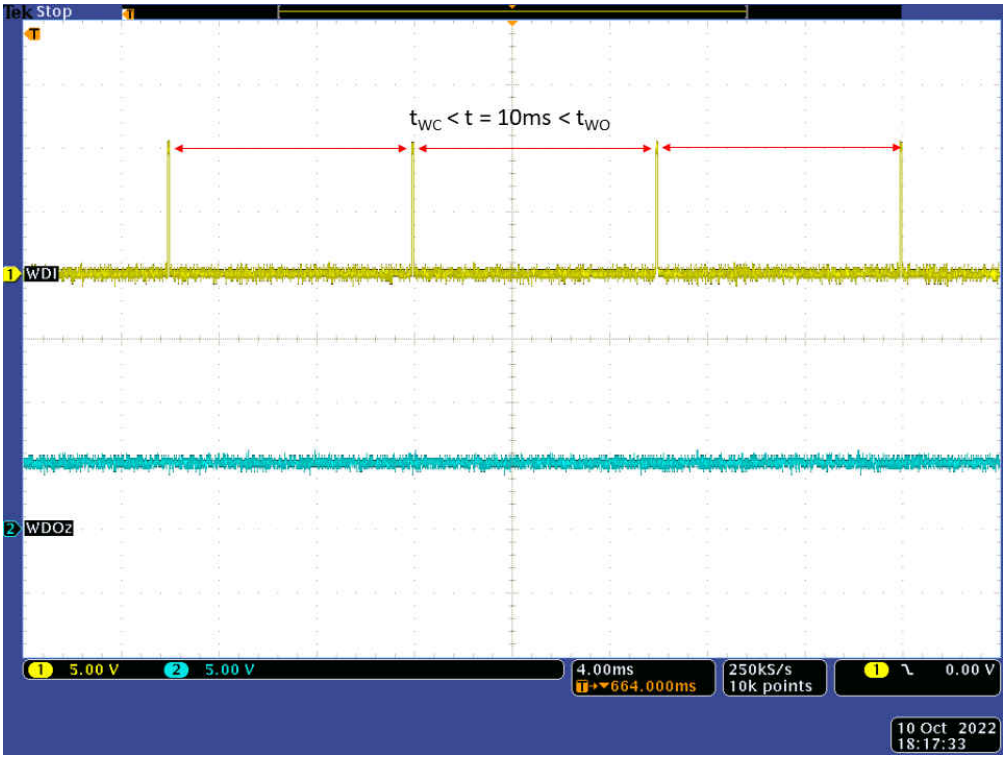

Figure 6-3. Valid Pulse

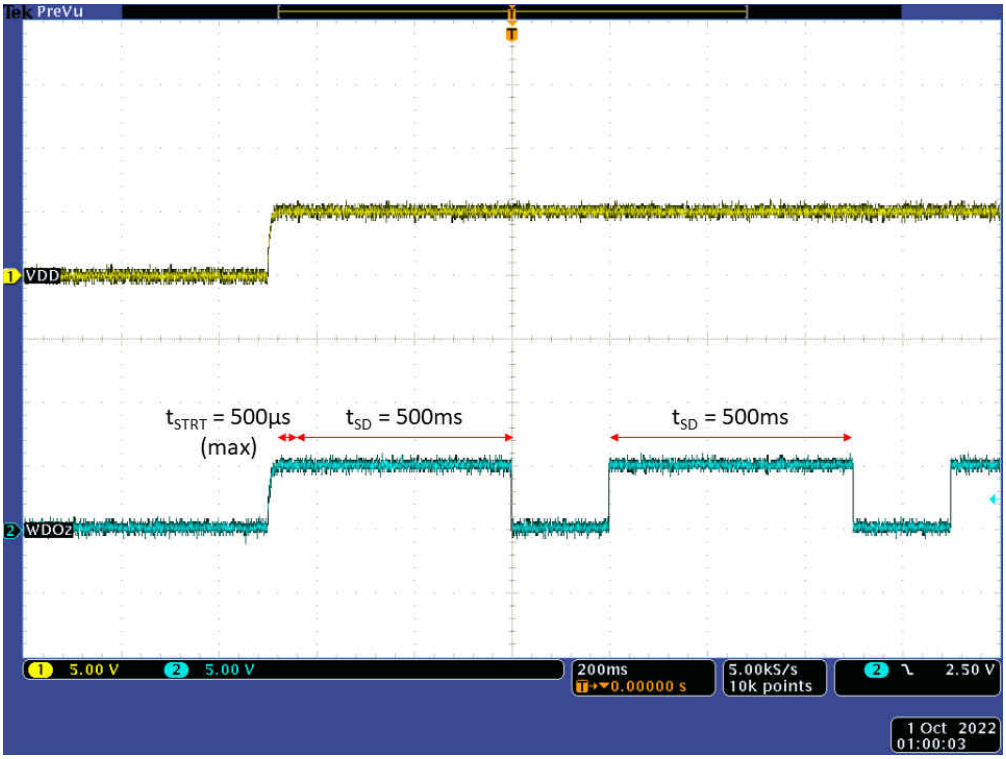

Figure 6-4. Startup Delay

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2022	*	Initial Release

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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