Technical Reference Manual

TPS6521903 Technical Reference Manual

ABSTRACT

This Technical Reference Manual (TRM) can be used as a reference for the default register bits after the NVM download. The end user is responsible for validating the NVM settings for proper system use including any safety impact. This TRM does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the device data sheet available on the TPS65219 product folder at ti.com.

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Trademarks

1 Introduction

The TPS65219/TPS65220 PMIC is a cost and space optimized solution that has flexible mapping to support the power requirements from different processors and SoCs. This PMIC contains seven regulators; 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). Additionally, it has I2C, GPIOs and configurable multi-function pins. TPS65219 is characterized for -40°C to +105°C ambient temperature and TPS65220 is characterized for -40°C to +125°C ambient temperature. The extended PMIC temperature range of TPS65220 allows support of AM64x based systems operating at higher temperatures. For safety sensitive applications, TPS65220 is functional safety capable. Therefore the TPS65220 development process is a TI-quality managed process, also functional safety FIT rate calculation and Failure mode distribution (FMD) is available for TPS65220. Whenever entering the INITIALIZE state, the PMIC reads its memory and loads the registers with the content from the EEPROM. The EEPROM loading takes approximately 2.3ms. The power-up sequence can only be executed after the EEPROM-load and all rails are discharged below the SCG threshold. This document describes the default configuration programmed on TPS6521903.

Note

The NVM configuration described in this document is ideal for the application described below but can also be used to power other processors or SoCs with equivalent power requirements:

- Processor: AM62, AM64
- CORE voltage: 0.75V
- Memory: DDR4
- Input Supply (VSYS, PVIN_Bx): 3.3V

2 EEPROM Device Settings

The following sections describe the default configuration on the EEPROM-backed registers. During the power-down-sequence, non-EEPROM-backed bits get reset, with the exception of unmasked interrupt bits and DISCHARGE_EN bits.

2.1 Device ID

This section lists all the register settings to identify the supported temperature and the NVM ID with the corresponding revision that represent a list of default register settings.

Table 2-1. Device ID

Register Name	Field Name	Value	Description
TI_DEV_ID	TI_DEVICE_ID	0x00	Device specific ID code to identify supported ambient and junction temperature.
NVM_ID	TI_NVM_ID	0x03	Identification code for the NVM ID
FACTORY_CONFIG_2	NVM_REVISION	0x2	Identification code for the NVM revision
I2C_ADDRESS_REG	I2C_ADDRESS	0x30	I2C address

2.2 Enable Settings

This section describes the PMIC rails that are enabled in Active and Standby state. Any rail that is disabled by default has the option to be enabled through I2C once the device is in Active state and I2C communication is available.

Table 2-2. Enable Settings - ACTIVE state

PMIC Rail	Register Name	Field Name	Value	Description
BUCK1	ENABLE_CTRL	BUCK1_EN	0x1	Enabled
BUCK2	ENABLE_CTRL	BUCK2_EN	0x1	Enabled
BUCK3	ENABLE_CTRL	BUCK3_EN	0x1	Enabled
LDO1	ENABLE_CTRL	LDO1_EN	0x1	Enabled
LDO2	ENABLE_CTRL	LDO2_EN	0x1	Enabled
LDO3	ENABLE_CTRL	LDO3_EN	0x1	Enabled
LDO4	ENABLE_CTRL	LDO4_EN	0x1	Enabled
GPO1	GENERAL_CONFIG	GPO1_EN	0x0	The GPO1 function is disabled. The output state is low.
GPO2	GENERAL_CONFIG	GPO2_EN	0x1	The GPO2 function is enabled. The output state is Hi-Z.
GPIO	GENERAL_CONFIG	GPIO_EN	0x0	The GPIO function is disabled. The output state is low.

Table 2-3. Enable Settings - STANBY (STBY) state

PMIC Rail	Register Name	Field Name	Value	Description
BUCK1	STBY_1_CONFIG	BUCK1_STBY_EN	0x1	Enabled in STBY Mode
BUCK2	STBY_1_CONFIG	BUCK2_STBY_EN	0x1	Enabled in STBY Mode
BUCK3	STBY_1_CONFIG	BUCK3_STBY_EN	0x1	Enabled in STBY Mode
LDO1	STBY_1_CONFIG	LDO1_STBY_EN	0x1	Enabled in STBY Mode
LDO2	STBY_1_CONFIG	LDO2_STBY_EN	0x1	Enabled in STBY Mode
LDO3	STBY_1_CONFIG	LDO3_STBY_EN	0x1	Enabled in STBY Mode
LDO4	STBY_1_CONFIG	LDO4_STBY_EN	0x1	Enabled in STBY Mode
GPO1	STBY_2_CONFIG	GPO1_STBY_EN	0x0	Disabled in STBY Mode
GPO2	STBY_2_CONFIG	GPO2_STBY_EN	0x1	Enabled in STBY Mode
GPIO	STBY_2_CONFIG	GPIO_STBY_EN	0x0	Disabled in STBY Mode

2.3 Regulator Voltage Settings

This section describes how each of the PMIC power resources were configured.

Table 2-4. Buck Regulator Settings

PMIC Rail	Register Name	Field Name	Value	Description
Bucks Switching Mode (Global for all Buck regulators)	BUCKS_CONFIG	BUCK_FF_ENABLE	0x0	Quasi-fixed frequency mode
	BUCKS_CONFIG	BUCK_SS_ENABLE	0x0	Spread spectrum disabled
BUCK1	BUCK1_VOUT	BUCK1_VSET	0x6	0.750V
	BUCK1_VOUT	BUCK1_UV_THR_SEL	0x0	-5% UV detection level
	BUCK1_VOUT	BUCK1_BW_SEL	0x1	high bandwidth
BUCK2	BUCK2_VOUT	BUCK2_VSET	0x24	1.800V
	BUCK2_VOUT	BUCK2_UV_THR_SEL	0x0	-5% UV detection level
	BUCK2_VOUT	BUCK2_BW_SEL	0x1	high bandwidth
	BUCKS_CONFIG	BUCK2_PHASE_CONFIG	0x3	270 degrees (only applicable if Bucks are configured for fixed frequency)
BUCK3	BUCK3_VOUT	BUCK3_VSET	0x18	1.200V
	BUCK3_VOUT	BUCK3_UV_THR_SEL	0x0	-5% UV detection level
	BUCK3_VOUT	BUCK3_BW_SEL	0x1	high bandwidth
	BUCKS_CONFIG	BUCK3_PHASE_CONFIG	0x2	180 degrees (only applicable if Bucks are configured for fixed frequency)

Note

- When Bucks are configured for quasi-fixed frequency (**BUCK_FF_ENABLE=0x0**), changing the switching mode between auto-PFM and forced-PWM can be triggered by I2C (MODE_I2C_CTRL) or with one of the multi-function pins (MODE/RESET or MODE/STBY) if one of them is configured as MODE. "Forced PWM" has priority over "Auto PFM".
- "BUCK2_PHASE_CONFIG", "BUCK3_PHASE_CONFIG" and "BUCK_SS_ENABLE" are only applicable when the Buck regulators are configured for fixed frequency (**BUCK_FF_ENABLE=0x1**).

Table 2-5. LDO Regulator Settings

PMIC Rail	Setting	Register Name	Field Name	Value	Description
LDO1	LDO1 output voltage	LDO1_VOUT	LDO1_VSET	0x36	3.300V
	LDO1 configuration	LDO1_VOUT	LDO1_LSW_CONFIG	0x0	Not Applicable (LDO1 not configured as load-switch)
		LDO1_VOUT	LDO1_BYP_CONFIG	0x1	LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG=0x0)
	LDO1 UV threshold	GENERAL_CONFIG	LDO1_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)
LDO2	LDO2 output voltage	LDO2_VOUT	LDO2_VSET	0x5	0.850V / reserved
	LDO2 configuration	LDO2_VOUT	LDO2_LSW_CONFIG	0x0	Not Applicable (LDO2 not configured as load-switch)
		LDO2_VOUT	LDO2_BYP_CONFIG	0x0	LDO2 configured as LDO (only applicable if LDO2_LSW_CONFIG=0x0)
	LDO2 UV threshold	GENERAL_CONFIG	LDO2_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)
LDO3	LDO3 output voltage	LDO3_VOUT	LDO3_VSET	0x18	1.800V
	LDO3 configuration	LDO3_VOUT	LDO3_LSW_CONFIG	0x0	LDO Mode
	LDO ramp configuration	LDO3_VOUT	LDO3_SLOW_PU_RAMP	0x1	Slow ramp for power-up (~3ms)
	LDO3 UV threshold	GENERAL_CONFIG	LDO3_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)
LDO4	LDO4 output voltage	LDO4_VOUT	LDO4_VSET	0x26	2.500V
	LDO3 configuration	LDO4_VOUT	LDO4_LSW_CONFIG	0x0	LDO Mode
	LDO ramp configuration	LDO4_VOUT	LDO4_SLOW_PU_RAMP	0x1	Slow ramp for power-up (~3ms)
	LDO4 UV threshold	GENERAL_CONFIG	LDO4_UV_THR	0x0	-5% UV detection level (only applicable if configured as LDO)

Note

- If a LDO is configured in bypass-mode or LSW-mode, UV-detection is not supported.
- If an LDO is configured in bypass-mode, the corresponding PVIN_LDOx supply must match the configured output voltage in the LDOx_VOUT register.
- If LDO is configured as load-switch (LSW_mode), the desired voltage does not need to be configured in the LDOx_VOUT register.
- In bypass- or LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance.
- If LDO1 or LDO2 is configured as bypass, it allows voltage and function changes between LDO (VOUT=1.8V) and VOUT=VSET register setting. This voltage/function change can be triggered by hardware (using the VSEL_SD pin when configured as SD) or by software (VSEL_SD_I2C_CTRL).

2.4 Power Sequence Settings

This section breaks out the power sequence settings for the device including the power-up/power-down slot assignment and duration. There may be slots in which no rail nor GPO is assigned to ramp. In this case, we use a combination of slot durations to achieve desired delay times or allow to increase/reduce the timings.

2.4.1 Power Sequence Settings - Slot assignments

Table 2-6. Power-UP Sequence Settings - Slot Assignments

	Register Name	Field Name	Value	Description
BUCK1	BUCK1_SEQUENCE_SLOT	BUCK1_SEQUENCE_ON_SLOT	0x4	slot 4
BUCK2	BUCK2_SEQUENCE_SLOT	BUCK2_SEQUENCE_ON_SLOT	0x2	slot 2
BUCK3	BUCK3_SEQUENCE_SLOT	BUCK3_SEQUENCE_ON_SLOT	0x3	slot 3
LDO1	LDO1_SEQUENCE_SLOT	LDO1_SEQUENCE_ON_SLOT	0x2	slot 2
LDO2	LDO2_SEQUENCE_SLOT	LDO2_SEQUENCE_ON_SLOT	0x5	slot 5
LDO3	LDO3_SEQUENCE_SLOT	LDO3_SEQUENCE_ON_SLOT	0x2	slot 2
LDO4	LDO4_SEQUENCE_SLOT	LDO4_SEQUENCE_ON_SLOT	0x2	slot 2
GPO1	GPO1_SEQUENCE_SLOT	GPO1_SEQUENCE_ON_SLOT	0x6	slot 6
GPO2	GPO2_SEQUENCE_SLOT	GPO2_SEQUENCE_ON_SLOT	0x0	slot 0
GPIO	GPIO_SEQUENCE_SLOT	GPIO_SEQUENCE_ON_SLOT	0x6	slot 6
nRSTOUT	nRST_SEQUENCE_SLOT	nRST_SEQUENCE_ON_SLOT	0x8	slot 8

Note

PMIC rails are turned ON during the power-up sequence if the corresponding EN bit on section "Enable Setting" is set to 0x01.

Table 2-7. Power-Down Sequence Settings - Slot Assignments

	Register Name	Field Name	Value	Description
BUCK1	BUCK1_SEQUENCE_SLOT	BUCK1_SEQUENCE_OFF_SLOT	0x2	slot 2
BUCK2	BUCK2_SEQUENCE_SLOT	BUCK2_SEQUENCE_OFF_SLOT	0x2	slot 2
BUCK3	BUCK3_SEQUENCE_SLOT	BUCK3_SEQUENCE_OFF_SLOT	0x0	slot 0
LDO1	LDO1_SEQUENCE_SLOT	LDO1_SEQUENCE_OFF_SLOT	0x2	slot 2
LDO2	LDO2_SEQUENCE_SLOT	LDO2_SEQUENCE_OFF_SLOT	0x0	slot 0
LDO3	LDO3_SEQUENCE_SLOT	LDO3_SEQUENCE_OFF_SLOT	0x2	slot 2
LDO4	LDO4_SEQUENCE_SLOT	LDO4_SEQUENCE_OFF_SLOT	0x2	slot 2
GPO1	GPO1_SEQUENCE_SLOT	GPO1_SEQUENCE_OFF_SLOT	0x0	slot 0
GPO2	GPO2_SEQUENCE_SLOT	GPO2_SEQUENCE_OFF_SLOT	0x2	slot 2
GPIO	GPIO_SEQUENCE_SLOT	GPIO_SEQUENCE_OFF_SLOT	0x0	slot 0
nRSTOUT	nRST_SEQUENCE_SLOT	nRST_SEQUENCE_OFF_SLOT	0x0	slot 0

2.4.2 Power Sequence Settings - Slot Durations

Table 2-8. Power Sequence Settings - Power-UP Slot Durations

	Register Name	Field Name	Value	Description
SLOT0	POWER_UP_SLOT_DURATION_1	POWER_UP_SLOT_0_DURATION	0x3	10ms
SLOT1	POWER_UP_SLOT_DURATION_1	POWER_UP_SLOT_1_DURATION	0x0	0ms
SLOT2	POWER_UP_SLOT_DURATION_1	POWER_UP_SLOT_2_DURATION	0x2	3ms
SLOT3	POWER_UP_SLOT_DURATION_1	POWER_UP_SLOT_3_DURATION	0x1	1.5ms
SLOT4	POWER_UP_SLOT_DURATION_2	POWER_UP_SLOT_4_DURATION	0x1	1.5ms
SLOT5	POWER_UP_SLOT_DURATION_2	POWER_UP_SLOT_5_DURATION	0x1	1.5ms
SLOT6	POWER_UP_SLOT_DURATION_2	POWER_UP_SLOT_6_DURATION	0x3	10ms
SLOT7	POWER_UP_SLOT_DURATION_2	POWER_UP_SLOT_7_DURATION	0x1	1.5ms

Table 2-8. Power Sequence Settings - Power-UP Slot Durations (continued)

	Register Name	Field Name	Value	Description
SLOT8	POWER_UP_SLOT_DURATION_3	POWER_UP_SLOT_8_DURATION	0x3	10ms
SLOT9	POWER_UP_SLOT_DURATION_3	POWER_UP_SLOT_9_DURATION	0x0	0ms
SLOT10	POWER_UP_SLOT_DURATION_3	POWER_UP_SLOT_10_DURATION	0x0	0ms
SLOT11	POWER_UP_SLOT_DURATION_3	POWER_UP_SLOT_11_DURATION	0x0	0ms
SLOT12	POWER_UP_SLOT_DURATION_4	POWER_UP_SLOT_12_DURATION	0x0	0ms
SLOT13	POWER_UP_SLOT_DURATION_4	POWER_UP_SLOT_13_DURATION	0x0	0ms
SLOT14	POWER_UP_SLOT_DURATION_4	POWER_UP_SLOT_14_DURATION	0x0	0ms
SLOT15	POWER_UP_SLOT_DURATION_4	POWER_UP_SLOT_15_DURATION	0x0	0ms

Table 2-9. Power Sequence Settings - Power-Down Slot Durations

	Register Name	Field Name	Value	Description
SLOT0	POWER_DOWN_SLOT_DURATION_1	POWER_DOWN_SLOT_0_DURATION	0x3	10ms
SLOT1	POWER_DOWN_SLOT_DURATION_1	POWER_DOWN_SLOT_1_DURATION	0x0	0ms
SLOT2	POWER_DOWN_SLOT_DURATION_1	POWER_DOWN_SLOT_2_DURATION	0x3	10ms
SLOT3	POWER_DOWN_SLOT_DURATION_1	POWER_DOWN_SLOT_3_DURATION	0x0	0ms
SLOT4	POWER_DOWN_SLOT_DURATION_2	POWER_DOWN_SLOT_4_DURATION	0x0	0ms
SLOT5	POWER_DOWN_SLOT_DURATION_2	POWER_DOWN_SLOT_5_DURATION	0x0	0ms
SLOT6	POWER_DOWN_SLOT_DURATION_2	POWER_DOWN_SLOT_6_DURATION	0x0	0ms
SLOT7	POWER_DOWN_SLOT_DURATION_2	POWER_DOWN_SLOT_7_DURATION	0x0	0ms
SLOT8	POWER_DOWN_SLOT_DURATION_3	POWER_DOWN_SLOT_8_DURATION	0x0	0ms
SLOT9	POWER_DOWN_SLOT_DURATION_3	POWER_DOWN_SLOT_9_DURATION	0x0	0ms
SLOT10	POWER_DOWN_SLOT_DURATION_3	POWER_DOWN_SLOT_10_DURATION	0x0	0ms
SLOT11	POWER_DOWN_SLOT_DURATION_3	POWER_DOWN_SLOT_11_DURATION	0x0	0ms
SLOT12	POWER_DOWN_SLOT_DURATION_4	POWER_DOWN_SLOT_12_DURATION	0x0	0ms
SLOT13	POWER_DOWN_SLOT_DURATION_4	POWER_DOWN_SLOT_13_DURATION	0x0	0ms
SLOT14	POWER_DOWN_SLOT_DURATION_4	POWER_DOWN_SLOT_14_DURATION	0x0	0ms
SLOT15	POWER_DOWN_SLOT_DURATION_4	POWER_DOWN_SLOT_15_DURATION	0x0	0ms

2.4.3 TPS6521903 Sequence and Power Block Diagram

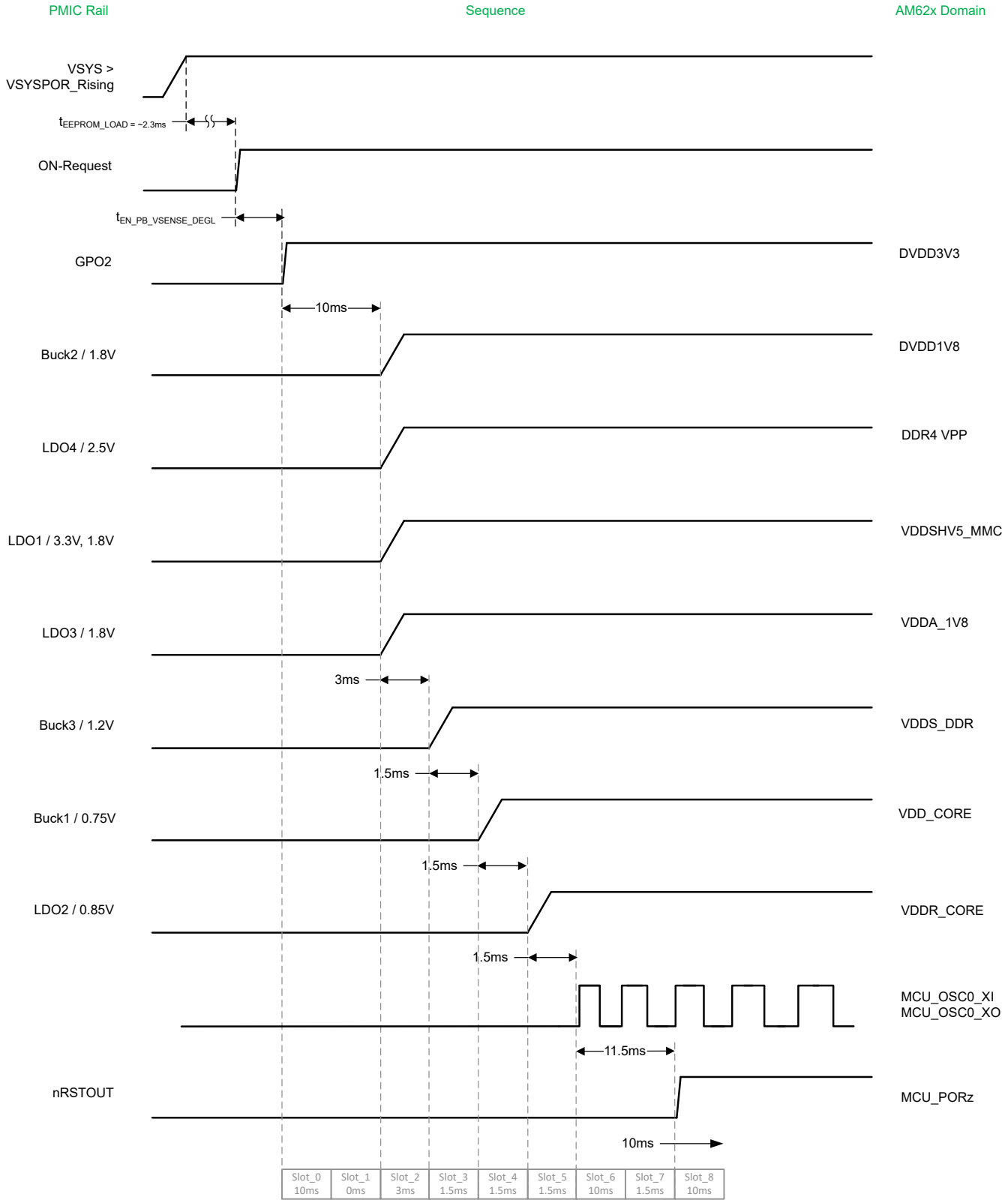

Figure 2-1. TPS6521903 Power-Up Sequence

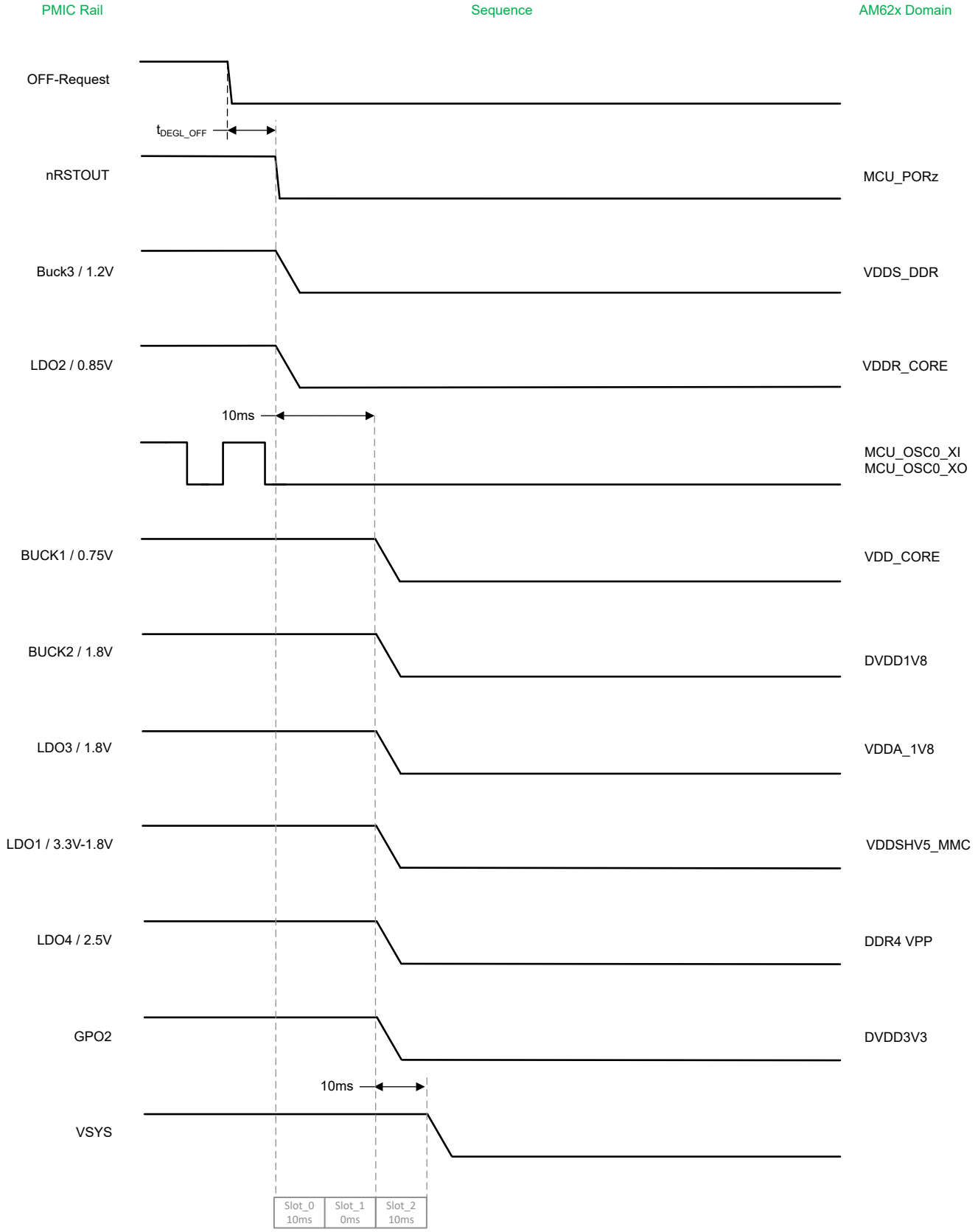

Figure 2-2. TPS6521903 Power-Down Sequence

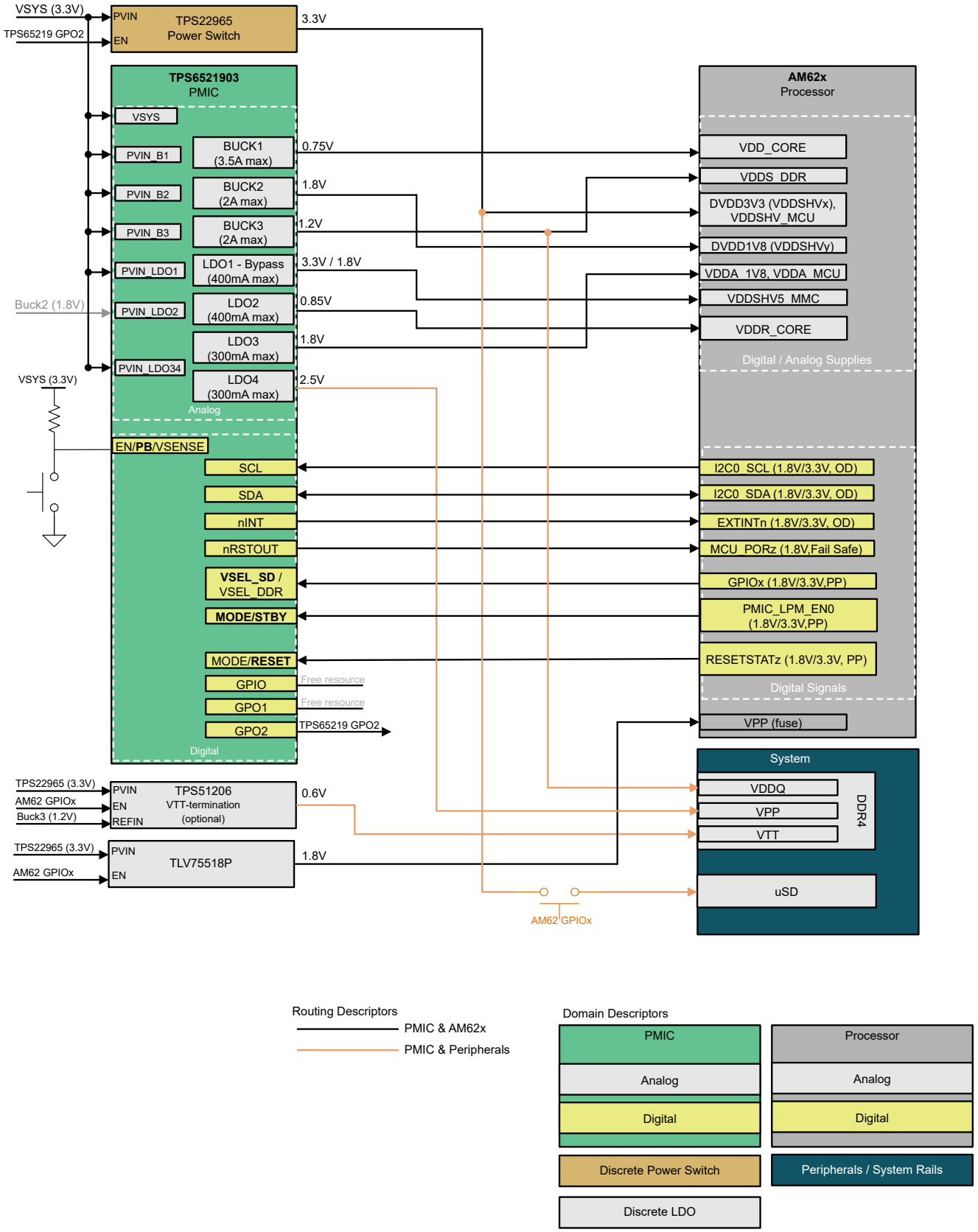

Figure 2-3. TPS6521903 Example Power Block Diagram

2.5 EN / PB / VSENSE Settings

The EN/PB/VSENSE pin is used to enable or disable the PMIC. This pin can be configured in one of three ways: EN, PB or VSENSE. The table below shows the default configuration on for this TRM which is linked to a specific part number. Please note, if the FSD (First supply detection) feature is enabled, the device goes from "No Power" to "Active" state, executing the power-up sequence as soon as the voltage on VSYS is above the POR threshold. In this scenario, the EN/PB/VSENSE pin is ignored ONLY during the first power-up.

Table 2-10. EN / PB / VSENSE Settings

Register Name	Field Name	Value	Description
MFP_2_CONFIG	EN_PB_VSENSE_CONFIG	0x01	Push Button Configuration
MFP_2_CONFIG	EN_PB_VSENSE_DEGL	0x1	long (typ: 50ms if configured as EN or VSENSE)
MFP_2_CONFIG	PU_ON_FSD	0x1	First Supply Detection (FSD) Enabled.

Note

When EN/PB/VSENSE is configured as Enable, the deglitch time selected on "EN_PB_VSENSE_DEGL" is for the rising edge. Falling edge deglitch is not configurable. See data sheet for more details.

2.6 Multi-Function Pin Settings

The TPS65219 PMIC has three multi-function pins that can be configured to set the voltage on a specific power rail or to change the frequency mode or to trigger a warm or cold reset. This section describes how each of the multi-function pins were configured.

Table 2-11. Multi-Function Pin Settings

Pin Name	Setting	Register Name	Field Name	Value	Description
VSEL_SD / VSEL_DDR	Function selection	MFP_1_CONFIG	VSEL_DDR_SD	0x1	VSEL pin configured as SD to set the voltage on the VSEL_RAIL
	Rail	MFP_1_CONFIG	VSEL_RAIL	0x0	LDO1
	pin polarity (only applicable if VSEL_DDR_SD=0x1)	MFP_1_CONFIG	VSEL_SD_POLARITY	0x0	LOW: 1.8V / HIGH: LDOx_VOUT register setting
MODE / STBY	function selection	MFP_2_CONFIG	MODE_STBY_CONFIG	0x2	MODE and STBY
	pin polarity	MFP_1_CONFIG	MODE_STBY_POLARITY	0x0	[if configured as MODE] LOW: auto-PFM / HIGH: forced PWM. [if configured as a STBY] LOW: STBY state / HIGH: ACTIVE state.
MODE / RESET	function selection	MFP_2_CONFIG	MODE_RESET_CONFIG	0x1	RESET
	reset selection	MFP_2_CONFIG	WARM_COLD_RESET_CONFIG	0x1	WARM RESET
	pin polarity	MFP_1_CONFIG	MODE_RESET_POLARITY	0x0	[if configured as mode] LOW: auto-PFM / HIGH: forced PWM. [if configured as RESET] LOW: reset / HIGH: normal operation.

Note

- If LDO1 or LDO2 is configured as bypass and the VSEL pin is not configured as SD (**VSEL_DDR_SD=0x0**), the voltage change on the selected VSEL_RAIL can be changed by I2C (register field: VSEL_SD_I2C_CTRL)

Table 2-12. Default register setting for VSEL_SD_I2C_CTRL

Register Name	Field Name	Value	Description
MFP_1_CONFIG	VSEL_SD_I2C_CTRL	0x1	0x0 = 1.8V 0x1 = LDOx_VOUT register setting

- If Bucks are configured for quasi-fixed frequency (**BUCK_FF_ENABLE=0x0**), and none of the multi-function pins are configured as MODE, switching between auto-PFM and forced-PWM can be changed by I2C (register field: MODE_I2C_CTRL).

Table 2-13. Default register setting for MODE_I2C_CTRL

Register Name	Field Name	Value	Description
MFP_1_CONFIG	MODE_I2C_CTRL	0x0	0x0 = Auto PFM 0x1 = Forced PWM

2.7 Over-Current Deglitch

This section describes the default settings for the over current deglitch. When any of these registers are set (value = 1b), it enabled the long-deglitch option for the corresponding rail.

Table 2-14. Over Current Deglitch

Register Name	Field Name	Value	Description
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_BUCK1	0x0	Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_BUCK2	0x0	Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_BUCK3	0x0	Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO1	0x0	Deglitch duration for OverCurrent signals of LDO1 is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO2	0x0	Deglitch duration for OverCurrent signals of LDO2 is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO3	0x0	Deglitch duration for OverCurrent signals of LDO3 is ~20us
OC_DEGL_CONFIG	EN_LONG_DEGL_FOR_OC_LDO4	0x0	Deglitch duration for OverCurrent signals of LDO4 is ~20us

2.8 Mask Settings

This section describes the settings that are masked by default and the effect they have on the device state as well as the nINT pin.

Table 2-15. Mask Settings

	Register Name	Field Name	Value	Description
Mask effects on device state and nINT pin	MASK_CONFIG	MASK_EFFECT	0x03	no state change, nINT reaction, bit set for Faults
UV Mask	INT_MASK_UV	BUCK1_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	BUCK2_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	BUCK3_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO1_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO2_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO3_UV_MASK	0x0	un-masked (Faults reported)
	INT_MASK_UV	LDO4_UV_MASK	0x0	un-masked (Faults reported)
Power-up retries/ attempts	INT_MASK_UV	MASK_RETRY_COUNT	0x0	Device does retry up to 2 times, then stay off
Die Temperature	MASK_CONFIG	SENSOR_0_WARM_MASK	0x0	un-masked (Faults reported)
	MASK_CONFIG	SENSOR_1_WARM_MASK	0x0	un-masked (Faults reported)
	MASK_CONFIG	SENSOR_2_WARM_MASK	0x0	un-masked (Faults reported)
	MASK_CONFIG	SENSOR_3_WARM_MASK	0x0	un-masked (Faults reported)
Masking bit to control whether nINT pin is sensitive to PushButton (PB)	MASK_CONFIG	MASK_INT_FOR_PB	0x1	masked (nINT not sensitive to any PB events)
Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage)	MASK_CONFIG	MASK_INT_FOR_RV	0x0	un-masked (nINT pulled low for any RV events during transition to ACTIVE state or during enabling of rails)

2.9 Discharge Check

Active discharge is enabled by default and not NVM based. Thus, if desired, it need to be disabled after each VSYS-power-cycle. During RESET or OFF-request, the discharge configuration is not reset, as long as VSYS is present. However, in INITIALIZE state and prior to the power-up-sequence, all rails are discharged, regardless of the setting. In case active discharge on a rail is disabled, it does not gate the disable of the subsequent rail, but the sequence is purely timing based. In case of residual voltage, the RV-bit is be set regardless.

Table 2-16. Discharge Check

Register Name	Field Name	Value	Description
GENERAL_CONFIG	BYPASS_RAILS_DISCHARGED_CHECK	0x0	Discharged checks enforced

2.10 Multi PMIC Config

The TPS65219 allows to synchronize multiple devices, in case more rails are required to be supplied. The GPIO (pin#16) is an input/output digital pin, however, the input-functionality is only used in multi-PMIC configuration. The I/O-configuration of the GPIO-pin is done by the MULTI_DEVICE_ENABLE bit in MFP_1_CONFIG register. The table below shows the default multi-device register setting. For more information about the TPS65219 multi-PMIC operation, please refer to the device data sheet available on ti.com.

Table 2-17. Multi-PMIC Configuration

Register Name	Field Name	Value	Description
MFP_1_CONFIG	MULTI_DEVICE_ENABLE	0x0	Single-device configuration, GPIO pin configured as GPO

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 28, 2023 to March 31, 2025 (from Revision * (February 2023) to Revision A (March 2025)) Page

- Updated TPS6521903 Example Power Block Diagram..... 7

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