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Introduction

The *Analog Applications Journal* (AAJ) is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they relate to the following applications:

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Understanding frequency variation in the DCS-Control™ topology

By Chris Glaser
Applications Engineer

Introduction

A common requirement in the automotive market is to avoid interfering with the AM radio band or other sensitive electronics, such as sensors. One example for power supplies is setting their switching frequency above ~1.8 MHz in order to keep all noise at a higher frequency than the highest AM radio signals.

If the frequency is set below the lowest radio signals, then higher frequency harmonics would be in band and possibly interfere. Most modern power supplies do not use an actual oscillator to set their switching frequency, as in traditional voltage- or current-mode control. Instead, either the on-time or off-time is controlled, which then provides a relatively constant operating frequency.

DCS-Control™ topology is an example of an on-time based topology which efficiently provides the low-noise and fast-transient response needed in many automotive applications. While its switching frequency does vary, this variation is understood, controlled, and usually sufficient for automotive and other frequency-sensitive applications.

Application example

Figure 1 shows the basic block diagram of the DCS-Control topology used in a typical automotive infotainment device.[1, 2]

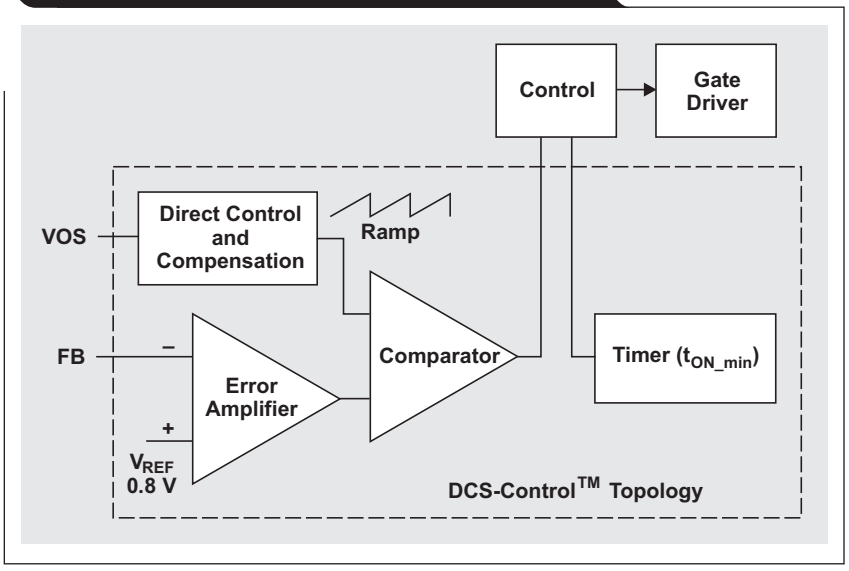
As explained in Reference 1, the timer (t_{ON_MIN}) is responsible for providing a controlled switching frequency by adjusting the on-time based on V_{IN} and V_{OUT} through Equation 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400\ \text{ns} \quad (1)$$

The 400-ns value sets the ideal switching frequency to 2.5 MHz when the DCS-Control device is operating with the on-time set by the timer. However, due to circuit losses, propagation delays, and in some specific application conditions, operation does not always follow the on-time set by the timer. As a result, the frequency varies. The reasons for this variation are grouped together based on the duty cycle, ideally V_{OUT}/V_{IN}, at which the device operates.

Measured data explains the principles behind the DCS-Control topology's frequency variation. To better explain the concepts, the TPS62130 (catalog version) was chosen and it offers two switching frequencies: 2.5 MHz and 1.25 MHz. The 2.5-MHz data exactly matches the TPS62130A-Q1 data because both converters offer the 2.5-MHz setting. All data was taken on the evaluation module with a 2.2-µH inductor and two 22-µF output capacitors (to overcome the DC bias effect).[3]

Figure 1. Block diagram of the DCS-Control™ topology in the TPS62130A-Q1 converter



Moderate duty cycles

In the typical application of converting the 12-V car battery to 5 V for universal serial bus (USB) ports, the required duty cycle is not extremely high or low. Frequency variation in this case is very low because the on- and off-times are not at their extremes. Figure 2 shows the measured switching frequency, on-time, and off-time with a 5-V output voltage, two frequency settings, and two different load currents. A moderate duty cycle refers to those input voltages above 9 V for the 2.5-MHz setting and above 7 V for the 1.25-MHz setting.

Figure 2b shows the reason behind the low levels of frequency variation. The on-time matches very well to the ideal on-time set by the timer and to Equation 1 for both loads and frequency settings. The reasons for the small frequency variation with moderate duty cycles are: overcoming losses and propagation delays.

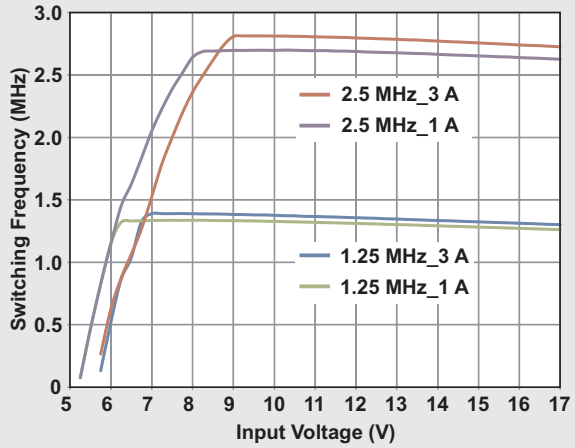
In Figure 2a, the frequency increases with heavier loads due to losses. Higher loads require slightly higher duty cycles to overcome resistive losses in the circuit. Since the on-times are the same for both the 1-A load and 3-A load, the off-time is decreased to achieve the higher duty cycle (Figure 2c). The same on-time and a shorter off-time results in a shorter period and higher frequency.

Also, the frequency decreases slightly with increasing input voltage. Because the on-time decreases with increasing input voltage, fixed propagation delays in the device have a more significant effect on the achieved on-time for smaller on-time values. The timer sets the on-time to achieve a certain frequency, but its output signal goes through the control and gate driver (shown in Figure 1) before reaching the power transistors. This path takes some finite amount of time. For example, if a 200-ns on-time is desired and the propagation delay is 20 ns, the actual on-time is 220 ns, which is 10% higher than desired. But, if the input voltage increases and the desired on-time reduces to 100 ns, the same 20-ns delay produces a 20% increase in the actual on-time. This effect is further pronounced for low duty cycles.

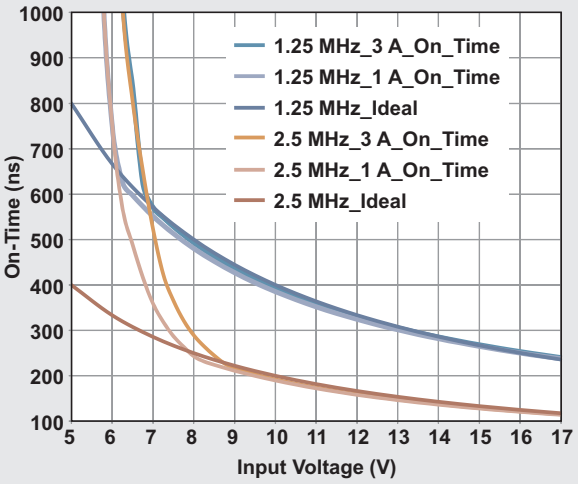
High duty cycles

While a car battery nominally operates at ~12 V, transients from high-current loads, such as starting the engine, can reduce the battery voltage. To the power supply this appears as a line transient, which means more advanced regulation is required in some applications. As long as the input voltage does not decrease below the level of the output voltage, the DCS-Control topology maintains output regulation during such line and load transients.

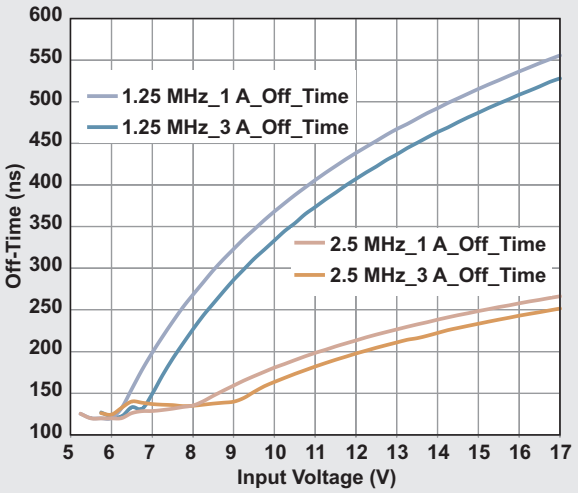
Figure 2. TPS62130 with a 5-V output



(a) Switching frequency



(b) On-time



(c) Off-time

Figure 3 shows measured data for a 3.3-V output. When the input voltage of the converter drops, the duty cycle increases. At high duty cycles, the switching frequency decreases due to losses and a minimum off-time. High duty cycles refers to the left-most portion of Figures 2a and 3a where the switching frequency decreases from its nominal value towards zero.

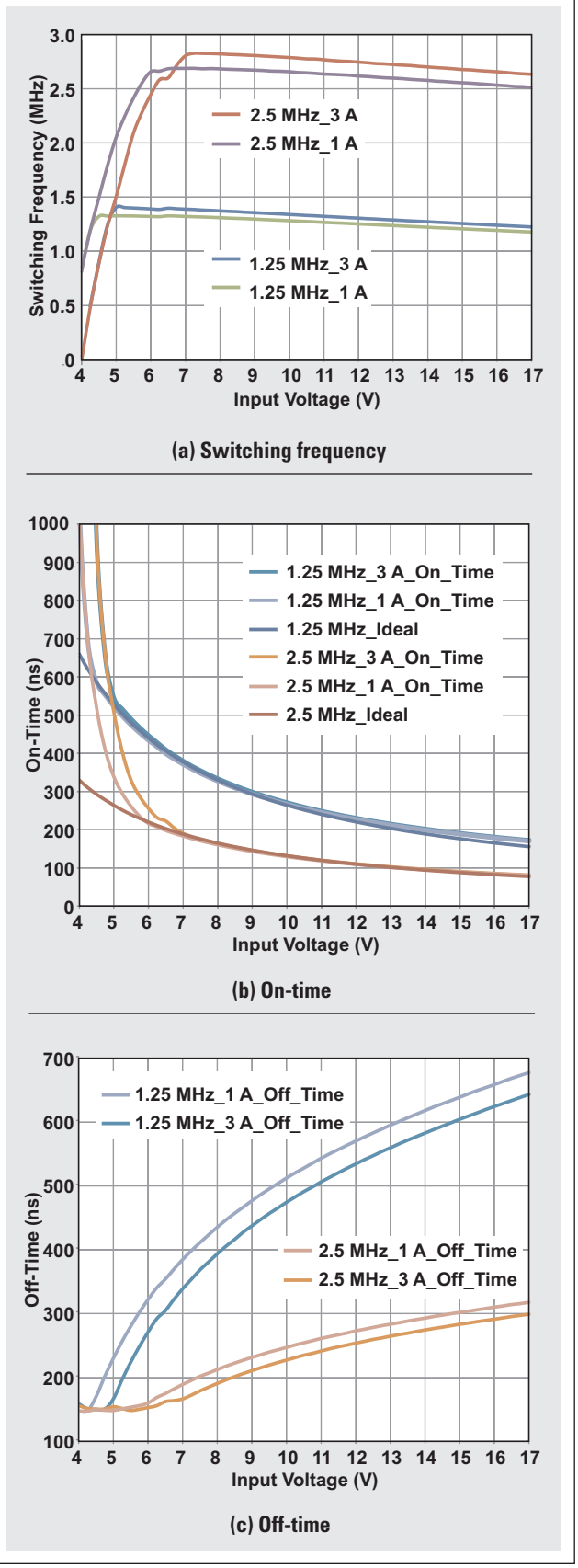
High duty cycles demonstrate a minimum off-time in the topology. Since high duty cycles occur at a lower input voltage and higher output voltage, the energy stored in the inductor during the on-time is lower. This outcome is because there is much less voltage across the inductor. To maximize efficiency, a minimum off-time is included to ensure that sufficient energy is delivered to the output. This is especially helpful in power-save mode, in which a certain amount of energy is delivered so the output stays higher for a longer time. This results in a gap between switching pulses and higher efficiency. From Figure 3c, once the minimum off-time is reached (around a 6-V input voltage for the 2.5-MHz setting), the on-time begins to rise from ideal in order to achieve the required increase in duty cycle that corresponds to the lower input voltage. Figure 2c and Figure 3c show the 120-ns approximate value of the minimum off-time.

Furthermore, the minimum off-time is quickly reached at high duty cycles because the input voltage value is lower as well. At input voltages below 6 V, the resistance of the high-side MOSFET ($R_{DS(on)}$) inside the DCS-Control device increases, thus creating higher losses and a greater required extension of the duty cycle. For example, 3-A loads show longer on-times than 1-A loads at lower input voltages.

Low duty cycles

Low duty cycles occur with lower output voltages, such as 1 V and 1.8 V. The relatively high 12-V input voltage requires duty cycles of sometimes less than 10%. With respect to the desired 400-ns period, this requires on-times near and even below 40 ns. Such small on-times are challenging for any converter to achieve, or are actually impossible due to absolute minimum on-times. The TPS62130 data sheet notes a typical 80-ns absolute minimum on-time that occurs in these cases. This is the primary source of frequency variation at low duty cycles. Fixed propagation delays added to small on-times are another source of variation, as explained before. Figure 4 shows measured data for a 1.8-V output voltage.

Figure 3. TPS62130 with a 3.3-V output



The 2.5-MHz curves in Figure 4b clearly show a minimum on-time in the 80-ns range. This sets an upper boundary on the achievable switching frequency. The 1.25-MHz curves show good frequency variation similar to Figures 2a and 3a. Due to smaller on-times with this 1.8-V output, fixed propagation delays cause a sharper downward frequency shift versus higher output voltages, which result in a lower frequency.

Additionally, the bumpiness seen in the 2.5-MHz curves (Figure 4a) shows a third impact to the on-time: the comparator. During a transient, the comparator extends the on-time past the output of the timer to deliver more energy to the output to make the output voltage recover faster. This is a key aspect of a hysteretic converter and explains the fast transient response of the DCS-Control topology.

While the 80-ns minimum on-time and the output of the timer do not change much over the input voltage range, the output signal does change due to the changing ripple on the inductor current. There is increased ripple with higher input voltages. Having more ripple across the equivalent series resistance (ESR) and equivalent series inductance (ESL) in the output capacitors creates more signal for the comparator on which to react, making the system faster. Between 12 and 13 V, there is enough signal and the comparator no longer controls the on-time. The minimum on-timer controls it. Thus, higher frequency is achieved above this input voltage.

One solution to the lower frequency is a two-stage conversion of the 12 V to the load. A two-stage conversion (via 5 V, for example) to very-low output voltages achieves a higher frequency in both stages because of the more moderate on-times of each stage.

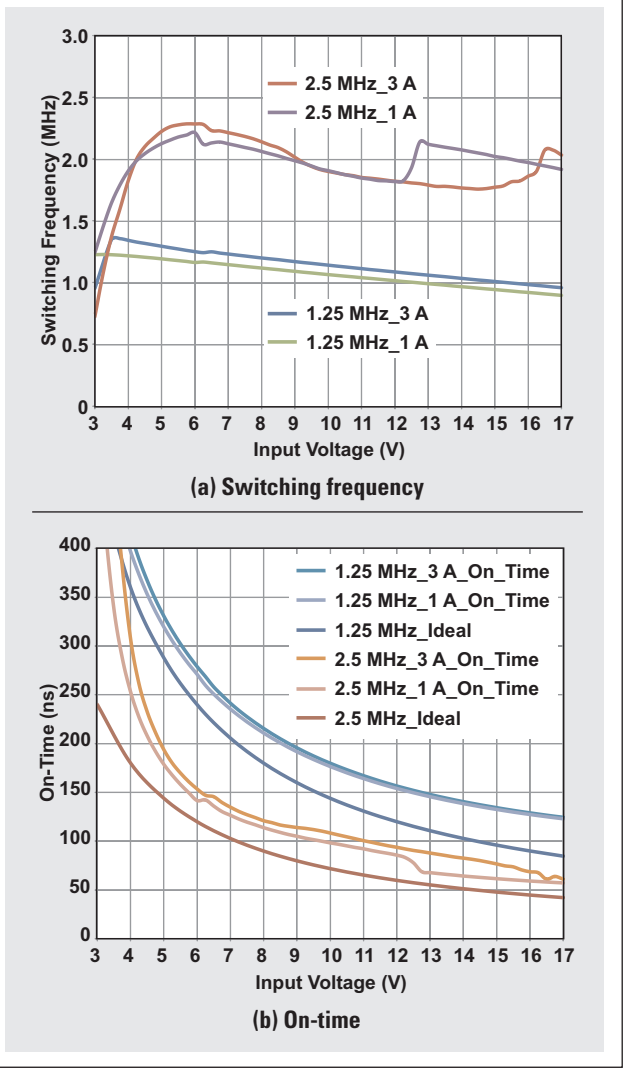
Finally, the lower switching frequency that occurs with lower output voltages will increase the inductor current ripple, but this ripple is already lowered because of the low output voltage (Equation 2). Lower output voltages have less current ripple to begin with. When following the datasheet recommendations for inductance and switching frequency, this lower switching frequency does not limit the output current below the 3-A device rating.

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{SW}} \right) \quad (2)$$

Conclusion

The switching frequency of the DCS-Control topology and other non-oscillator-based control topologies vary with changes in the application conditions. Depending on the duty cycle, the on-time and the frequency are affected by losses, the minimum off-time, the absolute minimum on-time, propagation delays, or the comparator. This behavior is understood and expected, and output voltage regulation is maintained. The lower operating frequency provides higher efficiency with no reduction in output current capability. High-frequency operation is maintained for the common applications of USB ports and system rails with higher voltages.

Figure 4. TPS62130 with a 1.8-V output



References

1. Chris Glaser, "High-efficiency, low-ripple DCS-Control offers seamless pulse-width modulation (PWM)/power-save transitions," *TI Analog Applications Journal*, 3Q 2013 (SLYT531)
2. Datasheet, "TPS6213xA-Q1 3V to 17-V 3A Step-Down Converter with DCS-Control™," Texas Instruments, May 2014
3. TPS62130EVM-505, "Evaluation Module for TPS62130 a 3-A, synchronous, step-down converter in a 3x3-mm, 16-pin QFN," Texas Instruments

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V_{CM} vs. V_{OUT} plots for instrumentation amplifiers with two op amps

By Pete Semig
Analog Applications Engineer, Precision Amplifiers

Background

The most common issue found in the TI E2E™ Community for instrumentation amplifiers involves interpreting the datasheet plot for common-mode voltage versus output voltage (V_{CM} vs. V_{OUT}). Misinterpretation or misunderstanding this plot results in forum posts that describe distorted output waveforms, incorrect device gain, or 'stuck' outputs. Verifying that the device is operating within the limits of the V_{CM} vs. V_{OUT} plot is always the first thing I check when responding to an application issue.

This article introduces the V_{CM} vs. V_{OUT} plot for an instrumentation amplifier with two operational amplifiers (op amps) and delivers a thorough treatment of this amplifier topology. Additionally, the internal node equations are derived and used to plot each internal amplifier's input common-mode and output-swing limits as a function of the instrumentation amplifier's common-mode voltage. Finally, a software tool that simulates the V_{CM} vs. V_{OUT} plot is introduced.

The V_{CM} vs. V_{OUT} plot

The input common-mode and output-swing limitations of all internal amplifiers of an instrumentation amplifier are represented in the V_{CM} vs. V_{OUT} plot.

A typical V_{CM} vs. V_{OUT} plot for a two-op-amp instrumentation amplifier is shown in Figure 1. The interior of the plot defines the linear operating region of the instrumentation amplifier because each line in the plot corresponds to either an input or output limitation of one of the two internal amplifiers. The V_{CM} vs. V_{OUT} plot is specified for a particular supply voltage, reference voltage, and gain as shown in Figure 1.

Operating outside the boundaries of a V_{CM} vs. V_{OUT} plot causes the device to operate in a non-linear mode as shown in Figure 2.

A three-part series article and blog post discuss the V_{CM} vs. V_{OUT} plot for the ubiquitous three-op-amp instrumentation amplifier.[1, 2] Two-op-amp instrumentation amplifiers are popular because of their low-cost and relatively large V_{CM} vs. V_{OUT} plots.

Figure 1. V_{CM} vs. V_{OUT} plot for two-op-amp instrumentation amplifier

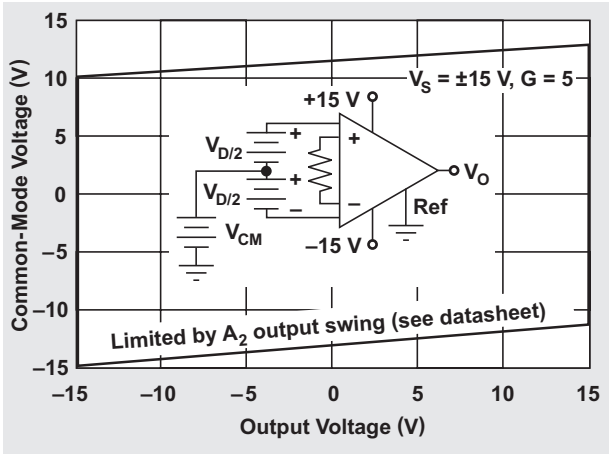
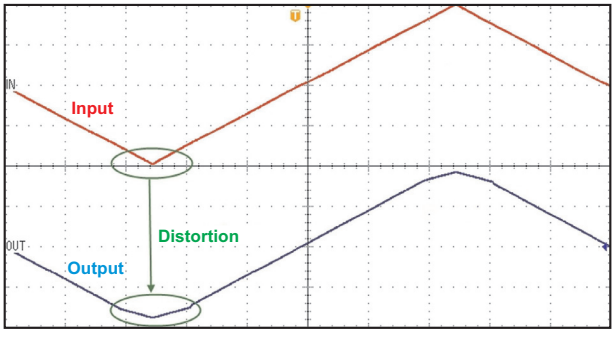


Figure 2. Instrumentation amplifier output distortion due to V_{CM} vs. V_{OUT} violation[1]



Analysis of a two-op-amp instrumentation amplifier

Figure 3 depicts a typical two-op-amp instrumentation amplifier connected to an input signal. This topology has high input impedance and requires only one resistor, R_G, to set the gain, which is the same as the three-op-amp topology.

Figure 3 also depicts the definition of common-mode (V_{CM}) and differential-mode (V_D) voltages. A differential amplifier (for example, op amp, difference amplifier, instrumentation amplifier) ideally rejects the common-mode voltage, V_{CM}.

However, the signal-path imbalance from V_{+IN} and $V_{–IN}$ to the output degrades the device's common-mode rejection ratio (CMRR), especially over frequency (Figure 4). This degradation in CMRR is one of the primary reasons why two-op-amp instrumentation amplifiers typically cost less than their three-op-amp counterparts.

The transfer function for the circuit in Figure 3 is given by Equation 1. Notice that the common-mode voltage does not appear in the equation because ideally it is rejected by the instrumentation amplifier.

$$V_O = (V_{+IN} - V_{-IN}) \times G + V_{REF} = V_D \times G + V_{REF} \quad (1)$$

Deriving the transfer function of this topology aids in understanding the V_{CM} vs. V_{OUT} plot.

Figure 5 depicts a more traditional drawing of the schematic in Figure 3. In order to determine the contribution of the reference voltage at the output, $V_{O(VREF)}$, apply superposition by shorting the input sources to ground.

Amplifier A_2 applies an inverting gain to V_{REF} based on the ratio of R_{FA2} and R_R. Similarly, A_1 applies an inverting gain to the output voltage of A_2 based on the ratio of R_{FA1} and R_{OA2}. Equation 2 depicts the transfer function for V_{REF}.

$$V_{O\_VREF} = V_{REF}\left(\frac{-R_{FA2}}{R_R}\right)\left(\frac{-R_{FA1}}{R_{OA2}}\right) = V_{REF}\left(\frac{R_{FA1} \times R_{FA2}}{R_R \times R_{OA2}}\right) \quad (2)$$

Figure 3. Topology of a two-op-amp instrumentation amplifier

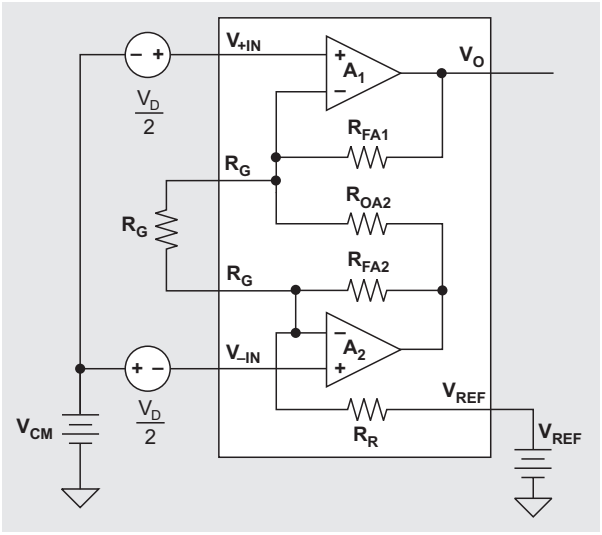


Figure 4. CMRR of two-op-amp vs. three-op-amp topologies

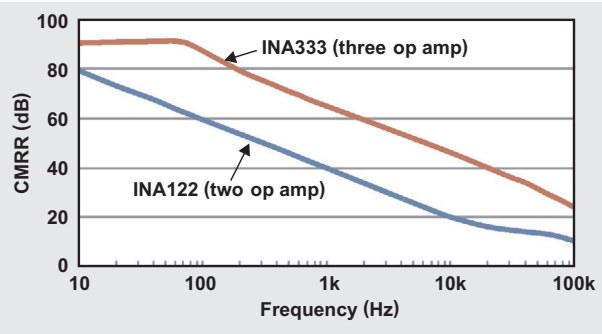
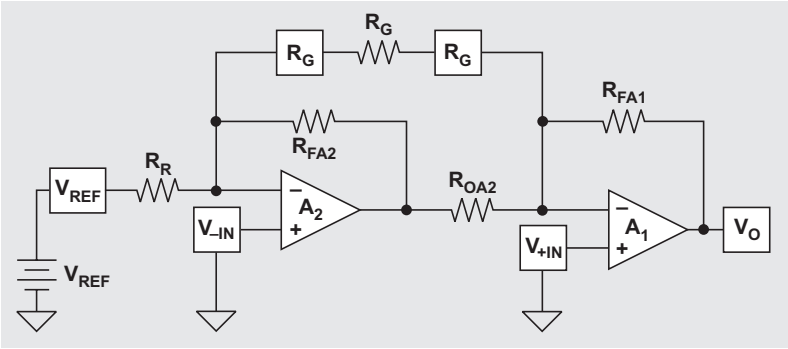


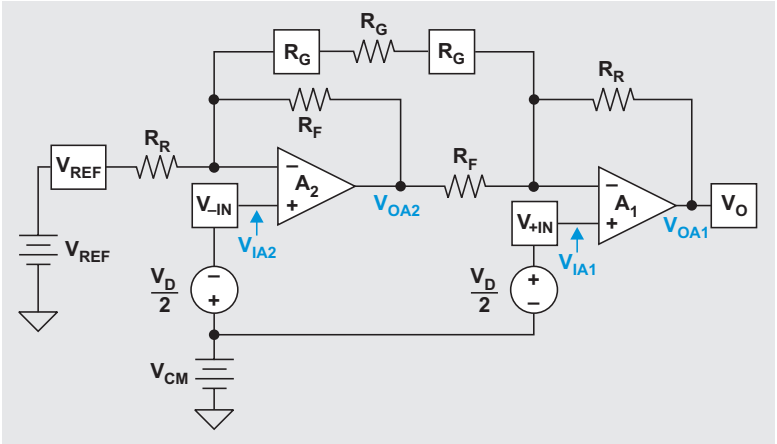
Figure 5. Alternate drawing for Figure 3



The gain applied to the instrumentation amplifier's reference voltage should be 1 V/V. To fulfill this requirement, set $R_{FA1} = R_R$ and $R_{FA2} = R_{OA2} = R_F$. Figure 6 depicts the updated two-op-amp topology that results in unity gain for the reference voltage. Furthermore, the internal nodes are labeled for future analysis.

Despite just two amplifiers and five resistors, the circuit in Figure 6 has six gain terms. This is because each amplifier applies gain to three input signals. While it may be obvious that A_2 applies gain to $V_{–IN}$ and V_{REF}, A_2 also applies gain to V_{+IN} via the virtual short across the inputs of A_1 and R_G. Similarly, A_1 applies gain to V_{OA2}, V_{+IN}, and $V_{–IN}$. Equations 3 through 8 depict the six gain terms associated with a two-op-amp instrumentation amplifier.

Figure 6. Two-op-amp topology with internal nodes labeled



$$G_{A2VR} = \frac{-R_F}{R_R} \quad (3)$$

$$G_{A2V-IN} = 1 + \frac{R_F}{R_G \parallel R_R} \quad (4)$$

$$G_{A2V+IN} = \frac{-R_F}{R_G} \quad (5)$$

$$G_{A1VOA2} = \frac{-R_R}{R_F} \quad (6)$$

$$G_{A1V+IN} = 1 + \frac{R_R}{R_G \parallel R_F} \quad (7)$$

$$G_{A1V-IN} = \frac{-R_R}{R_G} \quad (8)$$

Equations 9 and 10 depict the output voltages of amplifiers A_1 and A_2.

$$V_{OA1} = V_O = V_{+IN}\left(G_{A1V+IN}\right) + V_{-IN}\left(G_{A1V-IN}\right) + V_{OA2}\left(G_{A1VOA2}\right) \quad (9)$$

$$V_{OA2} = V_{+IN}\left(G_{A2V+IN}\right) + V_{-IN}\left(G_{A2V-IN}\right) + V_{REF}\left(G_{A2VR}\right) \quad (10)$$

Substituting Equation 10 for V_{OA2} in Equation 9 and simplifying yields Equation 11.

$$V_O = V_{+IN}\left(G_{A1V+IN} + G_{A2V+IN}G_{A1VOA2}\right) + V_{-IN}\left(G_{A1V-IN} + G_{A2V-IN}G_{A1VOA2}\right) + V_{REF} \quad (11)$$

The relationship between the gain terms in Equation 11 is shown in Equation 12.

$$\begin{aligned} G_{A1V+IN} + G_{A2V+IN}G_{A1VOA2} &= -\left(G_{A1V-IN} + G_{A2V-IN}G_{A1VOA2}\right) \\ &= G_{A1V+IN} - G_{A1V-IN} = 1 + \frac{R_R}{R_F} + \frac{2R_R}{R_G} \end{aligned} \quad (12)$$

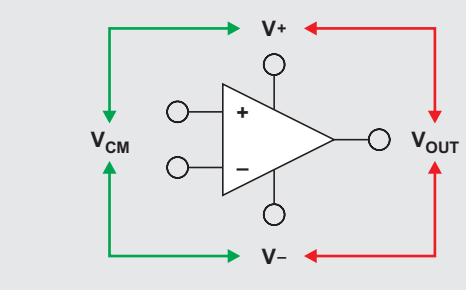
Finally, using Equations 11 and 12, the transfer function for a two-op-amp instrumentation amplifier is shown by Equation 13, which is consistent with Equation 1.

$$\begin{aligned} V_O = V_{OA1} &= \left(V_{+IN} - V_{-IN}\right) \times G + V_{REF} \\ &= V_D \times \left(1 + \frac{R_R}{R_F} + \frac{2R_R}{R_G}\right) + V_{REF} \end{aligned} \quad (13)$$

Op amp limitations

Linear operation of an instrumentation amplifier is contingent upon the linear operation of its primary building block; op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output-swing ranges, respectively. The supply voltages used to power the op amp (V+ and V–) define these ranges (Figure 7).

Figure 7: Op amp input common-mode and output-swing ranges depend on supplies[1]



A real-world example of common-mode and output-swing limits is shown in Figure 8. Notice that the common-mode range and output-swing ranges are not necessarily the same.

Two-op-amp node equations

With a solid understanding of the two-op-amp instrumentation amplifier and op-amp limitations, the next step is to examine the node equations as indicated in Figure 6. The equations for V_{OA2} and V_{OA1} are already given by Equations 10 and 13, respectively. Equations for V_{IA1} and V_{IA2} from Figure 6 are given as:

$$V_{IA1} = V_{+IN} = V_{CM} + \frac{V_D}{2} \quad (14)$$

$$V_{IA2} = V_{-IN} = V_{CM} - \frac{V_D}{2} \quad (15)$$

The V_{CM} vs. V_{OUT} plot can vary based on gain and reference voltage. Therefore, Equations 10 and 13 through 15 must be solved for V_O as a function of the gain terms, V_{CM}, and V_{REF}. One important relationship that allows for this is obtained by solving Equation 13 for V_D, as shown in Equation 16.

$$V_O = V_D \times G + V_{REF} \rightarrow V_D = \frac{V_O - V_{REF}}{G} \quad (16)$$

After making all of the proper substitutions and solving for V_O, Equations 17 through 20 capture the linear operating region of a two-op-amp instrumentation amplifier at its output as a function of the gain terms, V_{CM}, V_{REF}, and the common-mode and output limitations of each amplifier (V_{IA1}, V_{IA2}, V_{OA1}, V_{OA2}).

$$V_{O\_IA1} = 2 \times G \times (V_{IA1} - V_{CM}) + V_{REF} \quad (17)$$

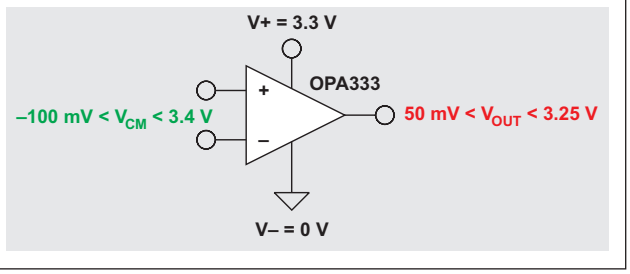
$$V_{O\_IA2} = -2 \times G \times (V_{IA2} - V_{CM}) + V_{REF} \quad (18)$$

$$V_{O\_OA1} = V_{OA1} \quad (19)$$

$$V_{O\_OA2} = 2V_{CM} - V_R + 2G_{A1VOA2}(V_{OA2} - V_{CM}) \quad (20)$$

In order to operate in a linear region, the voltage at V_{IA1} must not violate the input common-mode range of A_1. Similarly, the voltage at node V_{OA1} must not violate the output swing limitation of A_1. The same holds true for V_{IA2} and V_{OA2} for op amp A_2. The values of the internal op amp limitations are not usually explicitly stated in an instrumentation amplifier's data sheet. In lieu of such information, a combination of examining the device's limitations and measuring the linear operating region can be used to determine the values.

Figure 8. Op amp V_{CM} and V_{OUT} ranges for 3.3-V supply[1]



To move the input common-mode range closer to the negative supply voltage, some instrumentation amplifiers (for example, INA122) level-shift the inputs using precision transistor buffers.[1] This is particularly useful when operating with a single supply.

Figure 9 depicts a TINA-TI™ simulation that plots Equations 17 through 20 for both the maximum and minimum common-mode and output-swing limits for the internal amplifiers of the INA122. The linear operating region is the interior of all lines.

Figure 9. V_{CM} vs. V_{OUT} plot

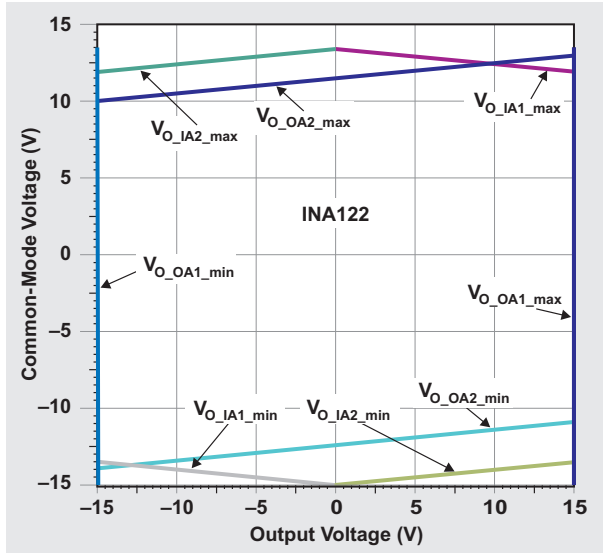
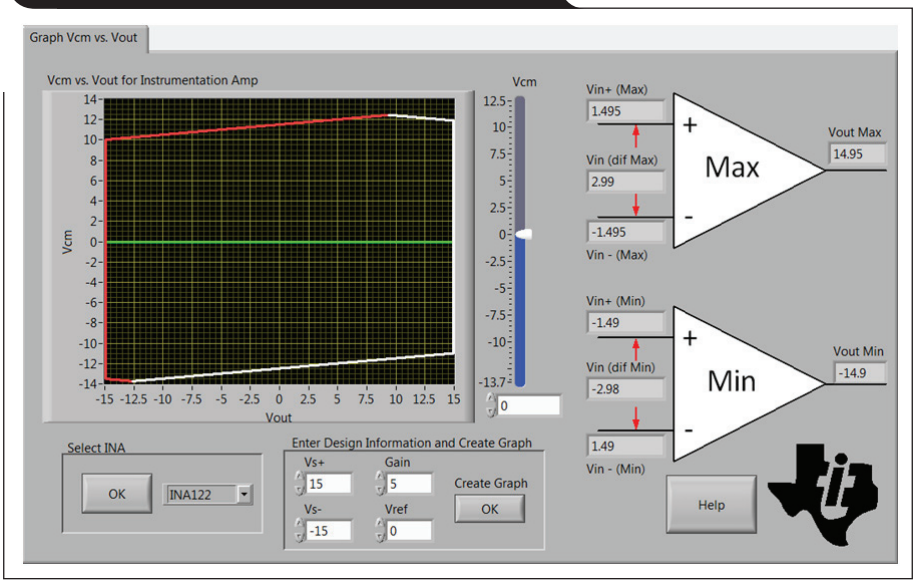


Figure 10. V_{CM} vs. V_{OUT} software tool



A software tool was developed to simplify the creation of V_{CM} vs. V_{OUT} plots for varying gains, reference voltages, and supply voltages. See Related Web sites an the end of this article for download links. Figure 10 depicts the V_{CM} vs. V_{OUT} plot for the INA122 given standard datasheet conditions. Notice that it compares well with Figure 1 and Figure 9. The datasheet plot in Figure 1, however, only depicts the output limitations of A_1 and A_2, whereas the software tool includes the common-mode limitations. Finally, note that the software tool can be downloaded to generate V_{CM} vs. V_{OUT} plots for both two- and three-op-amp instrumentation amplifiers.

Summary

This article addressed the most misunderstood concept of two-op-amp instrumentation amplifiers: the V_{CM} vs. V_{OUT} datasheet plot. A thorough analysis of the two-op-amp topology was delivered along with the derivation of the internal node equations. These equations were used to create the V_{CM} vs. V_{OUT} plots. The output from the downloadable software tool was found to correlate well with the plot in the INA122 datasheet. This tool gives designers a simple method for ensuring linear operation of the instrumentation amplifier in their design.

Acknowledgements

The author would like to thank Art Kay at Texas Instruments for developing the V_{CM} vs. V_{OUT} software tool and Collin Wells for his technical contributions to this article.

References

1. Peter Semig and Collin Wells, “Instrumentation amplifier V_{CM} vs. V_{OUT} plots,” Part 1, Part 2 and Part 3, EDN Network, December 2014
2. Peter Semig, “How Instrumentation Amplifier V_{CM} vs. V_{OUT} plots change with supply and reference voltage,” TI Precision Hub, January 30, 2015.

Related Web sites

Software tool:
V_{CM} vs. V_{OUT} plot generator

Product information:
INA122
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Common-mode transient immunity for isolated gate drivers

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Introduction

Isolated gate drivers are widely used for driving insulated-gate bipolar transistors (IGBTs) and MOSFETs in various applications such as motor drives, solar inverters and automobiles. In addition to turning the IGBTs or MOSFETs on and off, these drivers provide galvanic isolation. The device's switching rate depends on the application and type of the device being used. Switching frequencies of 10 to 20 kHz are common in IGBTs, however, silicon carbide (SiC) and gallium-nitride or GaN-based systems can operate at 50 kHz to 200 kHz. Some advantages for using a higher switching frequency are smaller filter size, fast control and lower distortion. However, these advantages come with an increased power loss during transition. Common-mode transient immunity (CMTI) is an important parameter of a gate driver to consider when operating it at higher switching frequencies. This article gives background on a general pulse-width modulation (PWM) scheme, the transition loss associated with high switching frequency, and isolated gate-driver solutions to reduce transition time.

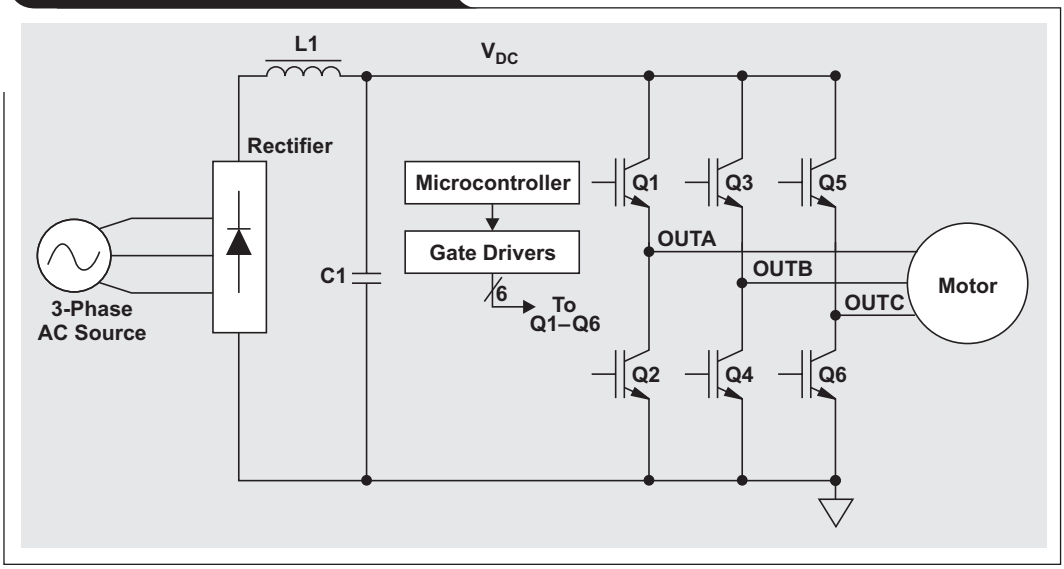
Typical inverter operation

An inverter configuration is used for a DC-to-AC conversion. These voltage-source inverters (VSIs) can be used either for general AC voltage-output generation or motor control. Examples of AC voltage-output applications are solar inverters, uninterruptable power supplies (UPSs), or AC applications powered from a battery in automobiles. The same inverter configuration allows for output-voltage amplitude and frequency control, which is more useful for a motor control. An induction-motor control is a common example of using an inverter for motor control.

Figure 1 contains a high-level diagram of an AC-to-DC and then DC-to-AC conversion. The system has a three-phase input and controllable three-phase AC output. The rectifier block converts the AC to DC, and a filter using L1 and C1 is used to filter out the residual ripple. A key parameter for the rectifier is its power factor. The simplest form of a rectifier uses diodes. Diode-based rectifiers have very poor power factor and are not suitable for high-power applications. Instead, rectifiers using active power factor correction (PFC) are preferred for high-power solutions.[1]

The inverter consists mainly of Q1 through Q6 IGBTs and the gate-driver circuit. Input to the inverter is the DC supply (V_{DC}) produced by the rectifier. The purpose of the inverter is to convert DC to AC voltage. The frequency and amplitude of the inverter output is controlled by how the IGBTs are switched. In applications such as UPSs or solar inverters, a battery supplies power to the inverter. The load can be any general-purpose AC load, or it can connect to the grid. The fundamental structure of the inverter remains the same for many applications.

Figure 1. Motor control diagram



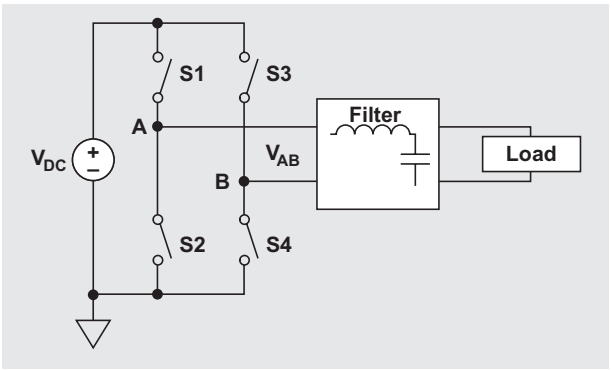
Battery-operated inverters are very common in electric vehicles. A microcontroller is used to produce a PWM waveform to drive the IGBTs and the outputs (OUTA, OUTB and OUTC) switch between 0 V and V_{DC}. An induction motor requires control of voltage and frequency to control its torque and speed. The microcontroller monitors the speed and current in the motor and provides the proper PWM pattern according to user inputs. IGBTs typically require gate drivers with isolated outputs because the output side is switching between 0 V and V_{DC}. The switching frequency of an IGBT-based inverter is typically in the range of 8 to 16 kHz and higher PWM switching frequencies are possible with SiC or GaN IGBTs.[2, 3] In this scenario, gate drivers also need to support faster switching speeds. The inverter can be configured as a single-phase output with only two legs and four switches. Three-phase systems are typically used to get more power.

Pulse-width modulation

PWM or pulse-width modulation is a way to achieve amplitude control by changing the duty cycle.

Figure 2 shows a simple form of a single-phase inverter. Input to the inverter is a DC voltage (V_{DC}) and the voltage across the load is $V_{AB} = V_A - V_B$. The voltage at node A switches between V_{DC} and 0 V via switches S1 and S2. Similarly, the voltage at node B switches between V_{DC} and 0 V via switches S3 and S4. Switches S1 and S2 are complementary, as are switches S3 and S4. The maximum output voltage that can be achieved using this system is V_{DC}. An example of switching waveforms at nodes A and B without filtering is shown in Figure 3. The switching rate

Figure 2. High-level diagram of a single-phase inverter



can range from 10 to 200 kHz, depending on the application and type of switch. In Figure 3a, the duty cycle at node A is more than 50% and in Figure 3b, the duty cycle is less than 50% at node B. This creates a positive voltage across the load as shown in Figure 3c.

In Figure 3d, the duty cycle at node A is less than 50% and more than 50% at node B (Figure 3e),which creates a negative voltage across the load (Figure 3f).

The average voltage, V_{AB}, across the load/filter can be written as:

$$V_{AB} = V_{DC} \times D_A - V_{DC} \times D_B \text{ or } V_{AB} = V_{DC} \times (D_A - D_B) \quad (1)$$

where D_A is the duty cycle at node A, and D_B is duty cycle at node B.

Figure 3. Simplified PWM operation with positive and negative output voltages

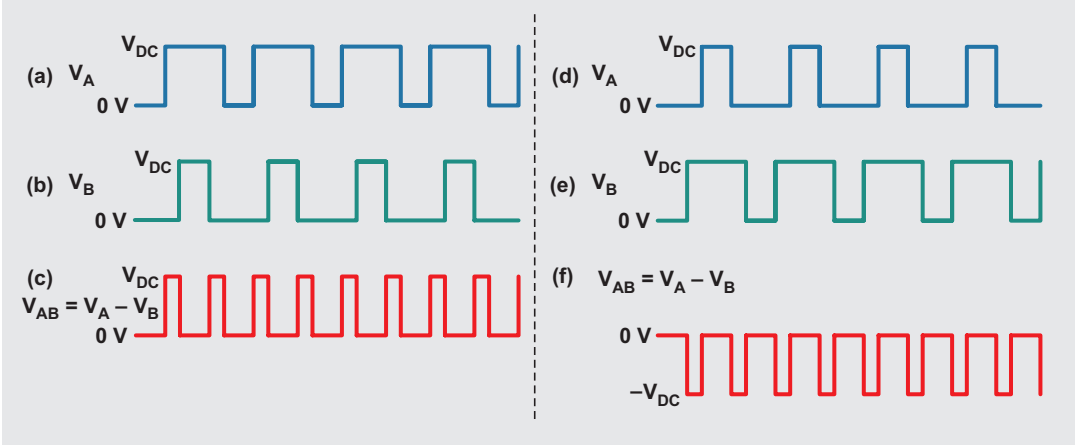
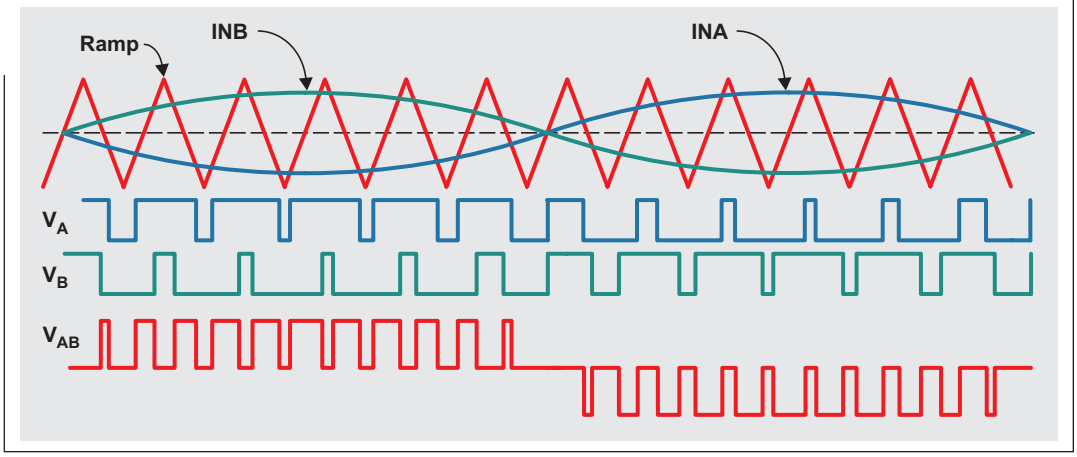


Figure 4. A single-phase PWM output waveform



Controlling the duty cycle, D_A and D_B, allows control of the output voltage, V_{AB}. A sinusoidal single-phase PWM waveform is obtained by comparing a reference sine wave INA and INB with a high-frequency triangular signal as shown in Figure 4.

The fundamental component of the output has an amplitude that is proportional to the differential reference input ($V_{INA} - V_{INB}$), and the frequency is the same as the reference frequency. This allows the voltage and frequency to be controlled by the reference signal. High-frequency tones are at frequencies $2nf_{SW} \pm mf_{IN}$, where f_{SW} is the triangular signal frequency, f_{IN} is the reference input frequency, and the n and m multipliers can be 1, 2, 3, etc. The high-frequency component is filtered by the LC filter, or the motor inductance in the case of motor control.

The ratio between the input signal amplitude and the triangular signal amplitude is called amplitude modulation ratio, or m_A.

$$m_A = \frac{V_{IN}}{V_{RAMP}} \tag{2}$$

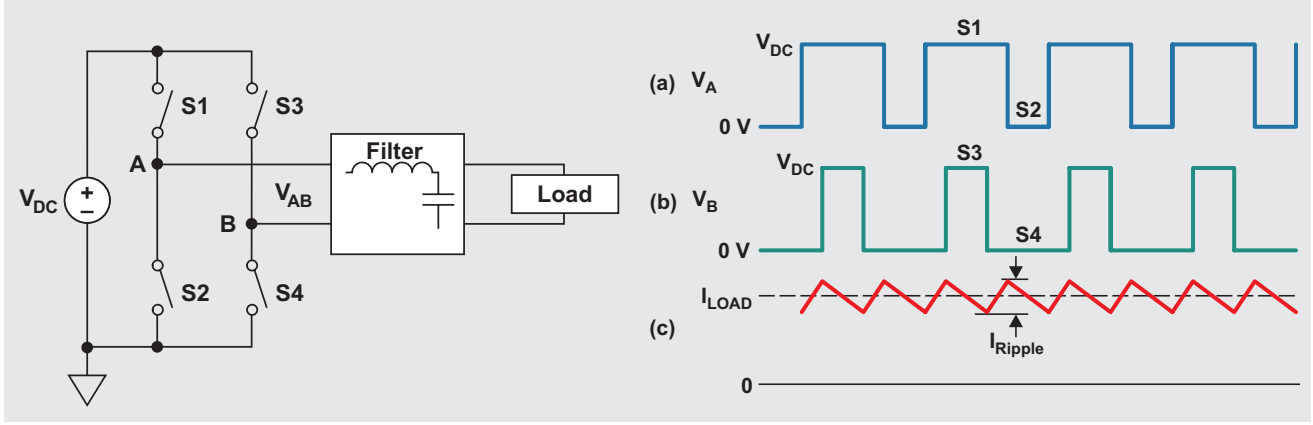
where V_{IN} is the amplitude of the reference input signal and V_{RAMP} is the amplitude of the triangular wave signal. The fundamental output voltage is $m_A \times V_{DC} \times \text{sine}(\omega t)$; where ω is the frequency of the reference input signal. The root mean square (rms) of the fundamental signal can be written as:

$$V_{RMS} = \frac{m_A \times V_{DC}}{\sqrt{2}} \tag{3}$$

Transition loss in inverters

The inverter outputs switch between ground and V_{DC} at the PWM frequency, however, the output current is filtered either by the LC filter or motor inductance. Figure 5 shows waveforms for voltage and current in a PWM switching output . Figure 5c shows a DC current with a very small ripple component. The ripple amplitude is dependent on the filter size. While this example shows a DC output, the same concept can be extended for a sine-wave output. However, the current is a sine wave with a small ripple riding on it.

Figure 5. An inverter's voltage and current waveforms with an LC filter



The instantaneous output power is $V_{AB} \times I_{LOAD}$, where V_{AB} is the average DC output, which is dependent on the duty cycles at nodes A and B. Assuming that there is no phase difference between the voltage and current, the output power for a sinusoidal output is:

$$P_{OUT} = V_{RMS} \times I_{RMS} = \frac{m_A \times V_{DC} \times I_{RMS}}{\sqrt{2}} \quad (4)$$

The transition time from 0 V to V_{DC} and vice versa of the voltage at node A is finite. The switch's ON impedance is very low when completely on, but higher during transition time. This leads to transition-switching losses. This loss occurs twice at every PWM cycle. Current through the switches during transition is same as the load current because it is filtered. Transition loss for a single event is $V_{DC} \times I_{LOAD} \times t_{RF} / 2$.

The total transition loss for a single-phase inverter is

$P_{LOSS} = 2 \times 2 \times f_{SW} \times I_{LOAD} \times V_{DC} \times t_{RF} / 2$
$= 2 \times V_{DC} \times I_{LOAD} \times t_{RF} \times f_{SW}$,

where t_{RF} is the rise/fall time of the voltage. In case of a sinusoidal current output, current through the switches is an average of the load current:

$$|I_{LOAD}| = \frac{2\sqrt{2} \times I_{RMS}}{\pi} \quad (5)$$

and the power loss is:

$$P_{LOSS} = \frac{4\sqrt{2} \times V_{DC} \times I_{RMS} \times t_{RF} \times f_{SW}}{\pi} \quad (6)$$

Ratio of the loss to output power is:

$$\frac{P_{LOSS}}{P_{OUT}} = \frac{8 \times t_{RF} \times f_{SW}}{\pi \times m_A} \quad (7)$$

Equation 6 suggests that loss is proportional to the switching frequency. An inverter with a switching frequency of 16 kHz and 200-ns rise/fall time will have a 1% transition loss, assuming $m_A = 0.8$. To reduce the transition loss, the rise/fall time has to be lower for a higher switching frequency. For example, a SiC-based inverter with a 64-kHz switching frequency needs a rise/fall time of 50 ns to keep a 1% transition loss.

Gate-drivers for Inverter

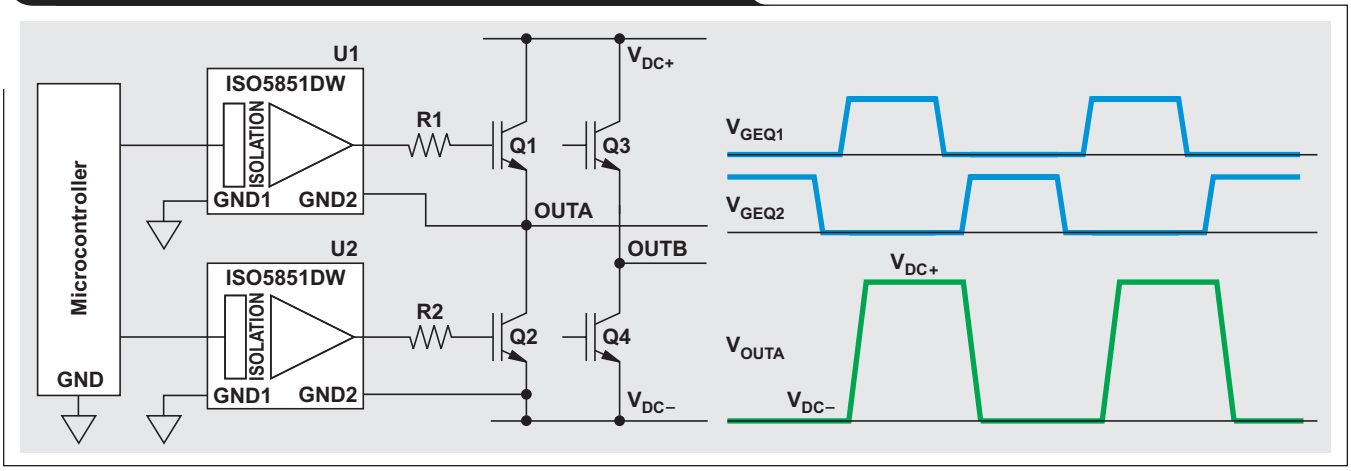
A typical drive of an IGBT-based, voltage-source inverter is shown in Figure 6. This figure shows a single-phase inverter, but it can be extended to a three-phase by adding one more leg of the bridge. The voltage at outputs OUTA or OUTB switches from V_{DC-} to V_{DC+}. The IGBT gate drives are isolated because the output-side ground of the driver is switching along with the inverter output while the input-side ground is fixed and connected to a chassis.

The potential differences between GND1 and GND2 of both gate drivers require the drivers to be isolated. The gate drivers support high-voltage isolation across the two grounds along with voltage transition rate at GND2. The gate drivers are also selected based on their isolation rating and their immunity to the transition on GND2, or common-mode transient immunity (CMTI). For example, if the DC bus is 1500 V and the transition time of OUTA is 100 ns, the immunity required by the gate driver is 15 V/ns. The immunity requirement for the driver increases if the rise/fall time is lower. A voltage-source inverter (VSI) with a higher switching frequency will have a higher CMTI requirement. A 1500-V VSI running at 64 kHz and 50-ns rise/fall time requires at least 30-V/ns CMTI. The CMTI requirement increases if the transition loss is to be lower.

The gate drivers are specified for CMTI in their datasheet. For example, the ISO5851 and ISO5852S both have a minimum CMTI of 100 kV/µs. Higher CMTI for a gate driver ensures there is no false fault or false output toggle because of the transient noise.

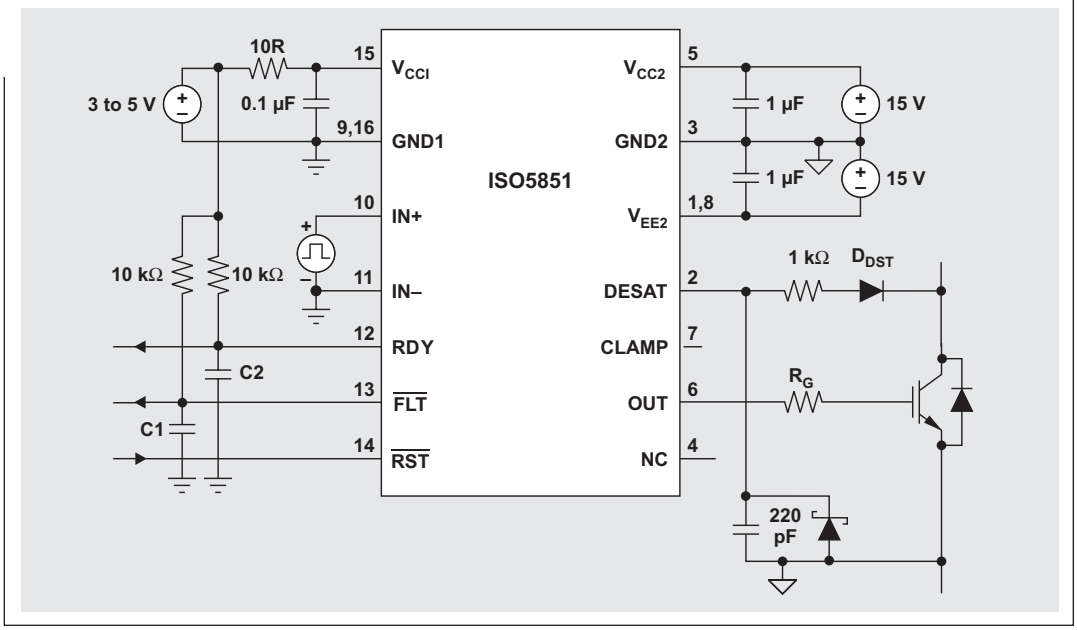
The component placement or board design also matters for a robustness to transient noise. The parasitic capacitance between one side of the driver to the other side of the driver should be minimized. Using a diagram from the

Figure 6: Single-phase inverter with isolated gate drivers



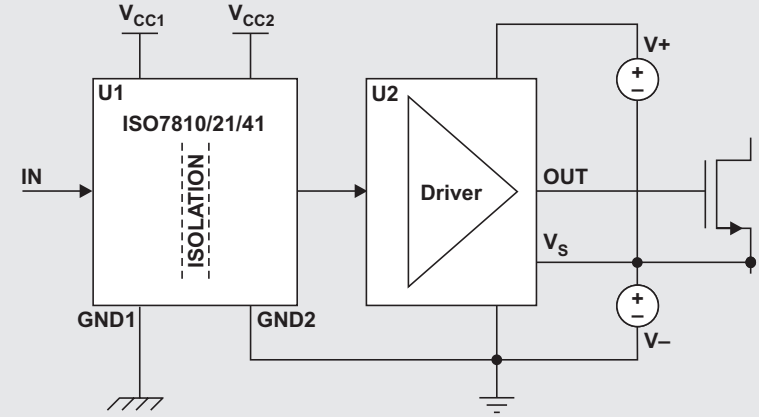
ISO5851 datasheet, Figure 7 shows a typical application diagram. The Ready (RDY) and Fault (FLT) pins are pulled up by 10-kΩ resistors. These resistor values may need to be lower for noise immunity. Transient noise can generate a false fault or low under-voltage lockout (UVLO) signal. This issue can be solved by either reducing the resistor values or increasing the capacitance of C1 and C2.

Figure 7. Typical application where C1 and C2 can be changed to adjust CMTI



Digital isolators such as the ISO7810, ISO7821 or ISO7841 also can be used in conjunction with SiC, GaN or IGBT drivers. Digital isolators provide reinforced isolation and a CMTI at a minimum of 100 kV/µs. Figure 8 shows an isolated driver solution using a digital isolator. The digital isolator can range from a single channel up to four channels, depending on the application. The digital isolator has an added benefit of low propagation delay, low skew and low jitter, which are useful in a high-frequency design.

Figure 8. Gate-driver solution using digital isolators



Conclusion

Voltage-source inverters (VSIs) with PWM topology are a good choice for a motor control because the output amplitude and frequency control have a lot of flexibility. A higher switching frequency of PWM VSIs allows for a smaller filter size. The rise/fall times should be lower with high switching frequencies to keep the transition loss lower. A gate driver with good CMTI supports faster switching speeds. Gate-driver solutions from Texas Instruments can support a CMTI minimum of 100-kV/µs.

References

1. A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," IEEE Trans. Power Electronics, 1991 pp. 83-92
2. Dr Scott Allen, "Silicon Carbide MOSFETs for High Powered Modules," CREE Inc., March 19, 2013
3. Jang-Kwon Lim, D. Peftitsis, J. Rabkowski, M. Bakowski, H.-P. Nee, "Analysis and Experimental Verification of the Influence of Fabrication Process Tolerances and Circuit Parasitics on Transient Current Sharing of Parallel-Connected SiC JFETs," Power Electronics, IEEE Transactions on, Volume: 29, Issue: 5, May 2014, pp. 2180 – 2191

Related Web sites

Product information:
ISO5851, ISO5852S, ISO7810, ISO7821, ISO7841

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Pushing the envelope with high-performance, digital-isolation technology

By Anant Kamath
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Introduction

Isolation is a means of preventing DC and uncontrolled AC currents between two parts of a system, while allowing signal and power transfer between those two parts. Electronic devices and integrated circuits (ICs) used for isolation are called isolators. Isolation is required in modern electrical systems for a variety of reasons. Some examples include protecting human operators and preventing damage to expensive processors in high-voltage systems, breaking the ground loop in communication networks, and communicating to high-side devices in motor-drive or power-converter systems (Figure 1). Examples of applications that need isolation include industrial automation systems, motor drives, medical equipment, solar inverters, power supplies, and electric vehicles (EVs).

Recent advances in isolation technology are enabling new solutions, reducing system cost, and allowing customers to push the performance envelope of their equipment. This article discusses key end applications that are driving cutting-edge innovations in isolation technology and benefitting from these innovations.

Reinforced isolation

Reinforced isolators are devices that can provide insulation equivalent to two basic isolators in series. By themselves, reinforced isolators are considered sufficient to ensure electrical safety against high voltage. However, reinforced isolators must satisfy increasingly tighter performance requirements. Motor-drive applications have the most stringent specifications for reinforced isolation because these systems use very high incoming supply voltages and they involve interfaces accessible to human operators. The requirements for isolation in motor control are defined in safety standards. For example, the IEC 61800-5-1 electrical, thermal and energy safety standard for adjustable speed drives. According to this standard, the requirements on reinforced isolation scale up with an increase in the system voltage which is defined as the root-mean-square (rms) voltage between incoming supply lines and earth.

To guarantee reinforced insulation for drives with system voltage greater than 600 V_{AC}, an isolator must withstand a 5-second temporary overvoltage of at least 4400 V_{RMS}. This isolator also must have a surge voltage

Figure 1. Typical isolation configuration for a power drive system

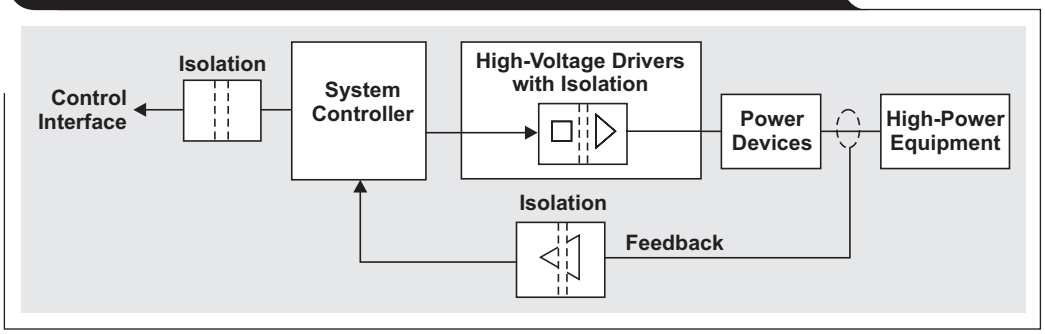
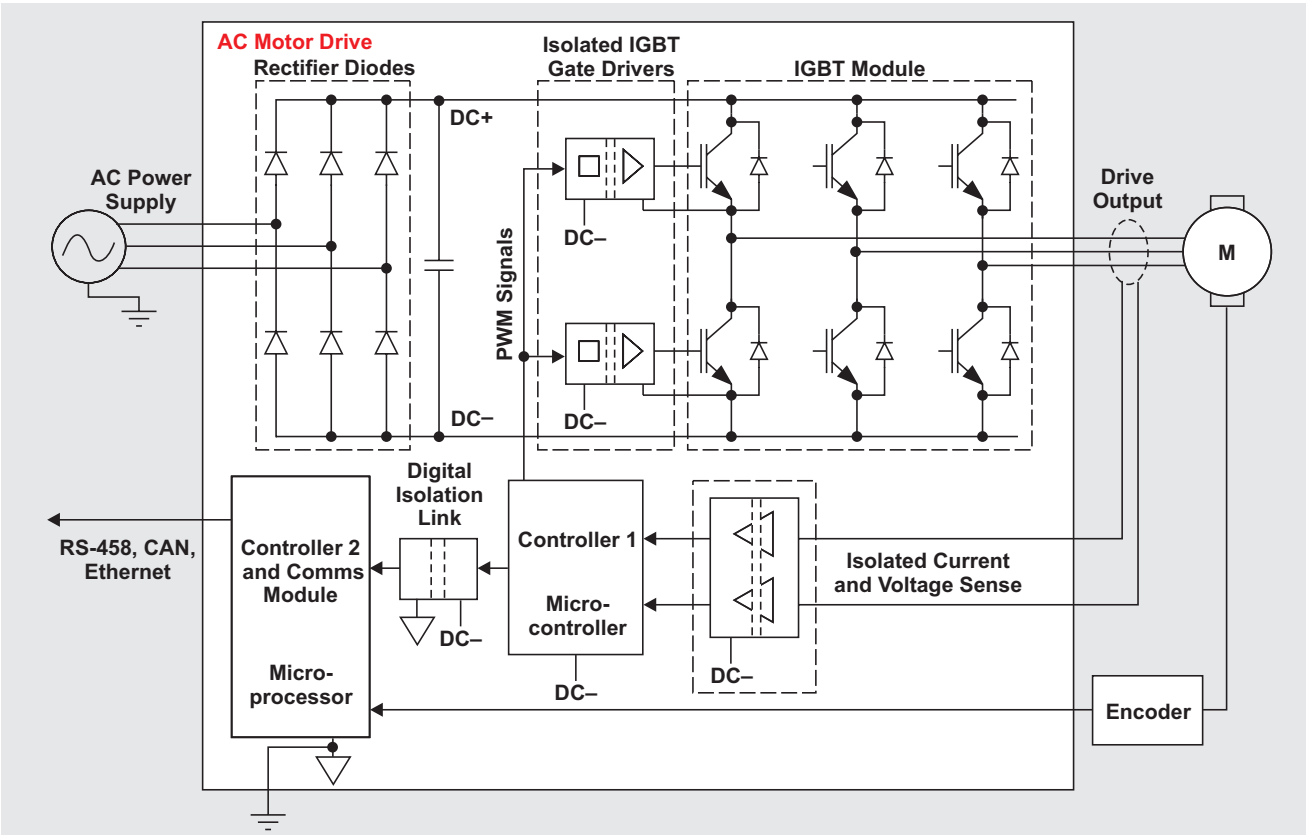


Figure 2. New motor drive architecture

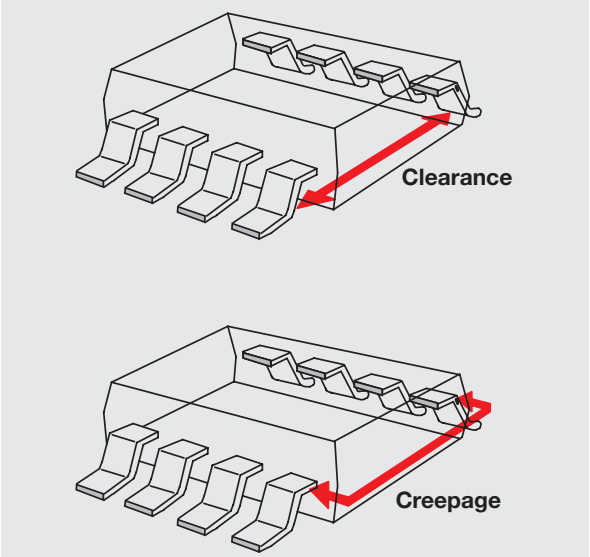


capability of at least 12 kV_{PK}, creepage and clearance of at least 14 mm, and a working voltage in the range of 600 V_{RMS} to 1000 V_{RMS}, which depends on the supply line voltages and drive architecture. To make matters more challenging, new motor-drive architectures are adding local field-programmable gate arrays (FPGAs) and controllers to the power board referenced to the DC bus (Figure 2, controller 2). This reduces the local isolation requirement on the power board. However, it increases the data rate and bandwidth requirement on one, multichannel integrated, high-speed reinforced link (Figure 2, digital isolation link). Until recently, isolators meeting these isolation requirements, as well as the timing and data rate requirements, were not available in the market. The only alternative was fiber-optic isolation.

Capacitive reinforced isolation solutions are now available that meet the above requirements for high isolation, wide packages, and high data rates. These solutions are a good fit for motor-drive applications with system voltages beyond 600 V_{AC}. Some optocouplers do meet the high-isolation requirements, but do not meet the data rate or multichannel integration requirements. Additionally, leading magnetic-isolation solutions do not meet the requirement on working voltage/long-term reliability.

Examples of creepage and clearance are illustrated in Figure 3.

Figure 3: Pictorial representation of clearance and creepage



High working voltage

Solar and wind energy applications generally use additional isolation barriers (for example, in the path of the network-communication channel) to achieve reinforced isolation. Hence, the requirements related to reinforced isolation are not as high as in motor-drive applications. However, the requirement for high working voltage can exceed values seen in motor drives. Power plant centralized solar inverters and wind-energy inverters are trending to operate with higher DC bus voltages, extending to 1500 V and beyond. Higher DC-bus voltages enable higher power ratings without increasing the current levels, which keeps copper costs the same. This helps reduce the per-unit cost of energy generated. Another bonus of higher voltage is increased efficiency because the total power output can increase with higher voltage, but when current does not change, the conduction losses also remain the same.

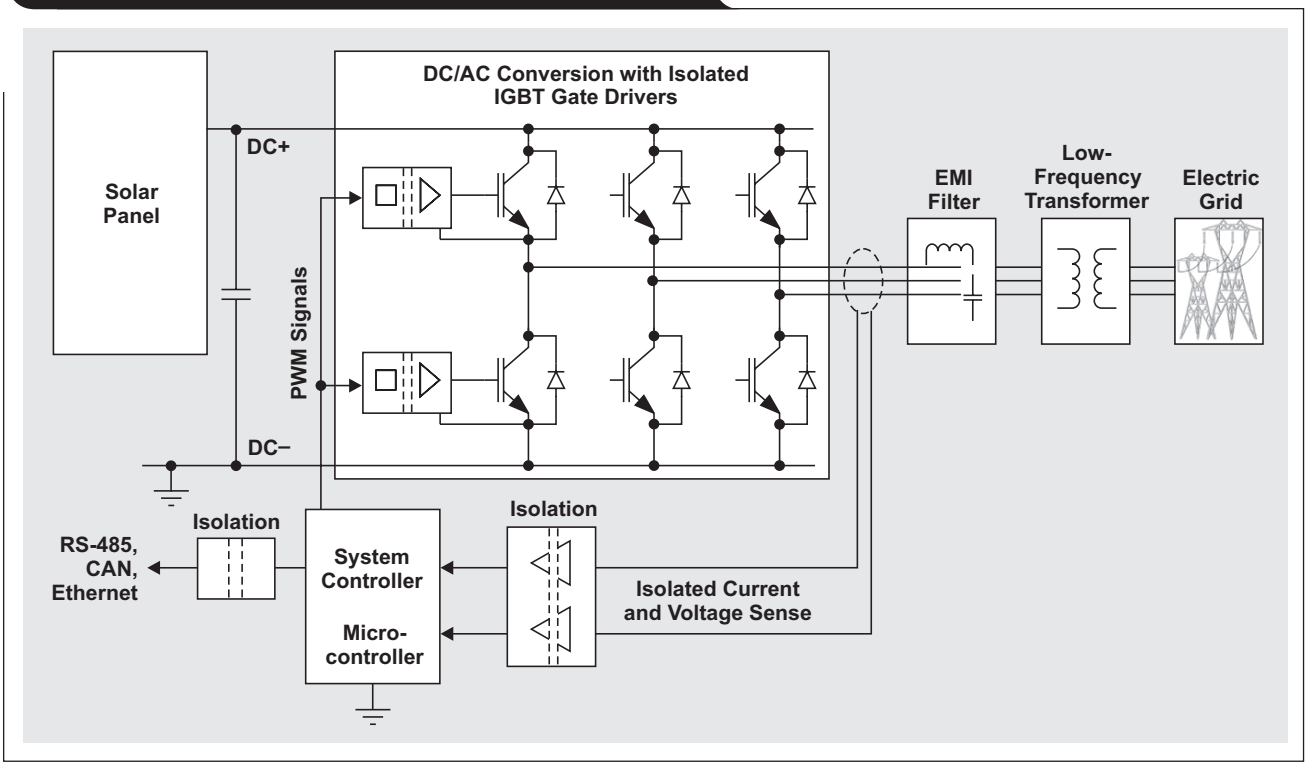
Higher DC bus voltages directly translate to higher working voltages for the isolators used in switching power transistors in the inverter. In Figure 4, the isolated gate drivers (or any digital isolators paired with discrete gate drivers) continuously see a trapezoidal voltage. These voltages appear between one side that is connected to the inverter output, and the other side is connected to earth reference. The peak-to-peak value of this voltage waveform is the DC link voltage. For any isolator, its lifetime degrades exponentially with increased voltage stress across the barrier. Solar and wind inverter systems target lifetimes in excess of 25 years. It is critical to choose an isolator that meets the working-voltage requirement with a liberal margin so that the lifetime of the complete system is not limited by the isolators.

New capacitive isolators achieve a working voltage of 1500 V_{RMS} (2121 V_{PK}). This voltage is a 50% increase compared to commonly available devices, which enables higher-voltage and more efficient inverter systems at a lower cost. Optocouplers have fair isolation and working-voltage performance; however, the LEDs they use limit their lifetimes from an electrical-performance point of view. As mentioned earlier, leading polyimide-based, magnetic-isolation technologies have low working voltage ratings and low long-term insulation reliability, which limits their use in high-voltage, solar-inverter applications.

High common-mode transient immunity

Common-mode transient immunity (CMTI) is the ability of an isolator to tolerate high-slew-rate voltage transients between its two grounds without corrupting signals passing through it. In electric-vehicle motor drives, as well as solar- and wind-energy inverter applications, the

Figure 4. Block diagram of a centralized solar inverter



isolated gate drivers or isolators passing gate controls to power transistors see large ground transients because one ground is connected to rapidly switching inverter outputs. Figure 5 shows the ground potential difference experienced by these gate drivers. In these systems, CMTI is a critical parameter because any bit errors caused by the transients can result in dangerous short-circuit events.

Recent application requirements are pushing the need for isolators with higher and higher CMTI. As stated, one requirement is increasing DC bus voltages. A second is reducing transition times with faster switching in the power transistors, which improves inverter efficiency. A third is increasing switching frequency, which results in lower-cost and less-bulky magnetics such as inductors, transformers and motors. Availability of reliable silicon-carbide or SiC-based power transistors, which can switch faster and tolerate higher voltages versus traditional IGBTs, is building on the trend for inverters that switch faster and more efficiently.

Capacitive isolators released in 2014 broke the barrier for 100-kV/µs CMTI. Capacitive isolators and gate drivers continue to lead the industry with the highest minimum guaranteed CMTI, thus enabling faster, more efficient, and lower-cost inverter designs.

High-altitude operation

Advanced packaging technology is required for isolators used in equipment operating at higher altitudes and in a polluted or high-moisture environments. Improved and wider packages prevent degradation along the package surface and arcing through the air between pins, which ensures isolation quality. Isolators used in solar, wind-energy and e-metering applications fall into this category.

Isolator voltages that continuously operate in heavy pollution can cause package surfaces to degrade and create a conductive path across the isolator. This phenomenon is called tracking. Choosing a higher-quality packaging mold compound that belongs to a lower material group with higher comparative tracking index (CTI) can minimize this effect for a given package creepage and working voltage. Another approach is to choose a wider package with increased creepage to reduce the risk of tracking.

Table 1 shows the requirements on creepage distances depending on working voltage, the pollution degree, and the material group of the isolator's package mold compound for reinforced isolation, according to IEC 60664-1. The requirements on creepage increase with working voltage and pollution degree, however, selecting a lower material group with a higher CTI can reduce the creepage requirement.

At higher altitudes of 2000 to 5000 meters above sea level, the air pressure is lower. Therefore, peak overvoltages, such as surge or temporary overvoltage, can more readily cause arching between the isolator pins. Equipment operating at high altitudes requires greater spacing between pins (more clearance). Table 2 shows the multiplication factors by which clearance must be increased at higher altitudes to prevent arcing per IEC 60664-1.

Traditionally, conformal coating or potting techniques involving deposition of insulating polymer or other material over the printed circuit board (PCB) have been used to reduce the pollution degree around the isolator. This reduces the requirement on creepage and clearance. However, these methods add cost, are less reliable, and need additional inspection steps in PCB manufacturing. Wide-body isolators manufactured with high-quality molding compounds eliminate the need for conformal coating or potting, simplify PCB design, and increase manufacturing reliability.

Figure 5. Inverter output switching profile translates to high CMTI for isolators

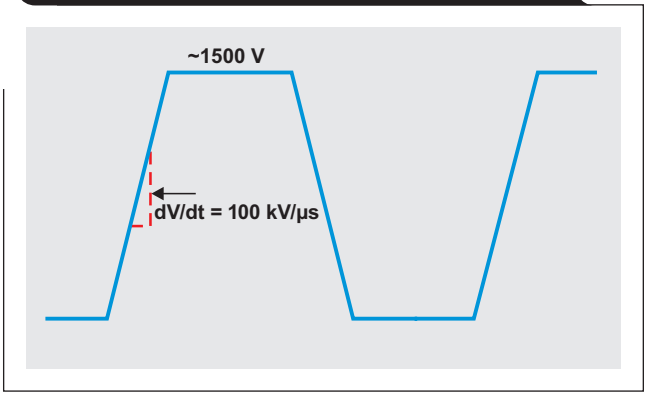


Table 1. Creepage requirements depending on working voltage and package material group

Working Voltage (V_{RMS})	Minimum Creepage (mm)					
	Pollution Degree 2 Material Group			Pollution Degree 3 Material Group		
	I	II	III	I	II	III
200	2	2.4	4	5	5.6	6.4
400	4	5.6	8	10	11.2	12.6
800	8	11.2	16	20	22	25
1000	10	14.2	20	25	28	32

Table 2. Multiplication factors for clearances at higher altitudes

Altitude	Multiplication Factor for Clearances
2000	1
3000	1.14
4000	1.29
5000	1.48
6000	1.7
7000	1.95

New isolators use the best quality mold compound (CTI material group I) and are available in wide packages (14.5 mm creepage/clearance). These isolators can enable high-altitude designs and tolerate higher pollution without requiring additional steps in PCB manufacturing.

Capacitive digital isolators

Recent advances in capacitive digital isolators place them at the forefront of technology. These new isolators offer higher isolation performance, long-term reliability, increased channel integration, higher data rates and precision timing performance, better quality package mold compound, wider packages (14.5-mm creepage/clearance), and CMTI exceeding 100 kV/µs. Combining these features enables new applications, reduces system cost, and allows end-equipment manufacturers to push the performance envelope of their solutions.

Texas Instruments offers the ISO78xx family of reinforced digital isolators and the ISO585x and ISO545x families of reinforced isolated IGBT gate drivers. These isolators offer features and capabilities that can solve difficult isolation problems. These isolators have a working voltage of up to 1500 V_{RMS}, are rated for 40 years, have surge voltage capability of 12.8 kV, and withstand a temporary overvoltage of 5700 V_{RMS}. They offer high data rates of up to 100 Mbps with low skews and part-to-part variations and CMTI exceeding 100 kV/us. They also use material group I mold compound and are available in industry-leading wide packages.

References

1. IEC 61800-5-1 Ed. 2.0, Adjustable speed electrical power drive systems, safety requirements, electrical, thermal and energy. July 2007
2. Anant S Kamath and Kannan Soundarapandian, “High-voltage reinforced isolation: Definitions and test methodologies,” Texas Instruments White Paper, November 2014 (SLYY063)
3. Anant S Kamath, “Isolation in AC Motor Drives: Understanding the IEC 61800-5-1 Safety Standard,” Texas Instruments White Paper, November 2015 (SLYY080)
4. IEC 60664-1 Ed. 2.0, Insulation coordination for equipment within low-voltage systems, principles, requirements and tests, April 2007

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Product information:
ISO7821, ISO7831
ISO7840, ISO7841, ISO7842
ISO5851, ISO5852S
ISO5451, ISO5452

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How to reduce current spikes at AC zero-crossing for totem-pole PFC

By Bosheng Sun
Systems Engineer, High Power Controller Solutions

Introduction

Power factor correction (PFC) is widely used in AC/DC power supplies with an input power of 75 watts or greater. PFC forces the input current to follow the input voltage so that any electrical load appears like a resistor. Amongst all the different PFC topologies, the totem-pole PFC[1, 2] has recently received more attention because it uses the least number of components, has the smallest conduction loss, and has the highest efficiency. Typically, a totem-pole PFC cannot operate in continuous-conduction mode (CCM) because of the slow reverse recovery of the MOSFET's body diodes. However, with the advent of the gallium-nitride (GaN) FET, its diode-free structure makes the CCM totem-pole PFC possible. Figure 1 is a totem-pole PFC structure.

In Figure 1, Q3 and Q4 are GaN FETs. Depending on V_{AC} polarity, they alternatively operate as a PFC active switch or a sync switch. To further improve efficiency, D1 and D2 are replaced with regular MOSFETs because the conduction loss for MOSFETs is lower than for diodes. The revised structure is shown in Figure 2 where Q1 and Q2 are regular MOSFETs and are driven at AC frequency.

The current flow paths for a totem-pole PFC are shown in Figures 3 and 4. During the positive AC cycle, Q4 is the active switch, while Q3 works as a sync FET. The driving signals for Q4 and Q3 are complementary: Q4 is controlled by D (duty cycle from control loop) and Q3 is controlled by 1 – D. When Q4 turns on, the current goes through the AC line, inductor, Q4, Q2, and then back to AC neutral. When Q4 turns off, Q3 turns on, the current goes through the AC line, inductor, Q3, load, Q2, and then back to AC neutral. Q2 stays on for the whole positive AC half-cycle and Q1 remains off.

Figure 1. Totem-pole PFC with GaN FETs and line-rectification diodes

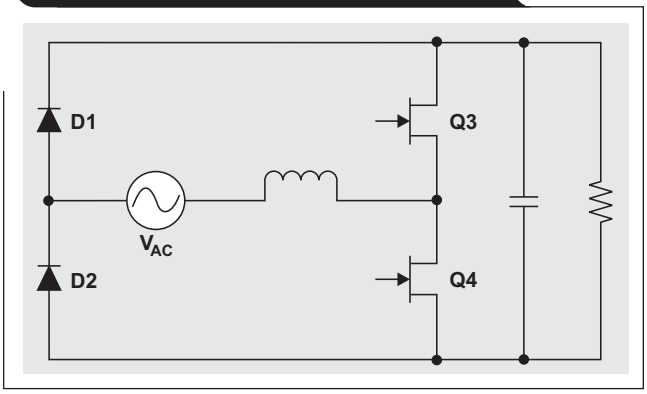


Figure 2. Totem-pole PFC with GaN FETs and line-rectification MOSFETs

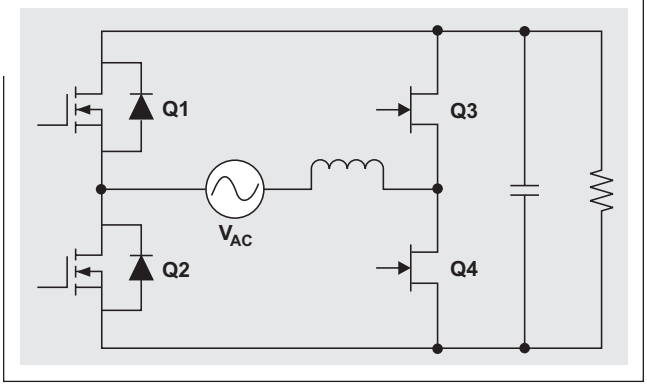


Figure 3. Current paths for positive AC cycle

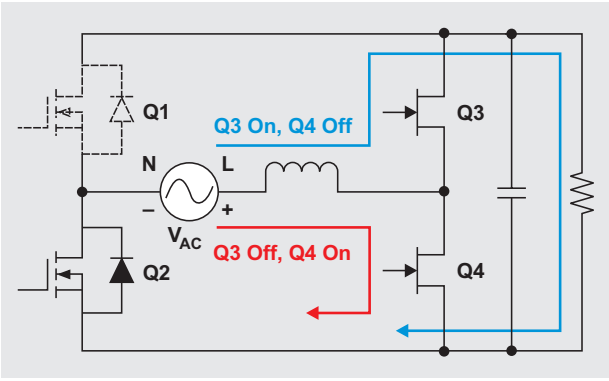
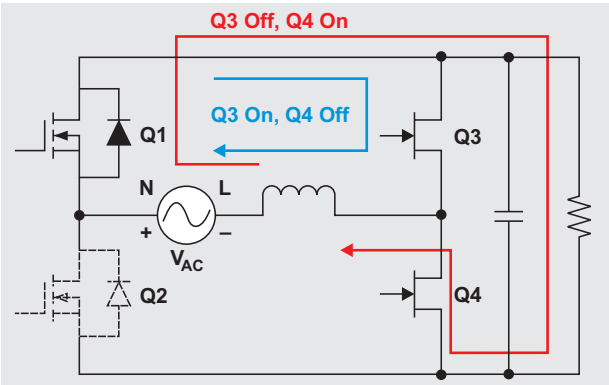


Figure 4. Current paths for negative AC cycle



During the negative AC cycle, the function of Q4 and Q3 swaps: Q3 becomes the active switch and Q4 works as a sync FET. The driving signal for Q4 and Q3 are still complementary, but Q3 is now controlled by D and Q4 is controlled by 1 – D. When Q3 turns on, the current goes through AC neutral, Q1, Q3, inductor, and then back to AC line. When Q3 turns off, Q4 turns on, the current goes through AC neutral, Q1, load, Q4, inductor, and then back to AC line. Q1 stays on for the whole negative AC half-cycle and Q2 remains off.

One of the challenges in totem-pole PFCs is that the input current has big spikes at the V_{AC} zero-crossing. The issue is inherent with totem-pole PFCs and very complicated. In fact, the spikes contain both positive and negative spikes, and they occur for different reasons. There are several scenarios that can cause current spikes.

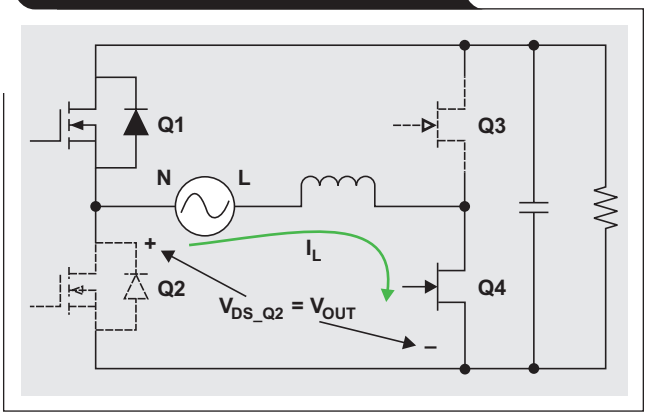
Scenario 1

As shown in Figure 5, when the operation mode changes from negative cycle to positive cycle at the AC zero-crossing, the duty ratio of switch Q3 changes abruptly from almost 100% to zero. The duty ratio of switch Q4 changes abruptly from zero to almost 100%. Because of the slow reverse recovery of the Q1 body diode and the large C_{OSS} of Q2, the V_{DS} voltage of Q2 still equals V_{OUT} (400 V). Since this high voltage is applied to the inductor when Q4 turns on, a positive current spike is generated. This scenario is analyzed in Reference 3 and a Q4 soft-start method is proposed to solve this issue.

Scenario 2

However, even with soft turn on of Q4, there are still excessive current spikes. This is because V_{AC} is very low right after zero-crossing and is therefore insufficient for the inductor current to build up. On the other hand, when Q3 turns on with 1 – D, even though its duty is not high, the voltage applied to the inductor is high (400-V V_{OUT}). The resulting high reverse current through the inductor causes a negative current spike.

Figure 5. Current spike caused by sudden turn on of Q4



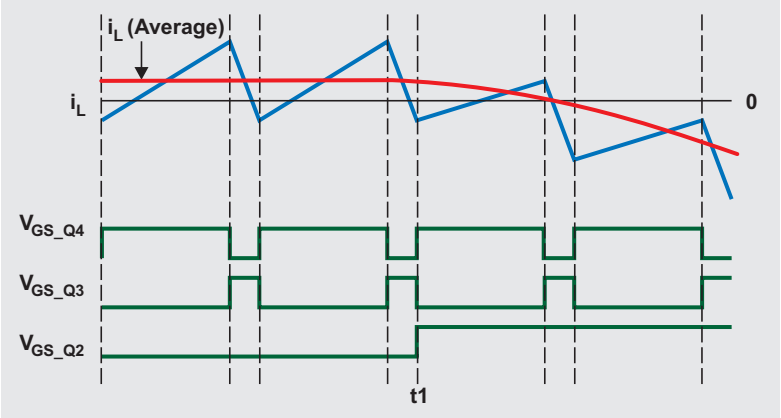
Scenario 3

Timing for Q2 turn on is also critical. A short-through can occur if Q2 turns on before Q4 soft start and if the body diode of Q1 does not recover quickly enough.

Scenario 4

If Q2 turns on too late, a negative current spike can be generated (Figure 6). The high V_{BUS} voltage generates a reverse inductor current when Q3 is on while Q2 is off. This reverse current first turns off the Q2 body diode, then starts to charge C_{OSS} of Q2 and the V_{DS} of Q2 builds up to a high voltage. Then, when Q4 turns on, the high voltage (V_{DS} + V_{IN}) that is applied to the inductor results in high rising current in the inductor. Therefore, the inductor's rising and falling currents are both large magnitude, which achieves a balance that maintains the average current at a small positive value. Now, if Q2 suddenly turns on at t1, V_{DS} of Q2 will be clamped to zero. When Q4 turns on, only V_{IN} is applied to the inductor. Since V_{IN} is very small, which is insufficient for the inductor to build up current high enough, the inductor's rising current becomes very small. Because the falling current still has a large magnitude, the balance is broken and results in a large negative current spike.

Figure 6. Current spike caused by turning on Q2 too late



Reducing current spikes at AC zero-crossing

A new control method is provided in this article to solve the current-spiking issue. In this method, Q1, Q2, Q3, and Q4 are turned on with a special sequence and each executes a soft-start mechanism. The driving signals for this new method are shown in Figure 7:

In this solution, when V_{AC} changes from a negative to positive cycle, after AC zero-crossing, Q4 first turns on with a very small pulse width. The pulse width then gradually increases to D (the duty cycle generated by control loop). By doing a soft-start on Q4, Q1 completely reverse recovers. Now the voltage, $V_{DS,}$ of Q2 gradually reduces to ground, thus the positive spike caused by scenario 1 is eliminated.

Once the Q4 soft-start is complete, the sync FET, Q3, starts a soft turn-on with a tiny pulse width and gradually increases until the pulse width reaches 1 – D. This eliminates the negative current spike caused by scenario 2.

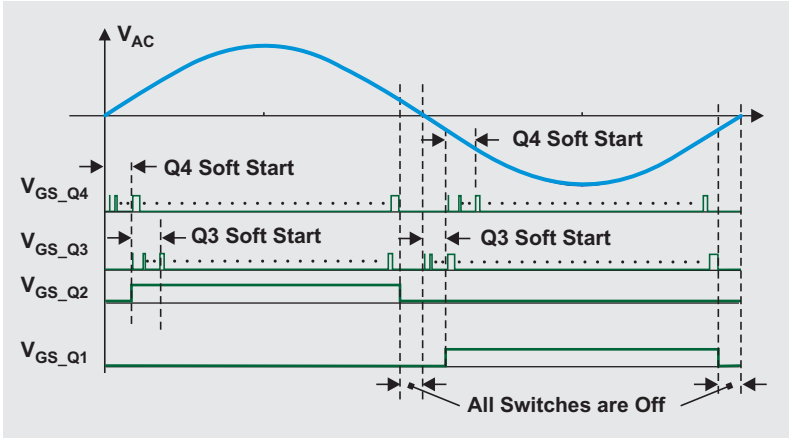
At the same time when the Q4 soft-start is complete and the Q3 soft-start begins, the low frequency switch, Q2, is turned on. Since the body diode of Q1 is already recovered, there is no short-through issue as mentioned in scenario 3.

Also, since Q3 starts with a very small pulse width, it is insufficient for an inductor to build a negative current high enough, and thus eliminates the current spike caused in scenario 4.

Finally, the zero-crossing detection could be mistriggered by noise. For safety purposes, all the switches are turned off at the end of a positive cycle. This leaves a small dead zone to prevent the input AC from short circuiting. Note that the control loop should freeze during this dead zone. Otherwise, when the PFC turns back on, the integrator build-up in the loop generates a large PWM pulse, which can cause a large current spike.

The same operation principle applies to the AC transition from a positive to a negative cycle.

Figure 7. Gate signals timing for proposed method



Experiment results

The method proposed earlier was verified on a 1-kW totem-pole PFC that was controlled with a UCD3138 digital controller from Texas Instruments. Figure 8 is the current waveform with a traditional control method and Figure 9 shows the current waveform with the proposed method. Both were tested with the same conditions. Notice how the current spikes are significantly reduced with the proposed method and the current waveform becomes much smoother at AC zero-crossing. As a result, the total harmonic distortion (THD) is reduced from 8.1% to 3.7%.

Figure 8. Current waveform using a traditional control method

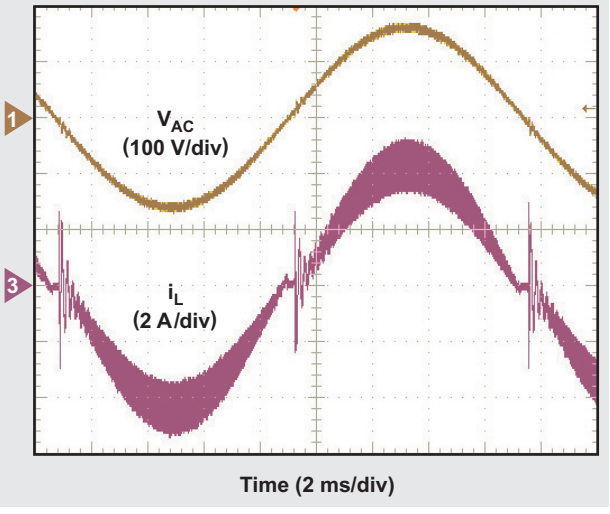
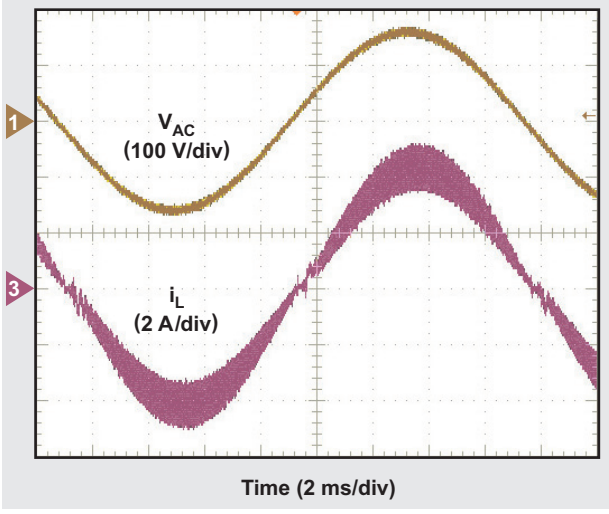


Figure 9. Current waveform with the proposed control method



Conclusion

While totem-pole PFC is attracting more attention, some design challenges prevent it from being widely adopted. One inherent issue in a totem-pole PFC is the current spikes at AC zero-crossing. The causes for current spikes are complicated: turn-on sequence, slow reverse-recovery of MOSFET's body diode, large C_{OSS} of MOSFET, sudden turn on of the active FET with almost 100% duty cycle, sudden turn on of the sync FET, and so on. All these scenarios contribute to spikes. By turning the switches on with a special sequence, and executing a soft-start mechanism on both the main and sync FETs, current spikes can be significantly reduced and THD is significantly improved.

References

1. J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs," in Proc. IEEE Applied Power Electronics Conf., Mar. 1995, pp. 473–479.
2. L. Huber, Y. Jang and M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers", IEEE Transaction on Power Electronics, Vol. 23, No. 3, May 2008.
3. B. Su, J. Zhang and Z. Lu, "Totem-pole Boost Bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," IEEE Trans. Power Electron., vol.26, no.2, Feb. 2011.
4. Z. Ye, A. Agular, Y. Bolurian and B. Daugherty, "GaN FET-Based CCM Totem-Pole Bridgeless PFC," The 23rd TI Power Supply Design Seminar, 2014.

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UCD3138

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Faster, cooler charging with dual chargers

By Jeff Falin
Applications Engineer, Power Management Battery Management Systems High Power Chargers

As the functionality and related power demands of the rechargeable battery-powered electronics such as smartphones and cameras grew, so did their batteries' capacities in order to extend run time. With higher-power wall adaptors and USB 3.x providing higher currents at 5 V, 9 V and 12 V, increasing the charger's input current limit to accept the additional power gives more charging current for faster charging. This also results in more losses that the charger dissipates as heat. Historically, these losses have been distributed through the PCB ground plane by careful placement of the external FETs with the charge-controller IC's. Consumer demand for smaller portable electronics has forced IC manufacturers to develop battery-charger ICs with integrated FETs (I-FETs) and with smaller packaging. Including thermal considerations early in the design is critical to ensure that these high-current, I-FET chargers provide the designed charge current without overheating the PCB.

Thermal management in portable devices requires careful PCB layout. For example, removing the heat from an IC in a QFN package with an exposed bottom thermal pad requires that the thermal pad be connected to a copper ground plane that is not thermally saturated, preferably exposed (as opposed to internal). Too many ICs in close proximity that are trying to use the same heat-sinking ground plane can saturate the plane with heat, causing the ICs to overheat and go into lower-power thermal-regulation mode, or even shutdown.

Additionally, when the ground plane of the printed-circuit board (PCB) is thermally saturated, the device's outside case temperature rises to unacceptable levels. To prevent this, each IC and a section of its adjacent ground plane should be allocated a portion of a thermal budget. The thermal budget sets a hard limit to the amount of heat that a single, small-footprint, I-FET charger, outputting several amperes of current, can dissipate without raising the device's case temperature.

For a buck charger with integrated FETs, the IC's efficiency is

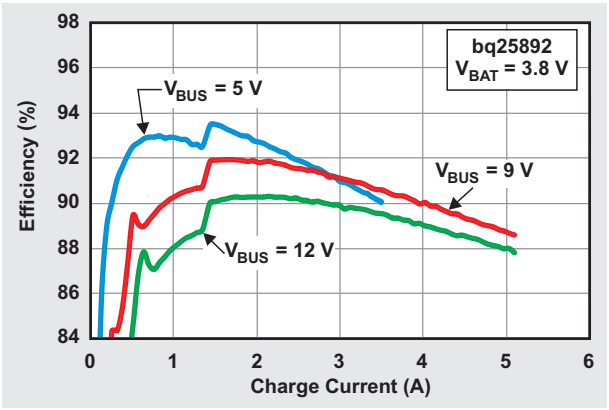
$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{BAT} \times I_{CHRG}}{V_{BUS} \times I_{BUS}}$$

and loss through heat is

$$P_L = P_{IN} - P_{OUT} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right)$$

At higher currents, this loss is dominated by the I^2R losses across the internal FETs. Figure 1 shows the efficiency of a battery charger, such as the bq25890, at different charging currents and input voltages.

Figure 1. Example of I-FET charger efficiency

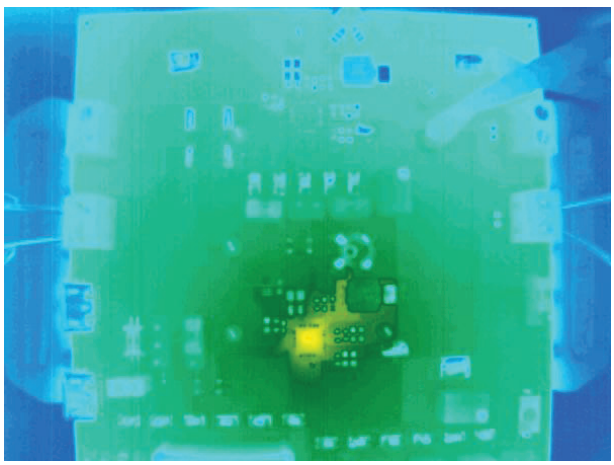


With a 9-V input adapter, a battery charger with 91% efficiency was set to provide a 3-A charging current to a 3.8-V charged battery with loses of

$$P_L = 3.8\ V \times 3\ A \times (1 / 0.91 - 1),$$

which equals 1.13 W in heat. The charger IC was soldered onto a four-layer, 31-mil thick, FR-4 board with 2-oz copper. The package's thermal pad was properly soldered down to the top-layer copper ground pour and through vias-to-ground pours on each of the internal and bottom layers. All of this copper acted as a heat sink. The image in Figure 2 shows a thermal image for a 4- by 4-mm QFN package where the temperature rise was 16.1°C at the IC's top-side case with a 25°C ambient air temperature. In this

Figure 2. Thermal image of single-charger operation (V_{IN} = 9 V, V_{BAT} = 3.8 V, I_{CHRG} = 3 A)



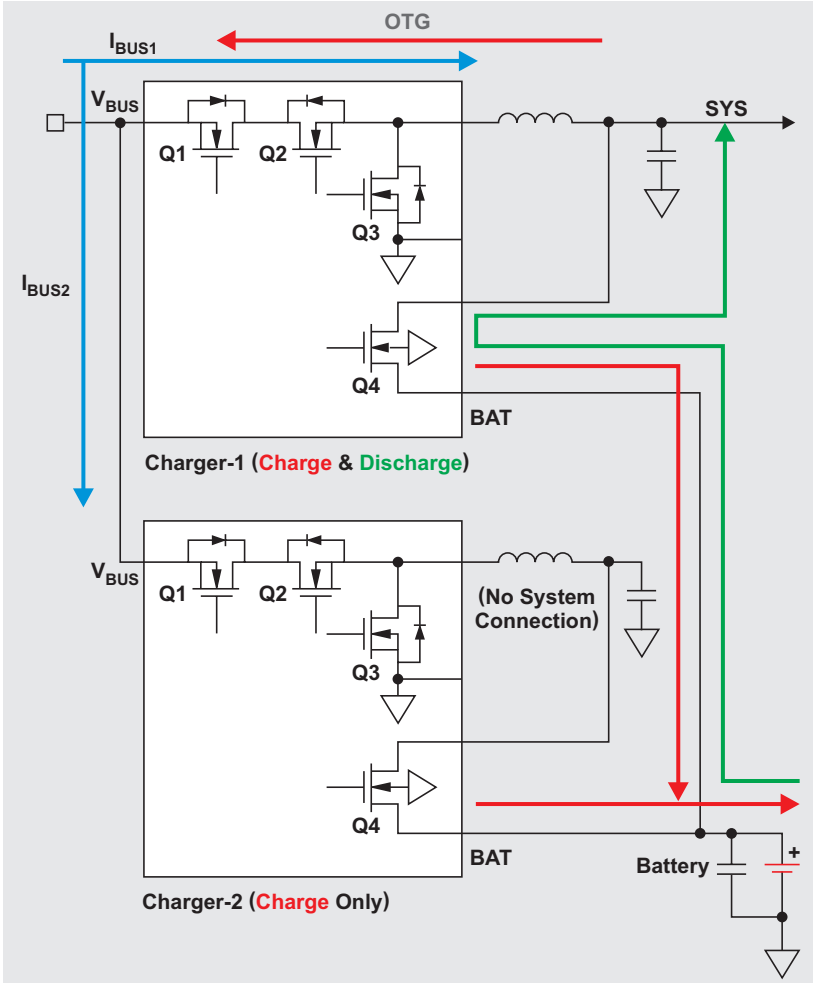
image, cool is shown as blue/green, warm as yellow, and hotter would show as red to white.

The PCB tested for Figure 2 contained no other power dissipating ICs, so the copper ground area approximates an infinite heat sink and was not saturated. This state is evidenced by the blue and green colors surrounding the yellow hot spot of the IC.

Increasing the charging current of this same charger by 50% to 4.5 A resulted in a temperature rise of 37°C compared to 25°C ambient. This temperature rise may be within the thermal budget of some devices, but not others.

Using the same concept of thermal distribution across the PCB as a charge controller with external FETs, two I-FET charger ICs in parallel, referred to as a dual-charger configuration, can be used. In general, there is no stability issue when connecting the battery-output pins of multiple chargers in parallel. This is because, while in constant-current (CC) mode, the charger's battery pin (BAT) has the characteristics of a high-impedance current source. While in constant-voltage (CV) mode, but well before termination, the battery pin characteristics are like a low-impedance voltage regulator. Dual-charger ICs in a parallel configuration are shown in Figure 3.

Figure 3: Dual-charger ICs in a parallel configuration



Charger-1 is configured for charging, however, if the internal battery FET (Q4) that provides a power path has low enough $R_{DS(on)}$, this IC also provides battery discharge through Q4. Charger-2 is configured only for charging. If required, charger-1 exclusively provides a USB On-The-Go (OTG) 5-V power rail at V_{BUS} after charger-2 has been configured for high-impedance mode. Even with the same termination voltage and current settings, and high regulation accuracy, one charger always attempts to terminate before the other due to the mismatch in each charger's internal reference voltages and currents. If both chargers are set to the same termination current, both chargers will have difficulty terminating the charge. Therefore, the termination current of one charger (typically charger-2) should be set higher than the other (typically charger-1) to allow for a smooth termination.

When the total required input current is high (for example, I_{CHARGE} > 5 A with a 5-V adapter), the parallel configuration is recommended for best thermal distribution. With both input pins connected, neither charger can use its control loop for automatic input-current-limit optimization (ICO) to extract maximum adapter power without causing loop instability at their mutual V_{BUS} node. Therefore, each charger's current-limit feature should be set to half the adapter's maximum output current. Inductor current ratings may also be reduced by half as well.

To prevent the V_{INDPM} loop from causing instability and to give charger-1 priority in powering the system, set the V_{INDPM} for charger-2 higher than that of charger-1. If the chargers have an integrated analog-to-digital converter (ADC) to provide real-time measurements of the charge current and the input, system and battery voltages, the host software must continuously monitor this information, as well as the loop status bits. The host software must then refresh each charger's current limit and charge current settings in order to maximize adapter power while balancing power and thermal loading between the two chargers.

When the total required input current is lower (for example, I_{CHARGE} < 5 A or an adapter change from 9 V to 12 V) and charger-1's reverse-blocking and current-limiting FET (Q1) has low enough $R_{DS(on)}$, the cascade configuration shown in Figure 4 may be a better option.

In the cascade configuration, charger-1 controls the total input current for both chargers. Host software development is greatly simplified because the V_{INDPM} and ICO features for charger-1 can be fully utilized to maximize adapter power extraction. In the event of a large system load transient while in the CV mode, the buck converter for charger-1 could see a higher input current. Therefore, the inductor for charger-1 needs to be sized to handle the adapter's full input current. If members of the same charger family with different I^2C addresses are available, say the bq25890 for charger-1 and bq25892 for charger-2, development is even easier because no additional hardware is required to switch between the I^2C communication lines of each charger.

Using the same PCB and test setup from Figure 2, the cascade chargers (Figure 4) were set to provide 2.25-A charge current to a 3.8-V battery and were 92% efficient. The heat loss for each charger was only

$P_L = 3.8\ V \times 2.25\ A\ (1/0.92 - 1) = 0.74\ W.$

The top-side case temperature of both chargers rose above 25°C ambient by only 17°C, as measured by the thermal camera image in Figure 5. This is only 1°C above the single-charger case from Figure 2 for a 50% increase in charge current.

Figure 4: Dual-charger ICs in a cascade configuration

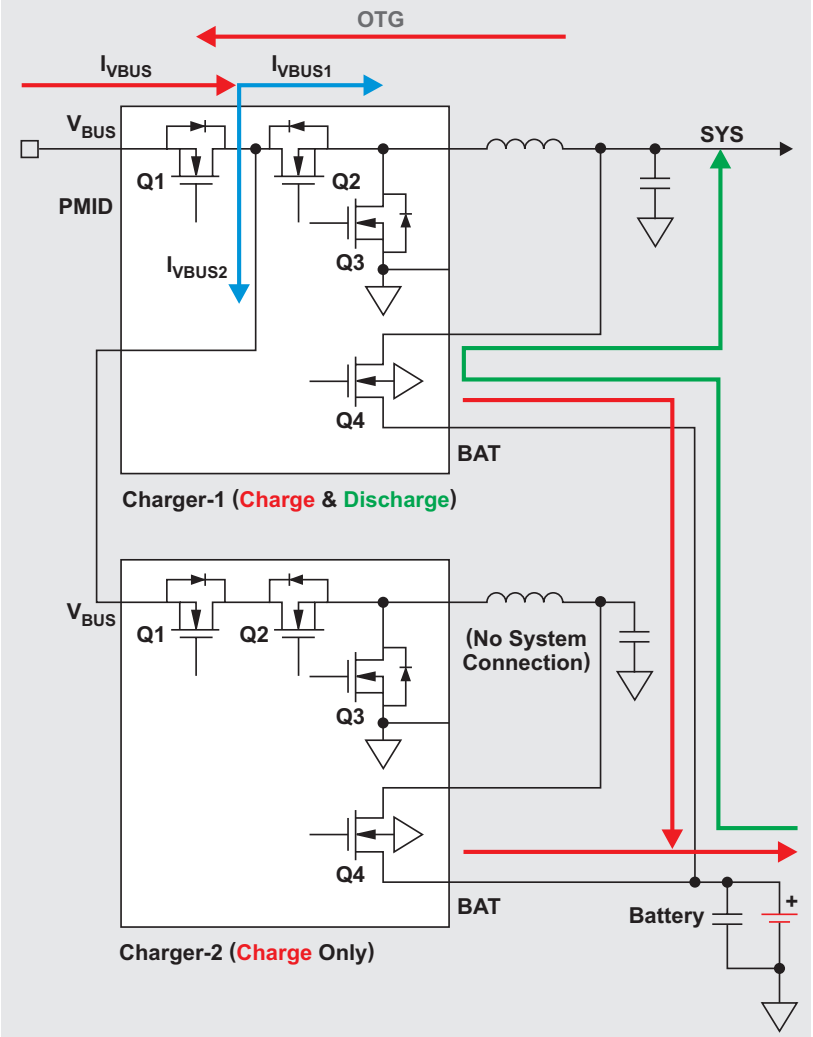


Figure 5. Thermal image of dual-charger operation (V_{IN} = 9 V, V_{BAT} = 3.8 V, I_{CHRG} = 4.5 A)

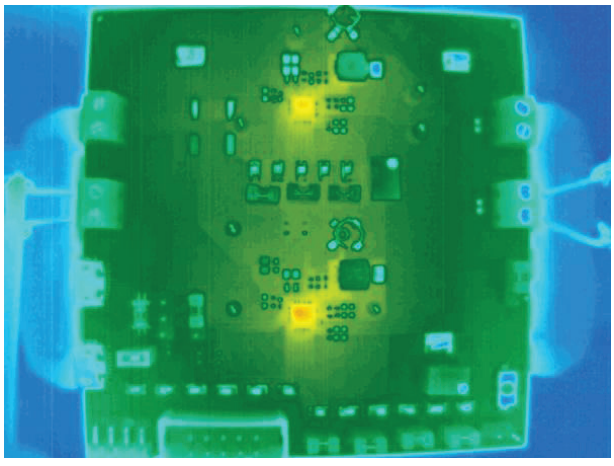


Figure 6 shows the typical charger-termination profile as the charger transitions from constant-current to constant-voltage regulation. Following the previous recommendation, for a clean termination, charger-2 terminates charging before charger-1.

Conclusion

Most battery-charger ICs have a thermal regulation loop that reduces their charge current in order to protect the IC from damage due to overheating. As such, PCB thermal management is critical to maximize the charge current (which reduces charge time) into today's high-capacity batteries in addition to maintaining practical outside case temperatures. Thermal management includes assigning thermal budgets to all heat-producing ICs, careful IC placement, and heat-sink grounding on the PCB to distribute heat without thermally saturating the copper pours and planes of PCB ground. Using I-FET dual chargers, either in a parallel or cascade configuration as the application allows, gives better heat distribution for lower IC and case temperatures along with faster, cooler charging and longer device run times.

Reference

1. "Dual Battery Charger IC Reference Design (connected in Cascode Configuration)," TI Designs, TIDA-00590

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bq25890
bq25892
bq24715

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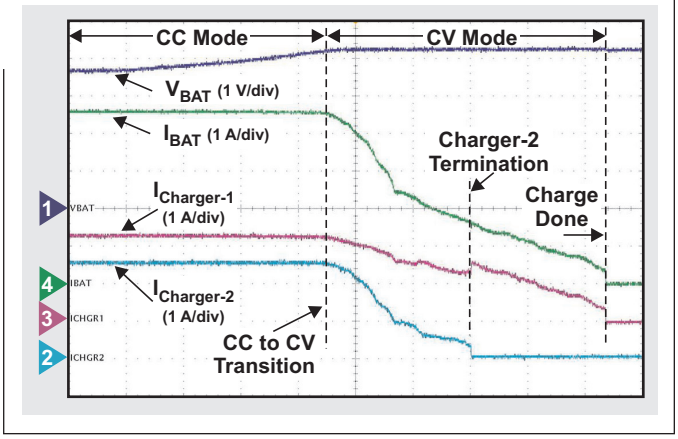
Figure 6. Dual-charger charge-termination profile



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