Selecting a Multichannel Ultra-Low-Current Measurement IC

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Introduction

When simultaneously measuring large numbers of very low current levels (<1 µA) in parallel at relatively low speeds (<100 kSPS) but with high accuracy (>16 bits), two solutions available to engineers include the Texas Instruments (TI) AFE family of X-ray analog front ends and the DDC family of analog-to-digital converters (ADCs). Although originally designed for medical imaging applications, these devices also work in instrumentation, in-vitro diagnostic applications, and any other applications with large numbers of photodiodes or a large parallel number of voltage measurements.

In both device families, the measured currents are not floating (shunt) but sinking or pulling from a fixed DC level (see **Figure 1** and **Figure 2**) because the input is virtually shorted to a voltage through the feedback action of an amplifier, like in the case of a discrete transimpedance amplifier. Unlike transimpedance amplifiers, however, which convert current into voltage by multiplying by a resistor (in the feedback of the input amplifier), both families use an integrator as the first stage.

Both device families integrate most of the required components into a single IC, enabling functionality from current input to digital output (a serial stream in both cases). This functionality includes the ability to adjust the full scale (the input gain) to optimize the signal-to-noise ratio for a particular application or even to use the same solution for different applications, creating a platform design. Besides the board-space savings, this level of integration – with many of the system-level specifications set and backed by the data sheet of these devices – enormously simplifies design work and testing strategies during production, which then results in reduced time to market and lower development costs.

Although many applications can use either device, their differences are significant enough that one or the other will be a better fit for a given application. In this article, we will explain why.

DDC

The DDC family extends from a two-channel device (the DDC112) all the way to a 256-channel device (the DDC2256), with intermediate versions for four, eight, 16, 32, 64 and 128 channels. Every DDC channel outputs a digital value corresponding to the integration (charge) of an input current between two instants (two consecutive edges of a clock signal). Engineers can see the DDCs as a transimpedance amplifier followed by an ADC equivalently, where instead of a resistor, a combination of the feedback capacitor and integration time (sampling rate) sets the gain (see **Figure 1**).

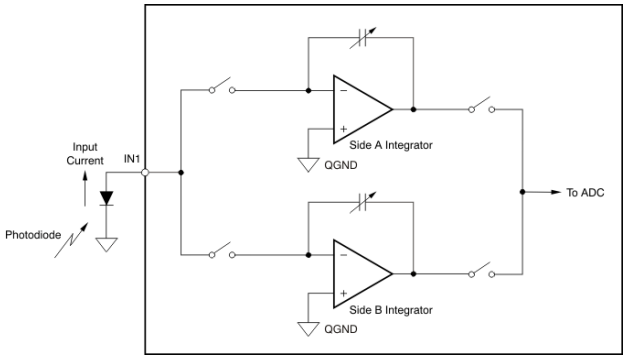

Figure 1. *A dual-integrator DDC input architecture*

In applications such as computed tomography scanners or fluorescence measurements, getting a charge value as the numerical device output has the advantage of directly providing, with a single reading, a value proportional to the total number of photons incident on the photodiode during that interval (instead of sampling the signal continuously and adding up the samples later). The signal does not have to be continuous during that time and the DDC's input integrator integrates even fast current pulses between two edges. The bandwidth of the front-end integrator is actually larger (approximately in the megahertz range) than what the sample rate could lead one to believe.

For applications in which users prefer to process the data in current units, dividing the charge result by the integration period (the time between the two edges) obtains the average current value. Any temporal information in that interval will be lost and translated into a single average current sample.

Depending on the DDC device, it is possible to adjust the sampling rate (the inverse of the integration period) from 1 SPS to 100 kSPS (with the DDC316 only at 12 bits). A more standard value for the maximum sample rate for most DDCs is around 6 kSPS per channel with 20-bit resolution. **Table 1** summarizes the top-level specifications for each device in the DDC family.

Device Name	Number of Channels	Minimum Maximum Channel Sample Rate [kSPS]	Maximum Full-Scale Charge [pC]	Maximum Full-Scale Current [µA]	Power [mW/ Channel]	Number of Bits
DDC112	2	0.001-3	1,000	3	85	20
DDC114	4	0.001-3	350	1	18	20
DDC118	8	0.001-3	350	1	18	20
DDC316	16	1-100	12	1.2	28	12 at 100 kSPS 16 at 50 kSPS
DDC232	32	0.001-6	350	2	10	20
DDC264	64	0.001-6	150	1	5.5	20
DDC1128	128	0.001-6	150	1	5.5	20
DDC2256	256	1-17	150	2.5	2	24

Table 1. *Top-level specification for devices in the DDC family*

The devices' programmable full scale (swapping the integration capacitor) enables you to optimize the noise floor for a given application, assay or run, which is particularly important for instrumentation applications. Increasing the input gain will lower the noise floor down to 0.2 fC_{rms} (1,250 electrons). Nevertheless, larger dynamic ranges are obtained at the lower gains (higher full-scale inputs), with typical values around 90 dB.

With current computed as the charge divided by the integration time, the maximum current (in the linear range) is given by the maximum full-scale charge setting and minimum integration time. **Table 1** also lists these results. Typical maximum full-scale charges range from 150 pC to 350 pC, although the DDC112 enables the use of an external feedback capacitor that can take the range beyond 1 nC. In current units, the maximum range will be approximately 1 µA.

One major difference between the X-ray AFE and DDC families is that DDCs can only measure current flowing into the input terminal. That said, all DDCs have about 0.4% of the full scale as margin for currents leaving the terminal, which enables calibration of the offset at the zero-current point. Also, there are relatively simple techniques that enable the measurement of negative currents with an external resistor [**3**].

Finally, the devices come in leaded or ball-grid array (BGA) packages, which makes their handling straightforward through standard assembly methods.

X-ray AFE ROICs

The AFE family of readout integrated circuits (ROICs) comprises three devices: the AFE0064, AFE1256 and AFE2256.

TI originally designed AFE devices to measure the charges collected by an array of pixels (photodiodes) in a thin-film-transistor flat-panel detector. Given the nature of the signals in this application, the devices are optimized for wider input bandwidths and shorter integration times (sampling periods) well below 20 µs. Conversely, their designs are not intended for integration times longer than a few milliseconds.

The maximum charge setting (full scale) is traditionally lower than the DDC family, on the order of 10 pC. But because they target lower signals, the sensitivity/noise floor is also better than DDCs, with typical numbers around 0.1 fC_{rms} (600 electrons). For small-charge ranges, an AFE will offer less than half the noise compared to a DDC.

The tighter dynamic range of the device (a lower noise floor but an even lower full scale) does not require the 20-plus bit converter used with DDC devices, and as such, the AFE devices support only 16-bit conversion.

Besides the increased sensitivity, one advantage is that AFE devices, unlike DDCs, can work with currents flowing either into or out of the device input without the need for external components, and even acquire bipolar signals.

The input voltage for the AFE is not zero but a different voltage level (for example, 1.68 V for the AFE0064 depending on the selected device). You must consider the voltage level when biasing the sensor. For instance, to read a photodiode while trying to keep the dark current close to zero, you would usually use a zero bias (no bias applied across the photodiode). Thus, if one terminal of the photodiode connects to the AFE input, the other terminal should be biased to the same non-zero voltage.

To explain the architecture of every channel further (see **Figure 2**), every sample is actually divided into two phases controlled by external signals: a reset/offset sample phase and a signal sample phase. These are the traditional phases of a correlated double sampler (CDS). In panel applications, during the reset/offset phase, the input of the device connects to the external world (usually a data line) but without the signal being present. The intention is to sample or baseline any existing offset or low-frequency noise (flicker) from external or internal sources. One-half of the CDS stores the resulting integration. In the signal sample phase, the external signal connects to the input; the other half of the CDS stores that integration. The sources of offset will still be present during this time; subtracting the two samples in the CDS will remove the offsets, leaving only the signal of interest.

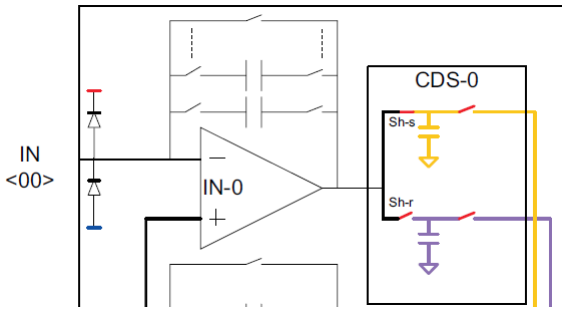

Figure 2. *The X-ray AFE input integrator architecture*

When applying such a scheme to the sampling of continuous current, the reset phase will also integrate a portion of the signal that the circuit will later subtract from the integration obtained during the signal sample phase. If the signal is constant during these two phases, the effect is an easily correctable gain error. But if the signal varies, you should take the potential induced errors into account.

If it is possible to synchronize the signal generation with CDS sampling operation, there will not be a gain error. For example, if it is possible to turn sensor illumination on and off synchronous to CDS operation, the photodiode current would be generated only during the signal sample phase, not during the reset/offset phase. The result would be no gain error, with the

additional advantage that any ambient light or offset would be sampled during the reset/offset phase and get rejected by the CDS.

The AFE0064 comes in a more traditional thin quad flat package (TQFP), while newer versions are available as chip-on-flex (COF) packages, driven by the flat-panel-detector application. This may present some complications versus the more common assembly methods.

Final comparison

Table 2 summarizes the differences between the two device families.

	DDC Family	AFE Family
Number of channels	2, 4, 8, 16, 32, 64, 128, 256	64, 256
Current direction	Into the device	Into or out of the device
Bipolar signal integration	No	Yes
Input DC voltage	0 V	Non-zero (1.68 V for the AFE0064)
Package	TQFP, small-outline IC, BGA	TQFP, COF
Full-scale charge range	12.5 pC to 350 pC, 1 nC	≅0.5 pC to >10 pC
Maximum full-scale current	3 µA	0.5 µA
Input referred noise (charge)	0.2 fC_{rms} (1,250 electrons)	<0.096 fC_{rms} (600 electrons)
Input referred noise (current)	0.5 fA_{rms} (at 1 SPS)	<96 fA_{rms} (at 1 ms)
Maximum sampling rate	≅5 kSPS	>50 kSPS
Maximum integration time	1 s	1 ms

Table 2. *Differences between the DDC and AFE families*

Assume that you want to measure all of the charge produced within 100 ms by each of the 64 photodiodes in an array. Also assume that the maximum current is 1.2 nA. In this case, the maximum charge is 1.2 nA × 100 ms = 120 pC, which the DDC264 could handle in range 3 (150-pC full scale) in a single integration.

Looking at **Figure 3** and assuming a 24-pF parasitic detector capacitance, you would expect the noise to be about 0.9 fC_{rms}.

RANGE	C_{SENSOR}								
	0 pF	10 pF	30 pF	43 pF	57 pF	100 pF	270 pF	470 pF	1000 pF
ppm of FSR, rms									
Range 0: 12.5 pC	16	20	30	37	44	71	160	270	510
Range 1: 50 pC	6.4	7.4	10	12	14	21	45	74	130
Range 2: 100 pC	5.1	5.5	7.1	8	9.1	12	25	39	71
Range 3: 150 pC	4.8	5	6	6.5	7.2	9.6	17	27	49
fC, rms									
Range 0: 12.5 pC	0.2	0.25	0.38	0.46	0.55	0.89	2	3.38	6.38
Range 1: 50 pC	0.32	0.37	0.53	0.62	0.73	1.09	2.29	3.73	6.88
Range 2: 100 pC	0.51	0.55	0.71	0.8	0.91	1.28	2.5	3.97	7.16
Range 3: 150 pC	0.72	0.75	0.9	0.98	1.08	1.45	2.67	4.14	7.36
Electrons, rms									
Range 0: 12.5 pC	1250	1560	2340	2890	3430	5540	12480	21070	39790
Range 1: 50 pC	2010	2310	3340	3910	4570	6800	14200	23300	42900
Range 2: 100 pC	3220	3440	4450	5000	5680	7990	15600	24800	44700
Range 3: 150 pC	4530	4730	5610	6120	6770	9050	16700	25800	45900

(1) Noise in Table 1 is expressed in three different units for reader convenience. The first section lists noise in units of parts per million of full-scale range; the second section shows noise as an equivalent input charge (in fC); and the third section converts noise to electrons.

Figure 3. *Noise vs* C_{sensor}

There is an additional noise factor from the low-frequency noise on the device, which is more visible as the integration time increases (see **Figure 4**). Because of this effect, the noise will actually be close to 9 ppm of the full-scale range (150 pC), or 1.35 fC_{rms}.

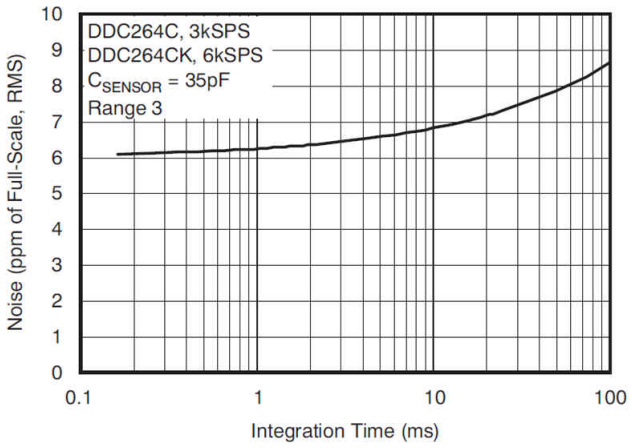

Figure 4. *Noise vs. integration time*

In comparison, the AFE0064 cannot handle the 100-ms interval with a single integration period; it would saturate. The solution is to integrate for shorter periods and add them together. There are many integration periods possible, but in this example we will skip the optimization exercise and choose to integrate for 5 ms, which would result in a maximum charge of 6 pC and hence select range 6 (7.2 pC). The noise for a single sample is then approximately 2,040 electrons (0.3 fC_{rms}); see **Figure 5**. The resulting noise after adding 20 consecutive samples for a 100-ms equivalent will be $\sqrt{20} \times 0.3\ fC_{rms} = 1.34\ fC_{rms}$, with a result very similar to the DDC.

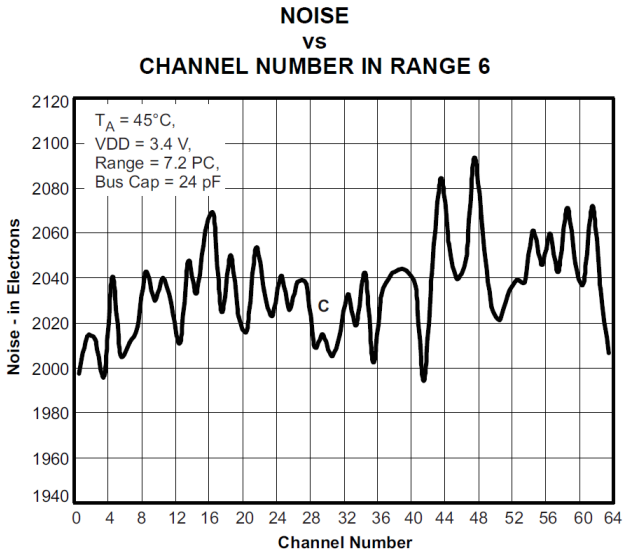

Figure 5. *Noise vs. channel number*

Conclusion

For applications where you can't sacrifice sensitivity and high sampling speeds, AFE devices are likely the best choice. Nevertheless, DDCs can improve sensitivity (beating the AFE devices in current terms) by measuring (integrating) over longer periods of time. DDC devices will also be the best choice in applications with a larger charge, although AFE devices can compensate for part of that by sampling faster; that is, dividing the same period in smaller (faster) samples and adding them in the end.

There will also be other nonperformance-related practical constraints that can force the choice one way or the other – like the fact that AFE devices are mostly available in COF packages, or that DDC struggle with currents flowing out of the device.

Related Websites

1. Bartolome, Eduardo. **Introduction to Medical Imaging**. (Nov. 17, 2013). Accessed Nov. 24, 2021 [Online Video].
2. Todsen, Jim. 1998. **Using External Integration Capacitors on the DDC112**. Burr-Brown application bulletin, Texas Instruments literature No. SBAA027, September 1998.
3. Todsen, Jim. 1999. **Creating a Bipolar Input Range for the DDC112**. Burr-Brown application bulletin, Texas Instruments literature No. SBAA034, October 1999.

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