The art of passive matching a high-speed ADC analog-input front end

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Introduction

Understanding the mechanisms involved in designing high-speed analog-to-digital converter (ADC) front ends is sometimes like an art of its own. Simply placing a balun down and drawing two trace lines from the balun's secondary outputs to the ADC's inputs is not recommended for any high-speed analog receiver front end design. Baluns are notorious for being parasitic-sensitive on bandwidth, along with other nuisances. In this article, we'll show you how to get the most out of your passive analog-input design using a balun. The added benefit is that you don't need a costly balun nor a costly attenuation pad in order to achieve the bandwidth you want.

The art of choosing the right balun or transformer

Let's begin with the assumption that you don't need to DC-couple; that is, sample the DC frequency bin. Because a balun does not require an additional power supply, the advantages of using one include lower overall power consumption and smaller board space requirements. Additionally, with no extra power supply to contend with, a balun won't add noise to the overall radio-frequency (RF) signal chain that leads up to the ADC itself, which means that no degradation in the signal-to-noise ratio (SNR) or noise spectral density will occur.

Figure 1 shows two different baluns used in the same application with TI's 16-bit, dual-channel **ADC3669** ADC. Even though both baluns are rated for the same bandwidth, they will ultimately respond differently given the combination of the ADC's varying input impedance from the ADC's internal sample network, as well as the printed circuit board (PCB) trace parasitics itself. Notice that with no "match" applied with either balun, the bandwidth falls quite rapidly [1].

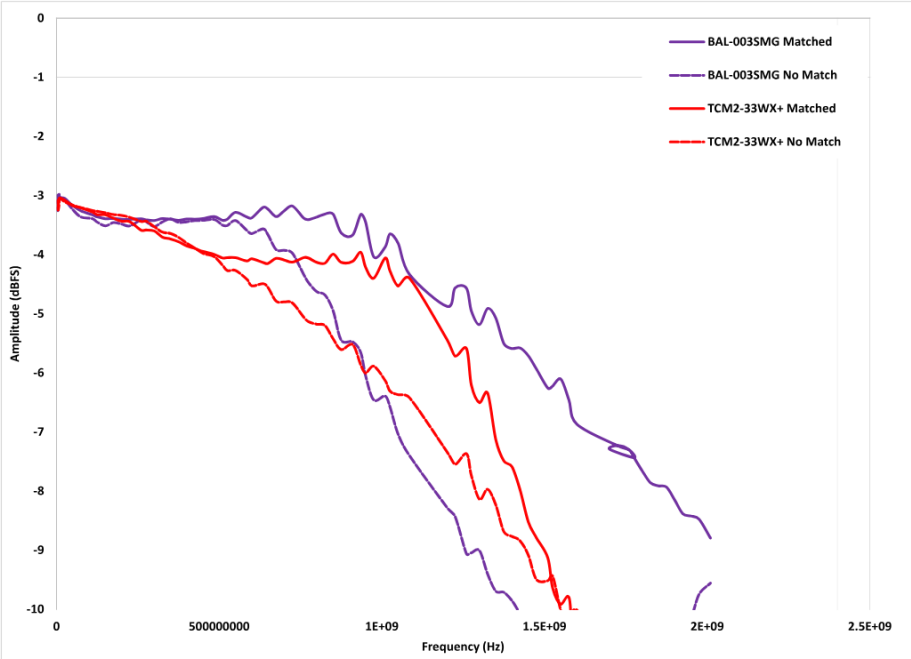

Figure 1. *ADC3669 and balun bandwidth comparison: match (solid lines) vs. no match (dashed lines).*

Take a close look at the balun's PCB footprint and layout recommendation in the data sheet. We recommend following these recommendations exactly, or else the balun will respond differently. The balun was characterized using this footprint both for data-sheet collection and measuring its S-parameters, and will only perform up to specifications under these circumstances.

To understand the balun's phase imbalance over your specific bandwidth, note that the poorer the balun's inherent phase imbalance, the worse even-order distortion (second harmonic distortion [HD2]) the ADC will manifest. If HD2 is important to your frequency planning application, we recommend picking a balun with good phase imbalance. There is really no good guidance on this, as each ADC can also have its own sensitivity to phase differences across its usable frequency range. Typically, choosing a balun with ≤5 degrees of phase imbalance over your application's operating bandwidth would be a good start. This amount of phase imbalance would add little to the aggregate even-order distortion already existing in your RF signal-chain lineup [2].

Figure 2 shows the difference between the same two matched baluns scenarios, and its impact on even-order distortion using the **ADC3669**. Notice that the third harmonic distortion (HD3) is relatively the same across frequency and has no significant differences.

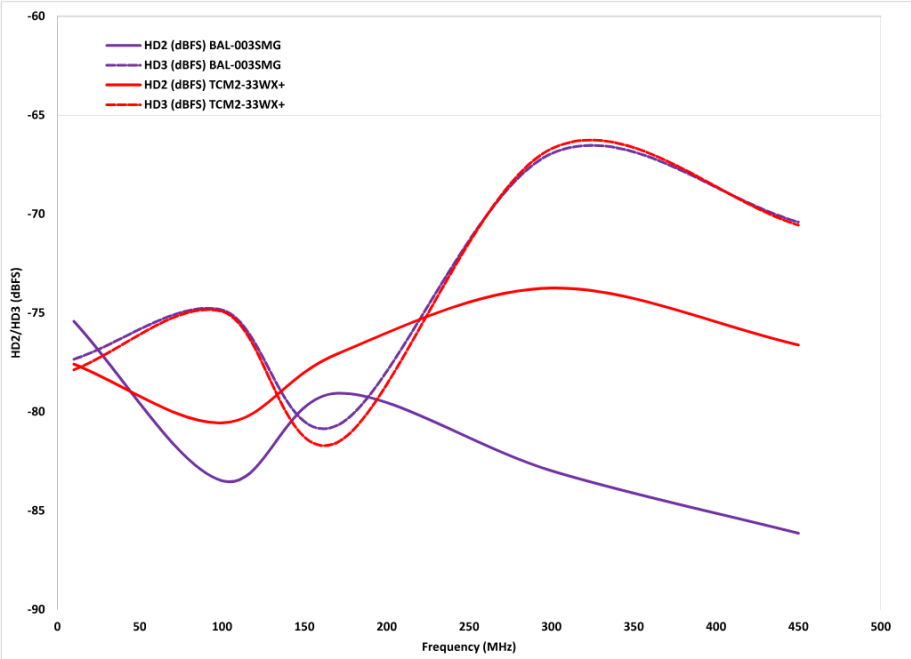

Figure 2. *ADC3669 HD2 and HD3 comparison between two baluns: high cost vs. lower cost.*

The art of choosing the right balun matching network

Over the years, there have been many attempts to simulate and perfect the balun match. After weeks to months of simulation and trying to understand some level of PCB parasitics, it's still possible that the match will not work out in your favor when fabricating the PCB design. We suggest starting the design process differently, using the topology shown in **Figure 3**.

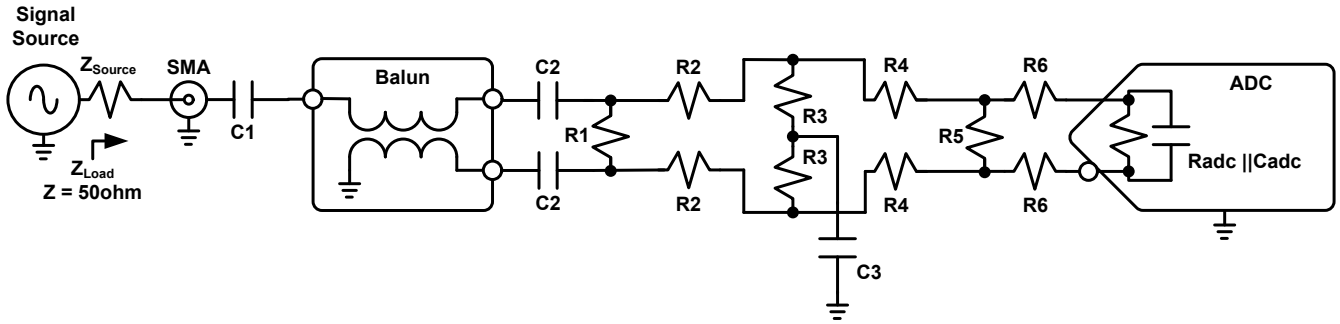

Figure 3. *Generalized passive network component placeholders.*

If you're wondering whether all of this effort and trade-offs are actually worth it, we suggest referring back to **Figure 1**.

Let's describe each component so that you know its need or function within the input matching network to the ADC:

- C1, C2. Typically 0.1µF, these components block DC from being fed into the balun or transformer. Some balun designs lead to ground, DC, or both, and may aggravate the balun's function, leading to poor performance.
- R1. This component enables back termination near the outputs of the balun after the DC blocking capacitors. If your trace lengths are long enough, you may need this component. Assuming that no perfect match across the band of interest is achievable, you may need to back terminate in order to handle any standing waves that accumulate as the imperfect match rolls back and forth across your frequency range.
- R2, R3, R4. These components enable you to employ various matching techniques and can take the form of several combinations in order to solve a balun and ADC matching conundrum. For the widest band matches, R2, R3 and R4 are generally configured as a matching pad, which helps dissolve the standing waves between the balun and ADC and provides a "stiff" 50Ω impedance that both the balun and the ADC need. Though these components are represented as resistors, they can take the form of capacitors or inductors as well.
- C3. This capacitor, typically 0.1µF, ties the center point of the R3s together and enables an AC current path. Adding C3 is also a good idea, because when over-ranging the ADC's input full scale, C3 allows this AC current to go somewhere. C3 could also be located at R5 instead.
- R5. This component allows back termination on the opposite side near the ADC's inputs, and is not always necessary. R5 provides the same function as R1, but from the opposite perspective in order to help resolve standing waves that may accumulate. Typically, R1 or R5 are required when trace connections are ≥300mils in length.
- R6. This is a kickback component, typically in the form of resistors, but in some cases inductors or low-Q ferrite beads that can help snub any residual charge kickback that comes back onto the analog input network from the internal sampling circuit in the ADC. These component placeholders are essential when using unbuffered ADCs.

Again, be wary if you just plan to run two traces from the output of the balun to the inputs of the ADC. Even if you collect S-parameters, simulate and prove the design to your colleagues, this methodology could prove to be costly unless you have previous experience with the balun and ADC combo.

Art using the ADC3669

Our example uses the 16-bit, dual-channel **ADC3669** ADC for a wideband front end match design of 1.5GHz of analog sampling bandwidth. The example also uses the **TCM2-33WX+** balun from Mini-Circuits, which has 3GHz of bandwidth and low insertion loss compared to higher-cost baluns that are easier to match with. This balun also has very good phase imbalance, <5degrees, when compared to other lower-cost baluns across the same frequency range.

Using the generalized circuit in **Figure 3**, the components needed are not purely resistive to define the match. In this case, we will use a resistor (R), internal parasitic capacitance (C) and inductor (L) (R2, R3 and R6) approach; see **Figure 4**.

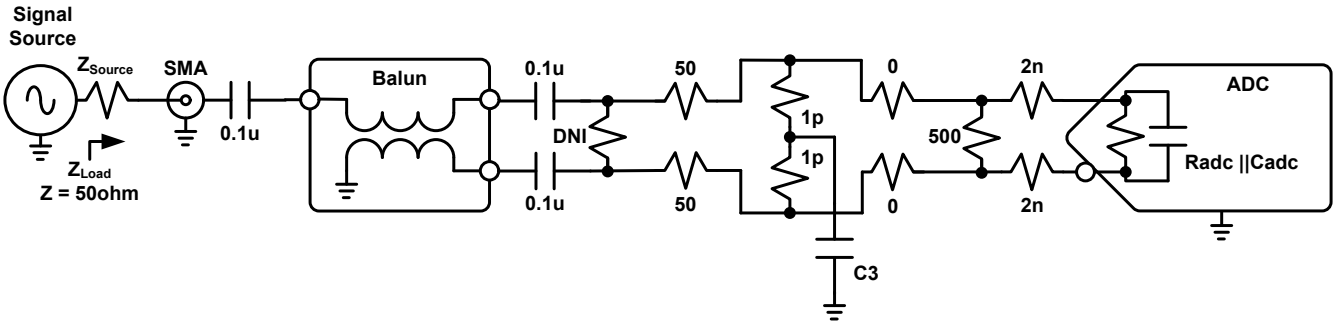

Figure 4. *Finalized passive network match.*

PCB parasitics will still be an issue, necessitating that you test a few different iterations on your board.

Get both sets of S-parameters (if available) for the balun and ADC and use your favorite simulation software. Use the matching network format given in **Figure 3** and one of these two approaches for R2, R3 and R4:

- The attenuation pad approach (approximately 8.6Ω, 140Ω and 8.6Ω for R2, R3 and R4, respectively) will give you a 3dB pad. To learn more about this approach, see the Electronic Products article, "Unraveling the Full-Scale Mysteries of Your RF Converter's Analog Inputs."
- The R, C and L approach for R2, R3 and R4, respectively, helps resonate away the ADC's C using L as the last component. This approach will flatten out the bandwidth, allowing the balun to perform at its rated bandwidth. This approach does take a bit of iteration, however.

The goal here is to not use a lossy attenuation pad. Therefore, to give more context to the R, C and L approach, see **Figure 5**, **Figure 6** and **Figure 7** as varying the L, C and R, respectively, in the network (see **Figure 4**) and its role in defining the ultimate bandwidth and network match.

Figure 5 shows how changing the value of L around influences the bandwidth while keeping all other component values the same. Notice that as L increases in value the bandwidth is slowly reduced. This means that the L value is having an adverse reactive effect on the C of the ADC.

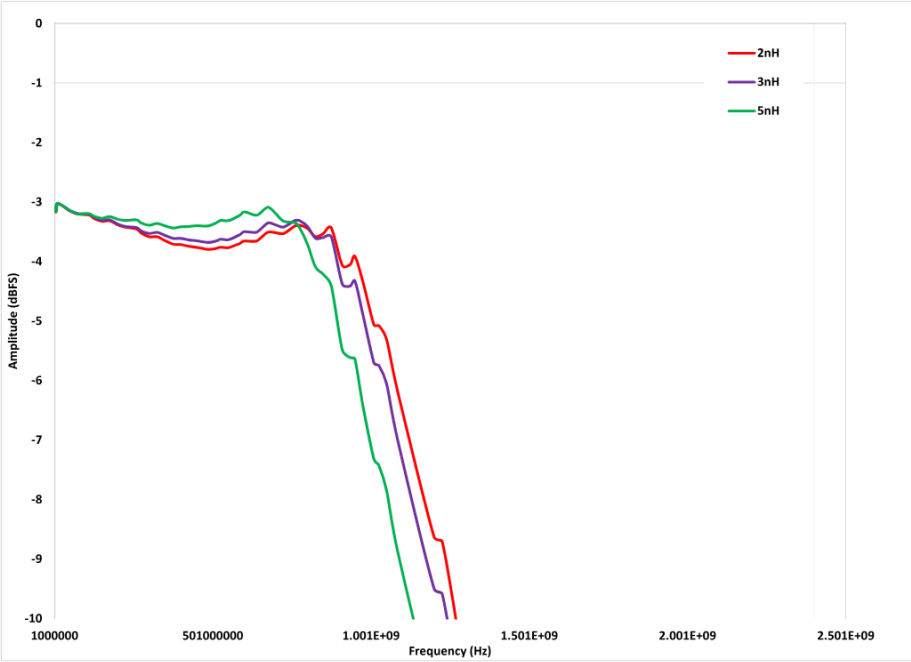

Figure 5. *Passband flatness response with various L values at R4.*

Figure 6 shows how moving the value of C around influences the bandwidth while keeping all other component values the same. Notice that as the value of C reduces, the bandwidth is slowly improving – at the cost of bandwidth flatness. This means that the C value is having a reactive effect on the balun's return loss over frequency. These capacitors help preserve the balun's bandwidth vs. frequency.

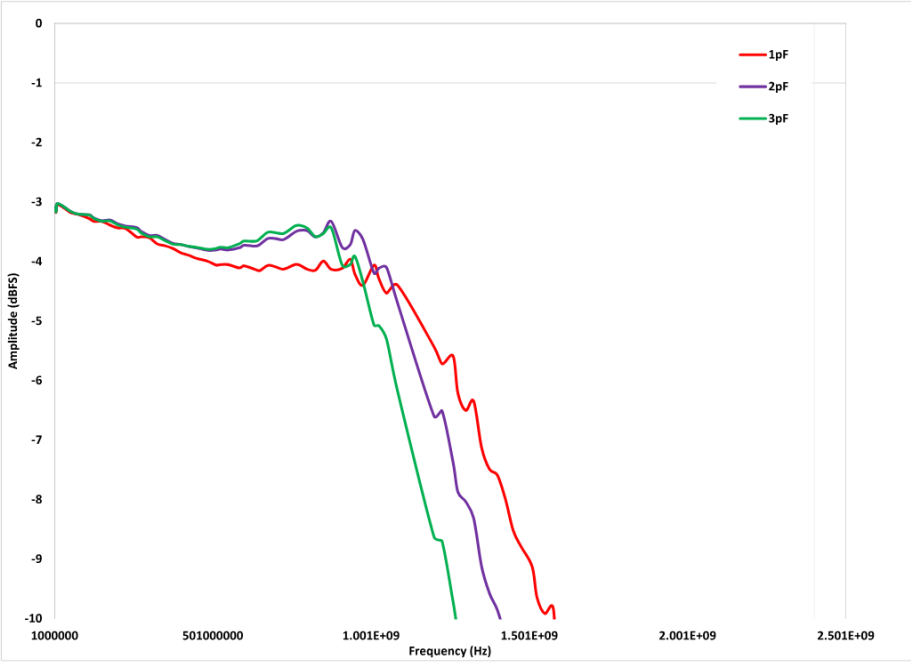

Figure 6. *Passband flatness response with various C values at R3.*

Figure 7 shows how moving the value of R around influences the bandwidth while keeping all other component values the same. Notice that as R increases in value, the bandwidth is slowly improving – at the cost of flatness or peaking in the bandwidth response. The effect of R's value is almost the same as the effect of L, therefore preserving the impedance requirements that both the balun and ADC should have in conjunction with each other.

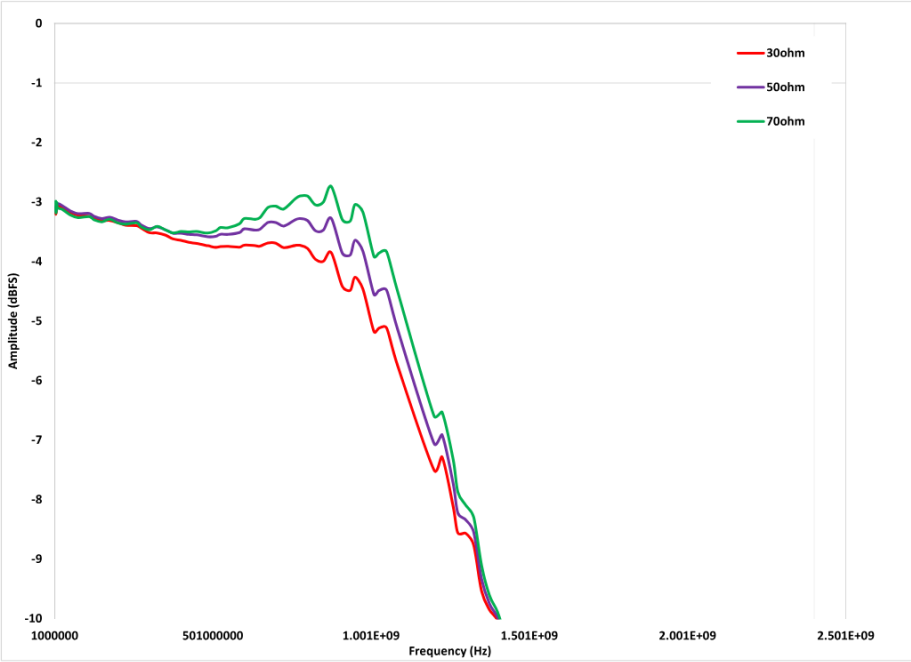

Figure 7. *Passband flatness response with various R values at R2.*

Simulating the R, C and L approach would give you a good starting point, using the "tune" feature in simulation software, and enables you to see the roles that each component plays in the network match. Settling on some good starting values can help define which direction to go when iterating and perfecting the match as needed for your application.

During the matching design effort, completing an AC performance sweep across the application bandwidth of the converter will give you insight as to how the performance is coming along dynamically, and ensure that nothing has gone wrong with the ADC.

Figure 8 illustrates the AC performance (SNR and spurious-free dynamic range [SFDR]) measured across the bandwidth of the **ADC3669**, using the method we've described to match the input network to 1.5GHz.

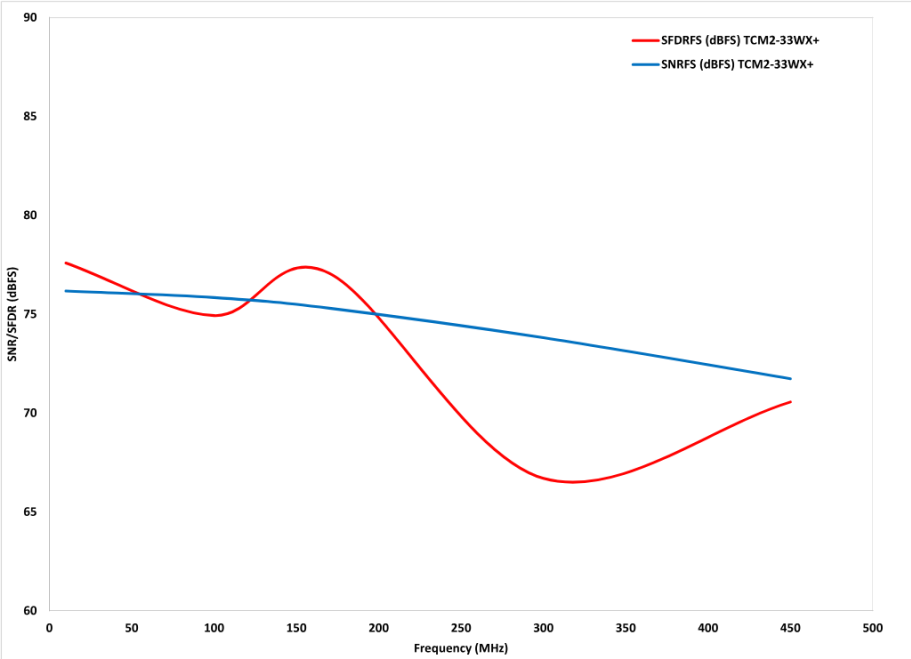

Figure 8. *Final matched network AC performance (SNR/SFDR) vs. frequency.*

Conclusion

Here are the basic steps when approaching a balun and ADC matching network design in the gigahertz region, in order to prevent your next matching effort from being bandwidth-hampered:

- Choose a balun or transformer that has some bandwidth overage for your particular application.
- If HD2 is important to your frequency application, choose a balun with ≤5 degrees of phase imbalance.
- A simplified input network can provide the initial placeholders required in most matching efforts when using a balun or amplifier and ADC.
- You may not need every component listed, but initially they can be beneficial, as it is not possible to capture all board layout and PCB parasitics in simulation.
- Understand the trade-offs that can affect your bandwidth performance. Some of these trade-offs can affect the linearity performance of the ADC.

References

1. Reeder, Rob. 2022. "**A Close Look at Active vs. Passive RF Converter Front Ends**." Planet Analog, Jan. 24, 2022.
2. Reeder, Rob. 2022. "**Evaluating high-speed RF converter front-end architectures**." Planet Analog, April 7, 2022

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