Simplifying Power Architectures With Low-Noise Power Devices

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Reducing inherent and system noise is critical to enabling high-precision signal chains in demanding electronic systems. Innovations in low-noise power devices are helping to mitigate system noise and improve accuracy and precision.

At a glance

1 **Defining noise and precision in a power architecture**

Noise is often application-specific, but in the context of this paper, noise is any unwanted signal that originates from thermal noise, 1/f noise and low-frequency oscillations, up to approximately 100 kHz.

2 **Innovations in low-noise and low-power voltage references**

Reducing noise in power architectures helps increase an analog-to-digital converter's resolution and precision but creates design challenges with power consumption, printed circuit board (PCB) size, manufacturing flow and cost.

3 **Innovations in precision battery monitoring**

Having creative solutions in silicon technologies enables designers to optimize their power architectures and battery systems.

Achieving the lowest noise in a signal chain is vital as industry trends push the boundaries of resolution and precision. And when pushing these boundaries, it's important to consider not just the noise of signal-chain components such as analog-to-digital converters (ADCs) and amplifiers, but also power products such as switching and low-dropout regulators (LDOs). Advances in silicon technologies have reduced the trade-offs when attempting to achieve low noise and high precision in power topologies.

Recent trends in 24-bit delta-sigma ADCs have increased sampling speeds and lowered power consumption. New low-noise power supplies and low-noise voltage references can take advantage of these trends and help ADCs achieve high-resolution measurements in low-power applications.

To achieve the lowest noise, let's review the sources of noise in the signal chain and power architecture. **Figure 1** shows a typical signal-chain application centered around an ADC that requires an external voltage reference, clock and signal-conditioning circuit. Every component in **Figure 1** contributes to system noise and requires optimization.

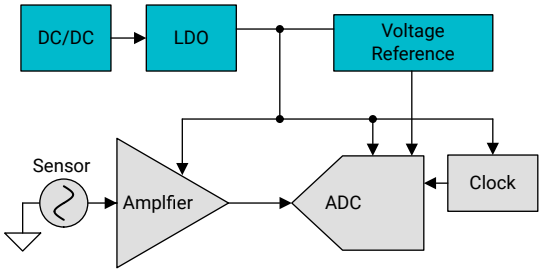


Figure 1. *Common signal-chain power architecture.*

Noise and ADCs

Noise in an ADC can cause errors in precise voltage measurements. You must consider the total contribution of noise in the signal chain from internal and external sources. Total noise is often a combination of ADC thermal noise, ADC-quantization noise, amplifier noise, voltage-reference noise and power-supply noise.

Equation 1 depicts the total referred noise at the input of the ADC (at full-scale voltage) as it measures the sensor based on **Figure 1**. The main design challenge is to optimize all noise sources to achieve the noise target that the application requires. In **Equation 1**, the ADC's power-supply rejection ratio (PSRR) reduces the power-supply noise, which is plotted out to 1 MHz:

$$\text{ADC Total Noise} = \sqrt{\text{ADC Thermal Noise}^2 + \text{ADC Quantization Noise}^2 + \left(\text{Power Supply Noise} \times 10^{\frac{\text{PSRR}}{20}}\right)^2 + \text{Voltage Reference Noise}^2} \quad (1)$$

Given the existence of uncorrelated noise sources, the total noise is the root sum square of all sources, which heavily favors the largest noise source. One noisy component can heavily skew the measurement. For example, if a voltage reference contributes more noise than an ADC and power supply, reducing noise on the voltage reference will be the best way to lower the system noise, as shown in **Figure 2** and **Figure 3**. In addition, ADC noise types vary with resolution: quantization noise is significant for a 16-bit ADC, but you can ignore it for a 24-bit ADC.

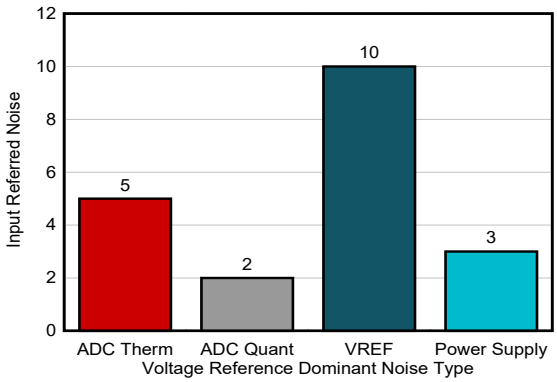


Figure 2. *Voltage reference dominant noise.*

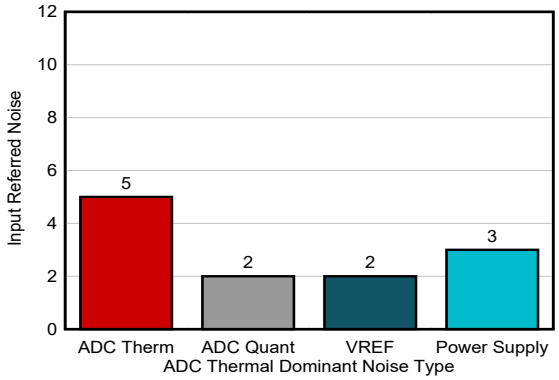


Figure 3. *ADC thermal dominant noise.*

Defining noise and precision in a power architecture

Power-supply noise is random and occurs in all semiconductor power devices and power topologies. The focus of this white paper is signals below 100 kHz, as signals above this are often attributable to switching ripple or electromagnetic interference (EMI). You can also further separate noise into low-frequency noise (0.1 Hz to 10 Hz) and high-frequency noise (100 Hz to 100 kHz), with differing requirements and design challenges, as shown in **Figure 4**.

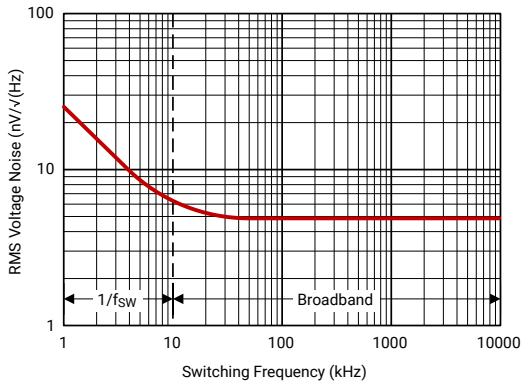


Figure 4. *Noise-frequency spectrum.*

Low-frequency noise is often specified as the peak-to-peak noise between 0.1 Hz and 10 Hz that a semiconductor device naturally produces given the combination of its silicon properties and design architecture. This low-frequency noise is often visible in an oscilloscope when zooming into a voltage rail at high resolution, as shown in **Figure 5**, and is often the cause of errors in precision DC measurements. ADC applications where low-frequency noise is a critical specification include battery measurements, energy metering, seismic measurements and even semiconductor test measurements.

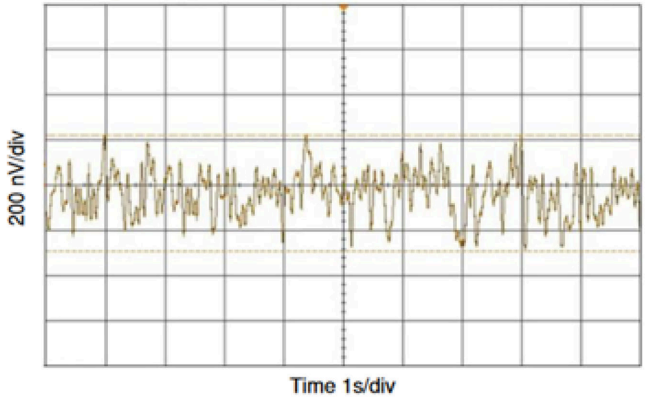


Figure 5. *Low-frequency noise on an oscilloscope.*

The alternative is high-frequency noise, which is in the band of 100 Hz to 100 kHz and can include white noise, switching noise and clock jitter, as shown in **Figure 6**. High-frequency noise sources can also come from the environment, through coupling from EMI. For example, an ADC can experience errors from a noisy power supply. EMI from the same noisy power supply can lead to increased clock jitter, which if excessive can degrade signal-to-noise performance.

It is becoming increasingly important to lower high-frequency noise caused by rising clock frequencies in digital circuits, which are more susceptible to jitter. ADC applications where high-frequency noise is a critical specification include power-line quality monitors, digital signal processing applications and radio-frequency (RF) communications equipment.

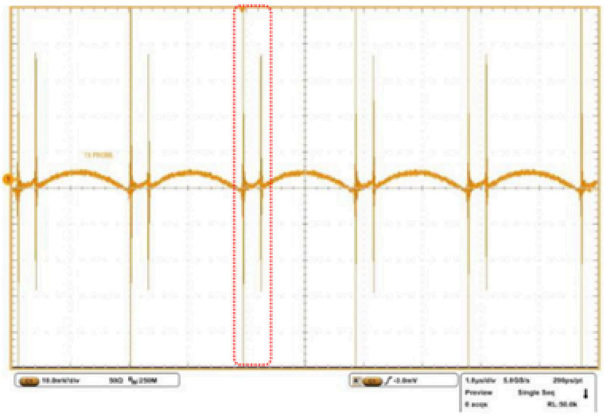


Figure 6. *Buck regulator switching noise.*

Innovations in low-noise and low-power voltage references

One way to lower noise is to increase the power in the system, but there is often a power budget, making it necessary to maximize noise performance with limited power. TI's low-noise voltage reference portfolio includes low-power options such as the REF33, REF34 and **REF35** families, which push the boundary between power and noise for low-power ADCs with high precision. A lower quiescent current (I_Q) voltage reference is beneficial for portable or edge applications, such as two-wire transmitters, that have a limited power budget.

Innovations in efficient band-gap circuits and output buffers have improved the power-to-noise ratio of voltage references. The REF33, REF34 and **REF35** are staple devices in TI's voltage reference portfolio for low

noise and low power. **Figure 7** compares their noise and power and highlights the innovation of the **REF35**.

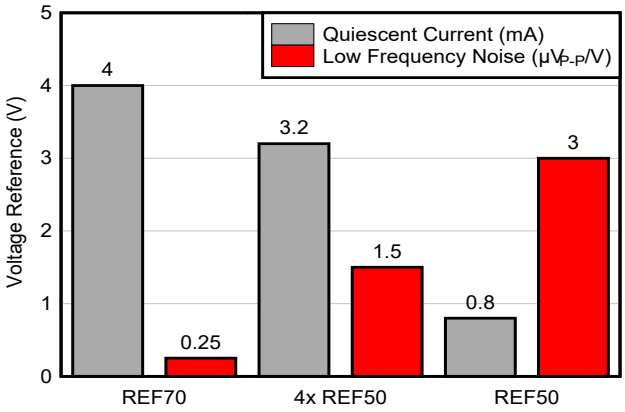


Figure 7. *Voltage reference power and noise.*

One common application for low noise is portable medical equipment such as portable electrocardiogram machines. The **ADS124S08** family of 24-bit ADCs has power consumption as low as 280 µA to minimize power draw in field instruments and edge devices that have limited power budgets. **Table 1** compares the **REF35** with the internal ADS124S08 voltage reference and highlights the improved accuracy with I_Q. The REF35's low noise and high accuracy improves both quantization and gain errors while lowering system power. The benefit of a flexible voltage reference voltage enables further optimization for maximizing the full-scale range of the ADS124S08.

Device	REF35	ADS124S08 internal voltage reference
Voltage level	1.25 V to 5 V	2.5 V
Low-frequency noise	8.5 μV_{PP}	9 μV_{PP}
I_Q	0.65 µA	280 µA

Table 1. *An external voltage reference vs. an internal voltage reference.*

The REF35 also pairs with the **ADS127L11**, which is an ADC focused on DC precision with low power consumption. The **REF35** offers a 10x reduction in supply current compared to the REF34 which makes it a stronger pairing with the ADS127L11 in low-speed mode. This pairing enables the ADS127L11 to achieve accuracy in power quality analyzer systems that require high precision, or machine vibration systems that need low power in order to balance solution size, resolution and bandwidth.

Innovations in ultra-low-noise voltage references

High-resolution ADCs are more sensitive to voltage reference noise, which directly impacts voltage measurements because of their direct connection to data-conversion circuitry. Ultra-low-noise voltage references help high-resolution ADCs reach their full resolution potential. The **REF70** has ultra-low 1/f noise that attaches with products that require ultra-low noise such as high-resolution ADCs or a multichannel analog front end such as the **AFE2256**. Adding low-pass filters on the output of the voltage reference lowers broadband noise and thus lowers system noise, as shown in **Figure 8**.

When designing a low-pass filter, it is important to ensure that the output impedance does not degrade AC performance. This can occur in resistor-capacitor low-pass filters where a large series resistance affects the load transients caused by output current fluctuations. Choose a low-pass filter bandwidth cutoff frequency under 10 Hz to limit the impact of broadband noise.

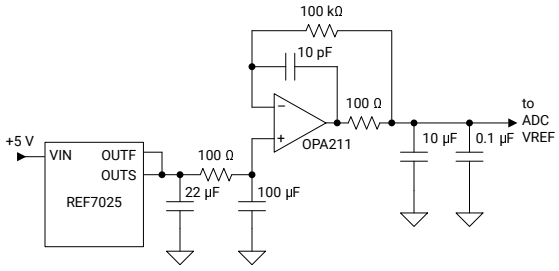


Figure 8. *REF7025 application with an external low-pass filter.*

Improving noise and thermal performance with simplified power architectures

The traditional setup for powering a clock, data converter or amplifier is to use a DC/DC converter (or module), followed by an LDO, followed by a ferrite-bead filter, as shown in **Figure 9**. This design approach minimizes both noise and ripple from the power supply and

works well for load currents below approximately 2 A. As loads increase, however, power losses in the LDO introduce issues in efficiency and thermal management; for example, a post-regulation LDO can add 1.5 W of power loss in a typical analog front-end application.

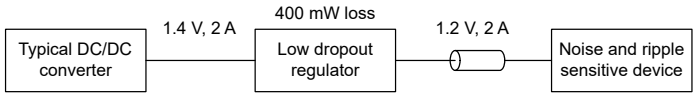


Figure 9. *A typical low-noise architecture using a DC/DC converter, LDO and ferrite-bead filter.*

The benefits of an LDO in a typical power architecture are to provide an accurate voltage rail while lowering switching noise in the high-frequency noise region with a high PSRR. The trade-off of using an LDO is an increase in thermals and power consumption. An effective way to ensure low noise while controlling power losses is to eliminate the LDO from the design altogether and use a low-noise DC/DC buck converter or module, as shown in **Figure 10**. This LDO-less design lowers power losses and improves thermals while achieving low noise.

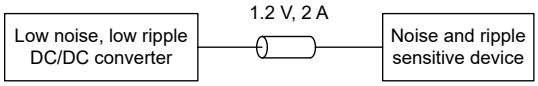


Figure 10. *Using a low-noise buck converter without an LDO.*

The **TPS62912** and **TPS62913** family of low-noise buck converters, as well as the **TPSM82912** and **TPSM82913** modules, implement a noise-reduction/soft-start pin for connecting a capacitor, forming a low-pass resistor-capacitor filter using the integrated R_f and externally connected$C_{NR/SS}$, as shown in **Figure 11**. This implementation essentially mimics the behavior of the band-gap low-pass filter in an LDO, which allows for an output-voltage ripple below 10 μV_{RMS}. The TPS62913 can also achieve a low noise floor in the high-frequency region that is absent of the typical switching noise by taking advantage of the 2.2-MHz switching frequency and optional second-stage ferrite-bead inductor-capacitor filter.

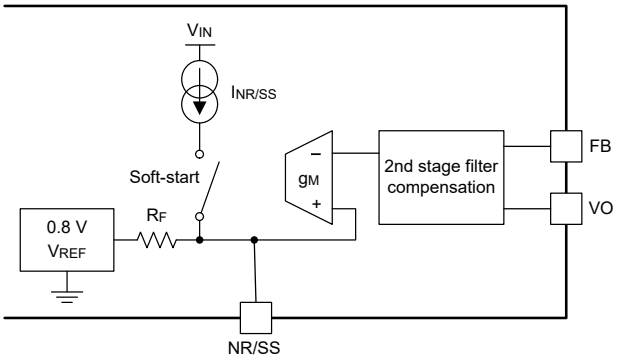


Figure 11. *Low-noise buck converter block diagram with band-gap noise filtering.*

The **ADC12DJ5200RF** is an RF-sampling ADC that samples from DC to 10 GHz with 4 W of power consumption. The PSRR attenuates any power-supply ripple and noise, but any residual ripple and noise will appear on the ADC output spectrum, which causes an error. The ADC12DJ5200RF has more sensitive power-supply requirements on the analog voltage rails, and therefore requires low noise. Using the TPS62912 for low-noise and high-power analog rails enables a simplified and efficient power architecture, while minimizing power losses compared to a DC/DC-plus-LDO combination.

High-current low noise with LDO supply rails

The biggest intrinsic noise source for an LDO is its internal voltage reference. In order to reduce noise and improve overall system performance, a variety of LDOs in the TI portfolio have incorporated a noise-reduction feature with a NR pin. Adding a capacitor ($C_{NR/SS}$) to the NR pin creates a resistor-capacitor filter with internal resistance at the V_{REF} node, as shown in **Figure 12**.

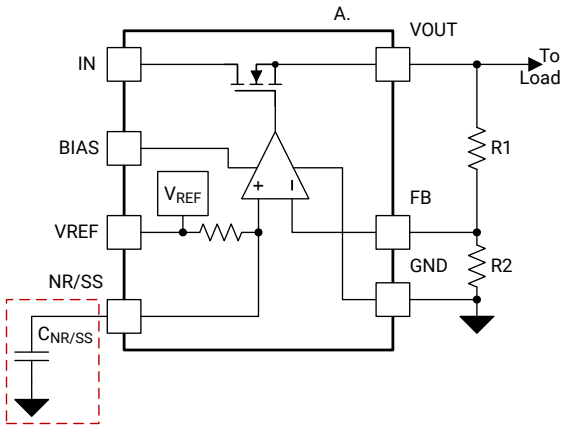
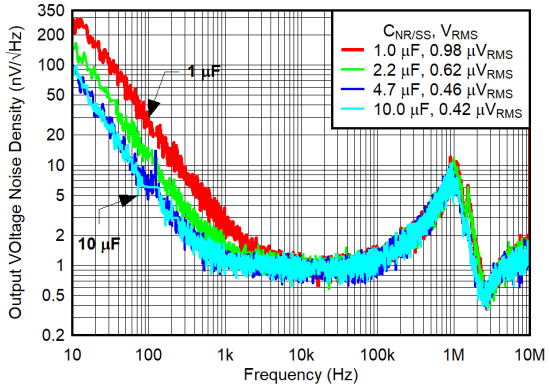


Figure 12. *N-channel metal-oxide semiconductor LDO with an NR/SS pin.*

A. $$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Newer LDOs implement a highly accurate, high-precision and low-noise current source, followed by an error amplifier. Implementing a unity-gain configuration also ensures low noise over the entire output range. A great example of one of these high-accuracy low-noise LDOs is the **TPS7A94**, which can achieve 0.46 μV_{RMS} over a 10-Hz to 100-kHz bandwidth. **Figure 13** shows the output noise density and the impact of increasing $C_{NR/SS}$ from 1 µF to 10 µF.



V_{OUT} = 3.3 V

$C_{IN} = C_{OUT}$ = 10 µF

I_{OUT} = 500 mA

10 Hz ≤ f_{SW} ≤100 kHz

Figure 13. *Output noise vs. $C_{NR/SS}$ of the TPS7A94.*

The combination of features that the TPS7A94 possesses represents a new generation of low-noise LDOs capable of achieving excellent voltage accuracy and ultra-low noise, which is important when the TPS7A94 is the primary power supply for a high-resolution signal chain, since higher-resolution ADCs are more sensitive to noise. In a typical application, shown in **Figure 14**, the TPS7A94 is the main power supply for the ADC, operational amplifier, clock and external voltage reference, which are high-performance devices. The goal of this signal chain is to maximize the total harmonic distortion, signal-to-noise ratio and gain error of the ADS127L11 by using the ultra-low input current noise with the low 1/f noise of the TPH210 and REF70. The low noise and high PSRR of the TPS7A94 provide a clean supply line that limits any noise that could couple into the active circuitry of the TPS210, ADC127L11 and REF70 and degrade performance.

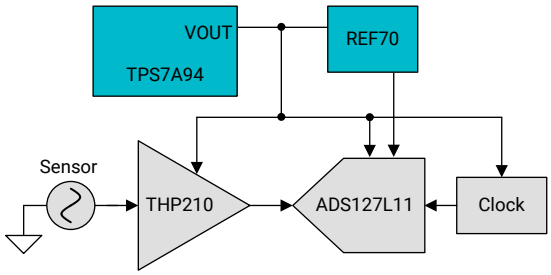


Figure 14. *TPS7A94 powering a signal chain.*

Innovations in precision battery monitoring

The **BQ79718-Q1** battery monitor for electric vehicles has an accuracy of 1 mV for measuring cell voltages. This higher accuracy and precision enable automotive original equipment manufacturers to deliver extended ranges without increasing the cost or capacity of the EV battery pack. As expected, many system and environmental factors contribute to inaccuracies in voltage measurements, including drift with temperature and lifetime, supply noise, and die stress induced from board flex.

TI has incorporated several technologies on a single die to reduce environmental effects and achieve higher-accuracy voltage measurements. For example:

- A buried Zener diode keeps the buried junction well below the surface and less susceptible to hot carriers. This diode enables a very stable voltage reference over an integrated circuit's (IC) temperature and lifetime.
- When soldering a battery monitor to a PCB, the flex of the PCB causes the die to bend very slightly, causing inaccuracies in voltage measurements. An integrated strain gauge measures this bend and corrects the voltage measurement.
- Integrated cell balancing field-effect transistors and power supplies cause the die to heat up, which results in voltage-measurement errors caused by temperature deviations. The **BQ79718-Q1** integrates temperature sensors so that the device can calibrate voltage measurements across temperature, ensuring the best accuracy.

Application-specific ICs such as the BQ79718 and **BQ79731-Q1** can help solve system-level issues in a single chip, enabling system designers to achieve the best performance without sacrificing time to market.

Conclusion

Traditional low-noise power architectures for low-noise ADCs and analog front ends often have challenges with power consumption and thermal performance. Designing with low-noise voltage references and power supplies enables designers to simplify power architectures and meet strict power budgets. Innovations in voltage references such as the REF35 are helping designers reach new levels of low noise and low power for edge devices. In noise-sensitive applications such as RF-sampling ADCs, low-noise switching regulators such as the TPS62913 allow for lower thermals compared to traditional switching regulators with an LDO.

Additional resources

- For more information about low noise and precision, visit ***Low noise & precision***.
- Read the technical article, ***How to enhance power and signal integrity with low-noise and low-ripple design techniques***.
- Download the e-books, ***Fundamentals of Precision ADC Noise Analysis*** and ***LDO Basics***.
- See the application notes, ***Powering Sensitive ADC Designs with the TPS62913 Low-Ripple and Low-Noise Buck Converter*** and ***Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter***.
- Read the white paper, ***How Innovation in Battery Management Systems is Increasing EV Adoption***.

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