AN-1799 LMV112 40 MHz Dual Clock Buffer Evaluation Board

1 General Description

This evaluation board is designed to aid in the characterization of Texas Instruments LMV112 40 MHz dual clock buffer. This board simplifies the connection and ease of use of any oscillating input device. Use this evaluation board as a guide for high frequency layout and as a tool to aid in device testing and characterization.

2 Basic Operation

The LMV112 contains two 40 MHz clock buffer amplifiers. These amplifiers are specially designed to minimize the effects of spurious signals from the digital chip to other analog or mixed-signal chip. The LMV112 also minimizes the influence of varying load resistance and capacitance to the oscillator and increases the drive capability. The buffers have a 120 V/µs internal slew rate at a supply current of only 2.5 mA for two enabled channels. Each amplifier in the LMV112 is capable of driving loads up to 20 pF. The input of each buffer is internally biased at 1 V. This allows AC coupling on the input. Each buffer offers an enable pin that can be used to disable the corresponding channel and to optimize consumption.

3 Channel Activation

Either channel can be independently enabled or shut down. The enable logic can be provided to the evaluation board by shunting a jumper on JR1 and JR2. For the required control logic, see Table 1.

Table 1. States of LMV112

Channel On	Enable1	Enable2
IN1 to OUT1	High	Don't Care
IN2 to OUT2	Don't Care	High

4 Layout Considerations

Careful consideration for circuitry design and PCB layout eliminates problems and optimizes the performance of the LMV112. It is best to have the same ground plane on the PCB for all decoupling and other ground connections.

To ensure a clean supply voltage it is best to place the decoupling capacitor close to the LMV112, between V_{DD} and V_{SS}. On the evaluation board this capacitor C1 is placed on the bottom side.

Another important issue is the value of the components, which also determines the sensitivity to disturbances. Resistor values have to be low enough to prevent noise coupling and large enough to avoid a significant increase in power consumption while loading inputs or outputs to heavily.

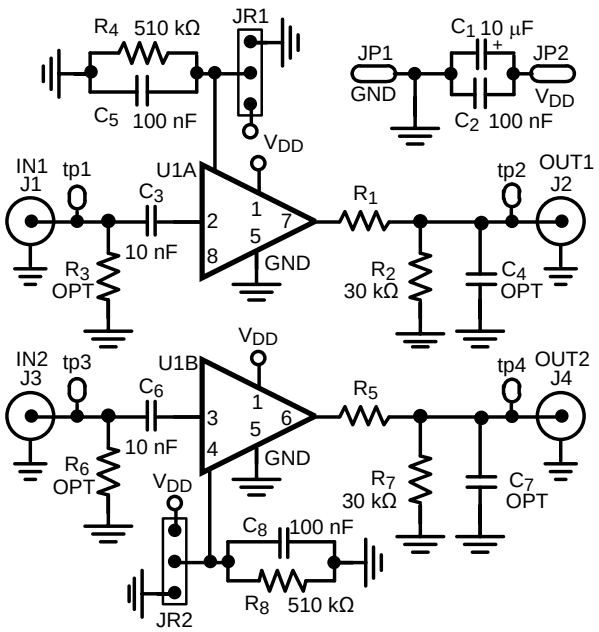

Figure 1. Schematic of the Evaluation Board

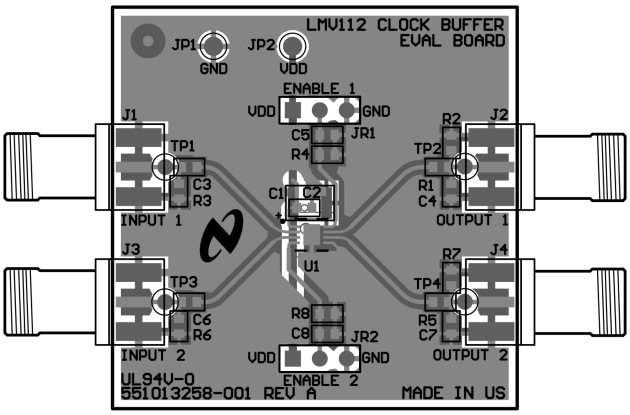

Figure 2. Layout of the Evaluation Board

The Bill of Material (BOM) of the evaluation board is given in Table 2.

Table 2. Bill of Materials

Designator	Description	Comment
R1, R5	0603 Resistor	0 Ω
R2, R7	0603 Resistor	30 kΩ
R3, R6	0603 Resistor	Optional
R4, R8	0603 Resistor	510 kΩ
C1	Case B, Tantalum Capacitor	10 µF 16V
C2, C5, C8	0603 Capacitor	100 nF
C3, C6	0603 Capacitor	10 nF
C4, C7	0603 Capacitor	Optional
JR1, JR2	Jumper	Header 1x3
J1, J2, J3, J4	Connector	SMA

Table 2. Bill of Materials (continued)

Designator	Description	Comment
JP1	Power Connector	pin 1.5mm, Black
JP2	Power Connector	pin 1.5mm, Red
U1	8-pin WSON	LMV112

5 Measurement Procedure

The performance of the LMV112 can be measured with the setup given in Figure 3.

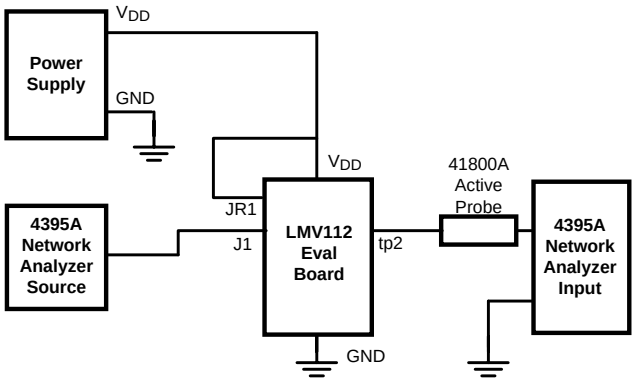

Figure 3. Measurement Setup

A supply voltage between 2.4 V to 5.0 V can be set by an external power supply connected to the JP2 (Red) V_{DD} pin and JP1 (Black) GND pin. In order to test its functionality, the buffer is tested by looking at the frequency response. Make sure to enable the buffer that has to be evaluated. The frequency response is tested by using a network analyzer (4395A). For small signal bandwidth evaluation the source input should be set at 0 dBm. Measure the output of the buffer with the probe directly connected to TP2 or TP4 to measure the highest available bandwidth.

6 Measurement Results

Figure 4 shows the frequency response of the LMV112 at 2.7 V and 5.0 V power supply and a source input of $V_{IN} = 0.63V_{PP}$ (0 dBm at 50 Ω).

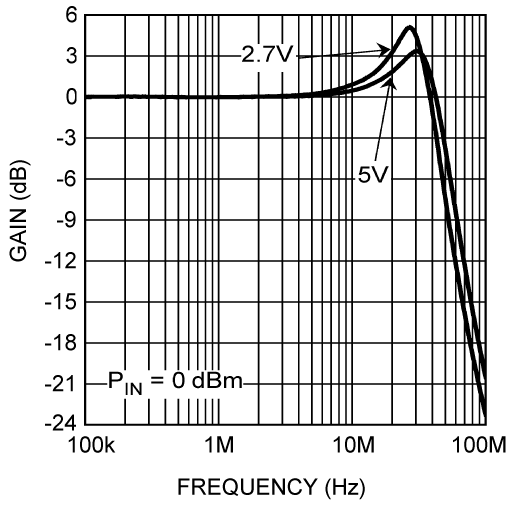

Figure 4. Frequency Response

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