AN-1964 LM49151 Demonstration Board and Software Guide

1 Introduction

To help you investigate and evaluate the LM49151's performance and capabilities, a fully populated demonstration board is available. This board is shown in Figure 1. Connected to an external power supply (2.7V to 5.5V), a signal source and an I^2C master controller, the LM49151 demonstration board easily demonstrates the amplifier's features. In addition, a GUI provides an easy evaluation of LM49151 I^2C settings and features.

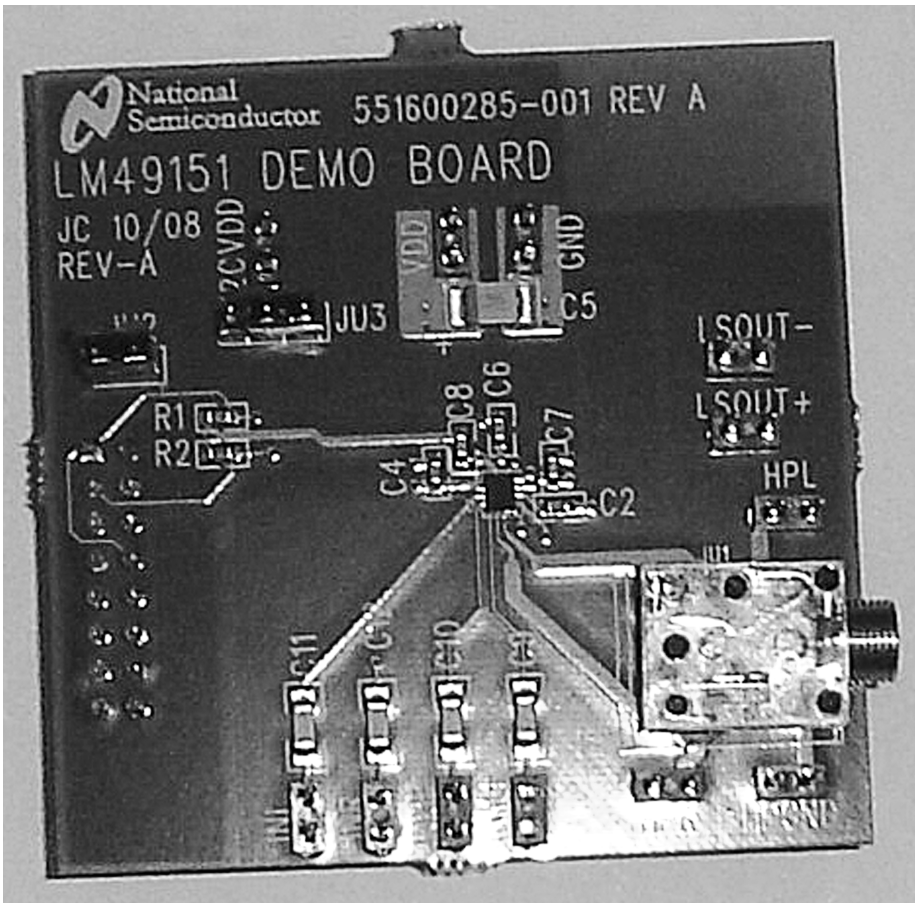

Figure 1. LM49151 Demonstration Board

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2 Quick Start Guide

1. Connect the I^2C signal generation USB Board X4 to J2 of the LM49151 demonstration board.
2. Install the LM49151 I2C interface software.
3. Apply a 2.7V to 5.5V power supply's positive output and its ground return to the "V_{DD}" and "GND" pins on the board, respectively.
4. Apply a mono differential or/and two single-ended signals to headers labeled INM+ and INM- or/and INL and INR, respectively.
5. Select output:
   (a) For class D speaker output, connect a speaker or load (≥4Ω) to LSOUT+ and LSOUT- header pins (a low pass filter may be required for measurements).
   (b) For headphone output, connect either through headphone output jack or HPR and HPL header pins.

Run the LM49151 I^2C interface software, select mode 1 for loudspeaker or mode 8 for headphone, set 0 dB volume gain, and Power on options from the GUI. See Section 9.

3 General Description

The LM49151 is a fully integrated audio subsystem designed for portable handheld applications such as cellular phones. The LM49151 combines a 1.25W mono E^2S class D amplifier, 125mW Class AB earpiece driver, 42mW/channel stereo ground referenced headphone drivers, volume control, input mixer/multiplexer, and speaker protection into a single device. The LM49151 class D speaker amplifier features a unique Automatic Level Control (ALC) that provides both an I2C programmable no-clip feature with Clip Controls and speaker protection. The E^2S (Enhanced Emission Suppression) class D amplifier features a patented, ultra low EMI PWM architecture that significantly reduces RF emissions while preserving audio quality and efficiency while delivering 1.25W into an 8Ω load with <1% THD+N with a 5V supply. The 42mW/channel headphone drivers feature a ground referenced architecture that creates a ground-referenced output from a single supply, eliminating the need for bulky and expensive DC-blocking capacitors, saving space and minimizing system cost. The LM49151 features separate volume controls for the loudspeaker and headphone inputs. Mode selection, shutdown control, and volume gains are controlled through an I^2C compatible interface. The LM49151's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

4 Operating Conditions

- Temperature Range $-40°C \le T_A \le +85°C$
- Supply Voltage (V_{DD}): $2.7V \le V_{DD} \le 5.5V$
- Supply Voltage (I^2CV_{DD}): $I^2CV_{DD} \le V_{DD}$

5 Board Features

The LM49151 demonstration board has all of the necessary connections, using 100 mil headers, to apply the power supply voltage and the audio input signals. The Class D amplifier's output is available on 100 mil headers. The Class AB headphone's amplified audio signal is available on both a stereo headphone jack and 100 mil headers. Also included with the demonstration board are an I^2C signal generation board and easy to use GUI interface software. With this board and the software, you can easily control the LM49151's different features of the device.

6 Schematic

Figure 2 shows the LM49151 demonstration board schematic. Refer to Table 1 for a list of connections and their functions.

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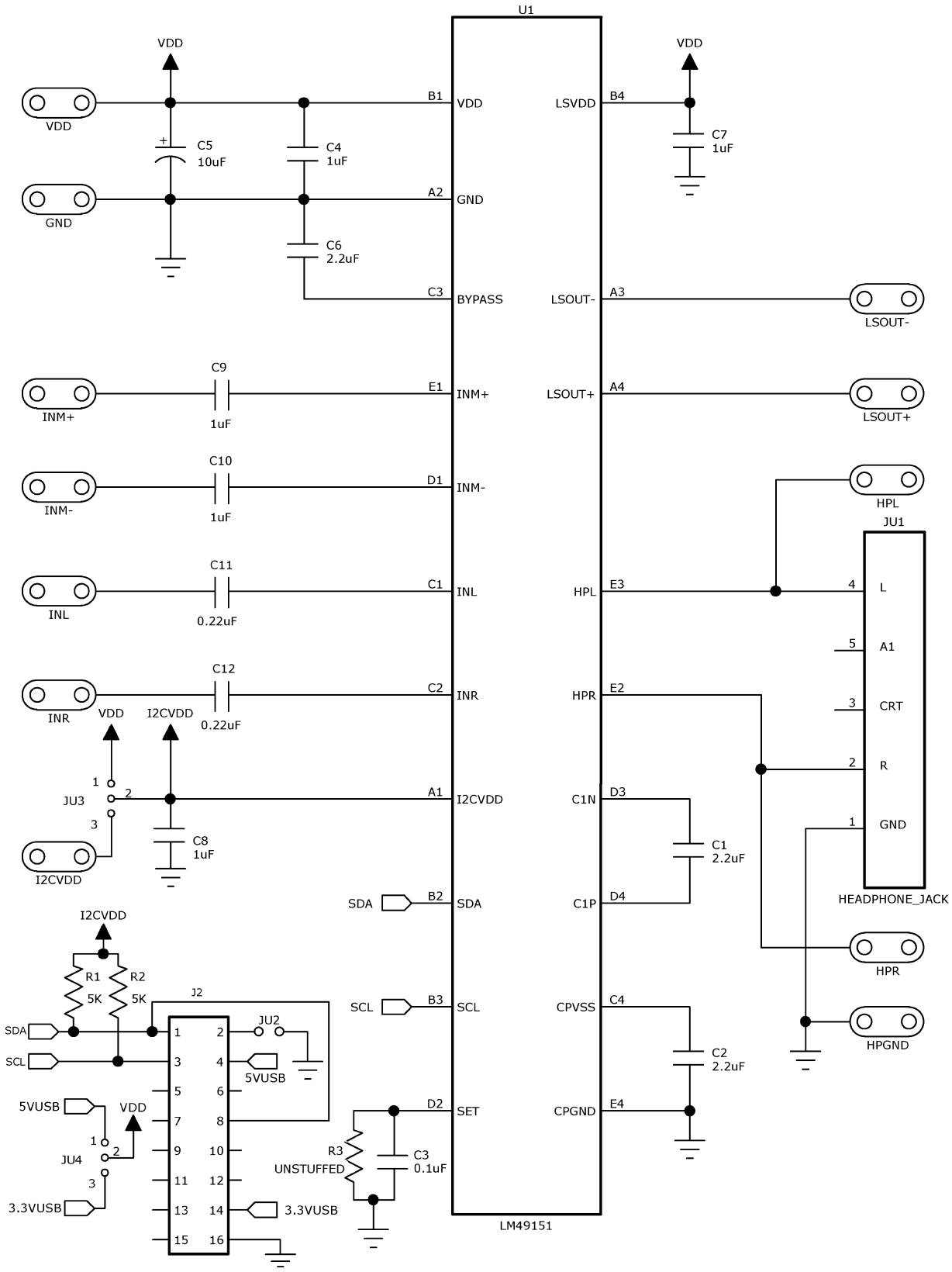

Figure 2. LM49151 Demonstration Board Schematic

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7 Connections

Connecting to the LM49151 demonstration board is accomplished through the 100mil headers on the LM49151 demonstration board. The functions of the different headers are detailed in Table 1.

Table 1. Connector and Header Functions

Designator	Function or Use
V_{DD} and GND	Power supply connection. Connect an external power supply's positive voltage source to V_{DD} and the supply's ground source GND header pins, respectively.
I^2CV_{DD}	If an external I^2C power supply voltage is used, connect this supply's positive voltage source to the I^2CV_{DD} header pin and the supply's ground source to the header pin labeled GND. If no external supply is used, leave this jumper's pins unconnected.
INM+ and INM-	These header pins provide a connection to a differential audio input signal which can be applied to the mono input.
INL and INR	These header pins provide a connection to stereo left and right single-ended input.
LSOUT- and LSOUT+	These header pins provide a connection to class D loudspeaker outputs. A load of greater than 4Ω can be applied at the inputs (a low pass filter may be required for measurements).
HPL and HPR	These header pins provide a connection to headphone outputs. A load of greater than 16Ω can be applied at the inputs.
JU1	Stereo, 0.125” headphone jack. Left channel is on the tip connector and the right channel is on the ring connector. Ground is on the sleeve connector.
JU2	It connects the USB board ground to main ground on the LM49151 demonstration board.
JU3	I^2C supply voltage as the source for I^2CV_{DD} pin.
JU4 (REV B ONLY)	These 3 pins jumper provides supply voltage through USB board. Either 5V or 3.3V can be selected. Use only if there is no external power supply is been used on V_{DD} and GND header pins.

8 Power Supply Sequencing

The LM49151 uses two power supply voltage: V_{DD} for the Class D power amplifier and the Class AB headphone amplifier and I^2CV_{DD} for the digital controls (volume, shutdown, ALC etc.). If using two separate power supplies and to ensure proper functionality, apply I^2CV_{DD} first, followed by V_{DD}. The part will power-up with shutdown active, the volume control set to minimum and ALC (Automatic Level Control) turned off.

9 I^2C Interface GUI Software

The I^2C signal generation USB interface board, along with the LM49151 GUI software, will generate the address byte and the data byte used in the I^2C control data transaction (see Figure 3). To use the I^2C signal generation USB interface board, plug it into a PC’s USB port (on either a notebook or a desktop computer). The software comes with an installer. See Section 10 for the software installation instructions.

10 Software Installation Instructions (Windows 200/NT/XP)

1. Unzip the LM49151 setup.zip file to a specified folder.
2. Run “LM49151 setup.msi” from the specified folder. (If asked to installed Microsoft framework 2.0, please proceed first; internet connection may be required)
3. The LM49151 Control Software installation will begin.

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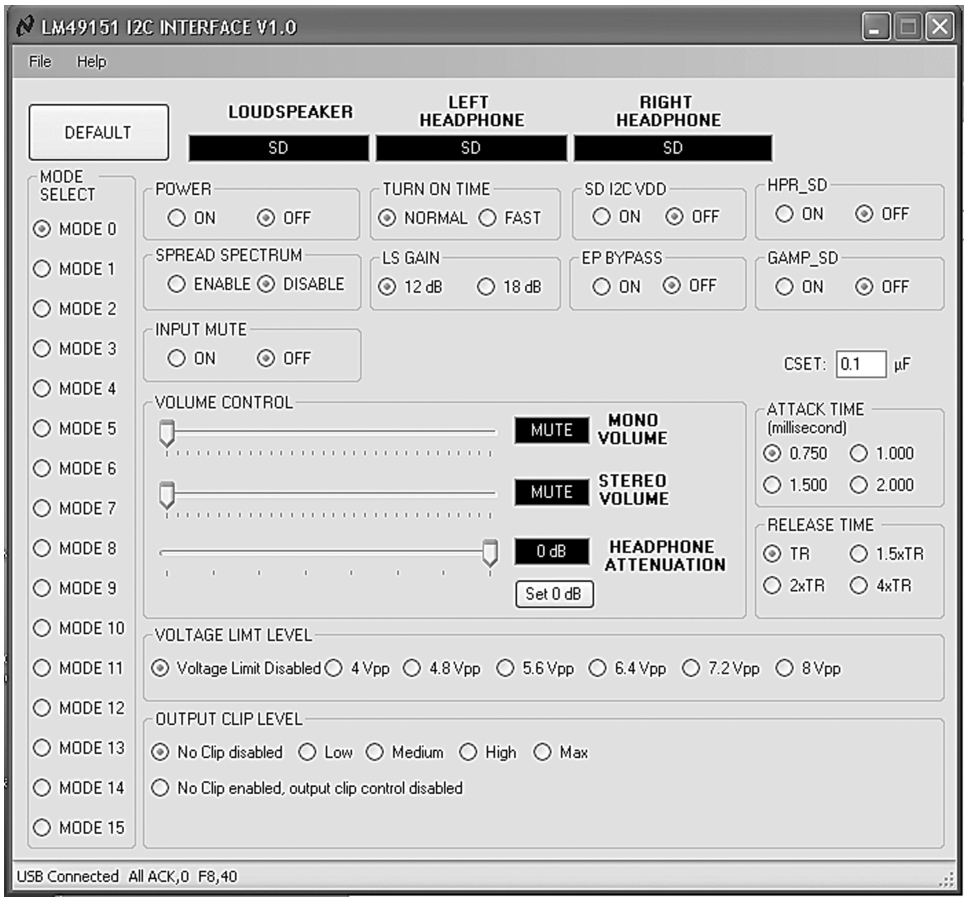

Figure 3. LM49151 I²C Interface GUI Software

11 Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM49151 and the load results in decreased output power and efficiency. Trace resistance between the power supply (V_{DD}) and the GND of the LM49151 has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces, for power-supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as providing heat dissipation from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with audio signal. Use of power and ground planes is recommended. The following recommendations should be considered when laying out the different grounds of the LM49151. Refer to the Demo Board Schematic for the corresponding component designators. Bypass capacitors for AV_{DD} (C4, C5), LSV_{DD} (C7) should be grounded to the GND pin via a ground plane. Bypass capacitor for CPV_{SS} (C4) should be grounded via a wide trace or a ground plane to the CPGND pin. The headphone grounds should be connected to the GND via a separate trace also. This will help prevent noise from the charge pump from feeding into the power supplies and the output. Place all digital components and digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer.

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12 Bill of Materials

Designator	Qty	Component Type	Value	Manufacture	Part Number
U1	1	Mono Class D Audio Subsystem with Earpiece Driver, Ground Referenced Headphone Amplifiers and Speaker Protection		TI	LM49151
C1, C2, C6	3	CAP CERAMIC 2.2UF 10V X5R 10% 0603	2.2µF	Panasonic	ECJ-1VB1A225K
C3	1	CAP CERAMIC .1UF 50V X7R 10% 0603	0.1µF	Panasonic	ECJ-1VB1H104K
C4, C7, C8	3	CAP 1.0UF 16V CERAMIC X5R 10% 0603	1µF	Panasonic	ECJ-1VB1C105K
C9, C10	2	CAP 1UF 16V CERAMIC X7R 10% 1206	1µF	Panasonic	ECJ-3YB1C105K
C11, C12	2	CAP .22UF 16V CERAMIC X7R 10% 1206	0.22µF	Panasonic	ECJ-3VB1C224K
C5	1	CAP TANT LOESR 10UF 16V 10% SMD	10µF	AVX	TPSB106K016R0800
R1, R2	2	5K 0.05 1/10W Thick Film SMT RES_0603_CHIP	5K	Vishay	CRCW06035R1KJNEA
		Alt: RES 5.1K OHM 1/10W 5% 0603 SMD			Alt: CRCW06035K10JNEA
JU1	1	5-Pole CONN JACK STEREO 3.5MM HORIZON		Switch Craft	35RAPC4BH3
J2	1	CONN SOCKET PCB VERT 16POS .1", Bottom Mount		3M	8516-4500PL
GND, HPGND, HPL, HPR, I^2CVDD, INL, INM-, INM+, INR, JU2, LSOUT-, LSOUT+, VDD	13	CONN HEADER VERT .100 2POS 30AU		AMP	87220-2
JU3, JU4	2	CONN HEADER VERT .100 3POS 30AU		AMP	87220-3
JU2_SH, JU3_SH	2	Jumper Shunt w/handle, 30uin gold plated, 0.100" pitch		Tyco/AMP	881545-2

13 Demonstration Board PCB Layout

Figure 4 through Figure 9 shows the different layers used to create the LM49151 four-layer demonstration board. Figure 4 is the top silkscreen that shows parts location, Figure 5 is the top layer, Figure 6 is the upper middle layer, Figure 7 is the lower middle layer, Figure 8 is the bottom layer, and Figure 9 is the bottom silkscreen that shows remaining parts location.

14 Revision History

Rev	Date	Description
1.0	05/13/09	Initial WEB released.

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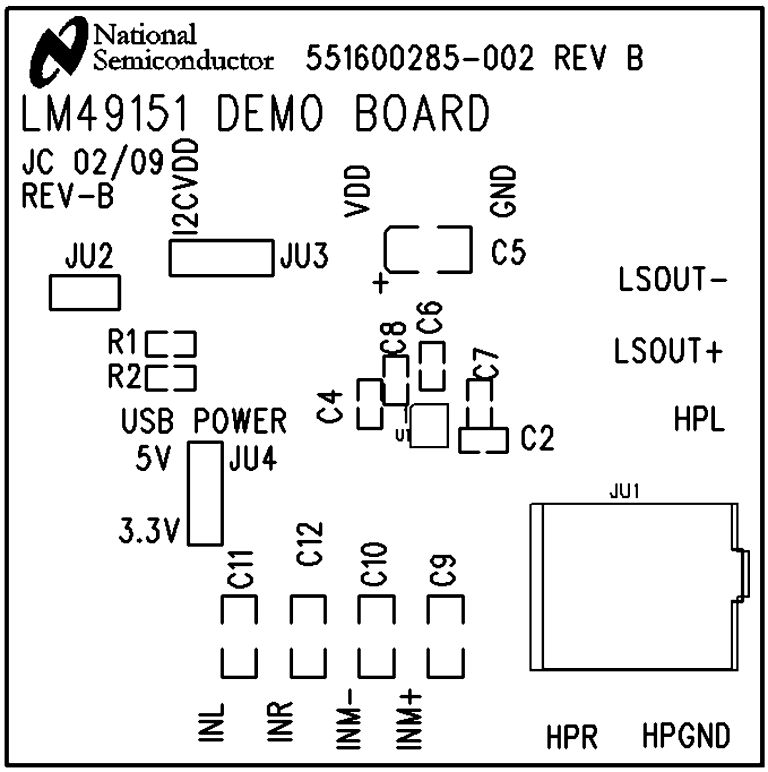

Figure 4. Top Silkscreen (Shown 2.6X actual size)

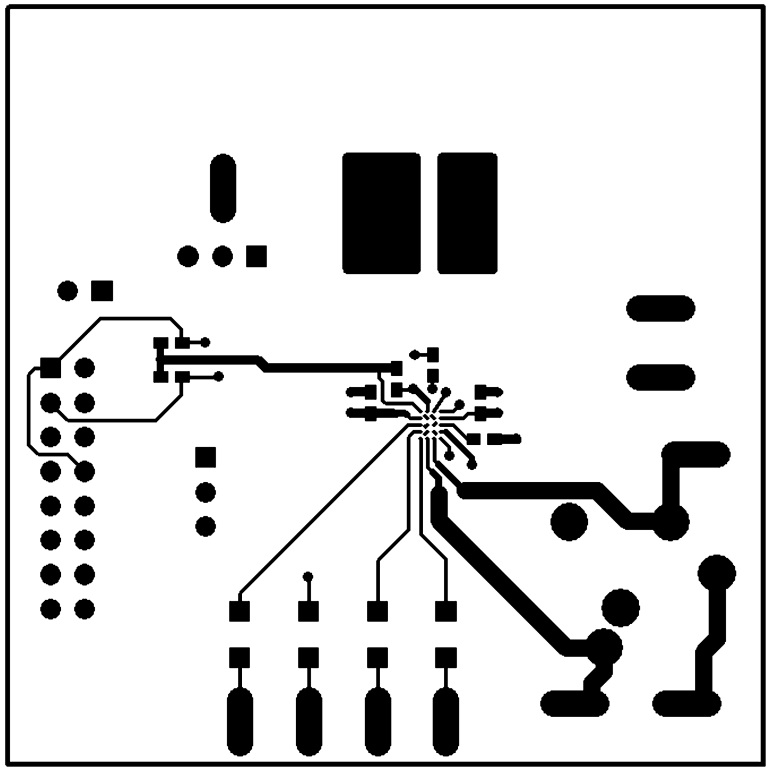

Figure 5. Top Layer (Shown 2.6X actual size)

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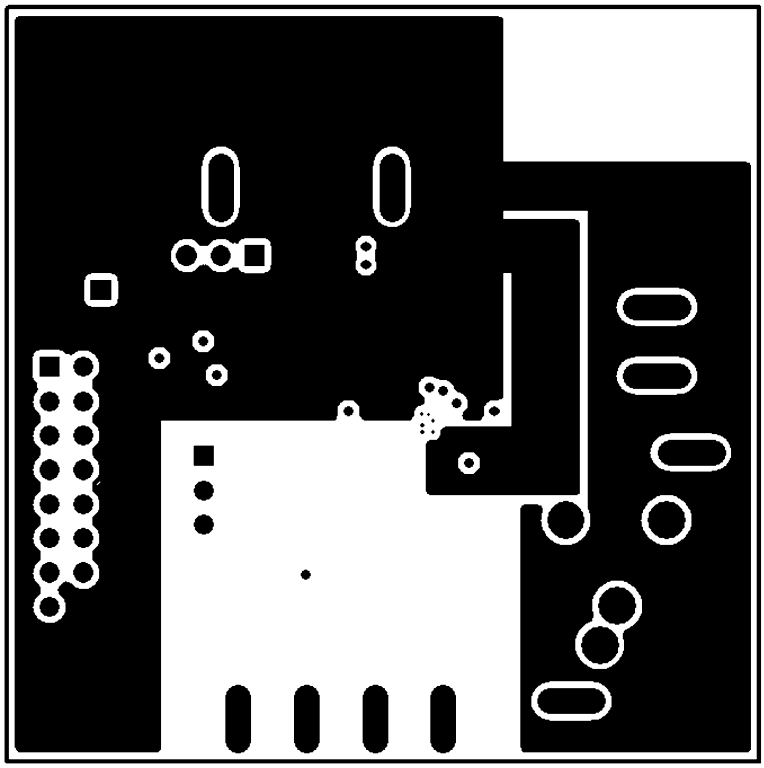

Figure 6. Upper Middle Layer (Shown 2.6X actual size)

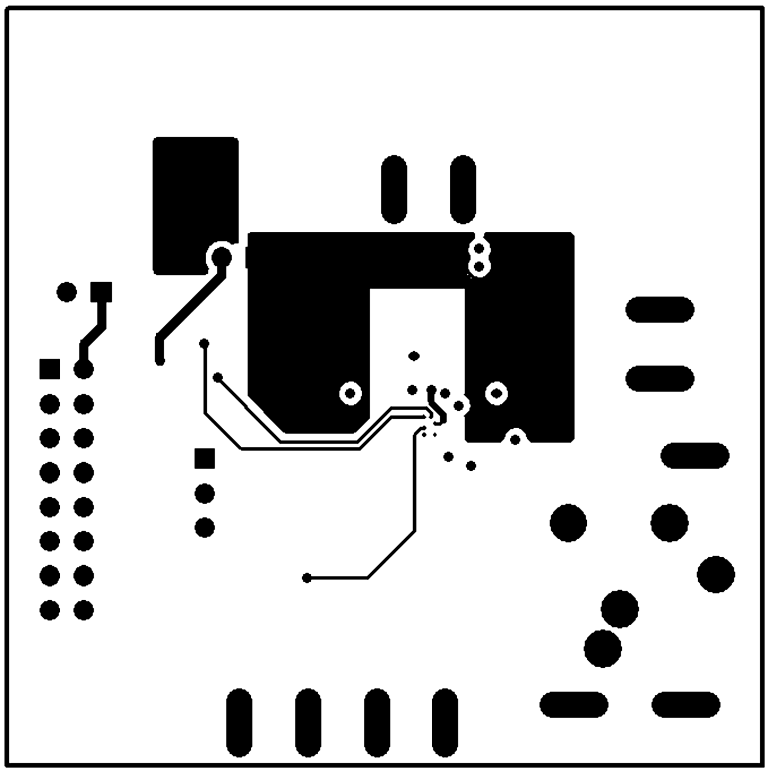

Figure 7. Lower Middle Layer (Shown 2.6X actual size)

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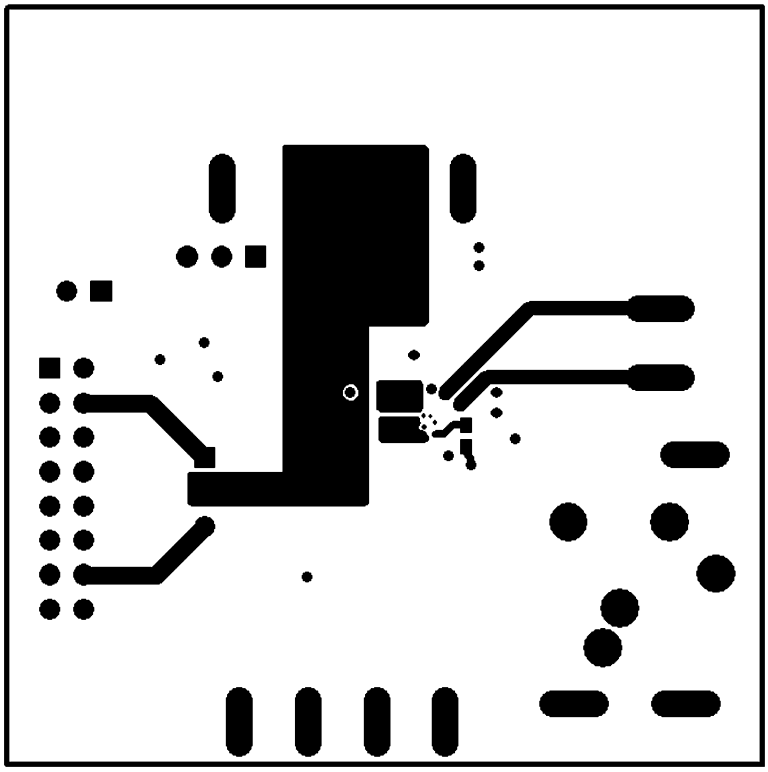

Figure 8. Bottom Layer (Shown 2.6X actual size)

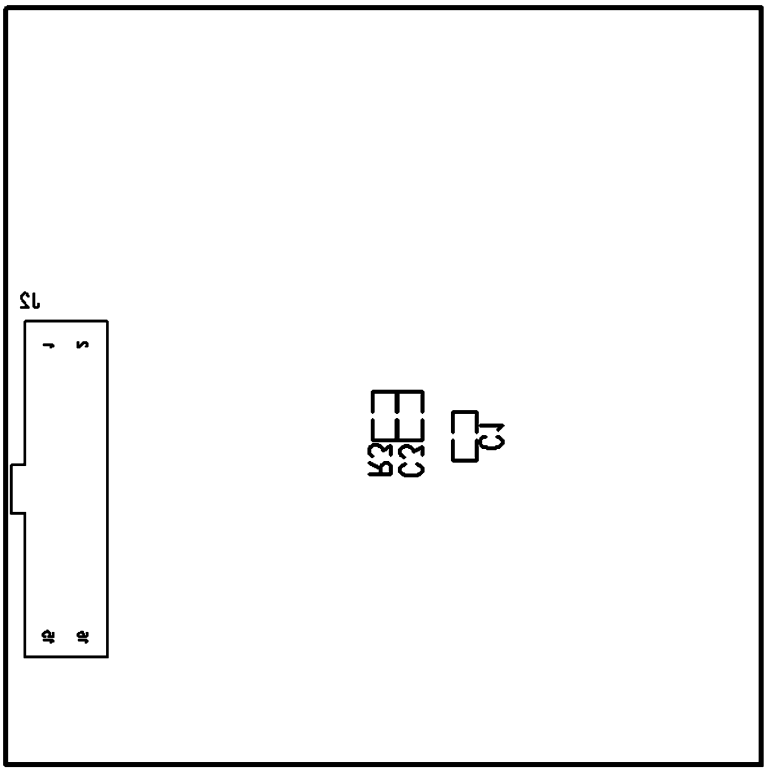

Figure 9. Bottom Silk Layer (Shown 2.6X actual size)

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