AN-1966 LMH2190 Evaluation Board

1 General Description

The evaluation board (Figure 1) is designed to help the evaluation of the LMH2190 Quad Channel 26 MHz Clock Tree Driver with I²C™ interface. The LMH2190 provides a digital system clock to peripheral devices in mobile handsets. It provides a solution to clocking issues such as limited drive capability for fanout or longer traces, protection of the master clock from varying loads and frequency pulling effects, isolation buffering from noisy modules, and crosstalk isolation. It has very low phase noise which enables it to drive sensitive modules such as Wireless LAN and Bluetooth.

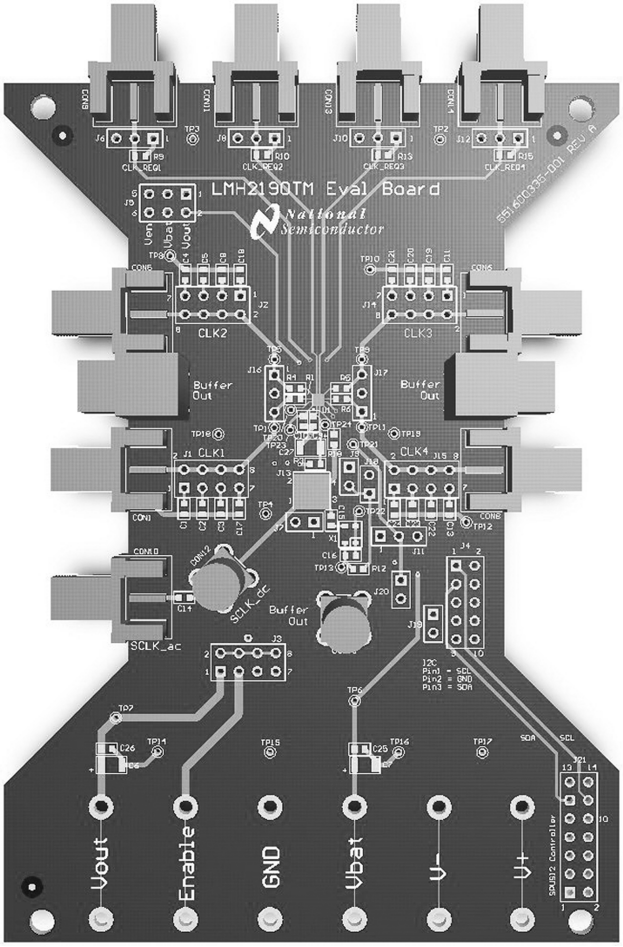

Figure 1. LMH2190 Evaluation Board

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2 Basic Operation

The LMH2190 evaluation board is designed such that it gives maximum flexibility in evaluating the LMH2190 in various configurations. The schematic, Bill of material and board layout can be found at the end of this document. In the following sections a description will be given on how to setup the measurement bench. For the factory default jumper setting, refer to Section 3.

2.1 Supply

The common ground of the evaluation board is connected via Connector CON3. The LMH2190 is powered via V_{BAT} (CON2). The typical supply voltage for V_{BAT} is 3.5V, but it may range from 2.5V to 5.5V. In the factory default configuration the ENABLE voltage is supplied externally via connector CON7 and should be 1.8V. Three on-board buffers are separately powered through Connector CON18 (+5V) and CON 19 (-5V). If they are not used for evaluation they can be left un-powered when jumper locations J7, J16 and J17 are open.

2.2 Applying Clock

In factory default configuration the clock to the LMH2190 is supplied by the on-board TCXO. Alternatively the clock can be applied externally either in DC mode via CON12 or in AC mode via CON10. The clock source can be selected by J13. Note that for DC mode, the I^2C registers also need to be changed.

The LMH2190 distributes the clock to a maximum of 4 outputs, CLK1 to CLK4, that are accessible via CON1, CON5, CON6 and CON8. An additional capacitive load can be connected between CLK to GND to simulate the load in the actual application via J1, J2, J14 and J15.

There is also a possibility to measure the clocks as well as the TCXO clock via a buffer. This buffer can drive 50 ohm making them excellent for connecting to measurement equipment, like a Signal Source Analyzer. This analyzer can for instance measure the Phase noise and Jitter. The three buffers can be connected to the clock's by J7, J16 and J17. When the buffers are not used it is recommended to disconnect them, since they increase the capacitive load on the clocks slightly.

2.3 Clock Request

The CLK's can be enabled by their appropriate CLK_REQ's. The CLK_REQ pin can be connected to a logic Low or High level via J6, J8, J10 and J12. The level of the Logic High can be selected by J5, either V_{OUT}, V_{BAT} or V_{ENABLE}. Instead of via the jumpers, the CLK_REQ's can also be controlled via CON9, CON11, CON13 and CON14. Make sure that the jumpers are removed in this case. In factory default configuration only CLK1 is enabled. The other clocks can simply be enabled by placing the jumper on J8, J10 and J12 in the other position.

2.4 I^2C Interface

The LMH2190 can be controlled by an I^2C host device that can be connected via J4. It can configure the registers inside the LMH2190 to change the default configuration. According to the I^2C specification one set of pull-up resistors needs to be present on the I^2C bus. If they are not present elsewhere in the system they can be connected on the evaluation board via J19. The evaluation board can be used without I^2C host device connected. It will then work in its default configuration.

3 Configuration

The LMH2190 evaluation board can be configured via jumper settings. An overview of the various jumper positions on the board is given in Figure 2. The settings of these jumpers and their functions are listed in Table 1.

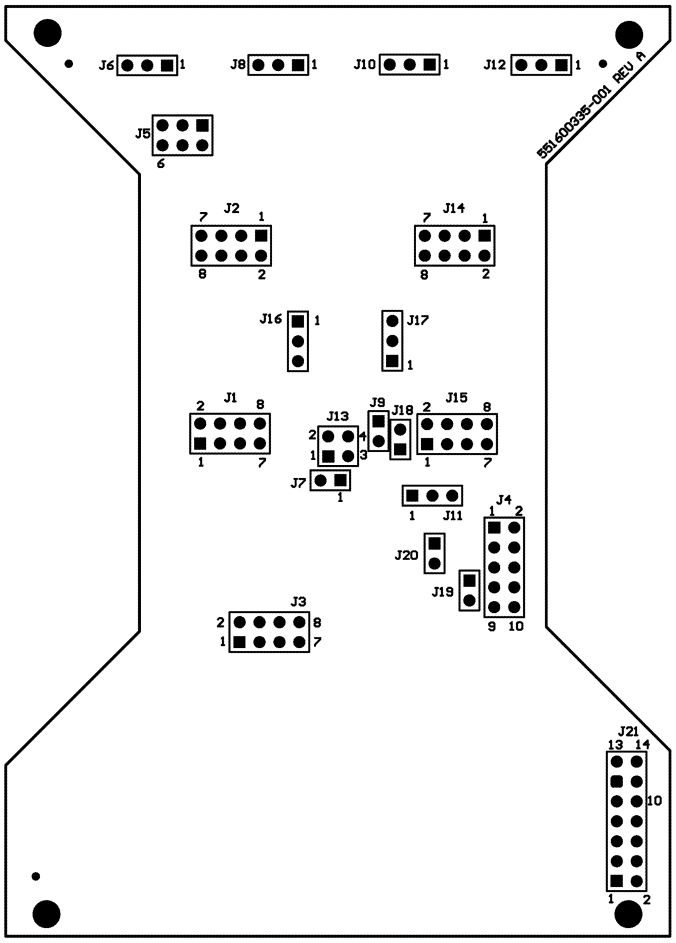

Figure 2. Jumper Positions

Table 1. Jumper and Header Overview [(1)]

Jumper	Function	Jumper Position	Desription
J1	CLK1 Capacitive load	1-2	Connects 10 pF from CLK1 to GND
		3-4	**Connects 22 pF from CLK1 to GND**
		5-6	Connects 33 pF from CLK1 to GND
		7-8	Connects 47 pF from CLK1 to GND
J2	CLK2 Capacitive load	1-2	Connects 10 pF from CLK2 to GND
		3-4	**Connects 22 pF from CLK2 to GND**
		5-6	Connects 33 pF from CLK2 to GND
		7-8	Connects 47 pF from CLK2 to GND
J3	ENABLE	1-2	ENABLE = V_{OUT}
		3-4	**ENABLE is supplied by CON7**
		5-6	ENABLE is supplied by I^2C conector J4 pin 4
		7-8	ENABLE = GND
J4	I^2C Header		Header to connect I^2C signals
J5	CLK_REQx Logic High Level	1-2	$CLK\_REQx_{HIGH} = V_{OUT}$
		3-4	**$CLK\_REQx_{HIGH} = V_{BAT}$**
		5-6	$CLK\_REQx_{HIGH} = V_{ENABLE}$

(1) Bold face jumper settings refer to the factory default configuration.

Table 1. Jumper and Header Overview [(1)] (continued)

Jumper	Function	Jumper Position	Desription
J6	CLK_REQ1	Open	CLK_REQ1 can be controlled externally via CON9
		1-2	CLK_REQ1 = GND
		2-3	**CLK_REQ1 = High. Level is determined by J5**
J7	Connects Buffer to TCXO OUT	**Open**	**No buffer connected to measure TCXO Clock**
		1-2	Buffer LMH6559MA (U2) is connected to measure TCXO Clock. Buffer can drive 50 Ohm.
J8	CLK_REQ2	Open	CLK_REQ2 can be controlled externally via CON11
		1-2	**CLK_REQ2 = GND**
		2-3	CLK_REQ2 = High. Level is determined by J5
J9	TCXO Supply	**1-2**	**TCXO is supplied by V_{OUT}**
J10	CLK_REQ3	Open	CLK_REQ3 can be controlled externally via CON13
		1-2	**CLK_REQ3 = GND**
		2-3	CLK_REQ3 = High. Level is determined by J5
J11	SCLK_REQ Pull Up / Pull Down	**Open**	**No Pull-up or Pull-down connected to SCLK_REQ**
		1-2	100 kΩ Pull-down resistor connected from SCLK_REQ to GND
		2-3	100 kΩ Pull-up resistor connected from SCLK_REQ to V_{BAT}
J12	CLK_REQ4	Open	CLK_REQ4 can be controlled externally via CON14
		1-2	**CLK_REQ4 = GND**
		2-3	CLK_REQ4 = High. Level is determined by J5
J13	SCLK_IN Source	1-2	SCLK_IN is connected to External Source, either through CON10 (AC-Coupled) or CON12 (DC-Coupled)
		3-4	**SCLK_IN is connected to on-board TCXO**
J14	CLK3 Capacitive load	1-2	Connects 10 pF from CLK3 to GND
		3-4	**Connects 22 pF from CLK3 to GND**
		5-6	Connects 33 pF from CLK3 to GND
		7-8	Connects 47 pF from CLK3 to GND
J15	CLK4 Capacitive load	1-2	Connects 10 pF from CLK4 to GND
		3-4	**Connects 22 pF from CLK4 to GND**
		5-6	Connects 33 pF from CLK4 to GND
		7-8	Connects 47 pF from CLK4 to GND
J16	Connects Buffer to CLK1/2	Open	No buffer connected to CLK1/2
		1-2	Buffer LMH6559MA (U3) is connected to measure CLK2. Buffer can drive 50 Ohm.
		2-3	**Buffer LMH6559MA (U3) is connected to measure CLK1. Buffer can drive 50 Ohm.**
J17	Connects Buffer to CLK3/4	**Open**	**No buffer connected to measure TCXO Clock**
		1-2	Buffer LMH6559MA (U4) is connected to measure CLK4. Buffer can drive 50 Ohm.
		2-3	Buffer LMH6559MA (U4) is connected to measure CLK3. Buffer can drive 50 Ohm.
J18	TCXO Supply Header		Header can be used to provide an (external) TCXO supply instead of the on-board V_{OUT} supply. Header J9 should be open in this case.
J19	I^2C Pull-up Resistors	Open	No Pull-up resistor connected to SDA and SCL line. Elsewhere should be pull-up resistors present on SDA and SCL
		1-2	**Pull-up resistors connected on SDA and SCL**
J20	SCLK_REQ Header		Header to monitor SCLK_REQ.
J21	Future purpose		Not Assembled

4 Measurement Setup

The performance of the LMH2190 can be measured with the setup shown in Figure 3.

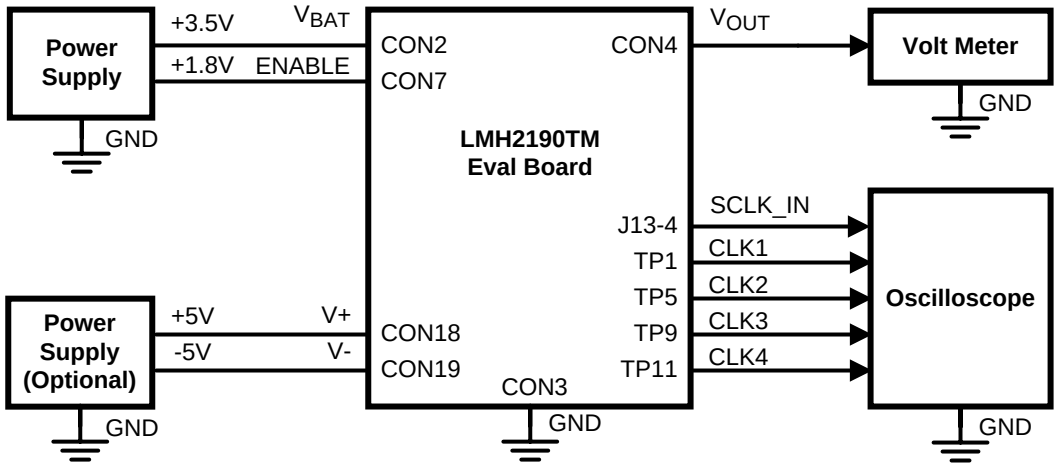

Figure 3. Measurement Setup

The +5V and -5V to connector CON18 and CON19 don't need to be applied unless buffers U2, U3 and/or U4 are used for the measurements. In factory default configuration, only CLK1 is enabled. With an oscilloscope and Hi-impedance probes the TCXO (J13–4) and CLK1 (TP1) can be measured. This should result in a measurement as depicted in Figure 4. Other CLK's can be enabled by connecting the appropriate CLK_REQ to V_{BAT} (J8, J10, J12). A schematic representation of the TCXO and all the CLKs is depicted in Figure 5. It can be seen that the CLK's are skewed from each other.

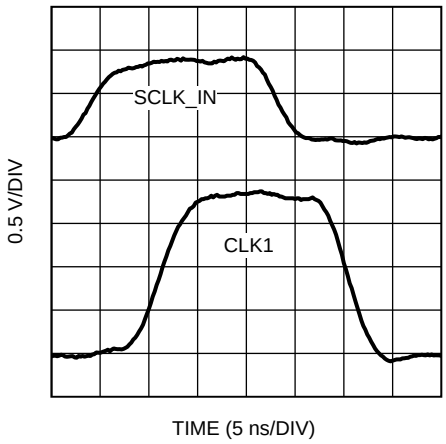

Figure 4. CLK1 Response, C_L = 22 pF

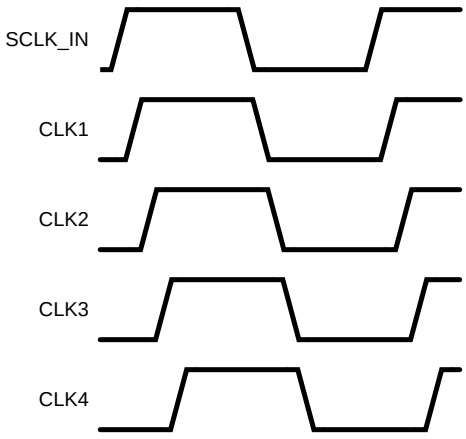

Figure 5. Clock Outputs Skewed

5 Schematic

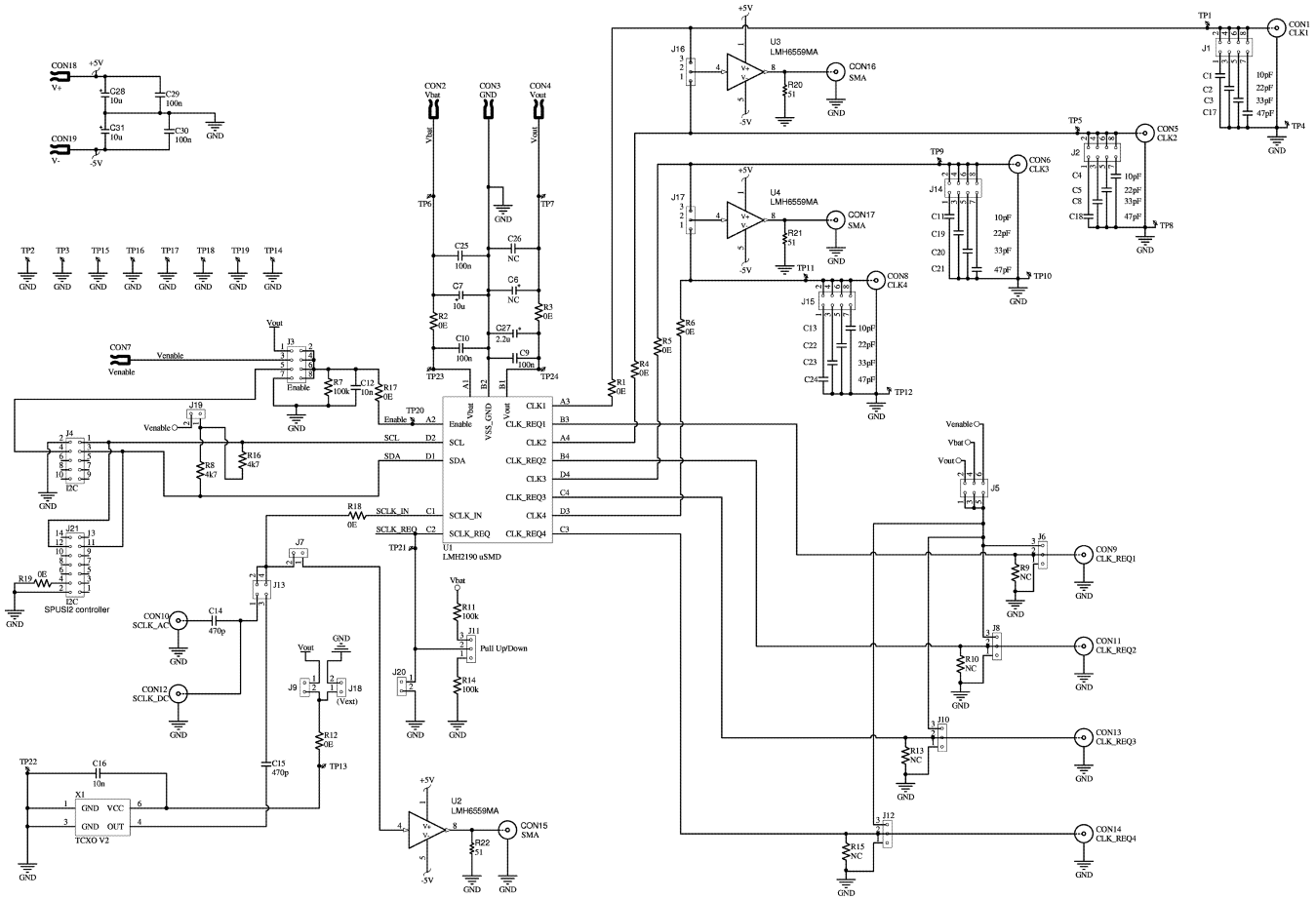

Figure 6. Evaluation Board Schematic

6 Bill of Material

The Bill of Material (BOM) of the evaluation board is in Table 2.

Table 2. Bill of Material

Designator	Description	Comment
C1, C4, C11, C13	0603 Capacitor	10 pF
C2, C5, C19, C22	0603 Capacitor	22 pF
C3, C8, C20, C23	0603 Capacitor	33 pF
C6	Case A Capacitor	NC
C7, C28, C31	Case A Capacitor	10 µF
C9, C10, C25, C29, C30	0603 Capacitor	100 nF
C12, C16	0603 Capacitor	10 nF
C14, C15	0603 Capacitor	470 pF
C17, C18, C21, C24	0603 Capacitor	47 pF
C26, R9, R10, R13, R15	0603 Capacitor / Resistor	NC
C27	Case A Capacitor	2.2 µF
CON1	Connector	SMA

Table 2. Bill of Material (continued)

Designator	Description	Comment
CON2	Connector	Banana
CON3	Connector	Banana
CON4	Connector	Banana
CON5	Connector	SMA
CON6	Connector	SMA
CON7	Connector	Banana
CON8	Connector	SMA
CON9	Connector	SMA
CON10	Connector	SMA
CON11	Connector	SMA
CON12	Connector	SMA
CON13	Connector	SMA
CON14	Connector	SMA
CON15	Connector	SMA
CON16, CON17	Connector	SMA
CON18	Connector	Banana
CON19	Connector	Banana
J1, J2, J14, J15	Header	2x4
J3	Header	2x4
J4	Header	2x5
J21	Header	2x7
J5	Header	2x3
J6, J8, J10, J11, J12	Header	1x3
J7, J9, J19, J20	Header	1x2
J13	Header	2x2
J16, J17	Header	1x3
J18	Header	1x2
R1, R2, R3, R4, R5, R6, R12, R17, R18, R19	0603 Resistor	0Ω
R7, R11, R14	0603 Resistor	100 kΩ
R8	0603 Resistor	4.7 kΩ
R16	0805 Resistor	4.7 kΩ
R20, R21, R22	0603 Resistor	51Ω
U1	DSBGA	LMH2190
U2, U3, U4	SOIC	LMH6559
X1	small	TCXO 26.0MHz

7 Board Layout

As with any other device, careful attention must be paid to the board layout. If the board is not properly designed, the performance of the device can be less than might be expected. Especially the input clock trace (SCLK_IN) and output traces (CLK1/2/3/4) should be as short as possible to reduce the capacitive load observed by the clock outputs. Also proper decoupling close to the device is necessary. Beside a capacitor in the µF range, a capacitor of 100 nF on V_{BAT} and V_{OUT} is recommended close to device. The equivalent series resistance (ESR) of the capacitors should be sufficiently low. A standard capacitor is usually adequate. The copper layers of the evaluation board are depicted in Figure 9, Figure 10, and Figure 11.

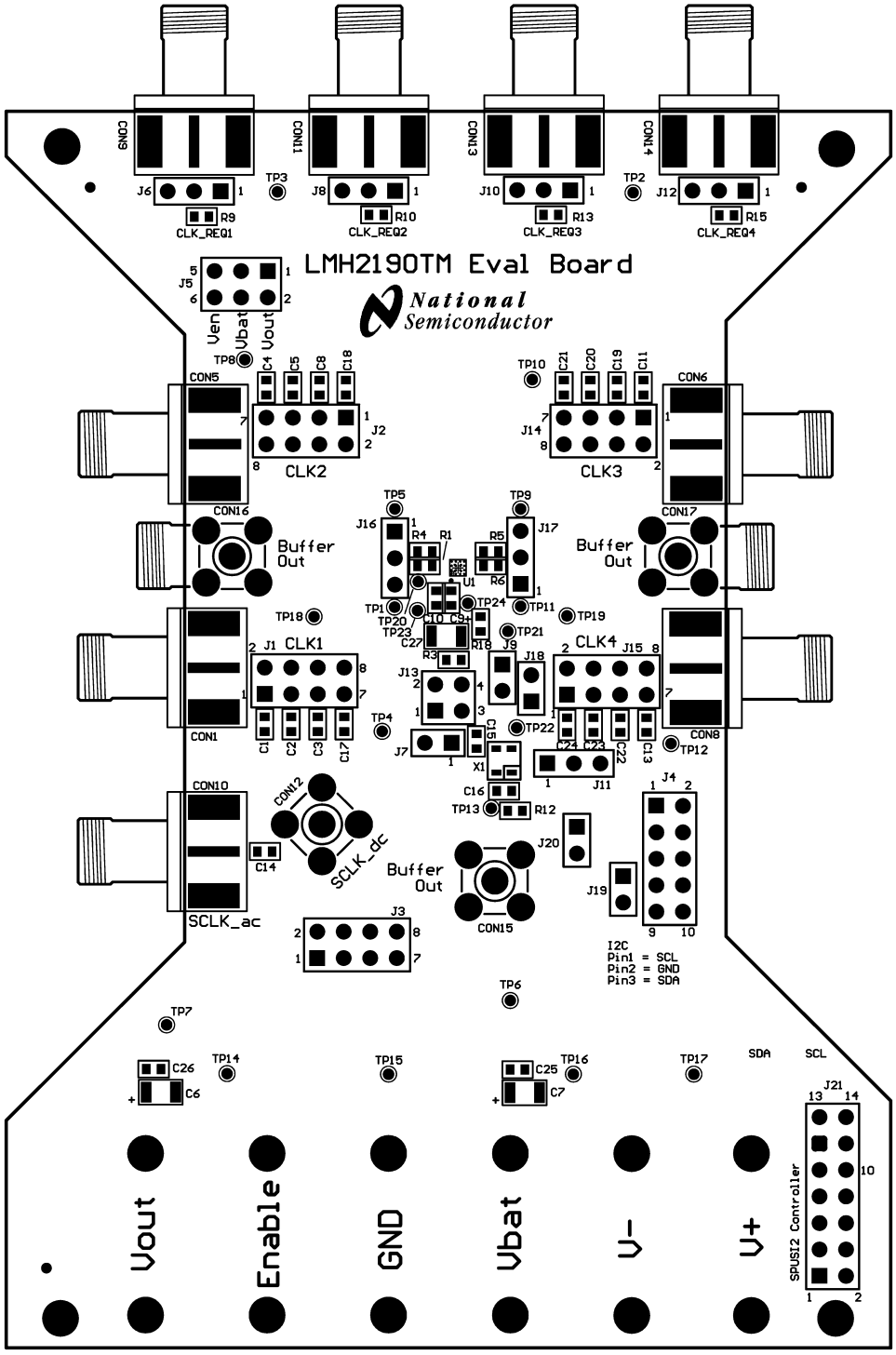

Figure 7. Component Locations Top Side

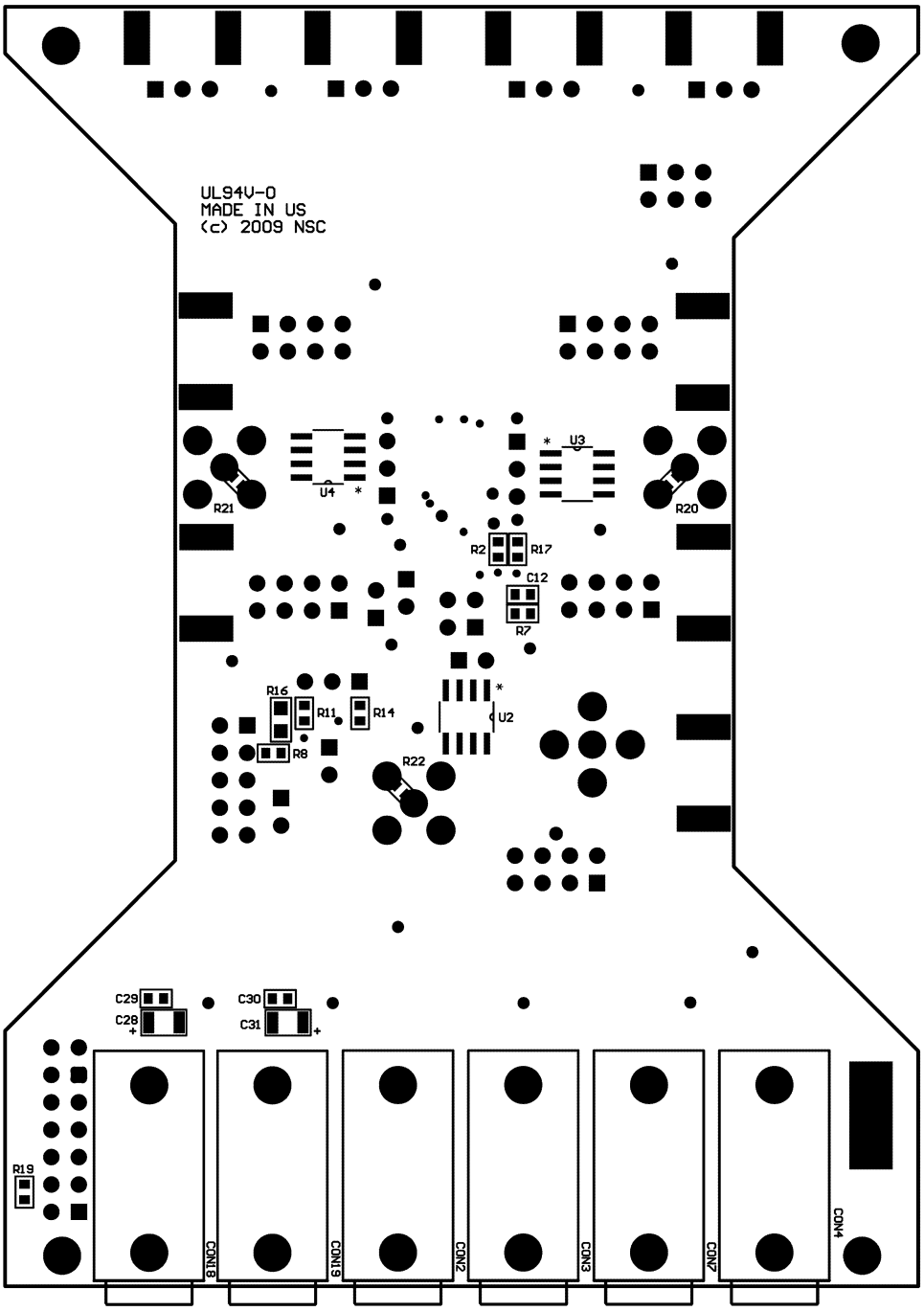

Figure 8. Component Locations Bottom Side (Bottom View)

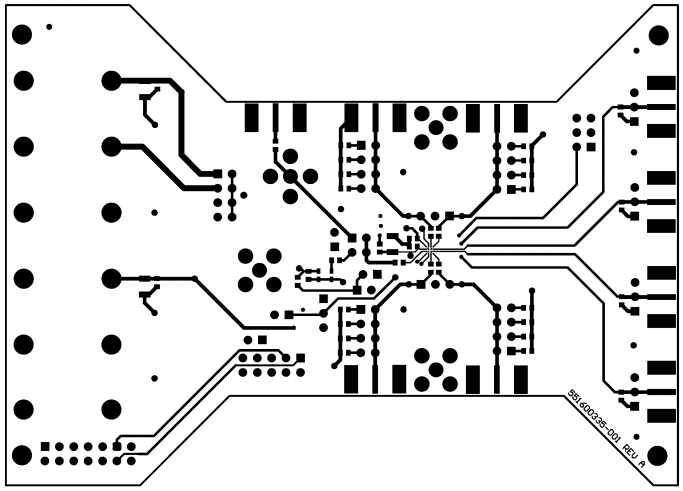

Figure 9. Top Layer of Evaluation Board

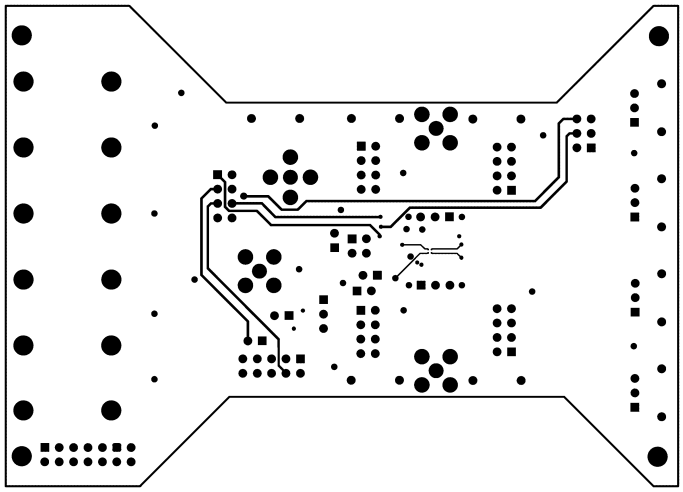

Figure 10. Inner Layer of Evaluation Board

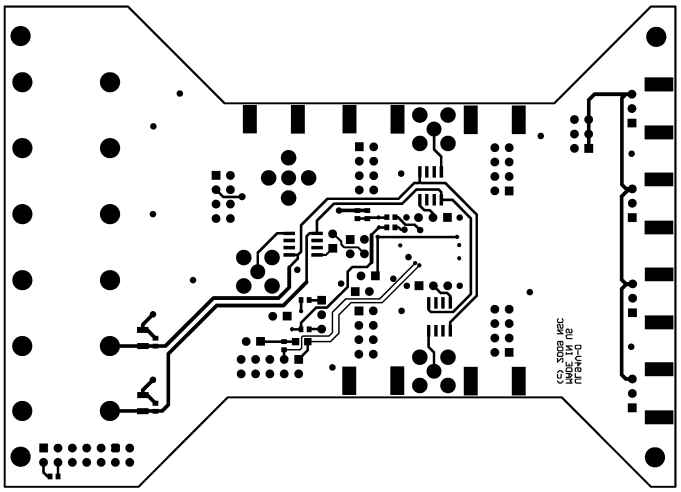

Figure 11. Bottom Layer of Evaluation Board

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