SCANSTA111,SCANSTA112

Partition IEEE 1149.1 SCAN Chains for Manageability!

Literature Number: SNLA153

Partition IEEE 1149.1 SCAN Chains For Manageability!

Application Brief 121

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Highlights

- **Partition JTAG Chains to Enhance Targeting, Throughput, and Isolation During JTAG Test**
- **Extend the IEEE 1149.1 Test Bus into a Multi-drop Backplane Environment, Allows Cards to be Removed from the Backplane without Breaking the JTAG Chain**
- **Multiple Slot Inputs Support Multiple Unique Addresses for Multi-card Systems**
- **A Mode Register Allows Local TAPS to be Bypassed, Selected for Insertion into the JTAG Chain Individually, or Serially in Groups**
- **BGA Packaging Minimizes Board Space**

The proliferation of IEEE 1149.1 supported devices is helping Design for Test (DfT) engineers solve complex test access problems during board test. As ICs become more complex and boards become denser, this dedicated 5-wire serial test bus provides simple, standardized access to internal test nodes unreachable with existing In-Circuit-Test (ICT) methods. Many new board designs are incorporating JTAG as a standard feature for test and programming access – in many cases there is simply no other methodology capable of achieving an acceptable level of board fault coverage, or a cost effective means of programming on-board.

If you're investigating this technology for addition to a new board design, consider this: Many 1149.1 devices on a single JTAG chain mean numerous boundary scan cells and long JTAG chains, large test vector sets, and long test times. A method of partitioning the JTAG chain will improve manageability, device targeting, and isolation *(Figure 1)*. Furthermore, if you're considering a system level test strategy at some point in the future, a method to support JTAG across the system backplane is needed to support this strategy.

The solution is to use a multi-drop JTAG multiplexer IC on each board to manage the test bus. The multi-drop capability supports a backplane JTAG bus with addressable access to each board *(Figure 2)*, while the multiplex capability supports multiple partitioned JTAG chains on a single board. This allows a design with critical IC components isolated into private JTAG chains for direct access, or isolation of JTAG programmable components for the fastest configuration access.

For instance, if you were using a JTAG accessible microprocessor to emulate bus cycles for FLASH programming, it would make sense to isolate the processor on a dedicated JTAG chain to optimize the speed of this approach. If you're using FPGAs from different vendors on the same board, be aware that FPGA vendors don't necessarily use the same vector formats, or some can't handle having any additional devices on the same chain with the target device, therefore isolation is necessary. It may also be prudent to isolate backplane buffer devices onto a single JTAG chain – this allows you to quickly verify the circuit board is inserted into the backplane properly.

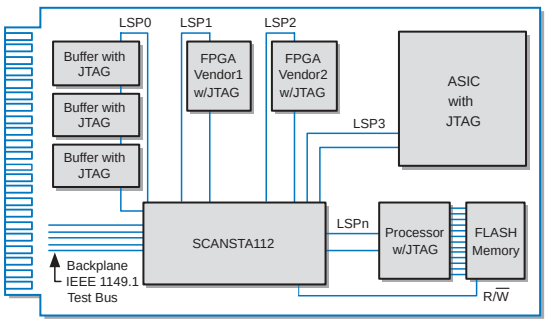

Figure 1: Typical Use of SCANSTA112 for Board Level Management of Multiple JTAG Chains

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SCANSTA111

The SCANSTA111 is a multi-drop addressable JTAG multiplexer that features three configurable local JTAG ports. When the 'STA111 is added to a board, the backplane test port can be accessed with a dedicated JTAG connector during board test, or connected to a backplane test bus. When multiple cards with a 'STA111 are connected to the backplane test bus – each with a unique address – the card can be selected for access to any combination of the three local JTAG ports on that board. The device also supports two pass thru bits on some local ports for emulators or for delivering write pulses for FLASH programming. The 'STA111 addressing and multiplexing scheme is well supported and automated by the major ATPG (Automatic Test Program Generation) software vendors such as JTAG Technologies, Goepel, and Corelis.

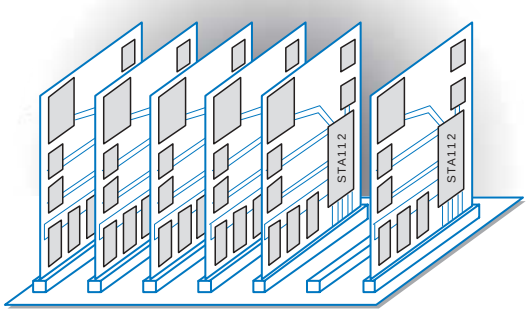

Figure 2: Example of SCANSTA112 in a Multi-card Backplane Environment

SCANSTA112

The SCANSTA112 is an enhanced version of the 'STA111, featuring seven local scan ports for designs which require additional partitioning of the JTAG test bus. In addition, this device has an interchangeable bidirectional backplane and LSP0 port to allow an alternate test master or an emulator to take control of the JTAG bus. Selection of the local JTAG ports can be accomplished by an instruction, or by external pins when the device is placed in stitcher mode.

The IEEE 1149.1 Standard for Boundary Scan Test (often referred to as JTAG, 1149.1, or just "dot 1") is an industry standard method for accessing test features on complex ICs and circuit boards. Compliant ICs and boards have a 4-wire serial bus (with optional reset) to support JTAG test – TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). In addition to its use for structural test, many CPLD manufacturers are using JTAG as a standard method for programming or configuring their devices. JTAG supports not only structural (interconnect) test, but is now a well supported standard approach for enabling system-level access for configuration, programming, and mixed signal test.

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