LMH0002,LMH0030,LMH0031

LMH0030 (CLC030), LMH0031 (CLC031A) - Frequently Asked Questions (FAQs)

Can I directly interface the LMH0030 to the LMH0002?

> The LMH0030 serializer can be directly (DC) coupled to the LMH0002 (CLC002) cable driver. It is best to do so differentially using as short a network as possible. Two termination methods are recommended.
>
> 1. Design the traces of the differential pair to have a basic impedance of 75 Ω and space them to give a 100 Ω differential impedance. The Transmission Line Rapidesigner Sliderule is a convenient tool for this calculation. The network will begin with the LMH0030 outputs and end with the LMH0030's normal 75 Ω output pull-up resistors. These will provide the proper line termination. The LMH0002 (CLC002) input will be located on the network between the ends and connected in "daisy chain" fashion. This technique uses no additional components.
>
> 2. Design the traces for a convenient impedance level between 50 and 75 Ω. Space the traces to give a 100 Ω differential impedance. Again, the network will begin with the LMH0030 outputs and end with the termination. The termination network will consist of 3 resistors, 2 output pull-ups and a parallel termination across the differential pair. The 2 pull-up resistors will be 115 Ω and the parallel termination will be 100 Ω. This combination of resistances provides a 75 Ω load for the LMH0030 outputs and a 100 Ω termination for the differential pair. The swing at each of the LMH0030 outputs will be 800mV. The swing developed across the differential termination will be about 740mV. This is the proper level for the LMH0002 (CLC002) inputs.
>
> **Relevant Part**: CLC030; CLC002; LMH0002; LMH0030

The LMH0030 generates a 75% saturation color bar test pattern. Can it be programmed to generate a 100% saturation color bar pattern?

> The test pattern generator data is produced from hard-coded stored sequences of parallel video data as well as algorithmically generated data. Provision is not made for altering the data or substituting other data sequences.
>
> **Relevant Part**: CLC030; CLC031A; CLC020; CLC021A; LMH0030; LMH0031

Can the LMH0030 and LMH0031 insert time code packets in ANC space?

> Yes. The time code data (LTC) is handled the same as other ANC data. Be sure that the appropriate DID and SDID are applied and the packets loaded for insertion in the correct lines.
>
> **Relevant Part**: CLC030; CLC031A; LMH0030; LMH0031

What type of multiplexed audio data packets do the LMH0030 and LMH0031 support?

The LMH0030 and LMH0031 are designed to handle parallel digital data samples of AES-ABU Level-A (default) synchronous 48kHz, 20-bit audio. The data is transported in the chrominance channel only for high definition operation. Level-A data does not require control packets in the luminance channel. Control packets that are needed for other levels of AES-EBU data are not supported. Multiplexed ancillary data is supported for standard definition parallel component video operation according to the requirements of SMPTE 125M.

The LMH0030 serializer multiplexes and encodes ancillary data packets stored in its on-board FIFO into the serial video data stream. Data is not retained in the FIFO after it has been inserted in the serial data.

The LMH0031 de-serializer decodes multiplexed ancillary data packets from the incoming serial video data stream. This data is replicated into and stored in the on-board FIFO. The data packets may then be read out of the FIFO in parallel format for further processing. Data is not retained in the FIFO after being read out.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Can the LMH0030 be used with 50Ω output loads and networks?

The LMH0030 can be used with 50Ω output networks and pull-up resistors. However, the peak-to-peak output swing will decrease by 1/3rd from 800mV to 530mV. The outputs are current sinking and the amount of current available at the output is limited by the current source supplying the outputs. The output level (current) adjustment does not have enough range to bring the output swing to 800mV with the lower resistance load. Generally, this reduced swing will be sufficient to drive virtually any device especially if driven differentially. The increased load may also reduce the transition times of the outputs. The amount of reduction depends on the capacitance characteristic of the particular load.

Relevant Part: CLC030; LMH0030

At what times can the LMH0031 FIFO EXTRACT ENABLE be asserted?

The FIFO EXTRACT ENABLE control should be asserted at a convenient time during the active video line interval. It should not be asserted during the ancillary data portion of the video line as that could corrupt reception of the data by the FIFO. Also, this signal should not be asserted while the data is being read from the FIFO. Otherwise, FIFO EXTRACT ENABLE can be asserted at any time prior to the EAV. It is probably most convenient to read data from the FIFO during the early portion of the active video interval and to update register controls such as FIFO EXTRACT ENABLE during the latter portion of this interval. The transition of the H-bit during the SAV can be used as the cue that it is time to read the FIFO and update the registers if needed.

Relevant Part: CLC031A; LMH0031

Can the LMH0031 deserialize formats other than those listed in the Table 4 of the datasheet?

The LMH0031 can deserialize and word-align HD formats other than those listed in Table 4 of the datasheet. The FORMAT 0 Register (register 0Bh) must be loaded with a code which will place the device in HD mode and which will suppress format identification.

Any of four codes can enable this type of operation. These codes differ in regard to how the device is set to re-frame the data with regard to out-of-place TRS sequences (also called NSP or new-sync-position). The codes are 10-bits in length. Bits AD[9:8] are data word identifier bits and are always set for a data word. Bits AD[7:0] are the register content bits. The data word format is therefore: 3XXh.

Register 0Bh bit-7 is the FRAMING MODE bit. This bit is set by default. It may be reset to change the manner in which NSP is arbitrated. Bit-5 is the HD-ONLY bit. This bit is set for processing HD data. And bit-6, SD_ONLY, is reset in this instance. The FORMAT[4:0] bits may all be either set or reset. Therefore, the control data codes that enable processing of unsupported HD formats can be 330h, 3B0h, 33Fh or 3BFh. Device deserialization operation when using these codes is virtually identical except for the way that re-framing is handled (re. bit-7). To maintain default framing arbitration, use codes 3B0h or 3BFh.

In addition to suppressing format identification and reporting, these codes also suppress the CRC error checking and line number functions.

Refer to the description of the FRAMING MODE and FRAMING ENABLE bits in the datasheet section on the FORMAT 0 Register for details of the operation of the framing mode options and operation.

Relevant Part: CLC031A; LMH0031

How can the LMH0034 be interfaced to the LMH0031?

The LMH0034 output can be DC-coupled to the LMH0034 input with a simple 100Ω differential termination since their common mode voltages are within the same range. The termination should be placed close to the receiver (LMH0031) input.

Relevant Part: CLC031A; LMH0034; LMH0031

Does the color bar test pattern in the LMH0030 and LMH0031 use the same chroma and luma data for SD and HD?

Yes, The color bars use the same color gamut (luminance and chrominance data) for both SD and HD. The extended HD gamut is not supported.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

When using the Test Pattern Generator (TPG) function, must the FORMAT SET bits of the FORMAT 0 register be loaded for the LMH0030 or LMH0031?

No. When using the TPG function, the video format should not be set using the FORMAT 0 register. The device will automatically recognize the format according to the setting of the TEST PATTERN SELECT bits of the TEST 0 register.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Are pull-down resistors needed on unconnected CMOS inputs of the LMH0030 or LMH0031?

No. All CMOS inputs (except ACLK and VCLK) are equipped with internal pull-down devices.
Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Can I connect and drive the Ancillary/Control Port of more than one LMH0030 or LMH0031 device with a data bus?

Yes. The Ancillary/Control Port may be bussed with other similar devices for control data functions. Control Port operation depends on three signals, ACLK, ANC/CTRL(bar) and RD/WR(bar). ACLK is the signal which activates the port to receive or drive data. ACLK may be gated with an externally derived chip select in order to affect reading or writing control data to the port. Gating used for this function should be carefully designed so as not to produce decoding glitches which could result in improper data transfers to multiple devices. Additionally, each device has one unique "do-nothing" mode: ANC+RD for the LMH0030 and ANC+WR(bar) for the LMH0031. When practical, non-addressed devices should be placed in their "do-nothing" state. Following Control+Read operations, be certain to issue a second ACLK to return the port to its address write (address load) mode.
Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Can the LMH0030 and LMH0031 handle both HD parallel rates, 74.25MHz and 74.25/1.001MHz?

Yes. Both of these rates and the corresponding serial rates, 1.485Gb/s and 1.485Gb/s/1.001, are supported. Since the formats for both rates are the same, the frequency difference is not reported via the Control Registers.
Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Can the TPG be used when other data is being input?

Yes. The TPG data will override the externally applied data and be output.
Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Does the duty cycle specification apply to ACLK when it is used for performing Control Register operations?

No. The duty cycle specification for ACLK applies only to Ancillary Data operations.
Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

How do I turn off the Control Data Read operation of the LMH0030 or the LMH0031?

The Control Data Read operation is terminated by clocking ACLK once (after the data has been read by the host system).

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

How does the Built-In Self-Test (BIST) test the device for the LMH0030 or LMH0031?

The BIST uses the Test Pattern Generator as the data source and either the CRC system (HD) or the EDH system (SD) as the data checking system. As the test data is processed through the device, CRC or EDH check words are computed. These check words are compared with internally stored correct values for the data being used. The device passes the test when the computed and stored values agree. The result of the test is stored in bit-7 of the TEST 0 register.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

How is the Video FIFO delay set for the LMH0030 or the LMH0031?

The Video FIFO delay is set from zero to four VCLK periods by writing a corresponding binary word from 000b to 100b into bits 7, 6 and 5 respectively of the ANC 0 Control Register (address 04h). To avoid overwriting other writable bits when writing data to this or other Control Registers, the present contents of the register should be read by the controller and logically OR-ed with the new data before writing the revised data into the register.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Is Ancillary Data supported in the Luminance Channel for HD?

No. Ancillary data is supported only in the Chrominance Channel.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Is power supply sequencing required for the LMH0030 and LMH0031?

Yes. The devices use two power supply voltages, 3.3V for I/O functions and 2.5V for internal logic and PLL functions. The 3.3V supply must be applied prior to or at the same time as the 2.5V supply.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is EDH?

EDH, Error Detection and Handling, is a practice for the generation of error detection checkwords and related status flags which is used optionally in conjunction with NTSC (system M, 525/59.94) and PAL (systems B, G, H, and I, 625/50) serial digital interfaces which use either 13.5MHz or 18MHz sampled 4:2:2 component or 4fsc composite digital signals. EDH requirements are covered in SMPTE RP 165. EDH functions may also be used in parallel digital interfaces supporting the above standards. EDH is not a means of error correction.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is LSB Dithering and what is its use?

Dithering is the addition of low-level random noise to the digital data during the encoding process by varying the two LSBs of the active picture data in a pseudo-random manner. This is equivalent to one quantizing level of the analog signal prior to sampling. In digital video, LSB dithering is used to break up the transitionless sequences that are produced by so-called pathological data patterns. If not removed by the decoding process, resolution will be affected by 1/2-LSB when the data is converted back to analog.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is a TRS?

TRS stands for Timing Reference Signal. A TRS is a sequence of four 10-bit words that are used as synchronizing events in digital video data. They function in a manner similar to the vertical and horizontal synchronizing pulses in analog video. The TRS word sequence is 3FF, 000, 000, XYZ in hexadecimal 10-bit representation. For digital component video (4:2:2), eight unique TRS sequences, the XYZ words, are used to denote the start and end of active video lines, SAV and EAV, for the two fields and vertical blanking intervals. For composite data (4fsc), the TRS consists of one sequence: 3FF, 000, 000, 000.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is the purpose of Ancillary/Control Data port bits 8 and 9?

Ancillary/Control Port bits 8 and 9 are used as handshaking bits during Control Data transactions. These bits identify the type of transaction and data being processed. When the data being sent to the port is a Control Register address, these bits must both be a binary-0. When the data being sent to the port is Control Register data, these bits must both be a binary-1. During a Control Data read operation, the device will assert these bits as binary-10 (hexadecimal-2). For Ancillary data transactions, data words may be 8 or 10 bits long. Therefore, all of the port's bits may be employed as data bits. For 8-bit ancillary data these bits should remain low.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is the purpose of the SD ONLY and HD ONLY bits of the FORMAT 0 register?

The SD ONLY bit, when set, limits the device to recognize and process only SDTV formats having parallel data rates of 27MHz, 36MHz or 54MHz. The HD ONLY bit serves the same purpose and limits the device to the HD rates, 74.176MHz and 74.25MHz, and formats. Enabling either the SD ONLY or HD ONLY mode reduces the time required by the device to lock to and identify the format being processed. When both of these bits are reset (0b), the device automatically detects the range. Also refer to information about setting the video format.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is the purpose of the Video FIFO for the LMH0030 or LMH0031?

The Video FIFO may be used to insert up to four VCLK periods delay in the processing of the parallel video data. This delay function might be used to align two or more video data streams for processing purposes. For example, two video data streams (of the same rate) could be aligned on SAV sequences so that data from one stream could be mixed with or replace data from the other stream.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

When is Control Data valid during a Control Data Read operation?

The device begins to turn and drive the Control Data port as soon as the address of the control register to be read is loaded. The device driving the Control Data port should be placed in tri-state immediately following the address load so as to minimize driver overlap with the port. Output data should only be sampled after the address driver is tri-stated. Data will be driven by the port until another ACLK is received.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Where are EDH checkwords located in the video raster data for the LMH0030 or the LMH0031?

EDH checkwords and status flags for NTSC component video rasters are located in the ancillary data just prior to the EAV (End of Active Video) in Line 9 (Fields I and III) and Line 272 (Fields II and IV). Corresponding locations for PAL systems are Line 5 (Fields I, III, V and VI) and Line 318 (Fields II, IV, VI and VIII). For composite video these locations are the same.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Which Test Patterns are Built-In Self-Test (BIST) patterns?

All of the HD test patterns are BIST data. For SD, the 270Mb/s NTSC colour bar and PAL PLL pathological test patterns are the test data.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Why is a "0" written instead when I try to write a "1" into a Control Register bit that is mapped as an input to the User I/O Port?

When configured (mapped) as an input to a Control Register bit, an unconnected I/O pin's internal pull-down overrides the data being written to that bit. Longer delay in the data path via the Ancillary/Control Port versus that from the I/O port makes this possible. When it is necessary to write data directly to a bit that has a corresponding input on the I/O Port, the I/O Port pin should be remapped to another control bit.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Why must ACLK be toggled three times after power-on reset or manual reset?

Toggling ACLK propagates the reset signal produced by the power-on reset or manual reset circuitry to the Ancillary/Control Port circuitry. This action completes the reset of the port and enables data transactions with the port.

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

What is the purpose of the FORMAT SET bits of the FORMAT 0 register for the LMH0030 or LMH0031?

The FORMAT SET bits are used to limit recognition and processing of the video data to only one of the fourteen SD or HD formats. These are listed in Table 4 of the respective datasheet for either the LMH0030 or LMH0031. Setting the format turns off the format recognition system and speeds format acquisition. The format will be reported in the FORMAT 1 register. Attempts to process video data of other formats will result in an error condition.

Relevant Part: CLC030; CLC031A; LMH0031; LMH0030

Some HD formats are described as 1080P/60 or 1080P/30. What is the difference? Do the LMH0030 and LMH0031 handle the higher frame rates?

There is a lot of confusion about how to refer to the eleven systems of 1125 line progressive scan formats in SMPTE 274M. This is probably because there are two different progressive format (P) scanning systems described in the same standard. Often, people either mix up these two systems or are not careful to be exact when referring to them. Regardless of which System is being described, all have 1920 active samples/line and 1080 active lines/frame, 1125 total lines.

The main differentiating factor for Systems 1-3 is the interface sampling frequency, 148.5MHz. Systems 1 through 3 use a 50Hz, 59.94Hz or 60Hz frame rate. These systems require a 60MHz transmission bandwidth. The LMH0030 and LMH0031 do not support this 148.5MHz interface sampling (i.e. Vclk) frequency.

Systems 4 through 11 require a 30MHz transmission bandwidth. They use a 74.25MHz (or 74.176MHz) interface sampling frequency. These Systems use a frame rate of 30Hz, 29.97Hz, 25Hz, 24Hz or 23.98Hz. The LMH0030 and LMH0031 support the 74.25MHz (74.176MHz) interface sampling (i.e. Vclk) frequency.

So, when speaking of a SMPTE 274M progressive format, be very careful to specify exactly the vertical scanning rate you mean. It can make a great deal of difference!

Relevant Part: CLC030; CLC031A; LMH0030; LMH0031

Can I include parallel ancillary data along with the parallel HD video data and will the LMH0030 serialize all of this data?

Ancillary (ANC) data may be included (embedded) in the proper locations in the applied parallel video data. The LMH0030 will serialize the combined ancillary and video data.

When the format is one of the supported HD formats, and CRC and Line Number insertion have not been defeated, the LMH0030 will insert these automatically. Line numbers and CRCs should not be included in the parallel data when using the normal format recognition capability of the part (default operation).

Relevant Part: CLC030; LMH0030

Can the LMH0030 and LMH0031 handle the progressive format segmented frame system described in SMPTE 274M, Annex A?

The progressive segmented frames (PsF) frames described in SMPTE 274M, Annex A, can be serialized (or deserialized) by the LMH0030. If the parallel input data to the LMH0030 is properly organized, it may be handled using the built-in automation of the LMH0030. The manner in which the PsF frames are defined in the standard specifies that they are to be handled as if they were interlaced frames. Before the LMH0030 can serialize the data, the 1125 line progressive picture must be externally organized into an interlaced format as described in Annex A. The progressive picture even-numbered lines map as interlaced lines 1 through 562 and the odd-numbered lines map as interlaced lines 563 through 1125. In both formats, the lines maintain consecutive numbers 1 to 1125. This means that the lines of the PsF raster will be given line numbers 1 through 1125 by the LMH0030, if the auto-line numbering is left enabled.

The PsF frames corresponding to SMPTE 274M, Annex A, Table A.1, numbers A through E, are equivalent to Table 1, system numbers 7 through 11, respectively. These should be handled by the LMH0030 as progressive frames.

The PsF formats correspond with the existing LMH0030 video raster formats as shown below. Refer to LMH0030 datasheet Table 4.

Table 1 LMH0030

System #	Format Code	PsF Equivalent
7	0x33	1920x1080/30/PsF
8	0x33	1920x1080/29.97/PsF
9	0x3A	1920x1080/25/PsF
10	0x3D	1920x1080/24/PsF
11	0x3D	1920x1080/23.98/PsF

After recovery of the data by the LMH0031, the interlaced format of the PsF frame can be converted back to the original progressive format, if needed.

Relevant Part: LMH0030; LMH0031; CLC030; CLC031A

Is the CLC030 the same as the LMH0030 and is the CLC031A the same as the LMH0031?

No, The LMH0030 is an upgrade to the CLC030.

Yes, the CLC031A is the same as the LMH0031.

Relevant Part: CLC030; LMH0030, CLC031A, LMH0031

IMPORTANT NOTICE