National Semiconductor
The Sight & Sound of Information

18-Bit SerDes Evaluation Kit

USER MANUAL

Part Number: LVDS-18B-EVK

January 2007
Rev 0.3

National Semiconductor Corporation
Interface Applications Group
18-Bit SerDes Evaluation Board User Manual

TABLE OF CONTENTS

1.0 Overview

The LVDS-18B-EVK is a complete kit for evaluation of National Semiconductor's 18-bit SerDes devices (DS92LV18 and SCAN921821) with low cost twisted pair cables as well as other 100-ohm differential cables.
The purpose of this document is to: familiarize you with the 18-Bit SerDes Evaluation Kit, suggest the test setup procedures and instrumentation, and to guide you through some typical measurements that will demonstrate the performance of the devices in typical applications.

2.0 Evaluation Kit Contents

- **18-Bit SerDes Evaluation Board** – The board features a single SCAN921821 and two DS92LV18 devices.
- **EVK User Manual (this document)**
- **EBLA**

3.0 Board Description

The Figure 1 below represents the top drawing of the board with the silkscreen annotations. It is a large 5 x 10 inch PCB that has a three-device layout capable of demonstrating the cable driving performance, control, and testability functions of the SCAN921821 and DS92LV18 devices.

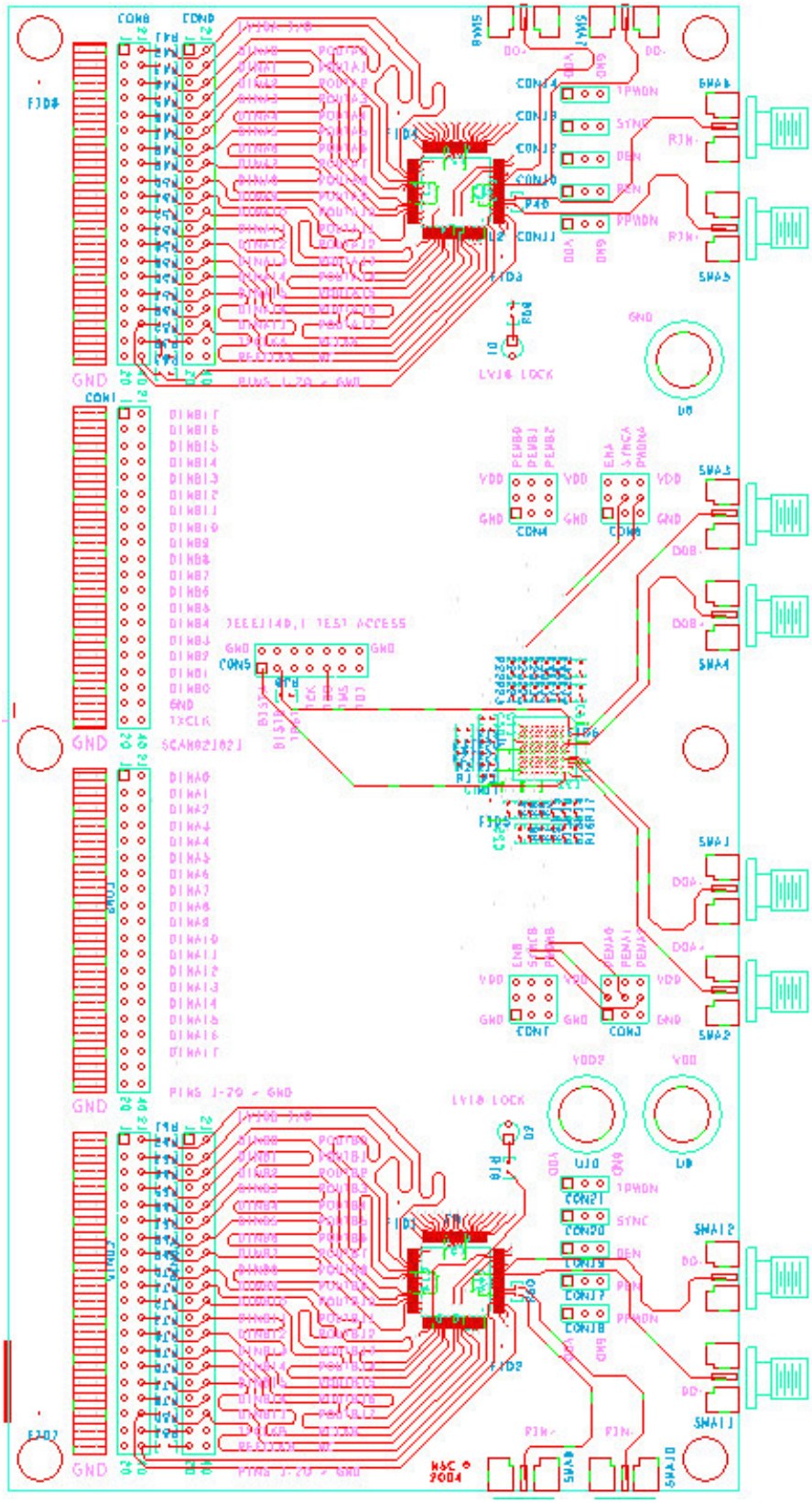


Figure 1: LVDS-18B-EVK Evaluation Board Top View

3.1 Traces

All LVDS inputs and outputs have been designed to maintain 100 ohms differential impedance from the SMA connector to the device inputs and outputs. A taper is used to minimize any discontinuity associated with the reduced trace separation near the device inputs. The traces have been routed for equal length between pairs.

The SCNA921821 input traces are 50 ohm single-ended. They have been routed to +/-250mils in length.

The DS92LV18 LVCMOS input and output traces have been designed as 60-ohm single-ended impedance. This impedance value is common in actual systems and is the result of using the same strip-line or micro-strip width as a 100-ohm differential pair. Without any coupling to an adjacent signal the single-ended impedance rises to about 60 ohms. For DS92LV18 designs, transmission line impedance should have a target range of 60-65 ohms.

3.2 Board Stack up

Figure 2 is a detailed drawing of the board cross-section showing the layers and layer spacing.

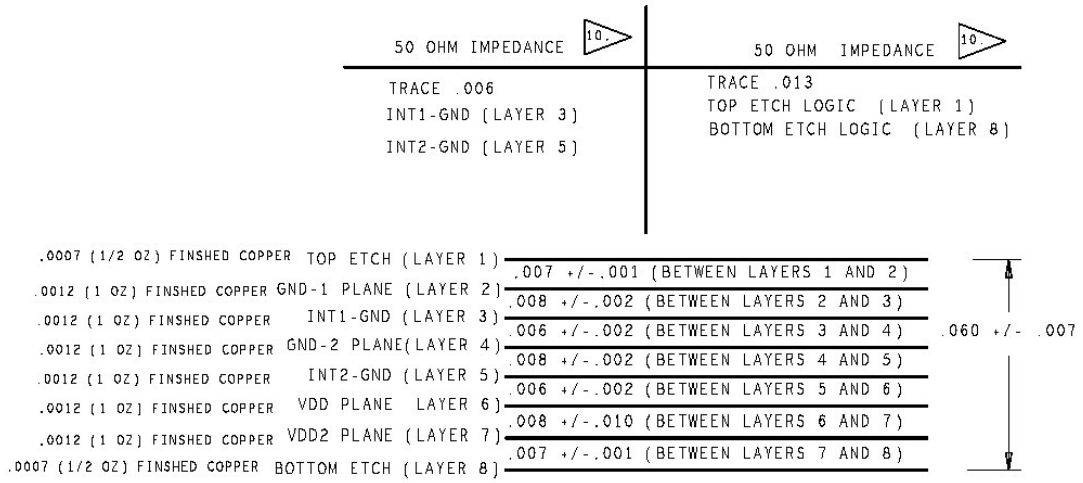


Figure 2: Board Stack up Detail

3.3 Power and Ground Rails

There are 3 separate VDD and Ground rails in the board stack up. The 3.3V VDD rail is used to supply power to the SCAN921821. A separate supply plane called VDD2 (also 3.3V) is used to supply power to the DS92LV18's on the board. The GND planes for both supply voltages are common across the board.

4.0 Test Configuration Examples with Typical Results

This section provides a quick reference for setting up some typical test configurations using the LVDS-18B-EVK that will enable you to evaluate the SCAN921821 and DS92LV18 as a standalone devices as well as a SerDes chipset in cable drive applications.

4.1 Configuration 1 – Evaluating the SCAN921821

The LVDS-18B-EVK can be used to evaluate the SCAN921821 as a standalone transmitter. In this case, a BERT receiver or an oscilloscope may be used to evaluate the transmitter output signals. Figure 3 is a simplified block diagram of the configuration.

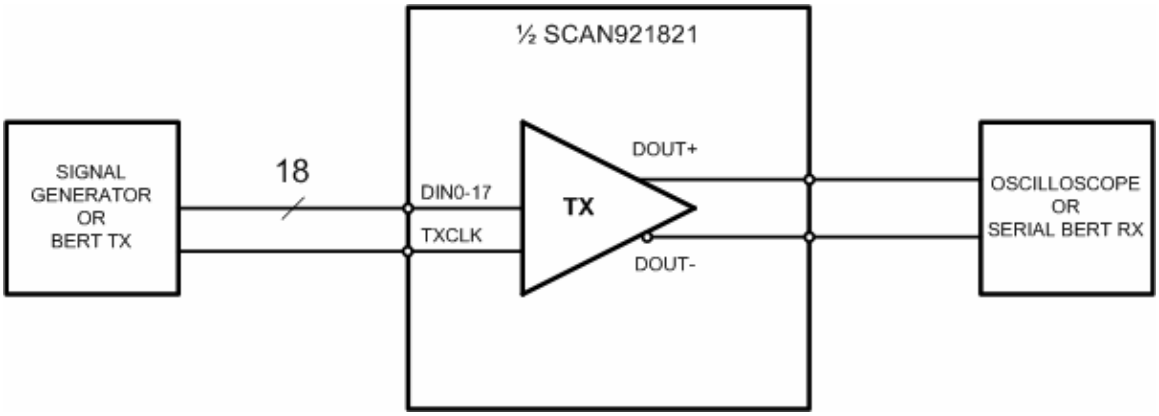


Figure 3. Test Setup for the SCAN921821 Only

You may follow these steps to set up the device for bench testing and performance measurements:

1. Provide 3.3 V between the U9 (VDD) and U8 (GND) banana jack receptacles. This will bring power to the SCAN921821 device only.
2. Power-up channel A or B of the device by setting the corresponding PWDN pin to high. This is accomplished by placing a jumper across VDD and PWDN pins on the connector CON6 for channel A, or CON7 for channel B.
3. Enable the outputs of channel A or B by setting the corresponding EN pin to high. This is accomplished by placing a jumper across VDD and EN pins on the connector CON6 for channel A, or CON7 for channel B.
4. Select pre-emphasis levels for the outputs of channel A or B by setting the corresponding PEM pins to high or low. This is accomplished by placing jumpers across VDD and PEM pins on the connector CON3 for channel A, or CON4 for channel B. As a reminder, the pre-emphasis has the lowest level when all three PEM pins are set to low, and it has the highest level when all three pins are set to high.
5. Disable PRBS generation of the outputs by placing jumpers across BIST and GND pins on the connector CON5.
6. Provide a 15-66 MHz TTL clock to the TXCLK pin (pin#40 of the connector CON1) from a signal generator.
7. Provide 18 bit TTL data signals to the transmitter inputs (DIN0-DIN17). For channels A and B of the device, the inputs are accessible through the connectors, CON1 and CON2, respectively. All data signals should be in phase and synchronous to the TXCLK.
8. Connect the outputs, DO+ and DO- (SMA1 and SMA2 for the channel A, and SMA3 and SMA4 for the channel B outputs) directly to an oscilloscope or a serial BERT receiver using coaxial cables. You may also use probes to sense the output signals, but first

make sure that the device has proper termination (usually 100 ohms between the output pins). The differential probes (>3GHz, <0.5pF) are recommended.

9. Observe the results on the oscilloscope or serial BERT receiver.

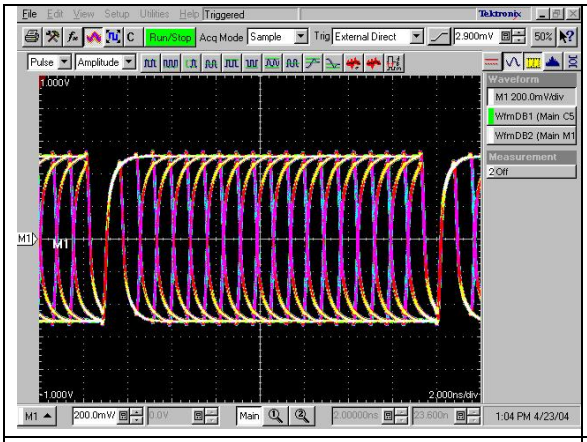
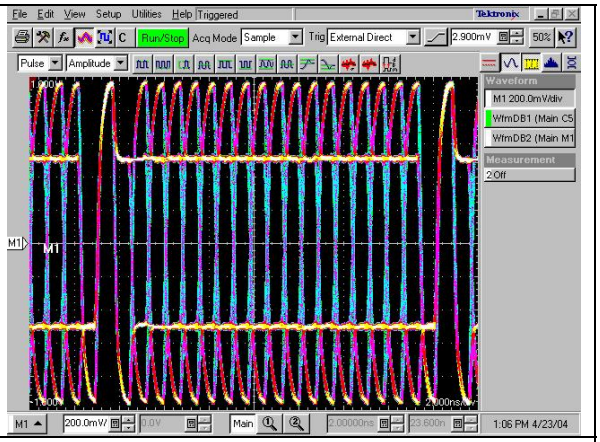
	
Measured by AC coupling SCAN921821 outputs directly to an oscilloscope; f_{TCLK} = 66 MHz; No Pre-emphasis;	Measured by AC-coupling SCAN921821 outputs directly to an oscilloscope; f_{TCLK} = 66 MHz; Max Pre-emphasis;

Table 1. Sample Results for the Configuration 1

4.2 Configuration 2 – Evaluating the DS92LV18

The LVDS-18B-EVK can also be used to evaluate the DS92LV18 in a typical cable drive application. In this case, a BERT analyzer or an oscilloscope may be used to evaluate the transmitter output signals. Figure 4 is a simplified block diagram of the configuration.

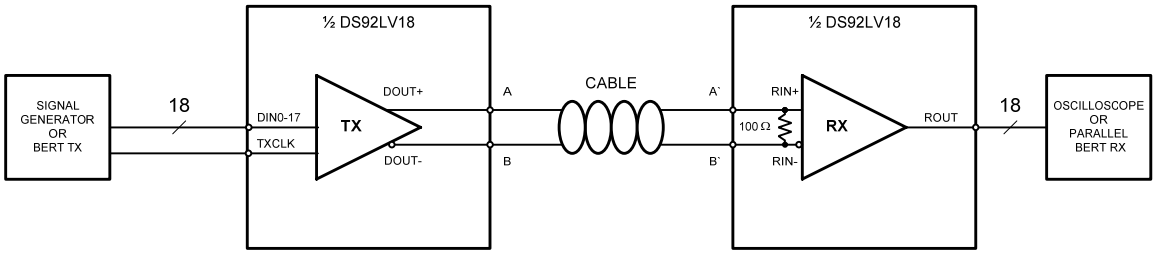


Figure 4. Test Setup for the SerDes Chipset Cable Drive Application

You may follow these steps to set up the devices for bench testing and performance measurements:

1. Provide 3.3 V between the U10 (VDD2) and U8 (GND) banana jack receptacles. This will bring power to both, A and B, DS92LV18 devices.
2. Configure the DS92LV18 device A or B as a transmitter as the following:

   a) Power-up the TX by setting the corresponding TPWDN pin to high. This is accomplished by placing a jumper across VDD and TPWDN pins on the connector CON14 for the device A (U2), or CON21 for the device B (U3).
   b) Enable the transmitter of the device A or B by setting the corresponding DEN pin to high. This is accomplished by placing a jumper across VDD and DEN pins on the connector CON12 for the device A (U2), or CON19 for the device B (U3).

c) Provide a 15-66 MHz TTL clock to the TXCLK pin (pin#39 of the connector CON8 for the device A (U2), or pin#39 of the connector CON15 for the device B (U3)) from a signal generator.

3. Configure the DS92LV18 device A or B as a single receiver as the following:

   a) Power-up the receiver by setting the corresponding RPWDN pin to high. This is accomplished by placing a jumper across VDD and RPWDN pins on the connector CON11 for the device A (U2), or CON18 for the device B (U3).
   b) Enable the receiver of the device A or B by setting the corresponding REN pin to high. This is accomplished by placing a jumper across VDD and REN pins on the connector CON10 for the device A (U2), or CON17 for the device B (U3).
   c) Provide a 15-66 MHz TTL clock to the REFCLK pin (pin#40 of the connector CON8 for the device A (U2), or pin#40 of the connector CON15 for the device B (U3)) from a signal generator. The clock frequency must be within 5% of the frequency provided to the TCLK pin of the transmitter.

4. Connect a cable assembly between transmitter outputs and receiver inputs.
5. Connect the outputs, ROUT0-17 and RCLK (pins 20-40 on the CON9 for the device A (U2), or pins 20-40 on the CON16 for the device B (U3)) directly to an oscilloscope or a BERT receiver using coaxial cables. You may also use probes to sense the output signals, but first make sure that the device has proper termination (usually 50 ohms to GND). The differential probes (>3GHz, <0.5pF) are recommended.
6. Observe the results on the oscilloscope or parallel BERT receiver.

4.3 Configuration 3 – Evaluating the SCAN921821 with the DS92LV18 Receiver

The LVDS-18B-EVK can also be used to evaluate the SCAN921821 together with the DS92LV18 receiver in a typical cable drive application. In this case, a BERT receiver or an oscilloscope may be used to evaluate the transmitter output signals. Figure 5 is a simplified block diagram of the configuration.

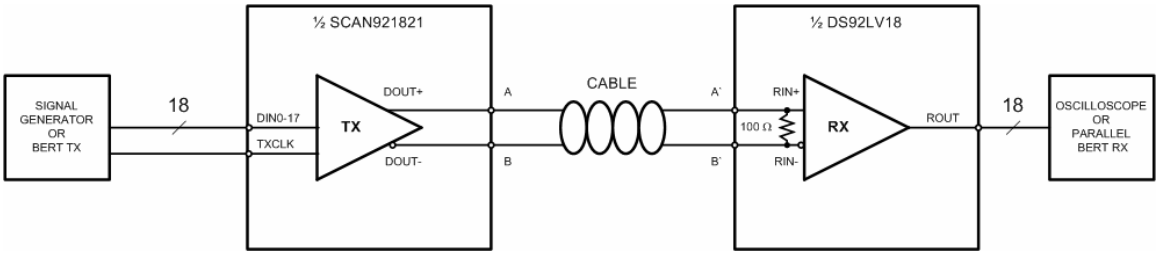


Figure 5. Test Setup for the SerDes Chipset Cable Drive Application

You may follow these steps to set up the devices for bench testing and performance measurements:

1. Provide 3.3 V between the U9 (VDD) and U8 (GND) as well as between the U10 (VDD2) and U8 (GND) banana jack receptacles. This will bring power to all devices on the board.

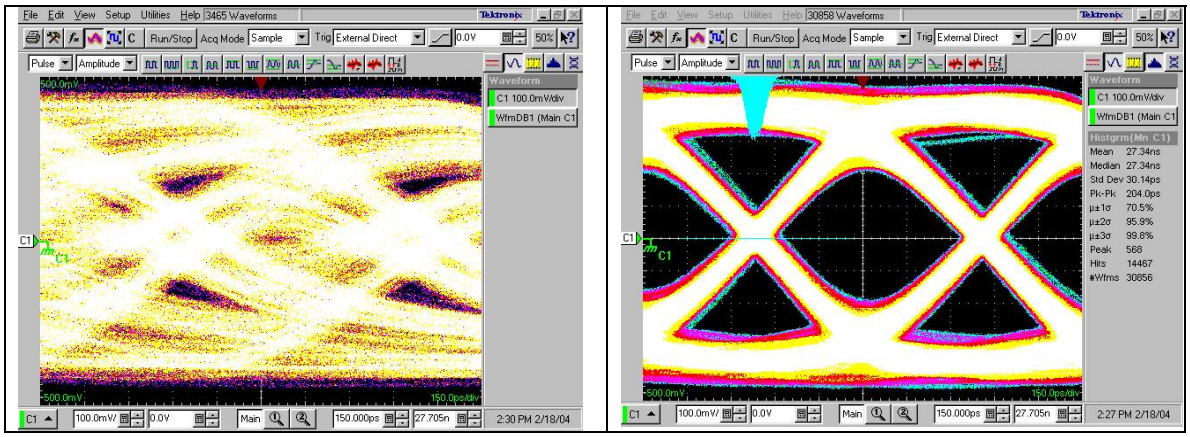
2. Configure the SCAN921821 as a single transmitter as the following:

a) Power-up channel A or B by setting the corresponding PWDN pin to high. This is accomplished by placing a jumper across VDD and PWDN pins on the connector CON6 for channel A, or CON7 for channel B.
b) Enable the outputs of channel A or B by setting the corresponding EN pin to high. This is accomplished by placing a jumper across VDD and EN pins on the connector CON6 for channel A, or CON7 for channel B.
c) Select pre-emphasis levels for the outputs of channel A or B by setting the corresponding PEM pins to high or low. This is accomplished by placing jumpers across VDD and PEM pins on the connector CON3 for channel A, or CON4 for channel B. As a reminder, the pre-emphasis has the lowest level when all three PEM pins are set to low, and it has the highest level when all three pins are set to high.
d) Disable PRBS generation of the outputs by placing jumpers across BIST and GND pins on the connector CON5.
e) Provide a 15-66 MHz TTL clock to the TXCLK pin (pin#40 of the connector CON1) from a signal generator.
f) Provide 18 bit TTL data signals to the transmitter inputs (DIN0-DIN17). For channels A and B of the device, the inputs are accessible through the connectors, CON1 and CON2, respectively. All data signals should be in phase and synchronous to the TXCLK.

3. Configure the DS92LV18 device A or B as a single receiver as the following:

g) Power-up the receiver by setting the corresponding RPWDN pin to high. This is accomplished by placing a jumper across VDD and RPWDN pins on the connector CON11 for the device A (U2), or CON18 for the device B (U3).
h) Enable the receiver of the device A or B by setting the corresponding REN pin to high. This is accomplished by placing a jumper across VDD and REN pins on the connector CON10 for the device A (U2), or CON17 for the device B (U3).
i) Provide a 15-66 MHz TTL clock to the REFCLK pin (pin#40 of the connector CON8 for the device A (U2), or pin#40 of the connector CON15 for the device B (U3)) from a signal generator. The clock frequency must be within 5% of the frequency provided to the TCLK pin of the transmitter.

4. Connect a cable assembly between the transmitter and the receiver.
5. Connect the outputs, ROUT0-17 and RCLK (pins 20-40 on the CON9 for the device A (U2), or pins 20-40 on the CON16 for the device B (U3)) directly to an oscilloscope or a BERT receiver using coaxial cables. You may also use probes to sense the output signals, but first make sure that the device has proper termination (usually 50 ohms to GND). The differential probes (>3GHz, <0.5pF) are recommended.
6. Observe the results on the oscilloscope or parallel BERT receiver.



Measured with Tektronix P6330 Differential probe after 15m of UTP Cable at the Input of the DS92LV18 Receiver; f_{TCLK} = 66 MHz; No Pre-emphasis;	Measured with Tektronix P6330 Differential probe after 15m of UTP Cable at the Input of the DS92LV18 Receiver; f_{TCLK} = 66 MHz; Max Pre-emphasis;

Table 2. Sample Results for the Configuration 2

7. If parallel BERT receiver is not available, you can utilize the DS92LV18 transmitter, TX, to deserializer the data, and than connect the TX outputs to the serial BERT receiver using coaxial cables. On the board, you can conveniently connect the ROUT0-17 outputs of the DS92LV18 RX and to the DS92LV18 TX inputs, DIN0-17 (pins 21-38 on the connectors CON8 and CON9 for the device A (U2) or on the connectors CON15 and CON16 for the device B (U3)), by simply placing 0 ohm SM0603 chip resistors on the resistor pads R41-R58 or R61-R78. Figure 6 is a simplified block diagram of the configuration.

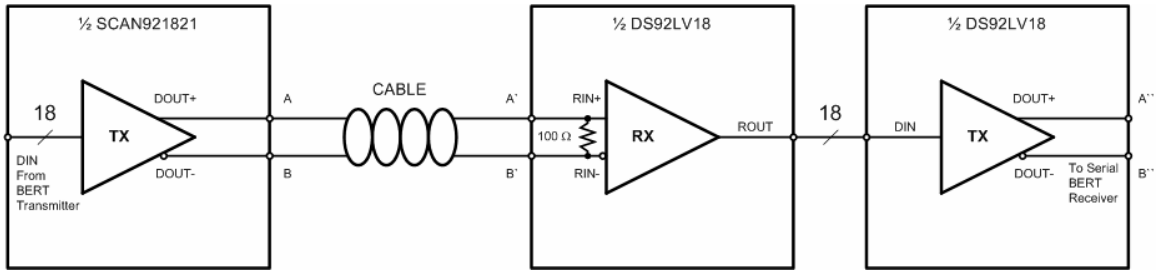
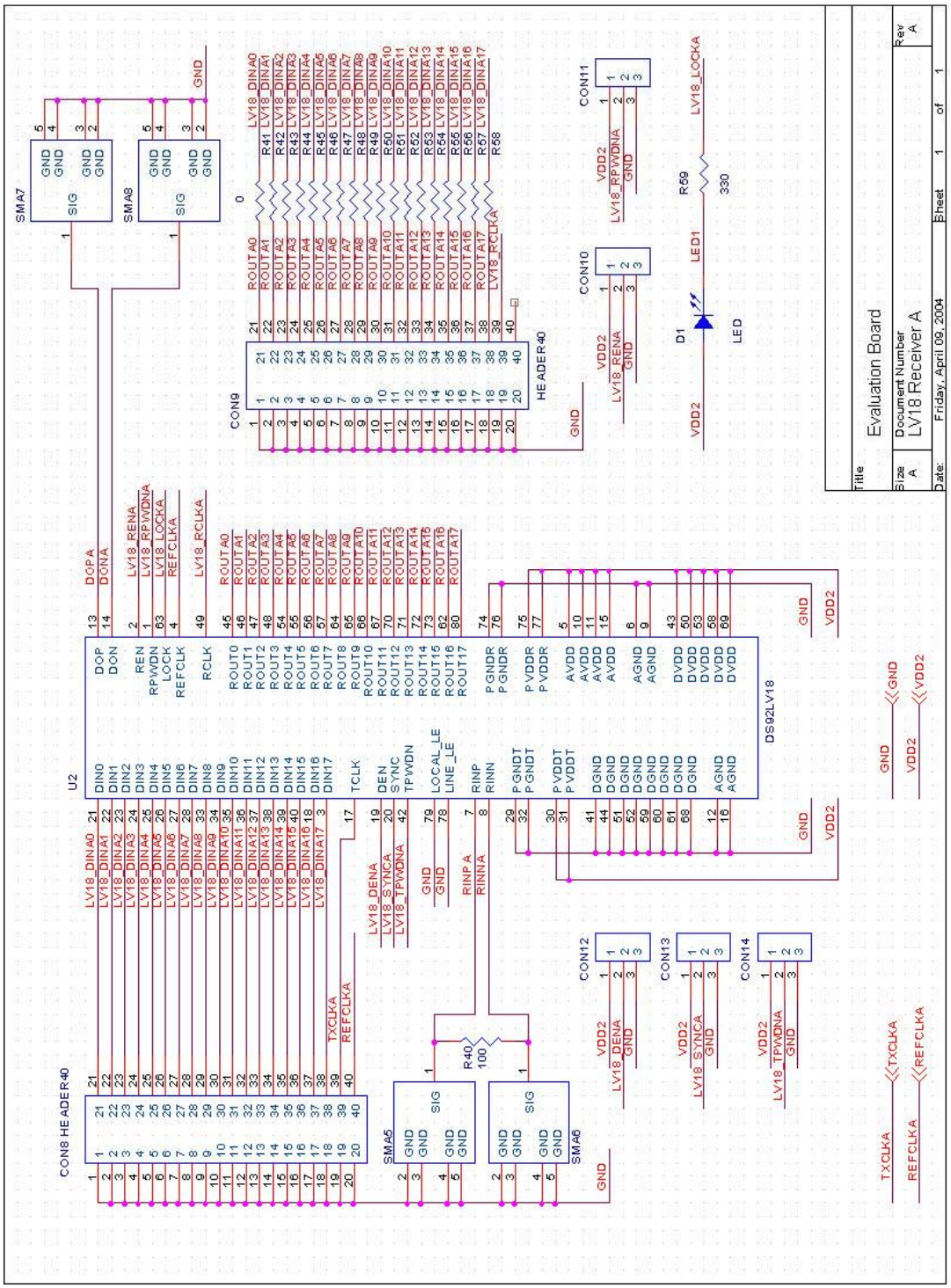


Figure 6. Test Setup for the SerDes Chipset Cable Drive Application

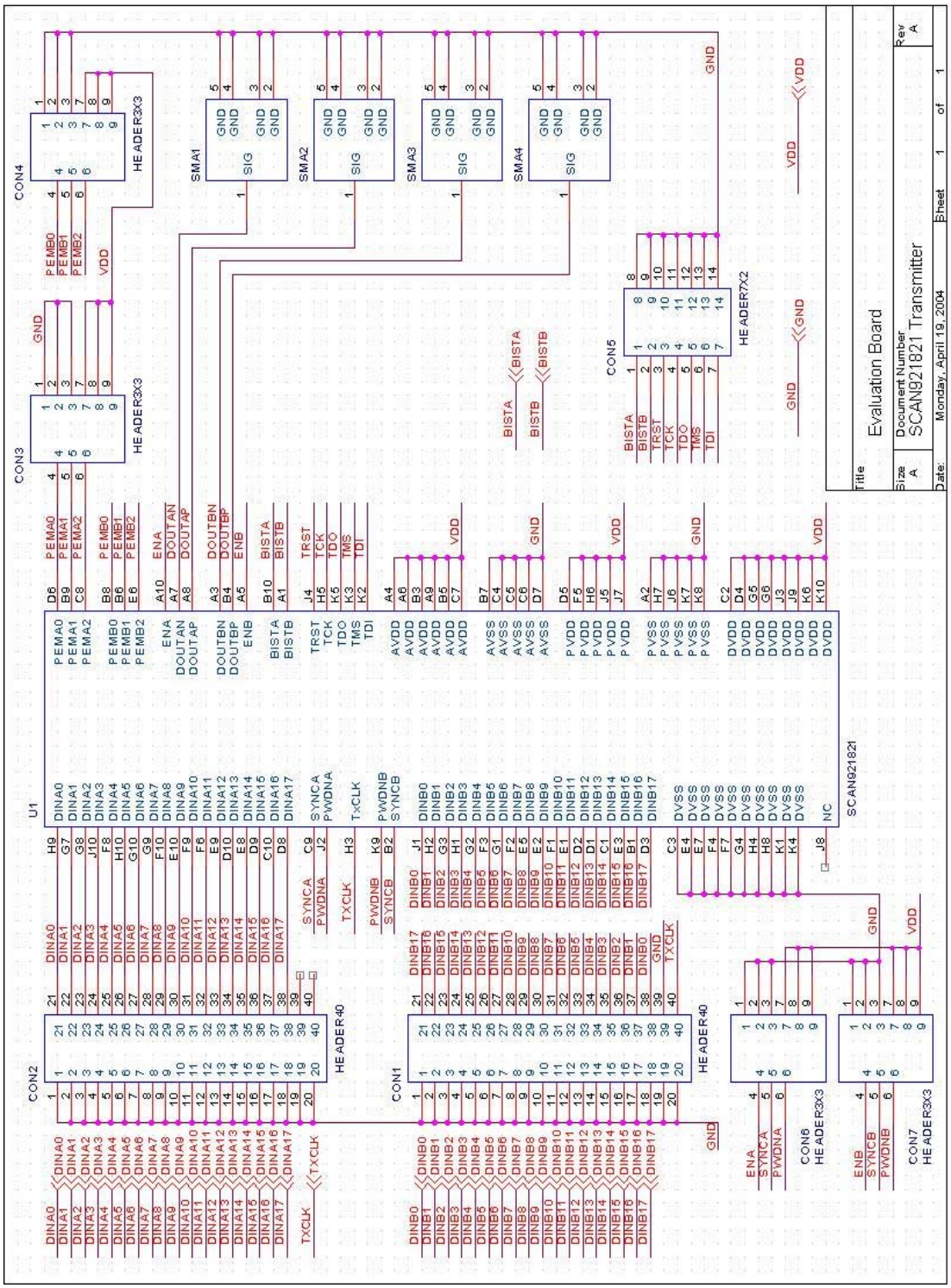
8. Configure the DS92LV18 device A or B as a transmitter as the following:

   j) Power-up the TX by setting the corresponding TPWDN pin to high. This is accomplished by placing a jumper across VDD and TPWDN pins on the connector CON14 for the device A (U2), or CON21 for the device B (U3).
   k) Enable the transmitter of the device A or B by setting the corresponding DEN pin to high. This is accomplished by placing a jumper across VDD and DEN pins on the connector CON12 for the device A (U2), or CON19 for the device B (U3).
   l) Provide a 15-66 MHz TTL clock to the TXCLK pin (pin#39 of the connector CON8 for the device A (U2), or pin#39 of the connector CON15 for the device B (U3)) from a signal generator. The clock frequency must have the same frequency as the clock provided to the TXCLK pin of the SCAN921821 transmitter.
   m) Connect the outputs, DO+ and DO- (SMA7 and SMA8 for the device A (U2), and SMA11 and SMA12 for the channel B outputs) directly to an oscilloscope or a serial BERT receiver using coaxial cables. You may also use probes to sense the output signals, but first make sure that the device has proper termination (usually 100 ohms between the output pins). The differential probes (>3GHz, <0.5pF) are recommended.
   n) Observe the results on the oscilloscope or serial BERT receiver.

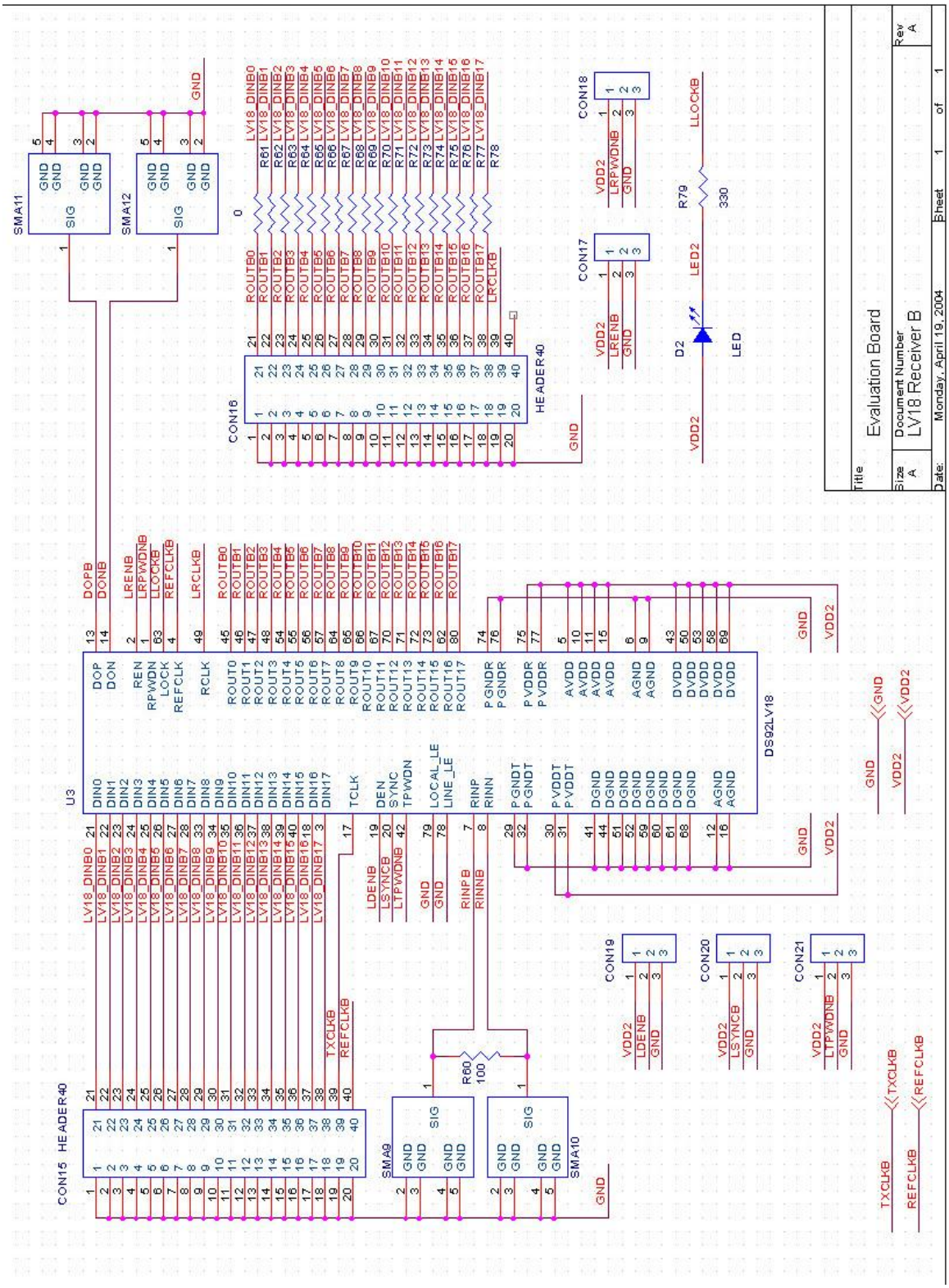
5.0 18-Bit SerDes Evaluation Board Schematic



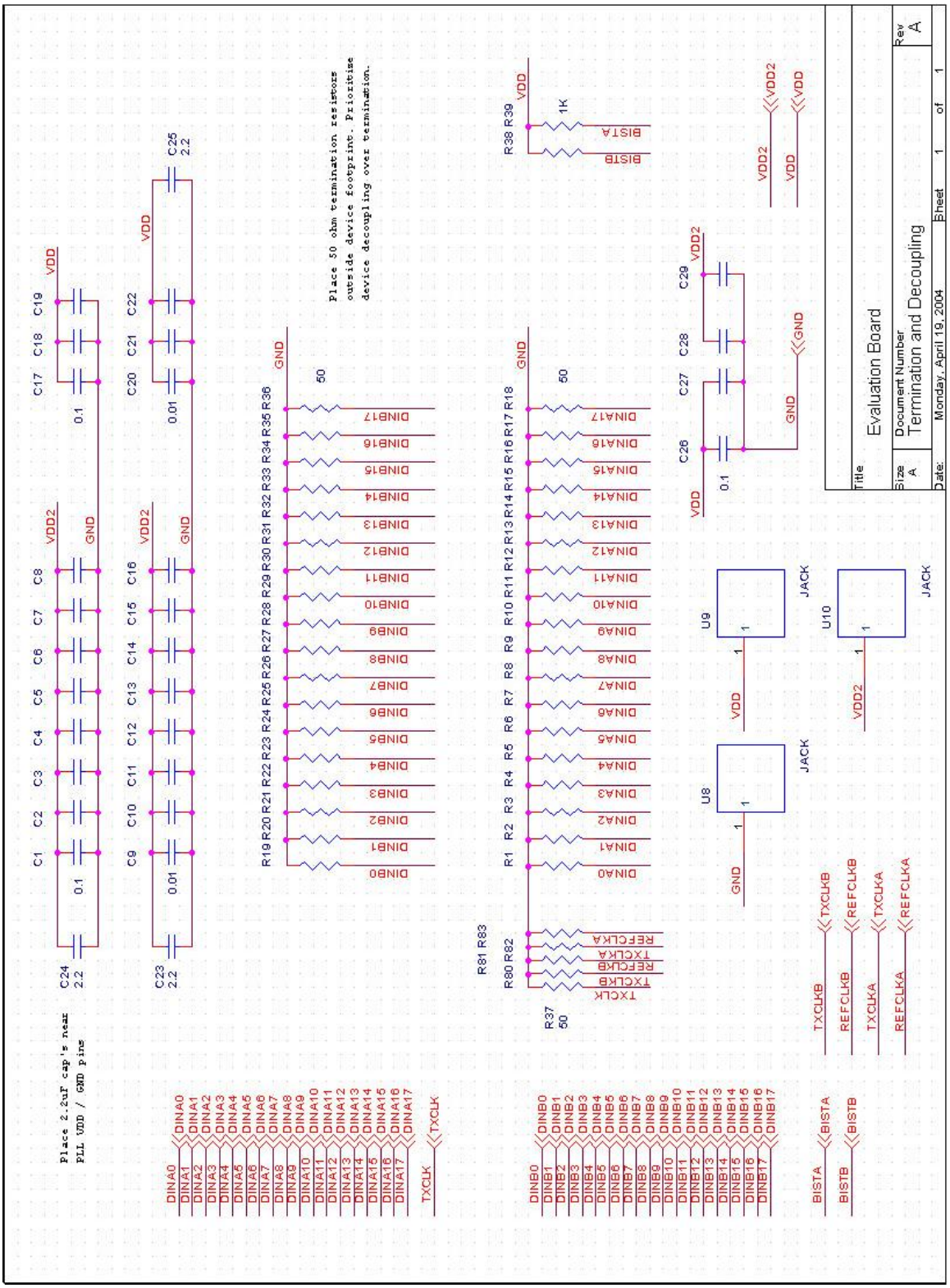
5.1 18-Bit SerDes Evaluation Board Schematic (cont.)



5.2 18-Bit SerDes Evaluation Board Schematic (cont.)



5.3 18-Bit SerDes Evaluation Board Schematic (cont.)



6.0 Bill of Materials:

18-Bit SerDes Evaluation Board Revised: Friday, August 6, 2004
Revision: A2

Bill Of Materials August 06, 2004 14:00:00 Page1

Item	Quantity	Reference		Part
1	6	CON1,CON2,CON8,CON9, CON15,CON16		HEADER40
2	4	CON3,CON4,CON6,CON7		HEADER3X3
3	1	CON5		HEADER7X2
4	10	CON10,CON11,CON12,CON13, CON14,CON17,CON18,CON19, CON20,CON21		HEADER3X1
5	13	C1,C2,C3,C4,C5,C6,C7,C8, C17,C18,C19,C26,C29	0.1uF	
6	11	C9,C10,C11,C12,C13,C14, C15,C16,C20,C21,C22		0.01uF
7	3	C23,C24,C25		2.2uF
8	2	C27,C28		22uF
9	2	D1,D2		LED
10	41	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31,R32, R33,R34,R35,R36,R37,R80, R81,R82,R83	50	
11	1	R38		1K
12	1	R39		10K
13	2	R40,R60		100
14	36	R41,R42,R43,R44,R45,R46, R47,R48,R49,R50,R51,R52, R53,R54,R55,R56,R57,R58, R61,R62,R63,R64,R65,R66, R67,R68,R69,R70,R71,R72, R73,R74,R75,R76,R77,R78	0	
15	2	R59,R79		330
16	12	SMA1,SMA2,SMA3,SMA4,SMA5, SMA6,SMA7,SMA8,SMA9, SMA10,SMA11,SMA12		SMAedge
17	1	U1		SCAN921821
18	2	U2,U3		DS92LV18
19	3	U8,U9,U10		JACK

6.1 Bill of Materials: (cont.)

18-Bit SerDes Evaluation Board Revised: Friday, August 6, 2004
Revision: A2

Bill Of Materials August 06, 2004 14:00:00 Page2

Part	Quantity	Order Info	Description
HEADER40	6	Digikey - Molex	WM6840-ND
HEADER3X3	4	Digikey – Molex	WM6703-ND (3 per Header)
HEADER7X2	1	Digikey – Molex	WM6814-ND
HEADER3X1	10	Digikey – Molex	WM6703-ND
0.1uF	13	Digikey	0603 package
0.01uF	11	Digikey	0603 package
2.2uF	3	Digikey	1206 package
22uF	2	Digikey	7343 package
LED	2	Digikey	67-1098-ND
50 ohm	41	Digikey	0402 package
1K	1	Digikey	0603 package
10K	1	Digikey	0603 package
100 ohm	2	Digikey	0402 package
0 ohm	36	Digikey	0603 package
330 ohm	2	Digikey	0603 package
SMAedge	12	Newark Electronics	16F3627
SCAN921821	1	National Semiconductor	
DS92LV18	2	National Semiconductor	
JACK	3	Newark Electronics	50F1460

ALL Resistors are +\- 5%
ALL Capacitors are +\- 20%

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated