LM10

National Semiconductor Develops New Complementary Bipolar Process For High Speed, High Performance Analog

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Technology Edge

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Today the market for high speed analog ICs is growing rapidly due to the ever-increasing demand for bandwidth. These ICs are finding applications such as xDSL and cable modems, set-top boxes, contact image scanners, DVD players and CD-ROMs. For portable, battery-powered and USB applications, power consumption must be low. In many of these designs, single-supply operation at 5V or 3V is preferred. National Semiconductor has developed its VIP10™ process in order to serve these markets.

VIP10 is the latest member of National's VIP™ (Vertically Integrated PNP) family of complementary bipolar processes, starting with VIP1 in 1986. It is a significant advancement of National Semiconductor's complementary bipolar process capabilities (see Table 1). Complementary bipolar transistor designs, by using high-performance NPN and PNP transistors, can offer the best combinations of features required in today's high speed amplifiers: high bandwidth, low power consumption, low supply voltages, large output swing, high output current and low distortion. In March 2001, National launched its LMH™ (Linear Monolithic High-Speed) family of high speed amplifiers designed on the VIP10 process.

TABLE 1: NATIONAL SEMICONDUCTOR COMPLEMENTARY BIPOLAR PROCESSES

Process	VIP1	VIP2	VIP3	VIP10	Units
Year	1986	1988	1994	2000	
NPN F_t	0.4	0.8	3.0	9.0	GHz
NPN β	250	250	150	100	
NPN V_a	200	150	150	120	V
PNP F_t	0.2	0.5	1.6	8.0	GHz
PNP β	150	80	60	55	
PNP V_a	60	40	50	40	V
Cjs	2.0	1.5	0.5	0.005	pF
Emitter Width	15	11	2	1	µm
Minimum Transistor Area	20000	18000	2400	300	μm^2
Max Supply V	36	36	32	12	V
Isolation	JI	JI	JI	DI	
Other	Implanted Emitter, Base	Implanted Emitter, Base	Poly Emitter	Double Poly	

Why Complementary Bipolar

Just as complementary MOS (CMOS) processes incorporate NMOS and PMOS field-effect transistors, complementary bipolar (CB) processes incorporate NPN and PNP bipolar junction transistors. CMOS is ubiquitous today because CMOS logic gates dissipate no static power yet have high drive current and speed. In a similar fashion, CB processes enable class AB output stages with very low quiescent current and high output drive in analog circuits.

Furthermore CB processes permit high-swing complementary common-emitter output stages, commonly known as "rail-to-rail outputs." On some processes, these output stages can be a challenge to design with well-controlled frequency and time-domain responses as the output transistors vary from quiescent conditions to sinking or sourcing high currents to near saturation. of the output transistors. Its low collector resistance and reduced quasi-saturation effects make VIP10 well suited for rail-to-rail output stages.

Low supply operation is increasing important today since many systems employing high-speed analog circuits employ only a single supply voltage such as 5V or 3V. The minimum supply voltage for bipolar designs is a forward base-emitter voltage plus a saturation voltage or approximately 1V. National Semiconductor's LM10 op amp/reference, introduced in 1978, operates down to a 1V supply. Since the LM10 was fabricated on a junction-isolated process lacking a high-performance PNP, its gain-bandwidth product is a low 100KHz. With VIP10, one could design an op amp with a 1V minimum supply voltage and a gain-bandwidth product about 1000x greater.

Rail-to-rail input stages can be designed on a CB process, by combining both PNP and NPN inputs stages. Other circuitry is required to steer current to the appropriate differential pair depending on the common-mode voltage and both stages usually require a folded-cascode to level shift. A CB process having high-performance BJTs of both types will ensure consistent performance stage when either input stage is active. Small device footprint reduces the die size required by this more complex circuit.

Advantages of CB over CMOS

The VIP10 process development had the goal of delivering the highest level of analog performance possible while minimizing wafer cost and development time. The performance benefits of complementary bipolar analog ICs can be seen in the analog circuits used in wired broadband applications such as xDSL and cable modems. The most critical analog blocks are the drivers and receivers. Receivers using low base-resistance BJTs can offer low input noise voltage with a much lower operating current and die area than CMOS designs, due to differences in device physics.

Line drivers must drive transmission-line loads to high power levels with low distortion. CB designs yield lower distortion than CMOS due to the higher transconductance of BJTs. Futhermore, the high gate capacitance of large MOSFETdevices would cause problems with stability or power dissipation. In practice, complementary bipolar designs are superior in combining low distortion, low power dissipation and frequency stability. The higher breakdown voltages achievable in high-speed BJTs gives CB line driver higher output swing.

In CMOS, the key dimension is the minimum channel length, which determines the power-delay product and the IC area. Reducing MOS channel length is expensive since it is set primarily by lithography. The analogous parameter for bipolar transistors is the vertical dimension of the active base region ("base width") , critical for determining current gain and transition frequency. These junction profiles are controlled by implantation and RTA. Since the minimum feature size for a BJT (usually the emitter stripe width) is less important than for CMOS, a high-performance CB process can be developed with a less investment of capital and time. VIP10's minimum emitter width is 1um, allowing it to be manufacturable at a low cost.

Process Architecture Minimizes Parasitic R and C for Higher Speed/Power Ratio

VIP10's excellent transistor performance stems from its advanced process architecture. See the VIP10 Transistor Cross-Section in **Figure 1.** The active area is Silicon-On-Insulator (SOI) which is fabricated using the bonded wafer technique. This produces a buried oxide layer which isolates the bottom of the epi tubs, which are usually the collectors of bipolar transistors. P and N type buried layers are followed by epi growth. Trenches are anisotropically etched into the silicon and filled to form the isolation sidewalls. Consequently the VIP10 transistor collectors are fully dielectrically isolated (DI) and have no P-N junction between the collectors and substrate or well. Previous generation processes were junction isolated (JI) so that the BJT collector-substrate capacitance (Cjs) was primarily a junction capacitance. Since junction capacitance varies with voltage, this caused undesirable variations in AC performance as supply voltage and output voltage are varied and increased distortion.

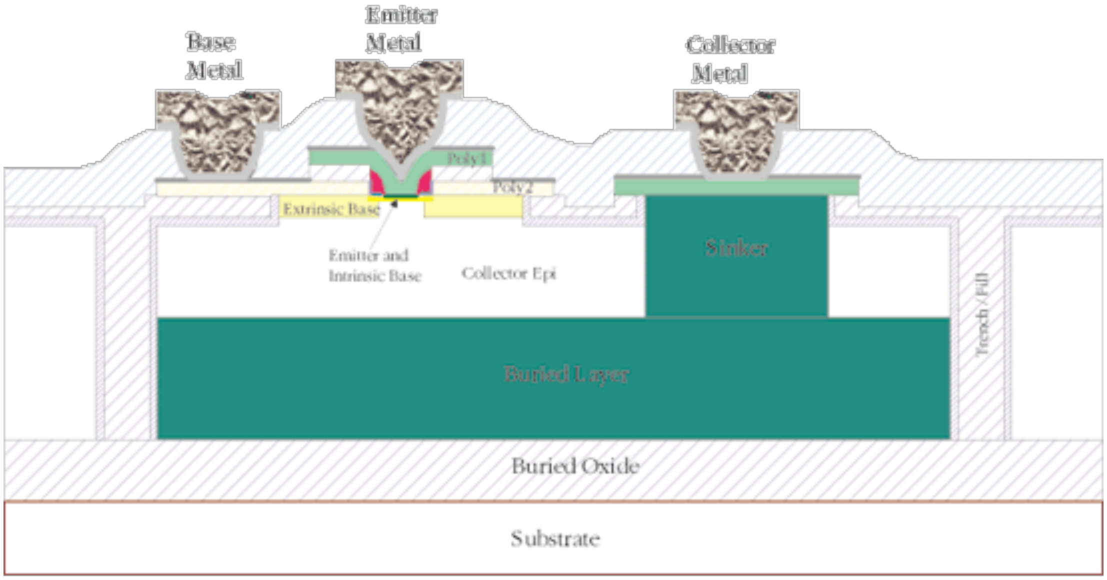

Figure 1: VIP10 Transistor Cross Section

Collector-substrate capacitance on a JI process is usually higher than on a DI process. High Cjs will either degrade amplifier frequency response or require increased quiescent current. The situation gets even worse for one transistor type on JI. National's VIP1, VIP2 and VIP3, like most bipolar processes, are fabricated on a p-type substrate wafer. In order to isolate the PNP transistor collectors from the substrate, an n-type buried isolation diffusion is employed. This n-type diffusion must be more highly doped than the p-substrate. This highly doped junction causes the Cjs of the PNP to be much higher than that of the NPN. On VIP10, thanks to its dielectric isolation, collector-substrate capacitance of the minimum devices is an extremely low 5 fF, independent of voltage and equal for both NPN and PNP.

The next parasitic capacitance to address is the collector-base or Cjc. Cjc is also critical in high speed designs. When referred to the input of a voltage gain stage, this capacitance will increase due to the Miller effect. In high speed transistors, a lightly doped intrinsic base is contacted by a highly doped extrinsic base diffusion. This extrinsic base region produces a large base sidewall capacitance. VIP10 eliminates this problem with dielectric isolation at the sidewalls. This is done with a shallow trench etch and fill rather than the using LOCOS oxidation, which could produce defects resulting in high leakage currents and poor analog circuit yield.

Two different polysilicon layers are used for emitter and base contacts. This permits the critical emitter and base regions to be self-aligned. A poly 1 region defines the extrinsic base region. A hole inside the poly 1 geometry is the emitter window and intrinsic base. The emitter is separated from the extrinsic base by a nitride spacer. The emitter is contacted by the Poly 2, allowing the base pickup to be very close to the emitter, reducing the extrinsic base resistance (Rbb'.) Both polysilicon layers are salicided, further reducing the parasitic resistances in series with emitter, base and collector.

The minimum VIP10 transistors have a very small 300um^2 footprint, 1/8 that of the previous generation. This is another benefit of the features just discussed. The double-poly architecture reduces spacing from the emitter to the base pickup compared to the conventional single-poly approach. The shallow trench isolation on the base sidewalls allows the collector pickup to be very close to the base without decreasing the breakdown voltage or increasing the capacitance. Finally, the trench isolation around the device drastically shrinks the area required for isolation

Transistor Characteristics for High Performance Circuits

The most common AC figure of merit for a bipolar transistor is the transition frequency or Ft., which is the frequency at which the common-emitter current gain decreases to unity. The Ft of the VIP10 NPN and PNP at Vce= 5V are 9GHz and 8GHz respectively, about 50% higher than on competitive processes. The transistor Ft being high means that its emitter-base diffusion capacitance will be low for a given operating point. With VIP10 transistors, National can design amplifiers either with bandwidths exceeding 1 GHz or with bandwidths in the 100MHz range with very low power consumption. This is because the internal stages will have low phase shifts even at very low operating currents, since both diffusion and parasitic capacitances have been greatly reduced. Ft can dramatically decrease at lower voltages on some bipolar process. But Ft's on VIP10 remain high at Vce=1V: 7GHz for the NPN and 5GHz for the PNP.

High-speed transistors tend to have poor DC performance, but this is not true for VIP10. Beta and Early voltage are 100 and 120V for the NPN and 55 and 40V for the PNP. A common DC figure of merit is beta multiplied times Early voltage which is related to the gain obtainable from a single amplifier stage. Due to the lower mobility of holes compared to electrons, PNP transistors have lower b *Va products than NPNs with comparable Fts and breakdown voltages. The VIP10 PNP has a b *Va product of 2200V, BVceo of 12V and Ft of 8GHz which is a world class combination for a complementary bipolar linear IC process.

Low current performance, sometimes a concern on high speed processes, is not an issue on VIP10. Transistor beta is very constant over more than 4 decades of collector current. Entire VIP10 operational amplifiers have been designed with supply currents below 10uA.

Future Directions

National is moving forward in process development and product development for high speed amplifiers. Increased integration capability will be added to the VIP10 process and new LMH designs will be released in the fall of 2001.