

LM2642 Evaluation Board Module User's Guide



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1 Introduction

The LM2642 evaluation board has been developed to aid in the design and evaluation of DC/DC converters based on the LM2642 controller IC. As shown in [Figure 3-1](#), the evaluation board is configured to provide two outputs of 2.5 V/2 A and 1.8 V/2 A from an input range of 4.5 V to 20 V. The corresponding bill of materials is given in [Table 3-1](#). [Figure 3-2](#) and [Figure 3-3](#) show the evaluation board layout.

2 Optional Components

The evaluation board provides several optional component pads for flexibility in changing components.

For more information regarding device operation and component selection, see the [LM26420/LM26420Q Dual 2.0A, High Frequency Synchronous Step-Down DC-DC Regulator Data Sheet](#).

In switching power supplies, the rapid increase of drain current in the top FET coupled with parasitic inductance generates unwanted $L\Delta i/\Delta t$ noise spikes at the source node of the FET (SWx node) and V_{IN} node.

The resistor in series with the SWx pin (**R6**, **R11**) slows down the gate drive (HDRVx), thus slowing the rise and fall time of the top FET, yielding a longer drain current transition time and reducing switch node ringing. Top FET switching losses will increase with higher resistance values. Small resistors (1 Ω –5 Ω) can also be placed in series with the CBOOTx pin (**R7**, **R12**). A CBOOT resistor will slow the rise time of the FET to reduce switch node ringing.

To maintain stable regulation, the FBx pins should remain free of noise. The LM2642 evaluation board has components **C15** and **C22** installed to suppress noise that may be picked up by the FBx traces. Notice that both of these capacitors are placed physically close to the FBx nodes. Pads **C17** and **C23** are provided for additional output capacitors.

3 Powering Up

Before powering up the LM2642 evaluation board, all external connections should be verified. The power supply input must be turned off and connected with proper polarity to the VIN post, also marked as **P1**. The channel 1 and channel 2 loads should be connected at the V_{OUT} posts, marked as **P2** and **P3**. Any type of load is acceptable up to 2 A. The load can be on or off at start-up. Output voltage can be monitored with a DVM or oscilloscope by connecting probes to the V_{OUT} posts, P2 and P3. The GND posts are provided primarily for scope probe ground connections. The PGOOD signal can be monitored with a scope probe or DVM at the **PGOOD** test pin.

Once all connections have been verified, input power can be applied. The input voltage must be set between 4.5 V and 20 V. The enable switches for each channel, **ON1** and **ON2**, can be used to turn on the evaluation board once the input power is on. Each channel can be enabled or disabled independently. The switches can also be left on for enabling the evaluation board directly from the power supply input.

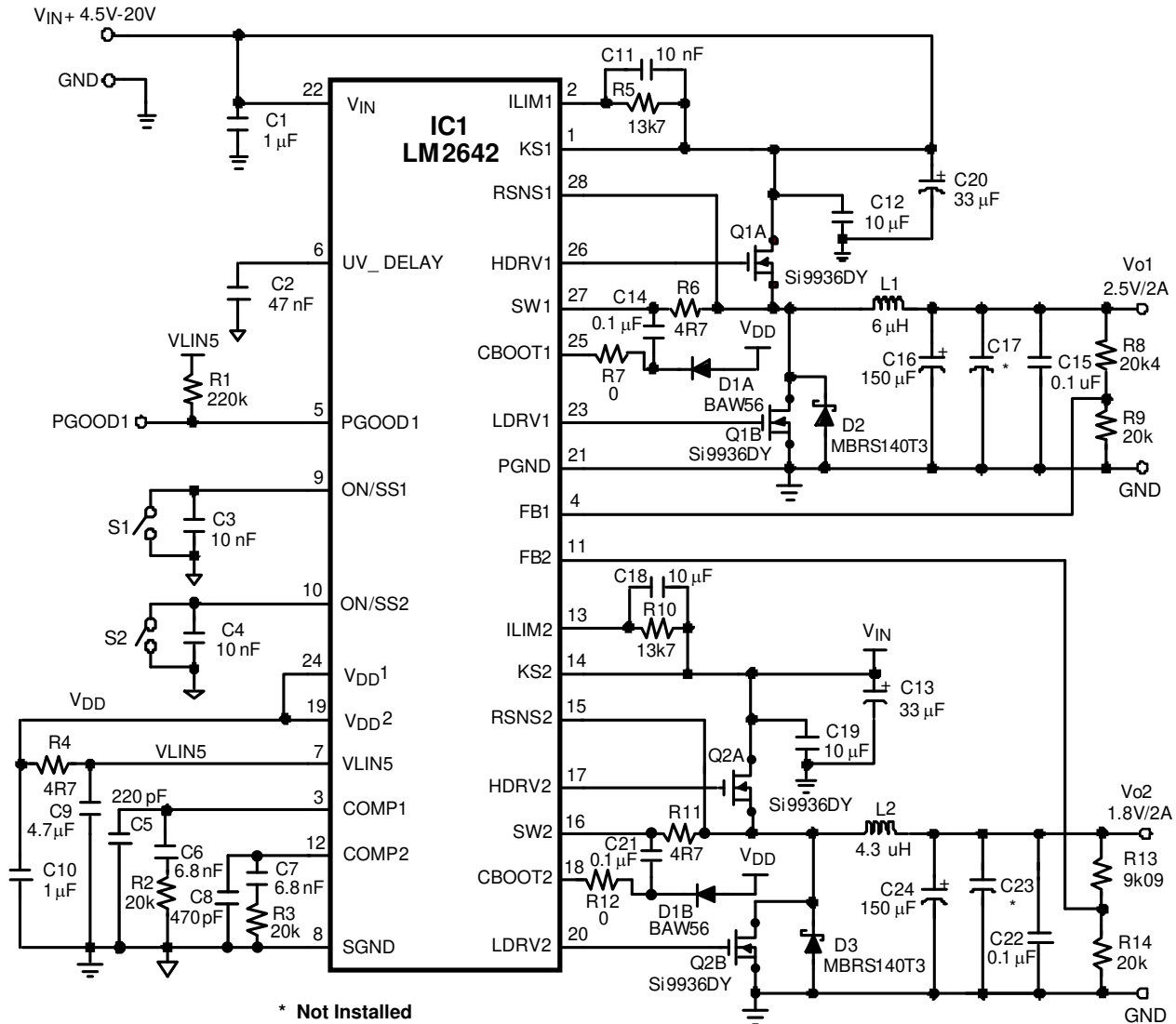


Figure 3-1. Complete Evaluation Board Schematic

Table 3-1. Bill of Materials

| Part # | Value | Supplier |
|--------|-----------------------------|--------------------------|
| C1 | Cer Cap 1 F 50 V Y5V 0805 | Taiyo Yuden UMK212F105ZG |
| C2 | Cer Cap 47 nF 50 V 10% 0805 | Vishay VJ0805Y473KXA |
| C3 | Cer Cap 10 nF 50 V 10% 0805 | Vishay VJ0805Y103KXA |

Table 3-1. Bill of Materials (continued)

| Part # | Value | Supplier |
|--------|---|------------------------------|
| C4 | Cer Cap 10 nF 50 V 10% 0805 | Vishay VJ0805Y103KXA |
| C5 | Cer Cap 220 pF 25 V 10% 0805 | Vishay VJ0805Y221KXA |
| C6 | Cer Cap 6.8 nF 50 V 10% 0805 | Vishay VJ0805Y682KXA |
| C7 | Cer Cap 6.8 nF 50 V 10% 0805 | Vishay VJ0805Y682KXA |
| C8 | Cer Cap 470 pF 25 V 10% 0805 | Vishay VJ0805Y471KXA |
| C9 | Cer Cap 4.7 μ F 10 V X7R 1206 | Taiyo Yuden LMK316BJ475ML |
| C10 | Cer Cap 1 μ F 10 V X7R 0805 | Taiyo Yuden LMK212BJ105ZG |
| C11 | Cer Cap 10 nF 50 V 10% 0805 | Vishay VJ0805Y103KXA |
| C12 | Cer Cap 10 μ F 35 V Y5V 1210 | Taiyo Yuden GMK325F106ZH |
| C13 | Electro Cap 33 μ F 50 V | Panasonic EEU-FC1H330 |
| C14 | Cer Cap 0.1 μ F 50 V 10% 0805 | Vishay VJ0805Y104KXA |
| C15 | Cer Cap 0.1 μ F 50 V 10% 0805 | Vishay VJ0805Y104KXA |
| C16 | Cap-SP 150 μ F 6.3 V 20% | Panasonic EEFUEOJ151R |
| C17 | Not Installed | |
| C18 | Cer Cap 10 nF 50 V 10% 0805 | Vishay VJ0805Y103KXA |
| C19 | Cer Cap 10 μ F 35 V Y5V 1210 | Taiyo Yuden GMK325F106ZH |
| C20 | Electro Cap 33 μ F 50 V | Panasonic EEU-FC1H330 |
| C21 | Cer Cap 0.1 μ F 50 V 10% 0805 | Vishay VJ0805Y104KXA |
| C22 | Cer Cap 0.1 μ F 50 V 10% 0805 | Vishay VJ0805Y104KXA |
| C23 | Not Installed | |
| C24 | Cap-SP 150 μ F 6.3 V 20% | Panasonic EEFUEOJ151R |
| D1 | Switching Diode-Dual 70 V 200 mA BAW56F | Fairchild BAW56F |
| D2 | Schottky Diode 40 V 1A | On Semiconductor MBRS140T31A |
| D3 | Schottky Diode 40 V 1A | On Semiconductor MBRS140T31A |
| L1 | Inductor 6 μ H | Sumida CEP125-6R0MC |
| L2 | Inductor 4.3 μ H | Sumida CEP125-4R3MC |
| Q1 | Si9936DY | Vishay |
| Q2 | Si9936DY | Vishay |
| R1 | Res 220 k Ω 0.1W 5% 0805 | Vishay CRCW0805224J |
| R2 | Res 20 k Ω 0.1W 5% 0805 | Vishay CRCW0805203J |
| R3 | Res 20 k Ω 0.1W 5% 0805 | Vishay CRCW0805203J |
| R4 | Res 4.7 Ω 0.1W 5% 0805 | Vishay CRCW08054R7J |
| R5 | Res 13.7 k Ω 0.1W 1% 0805 | Vishay CRCW08051372F |
| R6 | Res 4.7 Ω 0.1W 5% 0805 | Vishay CRCW08054R7J |
| R7 | Res 0 Ω 0.1W 5% 0805 | Vishay CRCW08050RJ |
| R8 | Res 20.5 k Ω 0.1W 1% 0805 | Vishay CRCW08052052F |
| R9 | Res 20 k Ω 0.1W 1% 0805 | Vishay CRCW08052002F |
| R10 | Res 13.7 k Ω 0.1W 1% 0805 | Vishay CRCW08051372F |
| R11 | Res 4.7 Ω 0.1W 5% 0805 | Vishay CRCW08054R7J |
| R12 | Res 0 Ω 0.1W 5% 0805 | Vishay CRCW08050RJ |
| R13 | Res 9.09 k Ω 0.1W 1% 0805 | Vishay CRCW08059092F |
| R14 | Res 20 k Ω 0.1W 1% 0805 | Vishay CRCW08052002F |
| S1 | Switch SPST 0.4VA 28 V AC/DC A12AB | NKK A12AB |
| S2 | Switch SPST 0.4VA 28 V AC/DC A12AB | NKK A12AB |

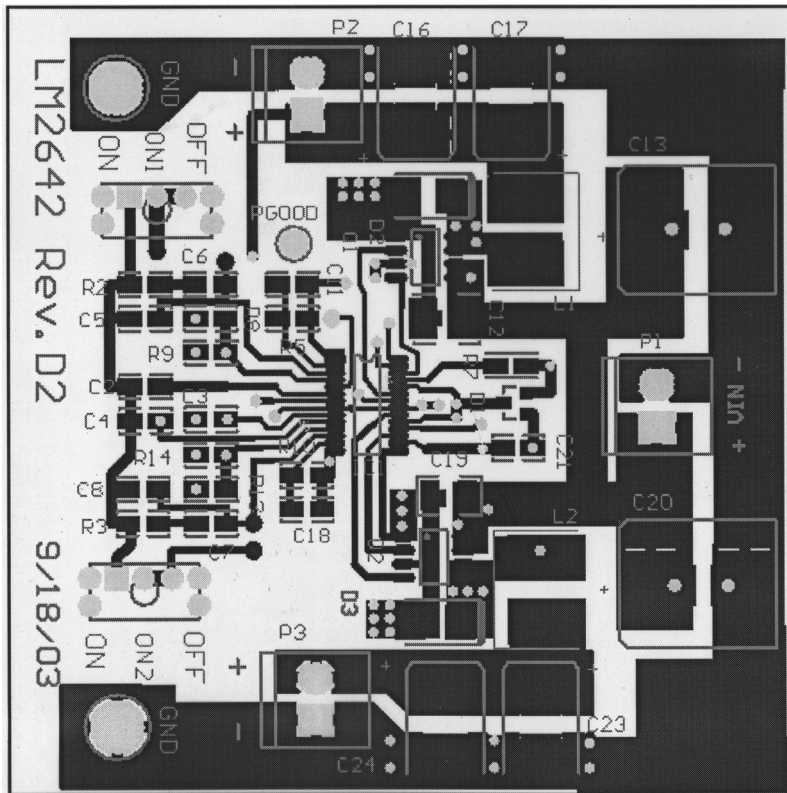


Figure 3-2. Top Layer

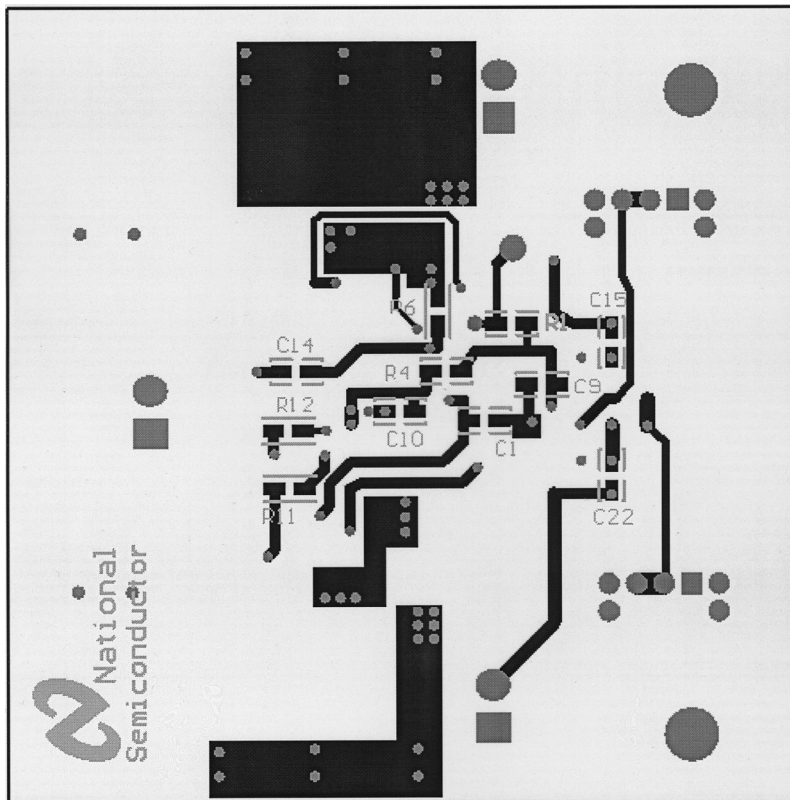


Figure 3-3. Bottom Layer

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision H (April 2013) to Revision I (January 2022) | Page |
|--|-------------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 2 |
| • Updated the user's guide title..... | 2 |

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