LM5039

Average Current Limit Balances Center Point of Half-Bridge Input Caps

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Average Current Limit Balances Center Point of Half-Bridge Input Caps

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Introduction

Power converters based on the half-bridge topology are widely employed in the power supply industry and are increasingly popular in telecom industry-standard quarter- and eighth-brick formats. The half-bridge topology offers high efficiency due to its transformer's double-ended nature and good power handling up to 500W. It has the least primary device ratings compared to any isolated topology. The half-bridge topology ideally requires only one-half the voltage ratings for its input capacitors when compared to a full bridge. However, during an extended overload condition, with traditional cycle-by-cycle current limiting, the center point of the half-bridge capacitive divider drifts either towards the input voltage or the ground. This leads to the saturation of the power transformer and requires the input capacitors to be rated to at least the input voltage.

From both performance and cost perspectives, these limitations are undesirable.

To overcome these limitations, average current limit is proposed. Average current limit balances the center point of the half-bridge capacitor divider and avoids its drift during an overload condition. Further, it does not alter the feed-forward voltage-mode control typically employed for the half bridge. It also retains the features of a standard current limit, such as cycle-by-cycle protection, fast response time during an overload event, and hiccup-mode restart.

Operation of a Half-Bridge Topology

A simplified schematic of a half-bridge topology is shown in ***Figure 1***. The input capacitors C1 and C2, which form one-half of the bridge, are arranged in series such that the mid-point is at half the input voltage.

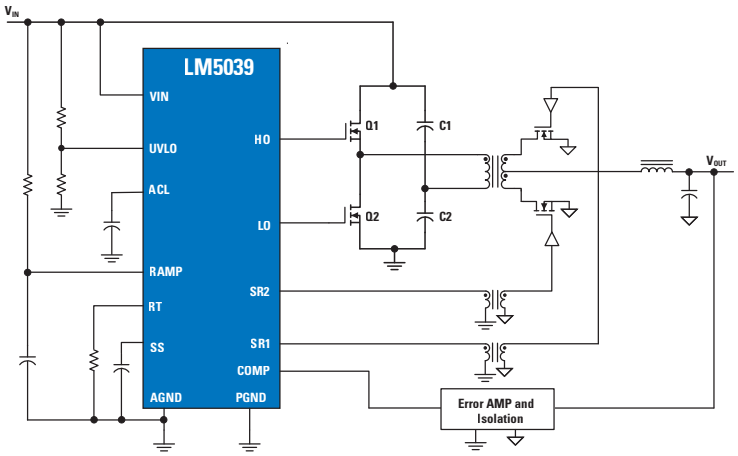

Figure 1. Simplified Schematic of a Half-Bridge Topology

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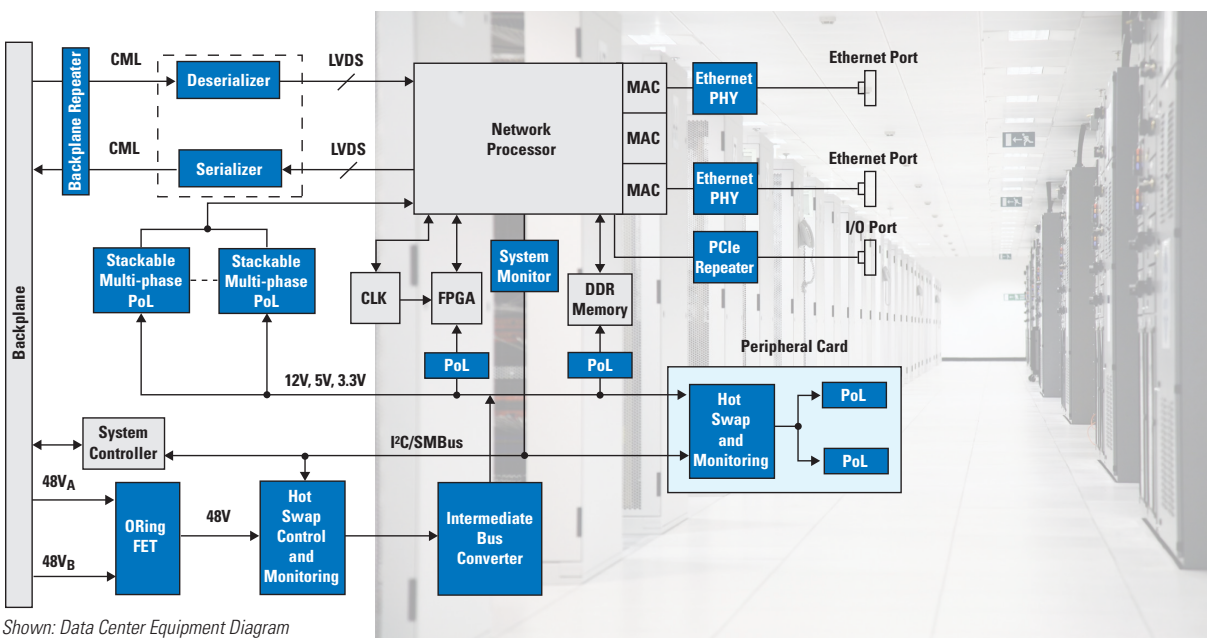

Shown: Data Center Equipment Diagram

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Average Current Limit Balances Center Point of Half-Bridge Input Caps

The other half of the bridge is formed by the switches Q1 and Q2. Switches Q1 and Q2 are turned on alternatively with a pulse width determined by the input and output voltages and the transformer turns ratio. When turned on, each switch applies one-half of the input voltage to the primary transformer. The resulting secondary voltage is then rectified and filtered with an LC filter to provide a constant output voltage.

Typically, half-bridge power converters are controlled using voltage-mode control. As with any other double-ended topologies, such as push-pull or full-bridge, the half-bridge topology is also susceptible to transformer core saturation. In peak current-mode control for a given load, the Pulse-Width Modulation (PWM) cycle is termi-nated at the same current peak. If volts applied to the transformer in one phase are different from the other, peak current-mode control adjusts the on-time to terminate at the same peak. Thereby, it balances the volt-second product in both of the phases and avoids transformer core saturation in both the push-pull and full-bridge topologies. However, this technique is not applicable to the half-bridge topology because of the soft center-point voltage of the half-bridge capacitor divider. Any on-time imbalance—which is inherent in peak current-mode control—will result in the center point drifting towards either the ground or the input voltage. And peak current-mode control merely reinforces this trend which leads to unregulated output voltage and, possibly, transformer saturation.

In voltage-mode control of the half-bridge topology, if one phase is on longer—whether due to device or timing mismatch—then the voltage applied to the transformer is lower because the capacitors are on longer and are discharged further. The volt-second product applied to the transformer from one phase to another is thus balanced. The drift of the center point of the capacitor divider acts as a negative feedback, avoiding transformer saturation.

Why Average Current Limit?

During an overload event in a conventional cycle-by-cycle current limit implementation, the PWM cycle is terminated by the current sense comparator instead of the PWM comparator. This is similar to peak current-mode control. As previously explained, peak current-mode control inherently results in unequal pulse widths resulting in an imbalance at the center point of the half-bridge capacitor divider. ***Figure 2*** shows the waveforms of a half-bridge topology employing traditional cycle-by-cycle current limit. The zoomed SW-node waveform in ***Figure 2*** shows unequal pulse widths causing the center point of the half-bridge capacitor divider to drift. To overcome this drawback, a current limit circuit which balances the pulse widths and hence balances the input capacitor divider is needed. This can be achieved by emulating voltage-mode control during current limit.

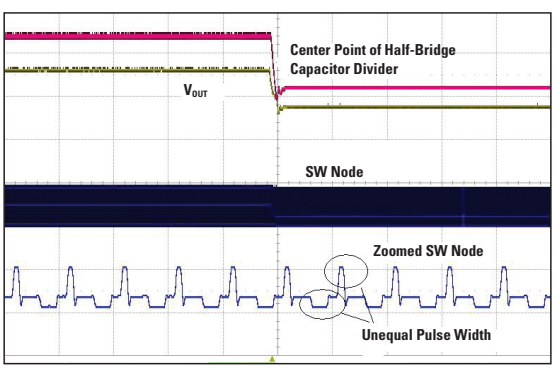

Figure 2. Current Limit Waveforms of Half-Bridge Topology Employing Peak Cycle-by-Cycle Current Limit

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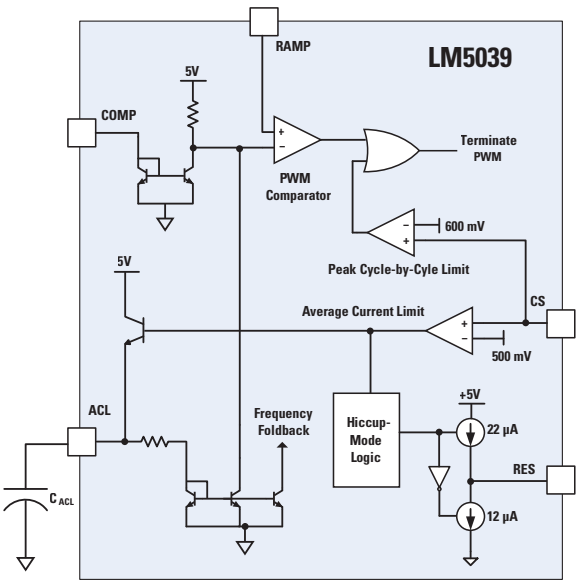

Figure 3. Average Current Limit Circuit Implementation in LM5039 Half-Bridge Controller

Average Current Limit Implementation

In the LM5039 half-bridge controller, the Average Current Limit (ACL) is implemented by monitoring the voltage at the CS pin with two comparators with different reference voltages. As shown in ***Figure 3***, the ACL comparator has a threshold that is set to 0.5V and is used to implement a slower average current limit. The cycle-by-cycle current limit comparator has a threshold of 0.6V and is used to provide instant protection to the power converter. When the 0.5V threshold is crossed at the CS pin, the ACL comparator enables a current source to charge the ACL pin as long as the CS pin is above 0.5V. This quickly charges the ACL capacitor to a level that will eventually terminate the PWM cycle by pulling down the internal COMP node. This allows the ACL comparator to take control of the current limit every cycle instead of the 0.6V cycle-by-cycle current limit comparator. The ACL capacitor provides an averaged signal that pulls down the internal COMP to ensure that equal pulse widths are delivered to both phases of the half-bridge in current limit. This approach to the current limit implementation is similar to the voltage-mode control.

The ACL capacitor should be selected for minimum ripple. Ripple on the ACL capacitor will result in ripple at the center point of the half-bridge capacitor divider. It should also be noted that a large value of the ACL capacitor can slow down the time taken for the ACL circuitry to take control. Therefore, the peak cycle-by-cycle current limit is in control longer, resulting in a drift at the half-bridge center-point voltage.

The response of the average current limit circuitry is the same whether the short is a soft or hard short. During an overload event, the ACL circuitry converts the power supply into a constant current source such that the average output current is equal to:

$$I_{OUT} = \left(\frac{N_{PRI}}{N_{SEC}}\right) \times \frac{500\ mV}{R_{CS}} \times CT_{TURNS}$$

Where N_{PRI} and N_{SEC} are primary and secondary turns of the power transformer, R_{CS} is the current sense resistor, and CT_{TURNS} is the number of turns of the current sense transformer. This scheme is often known as "brickwall" current limiting.

The brickwall current limiting feature is highly desirable because of the predictability of the onset of the current limit at different input line voltages. However, in a fixed-frequency converter, the average output current exhibits a tail in hard-short conditions.

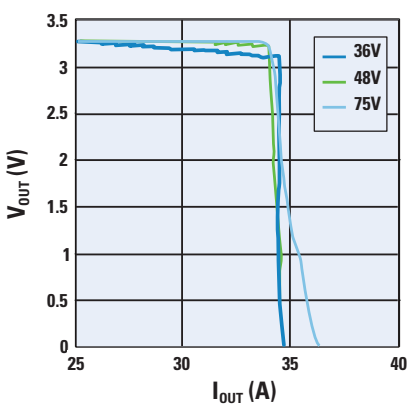

Figure 4. V_{OUT} vs I_{OUT} Curve Illustrating Brickwall Current Limiting

The peak output-inductor current creeps up during the on-time and does not have enough off-time to come back down. The minimum achievable on-time is limited due to propagation and turn-off delays. To avoid the output current tail when the power converter is in average current limit, the LM5039 controller's oscillator frequency is proportionally decreased. In a hard-short condition, the oscillator frequency is reduced to one-third the oscillator frequency set by the RT resistor. The frequency foldback is implemented only in the ACL condition and does not affect the AC response of the control loop. A V_{OUT} vs. I_{OUT} curve, shown in ***Figure 4***, illustrates the brickwall current limiting.

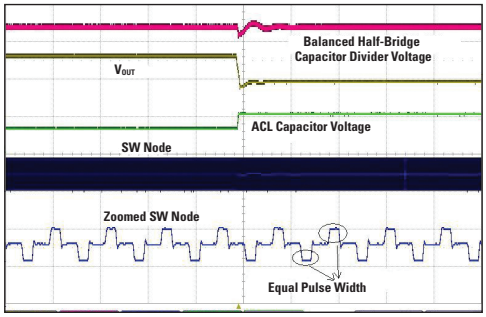

Figure 5. Balanced Half-Bridge Capacitor Waveform in a Soft-Short Condition Employing Average Current Limit

Results

It can be observed from ***Figures 5*** and ***6*** that the center point of the half-bridge capacitor divider is balanced in both soft-short and hard-short conditions. In both of the waveforms, it can be seen that prior to the ACL capacitor charging, the center point starts to drift, but once the ACL circuit is in control, the center point is balanced. From the zoomed trace, it is also clear that the average current limit circuitry maintains equal pulse width to both of the phases of the half bridge.

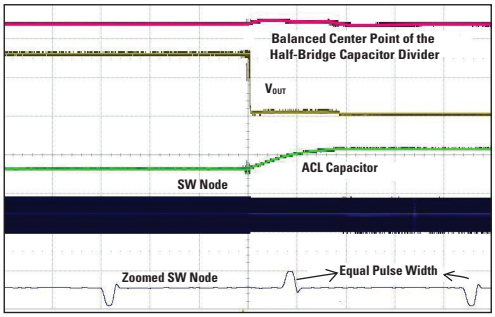

Figure 6. Balanced Half-Bridge Capacitor Waveform in a Hard-Short Condition Employing Average Current Limit

The ACL capacitor charges faster in a soft-short condition compared to a hard-short condition owing to the difference in pulse widths in both of these conditions. Frequency foldback can also be seen in ***Figure 6*** by closely observing the zoomed switch node waveform.

Summary

Traditional peak current cycle-by-cycle current limiting will cause the center point of the half-bridge capacitor divider to drift towards the input rail or ground. To avoid this, in the LM5039 PWM controller, a combination of peak current and average current limiting has been implemented. While the peak current limiting gives the instantaneous protection to the power converter, the average current limiting takes the control of current limiting in few cycles and prevents the voltage drift in the center point of the half-bridge capacitor divider. The average current limit is activated only during an overload condition and it does not affect the typical feed-forward control employed for the half-bridge topology or interfere with the AC response of the loop.

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