Application Note

How to Design a Boost Converter Using the LM5156

Garrett Roecker *Boost Converter and Controller Solutions*

ABSTRACT

The LM5156 is a versatile non-synchronous low-side N-FET controller for switching regulators. Common configurations for the LM5156 include boost, flyback, and SEPIC regulators. This application report focuses on how to configure and design the LM5156 as a boost regulator. This procedure is generic and focuses on selecting the correct components for continuos conduction mode (CCM) boost operation. The design example was used to create the LM5156EVM-BST evaluation model and the results are presented in *LM5156EVM-BST User's Guide*. For typical applications, the *LM5155/56 Boost Controller Quick Start Calculator* can be used to efficiently complete the calculations described in this report.

Table of Contents

List of Figures

List of Tables

1 LM5156 Design Example

This design guide follows typical design procedures and calculations to implement a non-synchronous boost controller operating in continuos conduction mode (CCM) at full load. The design example uses an unregulated 12-V rail (9 V–18 V nominal) (2.5 V to 42 V transients) to produce a regulated 12 V of up to 3-A load current. A switching frequency of 440 kHz is selected to avoid interference in the AM band (530 kHz to 1.8 MHz). The minimum supply voltage is selected to be 2.5 V, which is similar to many automotive applications that are required to operate during stop-start conditions and cold cranking conditions. This design is intended to operate continuously at an operating voltage of 4 V but support supply transients as low as 2.5 V. Section 3 details the component selection based on the general design parameters shown in Table 2-1.

2 Example Application

Table 2-1 indicates the parameters for the example application.

Table 2-1. Design Parameters

PARAMETER	SPECIFICATIONS
V_{SUPPLY}	2.5 V to 12 V (Unregulated above 12 V)
V_{LOAD}	12 V
I_{LOAD}	3 A
f_{SW}	440 kHz
η (estimated efficiency)	90%

3 Calculations and Component Selection

This section covers the equations specific to the LM5156 device to implement a boost controller that operates in continuous conduction mode. Component selection is based on the example application described in Table 2-1.

3.1 Switching Frequency

Selecting the proper switching frequency is the first step in the design process. Higher switching frequencies yield a smaller total solution size. However, the small size comes at the cost of increased switching losses, decreasing the total efficiency regulator. Higher efficiency is achieved by selecting a relatively lower switching frequency but requires physically larger components. Harmonics of the switching frequency should be considered in designs with strict EMC requirements. Equation 1 is used to set the frequency of the oscillator in the LM5156 device. The example application is selected to have a switching frequency of 440 kHz.

$$R_T = \frac{2.21 \times 10^{10}}{f_{SW}} - 955 = \frac{2.21 \times 10^{10}}{440\ kHz} - 955 = 49.2\ k\Omega \quad (1)$$

A standard value of 49.9 kΩ is chosen for R_T.

The internal oscillator of the LM5156 can be synchronized to an external clock as described in the data sheet. The LM5156 has a maximum duty cycle limit that is frequency dependent. See the LM5156 data sheet for details on step-up ratio limitations.

3.2 Inductor Calculation

Three main parameters are considered when selecting the inductance value: inductor current ripple ratio (RR), falling slope of the inductor current and the right-half plane zero frequency (ω_{Z_RHP}) of the control loop. Finding a balance between these three parameters helps simplify the rest of the design process.

- The inductor current ripple ratio is selected to balance the copper loss and core loss of the inductor. As the relative ripple current increases; the core loss increases and the copper loss decreases
- The falling slope of the inductor current should be small enough to prevent sub-harmonic oscillation. A relatively larger inductance value results in a smaller falling slope of the inductor current. This increases the impact internal slope compensation provided by the LM5156.
- The right-half plane zero should be placed at relatively high frequencies, allowing a higher crossover frequency of the control loop. As the relative inductance value decrease the right-half plane zero frequency increases.

A maximum ripple ratio between 30% and 70% results in a good balance between the power loss of the inductor, the down slope of the inductor current and the right-half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In continuos conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33% ($D_{max\Delta IL}$ = 0.33). In the case that the application specification does not result in a duty cycle of 33% the maximum supply voltage is used to calculate the maximum ripple ratio. Use Equation 2 to calculate the supply voltage that results in a duty cycle of 33% (D = 0.33).

$$V_{SUPPLY\_max\_\Delta IL} = V_{LOAD} \times \left(1 - D_{max\_\Delta IL}\right) = 12\ V \left(1 - 0.33\right) = 8.04\ V \tag{2}$$

where

- $D_{max\Delta IL}$ is the duty cycle where the maximum inductor ripple current occurs

Knowing $V_{SUPPLY\_max\_\Delta IL}$ the desired ripple ratio and the switching frequency, use Equation 3 to calculate the inductor value.

$$L_{M\_calc} = \frac{V_{SUPPLY\_max\_\Delta IL}}{I_{SUPPLY} \times RR \times f_{SW}} \times D = \frac{8.04\ V}{4.478\ A \times 0.60 \times 440\ kHz} \times 0.33 = 2.24\ \mu H \tag{3}$$

where

- D is the duty cycle where the maximum inductor ripple current occurs
- RR is the ripple ratio of inductor ripple current to average supply current

A standard value of 2.2 µH is selected for the value of L_M. The maximum peak inductor current occurs when the supply voltage is at the minimum value, V_{SUPPLY_min}, and the maximum load current, I_{LOAD_max}. The peak inductor current is calculated using Equation 4. This is the sum of the average input current and one-half the inductor ripple current.

$$IL_{PEAK\_MAX} = \frac{V_{LOAD} \times I_{OUT}}{V_{SUPPLY} \times \eta} + \frac{1}{2} \times \frac{V_{SUPPLY} \times D}{L_M \times f_{SW}} = \frac{12\ V \times 3\ A}{2.5\ V \times 0.9} + \frac{1}{2} \times \frac{2.5\ V \times 0.79}{2.2\ \mu H \times 440\ kHz} = 17.02\ A \tag{4}$$

where

- η is the estimated efficiency at the minimum supply voltage and maximum load current

The peak inductor current is used to properly size the current sense resistor, R_S.

3.3 Current Sense Resistor Calculation

Selecting the switch current sense network components is described in the following section. Figure 3-1 shows the four components that make up the current sense network of the LM5156. R_S is the current sense resistor. This resistor senses the switch current, and also sets the peak current limit of the inductor current. R_F and C_F form a low pass filter. This filter helps minimize high frequency noise on the current sense signal caused by the MOSFET turning on. R_{SL} sets the external slope compensation and is optional. In some applications where the internal slope compensation is not large enough R_{SL} will be required.

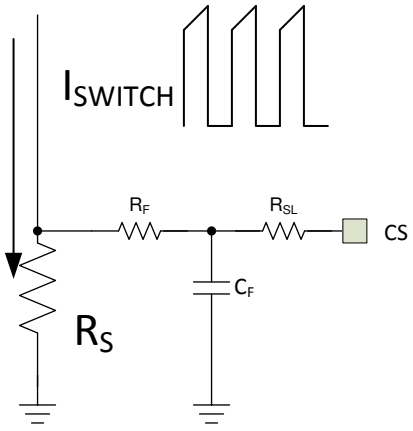

Figure 3-1. LM5156 Current Sense Network

3.3.1 Current Sense Resistor and Slope Compensation Resistor Selection

The current sense resistor is selected to avoid current limiting during the minimum supply voltage, V_{SUPPLY_min}, and the maximum load current, I_{LOAD_max}. Due to component tolerances and power loss of the regulator, the peak current limit should be set some margin above the calculate peak inductor current. A margin of 20% to 40% (M_{I_LIMIT} = 0.2) is a good starting point. Equation 5 is used to calculate the desired peak inductor current limit value. In this design example, M_{I_LIMIT} is selected to be 30%.

$$IL_{PEAK\_LIMIT\_SET} = \left(1 + M_{I\_LIMIT}\right) \times IL_{PEAK\_MAX} = \left(1 + 0.3\right) \times 17.02\ A = 22.13\ A \tag{5}$$

where

- IL_{PEAK_MAX} is the maximum peak inductor current

Selecting the correct current sense resistor is an iterative process. The first step is to calculate the maximum current sense resistor, assuming that no external slope compensation is required (R_{SL} = 0 Ω), using Equation 6.

$$R_{S\_MAX} = 1.667 \times \frac{V_{SLOPE} \times L_M \times f_{SW}}{V_{LOAD} - V_{SUPPLY_{MIN}}} = 1.667 \times \frac{40\ mV \times 2.2\ \mu H \times 440\ kHz}{12\ V - 2.5\ V} = 6.79\ m\Omega \tag{6}$$

where

- V_{SL} is the internal fixed internal slope compensation of the LM5156

Assuming that no external slope compensation is required, the current sense resistor value is calculated using Equation 7.

$$R_{S\_wo\_sl} = \frac{V_{CLTH}}{IL_{PEAK\_LIMIT\_SET}} = \frac{100\ mV}{22.13\ A} = 4.51\ m\Omega \tag{7}$$

where

- V_{CLTH} is the nominal current limit threshold of the LM5156

If the calculated $R_{S\_wo\_sl}$ resistance value is less than the R_{S_MAX} resistance value, the $R_{S\_wo\_sl}$ is selected for the current sense resistor value (R_S). If the calculated $R_{S\_wo\_sl}$ resistance value is greater than the calculated R_{S_MAX} resistance value, there are two approaches to take; decrease the current sense resistor value or add external slope compensation.

- Decreasing the current sense resistor increases the effectiveness of the internal slope compensation. With no external slope compensation the peak inductor current limit will be constant regardless of the duty cycle. A lower current sense resistor results in a larger inductor peak current limit value, which increases the required saturation current rating of the inductor.
- Adding external slope compensation. The peak inductor current limit varies with supply voltage when external slope compensation is added.

External slope compensation is added by setting R_{SL} to a non-zero value less than 1 kΩ. In applications where external slope compensation is added, R_S is calculated using Equation 8.

$$R_{S\_w\_sl} = \frac{L_M \times f_{SW} \times \left(V_{CLTH} + D \times V_{SLOPE}\right)}{D \times 0.833 \times \left(V_{LOAD} - V_{SUPPLY\_MIN}\right) + IL_{PEAK_{LIMIT_{SET}}} \times L_M \times f_{SW}}$$

$$R_{S\_w\_sl} = \frac{2.2\ \mu H \times 440\ kHz \times (100\ mV + 0.79 \times 40\ mV)}{0.79 \times 0.833 \times (12\ V - 2.5\ V) + 22.13\ A \times 2.2\ \mu H \times 440\ kHz} = 4.6\ m\Omega \quad (8)$$

where

- 0.833 is the ratio of the total slope compensation to the sensed falling inductor current.

R_{SL} is calculated using Equation 9.

$$R_{SL} = \frac{V_{CLTH} - IL_{PEAK\_LIMIT\_SET} \times R_{S\_w\_sl}}{I_{SLOPE} \times D} = \frac{100\ mV - 22.13\ A \times 4.6\ m\Omega}{30\ \mu A \times 0.79} = -75.6\ \Omega \quad (9)$$

where

- I_{SLOPE} is the slope compensation source of the LM5156
- D is the duty cycle at the minimum supply voltage

If the calculated R_{SL} value exceeds the maximum value of the 1 kΩ, the down slope of the sensed inductor current needs to be reduce. To reduce the down slope of the inductor current, the inductance value of L_M must be increased. If the L_M inductance value is changed the current sense resistor calculations must be recalculated. If the calculated value of R_{SL} is negative no external slope compensation is required.

For this design example a current sense resistor value is selected to be 4 mΩ (R_S), which is the nearest standard resistor value to the calculated value in Equation 7. This value is selected to keep from triggering current limit protection during load transients. No external slope compensation is required and R_{SL} is selected to be 0 Ω. The peak inductor current limit is calculated using Equation 10.

$$IL_{PEAK\_LIMIT} = \frac{V_{CLTH} - I_{SLOPE} \times R_{SL} \times D}{R_S} = \frac{100\ mV - 30\ \mu A \times 0\ \Omega \times 0.79}{4\ m\Omega} = 25\ A \quad (10)$$

The peak inductor current limit is constant, regardless of the supply voltage, because there is no external slope compensation. For this design the inductor saturation current rating should be greater than 25 A.

3.3.2 Current Sense Resistor Filter Calculation

For all designs is it recommended to add the low pass filter to the current sense signal. R_F and C_F implement a low pass filter as shown in Figure 3-1. The filter is added to help mitigate the impact of the leading edge spike on the current sense signal. R_F is selected to be between 10 Ω and 200 Ω. For this design R_F is selected to be 100 Ω. C_F must be less than the value specified in Equation 11 to ensure proper operation.

$$C_F < \frac{1 - D}{3 \times R_F \times f_{SW}} = \frac{1 - 0.79}{3 \times 100 \times 440\ kHz} = 1.59\ nF \quad (11)$$

C_F is selected to be 100 pF. Due to the delay of the low pass filter, the current limit is not valid when V_{SUPPLY} is greater than a given voltage calculated in. For this design the current limit is valid for the entire supply voltage range. Equation 12 is used to calculate this value.

$$V_{SUPPLY\_IL\_MAX} = V_{LOAD} \times \left(1 - 2 \times C_F \times R_F \times f_{SW}\right) = 12\ V \times \left(1 - 2 \times 100\ pF \times 100\ \Omega \times 440\ kHz\right) = 11.89\ V \quad (12)$$

3.4 Inductor Selection

R_S, the inductor must be selected according to three parameters; calculated inductance value (L_M), RMS inductor current at the minimum supply voltage and the peak inductor current limit (I_{LPEAK_LIMIT}) set by the current sense resistor (R_S).

- The inductance value is selected to be 2.2 µH. This is a standard value that is produced by most magnetic vendors.
- The RMS current of the inductor can be estimated by calculating the average inductor current (I_{LAVG}) and is approximately equal to the average supply current. The average inductor current is estimated to be 16 A when V_{SUPPLY} = 2.5 V. The inductor RMS current rating should be higher than calculated average inductor current and keep the inductor temperature rise to a reasonable level based on the application.
- The saturation current rating of the inductor should be larger than the calculated I_{LPEAK_LIMIT} value, 25 A. If the inductor becomes saturated, proper operation of the regulator is not ensured.

For this design example, the inductor is selected to have an inductance value of 2.2 µH, 40°C component temperature rise at an RMS of 20 A, and a saturation current limit of 32 A.

3.5 Diode Selection

The diode must be rated to handle the average load current, plus some margin, while being able to dissipate the conduction losses. The voltage rating of the diode must be greater than the load voltage, V_{LOAD}. Selecting a Schottky diode is recommended due to the small reverse recovery time and smaller forward voltage drop with respect to a standard fast recovery diode. For this design a 60-V reverse voltage, 10-A average forward current Schottky diode is selected. The wort case conducted power loss of this diode is calculated in Equation 13.

$$P_{D\_con} = V_F \times \left(1 - D\right) \times I_{SUPPLY} = 480\ mV \times \left(1 - 0.79\right) \times \frac{12\ V \times 2\ A}{2.5\ V} = 968\ mW \quad (13)$$

where

- V_F is the forward voltage drop of the diode

3.6 MOSFET Selection

MOSFET selection focuses on power dissipation and voltage rating. Power dissipation of MOSFET is composed of two different parts, conduction losses and switching losses. Conduction losses are dominated by the $R_{DS(on)}$ parameter of the MOSFET. Switching losses occur during the rise and fall time of the switch node, when the N-channel MOSFET is turning on and turning off. During the rise time and fall time, current and voltage are present in the channel of the MOSFET. The longer the rise and fall time of the switch node the higher the switching losses. Selecting a MOSFET with minimal parasitic capacitances lowers the switching losses. Ideally, conduction losses and switching losses should be approximately equal

The total gate charge (Q_{G_total}) must not be large enough to place the internal VCC regulator into current limit. The Q_{G_total} for a given MOSFET should be known. Equation 14 provides the maximum Q_{G_total} of the MOSFET.

$$Q_{G\_total} < \frac{35mA}{f_{SW}} \quad (14)$$

The drain to source break down voltage rating on the MOSFET needs to be higher than the load voltage, plus some margin, due to voltage spike on the switch node. The break down voltage rating should be at least 10 V higher than V_{LOAD} plus V_F . V_F is the forward voltage of the rectifying diode.

For this design, a 60-V MOSFET with low $R_{DS(on)}$ low threshold voltage is selected. A 60-V rating is selected to handle the maximum input voltage transient of 42 V.

3.7 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. A practical way to size the output capacitor is based on the required load transient output voltage ripple specification. The load transient specification is related to the control loop crossover frequency. The control loop cross over frequency is set to 1/5th the right half plane zero frequency. This crossover frequency is calculated using Equation 15.

$$f_{cross} = \frac{\frac{V_{LOAD}}{I_{LOAD}} \times \left(\frac{V_{SUPPLY\_min}}{V_{LOAD}}\right)^2}{5 \times 2\pi \times L_m} = \frac{\frac{12\ V}{3\ A} \times \left(\frac{2.5\ V}{12\ V}\right)^2}{5 \times 2\pi \times 2.2\ \mu H} = 2.51\ kHz \quad (15)$$

For this design example, the load transient specification indicates that the load voltage should not overshoot or undershoot more than 600 mV during a load transient from 50% load current (1.5 A) to 100% load current (3 A) occurs. Equation 16 is used to calculate the estimated load capacitance to achieve the specified load transient load voltage ripple requirements.

$$C_{LOAD\_min} = \frac{\Delta I_{LOAD}}{2\pi \times f_{cross} \times \Delta V_{LOAD}} = \frac{1.5\ A}{2\pi \times 2.51\ kHz \times 600\ mV} = 158\ \mu F \quad (16)$$

where

- ΔI_{LOAD} is the difference in the load current conditions (3 A - 1.5 A)
- ΔV_{LOAD} is the specified overshoot voltage specification and undershoot voltage specification

The output capacitor must be rated to handle the ripple current without being damaged or without significantly reducing operating lifetime. The maximum RMS output ripple current is estimated using Equation 17. Ceramic capacitors generally have a relatively high RMS ripple current rating than electrolytic capacitors. Ceramic capacitors are used to increase the total RMS current rating of the output capacitor bank.

$$I_{RMS\_CLOAD} = \sqrt{(1-D) \times \left[{I_{LOAD}}^2 \times \frac{D}{(1-D)^2} + \frac{\Delta IL^2}{3} \right]} = \sqrt{(1-0.79) \times \left[3\ A^2 \times \frac{0.79}{(1-0.79)^2} + \frac{2.045\ A^2}{3} \right]} = 5.844\ A \quad (17)$$

For this design, a total output capacitance of 200 µF is selected. The capacitor bank ESR (R_{ESR}) is estimated to be around 2 mΩ. The output capacitance and low R_{ESR} value help minimize the voltage drop during load transients.

3.8 Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. For this design and input capacitance of 100 µF is selected. Assuming that low ESR, high quality ceramic capacitor are used, Equation 18 is used to calculate the maximum supply voltage ripple based on input capacitance of 100 µF

$$\Delta V_{SUPPLY} = \frac{V_{LOAD}}{32 \times L_M \times C_{IN} \times {f_{SW}}^2} = \frac{12\ V}{32 \times 2.2\ \mu H \times 150\ \mu F \times 440\ kHz^2} = 5.86\ mV \quad (18)$$

The supply voltage ripple is a function of the load impedance of the supply voltage power supply. If the impedance of the input supply is large more input capacitance is required to minimize the ripple.

3.9 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating voltage of the regulator. Two levels must be specified; the voltage the LM5156 device starts operation ($V_{SUPPLY(ON)}$) and the voltage the LM5156 enters stand-by mode ($V_{SUPPLY(OFF)}$). In this example, $V_{SUPPLY(ON)}$ voltage is 2.6 V and the $V_{SUPPLY(OFF)}$ is 2.2 V. Using Equation 19, the top UVLO resistor (R_{UVLOT}) is calculated.

$$R_{UVLOT} = \frac{0.967 \times V_{SUPPLY(ON)} - V_{SUPPLY(OFF)}}{5\ \mu A} = \frac{0.967 \times 2.6\ V - 2.2\ V}{5\ \mu A} = 62.8\ k\Omega \quad (19)$$

A standard value of 60.4 kΩ is selected for R_{UVLOT}. Using Equation 20 the top UVLO resistor (R_{UVLOB}) is calculated

$$R_{UVLOB} = \frac{1.5\ V \times R_{UVLOT}}{V_{SUPPLY\_ON} - 1.5\ V} = \frac{1.5\ V \times 60.4\ k\Omega}{2.6\ V - 1.5\ V} = 82.36\ k\Omega \quad (20)$$

A standard value of 80.6 kΩ is selected for R_{UVLOB}

3.10 Soft-Start Capacitor Selection.

The soft-start capacitor is used to minimize and overshoot on the load voltage during the start-up of the regulator. Equation 21 is used to calculate the minimum recommended soft-start capacitor value.

$$C_{SS} > \frac{10\ \mu A \times V_{LOAD} \times C_{LOAD}}{I_{LOAD} \times V_{REF}} = \frac{10\ \mu A \times 12\ V\ 200 \mu F}{3\ A \times 1\ V} = 8\ nF \quad (21)$$

where

- V_{REF} is the feedback voltage reference of the LM5156.

For this design a CSS value of 220 nF is selected to minimize any overshoot on the load voltage during start-up.

3.11 Feedback Resistor Selection

The feedback resistors (R_{FBT}, R_{FBB}) set the regulated load voltage by comparing the scaled voltage to the internal voltage reference. To help limit the bias current of the feedback resistor divider, R_{FBT} is selected to be 49.9 kΩ. Equation 22 is used to calculate the value of R_{FBB}.

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{LOAD}}{V_{REF}} - 1} = \frac{49.9\ k\Omega}{\frac{12\ V}{1\ V} - 1} = 4.53\ k\Omega \quad (22)$$

R_{FBB} is selected to be 4.53 kΩ.

3.12 Control Loop Compensation

There are many different strategies to set the crossover frequency of the control loop, and placing the pole and zero of the error amplifier. In this section a general technique is described to adequately stabilize the control loop for a peak current mode controlled boost regulator in continuos conduction mode operation. A type II compensation network is implemented as shown in Figure 3-2. Type II compensation provides a programable low frequency zero and programable high frequency pole. For a detailed model of the control loop see Section 5. The loop compensation selection process is broken down into a number of distinct steps described in the following sections.

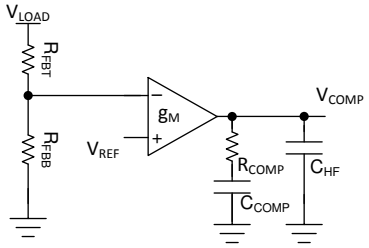

Figure 3-2. Type II Compensation Network

3.12.1 Select the Loop Crossover Frequency (f_{CROSS})

The crossover frequency of the loop is either selected to be 1/10th the switching frequency or 1/5th the right-half plane zero frequency, which ever is lower. Equation 23 shows the calculation for 1/10th the switching frequency. Equation 24 shows how to calculate the 1/5th the right half plane zero frequency.

$$f_{CROSS} = \frac{f_{SW}}{10} = \frac{440kHz}{10} = 44kHz \tag{23}$$

$$f_{cross} = \frac{R_{LOAD} \times (1-D)^2}{5 \times 2\pi \times L_m} = \frac{4\ \Omega \times (1-0.79)^2}{5 \times 2\pi \times 2.2\ \mu H} = 2.51\,kHz \tag{24}$$

where

- R_{LOAD} is the load resistance equal to V_{LOAD}/I_{LOAD}

The crossover frequency is selected to be 1/5th the right half plane zero frequency, 2.51 kHz.

3.12.2 Determine Required R_{COMP}

The R_{COMP} value directly affects the crossover frequency of the control loop. The higher the crossover frequency, the faster the control loop reacts to transient conditions. Knowing the desired loop crossover frequency, 2.51 kHz, R_{COMP} is calculate using Equation 25.

$$R_{COMP} = \frac{2\pi \times C_{LOAD} \times R_S \times V_{LOAD}{}^2 \times f_{cross}}{G_{COMP} \times g_m \times V_{SUPPLY\_MIN} \times V_{REF}} = \frac{2\pi \times 200\ \mu F \times 4\ m\Omega \times 12\ V^2 \times 2.51\,kHz}{G_{COMP} \times g_m \times 2.5\ V \times 1\ V} = 2.5\ k\Omega \tag{25}$$

where

- g_m is the transconductance of the error amplifier, 2 mA/V
- G_{COMP} is COMP to PWM gain, 0.142 V/V

R_{COMP} is selected to be 2.49 kΩ. Decreasing the R_{COMP} resistance value lowers the crossover frequency but helps ensure the control loop remains stable over the specified supply voltage range.

3.12.3 Determine Required C_{COMP}

The R_{COMP} resistor and C_{COMP} capacitor set the low frequency zero of the compensation network resulting in a phase boost. Placement of this zero frequency largely impacts the transient response of the control loop. A good strategy is placing the zero at the geometric mean of the crossover frequency (f_{CROSS}) and the low frequency pole of the plant. Equation 26 places the low frequency zero of error amplifier a the geometric mean of f_{CROSS} and low frequency pole of the plant (ω_{P_LF}). For this design the desired zero location is 999 Hz.

$$f_{z\_EA} = \sqrt{f_{cross} \times \frac{2}{2\pi \times C_{LOAD} \times R_{LOAD}}} = \sqrt{2.51\,kHz \times \frac{2}{2\pi \times 200\ \mu F \times 4\ \Omega}} = 999\ Hz \tag{26}$$

With the zero frequency selected, Equation 27 produces the value of C_{COMP}.

$$C_{COMP} = \sqrt{\frac{C_{LOAD} \times R_{LOAD}}{4\pi \times R_{COMP}{}^2 \times f_{cross}}} = \sqrt{\frac{200\ \mu F \times 4\ \Omega}{4\pi \times 2.49\ k\Omega^2 \times 2.51\,kHz}} = 63\ nF \tag{27}$$

C_{COMP} is chosen to be 68 nF.

3.12.4 Determine Required C_{HF}

The C_{HF} capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin achieved. It is recommended to set the pole frequency at the RHP zero (ω_{Z_RHP}) or between the RHP zero and half the switching frequency. For this design the pole frequency was selected to be 52 kHz. The is geometric mean

between the RHP zero when V_{SUPPLY} is 2.5 V and half switching frequency. Equation 28 is used to calculate the value of C_{HF}.

$$C_{HF} = \frac{C_{COMP}}{2\pi \times C_{COMP} \times R_{COMP} \times f_{p\_EA} - 1} = \frac{68\ nF}{2\pi \times 68\ nF \times 2.49\ k\Omega \times 52\ kHz - 1} = 1.2\ nF \quad (28)$$

C_{HF} is chosen to be 1 nF.

3.13 Efficiency Estimation

The total loss of the boost converter (P_{TOTAL}) can be expressed as the sum of the losses in the device (P_{IC}), MOSFET power losses (P_Q), diode power losses (P_D), inductor power losses (P_L), and the loss in the sense resistor (P_{RS}).

$$P_{TOTAL} = P_{IC} + P_Q + P_D + P_L + P_{RS}[W] \quad (29)$$

P_{IC} can be separated into gate driving loss (P_G) and the losses caused by quiescent current (P_{IQ}).

$$P_{IC} = P_G + P_{IQ}[W] \quad (30)$$

Each power loss is approximately calculated as follows:

$$P_G = Q_{G(@VCC)} \times V_{BIAS} \times F_{SW}[W] \quad (31)$$

$$P_{IQ} = V_{BIAS} \times I_{BIAS}[W] \quad (32)$$

For I_{BIAS} values in each mode, see the LM5156 data sheet.

P_Q can be separated into switching loss ($P_{Q(SW)}$) and conduction loss ($P_{Q(COND)}$).

$$P_Q = P_{Q(SW)} + P_{Q(COND)}[W] \quad (33)$$

Each power loss is approximately calculated as follows:

$$P_{Q(SW)} = 0.5 \times (V_{LOAD} + V_F) \times I_{SUPPLY} \times (t_R + t_F) \times F_{SW} \quad (34)$$

t_R and t_F are the rise and fall times of the low-side N-channel MOSFET device. I_{SUPPLY} is the input supply current of the boost converter.

$$P_{Q(COND)} = D \times {I_{SUPPLY}}^2 \times R_{DS(ON)}[W] \quad (35)$$

$R_{DS(on)}$ is the on-resistance of the MOSFET and is specified in the MOSFET data sheet. Consider the $R_{DS(on)}$ increase due to self-heating.

P_D can be separated into diode conduction loss (P_{VF}) and reverse recovery loss (P_{RR}).

$$P_D = P_{VF} + P_{RR}[W] \quad (36)$$

Each power loss is approximately calculated as follows:

$$P_{VF} = (1 - D) \times V_F \times I_{SUPPLY}[W] \quad (37)$$

$$P_{RR} = V_{LOAD} \times Q_{RR} \times F_{SW}[W] \quad (38)$$

Q_{RR} is the reverse recovery charge of the diode and is specified in the diode data sheet. Reverse recovery characteristics of the diode strongly affect efficiency, especially when the load voltage is high.

P_L is the sum of DCR loss (P_{DCR}) and AC core loss (P_{AC}). DCR is the DC resistance of inductor which is mentioned in the inductor data sheet.

$$P_L = P_{DCR} + P_{AC}[W] \tag{39}$$

Each power loss is approximately calculated as follows:

$$P_{DCR} = I_{SUPPLY}^2 \times R_{DCR}[W] \tag{40}$$

$$P_{AC} = K \times \Delta I^{\beta} F_{SW}^{\alpha}[W] \tag{41}$$

$$\Delta I = \frac{V_{SUPPLY} \times D \times \frac{1}{F_{SYNC}}}{L_M} \tag{42}$$

ΔI is the peak-to-peak inductor current ripple. K, α, and β are core dependent factors which can be provided by the inductor manufacturer.

P_{RS} is calculated as follows:

$$P_{RS} = D \times I_{SUPPLY}^2 \times R_S[W] \tag{43}$$

Efficiency of the power converter can be estimated as follows:

$$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{P_{TOTAL} + V_{LOAD} \times I_{LOAD}} \times 100[\%] \tag{44}$$

4 Component Selection Summary

See the *LM5156EVM-BST User's Guide* for more testing results.

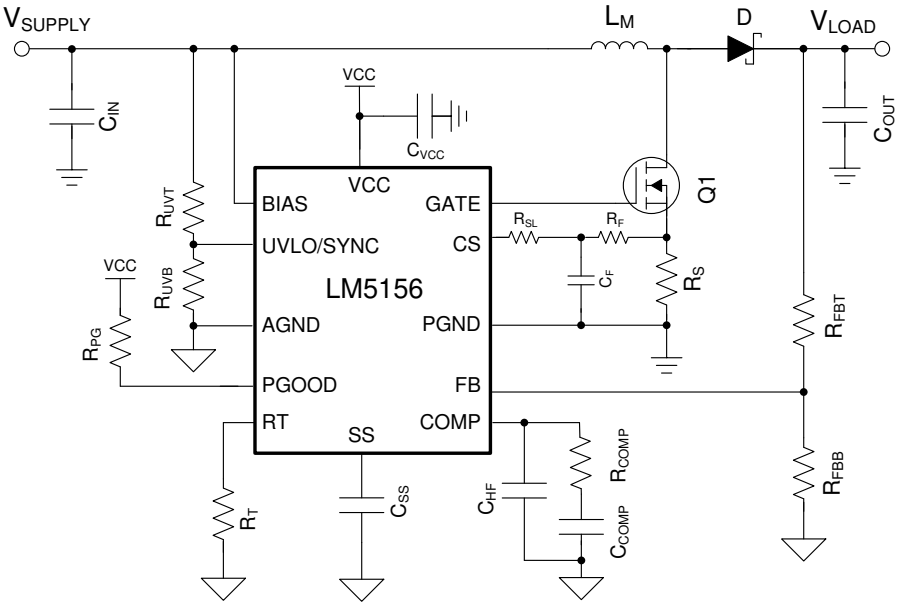

Figure 4-1. Application Circuit

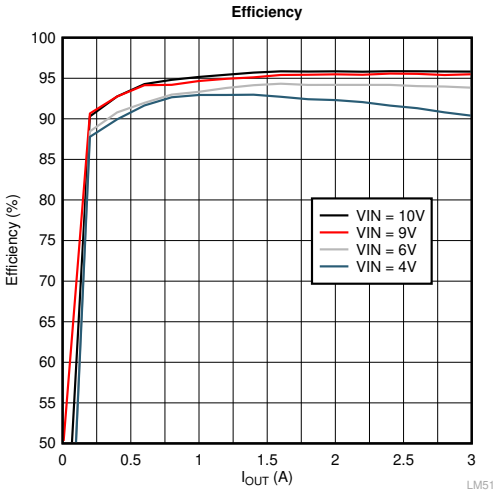

Figure 4-2. Efficiency vs I_{OUT}

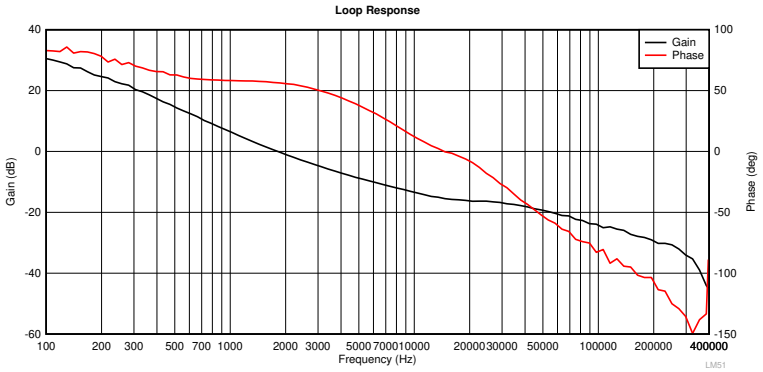

Figure 4-3. Control Loop Response V_{SUPPLY} = 4 V, I_{LOAD} = 3 A

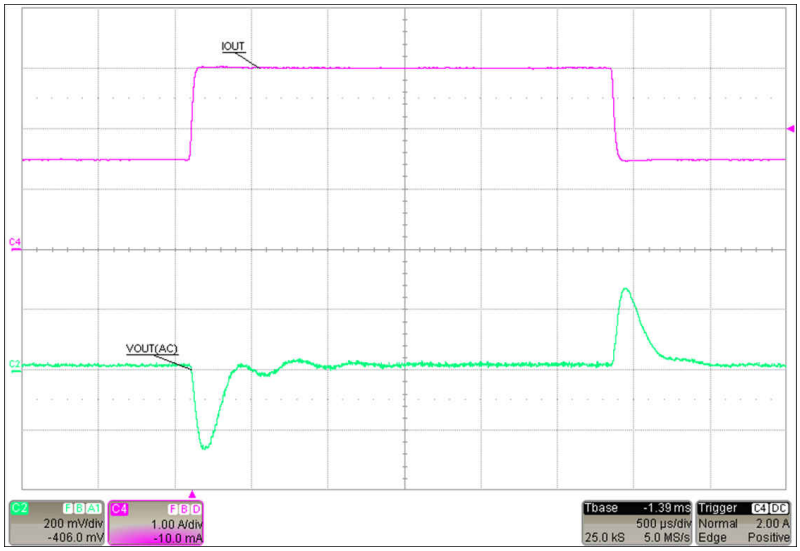

Figure 4-4. Load Step: I_{LOAD}1.5 A to 3 A, V_{SUPPLY} = 4 V

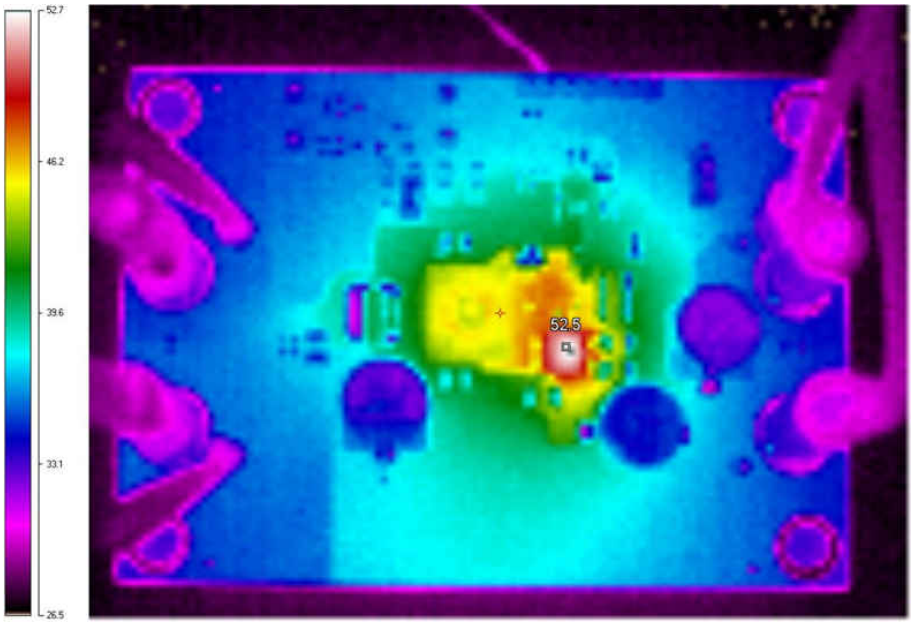

Figure 4-5. Thermal Image: V_{SUPPLY} = 4 V, I_{LOAD} = 3 A

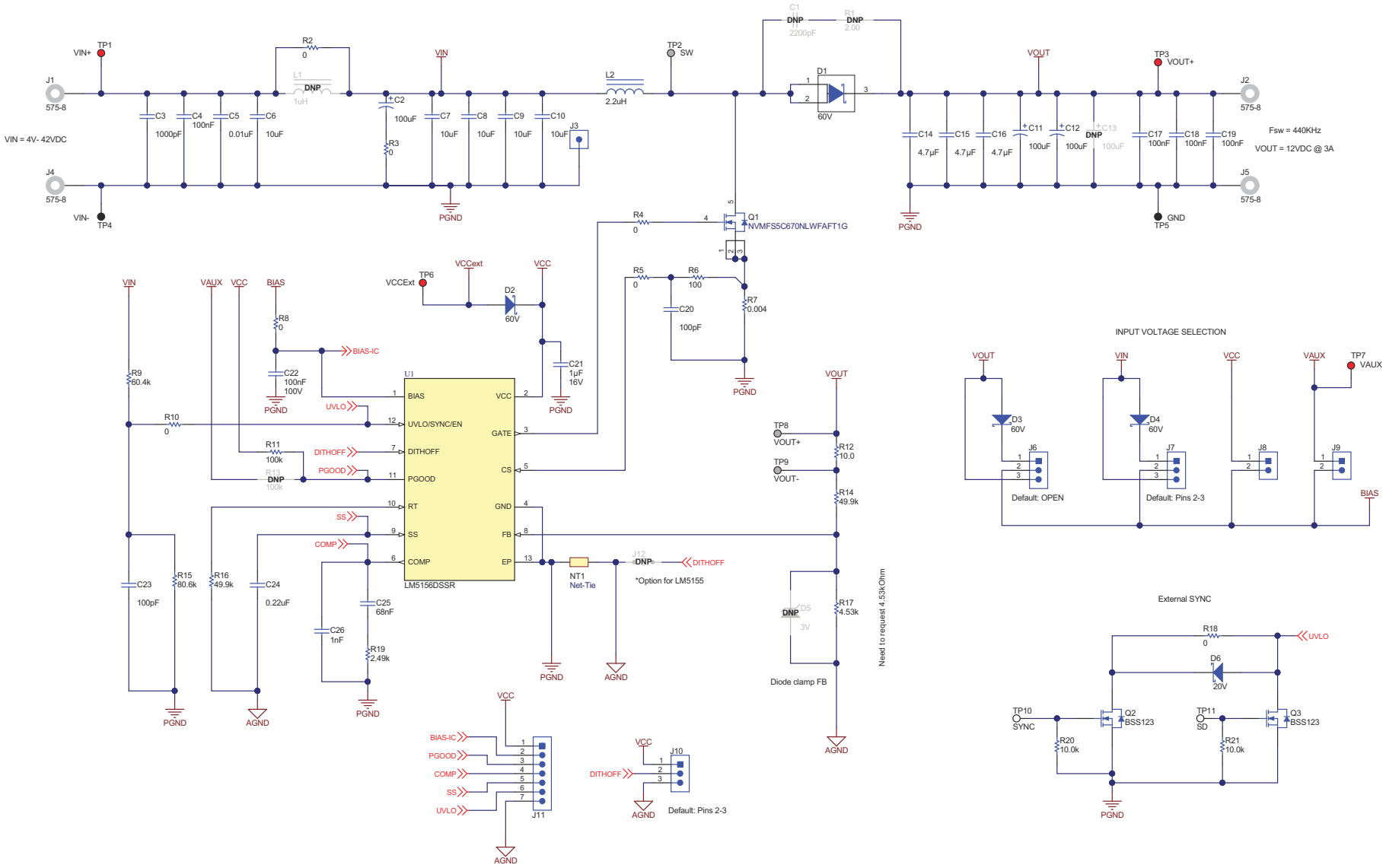

Figure 4-6. LM5156EVM-BST Schematic

5 Small-Signal Frequency Analysis

This section provides detailed equations used to model the control loop when the LM5156 is configured as a boost regulator. These equations are only valid when the regulator is operating in continuous conduction mode. The simplified formulas allow for quick evaluation of the control loop, but loose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

5.1 Boost Regulator Modulator Modeling

These equations model the plant of a peak current mode boost regulator in continuous conduction mode.

Table 5-1. Control Loop Equations

	Simplified Formula	Comprehensive Formula
Modulator Equations		
Modulator Transfer Function	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n{}^2}\right)}$
Modulator DC Gain	$A_M = G_{COMP}\frac{R_{LOAD}}{A_{CS}\cdot R_S}\times\frac{D'}{2}$	
RHP Zero	$\omega_{Z\_RHP} = \frac{R_{LOAD}\left(D'\right)^2}{L_M}$	
ESR Zero	$\omega_{Z\_ESR} = \frac{1}{C_{OUT}\cdot R_{ESR}}$	
Low Frequency Pole	$\omega_{P\_LF} = \frac{2}{C_{OUT}\cdot R_{LOAD}}$	
Sub-Harmonic Double Pole	Not Considered	$\omega_n = \pi\cdot f_{sw}$
Quality Factor	Not Considered	$Q = \frac{1}{\pi\left[D'\cdot\left(1+\frac{s_e}{s_n}\right)-\frac{1}{2}\right]}$
Slope Compensation	Not Considered	$s_e = \left(V_{SLOPE}+I_{SLOPE}\cdot R_{SL}\right)\cdot f_{sw}$
Sensed Rising Inductor Slope	Not Considered	$s_n = \frac{V_{SUPPLY}\cdot R_S\cdot A_{CS}}{L_M}$

5.2 Compensation Modeling

These equations model a type II compensation network implemented using a transconductance error amplifier.

Table 5-2. Compensation Modeling Equations

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback Transfer Function	$\frac{\hat{v}_{COMP}(s)}{\hat{v}_{LOAD}(s)} = -A_{FB} \frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$	
Feedback DC Gain	$A_{FB} = \frac{R_{FBB}\cdot g_m}{(R_{FBB}+R_{FBT})\cdot C_{COMP}}$	$A_{FB} = \frac{R_{FBB}\cdot g_m}{(R_{FBB}+R_{FBT})\cdot (C_{COMP}+C_{HF})}$
Low Frequency Zero	$\omega_{Z\_EA} = \frac{1}{R_{COMP}\cdot C_{COMP}}$	$\omega_{Z\_EA} = \frac{1}{R_{COMP}\cdot C_{COMP}}$
High Frequency Pole	$\omega_{P\_EA} = \frac{1}{R_{COMP}\cdot C_{HF}}$	$\omega_{P\_EA} = \frac{C_{COMP}+C_{HF}}{R_{COMP}\cdot C_{COMP}\cdot C_{HF}}$
Mid-band Gain	$G_{MID} = \frac{R_{COMP}\cdot R_{RFBB}\cdot g_m}{(R_{FBB}+R_{FBT})}$	$G_{MID} = \frac{C_{COMP}\cdot R_{COMP}\cdot R_{RFBB}\cdot g_m}{(C_{HF}+C_{COMP})\cdot (R_{FBB}+R_{FBT})}$

5.3 Open-Loop Modeling

These equations model the open-loop transfer function of the control loop.

Table 5-3. Open-Loop Modeling Equations

	Simplified Formula	Comprehensive Formula
Open-Loop Equations		
Open-Loop Transfer Function	$T(s) = A_M\cdot A_{FB}\cdot \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}\cdot \frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$	$T(s) = A_M\cdot A_{FB}\cdot \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n^2}\right)}\cdot \frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$
Crossover Frequency	$f_{CROSS} = \frac{G_{COMP}\cdot V_{SUPPLY}\cdot g_m\cdot R_{COMP}}{2\pi\cdot A_{CS}\cdot R_{CS}\cdot C_{OUT}\cdot V_{LOAD}^2}$	Use Bode Plot

6 Revision History

Changes from Revision * (June 2020) to Revision A (November 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265