Application Report

LP8864-Q1, LP8864S-Q1, LP8866-Q1, and LP8866S-Q1 Diagnostic Description and Fault Handling Routine

ABSTRACT

The LP8864-Q1, LP8864S-Q1, LP8866-Q1, and LP8866S-Q1 are powerful backlight devices with a huge variety of fault detections and diagnostic features. This document details how to use those fault detections and diagnostic features to bring higher reliability to the system.

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Trademarks

1 Fault Handling Routine

The LP8864-Q1, LP8864S-Q1, LP8866-Q1, and LP8866S-Q1 (hereafter, LP886XX-Q1) devices have a huge variety of fault detections and diagnostic features. The system could make use of all these features to better evaluate the current system condition, making the most suitable decision. It will help to avoid both overacting under minor faults and underacting under critical faults.

However, to fully leverage all those features, a well-organized fault handling routine is needed. The following figure is the recommended software handling routine which works with the LP886XX-Q1 devices.

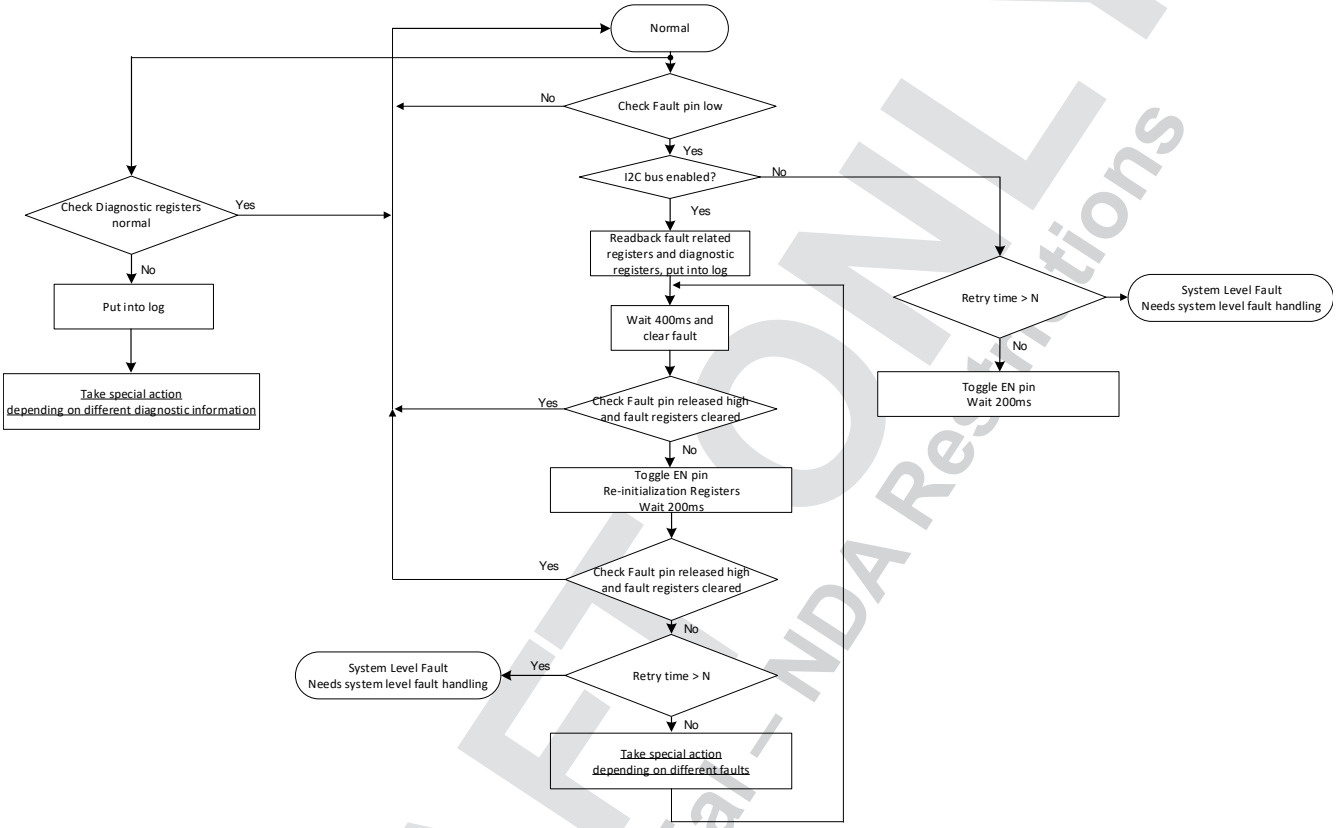

Figure 1-1. Software Recommended Fault Handling Routine

When a fault is detected through the FAULT pin, the software needs to take related action.

Faults can be resolved in the following ways by the fault handling routine:

- Automatically recovered by the internal fault recovery mechanism of the chip
- Recovered by powering cycle the chip
- Recovered by taking corresponding system-level action
- A fault which cannot be recovered by the previous three methods

Higher critical level actions are taken if current level actions do not solve the issue. The details of those specific actions are described in Section 2. The corresponding system-level action to handle faults and incorrect diagnostic information will differ based on different faults detected.

2 Different Fault and Diagnostic Handling Method Recommendation

2.1 Different Fault Handling Method

2.1.1 System Brightness Derating

The following faults can potentially be recovered by system brightness derating:

- V_{IN} Undervoltage Faults (VINUVLO)
- V_{DD} Undervoltage Faults (VDDUVLO)
- Charge Pump Faults (CACAP, CP)
- Boost Overcurrent Faults (BSTOCP)
- Thermal Shutdown Faults (TSD)

These power-related faults are mostly caused by the marginal behavior of the power related blocks. Derating the brightness will decrease the loading of the power blocks. It might help to recover those faults.

The brightness derating action could be removed after a certain period (for example, first time attempt after 1 minute, another attempt after 5 minutes). If no fault after brightness derating action is removed, the system could return to normal.

2.1.2 System-Level Unrecoverable Critical Fault

The following faults indicate that some critical faults have happened. If the fault cannot be recovered by either the auto-fault recovery mechanism or power cycle of the chip, a system power-down is recommended to avoid further hazard occurring. These include:

- V_{IN} Overvoltage Faults (VINOVP)
- V_{IN} Overcurrent Faults (VINOCP)
- Boost Overvoltage Faults (BSTOVPH)
- LED Short to GND Faults (GND_LED)

2.1.3 System-Level Sustainable Fault

The following faults indicate that something is wrong with the system. If only these faults are reported, the system could continue working if the faults cannot be recovered by the automatic fault recovery mechanism of the chip or the power cycle of the chip. These include:

- Boost Sync Clock Invalid Faults (BSTSYNC)
- CRC Error Faults (CRCERR)
- LEDSET Resistor Missing Faults (LEDSET)
- MODE Resistor Missing Faults (MODESEL)
- FSET Resistor Missing Faults (FSET)
- ISET Resistor Out of Range Faults (ISET)
- Open LED Faults (OPEN_LED)
- Short LED Faults (SHORT_LED)
- Invalid LED String Faults (INVSTRING)
- I2C timeout Faults (I2C_ERROR)

Remember that the performance of the system will degrade if it keeps working when these faults are detected, for example:

- System brightness level and uniformity degrade when OPEN_LED or SHORT_LED faults are detected.
- Some additional EMC noise might be generated when BSTSYNC or FSET faults are detected.

The engineer should decide whether the system could keep working with performance degradation based on the specified system requirement.

2.2 Different Diagnostic Wrong Information Handling Method

2.2.1 System-Level Critical Wrong Diagnostic Information

Incorrect diagnostic information might also indicate some critical faults which could not be directly detected by fault detection mechanism of the chip. These include:

- FSM_LIVE_STATUS is always not 10h (NORMAL) when the FAULT pin is not pulled low
- PWM_INPUT_STATUS is not matched with system input
- PWM_OUTPUT_STATUS is not matched with system input
- LED_CURRENT_STATUS is not matched with system input

If any of these critical diagnostic information is wrong, TI recommends power cycling the chip. Do not continue working under these situations.

2.2.2 System Level Sustainable Wrong Diagnostic Information

The following incorrect diagnostic information indicates that something is wrong with the system. If only the following diagnostic information is detected, the system may continue working. These include:

- VBOOST_STATUS calculated voltage is out of expected LED voltage range
- AUTO_PWM_FREQ_SEL is different from system intended settings
- AUTO_LED_STRING_CFG is different from system intended settings
- AUTO_BOOST_FREQ_SEL is different from system intended settings
- MODE_SEL is different from system intended settings

Software could try power cycling the chip once. If the fault is still not recovered, the system may continue working until other faults are detected. However, some problems like brightness degradation, higher EMC, and audible noise might occur if the system keeps working. The engineer should decide whether the system could keep working with such problems based on the specified system requirement.

3 Summary

This application note describes LP886XX-Q1 recommended fault handling routines and corresponding fault or wrong diagnostic information handling methods. System and software engineers are encouraged to use this application note as a reference to implement the corresponding backlight module fault handling mechanism into the system software.

A Fault-Related Functions

A.1 Protection and Fault Detections

The LP886XX-Q1 device device includes fault detections for LED open and short conditions, boost input undervoltage, overvoltage and overcurrent, boost output overvoltage and overcurrent, VDD undervoltage, and die overtemperature. The host can monitor the status of the faults in registers SUPPLY_FAULT_STATUS, BOOST_FAULT_STATUS and LED_STATUS.

A.1.1 Supply Faults

A.1.1.1 V_{IN} Undervoltage Faults (VINUVLO)

The LP886XX-Q1 device supports V_{IN} undervoltage and overvoltage protection. The undervoltage threshold is programmable through external resistor divider on UVLO pin. If during operation of the LP886XX-Q1 device, the UVLO pin voltage falls below the UVLO falling level (0.787 V typical), the boost, LED outputs, and power-line FET will be turned off, and the device will enter STANDBY mode. The VINUVLO_STATUS bit is also set in the SUPPLY_FAULT_STATUS register, and the INT pin is triggered. When the UVLO voltage rises above the rising threshold level the LP886XX-Q1 exits STANDBY and begins the start-up sequence.

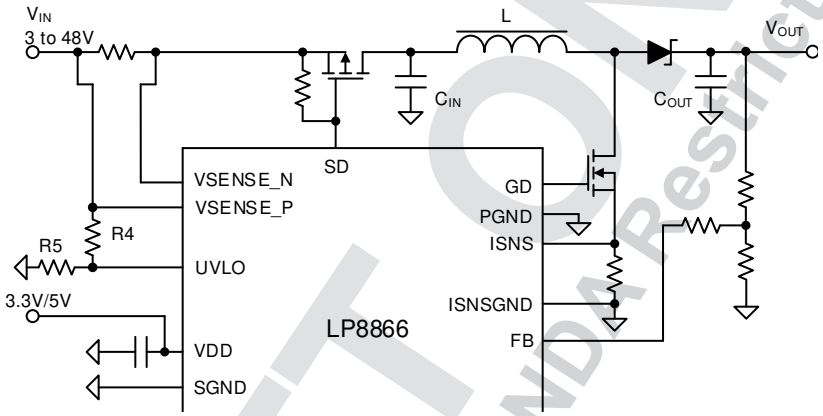

Figure A-1. V_{IN} UVLO Setting Circuit

The following equation is used to calculate the UVLO threshold for VIN rising edge:

$$VIN_{UVLO\_RISING} = \left(\frac{R_4}{R_5} + 1\right) \times VIN_{UVLO\_TH} \quad (1)$$

where

- VIN_{UVLO_TH} = 0.787 V

The hysteresis of UVLO threshold can be designed and calculated with the following equation.

$$VIN_{HYST} = R_4 \times I_{UVLO} \quad (2)$$

where

- I_{UVLO} = 5 µA

So the following equation can be used for UVLO threshold for VIN falling edge:

$$VIN_{UVLO\_FALLING} = VIN_{UVLO\_RISING} - VIN_{HYST} \quad (3)$$

The bottom resistors, R_5 of voltage divider is able to be disconnected to the GND through an additional external N-type of FET as Figure A-2. This design is to minimize the current leakage from VIN in shutdown mode to extend the battery life.

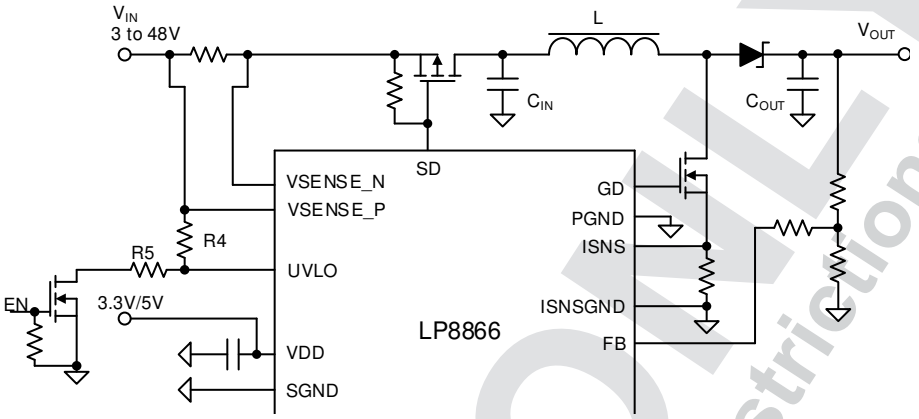

Figure A-2. V_{IN} UVLO Setting Circuit Without Current Leakage Path

A.1.1.2 V_{IN} Overvoltage Faults (VINOVP)

The overvoltage threshold for V_{IN} rising edge is internal fixed at typical 43 V. If during LP886XX-Q1 operation, VSENSE_P pin voltage rises above the OVP rising threshold, boost, LED outputs, and power-line FET will be turned off, and the device will enter STANDBY mode. The VINOVP_STATUS bit will also be set in the SUPPLY_FAULT_STATUS register, and the INT pin will be triggered. When the VSENSE_P pin voltage falls below the falling threshold level, the LP886XX-Q1 exits STANDBY and begins the start-up sequence.

A.1.1.3 V_{DD} Undervoltage Faults (VDDUVLO)

If during LP886XX-Q1 device operation VDD falls below VDDUVLO falling level, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode. The VDDUVLO_STATUS fault bit will be set in the SUPPLY_FAULT_STATUS register, and the INT pin will be triggered. The LP886XX-Q1 recovers automatically to ACTIVE mode when V_{DD} rises above VDDUVLO rising threshold.

A.1.1.4 V_{IN} OCP Faults (VINOCP)

If during LP886XX-Q1 device operation voltage drop on RISENSE resistor rises above 220 mV, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode and then attempt to restart 100 ms after fault occurs. The VINOCP_STATUS fault bit are set in the SUPPLY_FAULT_STATUS register, and the INT pin is triggered.

A.1.1.5 Charge Pump Faults (CPCAP, CP)

If during LP886XX-Q1 device operation voltage of CPUMP pin falls below typical 4.2-V, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode and then attempt to restart 100 ms after fault occurs. The CP_STATUS fault bit will beset in the SUPPLY_FAULT_STATUS register, and the INT pin are triggered.

If during LP886XX-Q1 device operation the charge pump fly capacitor is disconnected or shorted, charge pump are turned off. In result, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode and then attempt to restart 100 ms after fault occurs. Both CPCAP_STATUS and CP_STATUS fault bits are set in the SUPPLY_FAULT_STATUS register, and the INT pin are triggered.

A.1.1.6 Boost Sync Clock Invalid Faults (BSTSYNC)

If the LP886XX-Q1 device is enabled while a valid external SYNC clock is running and BST_SYNC stops or changes to an invalid frequency (< 75 kHz), the LP886XX-Q1 defaults to internal clock frequency selected by BST_FSET resistor and BSTSYNC_STATUS bit will be set. If BST_SYNC input is held high, spread spectrum is enabled. If the SYNC input is held low, the spread spectrum is disabled.

A.1.1.7 CRC Error Faults (CRCERR)

If during LP886XX-Q1 device initialization, the factory default configuration for registers, options and trim bits are not corrected loaded from memory, LP886XX-Q1 keeps operating normally, unless other fault criteria is triggered. The CRCERR_STATUS fault bit are set in the SUPPLY_FAULT_STATUS register and the INT pin are triggered.

A.1.2 Boost Faults

A.1.2.1 Boost Overvoltage Faults (BSTOVPL, BSTOVPH)

Boost overvoltage is detected if the FB pin voltage exceeds the V_{FB_OVPL} threshold. When boost overvoltage is detected, BSTOVPL_STATUS bit will be set in the BOOST_FAULT_STATUS register. The boost FET stops switching, and the output voltage will be automatically limited. If the BSTOVPL_STATUS bit is continually set (that is, reappears after clearing), it may indicate an issue in the application. Boost overvoltage low is monitored during device normal operation (ACTIVE mode).

A second boost overvoltage high fault is detected if the FB pin voltage exceeds the V_{FB_OVPH} threshold or the DISCHARGE pin voltage exceeds the V_{BST_OVPH}. The LP886XX-Q1 device enters the fault recovery state to protect system damage from a high boost voltage. When boost overvoltage is detected, BSTOVPH_STATUS bit is set in the BOOST_FAULT_STATUS register. A fault interrupt is also generated. The device enters STANDBY mode and then attempt to restart after 100 ms. Boost overvoltage high is monitored during device normal operation (ACTIVE mode).

A.1.2.2 Boost Overcurrent Faults (BSTOCP)

Boost overcurrent is detected if the FB pin voltage drops below the V_{UVP} threshold for 110 ms. If the boost overcurrent timer expires before the output voltage recovers, the BSTOCP_STATUS bit is set in the BOOST_FAULT_STATUS register. The fault recovery state is entered, and a fault interrupt is generated. The device will enter STANDBY mode and then attempt to restart after 100 ms. If the BSTOCP_STATUS bit is permanently set, it may indicate an issue in the application. Boost overcurrent is monitored from the boost start, and fault may trigger during boost start-up.

A.1.2.3 LEDSET Resistor Missing Faults (LEDSET)

The LEDSET resistor missing or invalid is detected if the resistor is not assembled or not valid value as requested during the initialization. The LP886XX-Q1 device defaults to 4 (LP8864-Q1 & LP8864S-Q1)/ 6(LP8866-Q1 & LP8866S-Q1)-channel/150 (in LP8864S-Q1 & LP8866S-Q1)/ 200 (in LP8864-Q1 & LP8866-Q1)-mA configuration if the LEDSET resistor is missing or invalid. The LEDSET_STATUS fault bit is set in the BOOST_FAULT_STATUS register. The LEDSET resistor missing or invalid fault will not be monitored after initialization, so that the LP886XX-Q1 is operating in the configuration determined during initialization even though the LEDSET resistor is missing or invalid after initialization.

A.1.2.4 MODE Resistor Missing Faults (MODESEL)

The MODE resistor missing or invalid is detected if the resistor is not assembled or not valid value as requested during the initialization. LP886XX-Q1 defaults to phase-shift PWM mode with I2C address 0x3A (LP8864-Q1 and LP8864S-Q1)/ 0x2A (LP8866-Q1 and LP8866S-Q1) if the MODE resistor is missing or invalid. The MODESEL_STATUS fault bit will be set in the BOOST_FAULT_STATUS register. The MODE resistor missing or invalid fault is not monitored after initialization, so that the LP886XX-Q1 operates in the mode determined during initialization even though the MODE resistor is missing or invalid after initialization.

A.1.2.5 FSET Resistor Missing Faults (FSET)

The FSET resistor missing or invalid for both BOOST_FSET and PWM_FSET is detected if any one of them is not assembled or not a valid value as requested during the initialization. LP886XX-Q1 defaults the switching frequency of boost to 400 kHz if BOOST_FSET resistor is missing or invalid, or PWM dimming frequency to 305 Hz if PWM_FSET resistor is missing or invalid. The FSET_STATUS fault bit is set in the BOOST_FAULT_STATUS register. The FSET resistor missing or invalid fault is not monitored after initialization, so that the LP886XX-Q1 device operates at the boost switching frequency and the PWM dimming frequency determined during initialization even though the FSET resistor is missing or invalid after initialization.

A.1.2.6 ISET Resistor Out of Range Faults (ISET)

If the ISET pin resistor is shorted to GND during normal operation, the maximum current for each LED channel can be calculated in the following equation:

$$I_{LED\_ISET\_FAULT} = \frac{I_{LED\_LIMIT}}{4} \times \left(\frac{LED\_CURRENT[11:0]}{4095} \right) \quad (4)$$

LED_CURRENT[11:0] register will be written to 1/4 of latest programmed data through I2C. The default value of LED_CURRENT[11:0] register is 0xFFF if it is not programmed after device enabling. If ISET pin voltage returns back to above 1.1 V, the LED_CURRENT[11:0] register data is written to latest programmed data through I2C. The ISET_STATUS fault bit will be set in the BOOST_FAULT_STATUS register and the INT pin is triggered.

A.1.2.7 Thermal Shutdown Faults (TSD)

If the die temperature of the LP886XX-Q1 device reaches the thermal shutdown threshold T_{SD}, the boost, power-line FET, and LED outputs on the LP886XX-Q1 shuts down to protect the device from damage. Fault status bit TSD_STATUS bit will be set, and the INT pin will be triggered. The device restarts the power-line FET, the boost, and LED outputs when temperature drops by TSD_HYS amount.

A.1.3 LED Faults

A.1.3.1 Open LED Faults (OPEN_LED)

During normal boost operation, boost voltage is raised if any of the used LED outputs falls below the LED_DRV_HEADROOM threshold level. Open LED fault is detected if boost output voltage has reached the maximum and at least one LED output is still below the threshold. The open string is then disconnected from the boost adaptive control loop and its output is disabled. Any LED fault sets the status bit LED_STATUS and an interrupt is generated unless LED interrupt is disabled. The detail of open LED faults can be read from bits OPEN_LED and LEDx_FAULT (x = 1...4 (LP8864-Q1 & LP8864S-Q1)/ 6 (LP8866-Q1 & LP8866S-Q1)), indicating the faulty LED) in LED_FAULT_STATUS register. These bits maintain their value until device power-down while the LED_STATUS bit is cleared by the interrupt clearing procedure. If a new LED fault is detected, LED_STATUS is set and an interrupt generated again.

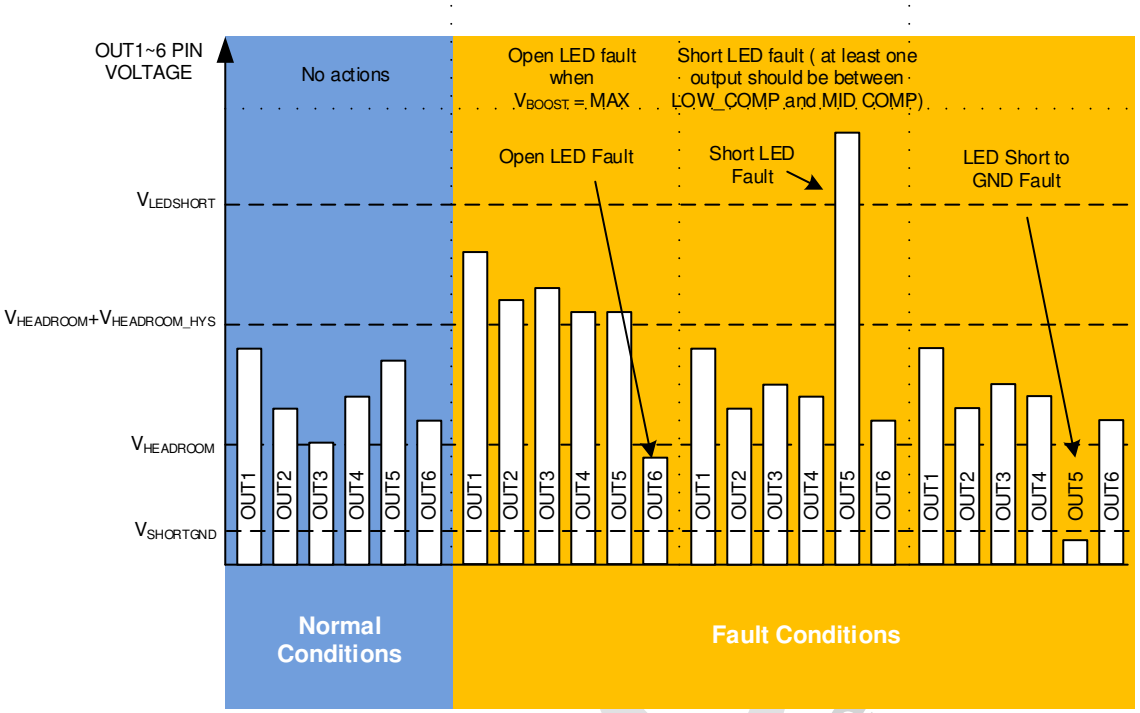

Figure A-3. LED Open and Short Detection Logic

A.1.3.2 Short LED Faults (SHORT_LED)

Short LED fault is detected if one or more LED outputs are above the $V_{LEDSHORT}$ typical 6 V and at least one LED output is inside the normal operation window (see Figure A-3). Shorted string is disconnected from the boost adaptive control loop and the LED PWM output is disabled. LED_STATUS status bit is set and an interrupt generated similarly as in open LED case. Detailed shorted LED fault can be read from bits SHORT_LED and LEDx_FAULT (x = 1...4 (LP8864-Q1 & LP8864S-Q1)/ 6 (LP8866-Q1 & LP8866S-Q1)), indicating the faulty LED) in LED_FAULT_STATUS register.

In HUD application, when output channels are connected as groups and only one or two groups are active, one more special condition will trigger the short LED fault. This is when boost adaptive voltage comes to minimum and one of the LED channels voltage is still higher than $V_{HEADROOM}$ + $V_{HEADROOM\_HYS}$.

A.1.3.3 LED Short to GND Faults (GND_LED)

During power line FET pre-charge state, each active LED output pins outputs a typical 6-mA current for 300-µs period. The LED output pin is recognized as short to GND if its voltage is lower than $V_{HEADROOM}$ in this time period. LED short to GND fault will be reported.

During boost soft start and normal boost operation, if LED output is lower than $V_{SHORTGND}$ for 20 ms, device turns off the corresponding LED output channel and output a typical 6-mA current for 300-µs period again. After this operation, if output voltage is still lower than $V_{HEADROOM}$, LED short to GND fault will be reported.

If LED short to GND is reported, boost, LED outputs and power-line FET is turned off, the device will enter STANDBY mode. LED_STATUS bit is set and an interrupt generated similarly as in open LED case. LED short to GND fault reason can be read from bits LED_GND and LEDx_FAULT (x = 1...4 (LP8864-Q1 & LP8864S-Q1)/ 6 (LP8866-Q1 & LP8866S-Q1)), indicating the faulty LED) in LED_FAULT_STATUS register. These bits maintain their value until device powers are down while the LED_STATUS bit is cleared by the interrupt clearing procedure.

A.1.3.4 Invalid LED String Faults (INVSTRING)

During device initialization, any of un-used LED outputs pins are checked whether connected to GND or not. If they are not connected to GND as expected, the LP886XX-Q1 reports invalid string fault and tries to function normally if possible. The INVSTRING_STATUS fault bit is set in the LED_FAULT_STATUS register, and the INT pin is triggered. The LEDSET resistor missing or invalid fault is not detected after initialization, so that the LP886XX-Q1 operates in the configuration determined during initialization even though the LEDSET resistor is missing or invalid after initialization.

A.1.3.5 I2C Timeout Faults

If chip receives I2C command without STOP signal for 500 ms, I2C communication block auto resets and waits for the next command. I2C_ERROR_STATUS fault bit is set in the LED_FAULT_STATUS register, and the INT pin is triggered.

A.2 Programming Examples

A.2.1 Clearing Fault Interrupts

The LP886XX-Q1 has an INT pin to alert the host when a fault occurs. If I2C interface is available, the Interrupt Fault Status registers can be read back to learn which fault(s) have been detected. These status bits are located in the SUPPLY_STATUS, BOOST_STATUS and LED_STATUS registers. Each interrupt status has a STATUS bit and a CLEAR bit. To clear a fault interrupt status a 1 must be written to both the STATUS bit and CLEAR bit at the same time.

A.2.2 Disabling Fault Interrupts

By default, most of the LP886XX-Q1 faults trigger the INT pin. Each fault has two INT_EN bits. These bits are located in the SUPPLY_INT_EN, BOOST_INT_EN, and LED_INT_EN registers. If the INT_EN bit is read and returns 2b'10, the INT pin is triggered when that fault occurs. The fault interrupt can be disabled by writing 2b'01 to its INT_EN bits, or it can be enabled by writing 2b'11 to its INT_EN bits. There is also a GLOBAL fault interrupt that can be disabled to prevent any faults from triggering the INT pin.

A.2.3 Diagnostic Registers

The LP886XX-Q1 contains several diagnostic registers than can be read with the serial interface for debugging or additional device information. Table A-2 is a summary of the available registers.

Table A-2. Diagnostic Registers

REGISTER NAME	FUNCTION
FSM_LIVE_STATUS	Current state of the functional state machine
PWM_INPUT_STATUS	Measured 16-bit duty cycle of the PWM pin input
LED_PWM_STATUS	16-bit LED PWM duty cycle from state machine
LED_CURRENT_STATUS	12-bit LED current DAC value from state machine
VBOOST_STATUS	10-bit value for adaptive boost voltage target — value is linear between VBOOST_MIN and VBOOST_MAX calculations
MODE_SEL_CFG	Dimming mode configuration from MODE detection
LED_STRING_CFG	LED string phase configuration from LEDSET detection
BOOST_FREQ_SEL	Boost switching frequency value from BST_FSET detection
PWM_FREQ_SEL	LED PWM frequency value from PWM_FSET detection

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