User's Guide

TPSM846C24 2-Phase Power Module Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPSM846C24DEVM-007 evaluation module (BSR007). This user's guide includes the performance specifications, schematic, bill of materials (BOM), and layout of the EVM.

Table of Contents

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1 Description

The TPSM846C24 device is a synchronous buck power module designed to provide up to 35 A of output current. The TPSM846C24 can be paralleled with two devices to achieve output current up to 70 A. The TPSM846C24 is a highly integrated, DC-DC power module that combines a 35-A DC/DC converter with power MOSFETs, a shielded inductor, some input and output capacitors, and passives into a low profile package. The input voltage range is from 4.5 V to 15 V. The output voltage range is from 0.5 V to 2 V.

This evaluation module is designed to demonstrate the ease-of-use and small printed-circuit-board area that can be achieved when paralleling two TPSM846C24 power modules. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Additionally, control test points are provided for use of the power good, enable control, and undervoltage lockout (UVLO) features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

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2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The polarized input power terminal block (TB1) is used for connection to the host input supply. TB2 and TB3 allow four terminals for VOUT and TB4 and TB5 allow four terminals for PGND for connection to the load. These terminal blocks can except up to 12-AWG wire.

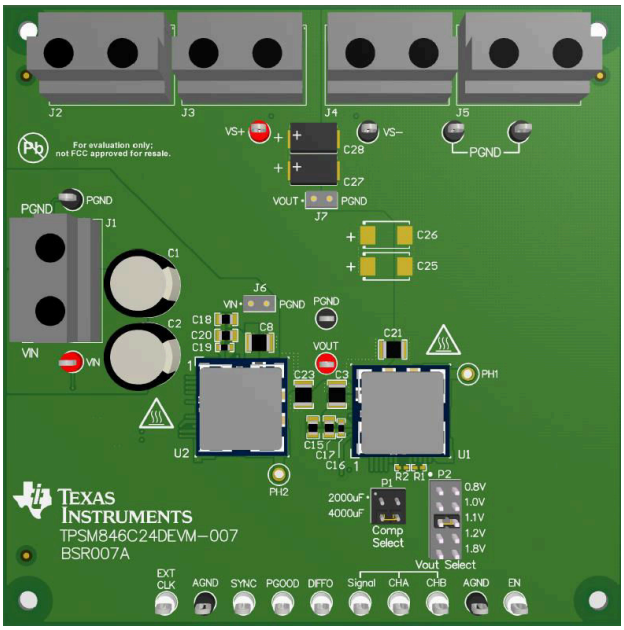

Figure 2-1. EVM User Interface

The VIN monitor (VIN and PGND) and VOUT monitor (VS+ and VS–) test points located near the input terminal block and the output terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure the input and output voltages. Do *not* use these VIN and VOUT monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

The VIN scope (J1) and VOUT scope (J2) test points can be used to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope barrel. The two sockets of each test point are on 0.1-inch centers. Insert the scope probe tip into the socket labeled VIN or VOUT, and insert the scope ground lead into the hole of the socket labeled PGND.

The test points located directly below the device are made available to test the features of the device. Any external connections made to these test points should be referenced to one of the AGND test points located along the bottom of the EVM. Refer to Section 3 for more information on the individual control test points.

The *Vout Select* jumper (P4) is used to set the output voltage. The default loading is the 1.0-V position.

The *Comp Select* jumper (P2) sets the proper frequency compensation for the total amount of output capacitance present on the V_{OUT} bus. The EVM is shipped with approximately 2000 µF of output capacitance loaded on the board. Locations are provided on the board to add another 2000 µF of output capacitance (C28–C31). The default jumper load is the 2000-µF position.

When two TPSM846C24 devices are paralleled, the SYNC pins of the controller and the target must be supplied with a 50% duty cycle external clock signal at the desired switching frequency. A 500-kHz clock is present on the EVM which supplies the required 50% duty cycle signal. The *Controller* device (U1) locks to the rising edge of the clock and the *Target* device (U2) locks to the falling edge of the clock.

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3 Test Point Descriptions

Wire-loop test points and scope probe test points are provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. Table 3-1 provides a description of each test point:

Table 3-1. Test Points

Test Point	Description
VIN	Input voltage monitor. Connect DVM to this point for measuring efficiency.
VS+	Supply path output voltage monitor. Connect DVM positive lead to this point for line regulation and load regulation.
VS–	Return path output voltage monitor. Connect DVM negative lead to this point for measuring line regulation and load regulation.
VOUT	Output voltage monitor. Connect DVM to this point and PGND for measuring efficiency.
PGND	Input and output voltage monitor grounds. Reference the VIN and VOUT DVMs to these ground points.
VIN MON (J1)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT MON (J2)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
AGND	Analog ground point. Use any of the AGND test points as the ground reference for the control signals.
EN	EN pin. Pull to AGND to stop power conversion. Float or pull to 3.3 V to enable power conversion. An internal 10-kΩ pullup resistor to 3.3 V is present on the EVM.
EXT CLK	External clock input. This is the input to a D flip-flop. Apply an external clock at a frequency that is twice the required switching frequency. Remove R13 before applying the clock signal.
SYNC	SYNC monitor pin. This pin is the output of a D flip-flop which supplies a clock to both devices.
PGOOD	Monitors the power good signal of the device. This is an open-drain signal that has an on-board 10-kΩ pullup resistor to 3.3 V.
DIFFO	Output of remote sense differential amplifier
Signal	Signal injection point for the Bode plot analyzer. Inject from Signal to CHB.
CHA	Input signal monitoring point for the Bode plot analyzer
CHB	Output signal monitoring point for the Bode plot analyzer
PH1	Switch node of the TPSM846C24 controller device (U1). Use an unshielded scope probe to monitor this point.
PH2	Switch node of the TPSM846C24 target device (U2). Use an unshielded scope probe to monitor this point.

Note

Refer to *TPSM846C24 4.5-V to 15-V Input, 0.5-V to 2.0-V Output, 35-A Power Module Data Sheet* for absolute maximum ratings associated with features in Table 3-1.

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4 Operation Notes

To operate the EVM, apply a valid input voltage from 4.5 V to 15 V. The output voltage can be set over the range from 0.5 V to 2.0 V.

The Power-Good (PGOOD) indicator of the EVM will assert high when the output voltage is within ±5% of the programmed output voltage value. A 10-kΩ pullup resistor (R18) is populated between the PGOOD pin and the 3V3 pin.

The TPSM846C24DEVM-007 is set-up to operate at 500 kHz. A clock circuit is present on the bottom of the EVM. The clock circuit produces a 500 kHz, 50% duty cycle clock that feeds both devices. If another switching frequency is required, R20 must be removed from the clock circuit on the bottom of the EVM and an external clock must be connected to the EXT CLK test point. The external clock applied to EXT CLK test point must be 2 × the required frequency. The device can be synchronized to an external clock over the frequency range of 300 kHz to 1 MHz. Refer to the *TPSM846C24 4.5-V to 15-V Input, 0.5-V to 2.0-V Output, 35-A Power Module Data Sheet* for further information on synchronization.

The TPSM846C24DEVM-007 includes both input and output capacitors. The EVM includes footprints for adding additional input and output capacitors to the EVM. Adding additional capacitance will improve transient response. The actual capacitance required will depend on the input and output voltage conditions of the particular application, along with the desired transient response. Refer to the product data sheet for further information on input and output capacitance and transient response.

CAUTION

Do *not* change jumper settings while the module is powered. Permanent damage can occur.

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5 Performance Data

Figure 5-1 through Figure 5-3 provide the EVM performance data with the following conditions:

V_{IN} = 12 V, F_{sw} = 500 kHz, C_{OUT} = 4 × 47-µF ceramic plus 4 × 470-µF polymer

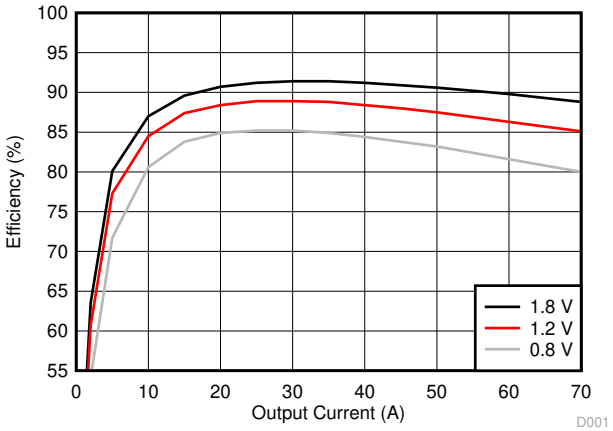

Figure 5-1. Efficiency

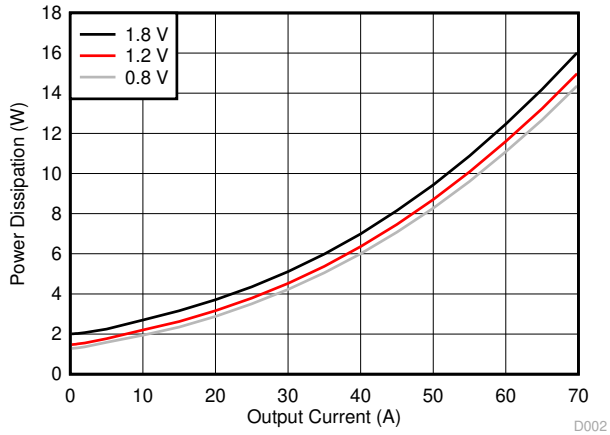

Figure 5-2. Power Dissipation

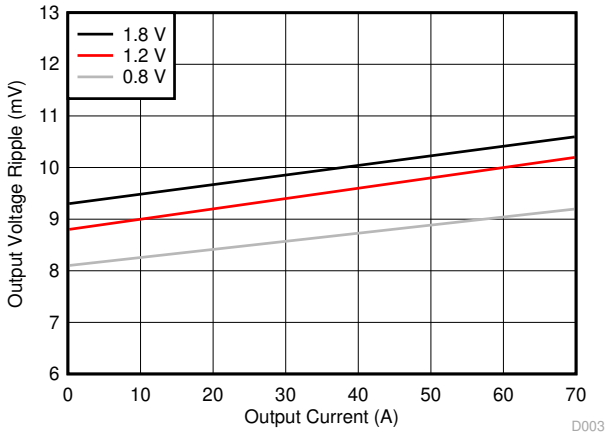

Figure 5-3. Output Voltage Ripple

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6 Schematic

Figure 6-1 illustrates the TPSM846C24DEVM-007 schematic.

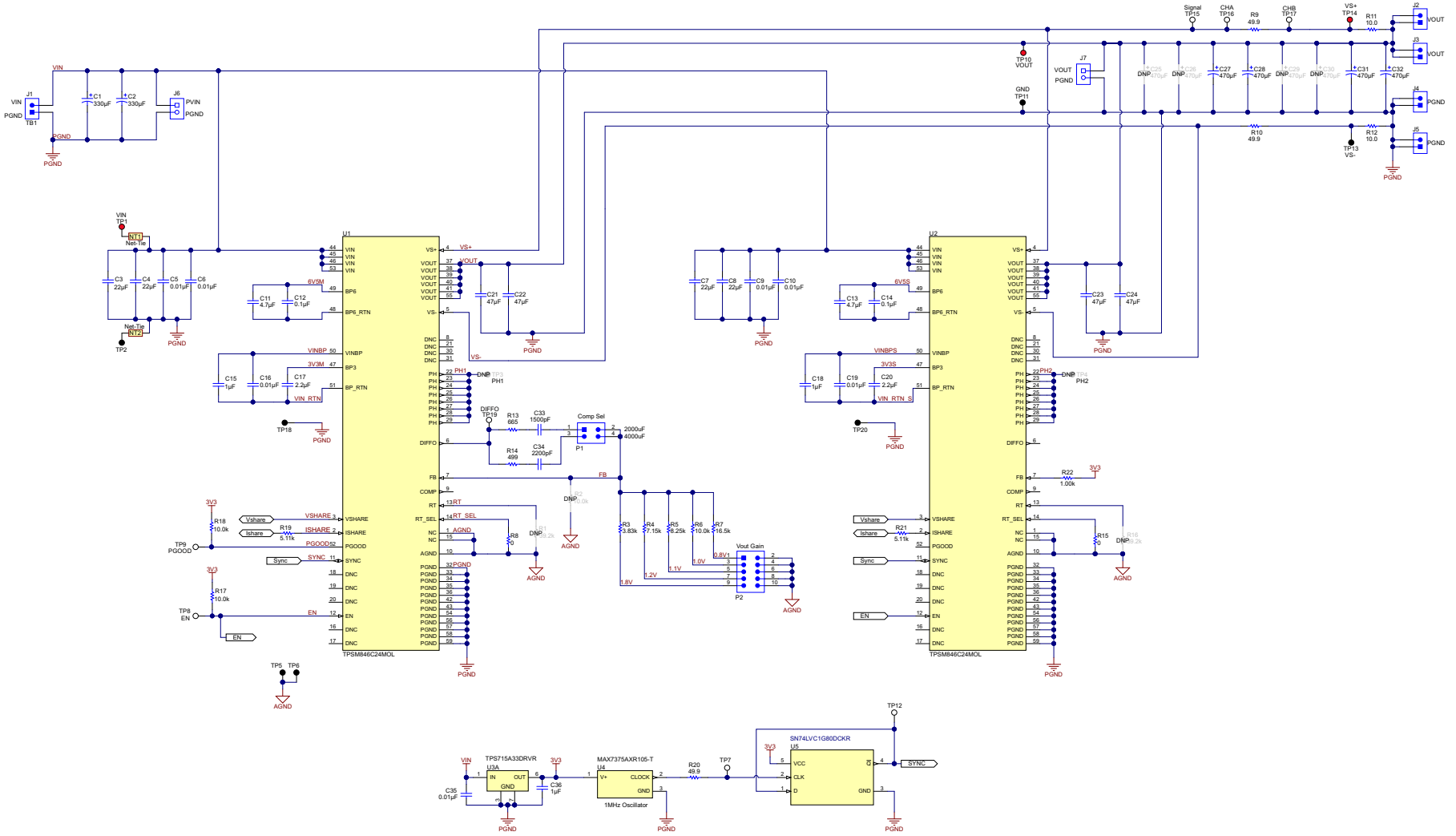

Figure 6-1. TPSM846C24DEVM-007 Schematic

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7 Bill of Material

Table 7-1 lists the EVM BOM.

Table 7-1. TPSM846C24DEVM-007 Bill of Material

Designator	QTY	Description	Part Number	Manufacturer
PCB	1	Printed Circuit Board	—	Any
U1, U2	2	TPSM846C24	TPSM846C24MOL	Texas Instruments
C1, C2	2	CAP, AL, 330 µF, 25 V, ±20%, 0.053 Ω, TH	25ZL330MEFC10X12.5	Rubycon
C3, C4, C7, C8	4	CAP, CERM, 22 µF, 25 V, ±10%, X5R, 1210	GRM32ER61E226KE15L	Murata
C5, C6, C9, C10, C16, C19, C35	7	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	GRM188R71H103KA01D	Murata
C11, C13	2	CAP, CERM, 4.7 µF, 16 V, ±10%, X5R, 0805	GRM21BR61C475KA88L	Murata
C12, C14	2	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0603	GRM188R71C104KA01D	Murata
C15, C18	2	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0805	GRM21BR71E105KA99L	Murata
C17, C20	2	CAP, CERM, 2.2 µF, 16 V, ±10%, X7R, 0805	GRM21BR71C225KA12L	Murata
C21–C24	4	CAP, CERM, 47 µF, 6.3 V, ±20%, X5R, 1210	GRM32ER60J476ME20L	Murata
C27, C28, C31, C32	4	CAP, Tantalum Polymer, 470 µF, 6.3 V, ±20%, 0.01 Ω, 7343-40 SMD	6TPF470MAH	Panasonic
C33	1	CAP, CERM, 1000 pF, 16 V, ±10%, X7R, 0402	GRM155R71C102KA01D	Murata
C34	1	CAP, CERM, 2200 pF, 50 V, ±10%, X7R, 0402	GCM155R71H222KA37D	Murata
C36	1	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	GRM188R71C105KA12D	Murata
C25, C26, C29, C30	0	CAP, Tantalum Polymer, 470 µF, 6.3 V, ±20%, 0.01 Ω, 7343-40 SMD	6TPF470MAH	Panasonic
D1	1	LED, Green, SMD	150060GS75000	Wurth Elektronik
J1, J2	2	Socket Strip, 2 × 1, 100 mil, Black, Tin, TH	310-43-102-41-001000	Mill-Max
P1	1	Header, 2.54 mm, 5 × 2, Gold, TH	AWHW-10G-0202-T	Assman WSW
P2, P4	2	Header, 100 mil, 2 × 2, Tin, TH	PEC02DAAN	Sullins Connector Solutions
R1, R3	2	RES, 0, 5%, 0.063 W, 0402	CRCW04020000Z0ED	Vishay-Dale
R5, R6, R7	3	RES, 121 k, 1%, 0.063 W, 0402	CRCW0402121KFKED	Vishay-Dale
R8	1	RES, 51.1 k, 1%, 0.063 W, 0402	CRCW040251K1FKED	Vishay-Dale
R9, R10, R23	3	RES, 49.9, 1%, 0.1 W, 0603	CRCW060349R9FKEA	Vishay-Dale
R11, R12	2	RES, 10.0, 1%, 0.1 W, 0603	CRCW060310R0FKEA	Vishay-Dale
R13	1	RES, 665, 1%, 0.063 W, 0402	CRCW0402665RFKED	Vishay-Dale
R14	1	RES, 499, 1%, 0.063 W, 0402	CRCW0402499RFKED	Vishay-Dale
R15, R16, R18, R20	4	RES, 10.0 k, 1%, 0.063 W, 0402	CRCW040210K0FKED	Vishay-Dale
R17	1	RES, 4.99 k, 1%, 0.063 W, 0402	CRCW04024K99FKED	Vishay-Dale
R19, R21	2	RES, 5.11 k, 1%, 0.063 W, 0402	CRCW04025K11FKED	Vishay-Dale
R22	1	RES, 1.00 k, 1%, 0.063 W, 0402	CRCW04021K00FKED	Vishay-Dale
R2, R4	0	RES, 39.2 k, 1%, 0.063 W, 0402	CRCW040239K2FKED	Vishay-Dale
TB1–TB5	5	Terminal Block, 30-A, 9.52-mm (.375) Pitch, 2-Pos, TH	OSTT7022150	On-Shore Technology
TP1, TP5, TP6–TP10, TP12, TP15, TP16, TP17, TP19, R24	13	Test Point, Multipurpose, White, TH	5012	Keystone
TP2, TP11, TP13, TP18, TP20–TP23	8	Test Point, Multipurpose, Black, TH	5011	Keystone
TP14	1	Test Point, Multipurpose, Red, TH	5010	Keystone
TP3, TP4	0	Test Point, Multipurpose, White, TH	5012	Keystone
U3	1	Single Output LDO, 80 mA, Fixed 3.3-V Output, 2.5-V to 24-V Input, 6-pin SON (DRV)	TPS715A33DRVR	Texas Instruments
U4	1	1MHz CMOS Silicon Oscillator, SOT-323	MAX7375AXR105-T	Maxim
U5	1	Single Positive-Edge-Triggered D-Type Flip-Flop, (SOT-5)	SN74LVC1G80DCKR	Texas Instruments

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8 PCB Layout

Figure 8-1 through Figure 8-8 display the EVM PCB layout images.

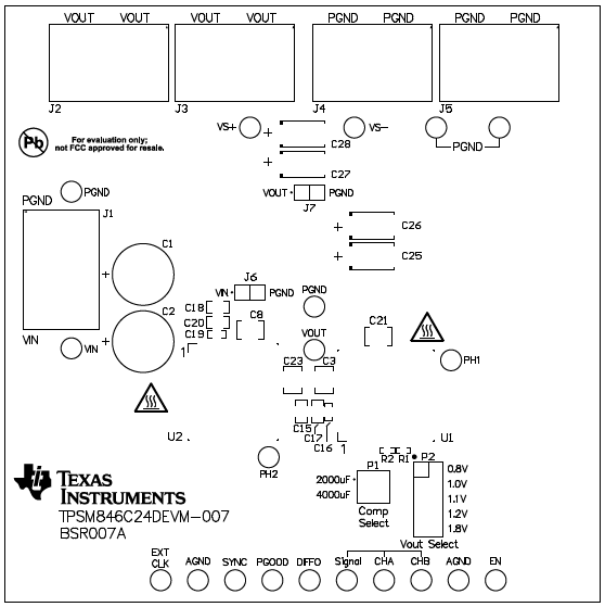

Figure 8-1. Top Components

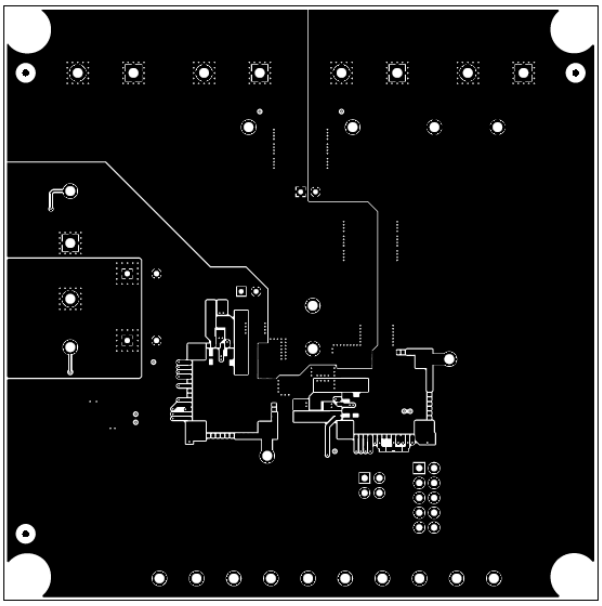

Figure 8-2. Topside Copper

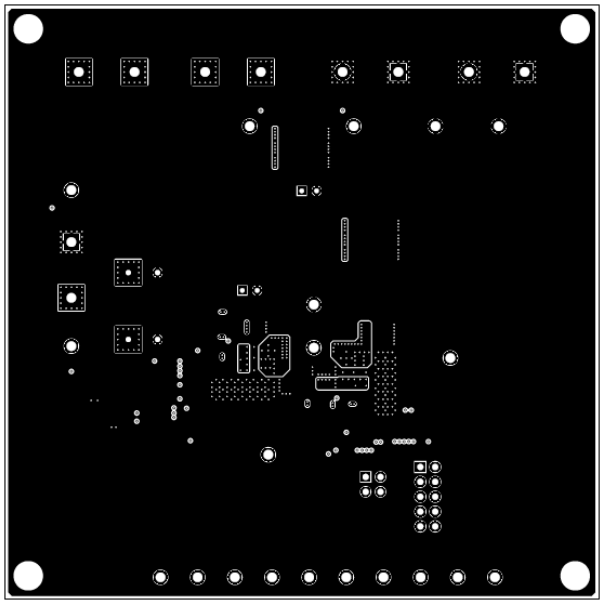

Figure 8-3. Layer 2 Copper

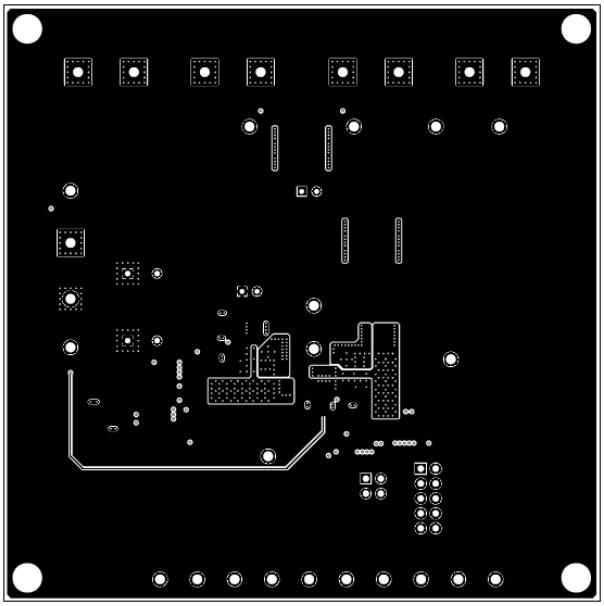

Figure 8-4. Layer 3 Copper

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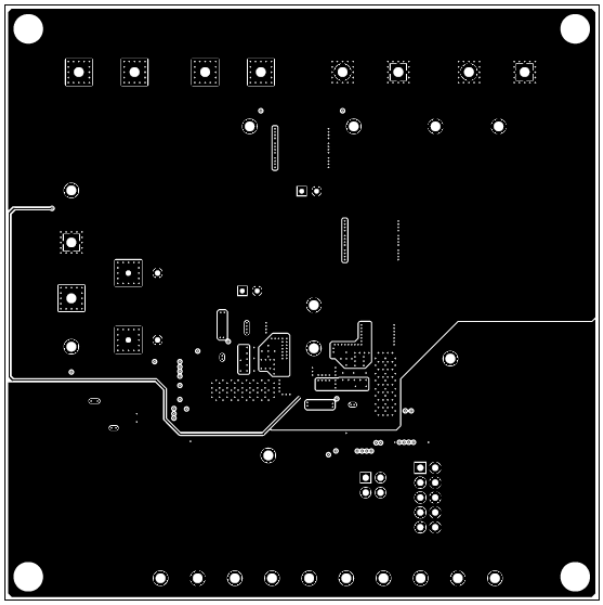

Figure 8-5. Layer 4 Copper

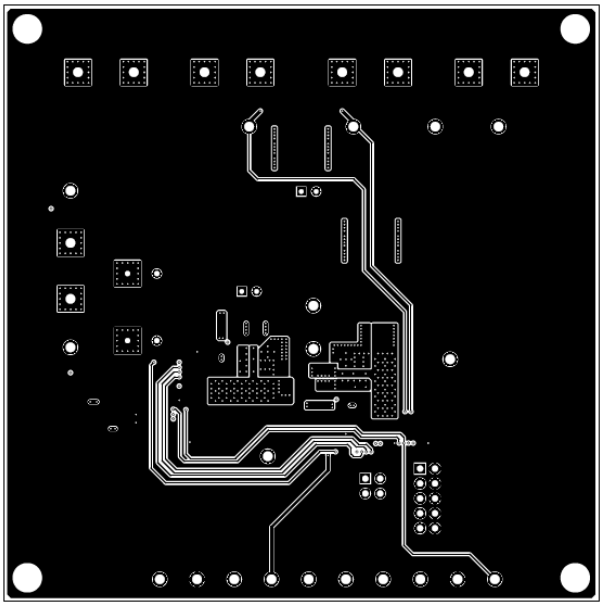

Figure 8-6. Layer 5 Copper

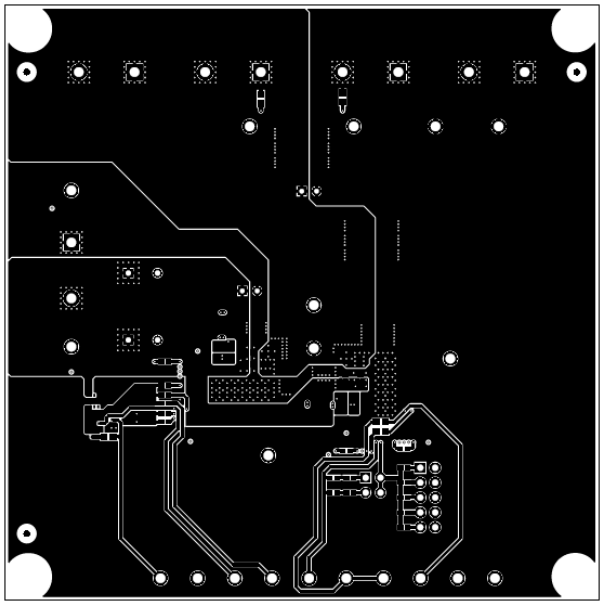

Figure 8-7. Bottom-Side Copper

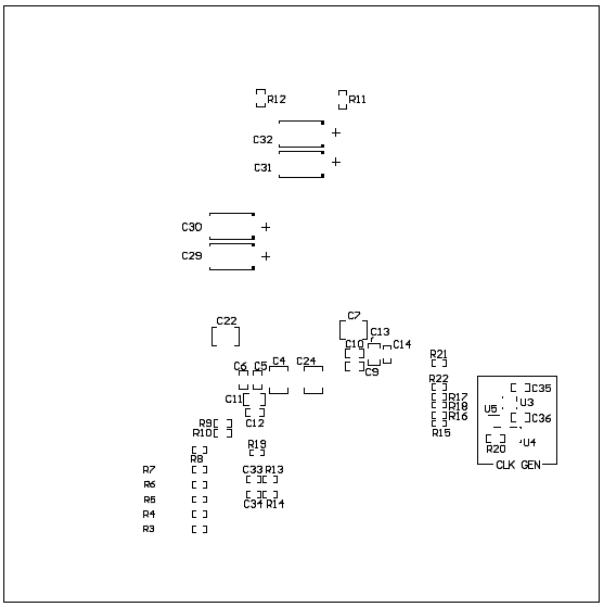

Figure 8-8. Bottom Components (Bottom View)

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2018) to Revision B (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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Changes from Revision * (December 2017) to Revision A (June 2018)	Page
• Corrected resistor references R18 and R20	5

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