User's Guide
SNVU706–February 2020

# LP877020-Q1 Configuration Guide

This configuration guide is designed to help one understand how to use a micro-controller unit (MCU) to configure an LP877020-Q1 PMIC. Instead of requiring a new one-time programmable (OTP) configuration for each design, LP877020-Q1 can be configured at startup through $I^2C$ bus to meet design requirements.

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## Trademarks

# 1 Introduction

The LP877020-Q1 contains one step-up DC/DC converter and two step-down DC/DC converter cores, which are configured as single phase outputs. The device is controlled by an $I^2C$-compatible serial interface and by an enable signal. Typically the settings for the LP877020-Q1 PMIC, such as output voltages, startup and shutdown sequences, and so fourth, are programmed during IC manufacturing by a one time programmable memory (OTP); however, with an MCU this device can also be configured after each start up to fit different design requirements. Default values for the configuration registers (volatile memory) are loaded from the OTP during device power-up, and through $I^2C$ bus the registers can be updated to desired values.

This guide explains how to set up an LP877020-Q1 PMIC to be configured at start up so that it can be used in different designs, without the need for a new OTP. For device specifications and detailed functionality, please refer to the device datasheet. *LP87702-Q1 Dual Buck Converter and 5-V Boost With Diagnostic Functions*

# 2 Setup

There are a few important connections to ensure the LP877020-Q1 is configured correctly, each of which are described in this section. A good example of how to connect an MCU to the LP877020-Q1 PMIC is shown in Figure 1.

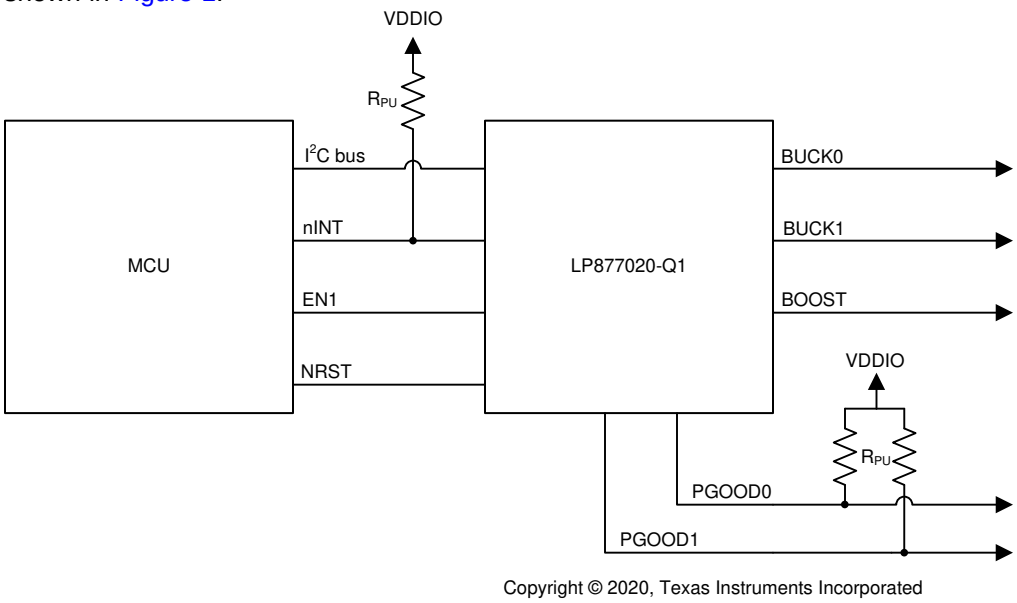




**Figure 1. Typical MCU Connection to LP877020-Q1 for Start-Up Configuration**

## 2.1 SCL/SDA Pins

The SCL and SDA lines (pins 20 and 21, respectively) are used to communicate between the MCU and the LP877020-Q1 PMIC using an $I^2C$ compatible Interface. The $I^2C$ compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP877020-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz). For all $I^2C$ protocol details refer to the device datasheet.

## 2.2 NRST Pin

The NRST pin (pin 11) is used to reset the device logic/enable device internal logic and IO interface. When the NRST voltage is below threshold level all power switches, references, controls, and bias circuitry of the LP877020-Q1 device are turned off. When NRST is set to high level (and VANA is above UVLO level) this initiates power-on-reset (POR), OTP reading and enables the system I/O interface. The $I^2C$ host must allow at least 1.2 ms before writing or reading data to the LP877020-Q1. Device enters STANDBY-mode after internal startup sequence. The host can change the default register setting by $I^2C$ if needed. One or more of the regulators can be enabled or disabled by EN1 pin or by $I^2C$ interface.

## 2.3 EN1 Pin

The EN1 pin (pin 19) is used to start the buck and boost converters startup sequence based on programmed timing. Shutdown times can be programmed as well. It is recommended that the EN1 pin be driven low to until the device is configured to the desired settings. Drive EN1 pin low to disable and high to enable when programmed as enable signal.

## 2.4 nINT

The nINT pin (pin 1) is an open-drain, active low output from the LP877020-Q1 PMIC, and should be connected to a pullup resistor. In the default OTP an interrupt is generated on this pin whenever the RESET_REG_INT bit is set high. The RESET_REG_INT bit is set high when either the VANA supply voltage has decreased below the undervoltage threshold level or the host has requested a reset using the SW_RESET bit in the RESET register or device is reset by NRST or watchdog expiration (depending on watchdog settings). By monitoring the nINT pin, the MCU will know when the PMIC registers are reset to the values determined by the OTP, and can take the necessary actions to ensure that the PMIC is configured as needed.

After a power-on reset the LP877020-Q1 PMIC requires a delay of 1.2 ms before there can be any communication through the $I^2C$ interface. This required delay can be ensured by monitoring the nINT pin. After a power-on reset the nINT pin is high while the registers are reset and the OTP is read to set the registers to their initial values. After 1.2 ms the nINT pin is driven low this signal, that the registers have been reset and can be configured to fit the design requirements.

**NOTE:** To allow monitor the nINT pin correctly, the MCU must clear all interrupts before enabling all of the outputs on the LP877020-Q1 PMIC. Write a 1 to the RESET_REG_INT bit in the INT_TOP2 register to clear this interrupt. If all interrupts are not cleared before enabling the LP877020-Q1 PMIC outputs, then there will be no change on the nINT pin state when an interrupt is generated and the MCU will not be able to detect a register reset.

# 3 Configuration

This section describes the default OTP settings, and how to configure these settings to meet design requirements.

## 3.1 Configuration Sequence

Using the setup described in Section 2 allows the MCU to easily configure the LP877020-Q1 PMIC after a power-on reset, or after any event causing a register reset. To ensure this is done correctly follow the sequence described in this section. The following list shows the actions to take in order to ensure the LP877020-Q1 PMIC is configured correctly. These actions should be taken after a power-on reset or a register reset.

1. Power on PMIC. ($V_{VANA}$ > $VANA_{UVLO}$)
2. Set the NRST high.
3. Wait for nINT line to be set low. (Check RESET_REG_INT bit, and set EN1 pin low if necessary.)
4. Set the new configuration using $I^2C$ communication in recommended order. See Section 3.3
    1. Voltage settings
    2. Current limit andRegulator settings
    3. GPO0 settings
    4. Clock sync functions
    5. PGOOD settings
    6. Interrupt settings
    7. Startup and shutdown settings
    8. Set EN1 pin control bits
    9. Set BUCKx_EN bits
    10. Set BOOST_EN bits
5. Clear Interrupts.
6. Set EN1 pin high to startup sequence.

Upon a power-on reset, waiting for the nINT line to be set low ensures that the PMIC is ready for $I^2C$ communication. Waiting for the nINT line to be set low at any other time allows the PMIC to know when a register reset has occurred. The timing diagrams in Figure 2 and Figure 3 show how to configure the LP877020-Q1 PMIC after a power-on reset or register reset has occurred. Once all of the $I^2C$ writes are finished the interrupts should be cleared and the PMIC enabled by the MCU. The MCU can do this by writing a 1 to the RESET_REG_INT bit to clear the interrupt and by pulling the EN1 pin high to turn on the PMIC outputs.

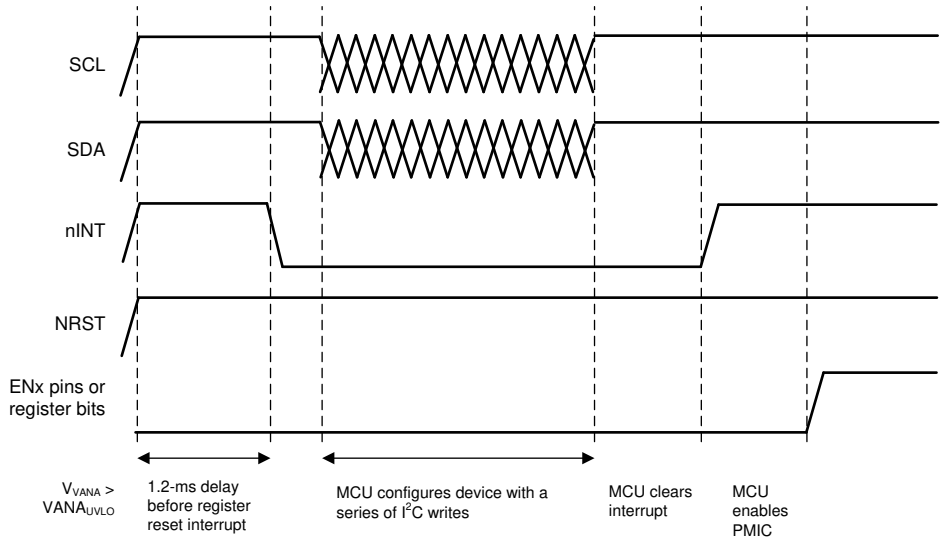


**Figure 2. Configuration Sequence During Startup**

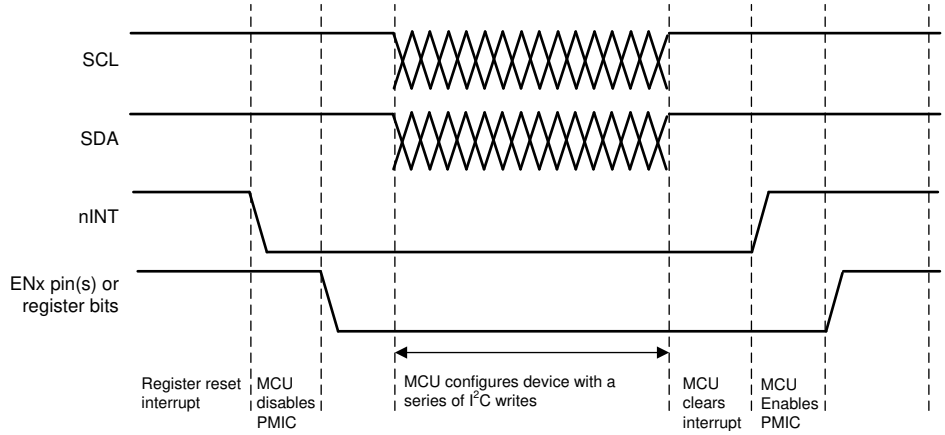


**Figure 3. Configuration Sequence During Reset**

## 3.2 Default OTP Configurations

All LP877020-Q1 PMIC resource settings are stored in the form of volatile registers. These settings define, for example, buck output voltages, boost output voltages, GPO functionality, and power-up and power-down sequences. The OTP by default has no sequencing so that the user can configure the desired sequence. Refer to the datasheet for a full list of the setting registers.

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device.

Table 1 shows device settings for BUCK0, BUCK1, and BOOST. Maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the device datasheets for output capacitance boundary conditions.

**Table 1. BUCK0, BUCK1, and BOOST OTP Settings**

| | Description | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| General settings | Buck phase configuration | | 1 + 1 | No |
| | Switching frequency | | 4 MHz | No |
| | Spread spectrum | EN_SPREAD_SPEC | No | Yes |
| | Startup and shutdown delay range, 0 – 7.5ms / 0 – 15ms | STARTUP_DELAY_SEL, SHUTDOWN_DELAY_SEL | 0 – 15 ms | Yes |
| BUCK0 | Output voltage | BUCK0_VSET | 700 mV | Yes |
| | Enable, EN1 pin or I$^2$C register | BUCK0_EN_PIN_CTRL | I$^2$C | Yes |
| | Control for BUCK0 | BUCK0_EN | Disabled | Yes |
| | Force PWM mode or auto mode | BUCK0_FPWM | Auto | Yes |
| | Peak current limit | BUCK0_ILIM | 4.5 A | Yes |
| | Maximum load current | - | 3.5 A | |
| | Slew rate | SLEW_RATE0 | 3.8 mV/µs | Yes |
| | Startup Delay | BUCK0_STARTUP_DELAY | 0 ms | Yes |
| | Shutdown Delay | BUCK0_SHUTDOWN_DELAY | 0 ms | Yes |
| BUCK1 | Output voltage | BUCK1_VSET | 700 mV | Yes |
| | Enable, EN1 pin or I$^2$C register | BUCK1_EN_PIN_CTRL | I$^2$C | Yes |
| | Control for BUCK1 | BUCK1_EN | Disabled | Yes |
| | Force PWM mode or auto mode | BUCK1_FPWM | Auto | Yes |
| | Peak current limit | BUCK1_ILIM | 4.5 A | Yes |
| | Maximum load current | - | 3.5 A | |
| | Slew rate | SLEW_RATE1 | 3.8 mV/µs | Yes |
| | Startup Delay | BUCK1_STARTUP_DELAY | 0 ms | Yes |
| | Shutdown Delay | BUCK1_SHUTDOWN_DELAY | 0 ms | Yes |
| BOOST | Boost Bypass | | Enabled | No |
| | Enable, EN1 pin or I$^2$C register | BOOST_EN_PIN_CTRL | I$^2$C | Yes |
| | Control for BOOST | BOOST_EN | Disabled | Yes |
| | Peak current limit | BOOST_ILIM | 2.8 A | Yes |
| | Maximum load current | - | 600 mA | |
| | Startup Delay | BOOST_STARTUP_DELAY | 0 ms | Yes |
| | Shutdown Delay | BOOST_SHUTDOWN_DELAY | 0 ms | Yes |

Table 2 lists the device settings for EN1, CLKIN, and GPO0.

**Table 2. EN1, CLKIN, and GPO0 Pin Settings**

| | Description | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| EN1 pin | EN1 pin pulldown resistor enable or disable | EN1_PD | Enabled | Yes |
| CLKIN pin | CLKIN pin pull-down resistor enable or disable | CLKIN_PD | Enabled | Yes |
| | Frequency of external clock when connected to CLKIN | EXT_CLK_FREQ | 2 MHz | Yes |
| | Mode for the internal PLL. When PLL disabled, internal RC OSC is used | EN_PLL | Disabled | Yes |
| GPO0 pin | Output type open drain or push-pull | GPO0_OD | Open drain | Yes |
| | Default state of GPO0 output | GPO0_OUT | Low | Yes |
| | Pin control of GPO0, EN1 pin or I$^2$C register | GPO0_EN_PIN_CTRL | I$^2$C | Yes |
| | Startup Delay | GPO0_ STARTUP_DELAY | 0 ms | Yes |
| | Shutdown Delay | GPO0_ SHUTDOWN_DELAY | 0 ms | Yes |

Table 3 shows device settings for PGOOD.

**Table 3. PGOOD OTP Settings**

| | Description | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| Signals monitored by PG0 | Thermal warning | SEL_PG0_TWARN | No | Yes |
| | Input voltage monitor of VMON1 | SEL_PG0_VMON1 | No | Yes |
| | Input voltage monitor of VMON2 | SEL_PG0_VMON2 | No | Yes |
| | Input voltage monitor of VANA | SEL_PG0_VANA | No | Yes |
| | Output voltage monitor of BUCK0 | SEL_PG0_BUCK0 | No | Yes |
| | Output voltage monitor of BUCK1 | SEL_PG0_BUCK1 | No | Yes |
| | Output voltage monitor of BOOST | SEL_PG0_BOOST | No | Yes |
| PG0 mode selections | PG0 polarity (active high or active low) | PG0_POL | Active high | Yes |
| | PG0 valid debounce time | PG0_RISE_DELAY | 11 ms | Yes |
| | PG0 signal mode (status or latched until fault source read) | PGOOD_FAULT_GATES_PG0 | Status | Yes |
| | PG0 output mode (push-pull or open drain) | PG0_OD | Open drain | Yes |
| | PG0 operating mode (detecting unusual situations UNUSUAL or showing when requested outputs are not valid UNVALID) | PG0_MODE | Unvalid | Yes |
| Signals monitored by PG1 | Thermal warning | SEL_PG1_TWARN | No | Yes |
| | Input voltage monitor of VMON1 | SEL_PG1_VMON1 | No | Yes |
| | Input voltage monitor of VMON2 | SEL_PG1_VMON2 | No | Yes |
| | Input voltage monitor of VANA | SEL_PG1_VANA | No | Yes |
| | Output voltage monitor of BUCK0 | SEL_PG1_BUCK0 | No | Yes |
| | Output voltage monitor of BUCK1 | SEL_PG1_BUCK1 | No | Yes |
| | Output voltage monitor of BOOST | SEL_PG1_BOOST | No | Yes |
| PG1 mode selections | PG1 polarity (active high or active low) | PG1_POL | Active high | Yes |
| | PG1 valid debounce time | PG1_RISE_DELAY | 11 ms | Yes |
| | PG1 signal mode (status or latched until fault source read) | PGOOD_FAULT_GATES_PG1 | Status | Yes |
| | PG1 output mode (push-pull or open drain) | GPO1_PG1_OD | Open drain | Yes |
| | PG1 operating mode (detecting unusual situations UNUSUAL or showing when requested outputs are not valid UNVALID) | PG1_MODE | Unvalid | Yes |
| PGOOD settings | PGOOD thresholds (Undervoltage or Window (undervoltage and overvoltage)) | PGOOD_WINDOW | Window | Yes |
| | PGOOD VMON1 enable or disable | EN_PGOOD_VMON1 | Disabled | Yes |
| | PGOOD VMON2 enable or disable | EN_PGOOD_VMON2 | Disabled | Yes |
| | PGOOD VANA enable or disable | EN_PGOOD_VANA | Disabled | Yes |
| | PGOOD BUCK0 enable or disable | EN_PGOOD_BUCK0 | Disabled | Yes |
| | PGOOD BUCK1 enable or disable | EN_PGOOD_BUCK1 | Disabled | Yes |
| | PGOOD BOOST enable or disable | EN_PGOOD_BOOST | Disabled | Yes |

Table 4 lists the device settings for thermal warning. Also refer to Table 7 for interrupt settings.

**Table 4. Protections OTP Settings**

| | Description | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| Protections | Thermal warning level (125°C or 140°C) | TDIE_WARN_LEVEL | 125 °C | Yes |
| | Input over-voltage protection | | Enabled | No |

Table 5 shows device settings for I²C and OTP revision ID values.

**Table 5. Device Identification and I²C Settings**

| | Description | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| I²C and OTP values | I²C slave ID (7-bit) | | 0x60 | No |
| | OTP ID | | 0x28 | No |

Table 6 lists device settings for watchdog.

**Table 6. Watchdog OTP settings**

| | Description | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| Watchdog settings | Long open time | WD_LONG_OPEN_TIME | 5 s | Yes |
| | Open time | WD_OPEN_TIME | 100 ms | Yes |
| | Close time | WD_CLOSE_TIME | 100 ms | Yes |
| | Counter for restart | WD_RESET_CNTR_SEL | Disabled | Yes |
| | Read OTP during restart | WD_EN_OTP_READ | Disabled | Yes |
| | Stop at restart if restart flag is active | WD_SYS_RESTART_FLAG_MODE | Status | Yes |
| | Watchdog reset output mode open drain or push pull | WDR_OD | Open drain | Yes |
| | Watchdog reset output polarity | WDR_POL | Active low | Yes |
| | Watchdog disable pin control | WD_DIS_CTRL | Enabled | Yes |
| | Watchdog pull down resistor enable or disable | WDI_PD | Enabled | Yes |

Table 7 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

**Table 7. Interrupt Mask Settings**

| | Interrupt event | Bit Name | LP877020-Q1 | Configurable |
|---|---|---|---|---|
| General | Thermal warning | TDIE_WARN_MASK | Unmasked | Yes |
| | Sync clock appears or disappears | SYNC_CLK_MASK | Masked | Yes |
| | Load measurement ready | I_MEAS_MASK | Masked | Yes |
| | Register reset | RESET_REG_MASK | Unmasked | Yes |
| BUCK0 | PGOOD valid detection | BUCK0_PGR_MASK | Masked | Yes |
| | PGOOD invalid detection | BUCK0_PGF_MASK | Masked | Yes |
| | Current limit triggered | BUCK0_ILIM_MASK | Masked | Yes |
| BUCK1 | PGOOD valid detection | BUCK1_PGR_MASK | Masked | Yes |
| | PGOOD invalid detection | BUCK1_PGF_MASK | Masked | Yes |
| | Current limit triggered | BUCK1_ILIM_MASK | Masked | Yes |
| BOOST | PGOOD valid detection | BOOST_PGR_MASK | Masked | Yes |
| | PGOOD invalid detection | BOOST_PGF_MASK | Masked | Yes |
| | Current limit triggered | BOOST_ILIM_MASK | Masked | Yes |
| VANA | PGOOD valid detection | VANA_PGR_MASK | Masked | Yes |
| | PGOOD invalid detection | VANA_PGF_MASK | Masked | Yes |
| VMON1 | PGOOD valid detection | VMON1_PGR_MASK | Masked | Yes |
| | PGOOD invalid detection | VMON1_PGF_MASK | Masked | Yes |
| VMON2 | PGOOD valid detection | VMON2_PGR_MASK | Masked | Yes |
| | PGOOD invalid detection | VMON2_PGF_MASK | Masked | Yes |

## 3.3 Recommended Order of Configuring Registers Through I²C

This section goes through the main settings that can be changed to fit a specific design, in the recommended order. Refer to the datasheet and Section 3.2 for all of these settings and their corresponding bits or registers.

### 3.3.1 Voltage Settings

By default all of the voltage settings for the converters and monitorings are set to their smallest values. These settings can be changed by writing to the fields listed below. Refer to the datasheet to see how the values of these registers correspond to different voltages.

- BUCK0_VSET field in BUCK0_VOUT register
- BUCK1_VSET field in BUCK1_VOUT register
- BOOST_VSET field in BOOST_CTRL register
- VMON1_THRESHOLD field in PGOOD_LEVEL_1 register
- VMON2_THRESHOLD field in PGOOD_LEVEL_2 register

### 3.3.2 Current Limit and Other Regulator Settings

Each regulator has 2 CTRL registers that can be used to set their current limits, slew rates as well as enable their output discharge resistors or set auto or forced PWM mode. Included in these registers is an BUCKx_EN_PIN_CTRL, BUCKx_EN, BUCKX_RDIS, BUCKx_FPWM, BUCKx_ILIM, BUCKx_SLEW_RATE, BOOST_EN, BOOST_EN_PIN_CTRL, BOOST_RDIS_EN and BOOST_ILIM bits for the regulators. It is recommended to set the BUCKx_EN_PIN_CTRL, BUCKx_EN, BOOST_EN_PIN_CTRL and BOOST_EN bits last to avoid any regulators turning on before configuration is complete. These regulator setting fields are summarized in Table 8. Refer to the datasheet for a full description of all registers and their settings.

**Table 8. Regulator Control Settings Registers**

| Regulator | Register | Fields that should be configured | Fields that should not be configured until the PMIC is ready to be powered up (Section 3.3.2.6) |
|---|---|---|---|
| BUCK0 | BUCK0_CTRL_1 | BUCK0_RDIS_EN, BUCK0_FPWM | BUCK0_EN, BUCK0_EN_PIN_CTRL |
| | BUCK0_CTRL_2 | BUCK0_ILIM[2:0], BUCK0_SLEW_RATE[2:0] | |
| BUCK1 | BUCK1_CTRL_1 | BUCK1_RDIS_EN, BUCK1_FPWM | BUCK1_EN, BUCK1_EN_PIN_CTRL |
| | BUCK1_CTRL_2 | BUCK1_ILIM[2:0], BUCK1_SLEW_RATE[2:0] | |
| BOOST | BOOST_CTRL | BOOST_RDIS_EN | BOOST_EN, BOOST_EN_PIN_CTRL |
| | BOOST_ILIM_CTRL | BOOST_ILIM[1:0] | |

#### *3.3.2.1 GPO Settings*

The LP877020-Q1 device supports one GPO signal (pin 20). Following settings can be adjusted in GPO_CONTROL_1 register

- GPO0_EN_PIN_CTRL defines the control for GPO0 output. Default setting 0x0 => $I^2C$ controlled (GPO_CONTROL_1 register)
- GPO0_OUT defines the polarity of the GPO0, logic low and logic high level. Default setting 0x0 => Logic low level (GPO_CONTROL_1 register)
- GPO0_OD defines the type of the output, either push-pull with VANA level or open-drain. Default setting 0x1 => Open drain output (GPO_CONTROL_1 register)

The GPO0 is defined as output, the logic level of the pin is set by GPO0_OUT bit (in GPO_CONTROL_1 register). The GPO0 output can be configured to include start-up and shutdown sequences. The GPO0 control for a sequence with EN1 signal is selected by GPO0_EN_PIN_CTRL (GPO_CONTROL_1 register). The delays during start-up and shutdown are set by GPO0_STARTUP_DELAY[3:0] and GPO0_SHUTDOWN_DELAY[3:0] bits (in GPO0_DELAY register) in the same way as control of the regulators. Refer to the datasheet for more information on each of the fields in the GPO registers.

#### 3.3.2.2 Clock Sync Functions

The LP877020-Q1 device contains a CLKIN input to synchronize switching clock of the buck and boost regulators with the external clock. Depending on the EN_PLL[1:0] bits (in PLL_CTRL register) and the external clock availability, the external clock is selected and interrupt is generated. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits (in PLL_CTRL register) and it can be from 1 MHz to 24 MHz with 1 MHz steps. The external clock must be inside accuracy limits (–30% / +10%) for valid clock detection. CLKIN pin has been multiplexed with function of watchdog disable (WD_DIS). When CLKIN pin is low level, watchdog is enabled. When CLKIN pin is high level, watchdog is disabled. Refer to the datasheet for more information on this function.

#### 3.3.2.3 PGOOD Settings

The PGOOD output can be used to monitor several signals and has multiple settings to configure as listed below.

- Monitoring of regulator output voltage (individual regulators can be selected)
- Undervoltage only or undervoltage and overvoltage monitoring (window)
- Monitoring output current
- Debounce time setting
- Push-pull or open drain output
- Detecting unusual situations or invalid situations (showing when requested outputs are not valid)
- Gated or continuous operating mode
- Adjustable polarity

Refer to the datasheet for more information on the PGOOD signal functionality.

#### 3.3.2.4 Interrupt Settings

The LP877020-Q1 PMIC has many interrupt signals that can be used to indicate different events including regulator overcurrent events, regulator PGOOD events, regulator short-circuit events, and clock events. The registers containing all of these interrupts are listed as follows:

- INT_TOP_1 register
- INT_TOP_2 register
- INT_BUCK register
- INT_BOOST register
- INT_DIAG register

These interrupts can all be masked or unmasked using the registers below. By default the OTPs defined specifically for $I^2C$ configuration has only RESET_REG_INT unmasked to allow the MCU to know when the PMIC registers are reset to the values determined by the OTP, so the MCU can take the necessary actions to ensure that the PMIC is configured as needed. Other interrupts can be unmasked as is needed. However, unmasking other interrupts will mean that when an interrupt is generated on the nINT line, the interrupt registers must be read to determine what caused the interrupt.

- TOP_MASK_1 register
- TOP_MASK_2 register
- BUCK_MASK register
- BOOST_MASK register
- DIAG_MASK register

#### 3.3.2.5 Startup and Shutdown Sequence

Each of the bucks, boost and GPO0 on the LP877020-Q1 can be set to startup and shutdown in a specific sequence. To configure the desired sequence the STARTUP_DELAY and SHUTDOWN_DELAY fields for each output need to be set to a value between 0x0 and 0xF. The delay time that this value corresponds to depends on the STARTUP_DELAY_SEL bit and SHUTDOWN_DELAY_SEL bit located in the CONFIG register. A value of 0x1 on both of these bits will allow a delay ranging from 0 ms to 15 ms with 1 ms steps. A value of 0x0 on both of these bits will allow a delay ranging from 0 ms to 7.5 ms with 0.5 ms steps. Figure 4 shows an example of how these delays can be used to configure a startup and shutdown sequence, in this case with EN1 signal. Refer to the datasheet for a full description of all registers and their settings.

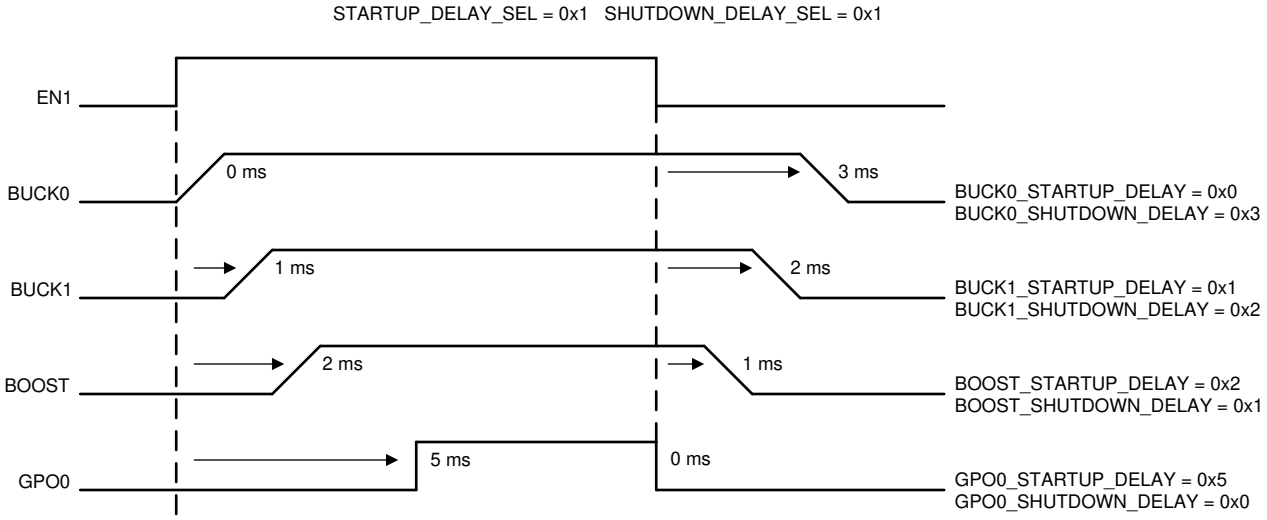


**Figure 4. Startup and Shutdown Sequence Timing Diagram**

#### 3.3.2.6 Set EN1 Pin Control Bits

Each output can be controlled by either $I^2C$ communication, or a combination of $I^2C$ communication and an EN1 pin, as determined by each output's BUCKx_EN_PIN_CTRL and BOOST_EN_PIN_CTRL bits. When controlled via $I^2C$ (BUCKx_EN_PIN_CTRL = 0 and BOOST_EN_PIN_CTRL = 0) the selected output is turned on using the corresponding BUCKx_EN and BOOST_EN bits. Note that the sequencing delay settings will not be effective in this case. When controlled using a combination of $I^2C$ and the EN1 pin (BUCKx_EN_PIN_CTRL = 1 and BOOST_EN_PIN_CTRL = 1), the corresponding BUCKx_EN and BOOST_EN bits must be set high in order to turn on an output. By default the OTP has the BUCKx_EN and BOOST_EN bits and BUCKx_EN_PIN_CTRL and BOOST_EN_PIN_CTRL bits set 0x0 for each output. This prevents the EN1 pin from accidentally setting an output high, and allows the user to choose which outputs to turn on with the EN1 pin.

Once all of the other device settings have been set, the BUCKx_EN_PIN_CTRL and BOOST_EN_PIN_CTRL bits should be set 0x1 for output that needs to be turned on for the design, allowing the EN1 pin to control each desired output.

#### 3.3.2.7 Set BUCKx_EN and BOOST_EN Bits

Once the BUCKx_EN_PIN_CTRL and BOOST_EN_PIN_CTRL bits are set high for each output that needs to be turned on for the design, the BUCKx_EN and BOOST_EN bits for each corresponding output can also be set high. It is important that the BUCKx_EN_PIN_CTRL and BOOST_EN_PIN_CTRL bits are set before the BUCKx_EN and BOOST_EN bits so that no outputs are turned on accidentally. Once the BUCKx_EN and BOOST_EN bits are set high the MCU must be finished with the required $I^2C$ commands and can move on to clearing interrupts and setting the EN1 pin high to start startup sequence as described in Section 3.1.

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