

EVM User's Guide: LM5125EVM-BST

LM5125EVM-BST Evaluation Module



Description

The LM5125EVM-BST evaluation module showcases the features and performance of the LM5125-Q1 wide input voltage synchronous dual-phase boost controller. This EVM is designed for ease of configuration, enabling the user to evaluate different conditions on the module. The standard configuration is designed to provide a 24V/300W output. The output voltage can be dynamically adjusted through the ATRK/DTRK pin.

Get Started

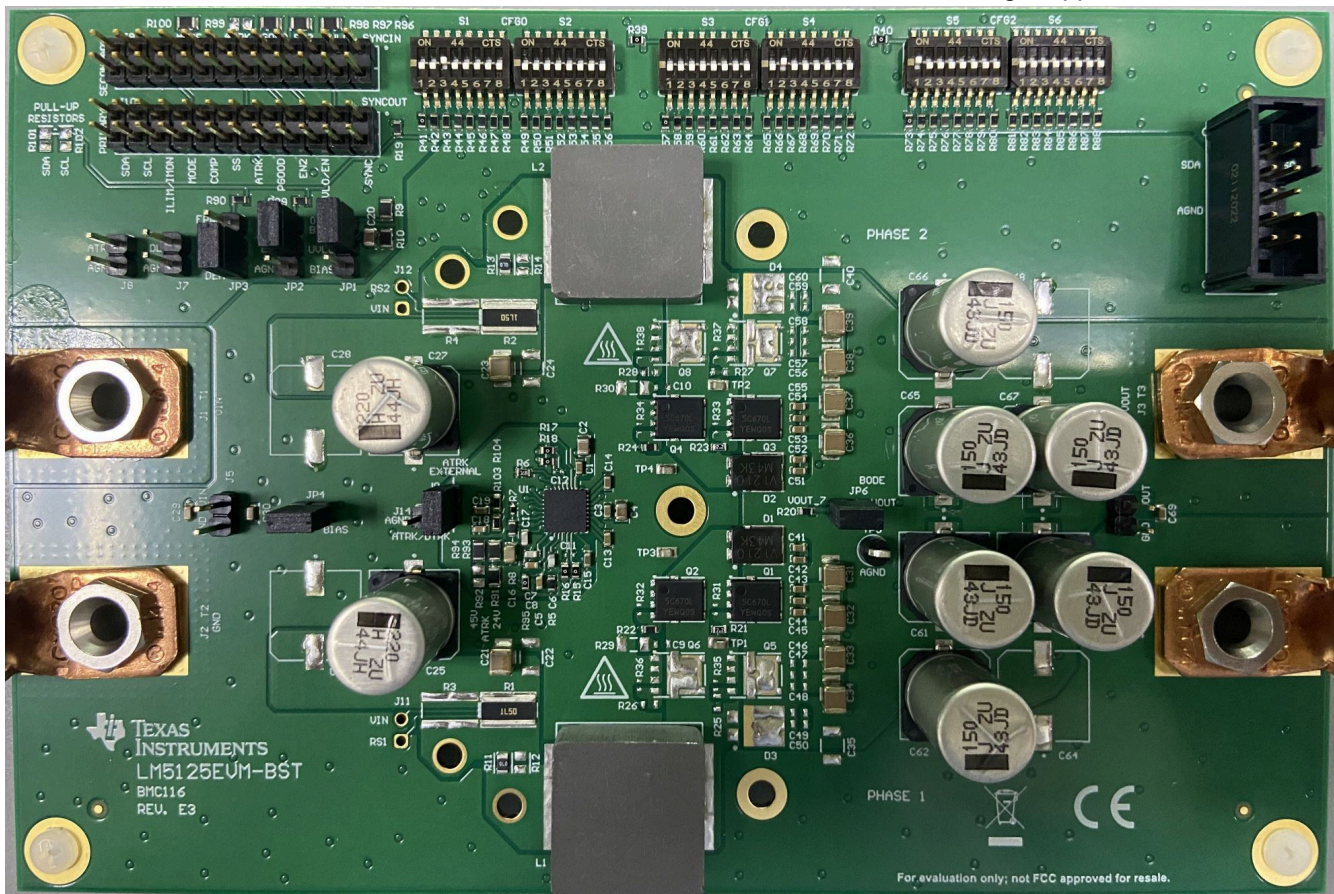
1. Set the jumpers and DIP switches properly
2. Connect EVM to power supply and load

Features

- Two phase interleaved boost converter
- Output voltage tracking from analog/PWM
- Bypass mode
- Optional Dual Random Spread Spectrum (DRSS)
- Programmable undervoltage lockout (UVLO), Soft-start, and dead time
- Comprehensive fault protections
 - Peak current limit
 - Average current limit
 - Over voltage protection
- Stackable with two EVMs

Applications

- Automotive Class H audio power amplifier
- Automotive LED headlight applications



1 Evaluation Module Overview

1.1 Introduction

The LM5125EVM-BST evaluation module provides a fully functional dual phase synchronous boost converter to evaluate LM5125-Q1. The EVM operates over an input voltage range of 8V to 18V and can handle input transients up to 42V. The EVM provides an output voltage of 24V with 300W rated power and 1kW peak power. The output voltage can also be adjusted up to 45V via ATRK/DTRK pin. Two EVMs can be stacked to support 4-phase operation.

1.2 Kit Contents

- One LM5125EVM-BST PCB assembly
- EVM Disclaimer Read Me

1.3 Specification

Table 1-1. EVM Specification

Parameter	Condition	MIN	TYP	MAX	UNIT
Input Voltage	Operation	9	14.4	18	V
Output Voltage	$R_{ATRK} = 40.2k\Omega$		24		V
	$R_{ATRK} = 75k\Omega$		45		V
Rated Output Power	$V_{in} = 14.4V$		300		W
Peak Output Power, 100ms	$V_{in} = 14.4V$		1000		W
Switching frequency			400		kHz
Efficiency	$V_{in} = 14.4V, V_{out} = 24V, P_{out}=300W$		97.5		%
	$V_{in} = 14.4V, V_{out} = 45V, P_{out}=300W$		95.7		%

1.4 Device Information

The LM5125-Q1 is a dual phase synchronous boost controller with below features:

- Wide input voltage range from 2.5V to 42V
- Programmable output voltage 6V to 60V
- Dynamic output voltage tracking
- Bypass mode
- Programmable OVP
- Cycle by cycle peak current limit
- Inductor current monitor
- Average input current limit
- Selectable dead time
- Stackable for 4-phase operation

2 Hardware

2.1 Connector, Jumper, DIP switch and Test point Description

The connectors, jumpers, DIP switches and test points of the EVM are introduced in this section.

2.1.1 Connector Descriptions

Table 2-1. Connectors

Connector	Pin	Description
J1/T1	VIN	Positive power input for the evaluation module
J2/T2	GND	Negative power input for the evaluation module
J3/T3	VOUT	Positive power output for the evaluation module
J4/T4	GND	Negative power output for the evaluation module
J5	1	Input voltage sensing VIN
	2	Input voltage sensing GND
J6	1	Output voltage sensing VOUT
	2	Output voltage sensing GND

2.1.2 Jumper Descriptions

Table 2-2. Jumper Descriptions

Connector	Pins	Description	Default Connection
JP1	1, 2	UVLO/EN pin connected to VIN resistor divider	Y
	2, 3	UVLO/EN pin connected to BIAS	
JP2	1, 2	Phase 2 is turned on	Y
	2, 3	Phase 2 is turned off	
JP3	1, 2	Set to FPWM	
	2, 3	Set to DEM	Y
JP4	1, 2	BIAS pin connected to VIN	Y
JP5	1, 2	RC filter from J8 connected to ATRK/DTRK pin.	Y
JP6	1, 2	Injection signal input for bode plot measurement	Y
J7	1, 2	DLY pin	
J8	1,2	Input to ATRK/DTRK pin. RC filter is inserted.	
J9	1	SYNCIN to the secondary EVM	
	3	No Connection	
	5	UVLO/EN to the secondary EVM	
	7	EN2 to the secondary EVM	
	9	PGOOD to the secondary EVM	
	11	ATRK/DTRK to the secondary EVM	
	13	SS to the secondary EVM	
	15	COMP to the secondary EVM	
	17	MODE to the secondary EVM	
	19	ILIM/IMON to the secondary EVM	
	21	SCL to the secondary EVM	
	23	SDA to the secondary EVM	
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	GND	

Table 2-2. Jumper Descriptions (continued)

Connector	Pins	Description	Default Connection
J10	1	SYNCOUT from the primary EVM	
	3	No Connection	
	5	UVLO/EN from the primary EVM	
	7	EN2 from the primary EVM	
	9	PGOOD from the primary EVM	
	11	ATRK/DTRK from the primary EVM	
	13	SS from the primary EVM	
	15	COMP from the primary EVM	
	17	MODE from the primary EVM	
	19	ILIM/IMON from the primary EVM	
	21	SCL to the primary EVM	
	23	SDA to the primary EVM	
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	GND	
J13	10-pin header	Connector for I ² C operation	

2.1.3 DIP Switch Descriptions

The CFG0 pin defines the dead time and the ATRK/DTRK pin 20 μ A current source for V_{OUT} programming.

Table 2-3. CFG0 Pin Settings

Level	Dead time (ns)	20 μ A ATRK current
1	18	on
2	30	on
3	50	on
4	75	on
5	100	on
6	125	on
7	150	on
8	200	on
9	18	off
10	30	off
11	50	off
12	75	off
13	100	off
14	125	off
15	150	off
16	200	off

The CFG1 pin setting defines the V_{OUT} Over Voltage Protection level, Clock Dithering, the 120% input current limit protection (I_{CL_latch}) operation, and the power good pin behavior.

Table 2-4. CFG1 Pin Settings

Level	OVP bit 0	Clock Dithering Mode	I _{CL} _latch	PGOOD _{OVP} _enable
1	0	enabled (DRSS)	disabled	disabled
2	1	enabled (DRSS)	disabled	disabled
3	0	enabled (DRSS)	disabled	enabled
4	1	enabled (DRSS)	disabled	enabled
5	0	enabled (DRSS)	enabled	disabled
6	1	enabled (DRSS)	enabled	disabled
7	0	enabled (DRSS)	enabled	enabled
8	1	enabled (DRSS)	enabled	enabled
9	0	disabled	disabled	disabled
10	1	disabled	disabled	disabled
11	0	disabled	disabled	enabled
12	1	disabled	disabled	enabled
13	0	disabled	enabled	disabled
14	1	disabled	enabled	disabled
15	0	disabled	enabled	enabled
16	1	disabled	enabled	enabled

The CFG2 pin defines the V_{OUT} Over Voltage Protection level, if the device uses the internal clock generator or an external clock applied at the SYNCIN pin. It configures as well if the device is a single device or part of a dual device configuration, the SYNCIN and SYNCOUT pin is enabled/disabled accordingly. During clock synchronization, the clock dither function is disabled.

Table 2-5. CFG2 Pin Settings

Level	OVP bit 1	Single / Dual chip	Phase 2 Phase Shift	SYNCIN	SYNCOUT	SYNCOUT Phase Shift	Clock Dithering
1	0	Single	180°	off	off	off	CFG1 pin
2	1						
3	0						
4	1	Single external clock	180°	on	off	off	disabled
5	0						
6	1						
7	0	Primary 3-phase	240°	off	on	120°	CFG1 pin
8	1						
9	0	Primary 4-phase	180°	off	on	90°	CFG1 pin
10	1						
11	0	Primary external clock 3-phase	240°	on	on	120°	disabled
12	1						
13	0	Primary external clock 4-phase	180°	on	on	90°	disabled
14	1						
15	0	Secondary	180°	on	off	off	disabled
16	1						

S1 through S6 are 8-bit DIP switches.

- S1 and S2 are for CFG0
 - S1-postion 1 selects Level 1, ..., S1-postion 8 selects Level 8
 - S2-postion 1 selects Level 9, ..., S2-postion 8 selects Level 16
- S3 and S4 are for CFG1

- S3-postion 1 selects Level 1, ..., S3-postion 8 selects Level 8
- S4-postion 1 selects Level 9, ..., S4-postion 8 selects Level 16
- S5 and S6 are for CFG2
 - S5-postion 1 selects Level 1, ..., S5-postion 8 selects Level 8
 - S6-postion 1 selects Level 9, ..., S6-postion 8 selects Level 16

Select position 3 for S1 by default. This selects Level 3 for CFG0:

- Deadtime = 50ns
- 20 μ A ATRK current source = on

Select position two for S4 by default. This selects Level 10 for CFG1:

- OVP bit 0 = 1
- DRSS = disabled
- I_{CL_latch} = disabled
- PGOOD_{OVP_enable} = disabled

Select position 1 for S5 by default. This selects Level 1 for CFG2:

- OVP bit 1 = 0
- Single chip
- Phase shift = 180°
- SYNCIN = off
- SYNCOUT = off

OVP bit 1 = 0 and OVP bit 0 = 1 select OVP level to 50V.

Note

The EVM can be damaged if lower than 50ns dead time is selected or $V_{out} > 50V$. Select OVP level no more than 50V.

2.1.4 Test Points Description

Table 2-6. Test Points Description

Test Point	Name	Description
TP1	SW1	Test point for switch node of phase 1
TP2	SW2	Test point for switch node of phase 2
TP3	GND	Test point for GND
TP4	GND	Test point for GND
TP5	GND	Test point for GND

2.1.5 Easy to Use Features

Output Voltage Tracking

Connect analog tracking voltage signal to J8. A high frequency PWM signal is also acceptable because a two-stage RC filter is inserted.

Set V_{out} to 45V

- Populate R91=0 Ω to set V_{out} to 24V (default)
- Populate R91=0 Ω to set V_{out} to 45V

Refer to [Figure 2-1](#).

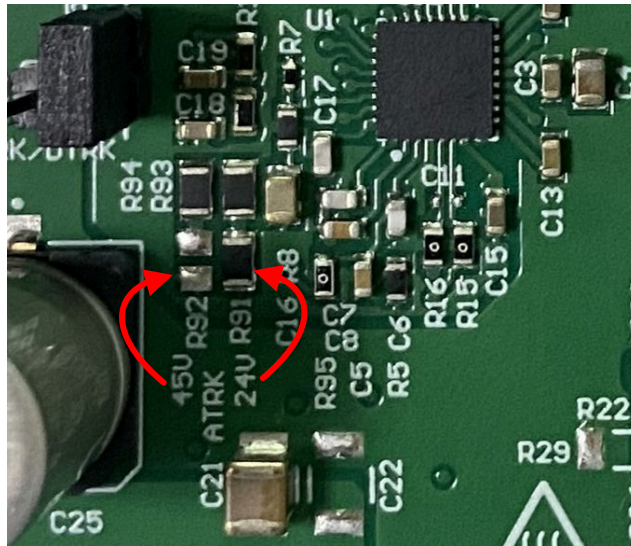


Figure 2-1. Select between 24V and 45V

Observe the inductor current with current probe

Remove R11 and R13, then solder wires in the plated through holes for current probes. Refer to [Figure 2-2](#).

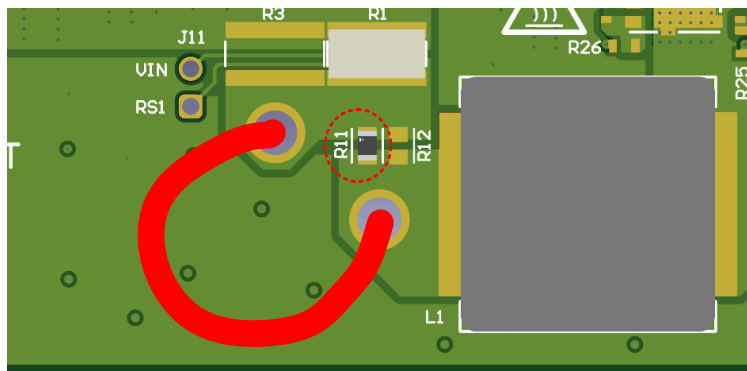


Figure 2-2. Observe the inductor current

3 Implementation Results

3.1 Test Setup and Procedure

3.1.1 Test Setup

Figure 3-1 shows the required test setup to evaluate the EVM.

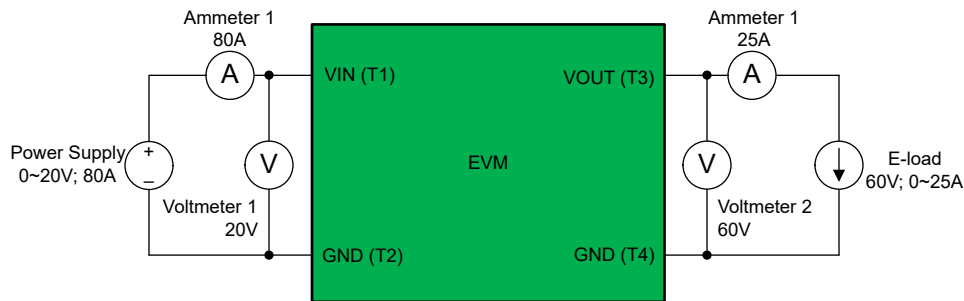


Figure 3-1. EVM Test Setup

The following test equipment is needed:

- Power supply: The power supply needs to support 20V/80A
- Electronic Load: The electronic load need to sink 1000W at 60V
- Multimeters (optional)
 - Voltmeter 1 (V_{IN}): Capable of measuring input voltage of 20V
 - Voltmeter 2 (V_{OUT}): Capable of measuring output voltage of 60V
 - Ammeter 1 (I_{IN}): Capable of 80A DC measurement
 - Ammeter 2 (I_{OUT}): Capable of 25A DC measurement
- Oscilloscope: Minimum 200MHz bandwidth

3.1.2 Configurations for Stacking Two EVMs

1. Connect VIN, VOUT, GND from two EVMs together with short, thick cables, respectively.
2. Select CFG2=Level 9 for the primary EVM for 4-phase interleaving operation. Select CFG2=Level 7 for 3-phase interleaving operation.
3. Select CFG2=Level 15 for the secondary EVM.
4. Connect J10 of the primary EVM and J9 of the secondary EVM with ribbon cable. Refer to Figure 3-2.

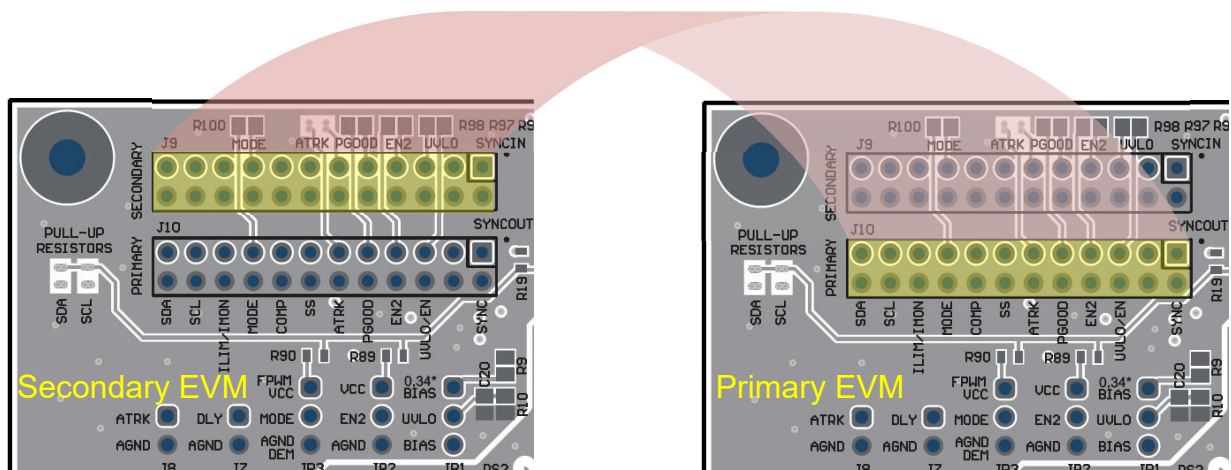


Figure 3-2. Connecting the Primary EVM and Secondary EVM with Ribbon Cable

3.1.3 Test Procedure

1. Make sure the jumpers and DIP switches are set properly.
2. Prepare the setup following Figure 3-1.

3. Set the power supply voltage to 14.4V and the electronic load to 0.1A. The electronic load voltage must be in regulation with a nominal 24V output.
4. The load and input voltage may be changed as required.

3.1.4 Precautions

	<p>Caution</p>	<p>Caution Hot surface. Contact can cause burns. Do not touch!</p>
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4 Application Curves

4.1 Efficiency

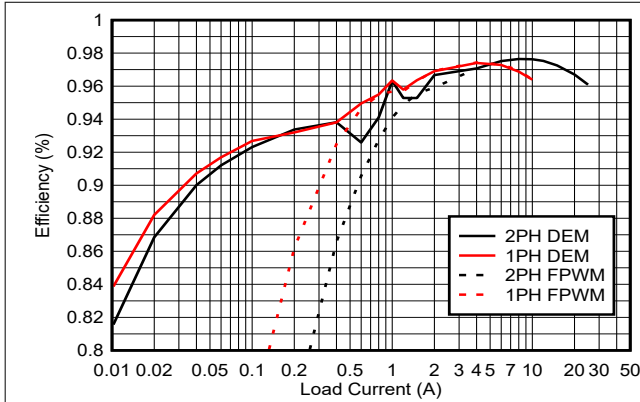


Figure 4-1. Efficiency vs Output Current, $V_{in} = 14.4V$, $V_{out} = 24V$

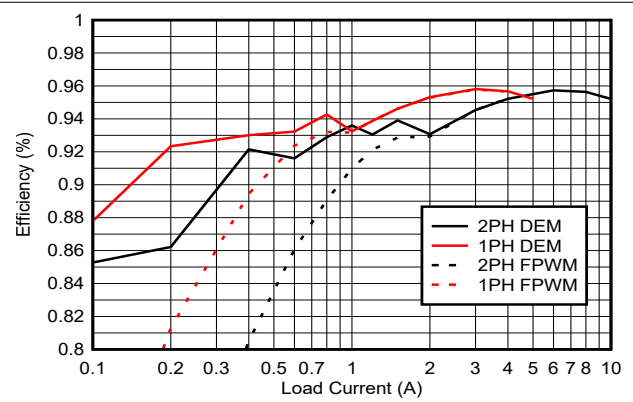


Figure 4-2. Efficiency vs Output Current, $V_{in} = 14.4V$, $V_{out} = 45V$

4.2 Steady State Waveforms

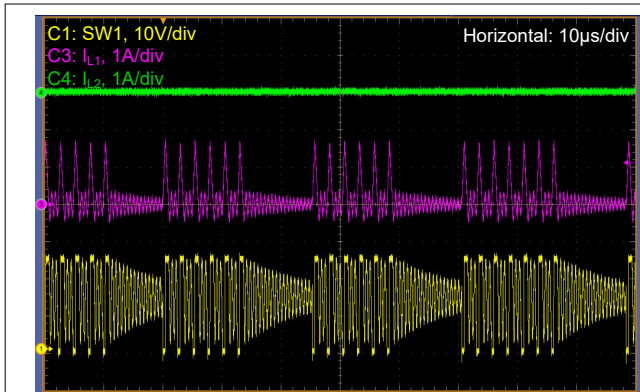


Figure 4-3. $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 0.1A$

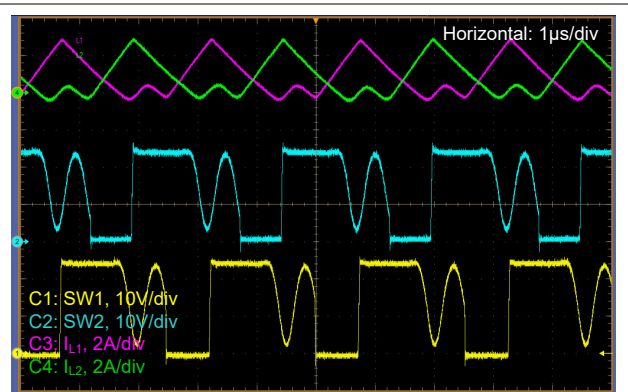


Figure 4-4. $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 1A$

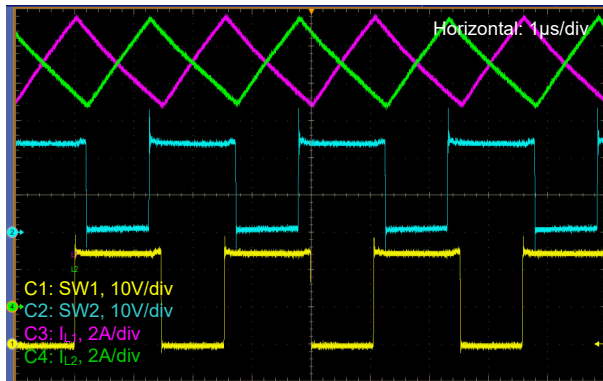


Figure 4-5. $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 15A$

4.3 Step Load Response

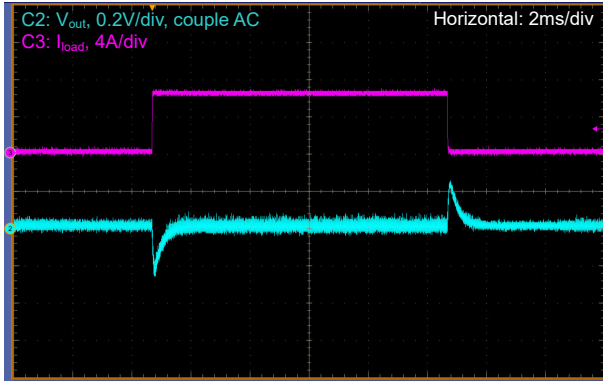


Figure 4-6. Load Transient, $V_{in} = 14.4V$, $V_{out} = 24V$, FPWM, $I_{load} = 0A$ to $6.25A$ at $1A/\mu s$

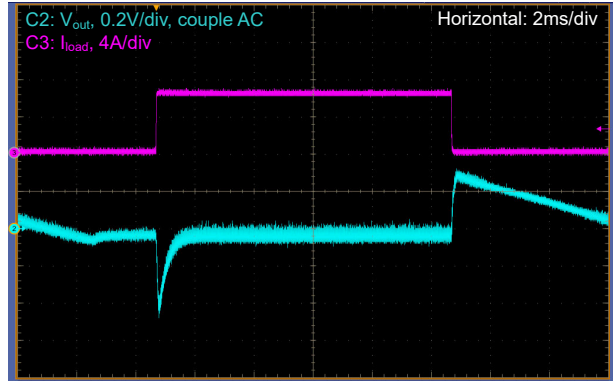


Figure 4-7. Load Transient, $V_{in} = 14.4V$, $V_{out} = 24V$, DEM, $I_{load} = 0A$ to $6.25A$ at $1A/\mu s$

4.4 Sync Operation

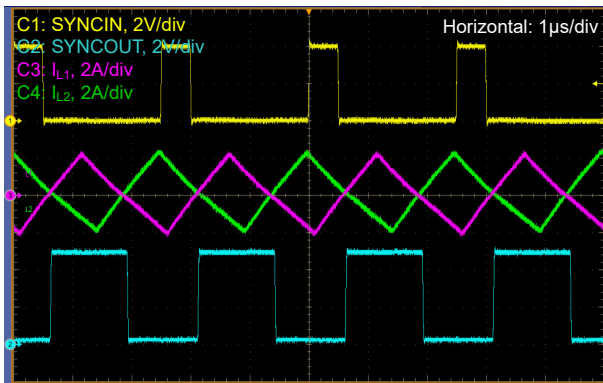


Figure 4-8. $V_{in} = 14.4V$, $V_{out} = 24V$, FPWM, $I_{load} = 0A$, CFG2 = Level 13

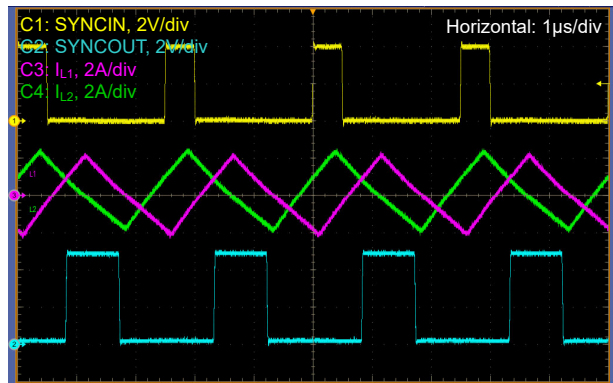


Figure 4-9. $V_{in} = 14.4V$, $V_{out} = 24V$, FPWM, $I_{load} = 0A$, CFG2 = Level 11

4.5 Thermal Performance

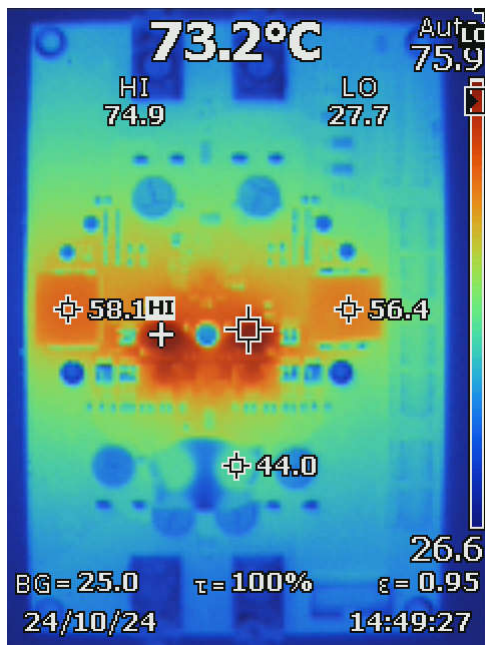


Figure 4-10. $V_{in} = 14.4V$, $V_{out} = 24V$, $P_{OUT} = 300W$,
Natural Convection

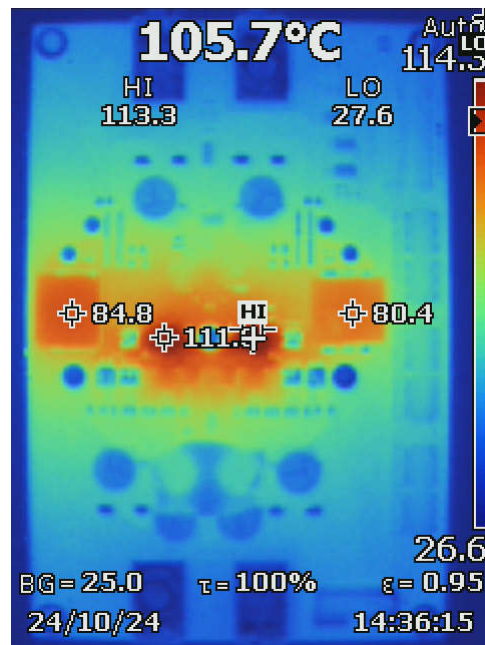
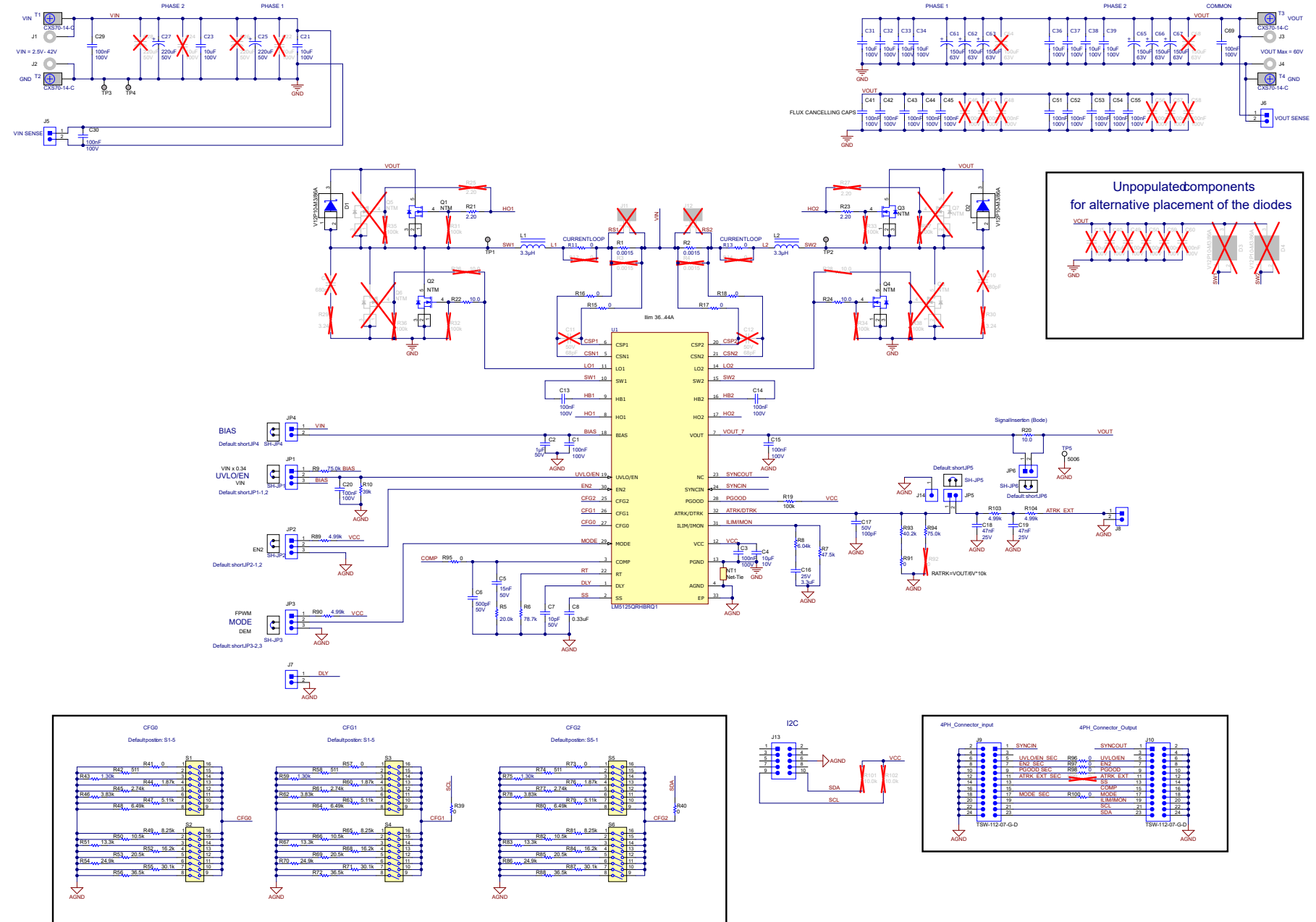


Figure 4-11. $V_{in} = 14.4V$, $V_{out} = 45V$, $P_{OUT} = 300W$,
Natural Convection

5 Hardware Design Files

5.1 Schematic



Copyright © 2024 Texas Instruments Incorporated **Figure 5.1 Schematic**

5.2 PCB Layers

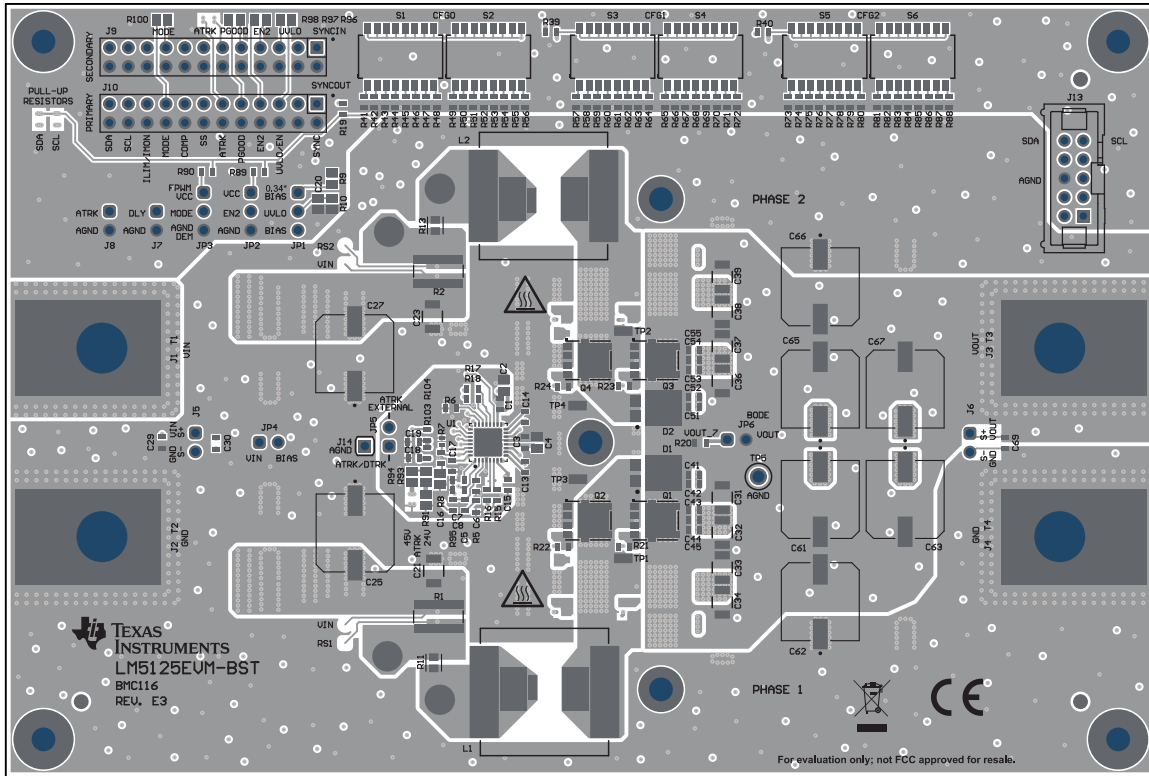


Figure 5-2. Top Silk Screen

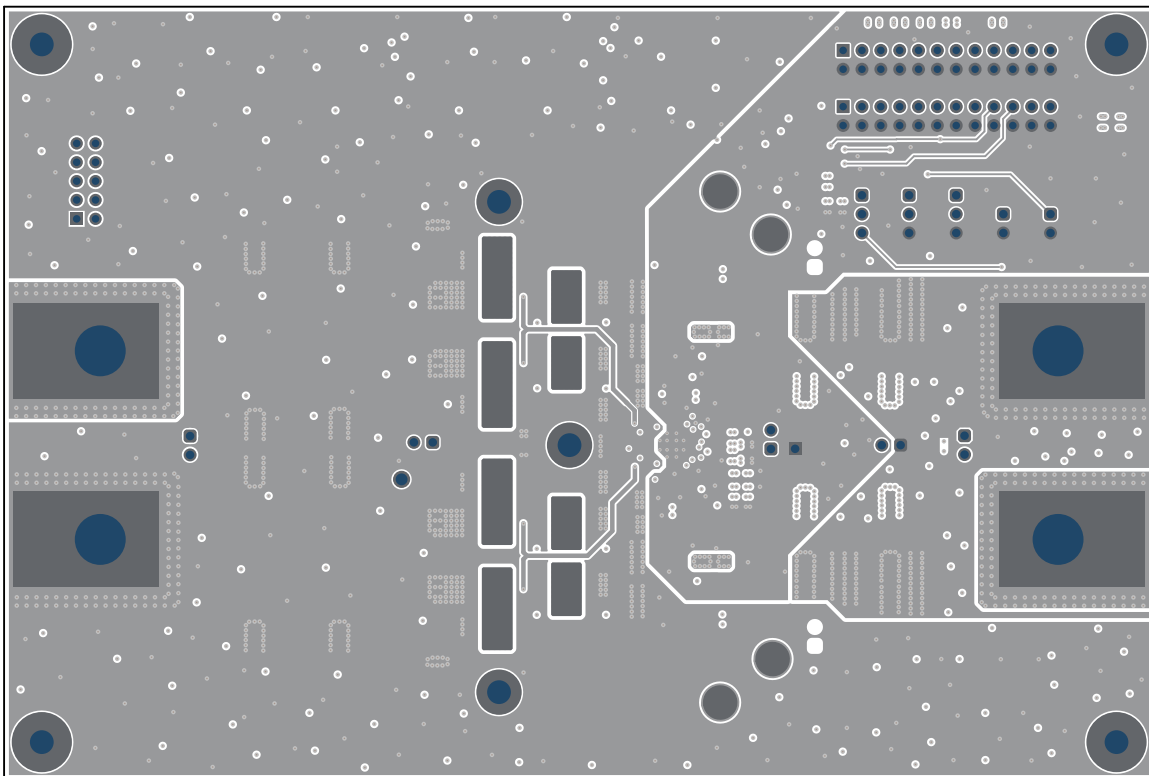


Figure 5-3. Bottom Silk Screen

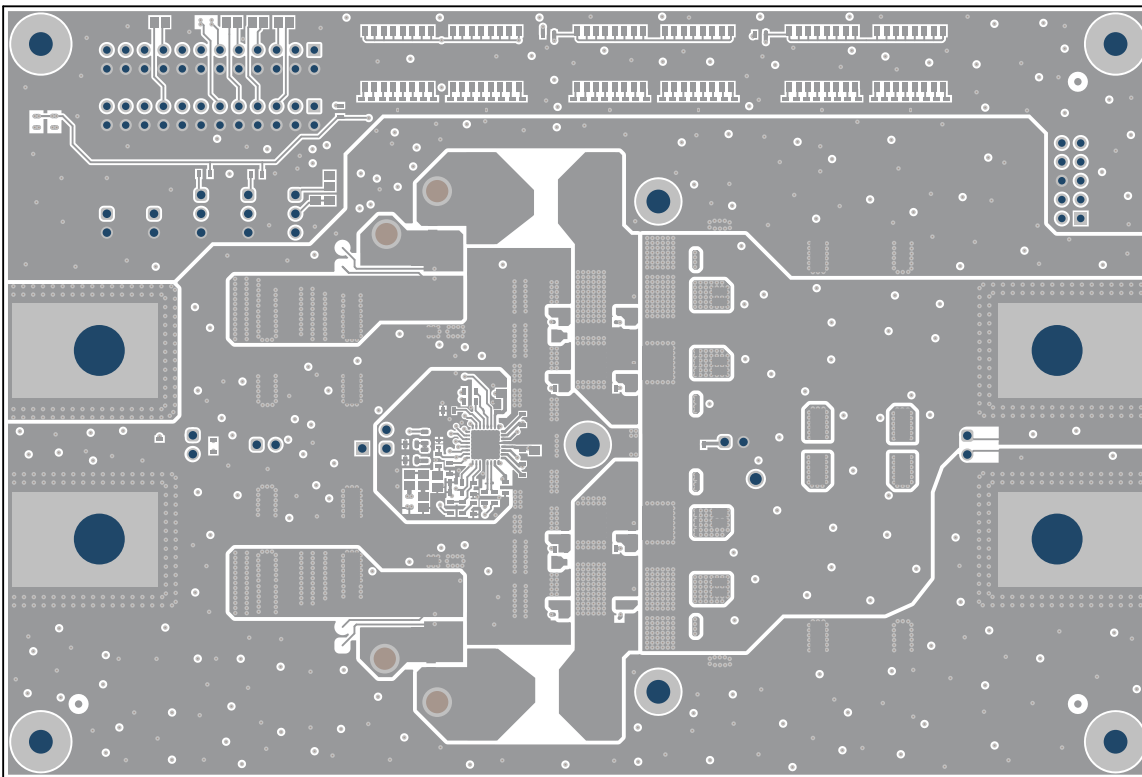


Figure 5-4. Top Layer

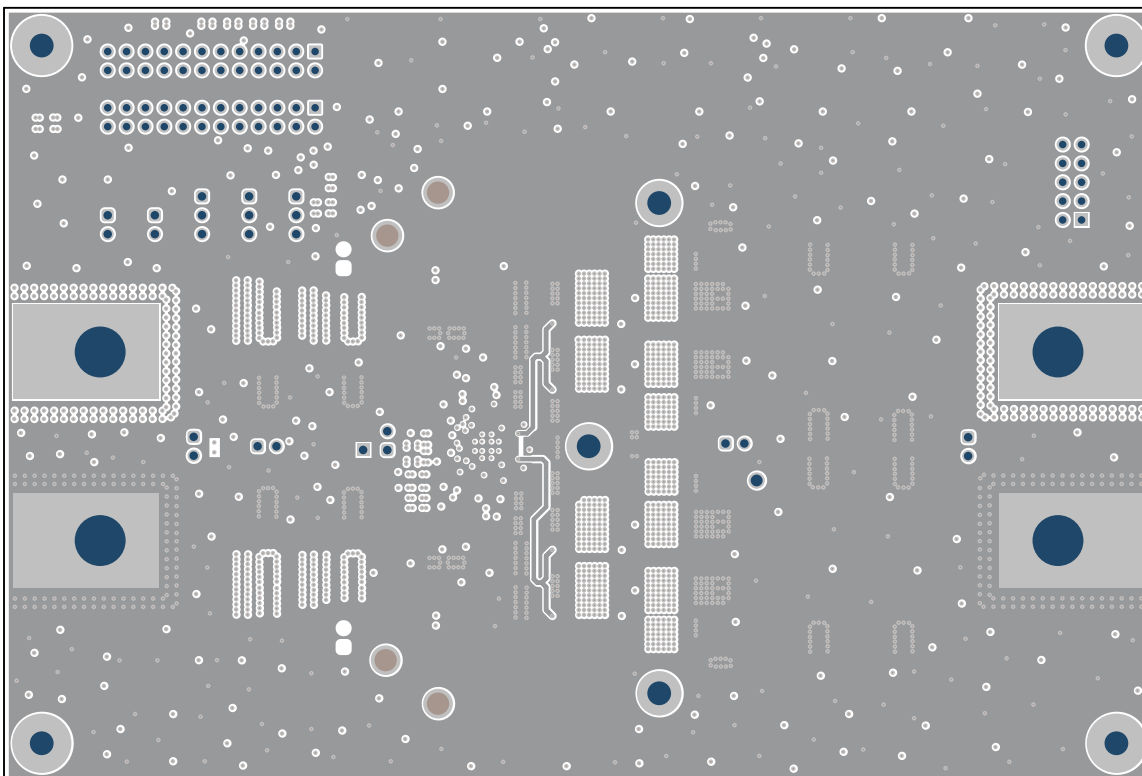


Figure 5-5. Signal Layer 1

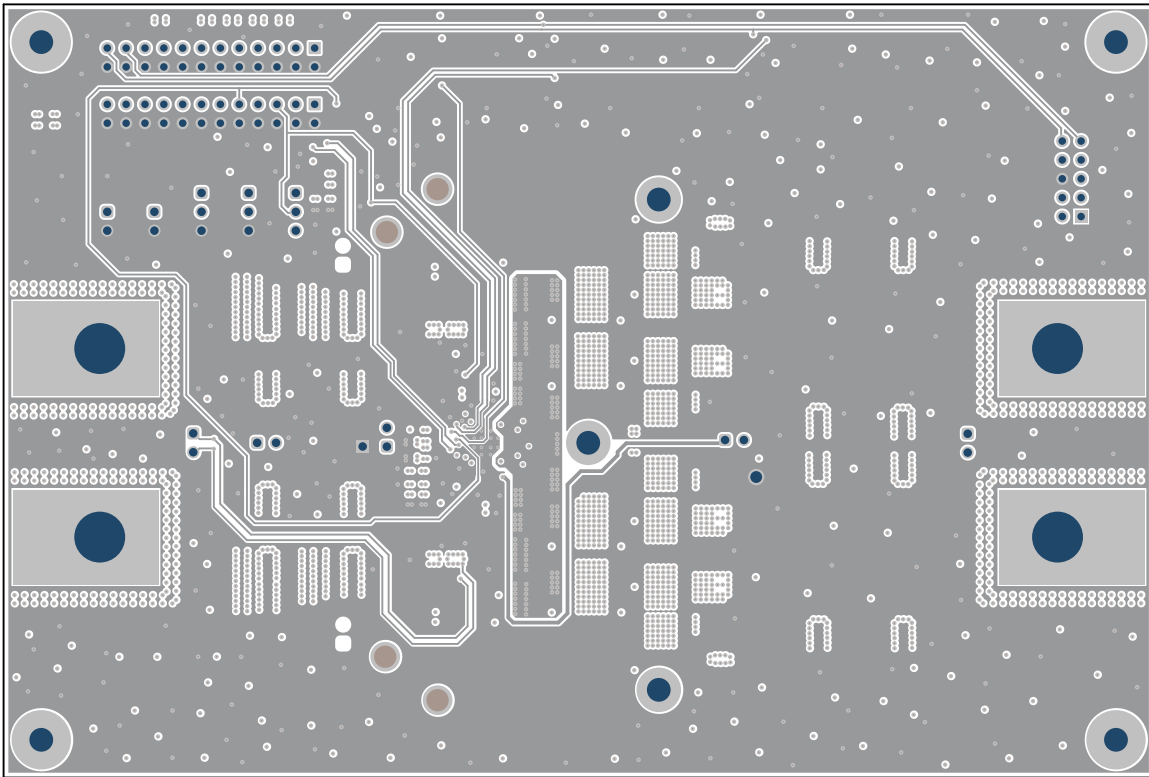


Figure 5-6. Signal Layer 2

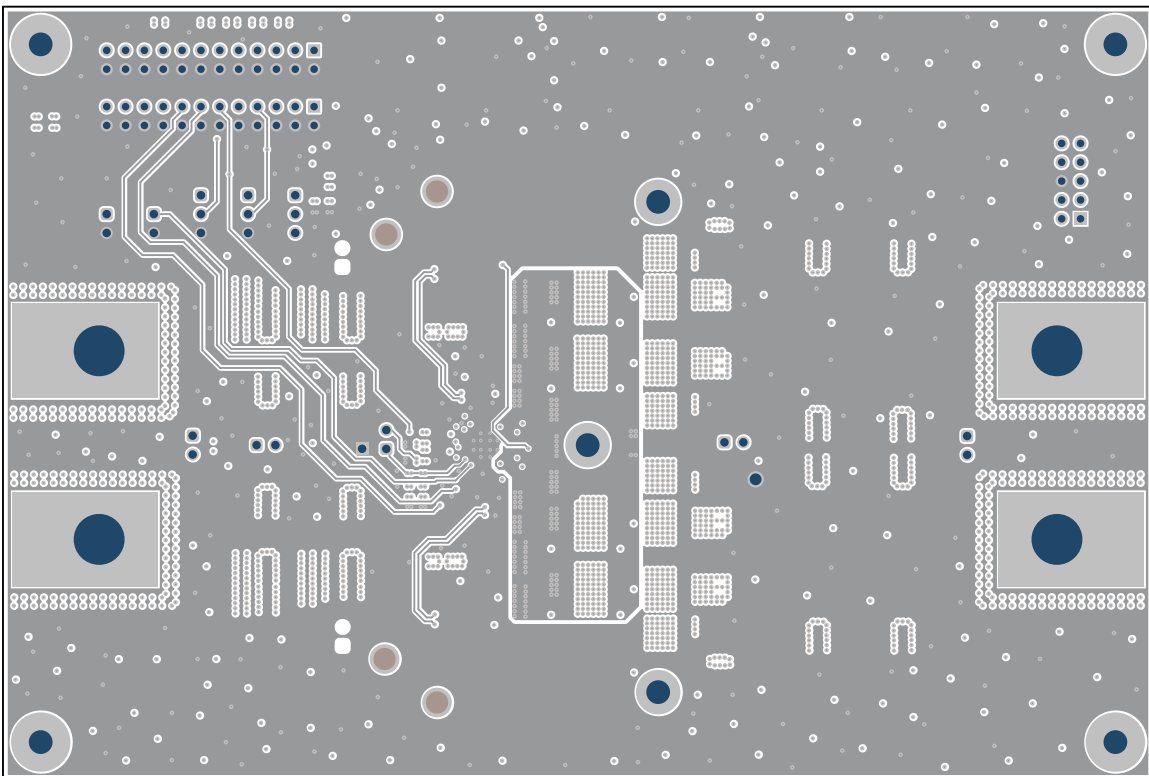


Figure 5-7. Signal Layer 3

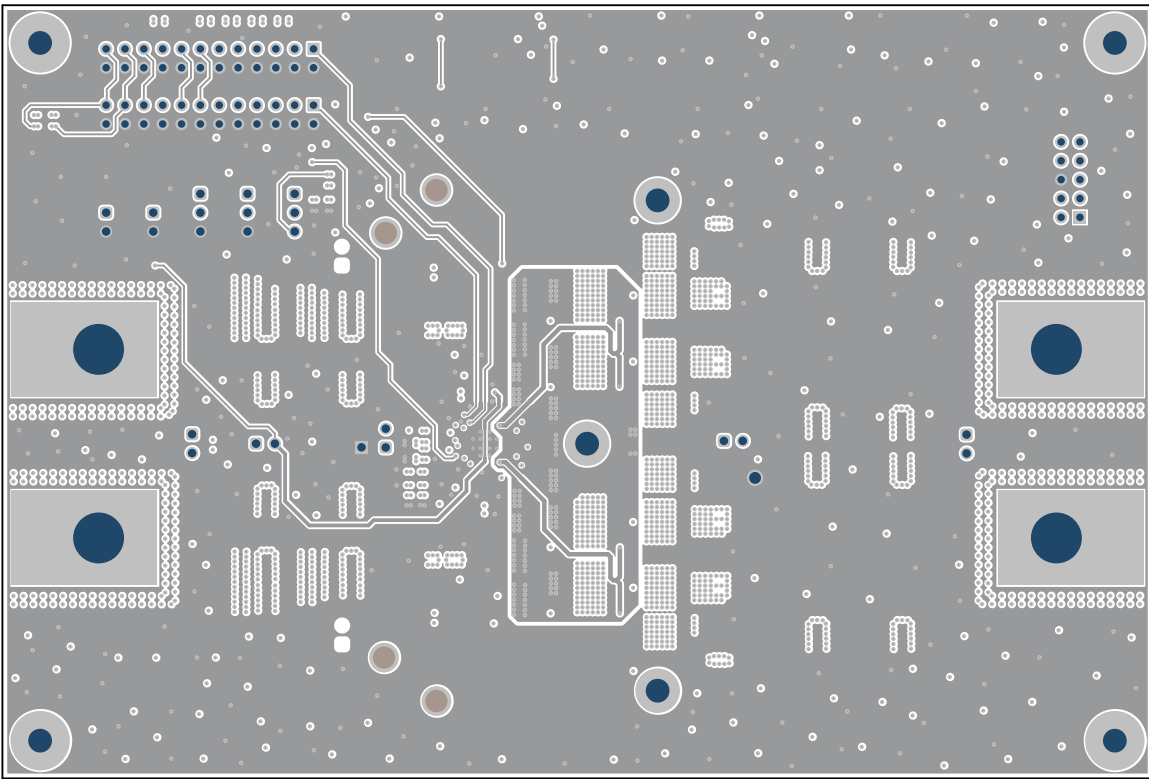


Figure 5-8. Signal Layer 4

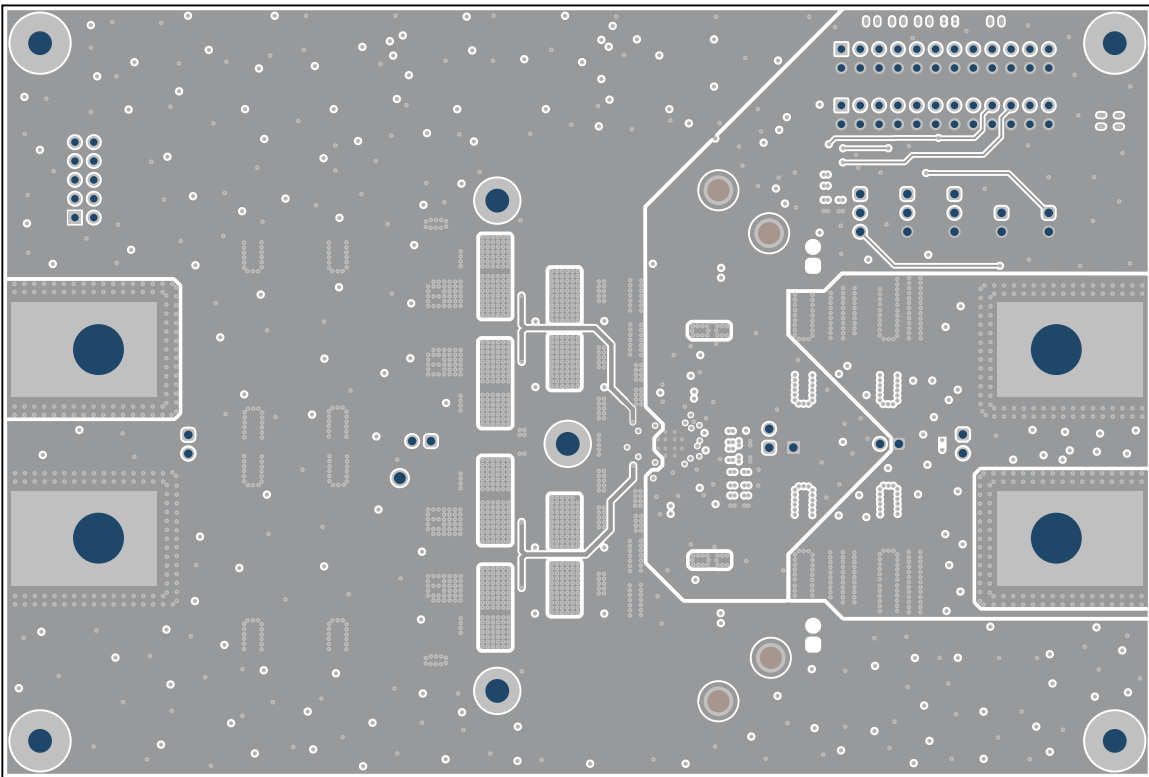


Figure 5-9. Bottom Layer

5.3 Bill of Materials

Table 5-1. Bill of Materials

Designator	Quantity	Description	Part Number	Manufacturer
C1, C3, C13, C14, C15, C29, C30, C41, C42, C43, C44, C45, C51, C52, C53, C54, C55, C69	18	CAP, CERM, 0.1uF, 100 V, ± 10%, X7R, 0603	GRM188R72A104KA35D	MuRata
C2	1	CAP, CERM, 1µF, 50V, ± 10%, X7R, AEC-Q200 Grade 1, 0805	GCM21BR71H105KA03K	MuRata
C4	1	CAP, CERM, 10µF, 10V, ± 10%, X7R, AEC-Q200 Grade 1, 0805	GCJ21BR71A106KE01L	MuRata
C5	1	CAP, CERM, 0.015uF, 50V, ± 10%, X7R, 0603	GRM188R71H153KA01D	MuRata
C6	1	CAP, CERM, 500pF, 50V, ± 5%, C0G/NP0, 0603	CC0603JRNPO9BN501	Yageo America
C7	1	CAP, CERM, 10pF, 50V, ± 5%, C0G/NP0, 0603	GRM1885C1H100JA01D	MuRata
C8	1	CAP, CERM, 0.33uF, 10V, ± 10%, X5R, 0603	C0603C334K8PACTU	Kemet
C16	1	CAP, CERM, 3.3uF, 25V, ± 10%, X6S, 0805	GRM21BC81E335KA73L	MuRata
C17	1	CAP, CERM, 100pF, 50V, ± 5%, C0G/NP0, 0603	GRM1885C1H101JA01D	MuRata
C18, C19	2	CAP, CERM, 0.047uF, 25V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R71E473KA37D	MuRata
C20	1	CAP, CERM, 0.1uF, 100V, ± 10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J2X7R2A104K125AA	TDK
C21, C23, C31, C32, C33, C34, C36, C37, C38, C39	10	10µF ± 10% 100V Ceramic Capacitor X7S 1210 (3225 Metric)	GRM32EC72A106KE05L	MuRata
C25, C27	2	Aluminum Hybrid Polymer Capacitors 220uF 20% 50V Life 4000 Hours AEC-Q200 RADIAL SMT	EEHZU1H221P	Panasonic
C61, C62, C63, C65, C66, C67	6	Aluminum Hybrid Polymer Capacitors 150uF 20% 63V Life 4000Hours AEC-Q200 RADIAL SMT	EEHZU1J151P	Panasonic
D1, D2	2	Diode, Schottky, 100V, 12A, AEC-Q101, TO-277A	V12P10-M3/86A	Vishay-Semiconductor
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 × 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
J1, J2, J3, J4	4	Standard Banana Jack, Uninsulated, 15A	108-0740-001	Cinch Connectivity
J5, J6, J7, J8, JP4, JP5, JP6	7	Header, 2.54mm, 2×1, Gold, TH	61300211121	Würth Elektronik
J9, J10	2	Header, 100mil, 12×2, Gold, TH	TSW-112-07-G-D	Samtec
J13	1	Header (shrouded), 100mil, 5×2, High-Temperature, Gold, TH	N2510-6002-RB	3M
J14	1	Header, 2.54mm, 1×1, Gold, TH	61300111121	Würth Elektronik
JP1, JP2, JP3	3	Header, 2.54mm, 3×1, Gold, TH	61300311121	Würth Elektronik
L1, L2	2	Inductor, Shielded, 3.3µH, 32.2A, 0.00327 ohm, AEC-Q200 Grade 0, SMD	IHLP6767GZER3R3M5A	Vishay-Dale
Q1, Q2, Q3, Q4	4	MOSFET, N-CH, 60V, 71A, SO-8FL	NTMFS5C670NLT1G	ON Semiconductor
R1, R2	2	RES, 0.0015, 5%, 2W, 2512 WIDE	PML100HZPJV1L5	Rohm
R5	1	RES, 20.0 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060320K0FKEA	Vishay-Dale
R6	1	RES, 78.7 k, 0.1%, 0.1W, 0603	RT0603BRD0778K7L	Yageo America

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
R7	1	RES, 47.5 k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW040247K5FKED	Vishay-Dale
R8	1	RES, 6.04k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06036K04FKEA	Vishay-Dale
R9, R94	2	RES, 75.0 k, 1%, 0.125W, AEC-Q200 Grade 0, 0805	CRCW080575K0FKEA	Vishay-Dale
R10	1	RES, 39 k, 5%, 0.125W, AEC-Q200 Grade 0, 0805	CRCW080539K0JNEA	Vishay-Dale
R11, R13	2	0 Ohms Jumper Chip Resistor 0805 (2012 Metric) Metal Element	WSL080500000ZEA9	Vishay
R15, R16, R17, R18, R41, R57, R73	9	RES, 0, 1%, 0.1W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R19	1	RES, 100 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R20, R22, R24	3	RES, 10.0, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060310R0FKEA	Vishay-Dale
R21, R23	2	RES, 2.20, 1%, 0.1W, 0603	ERJ-3RQF2R2V	Panasonic
R42, R58, R74	3	RES, 511, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW0603511RFKEA	Vishay-Dale
R43, R59, R75	3	RES, 1.30 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06031K30FKEA	Vishay-Dale
R44, R60, R76	3	RES, 1.87 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06031K87FKEA	Vishay-Dale
R45, R61, R77	3	RES, 2.74 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06032K74FKEA	Vishay-Dale
R46, R62, R78	3	RES, 3.83 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06033K83FKEA	Vishay-Dale
R47, R63, R79	3	RES, 5.11 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06035K11FKEA	Vishay-Dale
R48, R64, R80	3	RES, 6.49 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06036K49FKEA	Vishay-Dale
R49, R65, R81	3	RES, 8.25 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06038K25FKEA	Vishay-Dale
R50, R66, R82	3	RES, 10.5 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060310K5FKEA	Vishay-Dale
R51, R67, R83	3	RES, 13.3 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060313K3FKEA	Vishay-Dale
R52, R68, R84	3	RES, 16.2 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060316K2FKEA	Vishay-Dale
R53, R69, R85	3	RES, 20.5 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060320K5FKEA	Vishay-Dale
R54, R70, R86	3	RES, 24.9 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060324K9FKEA	Vishay-Dale
R55, R71, R87	3	RES, 30.1 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale
R56, R72, R88	3	RES, 36.5 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060336K5FKEA	Vishay-Dale
R89, R90, R103, R104	4	RES, 4.99 k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06034K99FKEA	Vishay-Dale
R91, R96, R97, R98, R100	5	RES, 0, 5%, 0.125W, AEC-Q200 Grade 0, 0805	CRCW08050000Z0EA	Vishay-Dale
R93	1	RES, 40.2 k, 1%, 0.125W, AEC-Q200 Grade 0, 0805	CRCW080540K2FKEA	Vishay-Dale
R95	1	RES, 0, 5%, 0.1W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
S1, S2, S3, S4, S5, S6	6	Switch, SPST, 8 Pos, 25mA, 24VDC, SMD	218-8LPST	CTS Electrocomponents
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6	6	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
T1, T2, T3, T4	4	Terminal 70A Lug	CXS70-14-C	Panduit
TP1, TP2, TP3, TP4	4	PC Test Point, SMT	RCU-0C	TE Connectivity

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
TP5	1	Test Point, Compact, Black, TH	5006	Keystone Electronics
U1	1	Wide-VIN, 2.2MHz dual-phase boost controller with VOUT tracking	LM5125QRHBRQ1	Texas Instruments

6 Additional Information

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

-
- 4 *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
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 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
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