Application Report
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TMS320C6000 Multichannel Communications System Interface

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ABSTRACT

This document describes a simple interface for development of multichannel telephony systems. Three interfaces are provided:

1. MVIP (Multi-Vendor Integration Protocol): Accomplished with the MT90810, Flexible MVIP Interface Circuit (FMIC).
2. T1/E1 interface: Accomplished with the PEB2254, Framing and Line Interface Component (FALC).
3. Voice Band Analog Input and Output: Accomplished through the TMS320AC3x Voice-Band Audio Processors (VBAP). The primary purpose of the VBAP in a T1/E1 or MVIP environment is to record messages for playback or transmission and to monitor incoming or outgoing voice.

Each of these devices has modes that go beyond the scope of this document. This application report addresses the physical interfaces between the DSP, the FMIC, the FALC, and the VBAP using the serial interface for voice and data and the parallel interface for control and status. The analog interfaces of the VBAP and FALC, as well as the T1/E1 and MVIP protocols and APIs, are not within the scope of this document. Application notes, reports, and component data sheets should be referenced for further details. The reference section of this application report provides a list of some of these documents.

Contents

List of Figures

List of Tables

1 Interface Overview

Figure 1 shows the physical interfaces between the TMS320C6000 DSP, the MT90810 FMIC, and the PEB2254 FALC, and between the MT90810 FMIC and the TCM320AC36 VBAP. The physical interface between the FMIC, FALC, and DSP consists of a serial interface that connects the FMIC to the DSP's McBSP0, and a parallel interface that connects the FMIC and FALC to the DSP's asynchronous EMIF. It is important to note that the FMIC and FALC are 5V devices, so any signals that are provided to the 3.3V I/O DSP must be translated using devices such as the TI SN74CBTD3384 bus switches, and / or SN74LVT16245 transceiver buffers. Signals originating from the DSP do not need to be translated since their V_{OH} and V_{OL} values are compatible with the FMIC and FALC.

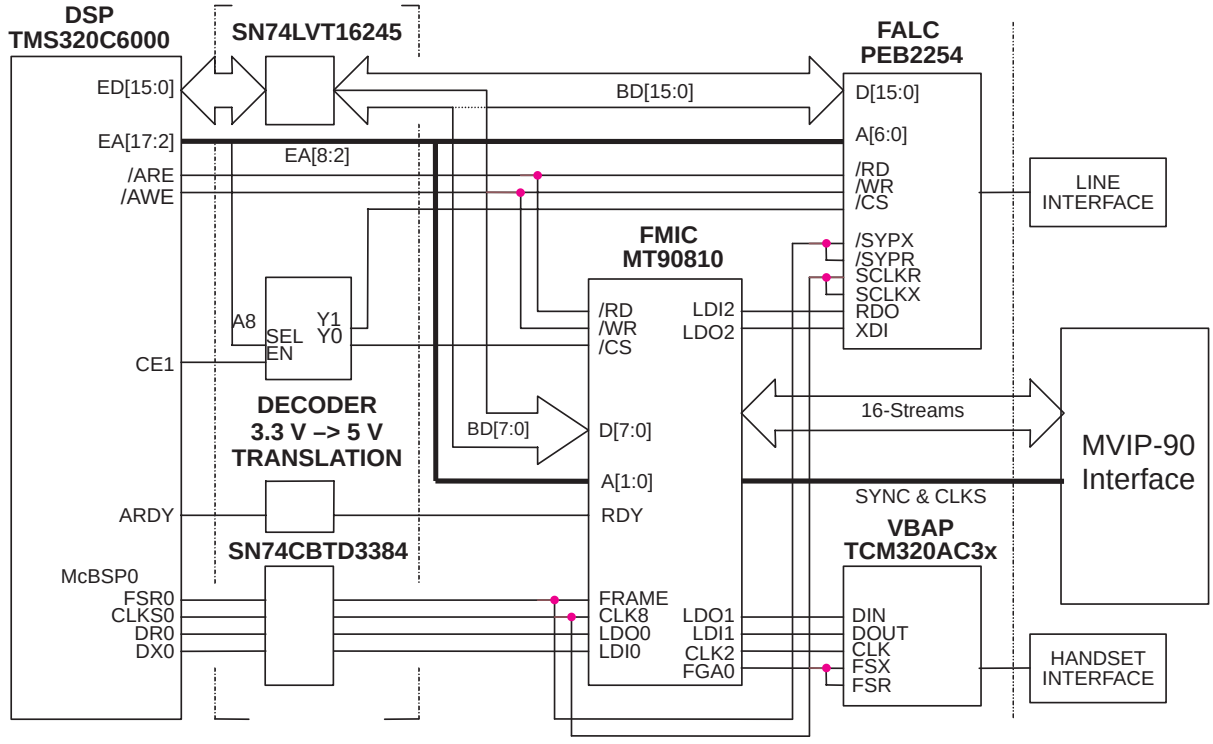

Figure 1. TMS320C6000 Interface to the FMIC, FALC, and VBAP

2 Parallel Interfaces

Both the FALC and FMIC have a parallel interface for control and status that is easily memory-mapped into the DSP's external memory interface (EMIF), sharing all signals except the chip enables. Additionally, the memory-mapped interface enables an external processor to control and monitor the FALC or FMIC through the DSP's host port interface (HPI). Direct access from a host processor may be useful in some applications. The chip selects are derived using a simple address decoder circuit. This circuit may be implemented in a programmable logic device (PLD) or with an SN74LVT138. The EMIF asynchronous control signals are directly connected to the FMIC's and FALC's read/write strobes since the EMIF memory space control register can be programmed with timing characteristics that match the requirements of these devices.

The FALC parallel interface consists of a 16-bit data bus, 7-bit address bus, a chip select, a read strobe, and a write strobe. The EMIF's lower sixteen bits (ED[15:0]) interface to the FALC's data bus using a voltage translation buffer. The DSP's EA[8:2] address signals are mapped directly to the FALC's A[6:0] address signals. The FALC registers are mapped on 32-bit word boundaries with only the lower sixteen data bits being valid.

The FMIC parallel interface consists of an 8-bit data bus, 2-bit address bus, chip select, read strobe, and a write strobe. The EMIF's lower eight bits (ED[7:0]) are connected to the FMIC's data bus using a voltage translation buffer. The DSP's EA[3:2] address signals are mapped directly to the FMIC's A[1:0] address signals. The FMIC registers are mapped on 32-bit word boundaries with only the lower eight data bits being valid.

2.1 Parallel Interface Timing

Since the FALC and FMIC share the parallel interface, the timing must be set to match the worse case of the two. Figure 2 shows the parallel interface timing. Table 1 provides the parametric timing indicated in the timing diagrams.

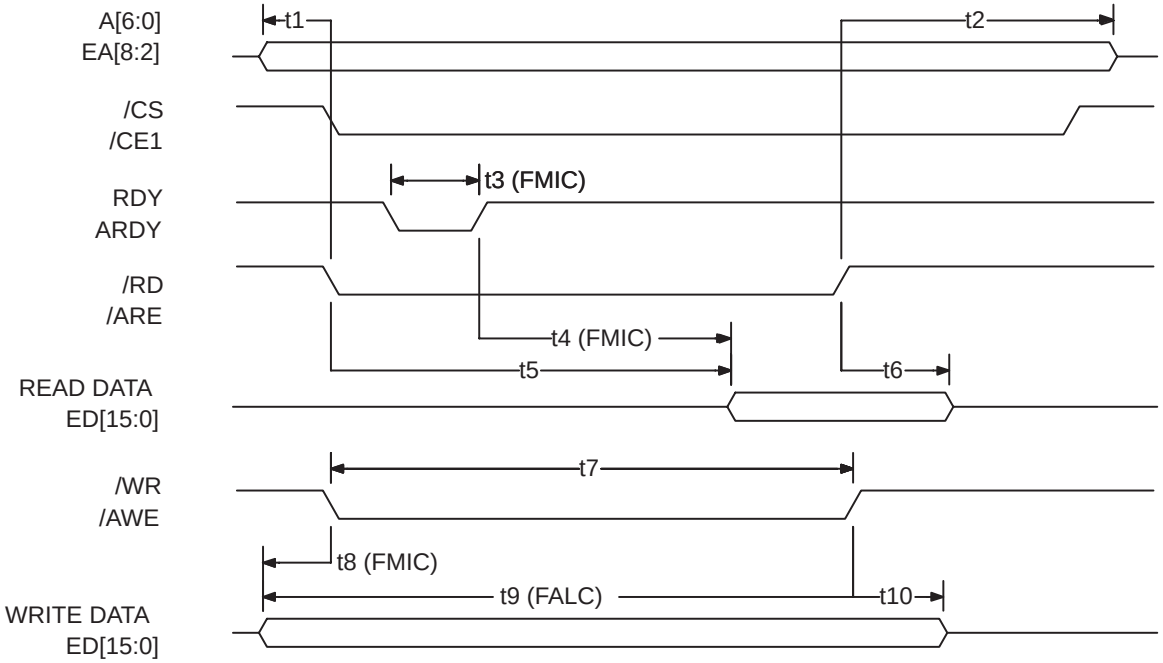

Figure 2. Combined Parallel Interface Timing

2.1.1 Address Setup Requirements

The start of the asynchronous EMIF access to the parallel interface begins with assertion of the chip enable 1 (CE1). The FALC and FMIC require address setup of 15 and 5 ns, respectively, prior to strobe assertion. This is shown as t1 in Figure 2. Since the EMIF CE1 and address signals transition on the same CPU clock edge, the worst-case setup time that has to be met is the15 ns setup time of the FALC. This time period (15ns) plus the delay of the decoder logic (assume to be 7ns) defines the asynchronous setup time that should be programmed in the CE1 memory space control register (minimum 22ns). Assuming a DSP clock of 200 MHz (CPU clock period = 5 ns), the read and write setup fields of the CE1 memory space control register should be set to 5 to give a 25ns address setup time t1, as shown in Table 1.

Table 1. Parallel Interface Parametric Timing

Parameter	Symbol	FMIC (ns)	FALC (ns)	FMIC + FALC (ns)	200 MHz DSP programmed to…
Address setup to WR or RD strobe (FMIC/FALC requirement)	t1	Min 5	Min 15	Min 22†	25 ns (Setup = 5)
Address hold from WR or RD strobe (FMIC/FALC requirement)	t2	Min 5	Min 0	Min 12†	20 ns (Hold = 4)
RDY inactive from WR or RD (FMIC delay)	t3	Max 25	–	–	
Data valid after RDY (FMIC delay)	t4	Max 25	–	–	
Read strobe to data valid (FMIC/FALC delay)	t5	Max 75	Max 95	Max 95	105 ns (Read Strobe = 21)
Data hold from RD rising (FMIC/FALC output data hold)	t6	Min 20	Min 10	Min 10	
WR or RD strobe width (FMIC/FALC requirement)	t7	Min 50	Min 100	Min 100	100 ns (Write Strobe = 20)
Data setup to WR asserted (FMIC requirement)	t8	Min 5	–	Min 5	
Data setup to WR de-asserted (FALC requirement)	t9	–	Min 30	Min 30	
Data hold from WR strobe (FMIC/FALC requirement)	t10	Min 5	Min 10	Min 17†	20 ns (Hold = 4)

† 7ns decoder delay added

2.1.2 Write Data Strobe Requirements

The FALC and FMIC require a minimum data strobe period (t7) of 100 ns and 50 ns, respectively. Thus, the write strobe fields of the control register should be set to 20 (100 ns) which covers both the FALC and FMIC minimums. This setting allows sufficient margin for the FMIC's RDY signal to control the strobe width on stalled accesses to the FMIC. During a write access, the FALC requires data setup at least 30 ns prior to strobe de-assertion (t9). Since the EMIF provides valid data at the beginning of the memory cycle for writes (at the beginning of the Address Setup), this requirement is easily met by the minimum setup time given the 20-cycle (100ns) strobe width. The FMIC, on the other hand, requires data setup at least 5ns before write strobe assertion (t8). This requirement is met by the 25 ns setup time described in the Address Setup section above.

2.1.3 Read Data Strobe Requirements

The FALC strobe to data valid time is 95 ns maximum (t5). The FMIC strobe to data valid time is 75 ns maximum (tACC + tDAC = 50 + 25 = 75ns in the FMIC data sheet), given the microprocessor is ready (RDY high). For additional margin and to meet the DSP's setup time, a read strobe width of 21 cycles (105 ns) is set, even though the FALC and FMIC only require a minimum combined data strobe period (t7) of 100ns.

2.1.4 DSP Read Hold Requirements

For EMIF reads, the FMIC and FALC data hold times (t6) are 20 ns and 10 ns minimum, respectively, after the rising edge of the read strobe. Since the rising edge of the read strobe happens after the clock edge that the DSP samples the data, and the DSP's hold time requirement is much smaller than the FALC's 10 ns minimum, this is not a problem.

2.1.5 Data and Control Signals Hold Requirements

The FMIC requires a data (t10) and address (t2) hold time of 5 ns, respectively. The FALC requires a data hold time of 10 ns (t10), but no address hold time (t2). The FALC and FMIC do not require chip selects to be held past the rising edge of the read or write data strobe. Therefore the longest hold requirement is the FALC's 10 ns data hold time (t10) plus the decoder delay of 7 ns (17 ns total). At 200 MHz, this means that the write hold field of the CE1 memory space control register should be set to 4 (20 ns) to meet the 17 ns requirement. The read hold field can be set to 3 (15 ns) to meet the 12 ns (t2 + decoder delay) requirement. For extra margin, the read hold field can also be set to 4 (20 ns), just as the write hold field.

2.1.6 Other Requirements

One significant timing parameter is not shown in the timing diagrams, i.e. the FALC requires at least 80 ns between the rising edge of a read, and 50 ns for a write strobe and the next falling edge of a read or write strobe. This means that FALC accesses need to be controlled, either by hardware or software, if the application would ever attempt to perform sequential register accesses. A hardware approach can be as simple as increasing the setup and strobe periods in the EMIF memory space.

3 Serial Interfaces

The FMIC's local serial streams interface directly to the C6000's McBSP (Multichannel buffered serial port), providing a convenient interface for T1/E1 serial data and the VBAP. This design uses just one of the DSP's two McBSP ports, leaving the second available for other interfaces, although the VBAP or FALC could alternatively interface directly to another McBSP.

Although the FMIC and FALC allow a variety of timing and clock source configurations, this application report assumes that the FMIC always sources the serial data clock and frame sync signals. After voltage translation, the serial data clock is connected to the DSP's McBSP0 CLKS. Similarly, the FMIC frame sync signal is connected to the FSR0, which is also programmed as an input. This configuration means that both transmit and receive data are synchronized with phase alignment. The FALC shares these FMIC frame and clock signals, with the frame being connected to both /SYPR and /SYPX, and the CLK8 being connected to SCLKR and SCLKX. The VBAP has a slightly different timing requirement, therefore it will have its frame connected to one of the FMIC's programmable frame circuits, and its clock connected to CLK2.

3.1 VBAP Serial Timing

To be compatible with the T1/E1 requirements, the VBAP is used in companding mode. Linear mode can also be selected instead for certain applications. The VBAP is available in μ-Law, TCM320AC36, for T1 applications; and A-Law, TCM320AC37, for E1. On a combined T1/E1application, the devices may be switched with a relay.

VBAP's serial timing is directly compatible with the FMIC using the FMIC's programmable Frame Group. This feature allows the Frame to be offset to allow for proper alignment of the clock and data. The VBAP can operate in two timing modes: Fixed and Variable. Since the VBAP is connected to a dedicated local stream on the FMIC, either mode could be used by appropriately programming the FMIC. In the Fixed Data mode, the VBAP provides a TSX signal that may be used to gate the output of the VBAP when sharing a PCM stream with another device. In the Fixed Data mode, the VBAP uses the master clock (CLK) and frame synchronization clocks (FSX) and (FSR). With the FMIC's programmable frame, the VBAP's clock and data requirements are directly compatible with the FMIC, since they both receive on the falling edge and transmit on the rising edge of clock. The only adjustment required is the alignment of frame sync. Figure 3 shows these timing relationships.

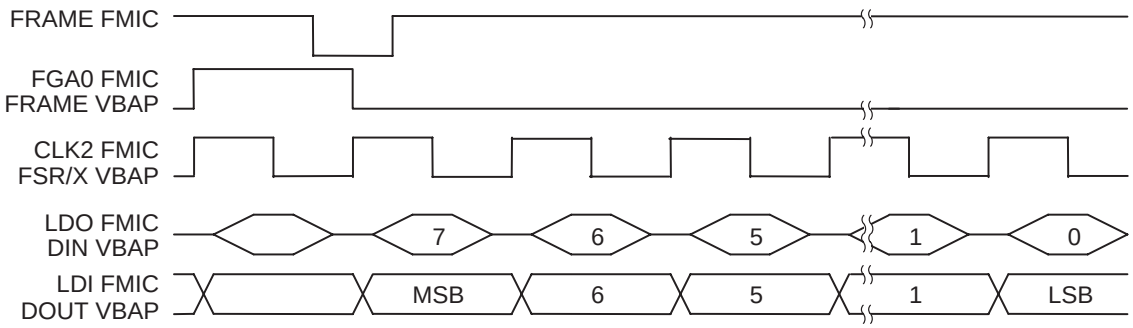

Figure 3. VBAP and FMIC 2-MHz Mode Serial Timing

3.2 FMIC Frame Group Registers

The VBAP contains no programmable features in companding mode. The FMIC provides two groups of independently programmable output framing signals:

1. FGA[0:11] group A output signals are programmed by the frame start register A (FRMA_STRT) and frame mode register A (FRMA_MODE).
2. FGB[0:11] group B output signals are programmed by the frame start register B (FRMB_STRT) and frame mode register B (FRMB_MODE).

The VBAP in this application is connected to FGA[0]. The FRMA_STRT register is at FMIC Control Register indirect address 4, and the FRMA_MODE register is at FMIC Control Register indirect address 5. The upper 2 bits of the FRMA_MODE register determine the mode of the FGA pins. Modes 2 and 3 are used for programming these pins as Frame signals. For a description of other available modes, refer to the MT90810 Data Sheet (number 5) in section 4, References. For these modes, bit 5 selects the Frame Type, (1-bit or 8-bit length); bit 4:3 select the bit rate and bits 2:0 are the upper three bits of the 11-bit quantity that determines the start position of the FGA[0] relative to Frame in 8-MHz clock edge boundaries. An offset of ‘0’ represents the rising edge of clock after the beginning of FRAME FMIC. The FRMA_STRT register then contains the lower 8 bits of the 11-bit quantity. For proper alignment of the VBAP frame signal, its frame needs to begin one 2-MHz clock before the normal start. This can be achieved by programming a 7F9 hex (2041 in decimal) for the 11-bit quantity in the FRMA register. The FRMA registers is programmed with a 2 in the MODE bits, a 0 in the FRM_TYPE bit, a 0 in the BIT_RATE bits, and a 7F9 hex for the 11-bit quantity. Furthermore the FRMA_MODE register is programmed with 87 hex, and the FRMA_STRT register is programmed with a F9 hex. Refer to the MT90810 Data Sheet, (number 5) in section 4, References for additional information.

3.3 DSP Serial Timing and McBSP Registers

The FALC and DSP McBSP serial ports are directly compatible with the FMIC 2-MHz serial timing when properly programmed, and therefore can share frame and clock signals from the FMIC. Note that the FMIC, FALC and DSP are also capable of operating at 4- and 8-MHz data rates. However, in 8-MHz mode, the FMIC only has one local stream. These data rates may be useful in certain applications.

The FALC requires a working clock of 8.192 MHz for all data rates, thus the FMIC’s CLK8 is used for the clock source. The DSP’s McBSP can be programmed to divide down CLK8 for a 2-MHz data rate. Figure 4 shows the timing relationships of the FMIC and DSP with an 8-MHz clock, after proper programming of the DSP McBSP registers.

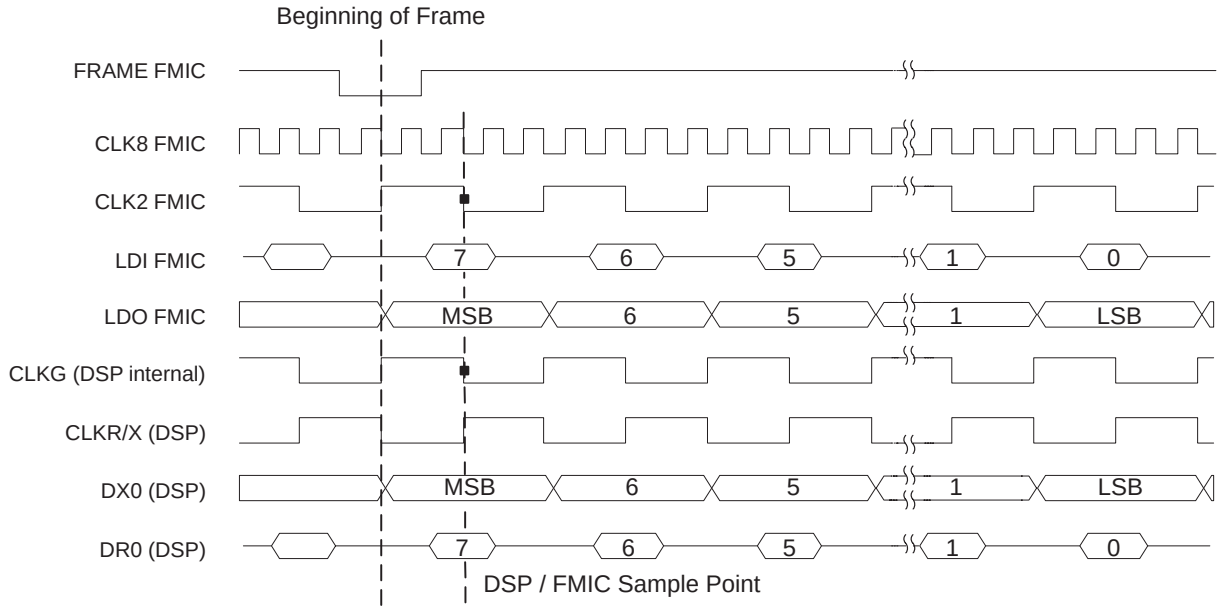

Figure 4. DSP and FMIC 2-MHz Mode Serial Timing, With 8-MHz Clock

McBSP configuration registers need to be programmed to accommodate the FMIC 2-MHz data. The McBSP takes the FMIC CLK8 signal at the CLKS pin as a clock source to the internal sample rate generator, which then divides the FMIC CLK8 input by 4 to generate a 2-MHz internal clock CLKG. CLKG is synchronized to the FSR input from the FMIC.

The McBSP parameters need to be configured appropriately for the McBSP/FMIC interface. Figure 5 and Figure 6 show the setup for the McBSP registers. The values in the shaded bit-fields are “don’t cares.”

3.3.1 Serial Port Control Register (SPCR)

- /FRST=/GRST=/RRST=/XRST=1. The internal frame sync generator, internal sample rate generator, receiver, and transmitter are enabled. Refer to application report *TMS320C6000 McBSP Initialization* (SPRA488), and the *TMS320C6000 Peripherals Reference Guide* (SPRU190C), Section 11.5.1.2, for details on the McBSP initialization procedure.
- The interrupt modes can be selected as needed by the application.

3.3.2 Pin Control Register (PCR)

- FSXM = 1. Transmit frame synchronization signal is generated internally by the sample rate generator. For the McBSP/FMIC interface, the FSX output is not used.
- FSRM = 1. Together with GSYNC = 1 in the Sample Rate Generator Register, receive frame synchronization signal FSR is an input from the FMIC to the McBSP. An active transition on the FSR pin marks the beginning of a new frame and synchronizes the internal sample rate generator clock CLKG to FSR.
- CLKXM = CLKRM = 1. CLKX and CLKR are generated internally by the sample rate generator. For the McBSP/FMIC interface, the CLKX and CLKR outputs are not used.

- FSXP = FSRP = 1. Transmit and receive frame synchronization polarity is active low, in consistent with the active low FRAME signal from the FMIC.
- CLKXP = CLKRP = don't care. Since the CLKX and CLKR signals are not used in the McBSP/FMIC interface, they are don't care values. Internally, data is always transmitted on the rising edge of CLKG and sampled on the falling edge of CLKG. If desired, CLKXP and CLKRP can be set to '1' to invert the CLKG signal on the external CLKX and CLKR pins.

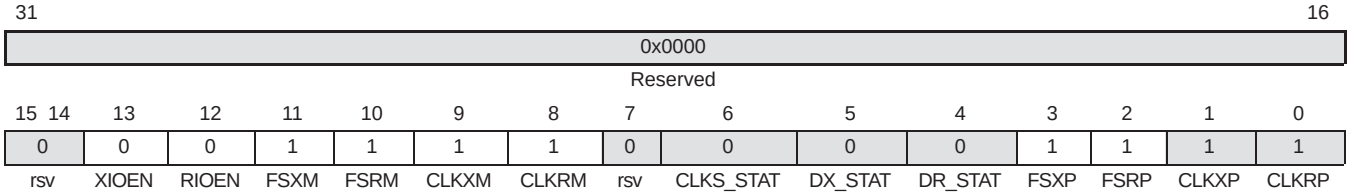

Figure 5. Pin Control Register (PCR)

3.3.3 Sample Rate Generator Register (SRGR)

- GSYNC = 1. Together with FSRM=1 in the PCR, internal sample rate clock CLKG is resynchronized to the input FSR signal.
- CLKSP = 1. The falling edge of CLKS (CLK8 FMIC) generates internal clock CLKG and internal frame sync FSG.
- CLKSM = 0. The sample rate generator clock is derived from CLKS (CLK8 FMIC).
- FSGM = 1. The transmit frame sync signal is driven by the sample rate generator frame sync signal FSG.
- FPER = don't care. Since GSYNC=1, the frame period is dictated by the external frame sync pulse at FSR.
- FWID = 0. Width of the internal frame sync pulse is 1 CLKG period.
- CLKGDV = 3. The sample rate generator clock frequency is CLKS (8 MHz) divided by 4 to give a 2-MHz data rate.

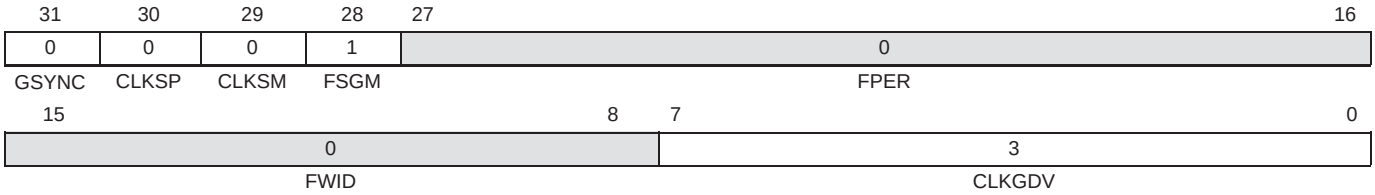

Figure 6. Sample Rate Generator Register (SRGR)

The remaining McBSP register settings will vary with application.

3.4 FALC Serial Timing and FALC Registers

The PEB2254 FALC is also a very flexible device and must be programmed to be compatible with the FMIC 2 MHz data rate and 8-MHz clock. Figure 7 shows the FALC to MVIP Serial Timing.

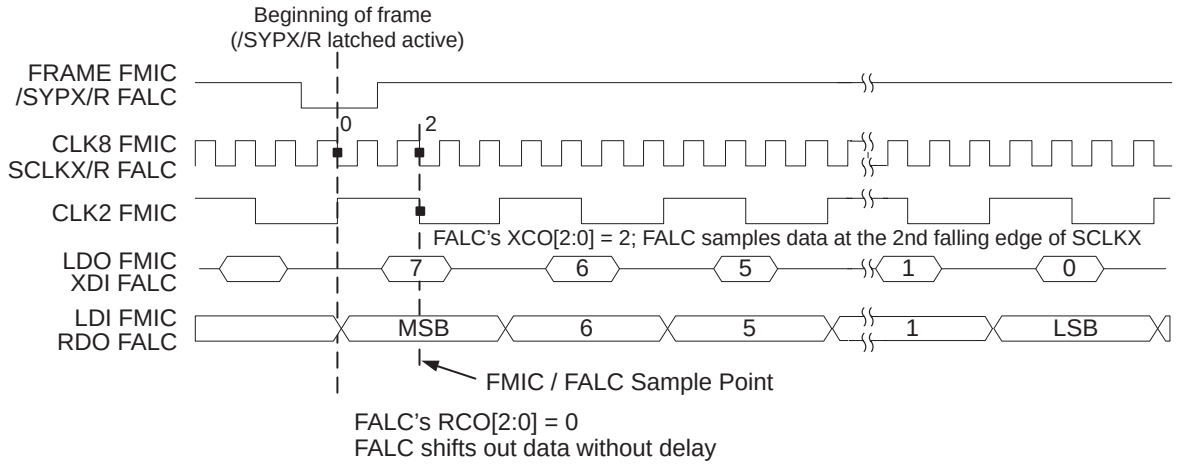

Figure 7. FALC and FMIC 2-MHz Mode Serial Timing, With 8-MHz Clock

The FALC allows selection between T1 or E1 with a single MODE bit (PMOD) in the FRAMER MODE REGISTER 1 (FRMR1) at byte offset 1B. Set this bit to a '1' for T1 (PCM 24) or '0' for E1 (PCM 30). Additionally, the FALC's local data rate must be set, with the IMOD bit in the same register. Set this bit to '1' for 2-MHz operation.

In this application, the FALC has two interfaces: external line interface, and the local system highway interface to the DSP and the FMIC. This application report only discusses the latter interface. For the FALC, the term "transmit" refers to the transmission of data from the FALC to the external line interface. Before transmitting this data to the external line interface, the FALC *receives* this transmit data from the FMIC through the Transmit Data In (XDI) pin on the local system internal highway. This incoming local interface data is sampled by the FALC at the second falling edge of SCLKX (time 2) after /SYPX is latched active (time 0), as shown in Figure 7. To achieve this, the Transmit Offset needs to be programmed to '010' in the XCO0 – XCO2 bits of the Transmit Control 0 Register (TC0) at byte offset 20 hex.

Similarly, the term "receive" refers to the reception of data from the external line interface to the FALC. The FALC then *transmits* this receive data to the FMIC via the Receive Data Out (RDO) pin. The FALC starts shifting out data from the RDO pin as soon as the /SYPR is latched active at time 0, as shown in Figure 7. Therefore the RCO0 – RCO2 bits of the Receive Control 0 (RC0) register at byte offset 21 are set to '000'.

4 References

1. *TMS320C6201 Fixed-Point Digital Signal Processor* Data Sheet, SPRS051, Texas Instruments Incorporated.
2. *TMS320C6000 Peripherals Reference Guide*, SPRU190, Texas Instruments Incorporated.
3. *TMS320C6x Multichannel Evaluation Module Reference Guide*, SPRU308, Texas Instruments Incorporated.
4. *MT90810, Flexible MVIP Interface Circuit* Data Sheet, Issue 3 - March 1997, Mitel Semiconductor.
5. *An Introduction to MVIP* ™ and *Details on Implementation using the MT90810* Application Note MSAN-148, Issue 1 - September 1994, Mitel Semiconductor.
6. PEB2254, *Framing and Line Interface Component for PCM 30 and PCM 24* Data Sheet, T2254-XV13-D1-7600, Nov 1996, Siemens Semiconductor Group.
7. *Designing a Generic E1/T1 Platform*, T2254-XVXX-A1-7600, June 1997, Siemens Semiconductor Group.
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10. *Designing with the Voice-Band Audio Processor* Application Report, SLWA001, Texas Instruments Incorporated.

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