Application Report
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USB Compliance Checklist

Jim Chen

ABSTRACT

This application report contains the USB checklist. This checklist supports a compliant full-speed USB device port, but does not support a low-speed USB device operation.

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1 Introduction

The USB Compliance Checklist Peripheral Silicon (excluding Hub Silicon) for the 2.0 USB Specification Checklist, Version 1.08, December 18, 2001 is written by the USB Organization. The purpose of the checklist is to help designers of USB peripherals to assess their product's compliance with the Universal Serial Bus Specification, Revision 2.0, and is necessary to qualify a USB interface silicon for the USB-IF Integrators List. For more information regarding the USB Specification Checklist, the Universal Serial Bus Specification, and qualifying a USB product for the USB-IF Integrators List, see the USB Organization's website at http://www.usb.org.

2 Signals and Timing

Table 1 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 1. Signals and Timing

ID	Question	Response	Sections in Spec.
ST1	Is the data line crossover voltage between 1.3 V and 2.0 V?	Yes	7.1.2
ST2	Do all single ended receivers recognize 0.8 V or below as a logic low?	Yes	7.1.4
ST3	Do all single-ended receivers recognize 2.0V or more as a logic high?	Yes	7.1.4
ST4	Do all differential receivers have an input sensitivity of at least 200 mV between 0.8 V and 2.5 V common mode?	Yes	7.1.4
ST5	Is the device's pull up active only when V_{BUS} is 1.17 V or more?	Yes	7.1.5
ST6	Is the input impedance of D+ and D- without termination and the pull up resistors more than 300 kΩ?	Yes	7.1.6
ST7	Does the device respond to a reset no sooner than 2.5 μs and no later than 10 ms after the SE0 begins, regardless of the SE0's position in a bitstream?	Yes	7.1.7.3
ST8	Is the device's reset recovery time less than 10 ms?	Yes	7.1.7.3
ST9	At the end of reset, is the device in the default state?	Yes	7.1.7.3 9.1.1
ST10	Does the device enter suspend if the bus is idle for 3 ms or more?	Yes	7.1.7.4
ST11	Has the device's power consumption dropped to its suspended value after the hub's upstream bus segment has been idle for 10 ms?	Yes	7.1.7.4
ST12	When suspended, does the device recognize any non-idle state on its upstream port, including a reset as a resume signal?	Yes	7.1.7.5
ST13	Does the device recognize the end of resume signaling and return to the state it was in prior to suspend?	Yes	7.1.7.5
ST14	Is the device able to accept a SetAddress() request 10 ms after resume is signaled?	Yes	7.1.7.5
ST15	Does the device complete its wakeup within 20 ms?	Yes	7.1.7.5
ST16	Do active data line outputs drive to 2.8 V – 3.6 V with a 14.25kΩ load to ground?	Yes	7.3.2
ST17	Do active data line outputs drive to 0–0.3V with a 1.425kΩ load to 3.6 V?	Yes	7.3.2

2.1 Low-Speed Ports

The USB device port does not support low-speed operation.

Table 2 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 2. Low-Speed Ports

ID	Question	Response	Sections in Spec
LS1	Are data line rise times between 75 ns and 300 ns when driving into any single ended, capacitive load between 200 pF and 450 pF?	N/A	7.1.2
LS2	Are data line fall times between 75 ns and 300 ns when driving into any single ended, capacitive load between 200 pF and 450 pF?	N/A	7.1.2
LS3	Are the rise and fall times matched to within 20% for J → K transitions?	N/A	7.1.2
LS4	Are the rise and fall times matched to within 20% for K → J transitions?	N/A	7.1.2
LS5	Is a SE0 less than 210 ns long ignored at all transitions in a bitstream?	N/A	7.1.4
LS6	Is a SE1 less than 100 ns long ignored at all transitions in a bitstream?	N/A	
LS7	Does the device drive the J state at the end of an end of period (EOP) for a full low-speed bit time?	N/A	7.1.7
LS8	Is the transmission data rate between 1.4775 Mb/s and 1.5225 Mb/s?	N/A	7.1.11
LS9	Is the differential driver jitter for consecutive transitions less than ± 25 ns?	N/A	7.1.13.1
LS10	Is the differential driver jitter for paired transitions less than ± 10 ns?	N/A	7.1.13.1
LS11	Is the EOP width between 1.25 μs and 1.5 μs at the transmitter?	N/A	7.1.13.2
LS12	Does the receiver accept an SE0 between 670 ns and 1.76 ms long, followed by a J, as an EOP?	N/A	7.1.13.2
LS13	Does the receiver accept a packet whose first bit has been distorted by as much as ± 25ns?	N/A	7.1.14
LS14	Does the receiver accept a packet whose last bit has been lengthened by as much as 260 ns (dribble bit)?	N/A	7.1.14 7.1.9
LS15	Is the receiver data jitter tolerance at least ± 141 ns for consecutive transitions?	N/A	7.1.15
LS16	Is the receiver jitter tolerance for paired transitions at least ± 184 ns?	N/A	7.1.15
LS17	Is the device's turn-around time between two and 6.5 low-speed bit times, or 7.5 bit times if the device has a fixed cable?	N/A	7.1.18
LS18	Is the time-out period 16–18 low-speed bit times?	N/A	7.1.19
LS19	Is D- between 2.7 V and 3.6 V and D+ between 0.0 V and 0.3 V when the bus is idle?	N/A	7.2.3

2.2 Full-Speed Ports

Table 3 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 3. Full-Speed Ports

ID	Question	Response	Sections in Spec
FS1	With series termination resistors, does the device's source impedance remain in the shaded areas of Figure 7-3 in the USB Specification, Revision 2.0?	Yes	7.1.1.1
FS2	Are data line rise times between 4.0 ns and 20 ns when driving into a singleended 50 pF load?	Yes	7.1.2
FS3	Are data line fall times between 4.0 ns and 20 ns when driving into a singleended 50 pF load?	Yes	7.1.2
FS4	Are the rise and fall times matched to within 10% for J → K transitions?	Yes	7.1.2
FS5	Are the rise and fall times matched to within 10% for K → J transitions?	Yes	7.1.2
FS6	Is a SE0 less than 14 ns long ignored at all transitions in a bitstream?	Yes	7.1.4
FS7	Is a SE1 less than 8 ns long ignored at all transitions in a bitstream?	Yes	
FS8	Does the device drive the J state at the end of an EOP for complete full speed bit time?	Yes	7.1.7
FS9	If the device tracks the K → low-speed EOP J transition on its upstream port at the end of resume, does it correctly handle the low-speed EOP?	Yes	7.1.7.5
FS10	Is the transmission data rate between 11.97 Mb/s and 12.03 Mb/s?	Yes	7.1.11
FS11	Is the differential driver jitter for consecutive transitions less than ± 2.0 ns?	Yes	7.1.13.1
FS12	Is the differential driver jitter for paired transitions less than ± 1.0 ns?	Yes	7.1.13.1
FS13	Is the EOP width between 160 ns and 175 ns at the transmitter?	Yes	7.1.13.2
FS14	Does the device accept an SE0 between 82 ns and 250 ns long, followed by a J, as an EOP?	Yes	7.1.13.2 7.1.14
FS15	Does the receiver accept a packet whose first bit has been distorted by as much as ± 25 ns?	Yes	7.1.14
FS16	Does the receiver accept a packet whose last bit has been lengthened by as much as 75 ns?	Yes	7.1.14 7.1.9
FS17	Is the receiver data jitter tolerance at least ± 20.0 ns for consecutive transitions?	Yes	7.1.15
FS18	Is the receiver jitter tolerance for paired transitions at least ± 12.0 ns?	Yes	7.1.15
FS19	Is the device's turn-around time between two and 6.5 full-speed bit times, or 7.5 bit times if the device has a fixed cable?	Yes	7.1.18
FS20	Is the time-out period 18 full-speed bit times?	Yes	7.1.19
FS21	Is D+ between 2.7 V and 3.6 V and D- between 0.0 V and 0.3 V when the bus is idle?	Yes	7.2.3

3 Signaling Protocol and Error Handling

3.1 Bitstreams

Table 4 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 4. Bitstreams

ID	Question	Response	Sections in Spec
B1	Is the possibility of both D+ and D- registering as NIB 1 during bus transitions accounted for?	Yes	7.1.2 7.1.13.1
B2	Is the USB signaling either full-speed or low-speed, but not both?	Yes	7.1.5
B3	Does the sense of USB signaling correspond to the signaling speed?	Yes	7.1.7
B4	Is the bitstream on the bus nonreturn to zero inverted (NRZI) encoded?	Yes	7.1.8
B5	Is bit stuffing performed on all data transmitted, including CRCs, prior to NRZI encoding?	Yes	7.1.9 8.3.5
B6	Is bit stuffing performed even if the stuffed bit follows the last bit of a packet?	Yes	7.1.9
B7	Is NRZI to nonreturn to zero (NRZ) decoding done before bit unstuffing?	Yes	7.1.9
B8	Is bit unstuffing performed on all received data, including CRCs?	Yes	7.1.9 8.3.5
B9	Is bit unstuffing done before the bitstream is parsed?	Yes	7.1.9

3.2 Fields

Table 5 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 5. Fields

ID	Question	Response	Sections in Spec
F1	Is the SYNC field, as measured on the bus wires, correct (NIB KJKJKJKK)?	Yes	8.2
F2	Are all PIDs used among those listed in Table 8-1?	Yes	8.3.1
F3	Are the PID check bits the ones complement of the packet type field?	Yes	8.3.1
F4	Are the CRC generator's contents inverted and sent to the checker MSb first?	Yes	8.3.5
F5	Is the token CRCs generated with the polynomial NZB 00101 on the ADDR and ENDP fields of the IN, SETUP, and OUT tokens?	Yes	8.3.5.1
F6	If all bits are received without error, does the CRC computation on a token or state of finish (SOF) leave a residual of NZB 01100 at the EOP?	Yes	8.3.5.1
F7	Is the data CRC generated with the polynomial NZB 1000000000000101 on the data field of a data packet?	Yes	8.3.5.2
F8	If all bits are received without error, does the CRC computation on the data field leave a residual of NZB 1000000000001101 at the EOP?	Yes	8.3.5.2

3.3 Packets

Table 6 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 6. Packets

ID	Question	Response	Sections in Spec
P1	Are all token packets 32 bits long and followed by an EOP?	Yes	8.4.1
P2	Are all token packets of the form SYNC PID address endpoint token CRC EOP?	Yes	8.4.1
P3	Are all data packets an integral number of bytes long (4 to 1027) excluding the EOP?	Yes	8.4.3
P4	Is the data packet constituted as sync followed by PID followed by 0 to 1023 bytes of data followed by data CRC followed by EOP	Yes	8.4.3
P5	Are all handshake packets 16 bits + EOP?	Yes	8.4.4
P6	Are all handshake packets of the form SYNC PID EOP?	Yes	8.4.4
P7	Is the data payload of a low-speed packet limited to a maximum of 8 bytes?	N/A (Low-Speed Only)	8.6.5
P8	Is the PRE packet 16 bits long?	N/A (Low-Speed Only)	8.6.5
P9	Does the PRE packet consist of only a SYNC followed by a PID?	N/A (Low-Speed Only)	8.6.5

3.4 Transactions

Table 7 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 7. Transactions

ID	Question	Response	Sections in Spec
TA1	Does an isochronous endpoint synthesize frame markers to replace SOFs which may be lost due to bus error?	Yes	5.10.6
TA2	Do handshakes conform to order of precedence described in section 8.4.5?	Yes	8.4.5
TA3	Does the generated packet comply with the flows show in Figure 8-9, 8-11, 8-13, or 8-14 in the USB Specification, Revision 2.0, as appropriate?	Yes	8.5 8.6.5
TA4	Do interrupt endpoints used in rate feedback mode toggle the sequence bit without regard to presence or type of handshake?	Yes	8.5.3
TA5	Is an unsuccessful (NAKed or timed-out in non-token phase) transaction retried?	Yes	8.6
TA6	Does the retried transaction use the same data PID as the original transaction?	Yes	8.6

3.5 Transfers

Table 8 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 8. Transfers

ID	Question	Response	Sections in Spec
TF1	Does the data stage always start with a data1 PID?	Yes	8.5.2
TF2	Are all the transactions of the data stage in the same direction?	Yes	8.5.2
TF3	Is there status stage's direction opposite that of the data stage?	Yes	8.5.2
TF4	Is the data packet used in the status stage zero bytes in length?	Yes	8.5.2

4 Recommended Questions/Device Robustness

4.1 Bistreams

Table 9. Bistreams

ID	Question	Response	Sections in Spec
RB1	Is a single ended NIB 1 more than one bit time long ignored?	Yes	—
RB2	Does an agent ignore a truncated (up to 90%) first bit of the sync field without impacting the rest of the bitstream?	Yes	—
RB3	Is the state of the differential receiver ignored during single ended signaling?	Yes	—
RB4	Does the target reject bitstreams less than one bit time long without impacting future transactions?	Yes	—
RB5	Does the target adjust to the difference in frequency and phase between incoming clock and its internal clock?	Yes	—
RB6	Is a packet with a bit-stuff error rejected by the target?	Yes	—
RB7	Is a bitstream, which is not part of a packet, with bit stuff error ignored by the target?	Yes	—
RB8	Does the target reject packets with bit stuff error at the last bit of the packet?	Yes	—

4.2 Fields

Table 10. Fields

ID	Question	Response	Sections in Spec
RF1	Is the sync field recognized as valid even if the first two bits of it are corrupted? (Only the last 3 bits actually need to be decoded.)	Yes	—
RF1	Is a packet with packet type not listed in Table 8-1 ignored by the target	Yes	—
RF2	Is a packet with a corrupt PID (PID check error) ignored by the target?	Yes	—
RF3	Is a token with a bad CRC ignored by the target?	Yes	—
RF4	Is a CRC error on a data packet recognized by the target?	Yes	—

4.3 Packets

Table 11 references sections from the Universal Serial Bus Specification, Revision 2.0, which is available at http://www.usb.org/developers/docs/.

Table 11. Packets

ID	Question	Response	Sections in Spec
RP1	Does the device ignore a token, whose address field does not match any address in the device?	Yes	—
RP2	Does the device ignore a token, whose endpoint field does not match any endpoint in the address?	Yes	—
RP3	Does the device ignore a token, which does not match the direction of its target endpoint?	Yes	—
RP4	Is a SETUP token to a unidirectional endpoint ignored by the device?	Yes	—
RP5	Is every endpoint capable of handling zero length data packets in its assigned directions?	Yes	—
RP6	Does an ISO endpoint use a zero length data packet if fresh frame data is not available?	Yes	—
RP7	Does the target, whose length does not match the standard length for the packet type, reject a packet?	Yes	—
RP8	Does the measurement of packet length take into account the possibility of jitter and hub repeater skews in the EOP?	Yes	—
RP9	Does the target reject a bitstream that does not constitute a valid packet?	Yes	—
RP10	Are low-speed packets received by full-speed upstream ports ignored?	Yes	8.6.5

4.4 Transactions

Table 12. Transactions

ID	Question	Response	Sections in Spec
RTA1	Do all pipes in the device return to normal operation when the device resumes from suspend?	Yes	—
RTA2	Is a packet which doesn't fit the current phase of a transaction rejected by the target?	Yes	—
RTA3	Does the receipt of a token always start a new transaction and end a pending transaction?	Yes	—
RTA4	Is a data packet with same PID as the previous data packet to an endpoint ignored, other than ACKing the data packet?	Yes	—
RTA5	Does a time-out or error in any phase cause the transaction to be terminated?	Yes	—
RTA6	Is a transaction always started with a token?	Yes	—
RTA7	Is the data toggle implemented independently for each unidirectional endpoint?	Yes	—
RTA8	Does an isochronous data source ignore a handshake without impacting subsequent transactions?	Yes	—
RTA9	Can consecutive packets in the same direction be handled , provided there are two or more bit times of interpacket gap between each packet?	Yes	—

4.5 Transfers

Table 13. Transfers

ID	Question	Response	Sections in Spec
RTF1	Does the receipt of a nonzero length data packet in the status stage cause the transfer to be terminated with an error indication?	Yes	—

5 References

- USB Compliance Checklist Peripheral Silicon (excluding Hub Silicon), for the 2.0 USB Specification Checklist Version 1.08, December 18, 2001, available from the USB Organization at http://www.usb.org.
- Universal Serial Bus Specification Revision 2.0, April 27, 2000, available from the USB Organization at http://www.usb.org.

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