Application Note

Intelligent LLC SR Control Using C2000 and UCD7138

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ABSTRACT

In order to achieve reliable and intelligent synchronous rectification (SR) control for LLC resonant converters, this application report provides a detailed guidance on how to leverage C2000™ devices advanced features together with UCD7138 low-side MOSFET driver. The proposed schemes could help minimize the body diode conduction time to optimize the system efficiency and prevent the negative current risks for robust operation.

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C2000™ is a trademark of Texas Instruments.
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1 Introduction

LLC resonant converters are becoming increasingly popular in industry power applications. In order to achieve higher efficiency, the rectification diodes are replaced with SR MOSFETs to reduce the conduction losses. And it is common to use digital control for LLC converters due to flexibility and scalability, especially in higher power level applications. The SR control signals usually follow the primary side PWM signals, and the desired SR driving signal under different switching frequency f_S is given in Figure 1-1 [1]. With digital control schemes, SR operation could be divided into two modes: the SR pulse width is equal to approximately half of the switching period if f_S is above the LLC resonant frequency; the SR turn-off edge is determined by approximately half of the resonant period if below or equal to resonant frequency, that is SR clamp mode. However, the present schemes could not ensure the turn-on and turn-off edges are exactly at the SR current zero crossing point, which will vary during different load and input voltage conditions. Turning the SR on/off too early or too late will result in lower efficiency, negative current, or high drain-to source stresses, especially during the load/line transient operation [2].

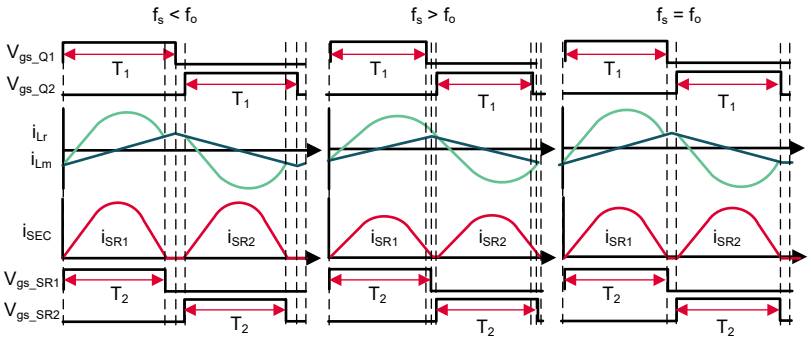

Figure 1-1. Desired SR Driving Signal Under Different f_S

In order to solve the SR control challenges, a smart gate driver UCD7138 was released with body-diode conduction sensing in the market. The UCD7138 gate driver senses the body diode conduction of the SR and reports to UCD3138A(A version of UCD3138 controllers), to achieve adaptive SR on-time control [3]. However, the turn-off edge optimization is handled by the DTC interface of UCD3138A, which also limits UCD7138's usage with other MCUs. The application report discusses how to use C2000 devices together with UCD7138 to provide an intelligent SR control scheme, mainly with the below three control targets, which it is challenging for conventional solutions to achieve.

- Minimize the body diode conduction time for high efficiency
- Fast negative current prevention for robust operation
- Automatically compensate the component variations during the SR clamp mode

The proposed control schemes apply for any third-generation of C2000 devices with configurable logic block (CLB) module inside.

2 SR Turn-On Edge Optimization

Figure 2-1 shows the system diagram for C2000 and UCD7138. Normally, digital control scheme will make the SR turn-on edge aligned with the primary side PWM, and further add the rising edge delay to the SR PWM signals. However, a fixed or larger than required rising edge delay could not provide optimal efficiency, due to longer body diode conduction time. Actually, using UCD7138 could optimize the turn-on edge essentially, with CTRL pin floating or connected to logic high (3.3 V).

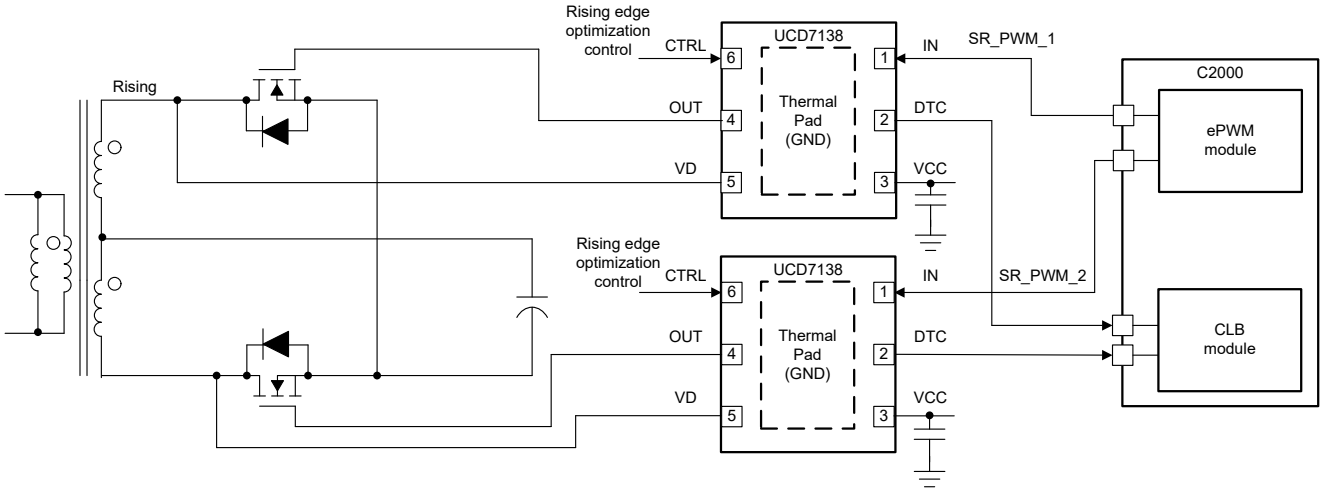

Figure 2-1. C2000 and UCD7138 System Diagram

Figure 2-2 shows the turn-on edge optimization scheme with UCD7138. IN is the gate-driver input-command signal from the digital controller, like C2000, and OUT is the SR-gate driver output signal. The DTC pin is the body-diode conduction detector output, and when the body diode of SR MOSFETs conducts, the DTC pin is low.

The actual gate turn-on timing is controlled by both the digital controller output IN and DTC. The OUT can only be turned on when IN is high. If DTC is already low at IN rising edge, turn on the gate driver output immediately; if DTC is still high at IN rising edge, turn on the gate driver output as soon as the DTC falling edge is received. While, the gate turn-off edge is determined by IN only. The gate is turned off immediately at the IN falling edge.

Thus, to make sure the turn-on edge to optimize freely, users could simply set the same rising edge for IN as the primary side PWM with C2000.

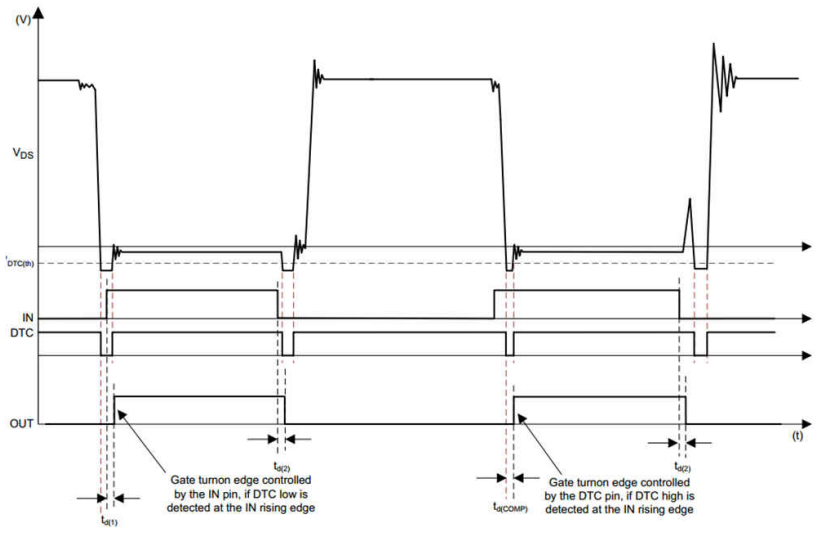

Figure 2-2. Turn-On Edge Optimization

3 Compensate the Component Variations During the SR Clamp Mode

As shown in Figure 1-1, normally most of present products will define a fixed value for the SR clamping width based on the ideal resonant tank parameters during the SR clamp mode. However, since the values of resonant capacitors and inductors must be different from part to part and might change over the lifetime. It is common to select a minimum resonant period for the SR clamp mode based on the possible variation ranges of resonant tank parameters, in order to avoid unexpected negative current. That means most of the products in mass production could not operate with the best efficiency, due to SR MOSFET turns off too early. It is also challenging for the time and cost required if the calibration process of the resonant tank is implemented during the manufacture process.

In order to compensate the component variations for the resonant tank and achieve optimal SR turn-off edge control, CLB module inside C2000 devices is used together with the DTC feedback from UCD7138.

As shown in Figure 3-1, the DTC signal from UCD7138 is fed into C2000, as one of the input signals for CLB module. The basic idea to is use CLB to count the body diode conduction time with the DTC signal under the SR clamp mode, so as to increase the SR on-time with turn off edge, until the captured duration time for the DTC low event is within the targeted value, shown in Figure 3-1.

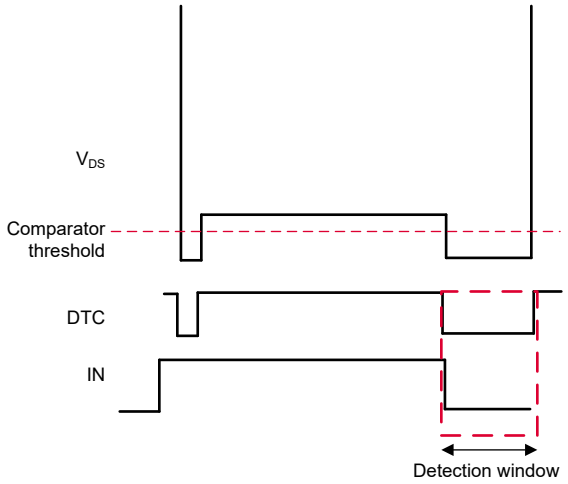

Figure 3-1. Body Diode Conduction Time Detection

The detailed steps are as follows.

1. During the initialization, the SR clamp on-time is set with the minimum value of resonant period/2, with the possible maximum values of the resonant capacitors and inductors.
2. Leverage CLB counter to detect the body diode conduction time. Since the UCD7138 turn-off edge is determined by the IN signal only, the detection window for the effective DTC low event is between the falling edge of the SR PWM signal and the rising edge of DTC signal. Thus, a counter of CLB could be used here.

   Since the counter will always reset to 0 if the “RESET” input remains high, the IN signal can be used to trigger the counter to start counting after the falling edge. Then, the inverting DTC signal is set as the MODE_0 input(active high to enable the counting). With MODE_1 set to 1, in this way, the duration of the DTC low event could be obtained.
3. During the SR clamp mode, increase the SR clamp on-time step by-step until the obtained DTC low time reduces to be less than a targeted value. Since such adjustment is not time critical, the software task could be placed in a background loop or a normal interrupt, with less CPU bandwidth occupied. In addition, the adjustment could be set as one-time effort or periodical event during the runtime depending on actual system requirements.

The below code snippets give an example for the SR clamp on-time adjustment, where the CLB counter value is required to be obtained through the R0 register in the High Level Controller (HLC) of CLB, and SR_clamp_mode refers to the SR clamp operation mode, and clamp_ajust_flag is used to indicate the adjustment is done, if the body diode conduction time after SR turns off is within 50 ns, for example.

```
if(clamp_ajust_flag && SR_clamp_mode)
{
   counter1_low = CLB_getRegister(CLB1_BASE, CLB_REG_HLC_R0);
   if(counter1_low>5)
   {
   SR_clamp_time=SR_clamp_time+2;
 }
 else
 {
   clamp_ajust_flag=0;
 }
}
```

4 Negative Current Detection and Prevention

During normal operation, SR control could be always aligned with the primary side PWM signals of LLC converters. However, during large load or line transient operation, the switching frequency of the LLC converter is changed rapidly. Due to the response discrepancy between the primary resonant current and the SR current, it is possible to induce a high risk that SR MOSFETs turn on too long than required, which will cause large negative current and high Vds spikes on SR MOSFETs. As shown in Figure 4-1, the negative current charges up the SR MOSFET drain-to-source capacitance and unexpected Vds overstress might pose a threat to SR MOSFETs when negative current occurs.

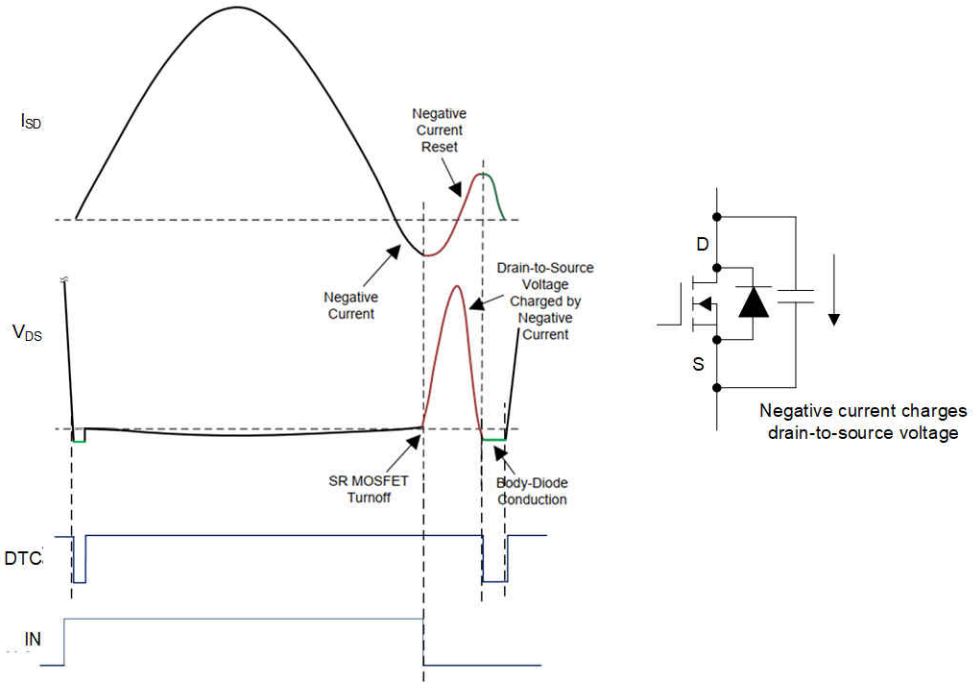

Figure 4-1. SR Drain-to-Source Voltage Shoot Up

In the previous art, there is a dedicated interface of UCD3183A controller to handle DTC signal so as to prevent the negative current issue [4]. Within the DTC detection window, shown in Figure 3-1, if no or very-short DTC low time is detected, it means the SR turns off too late. UCD3138A counts the body-diode conduction time of the current cycle and adjusts the SR on time in the next cycle. When the body diode conduction time sensed during the detection window is less than a certain threshold, UCD3138A will treat it as a fault and reduce the SR on time by a large pre-programmed amount.

Though C2000 devices did not provide the DTC interface for UCD7138, the application report discusses how to use CLB to implement the similar negative current prevention scheme with UCD7138. During the normal operations, it is safe to ensure the body diode conducts for a short time, so there will be no DTC high event during the detection window in Figure 3-1, while if turning off the SR too late, DTC will keep high for a while after the falling edge of IN. Thus, it is possible to count the duration of the DTC high time to detect the negative current event.

The below steps show how to leverage CLB module to detect the negative current and prevent it as soon as possible.

1. Define the detection window for the CLB counter, since only the high event between the falling edge of the IN signal and the rising edge of DTC signal is required to detect. The Finite State Machine (FSM) block is used to create the detection window, where E0 is referred to the falling edge of IN, while E1 is the rising edge of DTC, as shown in Figure 4-2. And the FSM equations for S0 can be deduced as

$$S0 = (S0 \,\&\sim E0) \mid (\sim S0 \,\& E1) \quad (1)$$

   Thus, S0 is used as the “RESET” input for Counter 0, which means the CLB counter will reset to 0 outside the detection window.

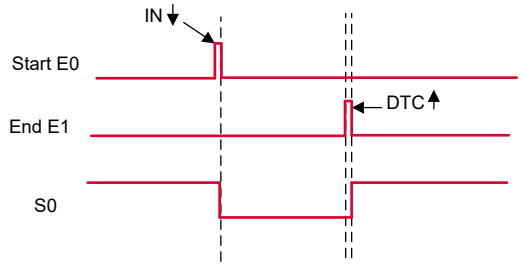

Figure 4-2. State Machine in the FSW Block

2. Then, the original DTC signal is set as the MODE_0 input for the counter, so that the DTC high time can be captured.
3. If the captured high-time of DTC is larger than a threshold, a CLB ISR is generated through HLC, indicating the negative current event, and then reduce the SR on time by a large pre-programmed amount for the next cycle. Note that the CLB ISR is suggested to set with highest priority, in order to protect the system with high reliability.

Figure 4-3 shows the completed CLB Tile configuration block diagram, including both resonant tank component compensation scheme in Section 3 and the negative current detection scheme. The CLB ISR is triggered by the Counter 0 MATCH1 event, where MATCH1 is set with the negative detection threshold, like 5, that is 50 ns. Besides, the S0 is also used to trigger HLC to move the counter value of Counter 1 from CLB to CPU at the rising edge of S0, that is also the end of the SR cycle, for the purpose of the SR clamp on-time adjustment.

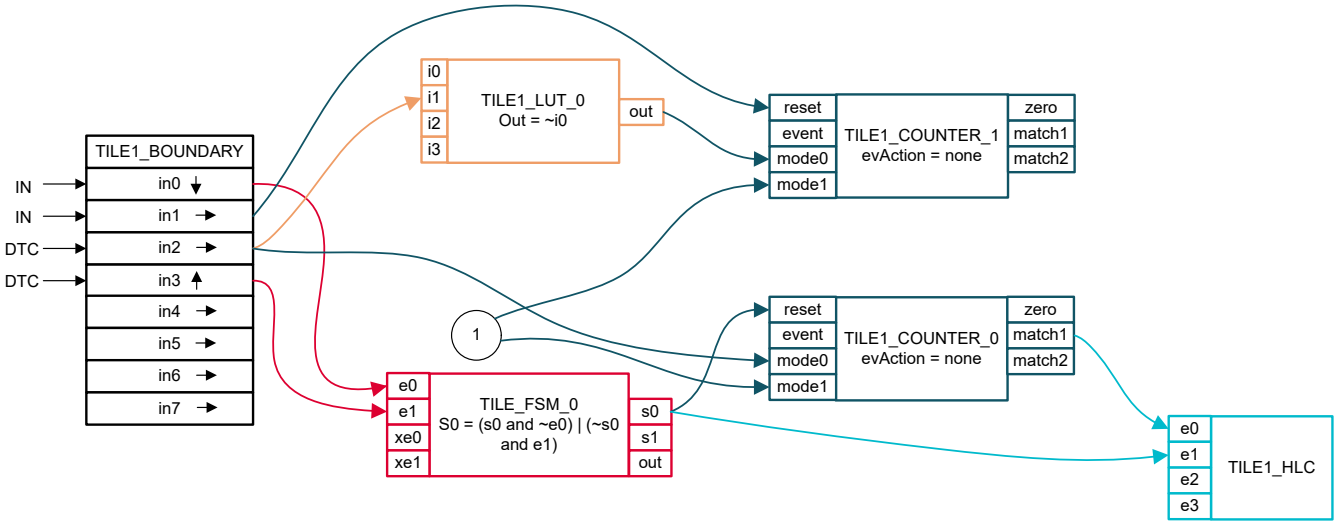

Figure 4-3. CLB Tile Configuration Block Diagram

The below code snippets give an example to show how to handle the negative event in the CLB ISR, where negative_current_flag is used to indicate the SR PWM register will change temporally due to the negative current event, and need to recover to the expected one later.

```
__interrupt void clb1ISR(void)
{

    negative_current_flag = 1;

EPWM2_CMPA = EPWM2_CMPA-reduce_step;
}
```

5 References

1. Fei C, Li Q, Lee F C. Digital implementation of adaptive synchronous rectifier (SR) driving scheme for high-frequency LLC converters with microcontroller[J]. IEEE Transactions on Power Electronics, 2017, 33(6): 5351-5361.
2. Wang F, McDonald B A, Langham J, et al. A novel adaptive synchronous rectification method for digitally controlled LLC converters [C]//2016 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2016: 334-338.
3. Texas Instruments: *Using UCD7138 and UCD3138A for Advanced Synchronous Rectification Control*
4. Texas Instruments: *UCD7138 4-A and 6-A Single-Channel Synchronous-Rectifier Driver With Body-Diode Conduction Sensing and Reporting Data Sheet*
5. Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Technical Reference Manual*

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2022) to Revision A (June 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updated Section 1	2

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