

Clocking Spreadsheet for K2E Device Family

ABSTRACT

This document discusses the internal clocking architecture of Texas Instruments K2Ex Digital Signal Processors (DSP) using a provided clocking spreadsheet.

The 66AK2Ex and AM5K2Ex devices have similar internal clocking architecture and peripherals except the corepac. The 66AK2Ex devices have both DSP corepac and ARM corepac, whereas, the AM5K2Ex devices have ARM corepac only.

Use the K2E clocking spreadsheet for 66AK2E05, 66AK2E02, AM5K2E04 and AM5K2E02.

The spreadsheet discussed in this document can be downloaded from the following URL:
<http://www.ti.com/lit/zip/sprac72>.

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1 Introduction

The PLL controllers on K2E devices offers flexibility and convenience with software configurable multipliers, dividers to modify the input clock signal internally. The PLL Controller also contains registers that are used to drive the PLLM, PLLD, OUTPUT DIVIDE and BYPASS logic of the PLL. The resulting clock outputs from the PLL Controller are passed to the corepac, peripherals and other modules inside the device. Furthermore, each input clock, PLL output and SerDes line rate has a frequency min and max limit and those have been considered in the clocking spreadsheet.

2 Peripheral Blocks Covered

The clocking spreadsheet has the following peripheral blocks:

- Main PLL
- NETCP PLL
- DDR3 PLL
- PCIe0
- PCIe1
- XFI
- SGMII
- MDIO (Ethernet)
- HYPERLINK0
- USB3.0
- EMIF16
- TIMER
- I2C
- SPI
- UART

3 References

- [66AK2Ex DSP+ARM](#)
- [AM5K2Ex ARM](#)
- [KeyStone Architecture Phase-Locked Loop \(PLL\) User's Guide](#)
- [Hardware Design Guide for KeyStone II Devices](#)

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