User's Guide

Hardware Design Considerations for Custom Board Using AM62P / AM62P-Q1 Family of Processors

ABSTRACT

This Hardware Design Considerations for Custom Board document gives an overview of the design considerations to be followed by the board designers while designing custom boards using any of the AM62P / AM62P-Q1 family of processors. This document is intended to be used as a guideline at different stages of custom board design by board designers.

Additionally, links are provided for processor product page, related collaterals, E2E FAQs and other commonly referenced documents that could help the board designers optimize the design efforts and schedule during custom board design.

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1 Introduction

The Hardware Design Considerations for Custom Board Using AM62P / AM62P-Q1 Family of Processors user's guide (document) provides a starting point for the board designers designing with any of these processors. This document provides an overview of the recommended design flow at different board design stages and highlights important design requirements that must be addressed. Note that this document does not include all of the information required to complete the custom board design. In many cases, this document refers to the device-specific collaterals and various other documents as sources for specific information.

This document is organized in a sequential manner. It starts from decisions that must be made during the initial planning stages of the custom board design, through the selection of processor and key attached devices, electrical and thermal requirements. For ensuring a successful board design, recommendations discussed in each of the section should be addressed before moving to the next section.

Note

This document may not cover every aspect of custom board design.

Note

These processors have capabilities to address safety requirements.

The focus of this document is non-safety applications.

1.1 Before Getting Started With the Custom Board Design

The processor family includes wide variety of peripherals and processing capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same processor can vary widely depending on the target application. Board designers must understand the requirements before selecting the processor and determining the board level implementation details. In addition, the custom board design may require additional circuitry to operate correctly in the target environment. Refer latest collaterals on TI.com including the device-specific data sheet, silicon errata, TRM and SK user's guide for selecting the processor and to determine the following:

- Expected environmental conditions for the processor operation, target boot mode, storage type and interfaces
- Processing (Performance) requirements for each of the cores in the selected processor
- Processor peripherals used for the attached devices

1.2 Processor Selection

Selection of processor is the most important stage of custom board design. To get an overview of the processor architecture and for selecting the processor variant, features, and speed grade, refer the *Functional Block Diagram* and *Device Comparison* sections of the device-specific data sheet.

1.3 Technical Documentation

A number of documents relevant to the selected processor are available on the processor product page on TI.com. It is strongly recommended to read through these documents before starting the custom board design.

The link below summarizes the collaterals that can be referred when starting the custom board design.

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – Collaterals to Get started

1.3.1 Updated Schematics With Design, Review and Cad Notes Added

During custom board design, customers tend to reuse the SK design files and make edits to the design file. Alternatively customers reuse some of the common implementations including the processor, memory and communication interfaces. Since the SK is expected to have additional functionalities, customers optimize the SK implementation to suit their board design requirements. While optimizing the SK schematics, errors get introduced into the custom design that could cause functional, performance or reliability issues. When optimizing customers have queries regarding the SK implementation resulting in design errors. Many of the optimization and design errors are common across designs. Based on the learning and data sheet pin connectivity

recommendations, comprehensive Design Notes (D-Note:), Review Notes (R-Note:) and Cad Notes (Cad Note:) have been added near each section of the SK schematic that customers could review and follow to minimize errors. Additional files as part of the design downloads have been included to support customer evaluation (https://www.ti.com/lit/zip/sprr487).

The list of available document in the single big zip files is listed in the below product overview document.

SK-AM62P-LP Design Package Folder and Files List (Rev. A)

Refer below FAQ that includes the PDF schematics and additional information related to starter kit SK-AM62P-LP:

[FAQ] AM62P / AM62P-Q1 - Custom board hardware design - Design and Review notes for Reuse of SK-AM62P-LP Schematics.

1.3.2 FAQs to Support Custom Board Design

Based on customer interactions we have been adding a number of FAQs for customer use.

The FAQ includes generic guidelines, learning based on customer interaction and some of the commonly asked queries related to the processor peripherals.

We have a master list that provides list of all available FAQs for the Sitara processor family.

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM64x, AM243x, AM335x) families

To make it easy for customers to use, we also listed the FAQs processor family wise.

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Note: The FAQs are being updated frequently. it is recommended to review the FAQs of interest on a regular basis for updated information,

1.4 Design Documentation

Updating the design documents periodically to capture all the requirements and design updates, observations during different stages of the custom board design is recommended. This updated information provides the basis for the documentation package and the design document is required when requesting external review support.

2 Block Diagram

A detailed block diagram, covering all the required functional blocks and interfaces is key to a successful custom board design.

2.1 Constructing the Block Diagram

Preparing a detailed block diagram is an important stage during the custom board design. The block diagram should include all major functional blocks, associated devices for processor functioning (Ex: PMIC) and attached devices. The block diagram should illustrate the interfaces and IOs used for interconnecting the processor and attached devices.

The below resources could be used as supporting documents when preparing the detailed block diagram:

- SK-AM62P-LP (AM62P / AM62P-Q1 starter kit for Sitara™ processors) and any other available SKs are a good source to start with the custom board design.
- The links referenced below for processor product folder on TI.com provides device-specific Functional Block Diagrams, Data Sheet, TRM, User Guides, Silicon Errata, Application Notes, design considerations, and other related information for different applications. The design and development section include SK information, design tools, simulation models and software information. As part of information related to support and training, links to commonly applicable E2E threads and FAQs are available.
  - AM62P Product Folder
  - AM62P-Q1 Product Folder

2.2 Configuring the Boot Mode

It is recommended to indicate the configured boot mode in the block diagram. This includes the primary boot and the backup boot.

The processor family includes multiple peripheral interfaces that support boot mode. Refer device-specific TRM for the available boot mode configurations and supported peripherals. The processor family supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode resistor configurations connected to the processor boot mode input pins provide information on the boot mode to be used by the ROM code during boot. The boot mode pins are sampled at power-on-reset (PORz_OUT), and the inputs must be stable before releasing (deassertion) the cold reset (MCU_PORz).

Boot mode configurations provide the below information:

PLL Config: BOOTMODE [02:00] – Indicates the system clock (PLL reference clock selection) frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration

Primary Boot Mode: BOOTMODE [06:03] – Configure the required primary boot mode, i.e, the peripheral/ memory to boot from

Primary Boot Mode Config: BOOTMODE [09:07] – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected

Backup Boot Mode: BOOTMODE [12:10] – Configure the required backup boot mode, i.e., the peripheral/ memory to boot from, in case primary boot fails

Backup Boot Mode Config: BOOTMODE [13] – This pin provides additional configuration options (optional - depends on the selected backup boot mode) for the backup boot devices

Reserved: BOOTMODE [14] – Reserved pin

POST: BOOTMODE [15] – Hardware Power-on-Self-test performed during processor power-up

Key considerations for boot mode configuration:

- It is recommended to always include provision to configure boot modes used during development, such as USB boot, UART boot or No-boot/Dev boot mode for JTAG debug
- Boot mode pins have alternate functions after latching of boot mode configuration. Ensure the board design takes this into account when choosing pullup or pulldown resistors for the boot mode pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the processor is reset (indicated by the PORz_OUT pin) to enable the processor to boot properly.
- Some boot mode pins functionalities are reserved. Any boot mode pins marked as Reserved or not used must not be left floating. It is recommended to pull the input high or low using a resistor. For details regarding connection of reserved boot mode pins, refer the *BOOTMODE Pin Mapping* section of the *Initialization* chapter of the device-specific TRM.

For details regarding supported boot modes, refer the *Initialization* chapter of the device-specific TRM.

Note

Board designer is responsible for providing provision to set the required boot mode configuration (using pullups or pulldowns, and optionally jumpers/switches and external ESD) depending on the required boot configuration. It is recommended to provide provision for pullup and pulldown for the boot mode pins that have configuration capability.

Shorting the boot mode pins together, leaving any of the boot mode pins unconnected or shorting of the boot mode inputs directly to supply or ground in not allowed or recommended.

Note

For updates related to supported boot modes and available boot mode functionality, see the device-specific silicon errata.

2.3 Confirming PinMux (PinMux Configuration)

The processor supports a number of peripheral interfaces. To optimize size, pin count and package while maximizing functionality, many of the processor pads (pins) provide provision to multiplex up to eight signal functions. Thus, not all peripheral interface instances would be available or can be used simultaneously.

TI provides SysConfig-PinMux Tool that supports board designer to configure the required function using PinMux tool for AM62P / AM62P-Q1 family of processors.

Note

Recommendation is to save the PinMux configuration generated using SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

After completion of the processor selection and block diagram updates, the next stage of the custom board design is to determine the power supply architecture for the selected processor.

3.1 Power Supply Architecture

The power supply architectures that could be considered are listed below:

3.1.1 Integrated Power

The power architecture could be based on Multi-channel ICs (PMIC) such as TPS65224-Q1.

For more information, refer the *Starter Kit SK-AM62P-LP* schematic.

For automotive functional safety use cases, connect MCU_I2C0 of the processor to PMIC (TPS65224/2) I2C1.

3.1.2 Discrete Power

The power architecture could be based on DC-DC converters and LDOs.

Currently TI does not have a discrete power architecture implementation to recommend but could be available in the future.

To get an overview of available solution, see the processor (AM62P / AM62P-Q1) product page.

3.2 Power (Supply) Rails

For the complete list of processor power supply rails and allowed supply range, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details for some select power rails.

Note

Ensure the power supplies connected to the processor supply rails are within the *Recommended Operating Conditions* of the device-specific data sheet.

3.2.1 Core Supply

Core supplies VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 are recommended to be powered from the same power source and can be operated at 0.75 V or 0.85 V (specified operating ranges defined in the *Recommended Operating Conditions* (ROC) table). When these supplies are operating at 0.75 V, it is recommended to ramp 0.75 V prior to all 0.85 V supplies.

VDDR_CORE is specified to operate only at 0.85 V. When VDD_CORE is configured to operate at 0.85 V, VDD_CORE and VDDR_CORE are recommended to be powered from the same source (ramp together).

VDD_CANUART is recommended to be connected to always on power sources when Partial IO (Low-power) mode is used. It is recommended to connect VDD_CANUART to the same power source as VDD_CORE when Partial IO mode is not used.

Peripheral core supplies VDD_MMC0 and VDDA_0P85_DLL_MMC0 are specified to operate at 0.85 V when MMC0 is used. It is recommended to connect VDD_MMC0 and VDD_0P85_DLL_MMC0 to the same power source as VDD_CORE when MMC0 is not used.

For more information, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

Note

For selection of core voltage, refer the *Operating Performance Points* section of the device-specific data sheet.

3.2.2 Peripheral Power Supply

The processor supports dedicated peripheral supplies for USB (common for USB0 and USB1), MMC0, PLLs and CSI_DSI (CSIRX0 and DSITX0). The recommended operating voltage is 1.8 V. An additional 3.3 V analog supply is required for USB.

For LPDDR4, DDR PHY IO (VDDS_DDR) and DDR clock IO (VDDS_DDR_C) supplies are recommended to be 1.1 V.

For more information, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Dynamic Switching Dual-Voltage IO Supply

An external LDO with capability to generate the dynamic voltage is recommended.

VDDSHV5 and VDDSHV6 IO supply rails for MMC1..2 have been designed to support power-up, power-down, or dynamic supply voltage change without any dependency on other supplies. This capability is required to support UHS-I speed.

3.2.4 Internal LDOs for IO Groups (Processor)

The processor supports eight internal LDOs (CAP_VDDSx [x = 0..3, 5..6], CAP_VDDS_CANUART and CAP_VDDS_MCU) and each of the LDO output connects to a separate ball (pin) for connecting an external capacitor. For guidance on recommended capacitance and connection, refer the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet.

3.2.5 Dual-Voltage IOs (for Processor IO Groups)

The processor supports eight Dual-voltage IO domains (VDDSHVx [x = 0..3, 5..6], VDDSHV_MCU and VDDSHV_CANUART), where each IO domain provides power to a predefined set of IOs. Each IO domain can be individually configured for 3.3 V or 1.8 V. This supply powers all the predetermined IOs in the IO supply group. All IOs (attached devices) connected to these IO domains must be powered from the same power source that is being used to power the respective processor Dual-voltage IO domains (VDDSHVx supply rail).

Most of the processor IOs are not fail-safe. For information on available fail-safe IOs, see the device-specific data sheet. It is recommended to power IO supply of attached devices from the same power source as the respective processor Dual-voltage IO domains (VDDSHVx supply rail) to ensure the system/board never applies potential to an IO that is not powered. This is needed to protect the IOs of processor and attached devices.

For more information, see the [FAQ] AM625 / AM623 Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe). This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

Available IO groups information is summarized below:

VDDSHV0 – Dual-voltage IO supply for General IO group

VDDSHV1 – Dual-voltage IO supply for Flash IO group

VDDSHV2 – Dual-voltage IO supply for GEMAC IO group

VDDSHV3 – Dual-voltage IO supply for GPMC IO group

VDDSHV5 – Dual-voltage IO supply for MMC1 IO group

VDDSHV6 – Dual-voltage IO supply for MMC2 IO group

VDDSHV_MCU – Dual-voltage IO supply for WKUP_MCU IO group

VDDSHV_CANUART – Dual-voltage IO supply for CANUART IO group

Note

VDDSHV4 IO supply rail is not available.

Note

It is recommended to connect VDDSHV_CANUART to an always on power sources when Partial IO (Low-power) mode is used.

3.2.6 VPP (eFuse ROM Programming) Supply

VPP power supply can be sourced on-board or externally.

VPP pin can be left floating (HiZ) or pulled down to ground through a resistor during processor power-up, power-down and during normal processor operation.

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must applied only after completion of processor power-up sequence.
- It is recommended to use a fixed LDO with higher input supply (2.5 V or 3.3 V) and enable input. The enable input is required to be controlled by the processor GPIO for timing.
- The VPP power supply is expected to see high load current transients and local bulk capacitors are likely required near the VPP pin to support the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor.
- A maximum current of 400-mA is specified during programming.
- When an external power supply is used, the supply is recommended to be applied after the processor power supplies ramp and are stable.
- When external power supply is used, recommend adding on-board bulk capacitor, decoupling capacitor and discharge resistor near to the processor VPP supply pin. Add a test point to connect external power supply and provision to connect one of the processor GPIO to control timing of the external supply.
- It is recommended to disable the VPP supply (left floating (HiZ) or grounded) when not programming the OTP eFuses.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

For more information, refer the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining Board Power Requirements

The current (maximum and minimum) requirements for each of the supply rails are not provided in the device-specific data sheet. These requirements are highly application dependent and must be estimated using TI provided tools for a specific use case.

3.4 Power Supply Filters

The processor supports multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_1P8_OLDI0, VDDA_1P8_CSI_DSI, VDDS_MMC0, VDDS_OSC0, VDDA_MCU and VDDA_PLLx [x = 0..4]. Refer *Starter Kit SK-AM62P-LP* for implementation of power supply filtering.

For more information, see the [FAQ] AM625 / AM623 Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

3.5 Power Supply Decoupling and Bulk Capacitors

To decouple the processor and attached device supplies from board noise, decoupling and bulk capacitors are recommended. Refer the *Starter Kit SK-AM62P-LP* schematic for implementing the decoupling and bulk capacitors.

For guidance on optimizing and placement of the decoupling and bulk capacitors, refer the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

3.5.1 Note on PDN Target Impedance

The PDN target impedance values are provided for specific supplies. The PDN target impedance values are not provided for all supply rails since the target impedance calculation includes reference to the maximum current on the power rails and is dependent on use case.

For updates on the PDN target impedance supplies and values, see the [FAQ] AM62P / AM62P-Q1 Custom board hardware design – Collaterals to Get started. Look for PDN target impedance values (VDD_CORE and VDDS_DDR).

3.6 Power Supply Sequencing

A detailed diagram of the required *Power Supply Sequencing* (Power-Up and Power-Down) are provided in the device-specific data sheet. All power supplies associated with the processor should allow for controlled supply ramp (Refer supply slew rate) and supply sequencing (using a PMIC-based power supply or using on-board logic when discrete power solution is used).

For more information, refer the *Power Supply Requirements, Power Supply Slew Rate Requirement, Power Supply Sequencing* section of the device-specific data sheet.

For more information, see the [FAQ] AM625/AM623 Custom board hardware design – Processor power-sequencing requirements for power-up and power-down. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

3.7 Supply Diagnostics

The processor supports below voltage monitors:

- VMON_VSYS (Recommend provisioning the external resistor voltage divider for early supply failure indication irrespective of the software implementation): For connecting the system voltage (main supply voltage such as 5 V or other voltage levels) through an external resistor voltage divider, refer the *System Power Supply Monitor Design Guidelines* section of the device-specific data sheet. It is recommend to implement a noise filter (capacitor) across the resistor voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients. It is recommended to always provide resistor divider provision for early detection.
- VMON_1P8_SOC and VMON_3P3_SOC (Monitoring): These pins are recommended to be connected directly to their respective 1.8 V and 3.3 V supplies. For the allowed supply voltage range, refer the *Recommended Operating Conditions* section of the device-specific data sheet.

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the voltage monitoring pins when not used.

3.8 Power Supply Monitoring

For optimizing the custom board performance, provide provision for external monitoring of supply rails and load currents.

For more information, refer the *Starter Kit SK-AM62P-LP* schematics for implementation.

Now that the power supply architecture and the power supply devices for generating the supply rails have been finalized, update the block diagram to include the power supply rails and interconnection. It is also recommended

to create a power supply sequence (Power-Up and Power-Down) diagram and verify the sequence with the device-specific data sheet.

4 Clocking

The next stage of the custom board design is proper clocking of processor and attached devices. The processor clock can be generated internally using external crystal or an LVCMOS compatible clock input can be used. Follow the connection recommendations in the device-specific data sheet when using an external clock. This section describes the available processor clock sources and the requirements.

4.1 Processor External Clock Source

The recommended processor clock sources and recommended connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

A 25 MHz external crystal interface pins connected to the internal high frequency oscillator (MCU_HFOSC0) or MCU_OSC0 LVCMOS digital clock is the default clock source for internal reference clock HFOSC0_CLKOUT.

Low-frequency oscillator (LFOSC0) has limited use case and is optional. Based on the use case, select a 32.768 kHz crystal as clock source. For more information, see the [FAQ] AM625: LFOSC usage in the device. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

4.1.1 Unused WKUP_LFOSC0

For guidance on the recommended connections for unused clock, refer the *WKUP_LFOSC0 Not Used* section in the *Specifications* chapter of the device-specific data sheet.

4.1.2 LVCMOS Digital Clock Source

The MCU_OSC0_XI and WKUP_LFOSC0_XI clock inputs can be sourced from a 1.8 V LVCMOS square-wave digital clock source. For more details, refer the *Timing and Switching Characteristics, Clock Specifications, Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to connect the MCU_OSC0_XO and WKUP_LFOSC0_XO pins as per the device-specific data sheet recommendation.

4.1.3 Crystal Selection

When selecting a crystal, the board designer must consider the temperature and aging characteristics based on the worst case operating environment and expected life expectancy of the board. Verify the crystal load and the crystal load cap value used matches the data sheet recommendations.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding Crystal selection. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

For more information, refer the *MCU_OSC0 Crystal Circuit Requirements* and *WKUP_LFOSC0 Crystal Electrical Characteristics* tables of the device-specific data sheet.

It is recommended to verify the crystal selection with the crystal manufacturer as required.

4.2 Processor Clock Outputs

Processor IOs (pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for attached devices (external peripherals).

For more details, refer the device-specific data sheet and TRM.

5 JTAG (Joint Test Action Group)

TI supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. Although JTAG is not required for operation, it is recommend to include the JTAG connection in the custom board design.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the processor configuration.

The BSDL Model for boundary scan testing can be downloaded.

- AM62Px Sitara™ BSDL Model

As an emulation interface, the JTAG port can be used in different modes:

- Standard emulation: requires only five standard JTAG signals.
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the processor configuration.

For supported JTAG clocking rates, refer the device-specific TRM.

5.1.2 Implementation of JTAG / Emulation

The JTAG and Emulation signals are in same power domain. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 signals are powered by the VDDSHV_MCU (Dual-voltage IO) supply rail (IO supply for IO group MCU). VDDSHV_MCU can be configured either 1.8 V or 3.3 V.

For proper implementation of the JTAG interface, refer the *Emulation and Trace Headers Technical Reference Manual* and *XDS Target Connection Guide* .

5.1.3 Connection of JTAG Interface Signals

For connecting the JTAG interface signals, refer the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

In case JTAG interface is not used, it is recommended to always provide provision for connecting the JTAG interface signals using test points for development testing and the required pulls as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

6 Configuration (Processor) and Initialization (Processor and Device)

It is recommended to deassert (release) the processor cold reset input (MCU_PORz) only after all the processor supplies ramp and delay of recommended hold time (in ms) for the crystal / oscillator to start-up and stabilize (refer device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor supports three external reset input pins (MCU and Main Domain cold reset request input (MCU_PORz), MCU and Main Domain warm reset request input (MCU_RESETz) and Main Domain warm reset request input (RESET_REQz)). Note the errata related to MCU_RESETz and MCU_RESETSTATz.

Be sure to make the recommended connections as per *Pin Connectivity Requirements* section of the device-specific data sheet.

The supported reset configurations are described in detail in the device-specific data sheet and TRM.

The processor provides three reset status output pins including Main Domain POR (cold reset) status (PORz_OUT) output, MCU Domain warm reset status (MCU_RESETSTATz) output and Main Domain warm reset status (RESETSTATz) output. Note the errata related to MCU_RESETz and MCU_RESETSTATz.

Use of reset status outputs are application dependent. Reset status outputs when not used can be left unconnected. It is recommended to provide provision for a test point for testing or future enhancements. An optional pulldown is recommended.

For MCU_PORz (3.3 V tolerant, fail-safe input), a 3.3 V input can be applied. The input thresholds are a function of the 1.8 V IO supply voltage (VDDS_OSC0).

It is recommended to hold the MCU_PORz low during the supply ramp-up and crystal/oscillator start-up. Follow the recommended MCU_PORz timing requirement in the *Power-Up Sequencing* diagram of the device-specific data sheet.

Additional reset modes are available through processor internal registers and emulation.

Note

MCU_RESETz and MCU_RESETSTATz have specific use case recommendation. Refer advisory i2407 of the device-specific silicon errata.

6.2 Latching of Boot Mode Configuration

For more details about the processor boot mode options, see above Section 2.2.

Boot mode configurations for processor are latched at the rising edge of PORz_OUT. The device configuration and boot mode input pins have alternate multiplexed functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their alternate functions. The PORz_OUT reset status output indicates latching of boot mode configuration. PORz_OUT optionally can be used for latching the Pin strap configuration for attached devices.

6.3 Resetting the Attached Devices

Using an ANDing logic to reset the attached devices as applicable (on-board Media and Data Storage devices, and other peripherals) is recommended. Processor general purpose input/output (GPIO) pin is connected to one of the AND gate input with provision for 0 Ω to isolate the GPIO input for testing or debug. Processor IO buffers are off during reset. It is recommended to place a pullup near to the AND gate input to prevent the AND gate input from floating and enabling the reset logic controlled by the processor IO during power-up. Main Domain POR (cold reset) status output (PORz_OUT) or Main Domain warm reset status output (RESETSTATz) signal could be connected as the other input to the AND gate. Ensure the processor IO supply and the pullup supply used near to the AND logic input are sourced from the same power source.

The choice of reset status output is application dependent. Ensure the attached device reset inputs are pulled as per the device recommendations.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of RESETSTATz matches IO voltage level of the attached device. A level translator is recommended to match the IO voltage level.

It is recommended to provision for a software enabled (controlled) power switch (load switch) that sources the SD Card power supply (VDD). A fixed 3.3 V supply (IO supply connected to the processor) is connected as input to the power switch.

Use of power switch allows power cycling of the SD Card (since this is the only way to reset the SD Card) and resetting the SD Card back to its default state.

For more information on implementing reset logic for the attached devices and power switch enable logic for SD Card, refer the *Starter Kit SK-AM62P-LP* schematic.

6.4 Watchdog Timer

Use of watchdog timer is based on the application requirement. Consider using internal or external watchdog timer.

7 Processor Peripherals

This section covers the processor peripherals and modules, and is intended to be used in addition to the information provided in the device-specific Data Sheet, TRM, and relevant Application Notes. The three types of documents could be used are:

- Data Sheet: Pin Description, Device operational modes, AC Timings, Guidance on pin functions, Pin mapping
- TRM: Functional Description, Programming Guide, Information regarding registers and configuration
- Application Notes: Board-level understanding and resolving commonly observed issues

7.1 Selecting Peripherals Across Domains

The processor architecture includes multiple domain, each domain includes specific processing cores and peripherals:

- MAIN Domain
- Microcontroller (MCU) Domain
- Wakeup (WKUP) Domain

For most use cases, peripherals from any of the domain can be used by any of the core. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access most of the peripherals in the MCU Domain. Similarly, MCU can access most of the peripherals in the Main Domain.

7.2 Memory (DDRSS)

DDR Subsystem currently supports LPDDR4 memory interface. Refer *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter of device-specific data sheet for data bus width, inline ECC support, speed and max addressable range selection.

The allowed memory configurations are 1 X 32-bit or 1 X 16-bit.

1 X 8-bit memory configuration is not a valid configuration.

Based on the application requirements, same memory (LPDDR4) device can be used with the AM625 / AM623 / AM625-Q1 / AM620-Q1 , AM62A7 / AM62A3 and AM62P / AM62P-Q1 processors due to the availability of 1 X 16-bit configuration.

When the AM62P / AM62P-Q1 processors are configured for 16-bit configuration, follow the DQS2..3 and other unused signal connection recommendations shown in the 16-Bit, Single Rank LPDDR4 Implementation example of the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* .

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the DDRSS signals when not used and DDR design guide for signals when LPDDR4 is used.

For more details, refer the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

For more information on DDR4 / LPDDR4 memory interface, see the [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDR4 / LPDDR4 MEMORY Interface.

7.2.1 Processor DDR Subsystem and Device Register Configuration

The DDR controller and DDR PHY have a large number of parameters to configure. To facilitate the configuration, an online tool (SysConfig tool) is provided that generates an output file that is consumed by the driver. Choose DDR Subsystem Register Configuration from the Software Product pulldown menu and choose the required processor. This tool takes board information, timing parameters from DDR device data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then initiates the full training sequence.

The SDK has an integrated configuration file for the memory (LPDDR4) device mounted on the SK. If you need a configuration file for a different memory (LPDDR4) device, a new configuration file has to be generated using the DDR Register Configuration tool.

For more information, see the [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

7.2.2 Calibration Resistor Connection

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations in the device-specific data sheet. Follow the device-specific SK schematics for connecting the recommended resistors (ZQ and Reset) to the memory devices and the values.

7.3 Media and Data Storage Interfaces

Media and Data Storage interface supports 3 X Multi-Media Card/Secure Digital (MMC/SD/SDIO) (8b+4b+4b).

MMC0 supports 8-bit eMMC interface (Refer *MMC0 - eMMC Interface* section of device-specific data sheet for speed). EMMCPHY is a dedicate hard PHY implementation. The required pulls for the eMMC interface is implemented internal to the hard PHY and JEDEC compliant. Refer *Pin Connectivity Requirements* section of device-specific data sheet for MMC0 interface signals connection recommendations when MMC0 interface is not used.

MMC1/MMC2 supports 4-bit SD/SDIO interface (Refer *MMC1/MMC2 - SD/SDIO Interface* section of device-specific data sheet for speed).

Additionally 1 X General-Purpose Memory Controller (GPMC) and 1 X OSPI/QSPI interfaces are supported.

For more information on eMMC memory interface, see the [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface.

For more information on OSPI/QSPI memory interface, see the [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface.

For information related to OSPI/QSPI, see the [FAQ] OSPI FAQ for Sitara/Jacinto devices.

For more details, refer the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Common Platform Ethernet Switch 3-port Gigabit (CPSW3G - for Ethernet Interface)

The CPSW3G interface can be configured either as a 3-port switch (interfaces to two external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having their own MAC address.

CPSW3G supports RMII (10/100) or RGMII (10/100/1000) interface for each of the external Ethernet interface port.

For RMII interface implementation, refer the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G RMII interface support interfacing to Ethernet PHY configured as controller (master) or device (slave).

CPSW3G interfaces to RMII EPHY configured for external 50 MHz (Buffered External Oscillator or processor clock out) as EPHY clock input (one of the buffered clock output connects to processor MAC) or 25 MHz EPHY clock input with 50 MHz clock output from EPHY connected to the processor.

One of the CPSW3G port is an internal CPPI (Communications Port Programming Interface) host port. It is a streaming interface to provide data from DMA to CPSW3G and vice-versa.

CPSW3G allows using mixed RGMII/RMII interface topology for the 2 X external interface ports.

RGMII_ID (internal delay) is not timed, tested, or characterized. RGMII_ID is enabled by default and the register bit is reserved.

For more details on the CPSW3G Ethernet interface, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Programmable Real-Time Unit Subsystem (PRUSS)

The processor family does not support PRUSS.

7.6 Universal Serial Bus (USB) Subsystem

The processor supports up to two USB 2.0 Ports. These Ports are configurable as host or device or Dual-Role Device (DRD). USBn_ID (identification) functionality is supported using any of the processor GPIO.

Follow the *USB VBUS Design Guidelines* section of the device-specific data sheet to scale the USB VBUS voltage (supply near the USB interface connector) before connecting to USBn_VBUS [n = 0..1] pins as applicable.

VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) input is recommended to be connected when the USB interface is configured in device mode. Connection of VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) is optional in host mode.

A power switch with OC (over current) output indication is recommended when the USB interface is configured as host for VBUS control. The USB DRVVBUS drives the power switch. It is recommended to connect the OC output to a processor GPIO (input), when the USB interface is configured as host.

For details related to USB connections and On-The-Go feature support, refer the device-specific TRM.

For more details, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

When USB0 and USB1 are not used, refer the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the USB supply pins.

When USB0 or USB1 is not used, refer the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the interface signals and USB supply pins.

For more information on USB2.0 interface, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – USB2.0 interface. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

7.7 General Connectivity Peripherals

The processor supports multiple instances of UART, Multichannel Serial Peripheral Interface (MCSPI), I2C, Multichannel Audio Serial Port (MCASP), Enhanced Pulse Width Modulator (EPWM), Enhanced Quadrature Encoder Pulse (EQEP), Enhanced Capture (ECAP), MCAN (Modular Controller Area Network) with Full CAN-FD support and GPIO modules.

Note

For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration. Refer *Pin Connectivity Requirements* section of device-specific data sheet.

When these open-drain output type buffer I2C interfaces are pulled to 3.3 V supply, the inputs have slew rate limit specified. An RC is recommended used to limit the slew rate. Refer *Starter Kit SK-AM62P-LP* for implementation.

An external pullup is recommended for the I2C interfaces (I2C0..3) with LVCMOS IOs emulated open-drain outputs when the IOs are configured for I2C interface. For the available LVCMOS IOs with emulated open-drain output I2C instances, refer the device-specific data sheet.

For more information, refer below FAQs:

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – I2C interface

[FAQ] AM62A7-Q1: Internal pull configuration registers for MCU_I2C0 and WKUP_I2C0. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

The number of peripheral instances available depends on the processor selection. The required interfaces can be configured using the SysConfig-PinMux tool based on the application.

For more details, refer the *Peripherals* chapter of the device-specific TRM.

7.8 Display Subsystem (DSS)

The processor supports OLDI (1 X OLDI-DL (Dual Link), 1 X OLDI-SL (Single Link), and 2 X OLDI-SL), MIPI® DSI: with 4 Lane MIPI® D-PHY and DPI (24-bit RGB parallel interface) display interfaces.

2 X OLDI-SL interface supports independent display streams (non-duplicate mode).

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the OLDI0 or DSITX0 signals when not used.

For more details, refer the *Display Subsystem and Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

For more information on DPI, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB. This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

For more information on OLDI, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM62P Custom board hardware design – OLDI (Open LVDS Display Interface) capabilities.

7.9 Camera Subsystem (CSI)

The processor supports one Camera Serial interface (CSI-2) Receiver with 4 Lane D-PHY. Support for 1,2,3 or 4 data lane mode. Refer *Multimedia, Camera Serial interface (CSI-2) Receiver with Lane D-PHY* section in the *Features* chapter of device-specific data sheet for supported data rate.

The DPHY-RX supports a single clock lane and all the data lanes are clocked at the same frequency. The frame rate is determined by start-of-frame, end-of-frame signaling and allows handling the input sources with different frame rates per channel.

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting interface pins and supply pins when CSIRX0 interface is not used.

For more details, refer the *Camera Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

For more information on DPI, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM62A / AM62P Custom board hardware design – CSI-2 capabilities.

7.10 Connection of Processor Power Supply Pins, Unused Peripherals and IOs

All the processor power supply pins must be supplied with the supply voltages specified in *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified.

The processor has pins (package balls) that have specific connectivity requirements and pins (package balls) that are recommended to be left unconnected or can be left unused.

For information on connecting specific unused processor peripherals and IOs, refer the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

For more information on processor unused peripherals and IOs, see the [FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC Unused peripherals and IOs.

7.10.1 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type buffer, fail-safe IO. It is recommended to connect an external pullup resistor when external configured as IO or external input is not actively driven or a PCB trace is connected to the

pad. Open-drain output type buffer IOs have slew rate specified. An RC is recommended when the IO is pulled up to 3.3 V.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1/ AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection.

7.10.2 Reserved Pins (Signals)

Pins named RSVD are Reserved. RSVD pins must be left unconnected. It is recommended not to connect any PCB trace or test points to the pins.

8 Interfacing of Processor IOs (LVCMOS or Open-Drain or Fail-Safe Type IO Buffers) and Simulations

An important check point during the custom board design before the schematic design and capture is to confirm electrical compatibility (DC and AC) between the processor and attached devices.

- The device-specific (processor and attached devices) data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, it is recommended to run simulations using IBIS models provided.

  The IBIS Model can be downloaded.

  – AM62Px Sitara™ IBIS Model

For more information, refer the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices* .

9 Power Consumption and Thermal Analysis

The board power consumption depends on selected processor, peripherals connected, features implemented, application, operating temperature requirements, and temperature/voltage variations.

9.1 Power Estimation

For estimating the processor power, use *AM62Px Power Estimation Tool*

9.2 Maximum Current for Different Supply Rails

For availability, check processor (AM62P / AM62P-Q1) product page.

9.3 Power Modes

For more details on the available power modes, refer the *Power Modes* sub-section, *Power* section in the *Device Configuration* chapter of the device-specific TRM.

9.4 Thermal Design Guidelines

The *Thermal Design Guide for DSP and Arm Application Processors* application report provides guidance for successful implementation of a thermal solution for custom board designs using Sitara family of processors. This application report provides background information on common terms and methods. Any follow-up design support that may be required will be provided only for board designs that follow thermal design guidelines contained in the application report.

The Thermal Model can be downloaded.

- AM62Px Sitara™ Thermal Model.

10 Schematic Design, Capture, Entry and Review

At this stage of the custom board design, schematic design, capture and entry can be started.

The below FAQ summarizes key collaterals that could be referenced during schematic design and review of the schematics.

[FAQ] AM64x, AM62x, AM62Ax, AM62Px Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

Refer below sections during the schematic design and capture stage:

10.1 Selection of Components and Values

Be sure to use the recommended values including the tolerance and voltage rating in the device-specific data sheet as applicable when selecting the passive components.

10.2 Schematic Design and Capture

During the schematic design and capture stage of the custom board design, the schematics can be drawn newly or SK schematics can be reused. Refer the *Starter Kit SK-AM62P-LP* schematic.

During schematic design and capture, follow *AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Schematic Design and Review Checklist* and device-specific silicon errata.

The link below summarizes the considerations board designers are required to be familiar when reusing TI SK design files.

[FAQ] AM62P / AM62P-Q1 Custom board hardware design - Reusing TI SK (EVM) design files.

Note

When SK schematics are reused, ensure completeness of functionality and change in net name due to redesign are reviewed. Read the notes added on the schematics pages near to the circuit implementation.

When SK schematics are reused, the DNI settings for the components could be reset. Make sure the DNIs are reconfigured (populating DNIs could affect the functionality). Read the notes added on the schematics pages near to the circuit implementation.

10.3 Schematics Review

After completing the schematic design and capture, verify the custom board design against the *AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Schematic Design and Review Checklist* .

For more information on used pins / unused pins / peripherals handling, see the [FAQ] AM62x, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals ? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSx, ...). This is a generic FAQ and can also be used for AM62P / AM62P-Q1 family of processors.

Plan a schematic review internally to review the schematics with reference to the *Schematic Design and Review Checklist*. Verify circuit implementation for design errors, value or connection inaccuracies, missing net connections, and so forth.

Be sure to verify the schematics with *Pin Connectivity Requirements* section of the device-specific data sheet.

11 Floor Planning, Layout, Routing Guidelines, Board Layers and Simulation

After completing the schematic design, capture and review (self, team and external), the recommendation is to perform floor planning of the board to determine the interconnect distances between the different devices, board size and outline.

The next stage in the custom board design is the layout. Refer below sections for recommendations related to the board layout.

11.1 Escape Routing for PCB Design

The *AM62Px Escape Routing for PCB Design* application note provides a sample PCB escape routing for the AM62P / AM62P-Q1 family of processor.

11.2 LPDDR4 Design and Layout Guidelines

Refer to *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* . The goal of the guide is to simplify the LPDDR4 implementation. Requirements have been captured as a set of layout (placement and routing)

guidelines that allow board designers to successfully implement a robust design for the topologies supported by the processor. Any follow-up design support that may be required will be provided only for board designs using LPDDR4 memory that follow the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*.

Refer to the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* for the recommended target impedance for the LPDDR4 clock, address and control signals and for information regarding LPDDR4 Count, Channel Width, Number of Channels, Number of Dies, Number of Ranks.

For the propagation delay, the delay to be considered for LPDDR4 is the delay related to the traces on the board. Refer *Appendix: SOC Package Delays* of *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* when required.

In-case package level propagation delay is required, reach-out to the local TI sales representative.

It is highly recommended to perform Signal Integrity (SI) simulations during board schematic design and layout stage.

Note

Data bits swizzle and byte swap is supported in the family of processors. Refer *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*.

Note

Interface to DDR4 memory is currently not supported.

Note

DDR2 and DDR3 interfaces are not supported.

11.3 High-Speed Differential Signal Routing Guidelines

The *High-Speed Interface Layout Guidelines* application note provides guidelines for successful routing of the high-speed differential signals. Guidelines include PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. Any follow-up design support that will be required will be provided only for board designs that follow *High-Speed Interface Layout Guidelines*.

Note

Consider using the *Starter Kit SK-AM62P-LP* layout as reference.

11.4 Board Layer Count and Stack-up

The critical constraint in determining layer count is the number of layers required to implement the high-speed LPDDR4 interface. Memory layout meeting the recommended guidelines typically requires the number of layers used in the Starter Kit (TI recommended). Optimization of layer count could be possible based on the custom board design and functionalities.

Refer the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* available on TI.com for further guidance and best practices in implementing the LPDDR4 memory interface.

Refer to *AM62Px Escape Routing for PCB Design* guide. Use of TI Via Channel Array (VCA) technology with the AMH package supports further layer optimization.

The AM62Px VCA solution package supports similar feature set as several other competition solutions with approximately 15% smaller package area and ~10% wider line width. This solution reduces the PCB foot print and utilizes lower cost PCB rules, enabling compact and cost optimized systems.

11.4.1 Simulation Recommendations

Simulation is recommended for any layout changes or optimizations done with respect to the SK layout.

11.5 Reference for Steps to be Followed for Running Simulation

To get an overview of the basic system-level board extraction, simulation, and analysis methodologies for high-speed LPDDR4 interfaces, refer *LPDDR4 Board Design Simulations* chapter of the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* .

12 Board Assembly and Bring-up

The next step in the board design is board assembly and bring-up.

Before powering the board do ensure no DNP or DNI components have been mounted.

Refer below FAQs during board bring-up:

[FAQ] AM625 / AM623 / AM62A Design Recommendations / Commonly Observed Errors during Circuit Optimization of Custom board hardware design

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62Ax, AM62Px)

[FAQ] AM625 / AM623 / AM62A Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics Design Update Note

13 Device Handling and Assembly

Moisture Sensitivity Level (MSL) rating/Peak reflow rating depends on the package dimensions (thickness and volume).

Recommended reviewing the device thickness information, ball pitch, Lead finish/Ball material and the recommended MSL rating/Peak reflow to be followed.

For more information, see the links below:

AM62P Ordering & quality

AM62P-Q1 Ordering & quality

13.1 Soldering Recommendations

Note the MSL rating/Peak reflow recommendation on TI.com for the selected processor.

13.1.1 Additional References

For more information on Moisture sensitivity level, refer below:

MSL Ratings and Reflow Profiles

Moisture sensitivity level search .

14 References

14.1 Processor Specific

- Texas Instruments: *AM62Px Sitara™ Processors Data Sheet*
- Texas Instruments: *AM62Px Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62Px Silicon Errata*
- Texas Instruments: *Starter Kit SK-AM62P-LP*
- Texas Instruments: *PMIC for Powering AM62Px Devices*
- Texas Instruments: *AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Schematic Design and Review Checklist*
- Texas Instruments: *AM62Px Escape Routing for PCB Design*
- Texas Instruments: *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*
- Texas Instruments: *SK-AM62P-LP Design Package Folder and Files List (Rev. A)*

14.2 Common

- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *XDS Target Connection Guide*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *High-Speed Layout Guidelines*
- Texas Instruments: *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines*

- Texas Instruments: *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Texas Instruments: *Moisture sensitivity level search*
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments: *Jacinto™ 7 DDRSS Register Configuration Tool*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *Clocking Design Guide for KeyStone Devices*
- Texas Instruments: *Using IBIS Models for Timing Analysis*
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs*

15 Terminology

BSDL	Boundary-Scan Description Language
CAN	Controller Area Network
CAN-FD	Controller Area Network Flexible Data-Rate
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
CSIRX	Camera Streaming Interface Receiver
DPI	Display Parallel Interface
DRD	Dual-Role Device
DSI	Display Serial Interface
DSITX	Display Serial Interface transmitter
E2E	Engineer to Engineer
ECAP	Enhanced Capture
ECC	Error-Correcting Code
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EPWM	Enhanced Pulse-Width Modulator
EQEP	Enhanced Quadrature Encoder Pulse
FAQ	Frequently Asked Question
GEMAC	Gigabit Ethernet Media Access Controller
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High-Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
JTAG	Joint Test Action Group
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
MAC	Media Access Controller
MCASP	Multichannel Audio Serial Ports
MCSPI	Multichannel Serial Peripheral Interfaces
MCU	Micro Controller Unit
MMC	Multi-Media Card
MSL	Moisture Sensitivity Level

OLDI - SL	Open LVDS Display Interface - Single Link
OLDI - DL	Open LVDS Display Interface - Dual Link
OPP	Operating Performance Point
OSPI	Octal Serial Peripheral Interface
OTP	One-Time Programmable
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select Input
TRM	Technical Reference Manual
TRSTn	Test Reset
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCA	Via Channel Array
WKUP	Wakeup
XDS	eXtended Development System

16 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 1, 2023 to August 6, 2024 (from Revision * (December 2023) to Revision A (August 2024)) **Page**

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