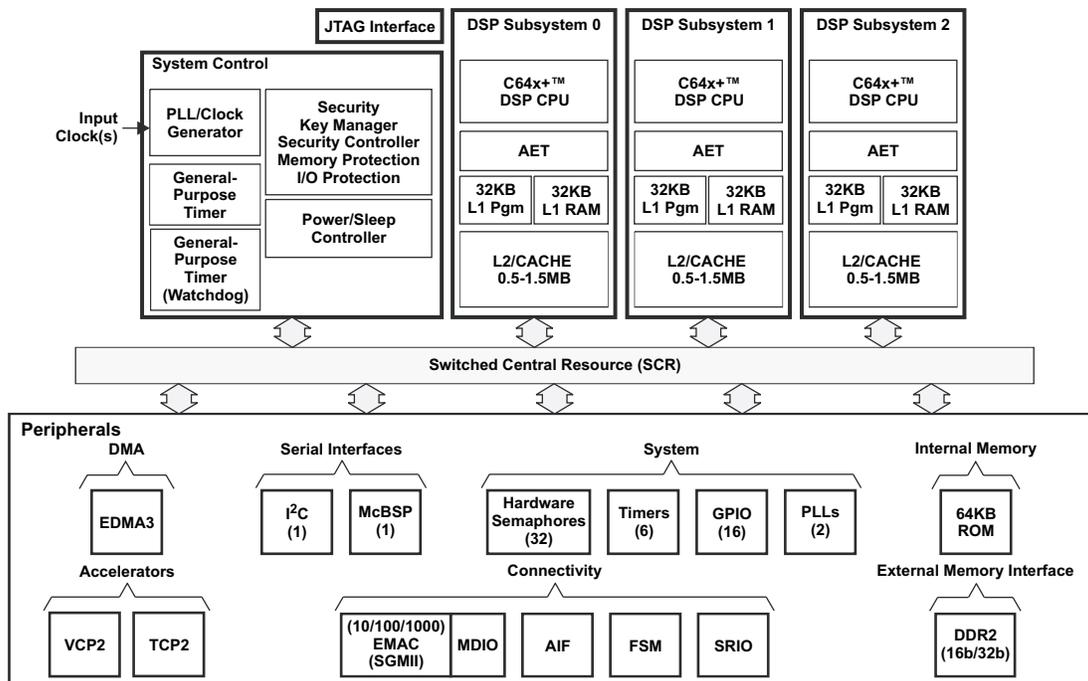# 1 Key Message

The TMS320C6474 DSP integrates three 1-GHz C64x+ DSP CPU cores, a host of high-speed peripherals, and large amounts of internal memory in a compact 23 mm by 23 mm package. These features allow the C6474 device to provide significant performance integration and high-performance density, along with substantial efficiencies in power, cost, and board space.

1.1 Key Features

- **High-Performance Multicore DSP (C6474)**
  - **1-ns Instruction Cycle Time**
  - **1.0-GHz Clock Rate**
  - **Eight 32-Bit Instructions/Cycle**
  - **Commercial Temperature 0°C to 100°C**
- **3 TMS320C64x+™ DSP Cores**
  - **Dedicated SPLOOP Instructions**
  - **Compact Instructions (16-Bit)**
  - **Exception Handling**
- **TMS320C64x+ Megamodule L1/L2 Memory Architecture**
  - **256 K-Bit (32 K-Byte) L1P Program Cache [Direct Mapped]**

- **256 K-Bit (32 K-Byte) L1D Data Cache [2-Way Set-Associative]**
  - **24 M-Bit (3072 K-Byte) Total L2 Unified Mapped RAM/Cache [Flexible Allocation]**
    - **Configurable at boot-time to 1 MB/ 1 MB/1 MB or 1.5 MB/1 MB/0.5 MB**
  - **512 K-Bit (64 K-Byte) L3 ROM**
- **561-Pin Ball Grid Array (BGA) Packages (CUN, GUN, or ZUN Suffix), 0.8-mm Ball Pitch**
- **SmartReflex™ Class 0 Enabled - 0.9-V to 1.2-V Adaptive Core Voltage**
- **Applications: Range from Communications Infrastructure/Basestations to Medical/High-Performance Imaging and Military/Aerospace/Avionics**

1.2 Functional Block Diagram

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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2   Peripherals

Table 2-1. Peripheral Description

PERIPHERALS	NO.	DESCRIPTION
EMIF DDR2 Controller	1	32-bit or 16-bit DDR2-667 with 512MB address space.
Enhanced DMA 3.0 [EDMA3]	1	64 independent channels, 8 Quick DMA (QDMA) channels, 6 transfer controllers. Programmable burst size.
10/100/1000 Ethernet MAC [EMAC] with Management Data I/O [MDIO]	1	SGMII interface. IEEE 802.3 compliant.
Serial RapidIO® [SRIO]	1	Two 1x links. Conforms to *RapidIO® Interconnect Specification, Part VI: Physical Layer 1x/4x LP-Serial Specification, Revision 1.2*.
Viterbi Decoder Coprocessor [VCP2]	1	Significantly speeds up channel-decoding operations on-chip. Flexible polynomials, can generate hard or soft decisions.
Turbo Decoder Coprocessor [TCP2]	1	Implements Max*-Log-MAP, Max-Log-MAP algorithms. Supports requirements of Third-Generation Partnership Projects (3GPP).
Antenna Interface [AIF]	1	Six lanes of high-speed differential serial interface to system devices including other processors and/or antenna modules.
Frame Synchronization Module [FSM]	1	Contains multiple timer/counters generates system timing references for AIF and related EDMA3 synchronization.
Multichannel Buffered Serial Port [McBSP]	2	Compatible with multiple industry standards. FIFO buffer for transmit/receive. Multichannel mode handles 128 channels.
I2C Interface	1	With master/slave operation that supports up to 400 Kbps.
Hardware Semaphores	1	Implements 32 independent general-purpose semaphore resources.
General-Purpose Timers	6	64-bit general-purpose timers, each also configurable as 2 separate 32-bit timers, or as a watchdog timer.
General-Purpose Input/Output [GPIO] Port	1	Up to 16 general-purpose input/output pins.
PLL Clock Generators	2	PLL1 supplies clocks to device logic other than DDR2 controller, PLL2 supplies clocks to DDR2 controller.

3 Key Electrical Characteristics

		MIN	NOM	MAX	UNIT
CV_{DD}	Supply core voltage (scalable)	$CV_{DD} - (0.03CV_{DD})$	0.9 - 1.2	$CV_{DD} + (0.03CV_{DD})$	V
DV_{DD11}	1.1-V supply core I/O voltage	1.045	1.1	1.155	V
DV_{DD18}	1.8-V supply I/O voltage	1.71	1.8	1.89	V
$V_{REFSSTL}$	DDR2 reference voltage	$0.49 * DV_{DD18}$	$0.5 * DV_{DD18}$	$0.51 * DV_{DD18}$	V
AIF_V_{DDA11}	AIF SERDES analog supply	1.045	1.1	1.155	V
AIF_V_{DDD11}	AIF SERDES digital supply	1.045	1.1	1.155	V
AIF_V_{DDR18}	AIF SERDES regulator supply	1.71	1.8	1.89	V
AIF_V_{DDT11}	AIF SERDES termination supply	1.045	1.1	1.155	V
SGR_V_{DDA11}	SRIO/SGMII SERDES analog supply	1.045	1.1	1.155	V
SGR_V_{DDD11}	SRIO/SGMII SERDES digital supply	1.045	1.1	1.155	V
SGR_V_{DDR18}	SRIO/SGMII SERDES regulator supply	1.71	1.8	1.89	V
SGR_V_{DDT11}	SRIO/SGMII SERDES termination supply	1.045	1.1	1.155	V
AV_{DD118}	PLL1 analog supply	1.71	1.8	1.89	V
AV_{DD218}	PLL2 analog supply	1.71	1.8	1.89	V
V_{SS}	Ground	0	0	0	V
P_{Tot}	Total Power Consumption. Includes static and active power for both Core and I/O supplies	Use Case 1: DSP CPU operating at 1 GHz.	6		W
T_C	Operating case temperature range	0		100	°C
F_{CPU}	DSP Operating Frequency	0		1000	MHz

3.1 Power Use Case Details

- **Use Case 1:** At 70°C, 1-GHz CPU frequency, 75% CPU usage, 50% 32-bit DDR2 usage at 667 MHz, 100% usage of both McBSPs, 75% usage of six timers, and 50% usage of both lanes of SRIO. The actual current draw varies across manufacturing processes and is highly application dependent.

4 Tools and Software Support

The C6474 device is supported by the following tools and software:

- Code Composer Studio™ 3.3
- DSP/BIOS™ 5.3
- DSP/BIOS™ 5.3-based Peripheral Device Drivers
- DSP Chip Support Library (CSL)
- TMS320C6474 Evaluation Module (EVM)

TMS320C6474 Multicore Digital Signal Processor
Technical Brief
SPRT489−OCTOBER 2008

TEXAS
INSTRUMENTS

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5   Mechanical Drawing

CUN (S−PBGA−N561)   PLASTIC BALL GRID ARRAY
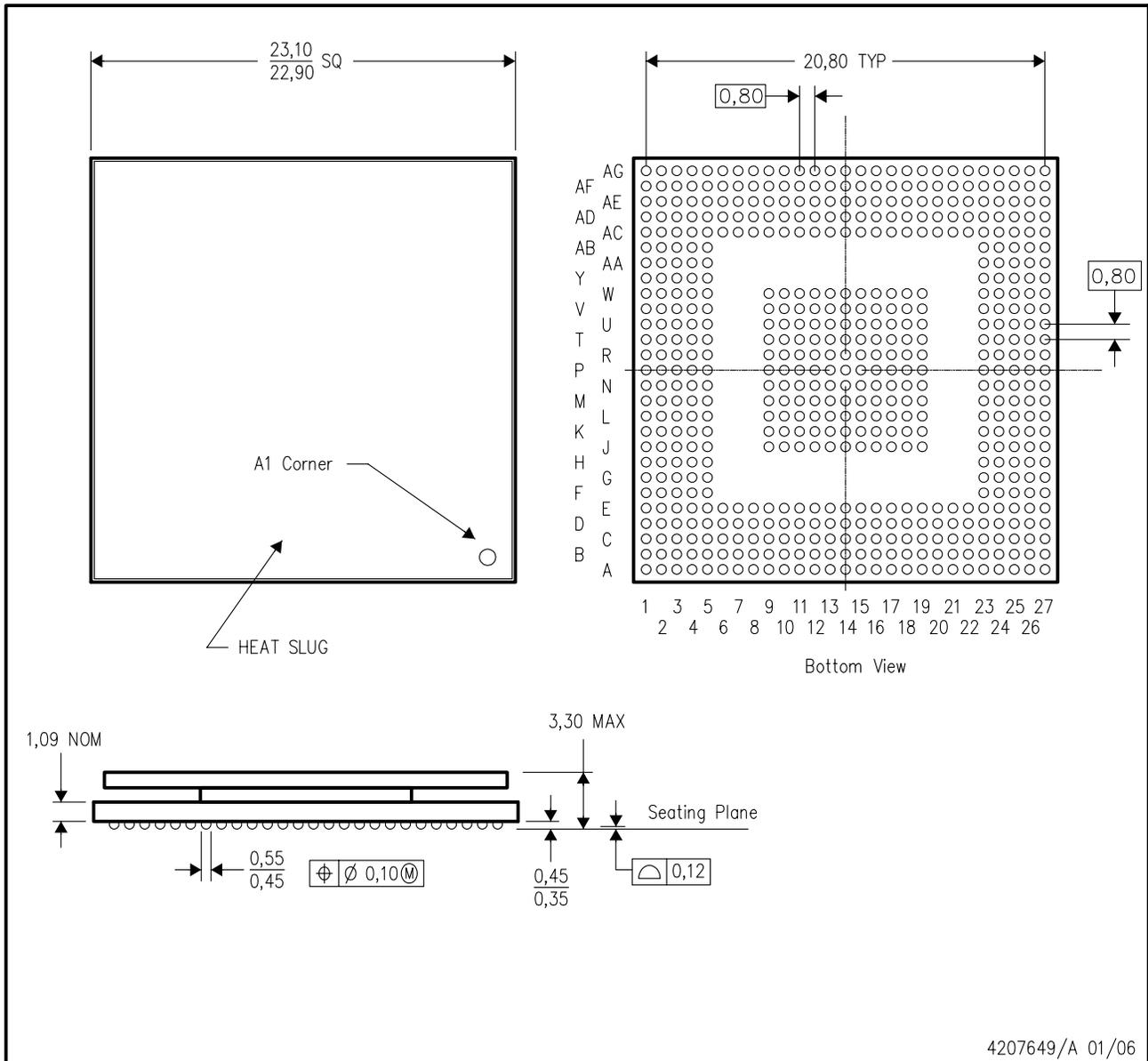
Bottom View

4207649/A 01/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Thermally enhanced plastic package with heat slug (HSL).
         D.   Flip chip application only.
         E.   Lead−free die bump and solder ball.

GUN (S−PBGA−N561)   PLASTIC BALL GRID ARRAY
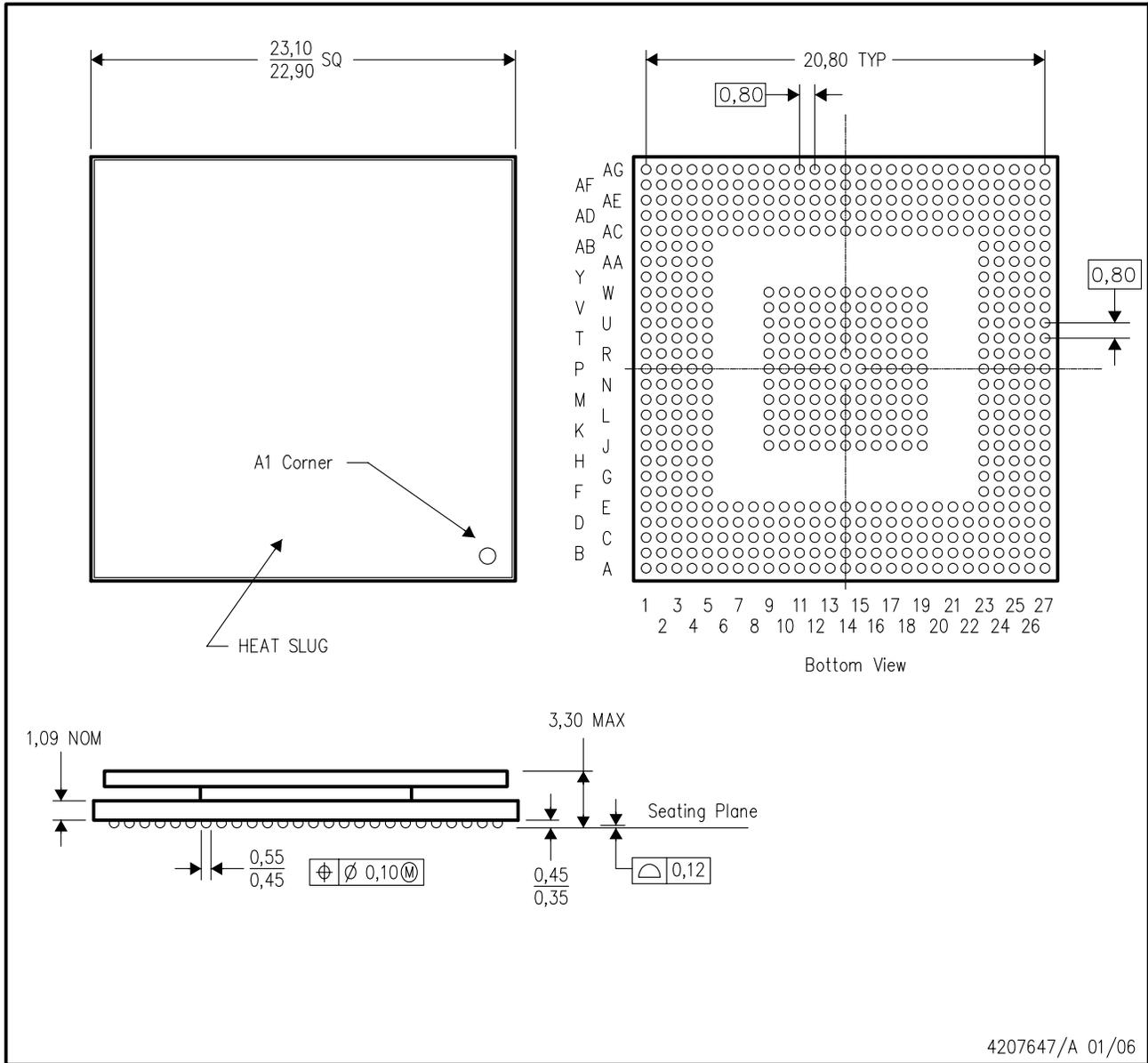
$\frac{23,10}{22,90}$ SQ

20,80 TYP

0,80

0,80

A1 Corner

HEAT SLUG

AG AF AE AD AC AB AA Y W V U T R P N M L K J H G F E D C B A

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

Bottom View

1,09 NOM

3,30 MAX

Seating Plane

$\frac{0,55}{0,45}$ ⊕ ∅ 0,10 Ⓜ

$\frac{0,45}{0,35}$ ◺ 0,12

4207647/A 01/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Thermally enhanced plastic package with heat slug (HSL).
         D.   Flip chip application only.
         E.   Leaded (Pb) solder balls.

ZUN (S−PBGA−N561)   PLASTIC BALL GRID ARRAY
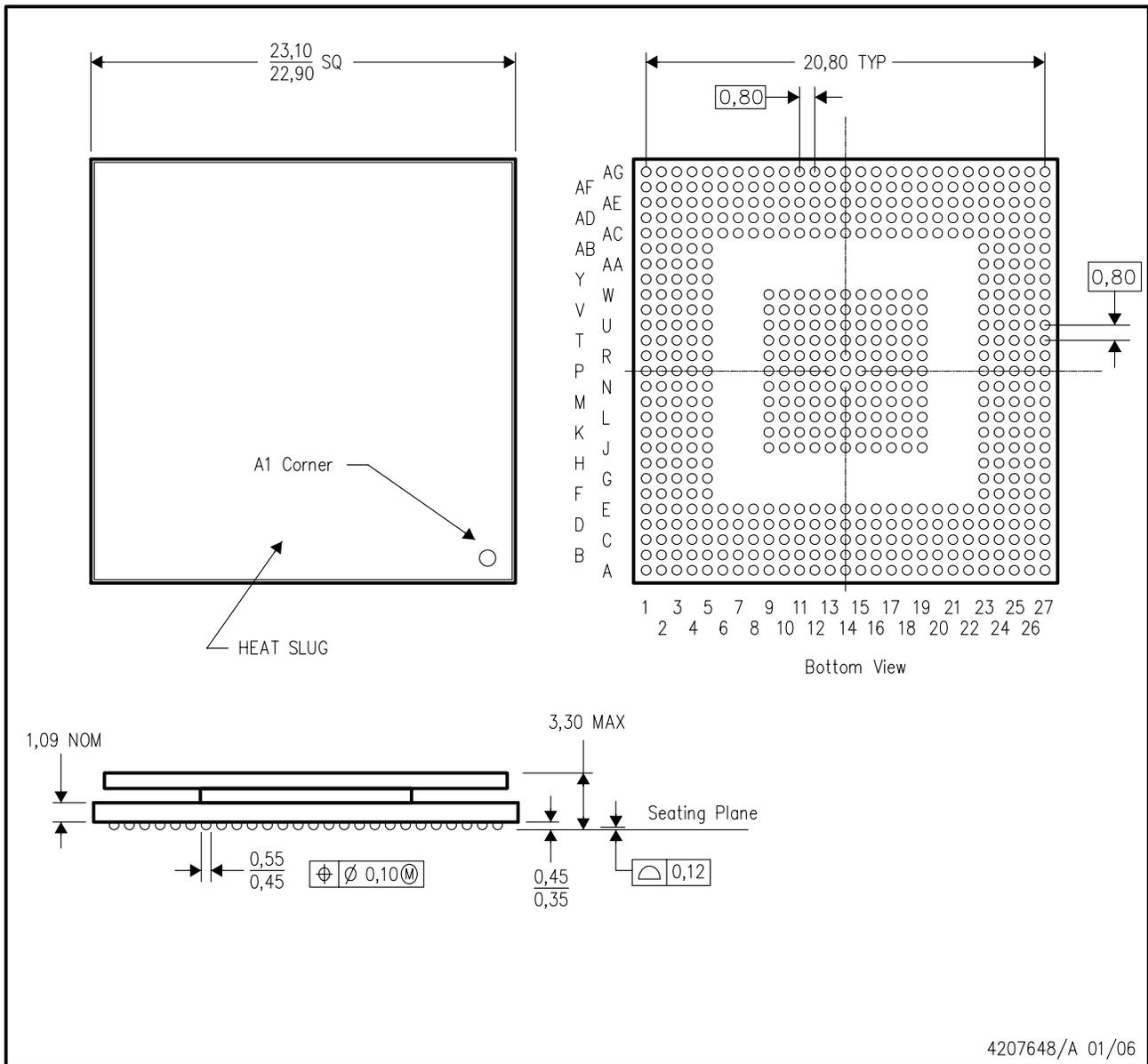
23,10 / 22,90 SQ

20,80 TYP

0,80

0,80

AG AF AE AD AC AB AA Y W V U T R P N M L K J H G F E D C B A

A1 Corner

HEAT SLUG

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

Bottom View

1,09 NOM

3,30 MAX

Seating Plane

0,55 / 0,45

⊕ Ø 0,10 Ⓜ

0,45 / 0,35

⌒ 0,12

4207648/A 01/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Thermally enhanced plastic package with heat slug (HSL).
         D.   Flip chip application only.
         E.   This package is lead−free.
         F.   This package has lead-free solder balls and leaded (Pb) die bumps.

IMPORTANT NOTICE