

# **TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller**

## **User's Guide**



Literature Number: SPRUFH5B  
March 2009–Revised April 2010



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## Read This First

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This document describes the Multimedia Card (MMC)/Secure Digital (SC) (SDIO) Card Controller on the TMS320DM36x Digital Media System-on-Chip (DMSoC).

### Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

### Related Documentation from Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at [www.ti.com](http://www.ti.com).

**[SPRUFG5](#) — TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide** This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

**[SPRUFG8](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide** This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

**[SPRUFG9](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide** This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

**[SPRUFH0](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

**[SPRUFH1](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide** This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

**[SPRUFH2](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

- [SPRUFH3](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.
- [SPRUFH5](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUFH6](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUFH7](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUFH8](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.
- [SPRUFH9](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.
- [SPRUF10](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.
- [SPRUF11](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.
- [SPRUF12](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.
- [SPRUF13](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.
- [SPRUF14](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUF15](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide** This document describes the operation of the ethernet media access controller interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).



- [SPRUF17](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUF18](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUF19](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.
- [SPRUFJ0](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).
- [SPRUGG8](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Face Detection User's Guide*** This document describes the face detection capabilities for the TMS320DM36x Digital Media System-on-Chip (DMSoC).

# **Multimedia Card (MMC)/Secure Digital (SD) Card Controller**

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## **1 Introduction**

This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

### **1.1 Purpose of the Peripheral**

The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards. The communication between the MMC/SD card controller and MMC/SD card(s) is performed according to the MMC/SD protocol.

### **1.2 Features**

The MMC/SD card controller has the following features:

- Supports interface to multimedia cards (MMC)
- Supports interface to secure digital (SD) memory cards
- Supports the use of both MMC/SD and SDIO protocols.
- Programmable frequency of the clock that controls the timing of transfers between the MMC/SD controller and memory card
- 512-bit read/write FIFO to lower system overhead
- Signaling to support enhanced direct memory access (EDMA) transfers (slave)
- Supports a max clock rate of 50 MHz for SD cards (spec. ver. 2.0 ).

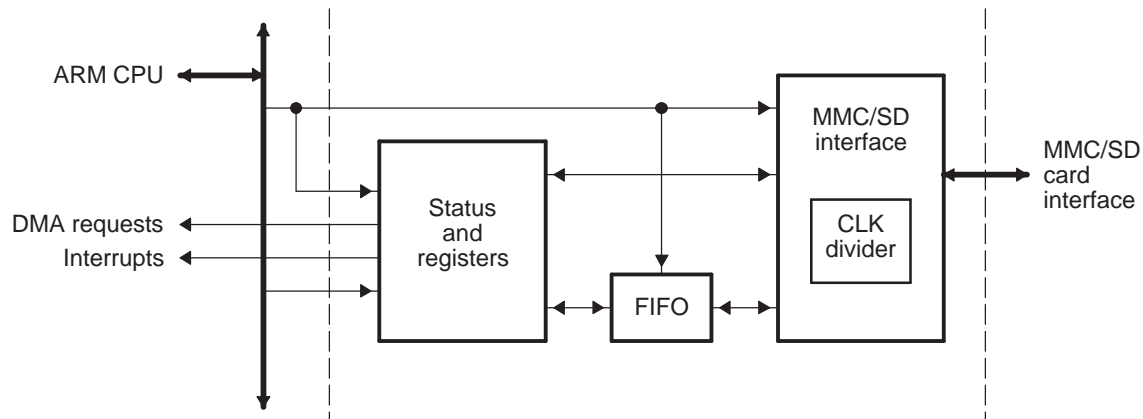
### **1.3 Functional Block Diagram**

The MMC/SD card controller transfers data between the ARM and EDMA controller on one side and MMC/SD card on the other side, as shown in [Figure 1](#). The ARM and EDMA controller can read/write the data in the card by accessing the registers in the MMC/SD controller.

### **1.4 Supported Use Case Statement**

The MMC/SD card controller supports the following user cases:

- MMC/SD card identification
- MMC/SD single-block read using CPU
- MMC/SD single-block read using EDMA
- MMC/SD single-block write using CPU
- MMC/SD single-block write using EDMA
- MMC/SD multiple-block read using CPU
- MMC/SD multiple-block read using EDMA
- MMC/SD multiple-block write using CPU
- MMC/SD multiple-block write using EDMA
- SDIO function

**Figure 1. MMC/SD Card Controller Block Diagram**


### 1.5 Industry Standard(s) Compliance Statement

The MMC/SD card controller will support the following industry standards (with the exception noted below):

- Multimedia Card (MMC) Specification V3.31
- Secure Digital (SD) Physical Layer Specification V1.1
- Secure Digital Input Output (SDIO) Specification V2.0

The information in this document assumes the reader is familiar with these standards.

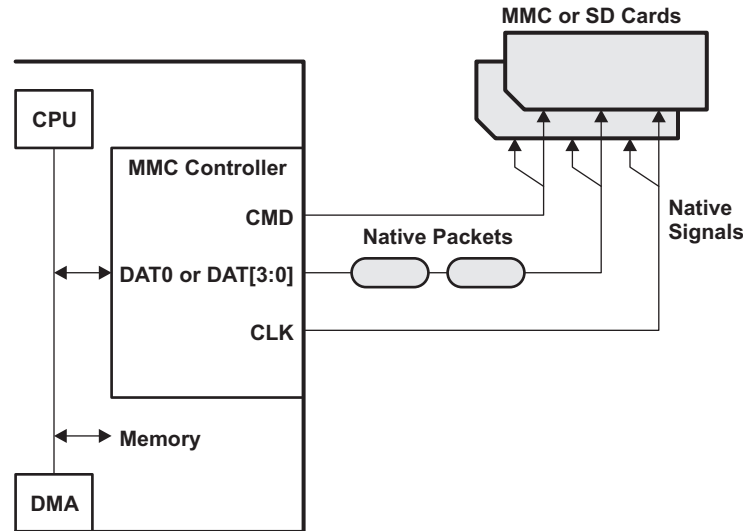
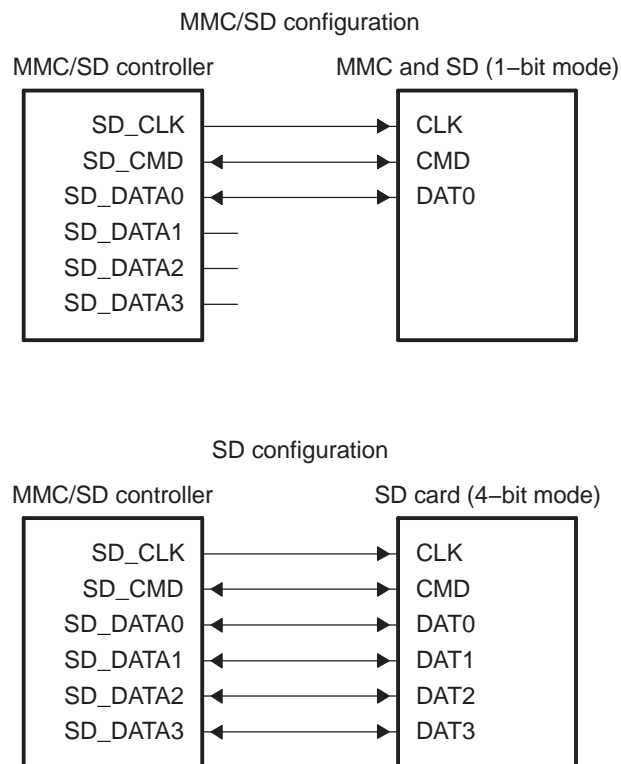
The MMC/SD controller does not support the SPI mode of operation.

## 2 Peripheral Architecture

The MMC/SD controller uses the MMC/SD protocol to communicate with the MMC/SD cards. The MMC/SD controller can be configured to work as an MMC or SD controller, based on the type of card with which the controller is communicating. [Figure 2](#) summarizes the MMC/SD mode interface. [Figure 3](#) illustrates how the controller is interfaced to the cards in MMC/SD mode.

In the MMC/SD mode, the controller supports one or more MMC/SD cards. When multiple cards are connected, the MMC/SD controller selects one by using identification broadcast on the data line. The following MMC/SD controller pins are used:

- **CMD:** This pin is used for two-way communication between the connected card and the MMC/SD controller. The MMC/SD controller transmits commands to the card and the memory card drives responses to the commands on this pin.
- **DAT0 or DAT0-3:** MMC cards use only one data line (DAT0) and SD cards use one or four data lines. The number of DAT pins (the data bus width) is set by the WIDTH bit in the MMC control register (MMCCTL, see ).
- **CLK:** This pin provides the clock to the memory card from the MMC/SD controller.

**Figure 2. MMC/SD Controller Interface Diagram**

**Figure 3. MMC Configuration and SD Configuration Diagram**


## 2.1 Clock Control

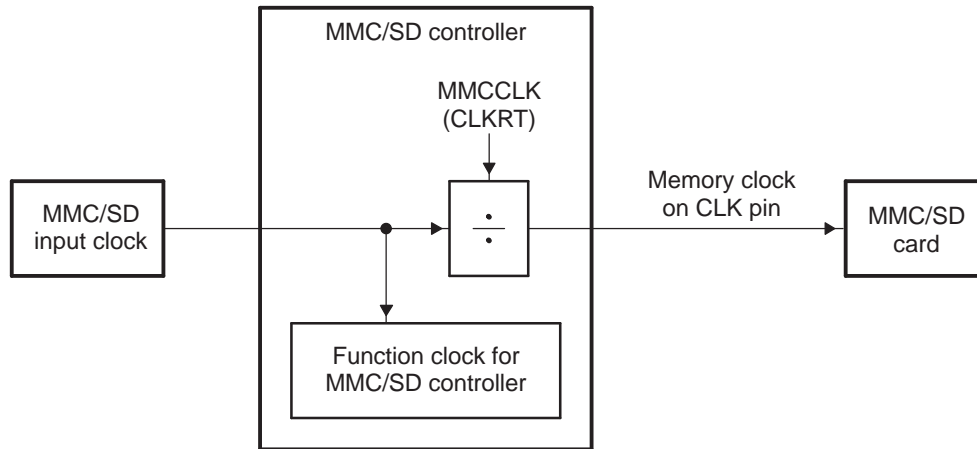
The MMC/SD controller has two clocks, the function clock and the memory clock (Figure 4).

The function clock determines the operational frequency of the MMC/SD controller and is the input clock to the MMC/SD controller on the device. The MMC/SD controller is capable of operating with a function clock up to 100 MHz.

The memory clock appears on the SD\_CLK pin of the MMC/SD controller interface. The memory clock controls the timing of communication between the MMC/SD controller and the connected memory card. The memory clock is generated by dividing the function clock in the MMC/SD controller. The divide-down value is set by CLKRT bits in the MMC memory clock control register (MMCCLK) and is determined by the equation:

$$\text{memory clock frequency} = \text{function clock frequency} / (2 \times (\text{CLKRT} + 1))$$

**Figure 4. MMC/SD Controller Clocking Diagram**



- (1) Maximum memory clock frequency for MMC card can be 20 MHz.
- (2) Maximum memory clock frequency for SD card can be 50 MHz.

## 2.2 Signal Descriptions

Table 1 shows the MMC/SD controller pins used in each mode. The MMC/SD protocol uses the clock, command (two-way communication between the MMC controller and memory card), and data ( DATA0 for MMC card, DATA0-3 for SD card) pins.

**Table 1. MMC/SD Controller Pins Used in Each Mode**

Pin	Type <sup>(1)</sup>	Function	
		MMC Communications	SD Communications
MMCS Dx_CLK	O	Clock line	Clock line
MMCS Dx_CMD	I/O	Command line	Command line
MMCS Dx_DAT0	I/O	Data line 0	Data line 0
MMCS Dx_DAT1	I/O	Not used	Data line 1
MMCS Dx_DAT2	I/O	Not used	Data line 2
MMCS Dx_DAT3	I/O	Not used	Data line 3

<sup>(1)</sup> I = input to the MMC/SD controller; O = output from the MMC/SD controller.

## 2.3 Protocol Descriptions

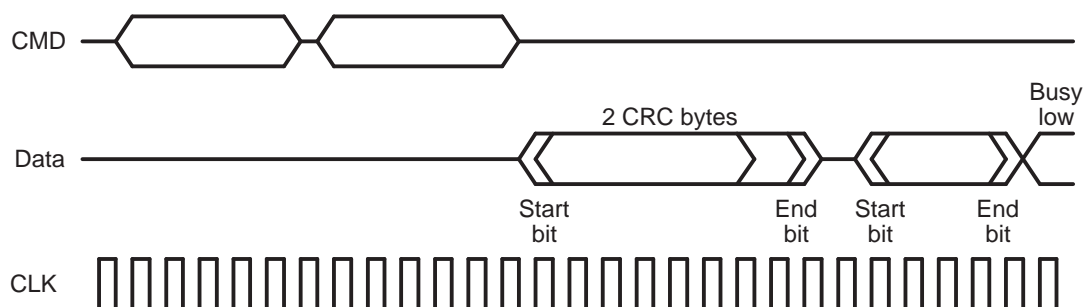
The MMC/SD controller follows the MMC/SD protocol for completing any kind of transaction with the multimedia card and secure digital cards. For detailed information, refer to the supported MMC and SD specifications in [Section 1.5](#).

### 2.3.1 MMC/SD Mode Write Sequence

[Figure 5](#) and [Table 2](#) show the signal activity when the MMC/SD controller is in the MMC/SD mode and is writing data to a memory card. Before initiating a write transfer ensure that the block length definition in the MMC/SD controller and the memory card is identical.

- The MMC/SD controller sends a write command to the card.
- The card receives the command and sends responses to the command.
- The MMC/SD controller sends a block of data to the card.
- The card sends the CRC status to the MMC/SD controller.
- The card sends a low BUSY bit until all the data has been programmed into the flash memory inside the card.

**Figure 5. MMC/SD Mode Write Sequence Timing Diagram**



**Table 2. MMC/SD Mode Write Sequence**

Portion of the Sequence	Description
WR CMD	Write command: A 6-byte WRITE_BLOCK command token is sent from the ARM to the card.
CMD RSP	Command response: The card sends a 6-byte response of type R1 to acknowledge the WRITE_BLOCK to the ARM.
DAT BLK	Data block: The ARM writes a block of data to the card. The data content is preceded by one start bit and is followed by two CRC bytes and one end bit.
CRC STAT	CRC status: The card sends a one byte CRC status information, which indicates to the ARM whether the data has been accepted by the card or rejected due to a CRC error. The CRC status information is preceded by one start bit and is followed by one end bit.
BSY	BUSY bit: The CRC status information is followed by a continuous stream of low busy bits until all of the data has been programmed into the flash memory on the card.

### 2.3.2 MMC/SD Mode Read Sequence

Figure 6 and Table 3 show the signal activity when the MMC controller is in the MMC/SD mode and is reading data from a memory card. Before initiating a read transfer, ensure that the block length definition in the MMC/SD controller and the memory card is identical. In a successful read sequence, the following steps occur:

- The MMC/SD controller sends a read command to the card.
- The card drives responses to the command.
- The card sends a block of data to the ARM.

Figure 6. MMC/SD Mode Read Sequence Timing Diagram

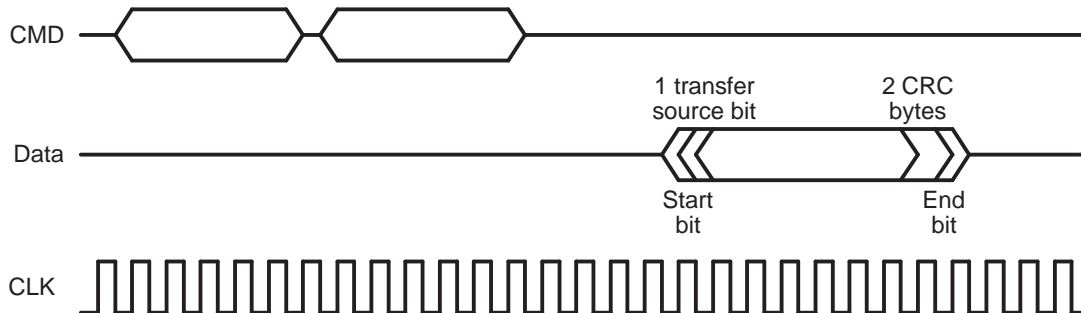


Table 3. MMC/SD Mode Read Sequence

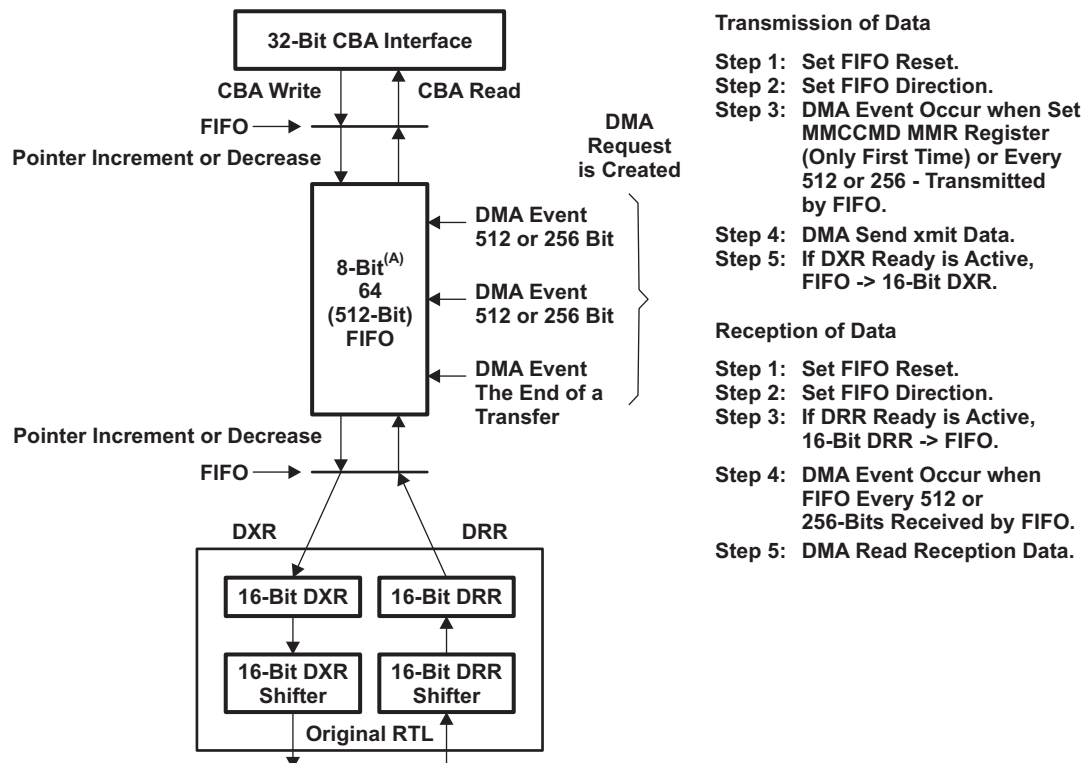
Portion of the Sequence	Description
RD CMD	Read command: A 6-byte READ_SINGLE_BLOCK command token is sent from the ARM to the card.
CMD RSP	Command response: The card sends a response of type R1 to acknowledge the READ_SINGLE_BLOCK command to the ARM.
DAT BLK	Data block: The card sends a block of data to the ARM. The data content is preceded by a start bit and is followed by two CRC byte and an end bit.

## 2.4 Data Flow in the Input/Output FIFO

The MMC/SD controller contains a single 512-bit FIFO that is used for both reading data from the memory card and writing data to the memory card (see Figure 7). The FIFO is organized as 64 eight-bit entries. The conversion from the 32-bit bus to the byte format of the FIFO follows the little-endian convention (details are provided in later sections). The FIFO includes logic to generate EDMA events and interrupts based on the amount of data available in the FIFO. FIFO depth (threshold) is a programmable number that describes how many bytes can be received/transmitted at a time. There are also flags set when the FIFO is full or empty. A high-level operational description is:

- Data is written to the FIFO through the MMC data transmit register (MMCDXR). Data is read from the FIFO through the MMC data receive register (MMCDRR).
- The ACCWD bits in the MMC FIFO control register (MMCFIFOCTL) determines the behavior of the FIFO full (FIFOFUL) and FIFO empty (FIFOEMP) status flags in the MMC status register 1 (MMCST1):
  - If ACCWD = 00b:
    - FIFO full is active when the write pointer + 4 > read pointer
    - FIFO empty is active when the write pointer - 4 < read pointer
  - If ACCWD = 01b:
    - FIFO full is active when the write pointer + 3 > read pointer
    - FIFO empty is active when the write pointer - 3 < read pointer
  - If ACCWD = 10b:
    - FIFO full is active when the write pointer + 2 > read pointer
    - FIFO empty is active when the write pointer - 2 < read pointer
  - If ACCWD = 11b:
    - FIFO full is active when the write pointer + 1 > read pointer
    - FIFO empty is active when the write pointer - 1 < read pointer

**Figure 7. FIFO Operation Diagram**

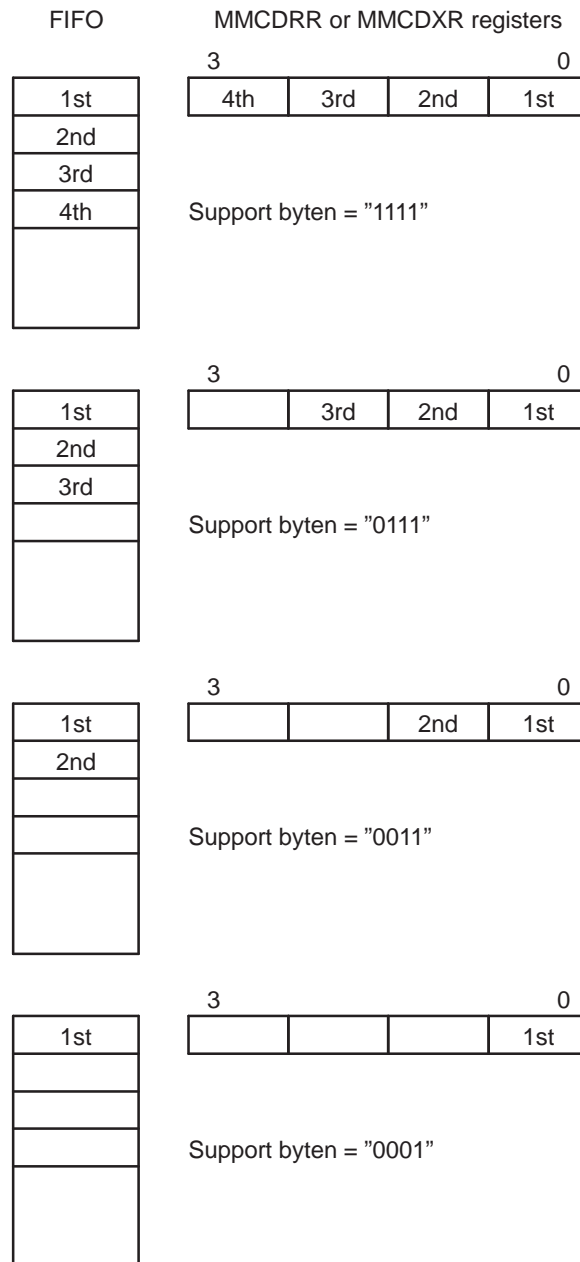


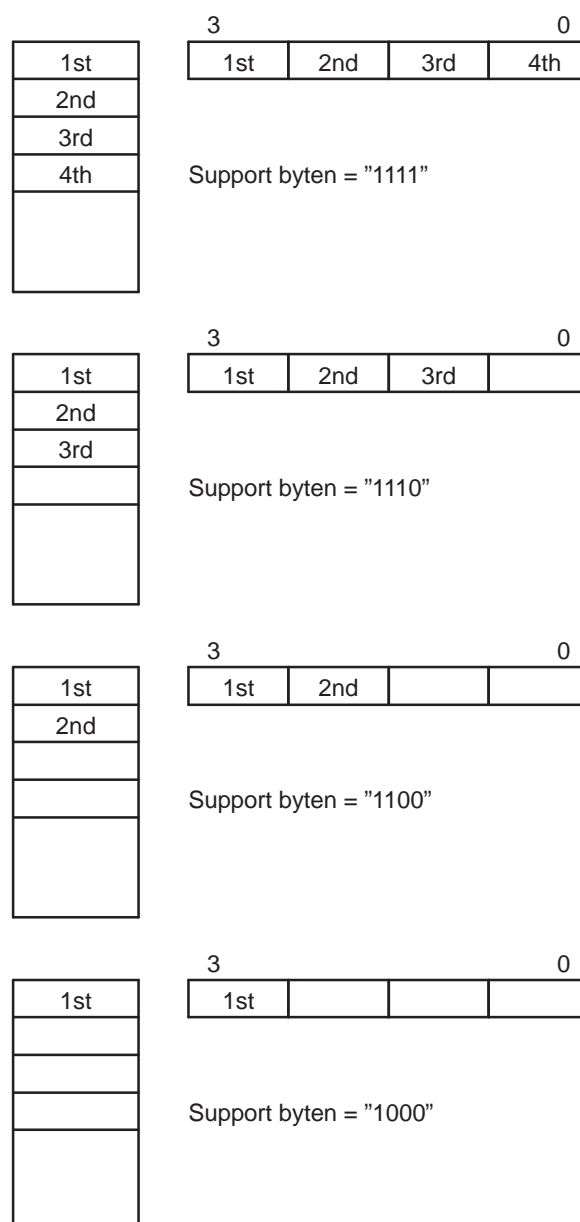


## 2.5 Data Flow in the Data Registers (MMCDRR and MMCDXR)

The ARM or EDMA controller can read 32 bits at a time from the FIFO by reading the MMC data receive register (MMCDRR) and write 32 bits at a time to the FIFO by writing to the MMC data transmit register (MMCDXR). However, since the memory card is an 8-bit device, it transmits or receives one byte at a time. Figure 8 and Figure 9 show how the data-size difference is handled by the data registers.

**Figure 8. Little-Endian Access to MMCDXR/MMCDRR from the ARM CPU or the EDMA**



**Figure 9. Big-Endian Access to MMCDXR/MMCDRR from the ARM CPU or the EDMA**


## 2.6 FIFO Operation During Card Read Operation

### 2.6.1 EDMA Reads

The FIFO controller manages the activities of reading the data in from the card and issuing EDMA read events. Each time an EDMA read event is issued, an EDMA read request interrupt is also generated.

[Figure 10](#) provides details of the FIFO controllers operation. As data is received from the card, it is read into the FIFO. When the number of bytes of data received is equal to the level set by the FIFOLEV bits in MMCFIFOCTL, an EDMA read event is issued and new EDMA events are disabled. Data is read from the FIFO by way of MMCDRR. The FIFO controller continues to read in data from the card while checking for the EDMA event to occur or the FIFO to become full. Once the EDMA event finishes, new EDMA events are enabled. If the FIFO fills up, the FIFO controller stops the MMC/SD controller from reading anymore data until the FIFO is no longer full.

An EDMA read event is also generated when the last data arrives as determined by the MMC block length register (MMCBLEN) and the MMC number of blocks register (MMCNBLK) settings. This EDMA event enables the FIFO to be flushed of all the data that was read from the card.

Each time an EDMA read event is generated, an interrupt (DRRDYINT) is generated and the DRRDY bit in the MMC status register 0 (MMCST0) is also set.

## 2.6.2 CPU Reads

The system CPU can also directly read the card data by reading the MMC data receive register (MMCDRR). The MMC/SD controller supports reads that are 1, 2, 3, or 4 bytes wide as shown in [Figure 8](#) and [Figure 9](#).

## 2.7 FIFO Operation During Card Write Operation

### 2.7.1 EDMA Writes

The FIFO controller manages the activities of accepting data from the ARM or EDMA and passing the data to the MMC/SD controller. The FIFO controller issues EDMA write events as appropriate. Each time an EDMA write event is issued, an EDMA write request interrupt is also generated. Data is written into the FIFO through MMCDXR.

[Figure 11](#) provides details of the FIFO controller's operation. Data is written by the ARM or EDMA to the FIFO by the way of MMCDXR. The FIFO then passes the data to the MMC/SD controller which manages to write the data to the card. When the number of bytes of data in the FIFO is less than the level set by the FIFOLEV bits in MMCFIFOCTL, an EDMA write event is issued and new EDMA events are disabled. The FIFO controller continues to transfer data to the MMC/SD controller while checking for the EDMA event to finish or the FIFO to become empty. Once the EDMA event finishes, new EDMA events are enabled. If the FIFO becomes empty, the FIFO controller informs the MMC/SD controller.

Each time an EDMA write event is generated, an interrupt (DXRDYINT) is generated and the DXRDY bit in the MMC status register 0 (MMCST0) is also set.

### 2.7.2 CPU Writes

The system CPU can also directly write the card data by writing the MMC data transmit register (MMCDXR). The MMC/SD controller will support writes that are 1, 2, 3, or 4 bytes wide as shown in [Figure 8](#) and [Figure 9](#).

Figure 10. FIFO Operation During Card Read Diagram

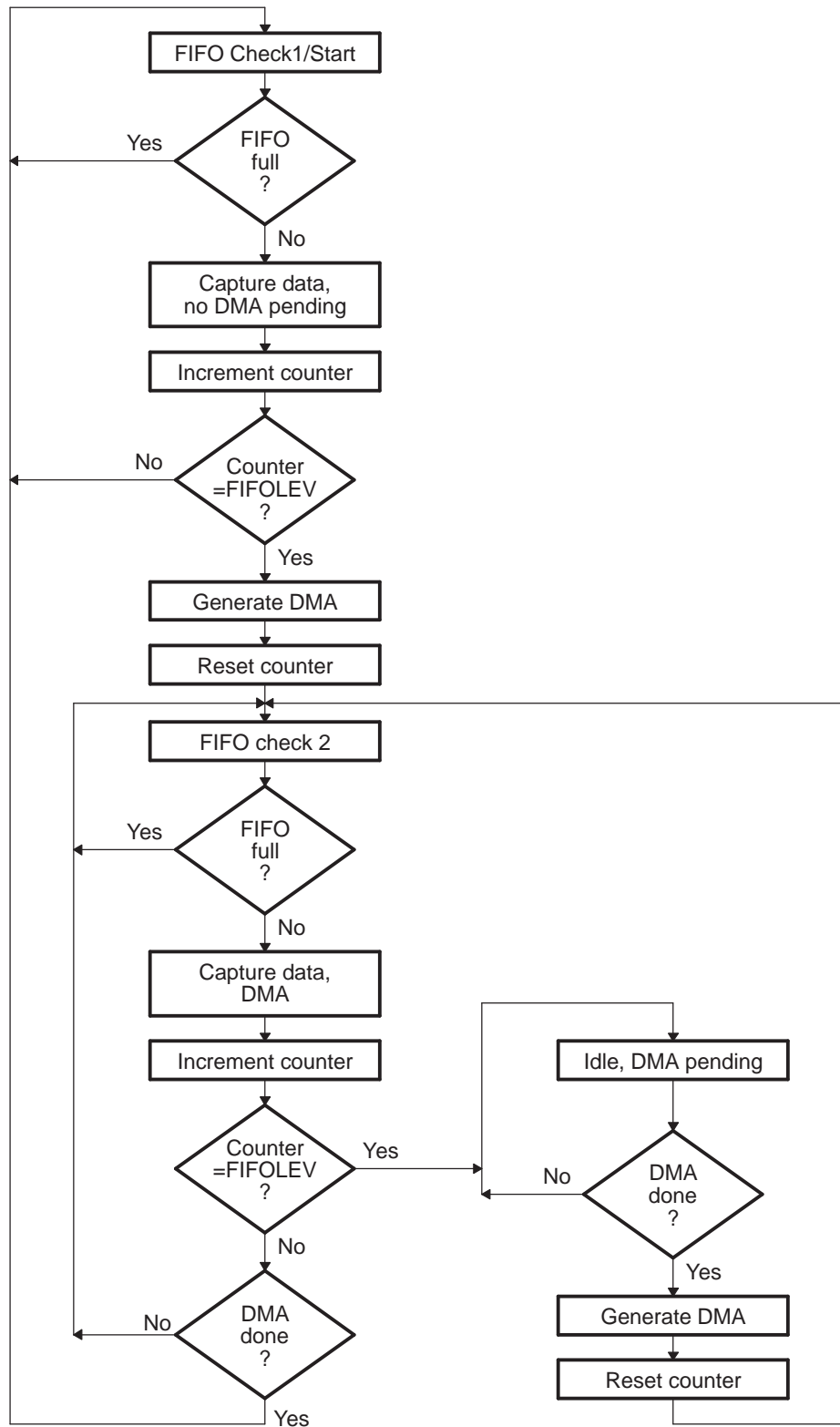
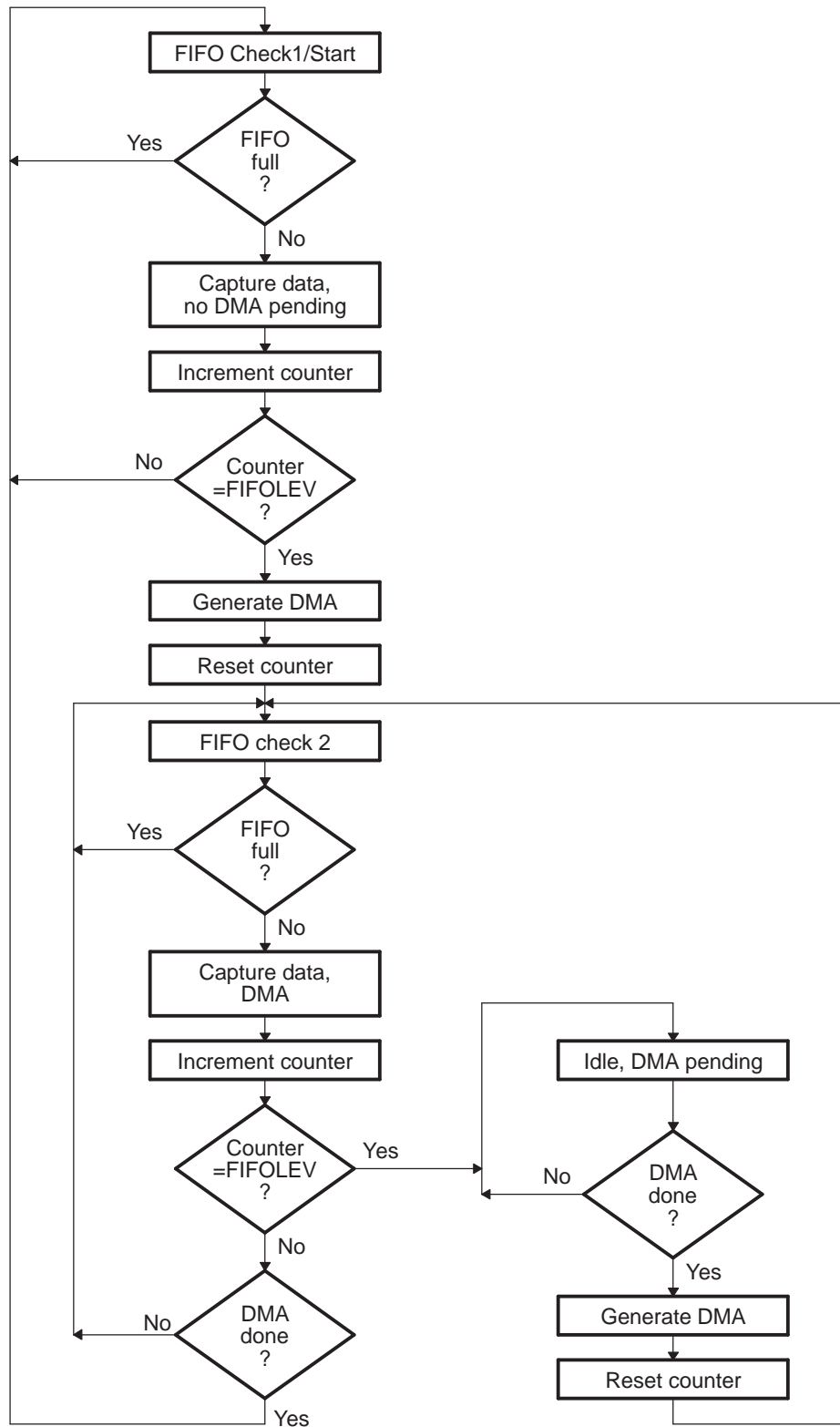


Figure 11. FIFO Operation During Card Write Diagram



## 2.8 Reset Considerations

The MMC/SD controller has two reset sources: hardware reset and software reset.

## 2.8.1 Software Reset Considerations

A software reset (such as a reset generated by the emulator) will not cause the MMC/SD controller registers to be altered. After a software reset, the MMC/SD controller continues to operate as it was configured prior to the reset.

## 2.8.2 Hardware Reset Considerations

A hardware reset of the processor will cause the MMC/SD controller registers to return to their default values after reset.

## 2.9 Initialization

### 2.9.1 MMC/SD Mode Initialization

The general procedure for initializing the MMC/SD controller is given in the following steps. Details about the registers or register bit fields to be configured in the MMC/SD mode are in the subsequent subsections.

1. Enable the SD\_CLK pin so that the memory clock is sent to the memory card by setting the CLKEN bit in the MMC memory clock control register (MMCCLK).
2. Place the MMC/SD controller in its reset state by setting the CMDRST bit and DATRST bit in the MMC control register (MMCCTL). After the reset, other bits in MMCCTL can be set.
3. Allow some delay of at least 50 MMC/SD clock cycles in order to allow the internal logic to reset properly.
4. Clear the CMDRST bit and DATRST bit in MMCCTL to release the MMC/SD controller from its reset state. It is recommended not to rewrite the values written to the other bits of MMCCTL in step 1.
5. Write the required values to MMC/SD controller registers to complete the MMC/SD controller configuration.

### 2.9.2 Initializing the MMC Control Register (MMCCTL)

When operating the MMC/SD controller in the MMC/SD mode, the bits in the MMC control register (MMCCTL) affect the operation of the MMC/SD controller. The subsections that follow help you decide how to initialize each of control register bits.

The DATEG bits in MMCCTL enable or disable edge detection on the SD\_DATA3 pin. If edge detection is enabled and an edge is detected, the DATEG flag bit in the MMC status register 0 (MMCST0) is set. In addition, if the EDATED bit in the MMC interrupt mask register (MMCIM) is set, an interrupt request is generated.

In the MMC/SD mode, the MMC/SD controller must know how wide the data bus must be for the memory card that is connected. If an MMC card is connected, specify a 1-bit data bus (WIDTH = 0 in MMCCTL); if an SD card is connected, specify a 4-bit data bus (WIDTH = 1 in MMCCTL).

To place the MMC/SD controller in its reset state and disable it, set the CMDRST bit and DATRST bit in MMCCTL. The first step of the MMC/SD controller initialization process is to disable both sets of logic. When initialization is complete but before you enable the SD\_CLK pin, enable the MMC/SD controller by clearing the CMDRST bit and DATRST bit in MMCCTL.

### 2.9.3 Initializing the Clock Controller Registers (MMCCLK)

A clock divider in the MMC/SD controller divides-down the function clock to produce the memory clock. Load the divide-down value into the CLKRT bits in the MMC memory clock control register (MMCCLK). The divide-down value is determined by the equation:

$$\text{memory clock frequency} = \text{function clock frequency} / (2^{(\text{CLKRT} + 1)})$$

The CLKEN bit in MMCCLK determines whether the memory clock appears on the SD\_CLK pin. If CLKEN is cleared to 0, the memory clock is not provided except when required.

### 2.9.4 Initialize the Interrupt Mask Register (MMCIM)

The bits in the MMC interrupt mask register (MMCIM) individually enable or disable the interrupt requests. To enable the associated interrupt request, set the corresponding bit in MMCIM. To disable the associated interrupt request, clear the corresponding bit. Load zeros into the bits not used in the MMC/SD mode.

### 2.9.5 Initialize the Time-Out Registers (MMCTOR and MMCTOD)

Specify the time-out period for responses using the MMC response time-out register (MMCTOR) and the time-out period for reading data using the MMC data read time-out register (MMCTOD).

When the MMC/SD controller sends a command to a memory card, it often must wait for a response. The MMC/SD controller can wait indefinitely or up to 255 memory clock cycles. If you load 0 into MMCTOR, the MMC/SD controller waits indefinitely for a response. If you load a nonzero value into MMCTOR, the MMC/SD controller stops waiting after the specified number of memory clock cycles and then sets a response time-out flag (TOUTRS) in the MMC status register 0 (MMCST0). If the associated interrupt request is enabled, the MMC/SD controller also sends an interrupt request to the ARM.

When the MMC/SD controller requests data from a memory card, it can wait indefinitely for that data or it can stop waiting after a programmable number of cycles. If you load 0 into MMCTOD, the MMC/SD controller waits indefinitely. If you load a nonzero value into MMCTOD, the MMC/SD controller waits the specified number of memory clock cycles and then sets a read data time-out flag (TOUTRD) in MMCST0. If the associated interrupt request is enabled, the MMC/SD controller also sends an interrupt request to the ARM.

### 2.9.6 Initialize the Data Block Registers (MMCBLEN and MMCNBLK)

Specify the number of bytes in a data block in the MMC block length register (MMCBLEN) and the number of blocks in a multiple-block transfer in the MMC number of blocks register (MMCNBLK).

In MMCBLEN, you must define the size for each block of data transferred between the MMC/SD controller and a memory card. The valid size depends on the type of read/write operations. A length of 0 bytes is prohibited.

For multiple-block transfers, you must specify how many blocks of data are to be transferred between the MMC/SD controller and a memory card. You can specify an infinite number of blocks by loading 0 into MMCNBLK. When MMCNBLK = 0, the MMC/SD controller continues to transfer data blocks until the transferring is stopped with a STOP\_TRANSMISSION command. To transfer a specific number of blocks, load MMCNBLK with a value from 1 to 65 535.

For high capacity cards (2 GB and larger), by default the read/write block length of the card is 1024 bytes. Note that CMD16 (SET\_BLOCK\_LEN) can only set the block length up to 512 bytes even for high capacity cards. Therefore if you want to change the block length of a high capacity card, you are limited to 512 bytes. In this case you should discard the block length read from the CSD register in the card and set the block length up to 512 bytes.

### 2.9.7 Monitoring Activity in the MMC/SD Mode

This section describes registers and specific register bits that you use to obtain the status of the MMC/SD controller in the MMC/SD mode. The status of the MMC/SD controller is determined by reading the bits in the MMC status register 0 (MMCST0) and MMC status register 1 (MMCST1).

#### 2.9.7.1 Detecting Edges on the DAT3 Pin

The MMC/SD controller sets the DATED bit in MMCST0 if SD\_DATA3 edge detection is enabled (DATEG bits are nonzero in MMCCCTL) and the specified edge is detected. The ARM is also notified of the SD\_DATA3 by an interrupt if the interrupt request is enabled (EDATED = 1 in MMCIM).

#### 2.9.7.2 Detecting Level Changes on the DAT3 Pin

The DAT3ST bit in MMCST1 monitors the signal level on the SD\_DATA3 pin.

### 2.9.7.3 Determining Whether New Data is Available in MMCDRR

The MMC/SD controller sets the DRRDY bit in MMCST0 when data in the FIFO is greater than the threshold set in MMCFIFOCTL. The ARM is also notified of the event by an interrupt if the interrupt request is enabled (EDRRDY = 1 in MMCIM). The DRRDY flag is cleared by a read of MMCDRR.

### 2.9.7.4 Verifying that MMCDXR is Ready to Accept New Data

The MMC/SD controller sets the DXRDY bit in MMCST0 when the amount of data in the FIFO is less than the threshold set in MMCFIFOCTL. The ARM is also notified of the event by an interrupt if the interrupt request is enabled (EDXRDY = 1 in MMCIM).

### 2.9.7.5 Checking for CRC Errors

The MMC/SD controller sets the CRCRS, CRCRD, and CRCWR bits in MMCST0 in response to the corresponding CRC errors of command response, data read, and data write. The ARM is also notified of the CRC error by an interrupt if the interrupt request is enabled (ECRCRS/ECRCRD/ECRCWR = 1 in MMCIM).

### 2.9.7.6 Checking for Time-Out Events

The MMC/SD controller sets the TOUTRS and TOUTRD bits in MMCST0 in response to the corresponding command response or data read time-out event. The ARM is also notified of the event by an interrupt if the interrupt request is enabled (ETOUTRS/ETOUTRD = 1 in MMCIM).

### 2.9.7.7 Determining When a Response/Command is Done

The MMC/SD controller sets the RSPDNE bit in MMCST0 when the response is done or, in the case of commands that do not require a response, when the command is done. The ARM is also notified of the done condition by an interrupt if the interrupt request is enabled. (ERSPDNE = 1 in MMCIM).

### 2.9.7.8 Determining Whether the Memory Card is Busy

The card sends a busy signal either when waiting for an R1b-type response or when programming the last write data into its flash memory. The MMC/SD controller has two flags to notify you whether the memory card is sending a busy signal. The two flags are complements of each other:

- BSYDNE flag in MMCST0 is set if the card did not send or is not sending a busy signal when the MMC/SD controller is expecting a busy signal (BSYEXP = 1 in MMCCMD). The interrupt by this bit is enabled by a corresponding interrupt enable bit (EBSYDNE = 1 in MMCIM).
- BUSY flag in MMCST1 is set when a busy signal is received from the card.

### 2.9.7.9 Determining Whether a Data Transfer is Done

For read operations, the MMC/SD controller sets the DATDNE bit in the MMCST0 register when it has received data without a CRC error and all data are read out from FIFO. For write operations, the MMC/SD controller sets the DATDNE bit in the MMCST0 register when it has finished sending data. CRC and card programming are complete. The DATDNE bit is polled to determine when to stop writing to the data transmit register (for a write operation) or when to stop reading from the data receive register (for a read operation). The ARM is also notified of the time-out event by an interrupt if the interrupt request is enabled (EDATDNE = 1 in MMCIM).

### 2.9.7.10 Determining When Last Data has Been Written to Card (SanDisk SD cards)

Some SanDisk brand SD™ cards exhibit a behavior that requires a multiple-block write command to be terminated with a STOP (CMD12) command before the data write sequence is completed. To enable support of this function, the transfer done interrupt (TRNDNE) is provided. The TRNDNE interrupt is enabled by setting the ETRNDNE bit in MMCIM. This interrupt is issued when the last byte of data (as defined by MMCNBLK and MMCBLEN) is transferred from the FIFO to the output shift register. The CPU should respond to this interrupt by sending a STOP command to the card. This interrupt differs from DATDNE by timing. DATDNE does not occur until after the CRC and memory programming are completed.



### 2.9.7.11 Checking For a Data Transmit Empty Condition

During transmission, a data value is passed from the MMC data transmit register (MMCDXR) to the data transmit shift register. The data is then passed from the shift register to the memory card one bit at a time. The DXEMP bit in MMCST1 indicates when the shift register is empty.

Typically, the DXEMP bit is not used to control data transfers; rather, it is checked during recovery from an error condition. There is no interrupt associated with the DXEMP bit.

### 2.9.7.12 Checking for a Data Receive Full Condition

During reception, the data receive shift register accepts a data value one bit at a time. The entire value is then passed from the shift register to the MMC data receive register (MMCDRR). The DRFUL bit in MMCST1 indicates when the shift register is full; no new bits can be shifted in from the memory card.

Typically, the DRFUL bit is not used to control data transfers; rather, it is checked during recovery from an error condition. There is no interrupt associated with the DRFUL bit.

### 2.9.7.13 Checking the Status of the SD\_CLK Pin

Read the CLKSTP bit in MMCST1 to determine whether the memory clock has been stopped on the SD\_CLK pin.

### 2.9.7.14 Checking the Remaining Block Count During a Multiple-Block Transfer

During a transfer of multiple data blocks, the MMC number of blocks counter register (MMCNBLC) indicates how many blocks are remaining to be transferred. MMCNBLC is a read-only register.

## 2.10 Interrupt Support

### 2.10.1 Interrupt Events and Requests

The MMC/SD controller generates the interrupt requests described in [Table 4](#). When an interrupt event occurs, its flag bit is set in the MMC status register 0 (MMCST0). If the enable bits corresponding to each flag are set in the MMC interrupt mask register (MMCIM), an interrupt request is generated. All such requests are multiplexed to a single MMC/SD interrupt request from the MMC/SD controller to the ARM CPU.

The MMC/SD interrupts are part of the maskable ARM interrupts. ARM interrupt 26 (INT26) is associated with MMC/SD0 functions and ARM interrupt 23 (INT23) is associated with SDIO0 functions. ARM interrupt 27 (INT27) is associated with MMC/SD1 functions and ARM interrupt 31 (INT31) is associated with SDIO1 functions. The interrupt service routine (ISR) for the MMC/SDIO0 interrupt can determine the event that caused the interrupt by checking the bits in MMCST0. When MMCST0 is read (either by CPU or emulation), all of the register bits are automatically cleared.

### 2.10.2 Interrupt Multiplexing

The total number of interrupts in the device exceeds 64, which is the maximum number of interrupts supported by the ARM Interrupt Controller (AINTC) module. Therefore, several interrupts are multiplexed, and you must use the register ARM\_INTMUX in the System Control Module to select the interrupt source for multiplexed interrupts. Refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* ([SPRUFG5](#)) for more information on the System Control Module and ARM Interrupt Controller.

**Table 4. Description of MMC/SD Interrupt Requests**

Interrupt Request	Interrupt Event
TRNDNEINT	<b>For read operations:</b> The MMC/SD controller has received the last byte of data (before CRC check). <b>For write operations:</b> The MMC/SD controller has transferred the last word of data to the output shift register.
DATEDINT	An edge was detected on the DAT3 pin.
DRRDYINT	MMCDRR is ready to be read (data in FIFO is above threshold).

**Table 4. Description of MMC/SD Interrupt Requests (continued)**

<b>Interrupt Request</b>	<b>Interrupt Event</b>
DXRDYINT	MMCDXR is ready to transmit new data (data in FIFO is less than threshold).
CRCRSINT	A CRC error was detected in a response from the memory card.
CRCRDINT	A CRC error was detected in the data read from the memory card.
CRCWRINT	A CRC error was detected in the data written to the memory card.
TOUTRSINT	A time-out occurred while the MMC controller was waiting for a response to a command.
TOUTRDINT	A time-out occurred while the MMC controller was waiting for the data from the memory card.
RSPDNEINT	<b>For a command that requires a response:</b> The MMC controller has received the response without a CRC error. <b>For a command that does not require a response:</b> The MMC controller has finished sending the command.
BSYDNEINT	The memory card stops or is no longer sending a busy signal when the MMC controller is expecting a busy signal.
DATDNEINT	<b>For read operations:</b> The MMC controller has received data without a CRC error and all data are read out from FIFO. <b>For write operations:</b> The MMC controller has finished sending data. CRC and card programming are complete.

### 2.11 DMA Event Support

The MMC/SD controller is capable of generating EDMA events for both read and write operations in order to request service from an EDMA controller. Based on the FIFO threshold setting, the EDMA event signals would be generated every time 256-bit or 512-bit data is transferred from the FIFO.

### 2.12 Power Management

The MMC/SD controller can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the MMC/SD controller is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide (SPRUFG5)*.

### 2.13 Emulation Considerations

The MMC/SD controller is not affected by emulation halt events (such as breakpoints).

### 3 Procedures for Common Operations

#### 3.1 Card Identification Operation

Before the MMC/SD controller starts data transfers to or from memory cards in the MMC/SD native mode, it has to first identify how many cards are present on the bus and configure them. For each card that responds to the ALL\_SEND\_CID broadcast command, the controller reads that card's unique card identification address (CID) and then assigns it a relative address (RCA). This address is much shorter than the CID and is used by the MMC/SD controller to identify the card in all future commands that involve the card.

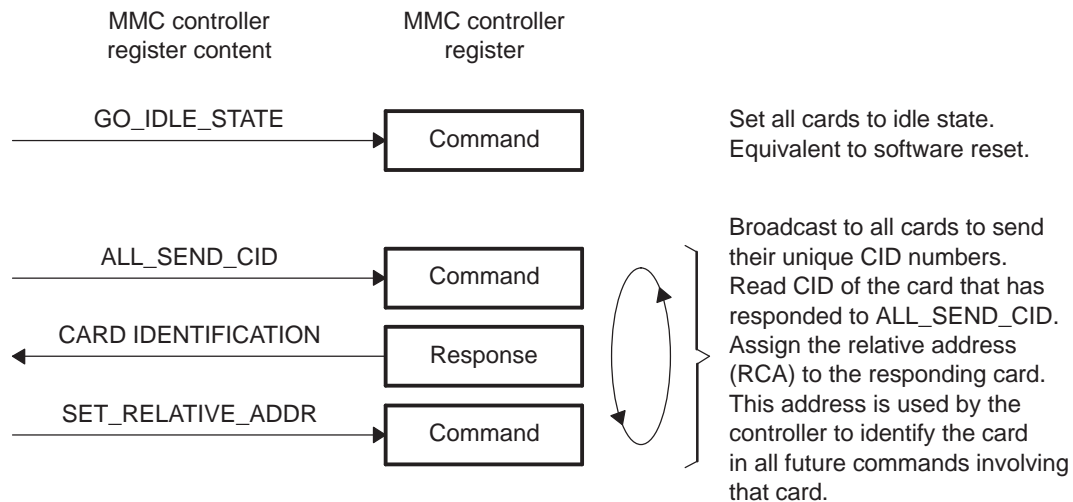
Only one card completes the response to ALL\_SEND\_CID at any one time. The absence of any response to ALL\_SEND\_CID indicates that all cards have been identified and configured.

The procedure for a card identification operation is:

1. Use the MMC command register (MMCCMD) to send the GO\_IDLE\_STATE command to the cards. This puts all cards in the idle state.
2. Use MMCCMD to send the ALL\_SEND\_CID command to the cards. This notifies all cards to identify themselves.
3. Wait for a card to respond. If a card responds, go to step 4; otherwise, stop.
4. Read the CID from the MMC response registers (MMCRSP01-MMCRSP67) and assign a relative address to the card by sending the SET\_RELATIVE\_ADDR command.

The sequence of events in this operation is shown in [Figure 12](#).

**Figure 12. Card Identification (Native MMC/SD Mode)**



#### 3.2 MMC/SD Mode Single-Block Write Operation Using CPU

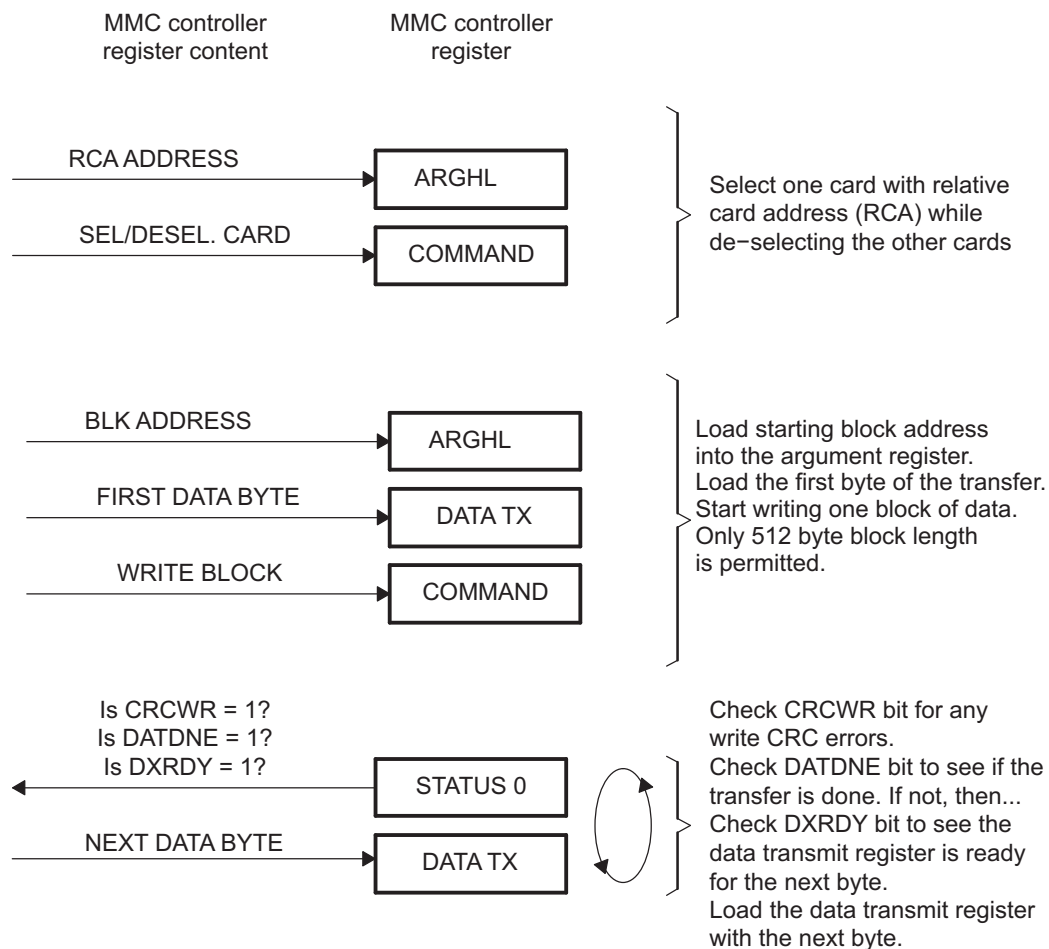
To perform a single-block write, the block length must be 512 bytes and the same length needs to be set in both the MMC/SD controller and the memory card. This sequence description assumes that the DMATRIG bit (bit 16) of the MMCCMD register is set. The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Use the MMC command register (MMCCMD) to send the SELECT/DESELECT\_CARD broadcast command. This selects the addressed card and deselects the others.
3. Write the destination start address to the MMC argument registers.
4. Read card CSD to determine the card's maximum block length.
5. Use MMCCMD to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
6. Reset the FIFO (FIFORST bit in MMCFIFOCTL).

7. Set the FIFO direction to transmit (FIFODIR bit in MMCFIFOCTL).
8. Set the access width (ACCWD bits in MMCFIFOCTL).
9. Enable the MMC interrupt.
10. Enable DXRDYINT interrupt.
11. Write the first 32 bytes of the data block to the data transmit register (MMCDXR).
12. Use MMCCMD to send the WRITE\_BLOCK command to the card.
13. Wait for the MMC interrupt
14. Use the MMC status register 0 (MMCST0) to check for errors and the status of the FIFO. If all of the data has not been written and if the FIFO is not full, go to step 15. If all of the data has been written, stop.
15. Write the next  $n$  bytes (depends on setting of FIFOLEV in MMCFIFOCTL: 0 = 32 bytes , 1 = 64 bytes ) of the data block to the MMC data transmit register (MMCDXR) and go to step 13.

The sequence of events in this operation is shown in [Figure 13](#).

**Figure 13. MMC/SD Mode Single-Block Write Operation**



### 3.3 MMC/SD Mode Single-Block Write Operation Using EDMA

To perform a single-block write, the block length must be 512 bytes and the same length needs to be set in both the MMC/SD controller and the card. The procedure for this operation is:

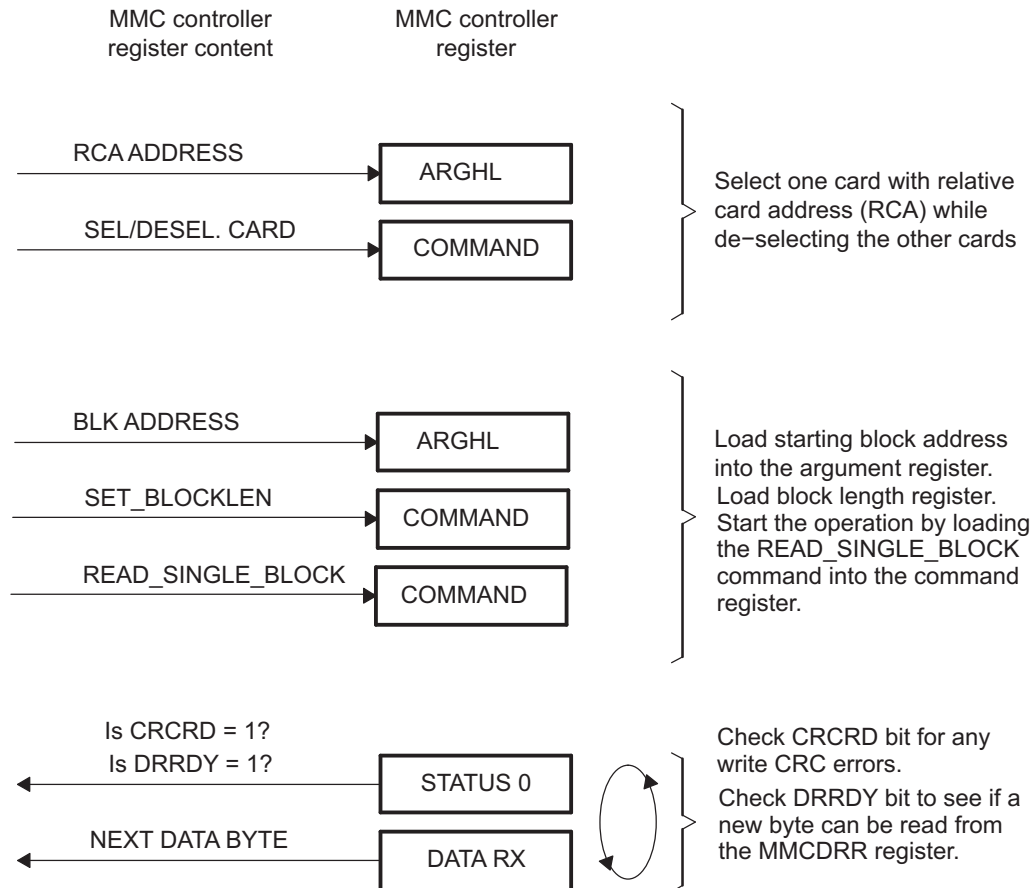
1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Read card CSD to determine the card's maximum block length.
3. Use the MMC command register (MMCCMD) to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
4. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
5. Set the FIFO direction to transmit (FIFODIR bit in MMCFIFOCTL).
6. Set the access width (ACCWD bits in MMCFIFOCTL).
7. Set the FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
8. Set up DMA (DMA size needs to be greater than or equal to FIFOLEV setting).
9. Use MMCCMD to send the WRITE\_BLOCK command to the card (set DMATRIG bit in MMCCMD to trigger first DMA).
10. Wait for DMA sequence to complete or the DATADNE flag in the MMC status register 0 (MMCST0) is set.
11. Use MMCST0 to check for errors.

### 3.4 MMC/SD Mode Single-Block Read Operation Using CPU

To perform a single-block read, the same block length needs to be set in both the MMC/SD controller and the card. The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Use the MMC command register (MMCCMD) to send the SELECT/DESELECT\_CARD broadcast command. This selects the addressed card and deselects the others.
3. Write the source start address to the MMC argument registers.
4. Read card CSD to determine the card's maximum block length.
5. Use MMCCMD to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
6. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
7. Set the FIFO direction to receive (FIFODIR bit in MMCFIFOCTL).
8. Set the access width (ACCWD bits in MMCFIFOCTL).
9. Set the FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
10. Enable the MMC interrupt.
11. Enable DRRDYINT interrupt.
12. Use MMCCMD to send the READ\_SINGLE\_BLOCK command (set the DMATRIG bit in the MMCCMD register to trigger).
13. Wait for MMC interrupt.
14. Use the MMC status register 0 (MMCST0) to check for errors and the status of the FIFO. If the FIFO is not empty, go to step 14. If the all of the data has been read, stop.
15. Read the next  $n$  bytes of data (depends on setting of FIFOLEV in MMCFIFOCTL: 0 = 32 bytes , 1 = 64 bytes ) from the MMC data receive register (MMCDRR) and go to step 13.

The sequence of events in this operation is shown in [Figure 14](#).

**Figure 14. MMC/SD Mode Single-Block Read Operation**


### 3.5 MMC/SD Mode Single-Block Read Operation Using EDMA

To perform a single-block read, the same block length needs to be set in both the MMC/SD controller and the card. The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Read card CSD to determine the card's maximum block length.
3. Use the MMC command register (MMCCMD) to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
4. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
5. Set the FIFO direction to receive (FIFODIR bit in MMCFIFOCTL).
6. Set the access width (ACCWD bits in MMCFIFOCTL).
7. Set the FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
8. Set up DMA (DMA size needs to be greater than or equal to FIFOLEV setting).
9. Use MMCCMD to send the READ\_BLOCK command to the card (set the DMATRIG bit in the MMCCMD register to trigger).
10. Wait for DMA sequence to complete.
11. Use the MMC status register 0 (MMCST0) to check for errors.

### 3.6 MMC/SD Mode Multiple-Block Write Operation Using CPU

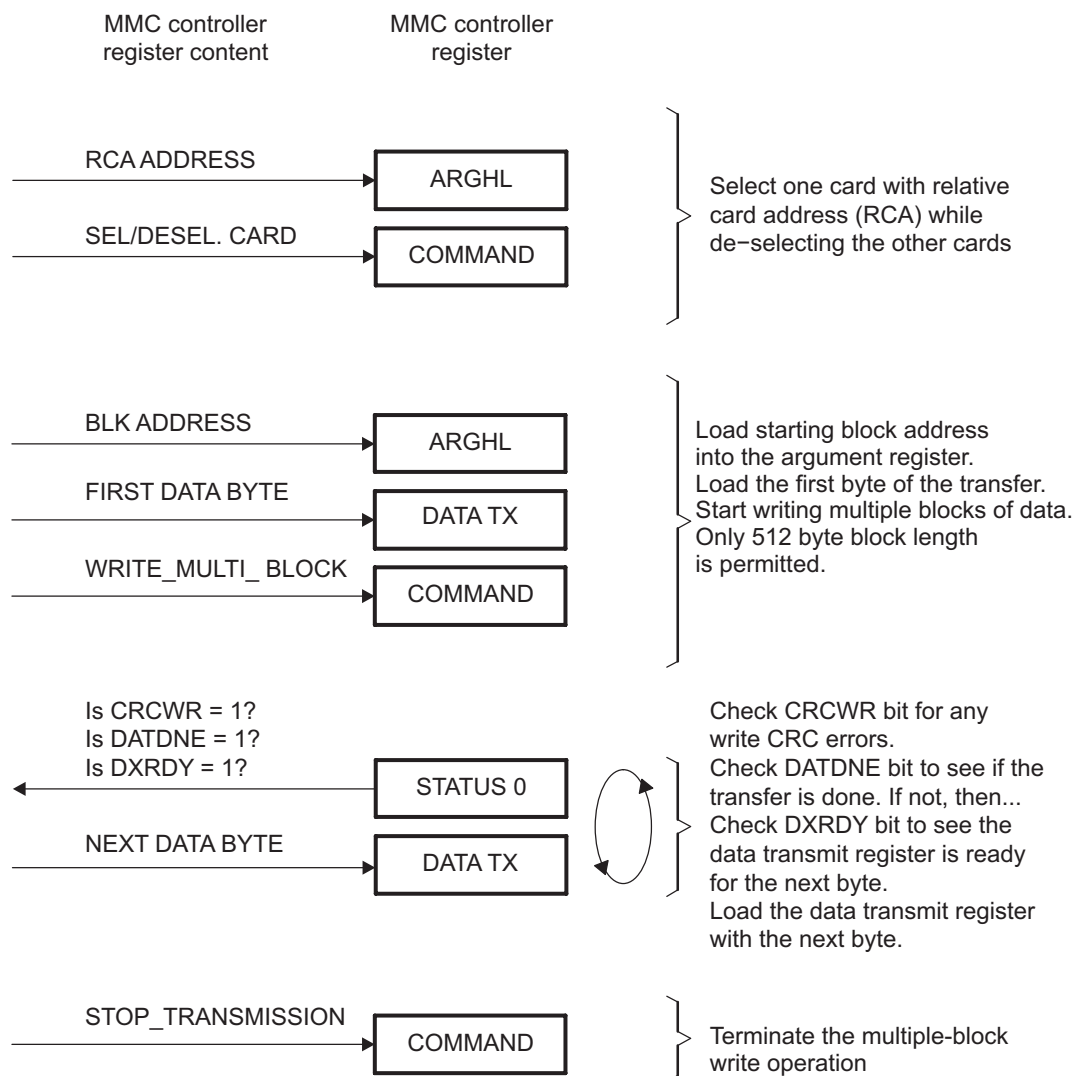
To perform a multiple-block write, the same block length needs to be set in both the MMC/SD controller and the card.

**Note:** The procedure in this section uses a STOP\_TRANSMISSION command to end the block transfer. This assumes that the value in the MMC number of blocks counter register (MMCNBLK) is 0. A multiple-block operation terminates itself if you load MMCNBLK with the exact number of blocks you want transferred. This sequence description assumes that the DMATRIG bit (bit 16) of the MMCCMD register is set.

The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Read card CSD to determine the card's maximum block length.
3. Use the MMC command register (MMCCMD) to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
4. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
5. Set the FIFO direction to transmit (FIFODIR bit in MMCFIFOCTL).
6. Set the access width (ACCWD bits in MMCFIFOCTL).
7. Set the FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
8. Enable the MMC interrupt.
9. Enable DXRDYINT interrupt.
10. Write the first 32 bytes of the data block to the MMC data transmit register (MMCDXR).
11. Use MMCCMD to send the WRITE\_MULTI\_BLOCK command to the card.
12. Wait for MMC interrupt.
13. Use the MMC status register 1 (MMCST1) to check for errors and to determine the status of the FIFO. If more bytes are to be written and the FIFO is not full, go to step 14. If the all of the data has been written, go to step 15.
14. Write the next  $n$  bytes (depends on setting of FIFOLEV in MMCFIFOCTL: 0 = 32 bytes , 1 = 64 bytes ) of the data block to MMCDXR, and go to step 12.
15. Use MMCCMD to send the STOP\_TRANSMISSION command.

The sequence of events in this operation is shown in [Figure 15](#).

**Figure 15. MMC/SD Multiple-Block Write Operation**


### 3.7 MMC/SD Mode Multiple-Block Write Operation Using EDMA

To perform a multiple-block write, the same block length needs to be set in both the MMC/SD controller and the card. The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Read card CSD to determine the card's maximum block length.
3. Use the MMC command register (MMCCMD) to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
4. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
5. Set the FIFO direction to transmit (FIFODIR bit in MMCFIFOCTL).
6. Set the FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
7. Set the access width (ACCWD bits in MMCFIFOCTL).
8. Set up DMA (DMA size needs to be greater than or equal to FIFOLEV setting).
9. Use MMCCMD to send the WRITE\_MULTI\_BLOCK command to the card (set DMATRIG bit in MMCCMD to trigger first DMA).



10. Wait for DMA sequence to complete or the DATADNE flag in the MMC status register 0 (MMCST0) is set.
11. Use MMCST0 to check for errors.
12. Use MMCCMD to send the STOP\_TRANSMISSION command.

### 3.8 MMC/SD Mode Multiple-Block Read Operation Using CPU

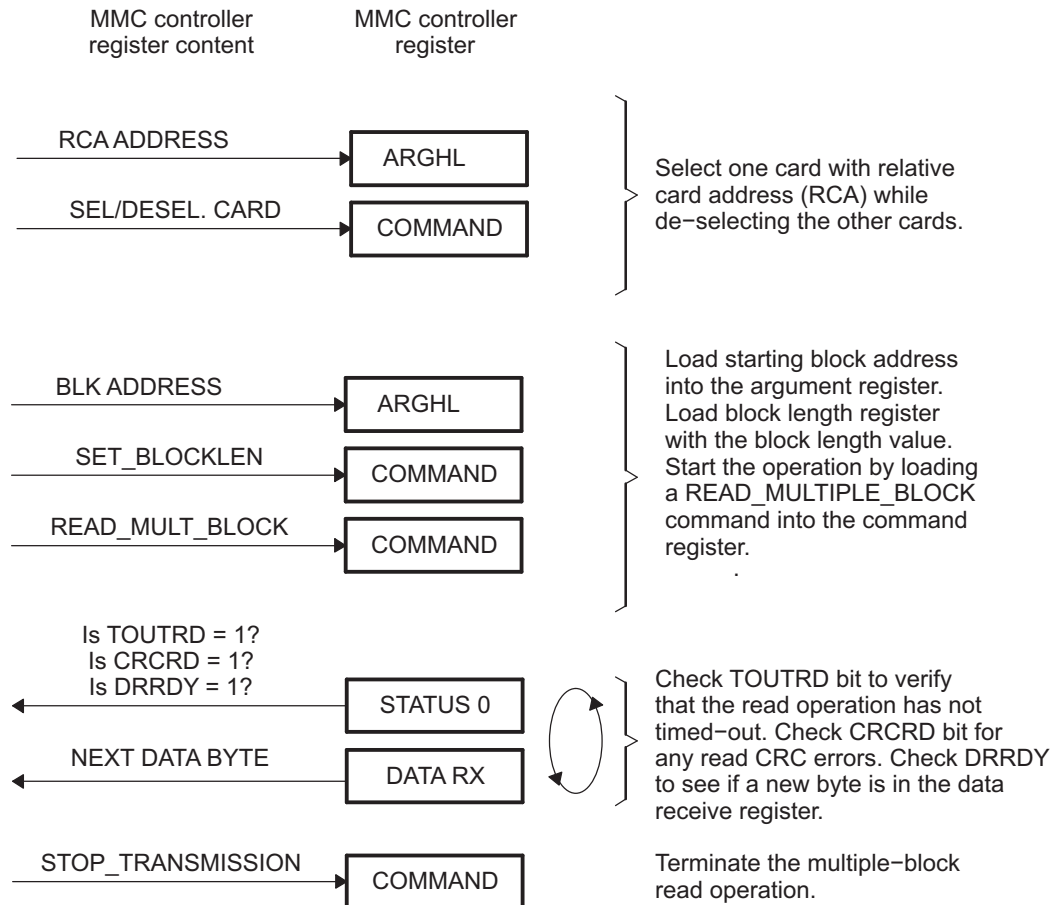
To perform a multiple-block read, the same block length needs to be set in both the MMC/SD controller and the card.

**Note:** The procedure in this section uses a STOP\_TRANSMISSION command to end the block transfer. This assumes that the value in the MMC number of blocks counter register (MMCNBLK) is 0. A multiple-block operation terminates itself if you load MMCNBLK with the exact number of blocks you want transferred.

The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Read card CSD to determine the card's maximum block length.
3. Use the MMC command register (MMCCMD) to send the SET\_BLOCKLEN command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
4. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
5. Set the FIFO direction to receive (FIFODIR bit in MMCFIFOCTL).
6. Set FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
7. Set the access width (ACCWD bits in MMCFIFOCTL).
8. Enable the MMC interrupt.
9. Enable DRRDYINT interrupt.
10. Use MMCCMD to send the READ\_MULT\_BLOCKS command (set the DMATRIG bit in the MMCCMD register to trigger).
11. Wait for MMC interrupt.
12. Use the MMC status register 1 (MMCST1) to check for errors and to determine the status of the FIFO. If FIFO is not empty and more bytes are to be read, go to step 13. If the all of the data has been read, go to step 14.
13. Read  $n$  bytes (depends on setting of FIFOLEV in MMCFIFOCTL: 0 = 32 bytes , 1 = 64 bytes ) of data from the MMC data receive register (MMCDRR) and go to step 10.
14. Use MMCCMD to send the STOP\_TRANSMISSION command.

The sequence of events in this operation is shown in [Figure 16](#).

**Figure 16. MMC/SD Mode Multiple-Block Read Operation**


### 3.9 MMC/SD Mode Multiple-Block Read Operation Using EDMA

To perform a multiple-block read, the same block length needs to be set in both the MMC/SD controller and the card. The procedure for this operation is:

1. Write the card's relative address to the MMC argument registers (MMCARGHL).
2. Read card CSD to determine the card's maximum block length.
3. Use the MMC command register (MMCCMD) to send the **SET\_BLOCKLEN** command (if the block length is different than the length used in the previous operation). The block length must be a multiple of 512 bytes and less than the maximum block length specified in the CSD.
4. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
5. Set the FIFO direction to receive (FIFODIR bit in MMCFIFOCTL).
6. Set the FIFO threshold (FIFOLEV bit in MMCFIFOCTL).
7. Set the access width (ACCWD bits in MMCFIFOCTL).
8. Set up DMA (DMA size needs to be greater than or equal to FIFOLEV setting).
9. Use MMCCMD to send the **READ\_MULT\_BLOCK** command to the card (set the DMATRIG bit in the MMCCMD bit to trigger).
10. Wait for DMA sequence to complete.
11. Use the MMC status register 0 (MMCST0) to check for errors.
12. Use MMCCMD to send the **STOP\_TRANSMISSION** command.

### 3.10 SD High Speed Mode

To perform the high-speed mode operation, the card need to be placed in high-speed mode. For all the data transfer commands, it is necessary to set the DMATRIG bit in the MMCCMD register while giving the command. The procedure for this operation is:

1. Follow the normal card identification procedure, since all the high-speed cards are by default initially normal SD cards. Once card is successfully identified it needs to be switched into high-speed mode.
2. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
3. Send CMD16 (SET\_BLOCK\_LEN) with argument as 8 (8 bytes) to set the block length in the card.
4. Set the block length as 8 bytes and number of blocks as 1 in MMCS controller registers MMCBLLEN and MMNBLK respectively.
5. Read the SCR register by sending ACMD51
6. Parse the 64-bit response received from the card to check whether the card has support of SD spec Ver1.10. The high-speed support is available only cards those are supporting SD VER 1.10.
7. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
8. Send CMD16 (SET\_BLOCK\_LEN) with argument as 64 (64 bytes) to set the block length in the card.
9. Set the block length as 64 bytes and number of blocks as 1 in MMCS controller registers MMCBLLEN and MMNBLK respectively.
10. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
11. Send CMD6 with Mode 0.
12. Parse the 512-bit response received from the card to check whether the card has high-speed function support. If yes, check that the Maximum current consumption for this function is within the limit which is specified in CSD register (CSD register bits 61:50, response for the CMD9, SEND\_CSD).
13. Reset the FIFO (FIFORST bit in MMCFIFOCTL).
14. Send CMD6 with Mode 1 to enable the high-speed function.
15. Parse the 512-bit response received from the card to check whether the card has successfully been placed in high-speed mode.
16. Increase the MMCS clock rate up to 50 MHz.
17. Follow normal Read/Write operation.

### 3.11 SDIO Card Function

To support the SDIO card, the following features are available in the MMC/SD controller:

- Read wait operation request
- Interrupt to ARM at the start of read wait operation (INT23 and INT31)
- Interrupt to ARM at the detection of SDIO interrupt (INT23 and INT31)

When in 1-bit mode and the transfer clock (memory clock) is off, this peripheral cannot recognize an SDIO interrupt from SD\_DATA1 line. Two options are available to deal with this situation:

1. Do not turn off the memory clock in 1-bit mode. The clock is enabled by the CLKEN bit in the MMC memory clock control register (MMCCCLK).
2. If the memory clock needs to be turned off, physically connect a GPIO signal and SD\_DATA1, and use the GPIO as an external interrupt input. When the memory clock is enabled, disable the GPIO interrupt and enable the SDIO interrupt. When the memory clock is disabled, enable the GPIO interrupt and disable the SDIO interrupt by software.

#### 3.11.1 SDIO Control Register (SDIOCTL)

The SDIO card control register (SDIOCTL) is used to configure the read wait operation using the SD\_DATA2 line.

#### 3.11.2 SDIO Status Register 0 (SDIOST0)

The SDIO card status register 0 (SDIOST0) is used to check the status of the SD\_DATA1 signal, check the status of being in an interrupt period, or check the status of being in a read wait operation.

### 3.11.3 SDIO Interrupt Control Registers (SDIOIEN, SDIOIST)

The SDIO card controller issues an interrupt to the ARM CPU when the read wait operation starts or when an SDIO interrupt is detected on the SD\_DATA1 line.

Interrupt flags of each case are checked with the SDIO interrupt status register (SDIOIST). To issue an actual interrupt to ARM, enabling each interrupt in the SDIO interrupt enable register (SDIOIEN) is required.

When both interrupts are enabled, they are both reported to the ARM CPU as a single interrupt (whether one or both occurred). The interrupt(s) that occurred are determined by reading SDIOIST.

## 4 Registers

[Table 5](#) lists the memory-mapped registers for the multimedia card/secure digital (MMC/SD) card controller. See the device-specific data manual for the memory address of these registers.

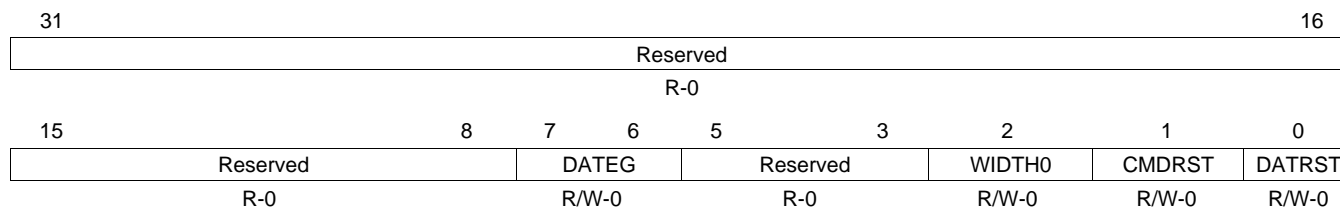
**Table 5. Multimedia Card/Secure Digital (MMC/SD) Card Controller Registers**

Offset	Acronym	Register Description	Section
00h	MMCCTL	MMC Control Register	<a href="#">Section 4.1</a>
04h	MMCCLK	MMC Memory Clock Control Register	<a href="#">Section 4.2</a>
08h	MMCST0	MMC Status Register 0	<a href="#">Section 4.3</a>
0Ch	MMCST1	MMC Status Register 1	<a href="#">Section 4.4</a>
10h	MMCIM	MMC Interrupt Mask Register	<a href="#">Section 4.5</a>
14h	MMCTOR	MMC Response Time-Out Register	<a href="#">Section 4.6</a>
18h	MMCTOD	MMC Data Read Time-Out Register	<a href="#">Section 4.7</a>
1Ch	MMCBLEN	MMC Block Length Register	<a href="#">Section 4.8</a>
20h	MMCNBLK	MMC Number of Blocks Register	<a href="#">Section 4.9</a>
24h	MMCNBLC	MMC Number of Blocks Counter Register	<a href="#">Section 4.10</a>
28h	MMCDRR	MMC Data Receive Register	<a href="#">Section 4.11</a>
2Ch	MMCDXR	MMC Data Transmit Register	<a href="#">Section 4.12</a>
30h	MMCCMD	MMC Command Register	<a href="#">Section 4.13</a>
34h	MMCARGHL	MMC Argument Register	<a href="#">Section 4.14</a>
38h	MMCRSP01	MMC Response Register 0 and 1	<a href="#">Section 4.15</a>
3Ch	MMCRSP23	MMC Response Register 2 and 3	<a href="#">Section 4.15</a>
40h	MMCRSP45	MMC Response Register 4 and 5	<a href="#">Section 4.15</a>
44h	MMCRSP67	MMC Response Register 6 and 7	<a href="#">Section 4.15</a>
48h	MMCDRSP	MMC Data Response Register	<a href="#">Section 4.16</a>
50h	MMCCIDX	MMC Command Index Register	<a href="#">Section 4.17</a>
64h	SDIOCTL	SDIO Control Register	<a href="#">Section 4.18</a>
68h	SDIOST0	SDIO Status Register 0	<a href="#">Section 4.19</a>
6Ch	SDIOIEN	SDIO Interrupt Enable Register	<a href="#">Section 4.20</a>
70h	SDIOIST	SDIO Interrupt Status Register	<a href="#">Section 4.21</a>
74h	MMCFIFOCTL	MMC FIFO Control Register	<a href="#">Section 4.22</a>

#### 4.1 MMC Control Register (MMCCTL)

The MMC control register (MMCCTL) is used to enable or configure various modes of the MMC controller. Set or clear the DATRST and CMDRST bits at the same time to reset or enable the MMC controller. MMCCTL is shown in Figure 17 and described in Table 6.

**Figure 17. MMC Control Register (MMCCTL)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 6. MMC Control Register (MMCCTL) Field Descriptions**

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-6	DATEG	0-3h	DAT3 edge detection select. 0    DAT3 edge detection is disabled. 1h    DAT3 rising-edge detection is enabled. 2h    DAT3 falling-edge detection is enabled. 3h    DAT3 rising-edge and falling-edge detections are enabled.
5-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	WIDTH0	0-1	Data bus width bit 0 (MMC mode only). 0    Data bus has 1 bit (only DAT0 is used). 1    Data bus has 4 bits (all DAT0-3 are used).
1	CMDRST	0-1	CMD logic reset. 0    CMD line portion is enabled. 1    CMD line portion is disabled and in reset state.
0	DATRST	0-1	DAT logic reset. 0    DAT line portion is enabled. 1    DAT line portion is disabled and in reset state.

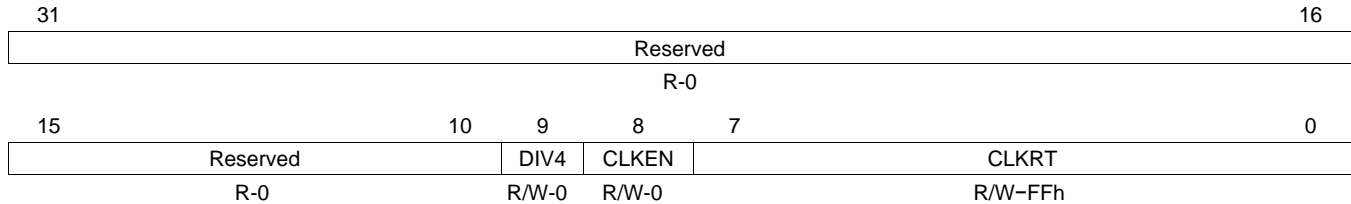
## 4.2 MMC Memory Clock Control Register (MMCCLK)

The MMC memory clock control register (MMCCLK) is used to:

- Select whether the CLK pin is enabled or disabled (CLKEN bit).
- Select how much the function clock is divided-down to produce the memory clock (CLKRT bits). When the CLK pin is enabled, the MMC controller drives the memory clock on this pin to control the timing of communications with attached memory cards. For more details about clock generation, see [Section 2.1](#).

MMCCLK is shown in [Figure 18](#) and described in [Table 7](#).

**Figure 18. MMC Memory Clock Control Register (MMCCLK)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7. MMC Memory Clock Control Register (MMCCLK) Field Descriptions**

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9	DIV4	0	MMC clock = function clock frequency/(2 * (CLKRT + 1) )
		1	MMC clock = function clock frequency/(4 * (CLKRT + 1) )
8	CLKEN		CLK pin enable.
		0	CLK pin is disabled and fixed low.
		1	The CLK pin is enabled; it shows the memory clock signal.
7-0	CLKRT	0-FFh	Clock rate. Use this field to set the divide-down value for the memory clock. The function clock is divided down as follows to produce the memory clock: memory clock frequency = function clock frequency/(2 * (CLKRT + 1) )

### 4.3 MMC Status Register 0 (MMCST0)

The MMC status register 0 (MMCST0) records specific events or errors. The transition from 0 to 1 on each bit in MMCST0 can cause an interrupt signal to be sent to the CPU. If an interrupt is desired, set the corresponding interrupt enable bit in the MMC interrupt mask register (MMCIM).

When a status bit is read (by CPU or emulation) it is cleared. Additionally DRRDY bit and the DXRDY bit are also cleared in response to the functional events described for them in Table 8, or in response to a hardware reset.

MMCST0 is shown in Figure 19 and described in Table 8.

**Figure 19. MMC Status Register 0 (MMCST0)**

Reserved							
R-0							
15	14	13	12	11	10	9	8
Reserved		CCS	TRNDNE	DATED	DRRDY	DXRDY	SPIERR
R-0		R-0	R-0	R-0	R-0	R-0	R-0
7	6	5	4	3	2	1	0
CRCRS	CRCRD	CRCWR	TOUTRS	TOUTRD	RSPDNE	BSYDNE	DATDNE
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; RC = Cleared to 0 when read; -n = value after reset

**Table 8. MMC Status Register 0 (MMCST0) Field Descriptions**

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13	CCS	0	Command 61 is not completed.
		1	Command 61 is completed.
12	TRNDNE	0	No data transfer is done.
		1	Data transfer of specified length is done.
11	DATED	0	A DAT3 edge has not been detected.
		1	A DAT3 edge has been detected.
10	DRRDY	0	MMCDRR is not ready.
		1	MMCDRR is ready. New data has arrived and can be read by the CPU or by the DMA controller.
9	DXRDY	0	MMCDXR is not ready.
		1	MMCDXR is ready. The data in MMCDXR has been transmitted; MMCDXR can accept new data from the CPU or from the DMA controller.
8	SPIERR	0	Data Error (in SPI mode)
		0	No data error is received.
		1	Data error token has been received.
7	CRCRS	0	A response CRC error has not been detected.
		1	A response CRC error has been detected.



**Table 8. MMC Status Register 0 (MMCST0) Field Descriptions (continued)**

Bit	Field	Value	Description
6	CRCRD	0	A read-data CRC error has not been detected.
		1	A read-data CRC error has been detected.
5	CRCWR	0	A write-data CRC error has not been detected.
		1	A write-data CRC error has been detected.
4	TOUTRS	0	A response time-out event has not occurred.
		1	A time-out event has occurred while the MMC controller was waiting for a response to a command.
3	TOUTRD	0	A read-data time-out event has not occurred.
		1	A time-out event has occurred while the MMC controller was waiting for data.
2	RSPDNE	0	Command/response done. No response is received.
		1	Command has been sent without response or response has been received for the command sent.
1	BSYDNE	0	Busy done. No busy releasing is done.
		1	Released from busy state or expected busy is not detected.
0	DATDNE	0	Data done The data has not been fully transmitted.
		1	The meaning of this status bit is different for write and read operation. For read operations: The MMC/SD controller has received data without a CRC error and all data are read out from FIFO. For write operations: The MMC/SD has finished sending data. CRC and card programming are complete.

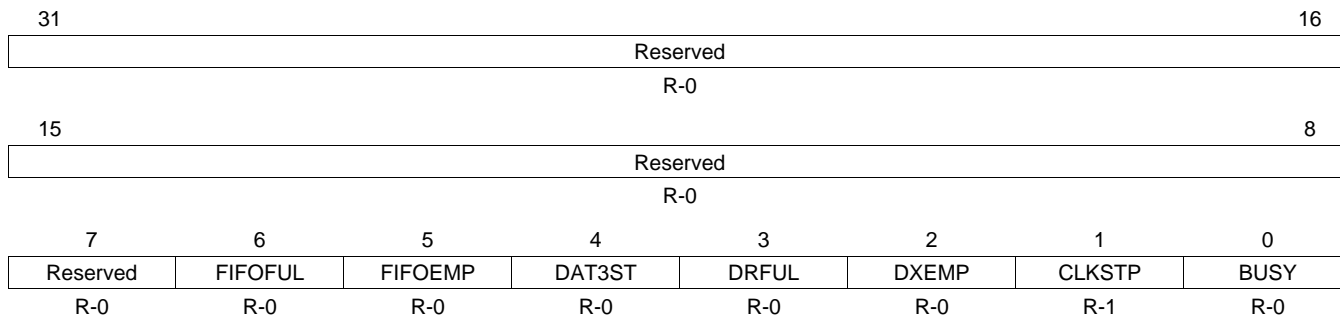
**NOTE:** 1) As the command portion and the data portion of the MMC/SD controller are independent, any command such as CMD0 (GO\_IDLE\_STATE) or CMD12 (STOP\_TRANSMISSION) can be sent to the card, even if during block transfer. In this situation, the data portion will detect this and wait, releasing the busy state only when the command sent was R1b (to be specific, command with BSYEXP bit), otherwise it will keep transferring data.

2) Bit 12 (TRNDNE) indicates that the last byte of a transfer has been completed. Bit 0 (DATDNE) occurs at end of a transfer but not until the CRC check and programming has been completed.

#### 4.4 MMC Status Register 1 (MMCST1)

The MMC status register 1 (MMCST1) records specific events or errors. There are no interrupts associated with these events or errors. MMCST1 is shown in Figure 20 and described in Table 9.

**Figure 20. MMC Status Register 1 (MMCST1)**



LEGEND: R = Read only; -n = value after reset

**Table 9. MMC Status 1 (MMCST1) Register Field Descriptions**

Bit	Field	Value	Description
31-7	Reserved	0	Reserved
6	FIFOFUL	0	FIFO is full.
		0	FIFO is not full.
		1	FIFO is full.
5	FIFOEMP	0	FIFO is empty.
		0	FIFO is not empty.
		1	FIFO is empty.
4	DAT3ST	0	DAT3 status. The signal level on the DAT3 pin is a logic-low level.
		1	The signal level on the DAT3 pin is a logic-high level.
		1	
3	DRFUL	0	Data receive register (MMCDRR) is full.
		0	A data receive register full condition is not detected.
		1	A data receive register full condition is detected.
2	DXEMP	0	Data transmit register (MMCDXR) is empty.
		0	A data transmit register empty condition is not detected. The data transmit shift register is not empty.
		1	A data transmit register empty condition is detected. The data transmit shift register is empty. No bits are available to be shifted out to the memory card.
1	CLKSTP	0	Clock stop status. CLK is active. The memory clock signal is being driven on the pin.
		1	CLK is held low because of a manual stop (CLKEN = 0 in MMCCLK), receive shift register is full, or transmit shift register is empty.
		1	
0	BUSY	0	Busy.
		0	No busy signal is detected.
		1	A busy signal is detected (the memory card is busy).

#### 4.5 MMC Interrupt Mask Register (MMCIM)

The MMC interrupt mask register (MMCIM) is used to enable (bit = 1) or disable (bit = 0) status interrupts. If an interrupt is enabled, the transition from 0 to 1 of the corresponding interrupt bit in the MMC status register 0 (MMCST0) can cause an interrupt signal to be sent to the CPU. MMCIM is shown in [Figure 21](#) and described in [Table 10](#).

**Figure 21. MMC Interrupt Mask (MMCIM) Register**

Reserved							
R-0							
15	14	13	12	11	10	9	8
Reserved	ECCS	ETRNDNE	EDATED	EDRRDY	EDXRDY	Reserved	Reserved
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0
7	6	5	4	3	2	1	0
ECRCRS	ECRCRD	ECRCWR	ETOUTRS	ETOUTRD	ERSPDNE	EBSYDNE	EDATDNE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. MMC Interrupt Mask(MMCIM) Register Field Descriptions**

Bit	Field	Value	Description
31-14	Reserved	0	Reserved
13	ECCS	0 1	Command Completion Signal permission bit Prohibited Permitted
12	ETRNDNE	0 1	Transfer done (TRNDNE) interrupt enable. Transfer done interrupt is disabled. Transfer done interrupt is enabled.
11	EDATED	0 1	DAT3 edge detect (DATED) interrupt enable. DAT3 edge detect interrupt is disabled. DAT3 edge detect interrupt is enabled.
10	EDRRDY	0 1	Data receive register ready (DRRDY) interrupt enable. Data receive register ready interrupt is disabled. Data receive register ready interrupt is enabled.
9	EDXRDY	0 1	Data transmit register (MMCDXR) ready interrupt enable. Data transmit register ready interrupt is disabled. Data transmit register ready interrupt is enabled.
8	Reserved	0	Reserved
7	ECRCRS	0 1	Response CRC error (CRCRS) interrupt enable. Response CRC error interrupt is disabled. Response CRC error interrupt is enabled.
6	ECRCRD	0 1	Read-data CRC error (CRCRD) interrupt enable. Read-data CRC error interrupt is disabled. Read-data CRC error interrupt is enabled.
5	ECRCWR	0 1	Write-data CRC error (CRCWR) interrupt enable. Write-data CRC error interrupt is disabled. Write-data CRC error interrupt is disabled.
4	ETOUTRS	0 1	Response time-out event (TOUTRS) interrupt enable. Response time-out event interrupt is disabled. Response time-out event interrupt is enabled.

**Table 10. MMC Interrupt Mask(MMCIM) Register Field Descriptions (continued)**

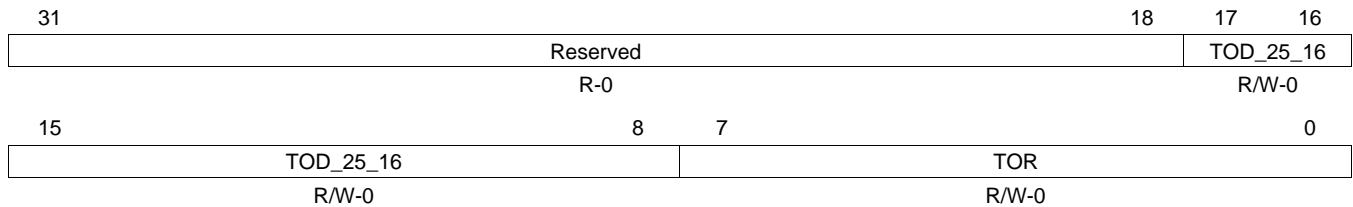
Bit	Field	Value	Description
3	ETOUTRD		Read-data time-out event (TOUTRD) interrupt enable.
		0	Read-data time-out event interrupt is disabled.
		1	Read-data time-out event interrupt is enabled.
		2	ERSPDNE
0	Command/response done interrupt is disabled.		
		1	Command/response done interrupt is enabled.
		1	EBSYDNE
0	Busy done interrupt is disabled.		
		1	Busy done interrupt is enabled.
		0	EDATDNE
0	Data done interrupt is disabled.		
		1	Data done interrupt is enabled.

#### 4.6 MMC Response Time-Out Register (MMCTOR)

The MMC response time-out register (MMCTOR) defines how long the MMC controller waits for a response from a memory card before recording a time-out condition in the TOUTRS bit of the MMC status register 0 (MMCST0). If the corresponding ETOUTRS bit in the MMC interrupt mask register (MMCIM) is set, an interrupt is generated when the TOUTRS bit is set in MMCST0. If a memory card should require a longer time-out period than MMCTOR can provide, a software time-out mechanism can be implemented.

MMCTOR is shown in [Figure 22](#) and described in [Table 11](#).

**Figure 22. MMC Response Time-Out Register (MMCTOR)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. MMC Response Time-Out Register (MMCTOR) Field Descriptions**

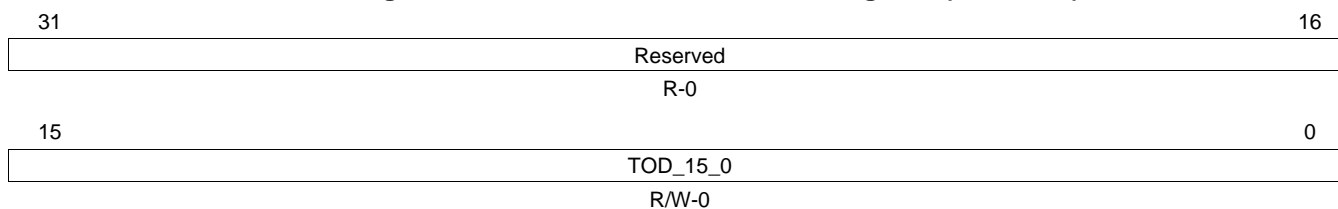
Bit	Field	Value	Description
31-18	Reserved	0	Any writes to these bit(s) must always have a value of 0.
17-8	TOD_25_16	0-1Fh	Data read time-out count upper 10 bits. Used in conjunction with the TOD_17_0 bits in MMCTOD to form a 24-bit count. See MMCTOD ( <a href="#">Section 4.7</a> ).
7-0	TOR	0-FFh	Time-out count for response.
		0	No Time Out
		1	CLK memory clock cycle to 255 CLK memory clock cycles

#### 4.7 MMC Data Read Time-Out Register (MMCTOD)

The MMC data read time-out register (MMCTOD) defines how long the MMC controller waits for the data from a memory card before recording a time-out condition in the TOUTRD bit of the MMC status register 0 (MMCST0). If the corresponding ETOUTRD bit in the MMC interrupt mask register (MMCIM) is set, an interrupt is generated when the TOUTRD bit is set in MMCST0. If a memory card should require a longer time-out period than MMCTOD can provide, a software time-out mechanism can be implemented.

MMCTOD is shown in [Figure 23](#) and described in [Table 12](#).

**Figure 23. MMC Data Read Time-Out Register (MMCTOD)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

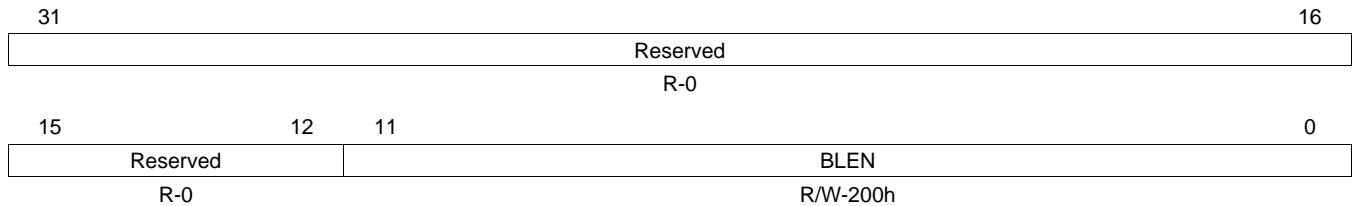
**Table 12. MMC Data Read Time-Out Register (MMCTOD) Field Descriptions**

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	TOD_15_0	0-FFFFh	Data read time-out count. Used in conjunction with the TOD_23_16 bits in MMCTOR to form a 24-bit count. See MMCTOR ().
		0	No time out
		1-FFFFh	1 CLK clock cycle to 64,000 CLK clock cycles. When used in conjunction with TOD_23_16, the value range will be 1-1F FFFF clock cycles.

#### 4.8 MMC Block Length Register (MMCBLEN)

The MMC block length register (MMCBLEN) specifies the data block length in bytes. This value must match the block length setting in the memory card. MMCBLEN is shown in [Figure 24](#) and described in [Table 13](#).

**Figure 24. MMC Block Length Register (MMCBLEN)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 13. MMC Block Length Register (MMCBLEN) Field Descriptions**

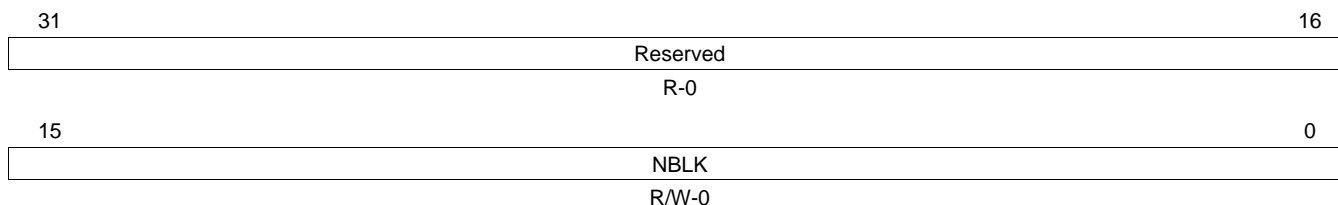
Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	BLEN	1h-FFFh	Block length. This field is used to set the block length, which is the byte count of a data block. The value 0 is prohibited.

**NOTE:** The BLEN bits value must be the same as the CSD register settings in the MMC/SD card. To be precise, it should match the value of the READ\_BL\_LEN field for read, or WRITE\_BL\_LEN field for write.

#### 4.9 MMC Number of Blocks Register (MMCNBLK)

The MMC number of blocks register (MMCNBLK) specifies the number of blocks for a multiple-block transfer. MMCNBLK is shown in [Figure 25](#) and described in [Table 14](#).

**Figure 25. MMC Number of Blocks Register (MMCNBLK)**



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

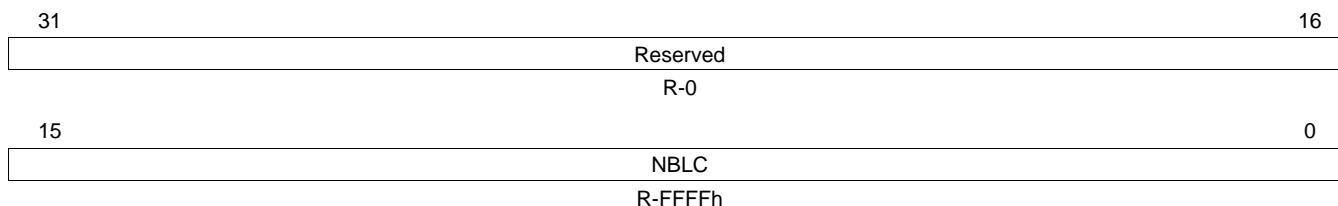
**Table 14. MMC Number of Blocks Register (MMCNBLK) Field Descriptions**

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	NBLK	0-FFFFh	Number of blocks. This field is used to set the total number of blocks to be transferred.
		0	Infinite number of blocks. The MMC controller reads/writes blocks of data until a STOP_TRANSMISSION command is written to the MMC command register (MMCCMD).
		1h-FFFFh	<i>n</i> blocks. The MMC controller reads/writes only <i>n</i> blocks of data, even if the STOP_TRANSMISSION command has not been written to the MMC command register (MMCCMD).

#### 4.10 MMC Number of Blocks Counter Register (MMCNBLC)

The MMC number of blocks counter register (MMCNBLC) is a down-counter for tracking the number of blocks remaining to be transferred during a multiple-block transfer. MMCNBLC is shown in [Figure 26](#) and described in [Table 15](#).

**Figure 26. MMC Number of Blocks Counter Register (MMCNBLC)**



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Table 15. MMC Number of Blocks Counter Register (MMCNBLC) Field Descriptions**

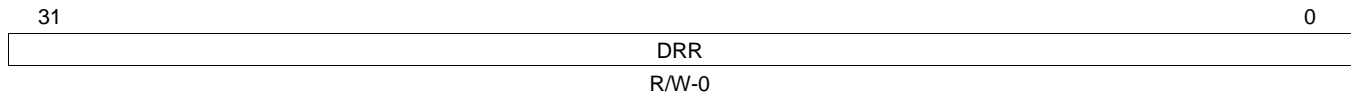
Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	NBLC	0-FFFFh	Read this field to determine the number of blocks remaining to be transferred.



#### 4.11 MMC Data Receive Register (MMCDRR)

The MMC data receive register (MMCDRR) is used for storing the data received from the MMC card. The CPU or the DMA controller can read data from this register. MMCDRR expects the data in little-endian format. MMCDRR is shown in [Figure 27](#) and described in [Table 16](#).

**Figure 27. MMC Data Receive Register (MMCDRR)**



LEGEND: R/W = Read/Write; -n = value after reset

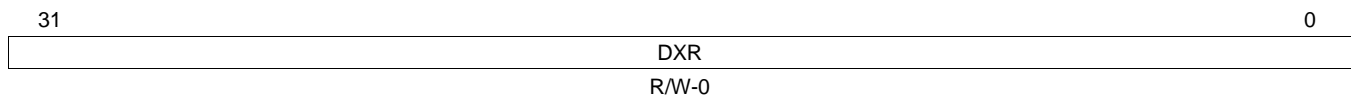
**Table 16. MMC Data Receive Register (MMCDRR) Field Descriptions**

Bit	Field	Value	Description
31-0	DRR	0-FFFF FFFFh	Data receive.

#### 4.12 MMC Data Transmit Register (MMCDXR)

The MMC data transmit register (MMCDXR) is used for storing the data to be transmitted from the MMC controller to the memory card. The CPU or the DMA controller can write data to this register to be transmitted. MMCDXR expects the data in little-endian format. MMCDXR is shown in [Figure 28](#) and described in [Table 17](#).

**Figure 28. MMC Data Transmit Register (MMCDXR)**



LEGEND: R/W = Read/Write; -n = value after reset

**Table 17. MMC Data Transmit Register (MMCDXR) Field Descriptions**

Bit	Field	Value	Description
31-0	DXR	0-FFFF FFFFh	Data transmit.

### 4.13 MMC Command Register (MMCCMD)

**NOTE:** Writing to the MMC command register (MMCCMD) causes the MMC controller to send the programmed command. Therefore, the MMC argument register (MMCARGHL) must be loaded properly before a write to MMCCMD.

The MMC command register (MMCCMD) specifies the type of command to be sent and defines the operation (command, response, additional activity) for the MMC controller. The content of MMCCMD is kept after the transfer to the transmit shift register. MMCCMD is shown in [Figure 29](#) and described in [Table 18](#).

When the ARM writes to MMCCMD, the MMC controller sends the programmed command, including any arguments in the MMC argument register (MMCARGHL). For the format of a command (index, arguments, and other bits), see [Figure 30](#) and [Table 19](#).

**Figure 29. MMC Command Register (MMCCMD)**

31							24								
Reserved															
R-0															
23							17							16	
Reserved												DMATRIG			
R-0												W-0			
15		14		13		12		11		10		9		8	
DCLR		INITCK		WDATX		STRMTP		DTRW		RSPFMT		BSYEXP			
R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0			
7		6		5								0			
PPLEN		Reserved		CMD											
R/W-0		R-0		R/W-0											

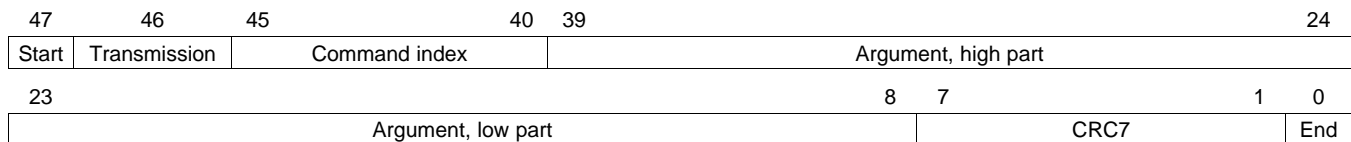
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 18. MMC Command Register (MMCCMD) Field Descriptions**

Bit	Field	Value	Description
31-17	Reserved	0	Reserved
16	DMATRIG		Data transfer trigger. This bit is used to kick start a CPU or DMA data transfer. Set this bit when issuing a data transfer command.
		0	Data transfer has not been triggered.
		1	Data transfer has been triggered.
15	DCLR		Data receive/transmit clear. Use this bit to clear the data receive ready (DRRDY) bit and the data transmit ready (DXRDY) bit in the MMC status register 0 (MMCST0) before a new read or write sequence. This clears any previous status.
		0	Do not clear DRRDY and DXRDY bits in MMCST0.
		1	Clear RRDY (=0) when in read command; set XRDY (=1) when in write command.
14	INITCK		Initialization clock cycles.
		0	Do not insert initialization clock cycles.
		1	Insert initialization clock cycles; insert 80 CLK cycles before sending the command specified in the CMD bits. These dummy clock cycles are required for resetting a card after power on.
13	WDATX		Data transfer indicator.
		0	There is no data transfer associated with the command being sent.
		1	There is data transfer associated with the command being sent.

**Table 18. MMC Command Register (MMCCMD) Field Descriptions (continued)**

Bit	Field	Value	Description
12	STRMTP	0	Stream transfer enable. If WDATX = 1, the data transfer is a block transfer. The data transfer stops after the movement of the programmed number of bytes (defined by the programmed block size and the programmed number of blocks).
		1	If WDATX = 1, the data transfer is a stream transfer. Once the data transfer is started, the data transfer does not stop until the MMC controller issues a stop command to the memory card.
11	DTRW	0	Data transfer write enable. If WDATX = 1, the data transfer is a read operation.
		1	If WDATX = 1, the data transfer is a write operation.
10-9	RSPFMT	0-3h	Response format (expected type of response to the command).
		0	No response.
		1h	R1, R4, R5, or R6 response. 48 bits with CRC.
		2h	R2 response. 136 bits with CRC.
8	BSYEXP	3h	R3 response. 48 bits with no CRC.
		0	Busy expected. If an R1b (R1 with busy) response is expected, set RSPFMT = 1h and BSYEXP = 1. A busy signal is not expected.
7	PPLEN	1	A busy signal is expected.
		0	Push pull enable. Push pull driver of CMD line is disabled (open drain).
6	Reserved	1	Push pull driver of CMD line is enabled.
		0	Reserved.
5-0	CMD	0-3Fh	Command index. This field contains the command index for the command to be sent to the memory card.

**Figure 30. Command Format****Table 19. Command Format**

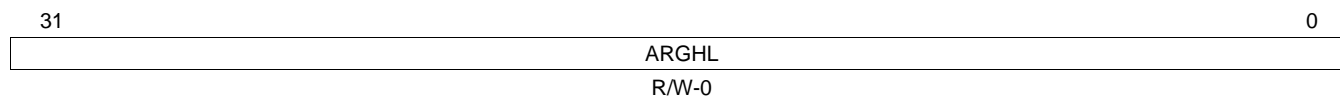
Bit Position of Command	Register	Description
47	-	Start bit
46	-	Transmission bit
45-40	MMCCMD(5-0)	Command index (CMD)
39-24	MMCARGHL	Argument, high part
23-8	MMCARGHL	Argument, low part
7-1	-	CRC7
0	-	End bit

#### 4.14 MMC Argument Register (MMCARGHL)

**NOTE:** Do not modify the MMC argument register (MMCARGHL) while it is being used for an operation.

The MMC argument register (MMCARGHL) specifies the arguments to be sent with the command specified in the MMC command register (MMCCMD). Writing to MMCCMD causes the the MMC controller to send a command; therefore, MMCARGHL must be configured before writing to MMCCMD. The content of MMCARGHL is kept after the transfer to the shift register; however, modification to MMCARGHL is not allowed during a sending operation. MMCARGHL is shown in [Figure 31](#) and described in [Table 20](#). For the format of a command, see [Figure 30](#) and [Table 19](#).

**Figure 31. MMC Data Transmit Register (MMCARGHL)**



LEGEND: R/W = Read/Write; -n = value after reset

**Table 20. MMC Argument Register (MMCARGHL) Field Descriptions**

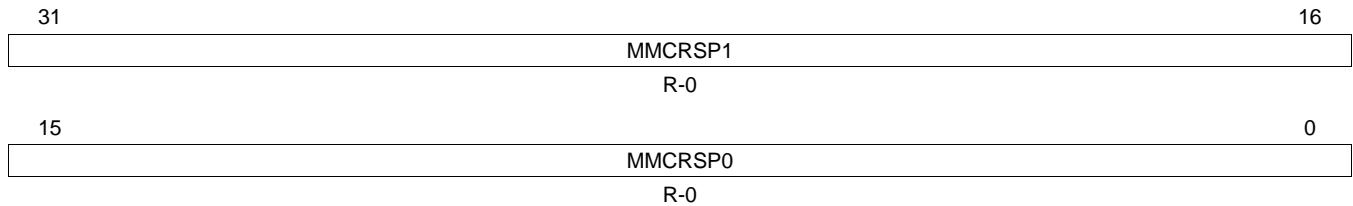
Bit	Field	Value	Description
31-0	ARGHL	0-FFFF FFFFh	Argument, high and low parts.

#### 4.15 MMC Response Registers (MMCRSP01-MMCRSP67)

Each command has a preset response type. When the MMC controller receives a response, it is stored in some or all of the 4 MMC response registers (MMCRSP01-MMCRSP67). The response registers are updated as the responses arrive, even if the CPU has not read the previous contents.

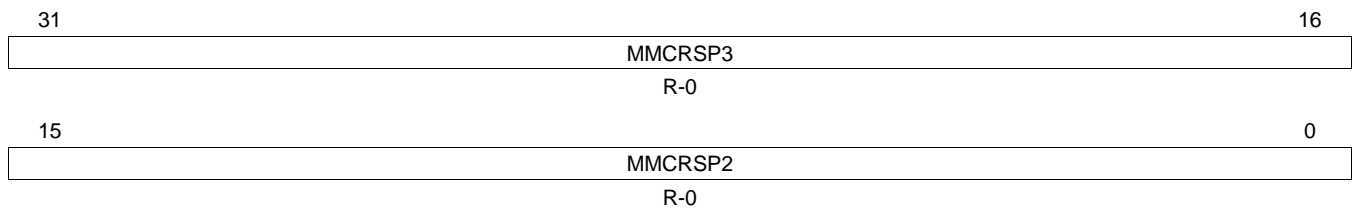
As shown in [Figure 32](#), [Figure 33](#), [Figure 34](#), and [Figure 35](#) each of the MMC response registers holds up to 32 bits. [Table 21](#) and [Table 22](#) show the format for each type of response and which MMC response registers are used for the bits of the response. The first byte of the response is a command index byte and is stored in the MMC command index register (MMCCIDX).

**Figure 32. MMC Response Register 01 (MMCRSP01)**



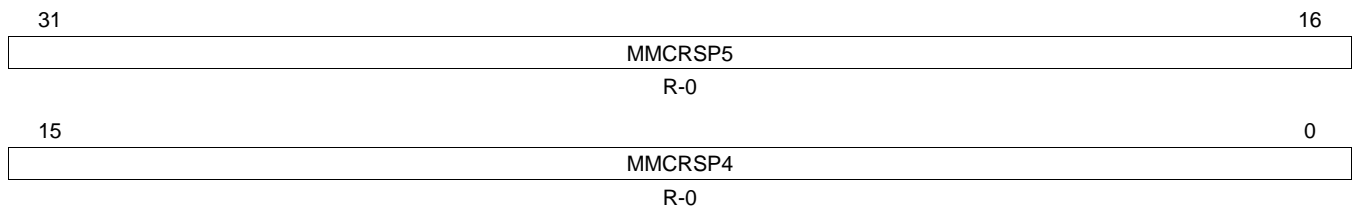
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Figure 33. MMC Response Register 23 (MMCRSP23)**



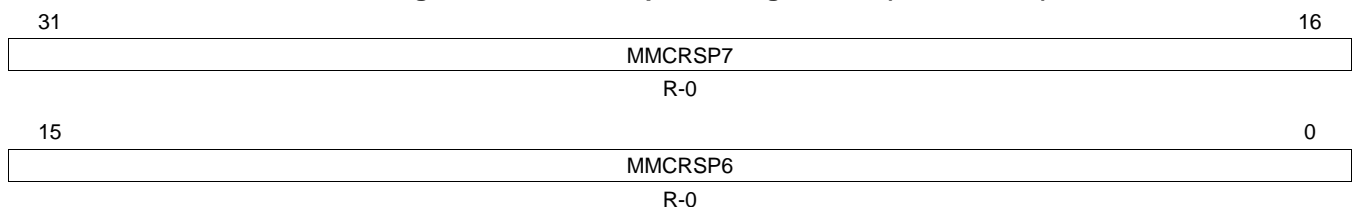
LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Figure 34. MMC Response Register 45 (MMCRSP45)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Figure 35. MMC Response Register 67 (MMCRSP67)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21. R1, R3, R4, R5, or R6 Response (48 Bits)**

<b>Bit Position of Response</b>	<b>Register</b>
47-40	MMCCIDX
39-24	MMCRSP7
23-8	MMCRSP6
7-0	MMCRSP5
-	MMCRSP4-0

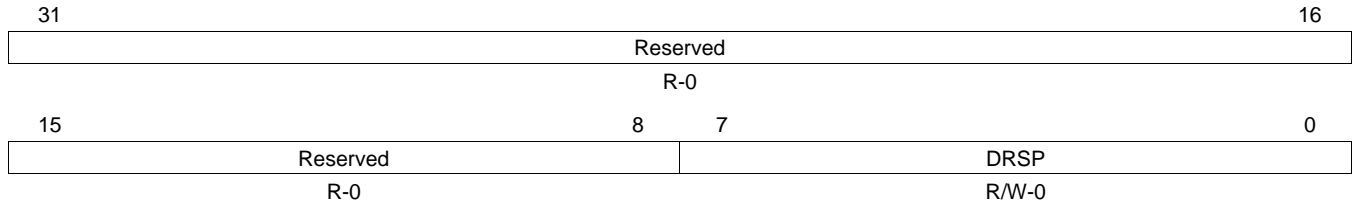
**Table 22. R2 Response (136 Bits)**

<b>Bit Position of Response</b>	<b>Register</b>
135-128	MMCCIDX
127-112	MMCRSP7
111-96	MMCRSP6
95-80	MMCRSP5
79-64	MMCRSP4
63-48	MMCRSP3
47-37	MMCRSP2
31-16	MMCRSP1
15-0	MMCRSP0

#### 4.16 MMC Data Response Register (MMCDRSP)

After the MMC controller sends a data block to a memory card, the CRC status from the memory card is stored in the CRC status register, shown in [Figure 36](#) and described in [Table 23](#).

**Figure 36. MMC Data Response Register (MMCDRSP)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

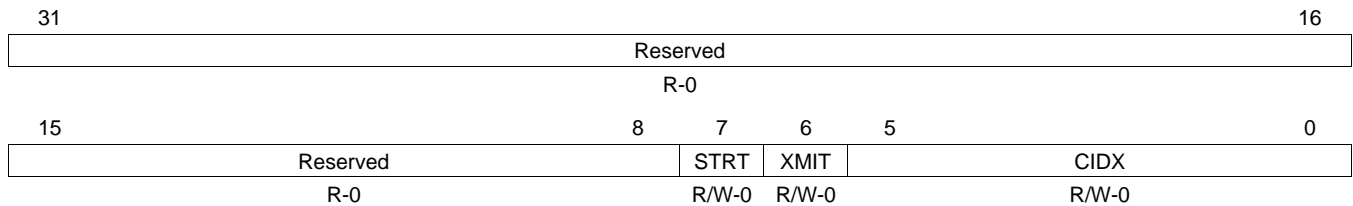
**Table 23. MMC Data Response Register (MMCDRSP) Field Descriptions**

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	DRSP	0-FFh	During a write operation (see <a href="#">Section 2.3.1</a> ), the CRC status token is stored in DRSP.

#### 4.17 MMC Command Index Register (MMCCIDX)

The MMC command index register (MMCCIDX) stores the first byte of a response from a memory card. [Table 21](#) and [Table 22](#) show the format for each type of response. MMCCIDX is shown in [Figure 37](#) and described in [Table 24](#).

**Figure 37. MMC Command Index Register (MMCCIDX)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

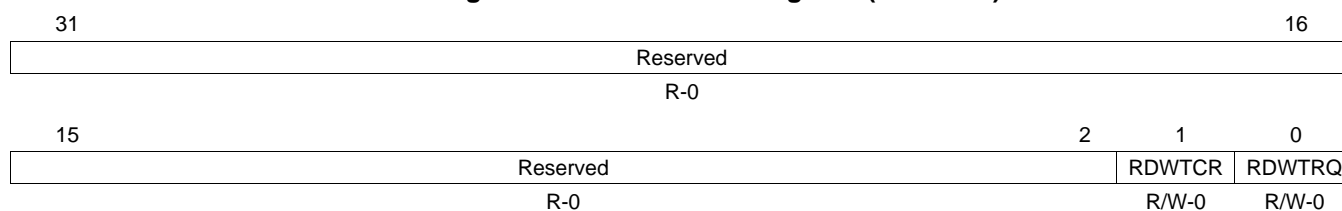
**Table 24. MMC Command Index Register (MMCCIDX) Field Descriptions**

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7	STRT	0-1	Start bit. When the MMC controller receives a response, the start bit is stored in STRT.
6	XMIT	0-1	Transmission bit. When the MMC controller receives a response, the transmission bit is stored in XMIT.
5-0	CIDX	0-3Fh	Command index. When the MMC controller receives a response, the command index is stored in CIDX.

#### 4.18 SDIO Control Register (SDIOCTL)

The SDIO control register (SDIOCTL) is shown in [Figure 38](#) and described in [Table 25](#).

**Figure 38. SDIO Control Register (SDIOCTL)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 25. SDIO Control Register (SDIOCTL) Field Descriptions**

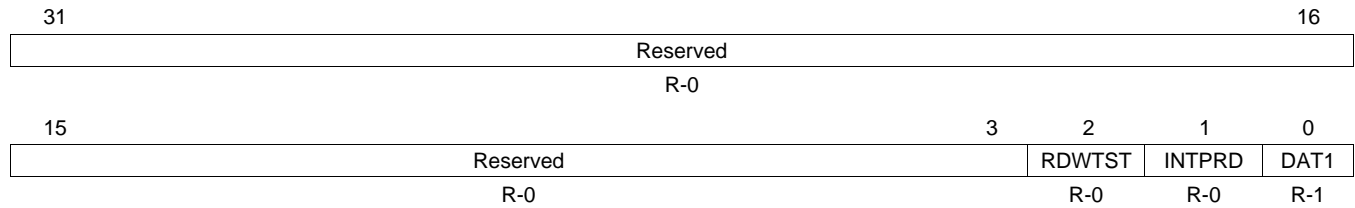
Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	RDWTCR	0 1	Read wait enable for CRC error. To end the read wait operation, write 0 to RDWTRQ. (No need to clear RDWTCR). Read wait is disabled. Automatically start read wait on CRC error detection during multiple block read access and not the last block to be transferred. RDWTRQ is automatically set to 1.
0	RDWTRQ	0 1	Read wait request. To end the read wait operation, write 0 to RDWTRQ. End read wait operation and release DAT[2]. Set a read wait request. Read wait operation starts 2 clocks after the end of the read data block. MMC interface asserts low level on DAT[2] until RDWTRQ is cleared to 0.



#### 4.19 SDIO Status Register 0 (SDIOST0)

The SDIO status register 0 (SDIOST0) is shown in [Figure 39](#) and described in [Table 26](#).

**Figure 39. SDIO Status Register 0 (SDIOST0)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

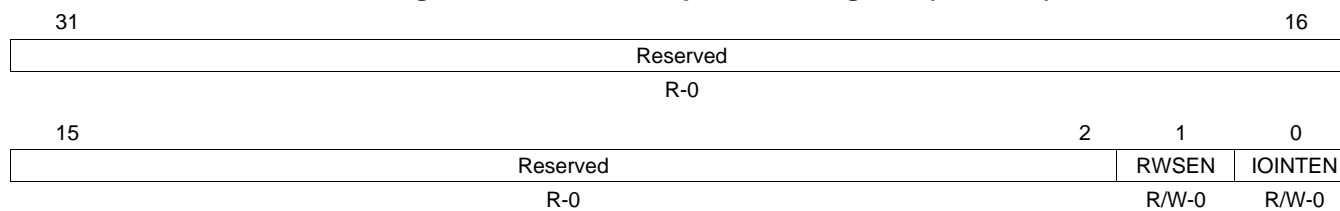
**Table 26. SDIO Status Register 0 (SDIOST0) Field Descriptions**

Bit	Field	Value	Description
31-3	Reserved	0	Reserved
2	RDWTST	0 1	Read wait status. Read wait operation not in progress. Read wait operation in progress.
1	INTPRD	0 1	Interrupt period. Interrupt not in progress. Interrupt in progress.
0	DAT1	0 1	This bit reflects the external state of the SD_DATA1 pin. Logic-low level on the SD_DATA1 pin. Logic-high level on the SD_DATA1 pin.

## 4.20 SDIO Interrupt Enable Register (SDIOIEN)

The SDIO interrupt enable register (SDIOIEN) is shown in [Figure 40](#) and described in [Table 27](#).

**Figure 40. SDIO Interrupt Enable Register (SDIOIEN)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

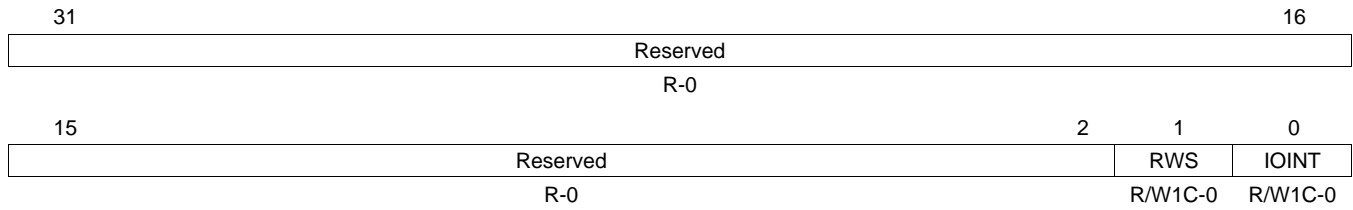
**Table 27. SDIO Interrupt Enable Register (SDIOIEN) Field Descriptions**

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	RWSEN	0	Read wait interrupt enable. Read wait interrupt is disabled.
		1	Read wait interrupt is enabled.
0	IOINTEN	0	SDIO card interrupt enable. SDIO card interrupt is disabled.
		1	SDIO card interrupt is enabled.

#### 4.21 SDIO Interrupt Status Register (SDIOIST)

The SDIO interrupt status register (SDIOIST) is shown in [Figure 41](#) and described in [Table 28](#).

**Figure 41. SDIO Interrupt Status Register (SDIOIST)**



LEGEND: R/W = Read/Write; R = Read only; W1C = Write 1 to clear (writing 0 has no effect); -n = value after reset

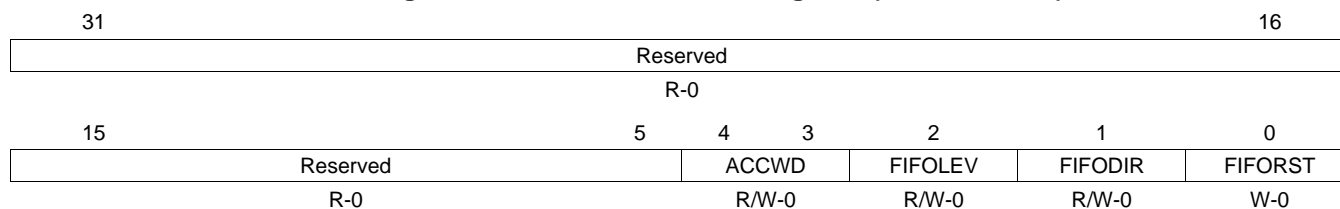
**Table 28. SDIO Interrupt Status Register (SDIOIST) Field Descriptions**

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	RWS	0	Read wait interrupt did not occur.
		1	Read wait interrupt occurred. Read wait operation starts and read wait interrupt is enabled (RWSEN = 1 in SDIOIEN).
0	IOINT	0	SDIO card interrupt did not occur.
		1	SDIO card interrupt occurred. SDIO card interrupt is detected and SDIO card interrupt is enabled (IOINTEN = 1 in SDIOIEN).

## 4.22 MMC FIFO Control Register (MMCFIFOCTL)

The MMC FIFO control register (MMCFIFOCTL) is shown in [Figure 42](#) and described in [Table 29](#).

**Figure 42. MMC FIFO Control Register (MMCFIFOCTL)**



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 29. MMC FIFO Control Register (MMCFIFOCTL) Field Descriptions**

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4-3	ACCWD	0-3h	Access width. Used by FIFO control to determine full/empty flag.
		0	CPU/EDMA access width of 4 bytes
		1	CPU/EDMA access width of 3 bytes
		2	CPU/EDMA access width of 2 bytes
		3	CPU/EDMA access width of 1 byte
2	FIFOLEV	0	FIFO level. Sets the threshold level that determines when the EDMA request and the FIFO threshold interrupt are triggered.
		1	EDMA request every 256 bits sent/received.
		1	EDMA request every 512 bits sent/received.
1	FIFODIR	0	FIFO direction. Determines if the FIFO is being written to or read from.
		0	Read from FIFO.
		1	Write to FIFO.
0	FIFORST	0	FIFO reset. Resets the internal state of the FIFO.
		0	FIFO reset is disabled.
		1	FIFO reset is enabled.

## Appendix A Revision History

This document has been revised to include the following technical change(s).

**Table 30. Revisions**

<b>Location</b>	<b>Additions/Modifications/Deletions</b>
<a href="#">Section 4.4</a>	Added MMC Status Register 1 (MMCST1).

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