TMS320C5515/14/05/04/VC05/VC04 DSP Timer/Watchdog Timer

User's Guide

Literature Number: SPRUFO2
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About This Manual

This document provides an overview of the three 32-bit timers in the TMS320C5515/14/05/04/VC05/VC04 digital signal processor (DSP). The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer2 contains both a CP and a Watchdog (WD) timer.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C5515/14/05/04 Digital Signal Processor (DSP) Digital Signal Processor (DSP). Copies of these documents are available on the internet at http://www.ti.com.

SWPU073 — TMS320C55x 3.0 CPU Reference Guide. This manual describes the architecture, registers, and operation of the fixed-point TMS320C55x digital signal processor (DSP) CPU.

SPRU652 — TMS320C55x DSP CPU Programmer's Reference Supplement. This document describes functional exceptions to the CPU behavior.

SPRUFO0 — TMS320VC5505/5504 Digital Signal Processor (DSP) Universal Serial Bus 2.0 (USB) User's Guide. This document describes the universal serial bus 2.0 (USB) in the TMS320VC5505/5504 Digital Signal Processor (DSP). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices.

SPRUFO1 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Inter-Integrated Circuit (I2C) Peripheral User's Guide. This document describes the inter-integrated circuit (I2C) peripheral in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The I2C peripheral provides an interface between the device and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFO2 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Timer/Watchdog Timer User's Guide. This document provides an overview of the three 32-bit timers in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer 2 can be configured as a GP, a Watchdog (WD), or both simultaneously.

SPRUFO3 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Serial Peripheral Interface (SPI) User's Guide. This document describes the serial peripheral interface (SPI) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only.

SPRUFO4 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) General-Purpose Input/Output (GPIO) User's Guide. This document describes the general-purpose input/output (GPIO) on the TMS320VC5505/5504 digital signal processor (DSP). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.

SPRUFO5 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Universal Asynchronous Receiver/Transmitter (UART) User's Guide. This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.

SPRUFO6 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide. This document describes the Multimedia Card (MMC)/Secure Digital (SD) Card Controller on the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards.

SPRUF07 — TMS320VC5505/5504 Digital Signal Processor (DSP) Real-Time Clock (RTC) User's Guide. This document describes the operation of the Real-Time Clock (RTC) module in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The RTC also has the capability to wake-up the power management and apply power to the rest of the device through an alarm, periodic interrupt, or external WAKEUP signal.

SPRUFO8 — TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) External Memory Interface (EMIF) User's Guide. This document describes the operation of the external memory interface (EMIF) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The purpose of the EMIF is to provide a means to connect to a variety of external devices.

SPRUFO9 — TMS320VC5505/5504 Digital Signal Processor (DSP) Direct Memory Access (DMA) Controller User's Guide. This document describes the features and operation of the DMA controller that is available on the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

SPRUFP0 — TMS320VC5505 Digital Signal Processor (DSP) System User's Guide. This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUGL6 — TMS320VC5504 Digital Signal Processor (DSP) System User's Guide. This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUFP1 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Successive Approximation (SAR) Analog to Digital Converter (ADC) User's Guide. This document provides an overview of the Successive Approximation (SAR) Analog to Digital Converter (ADC) on the TMS320VC5505/5504 Digital Signal Processor (DSP). The SAR is a 10-bit ADC using a switched capacitor architecture which converts an analog input signal to a digital value.

SPRUFP3 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Liquid Crystal Display Controller (LCDC) User's Guide. This document describes the liquid crystal display controller (LCDC) in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. The LCD controller includes a LCD Interface Display Driver (LIDD) controller.

SPRUFP4 — TMS320VC5505/5504 Digital Signal Processor (DSP) Inter-IC Sound (I2S) Bus User's Guide. This document describes the features and operation of Inter-IC Sound (I2S) Bus in the TMS320VC5505/5504 Digital Signal Processor (DSP) device. This peripheral allows serial transfer of full duplex streaming data, usually streaming audio, between DSP and an external I2S peripheral device such as an audio codec.

32-Bit Timer/Watchdog Timer

1 Introduction

This document describes the operation of the three 32-bit software programmable timers in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP). Each timer can be used as a general-purpose (GP) timer. Timer2 also contains a 16-bit Watchdog (WD) which shares the same clock gating bit as the GP but works independently.

1.1 Purpose of the Timers

General purpose timers are typically used to provide interrupts to the CPU to schedule periodic tasks or a delayed task. The general-purpose (GP) timers are 32-bit timers with a 13-bit prescaler that divides the CPU system clock and uses this scaled value as a reference clock. These timers can be used to generate periodic interrupts.

Watchdog timers are used to reset the CPU in the event of a deadlocked state, such as a non-exiting code loop. C5505 includes a timer that functions as a timer or a watchdog timer simultaneously, Timer2. This C5505's watchdog timer is a 32-bit timer composed of a 16-bit counter with a 16-bit prescaler that divides the CPU system clock and uses this scaled value as a reference clock. The programmer must continuously service the watchdog timer to prevent it from resetting the device. Once the code fails to service the watchdog timer due to a deadlock or non-exiting code loop, the watchdog expires and resets the device.

1.2 Features

32-bit Timers:

- 32-bit programmable count down timer.
- 13-bit prescaler divider.
- Auto reload option.
- Generates a single interrupt to the CPU. The interrupt is individually latched to determine which timer triggered the interrupt.
- Interrupt can be used for DMA event.

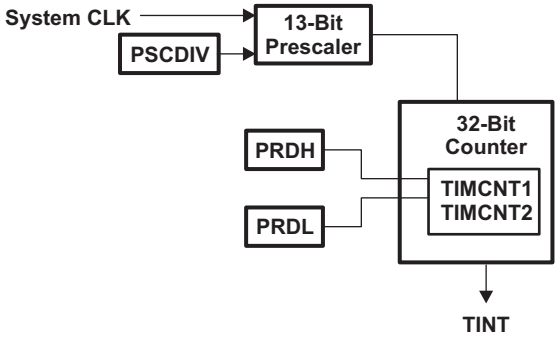
Watchdog Timer:

- 16-bit programmable count down timer
- 16-bit prescaler divider
- Lock registers require a specific sequence of keys to enable and change the watchdog settings. These sequence of keys prevent loose pointers from corrupting the state of the watchdog.
- Generated an active low pulse to the hardware reset when the Watchodg timer expires.

1.3 Functional Timer Block Diagram

A block diagram of the timer is shown in Figure 1. Detailed information about the architecture and operation of the timers is in Section 3.

Figure 1. The Architecture and Operation of the GP Timers



2 General-Purpose Timer

All three timers (Timer0, Timer1, and Timer2) can be used as GP timers. Timer2 can also be used as a WD timer. To use the WD timer see Section 3.

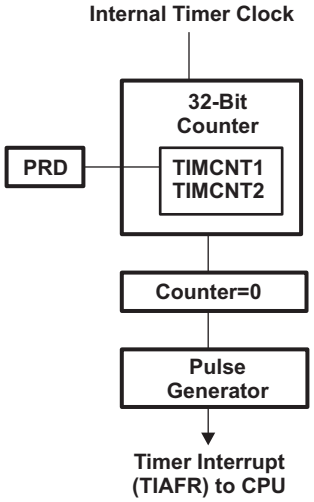
2.1 General-Purpose Timer Clock Control

The clock source to the GP timer and to the WD timer is driven by the system clock. This clock source determines the speed of the timer since the timer counts down in units of source clock cycles. The source clock for the GP timer can be divided down by a 13-bit prescaler and uses this scaled value as the reference clock to the timer. Each GP timer has its own 13-bit prescaler. When determining the period and prescaler setting for the timer, choose the desired period in units of source clock cycles.

2.2 Using the 32-bit General Purpose Timer

The general-purpose timers consist of a 32-bit timer with a 13-bit prescaler. Figure 2 shows a high-level diagram of the timer.

Figure 2. 32-Bit GP Timer With a 13-Bit Prescaler



Each GP timer has a count register (TIMCNT*n*) which consists of two 16-bit words (TIMCNT1 and TIMCNT2) and a period register (TIMPRD*n*) which also consists of two 16-bit words (TIMPRD1 and TIMPRD2). When the timer is set to start the contents of the TIMPRD*n* register is loaded into the TIMCNT register and begins to count down. A timer control register (TCR) controls the operation of the timer.

The Prescaler Divider (PSCDIV), located in the TCR, is used to divide the internal CPU clock.

When the START bit is set to 1 in the TCR, the contents of the Timer Period Registers (TIMPRD1 and TIMPRD2) are loaded into the concatenated Timer Counter Registers (TIMCNT1 and TIMCNT2) and the timer starts to count down with every cycle of the prescale divided clock. When TIMCNT1 and TIMCNT2 reach 0, the timer sends an interrupt request (TINT) to the CPU and a DMA event to the four DMA's.

The timer can be configured in auto-reload mode by setting the AUTORELOAD bit in the TCR. In this mode, the timer counter is reloaded with the timer period register when the timer counter reaches 0 and the timer re-starts its count down.

3 Watchdog Timer

This section describes the timer in the watchdog (WD) timer mode. Only Timer2 can be used as a Watchdog timer. This timer can also be used as general-purpose timer. To use it as a general-purpose timer, see Section 2.

3.1 Watchdog Timer Function

The watchdog timer function consists of a 16-bit main counter preceded by 16-bit prescaler. The combination of the 16-bit counter with the 16-bit prescaler allows for a maximum countdown value of 4,294,967,296. As a watchdog, the timer can be used to prevent system lockup when the software becomes deadlocked or trapped in a loop with no controlled exit. When the counter expires, a hardware reset is generated. To prevent the hardware reset from being generated, the watchdog must be serviced periodically before the counter expires. The service reinitializes the counter to its starting value and starts counting down again.

After a hardware reset occurs, the watchdog timer is disabled, allowing a flexible period of time for code to be loaded into the on-chip memory. To configure the watchdog timer, each control register has a corresponding lock register that requires a specific key sequence (with two or three keys written in order) to unlock that control register. Once the appropriate key sequence has been written to the lock register, then the corresponding control register is unlocked and can be written. After the control register is written, it is automatically locke. To write the register, the sequence must be repeated to unlock the register. If the wrong value is written for any of the keys, then it is necessary to restart at the first key. Each control and lock register pair has its own state machine to keep track of the key sequence. Therefore, it is possible to write the 1st key to each of the 4 lock registers, and then proceed to write the 2nd key to each of the 4 lock registers, and so on until all of the keys have been written. In other words, each control register must have it's specific keys written in order; but the CPU can perform other things while writing the keys in order. In the watchdog timer mode, the timer requires a periodic execution of this unlock/write sequence to reinitialize the watchdog counter to its starting value. Without this periodic servicing, the watchdog timer counter reaches zero and causes a watchdog timeout event.

When the timeout event occurs, the watchdog timer resets the entire chip with the exception of the RTC (real time clock).

3.2 Watchdog Timer Operation

The Watchdog (WD) timer function is enabled when:

- The Start Value and Prescale registers have been unlocked.
- The Start Value and Prescale registers have been programmed.
- The Watchdog Enable Lock register is unlocked.
- A 1 is written to bit 0 of the Watchdog Enable register.

There are example codes in the Chip Support Library (CSL) on how to program GP and WD timers. After the Watchdog timer is enabled, a write to the Watchdog Kick register when it is unlocked starts the count down. To enable the watchdog timer, a certain sequence of events must be followed. First, to configure the watchdog timer, each control register has a lock register that requires a specific key sequence (with two or three keys written in the proper order) to unlock the corresponding control register. Table 1 details the unlock sequence for the watchdog lock registers:

Table 1. Unlock Sequence for the Watchdog Lock Registers

Address	Register	First Key Sequence	Second Key Sequence	Third Key Sequence
1880h	Watchdog Kick Lock Register	5555h	AAAAh	n/a
1884h	Watchdog Start Value Lock Register	6666h	BBBBh	n/a
1888h	Watchdog Enable Lock Register	7777h	CCCCh	DDDDh
188Ch	Watchdog Prescale Lock Register	5A5Ah	A5A5h	n/a

Once the Start Value and Prescale register have been unlocked with their corresponding two word sequence and programmed for the desired interval, the Watchdog is enabled by unlocking the Enable Lock Register with a sequence of three words (7777h, CCCCh, and DDDDh) and writing a 1 on the EN bit (bit 0) of the WDEN register. The Watchdog starts counting down by unlocking the Kick Lock register and writing any value into the Kick register. At this time, the counter starts to count down from the programmed start value. The Watchdog counts down by first decrement the Prescale register by one with each CPU clock cycle. After the watchdog Prescale register reaches 0, the internal watchdog counter register is decremented by one and the Prescale register restarts its countdown from its programmed value. The counter will reach zero when the counter value and pre-scalar value are exhausted, consequently, triggering a hardware reset of the device. To prevent the hardware reset from occurring, the Kick Lock register must be unlocked and the Kick register bit 0 set to 1 to restart the countdown before the countdown is exhausted.

Once the Watchdog is enabled, it can be disabled with software by unlocking the Enable Lock Register with the three word sequence and setting the EN bit (bit 0) of the WDEN register to 0.

4 Reset Considerations

The timers will be reset upon a hardware reset. The timers may also be reset by software reset (see PER_RESET). However, the timer interrupt aggregation flag register (TIAFR) is not affected by software reset of the timers.

4.1 Hardware Reset Considerations

When a hardware reset is asserted, all timer registers, including the TIAFR register, are set to their default values.

5 Interrupt Support

The general-purpose timer has a timer interrupt signal. The timer interrupt request is sent to the CPU when the main count register (TIMCNT1 and TIMCNT2) counts down to 0. The same interrupt signal is also routed to the DMAs and can be used as a DMA trigger event.

The TIAFR latches each timer's interrupt signal when the timer counter expires. Using this register, the programmer can determine which of the three timers generated the timer interrupt since the bits in the TIAFR are OR'ed together and sent to the DSP as a single interrupt. Each timer interrupt flag needs to be cleared by the CPU with a write of "1" to the corresponding flag bit.

6 Registers

Table 2 through Table 6 list the memory mapped registers associated with the 3 Timers.

The timer registers can be accessed by the CPU at the 16-bit addresses.

Table 2. Watchdog Timer Registers

CPU Word Address	Acronym	Register Description	Section
1880h	WDKCKLK	Watchdog Kick Lock Register	Section 6.1
1882h	WDKICK	Watchdog Kick Register	Section 6.2
1884h	WDSVLR	Watchdog Start Value Lock Register	Section 6.3
1886h	WDSVR	Watchdog Start Value Register	Section 6.4
1888h	WDENLOK	Watchdog Enable Lock Register	Section 6.5
188Ah	WDEN	Watchdog Enable Register	Section 6.6
188Ch	WDPSLR	Watchdog Prescale Lock Register	Section 6.7
188Eh	WDPS	Watchdog Prescale Register	Section 6.8

Table 3. General-Purpose Timer 0 Registers

CPU Word Address	Acronym	Register Description	Section
1810h	TCR	Timer 0 Control Register	Section 6.9
1812h	TIMPRD1	Timer 0 Period Register 1	Section 6.10
1813h	TIMPRD2	Timer 0 Period Register 2	Section 6.11
1814h	TIMCNT1	Timer 0 Counter Register 1	Section 6.12
1815h	TIMCNT2	Timer 0 Counter Register 2	Section 6.13

Table 4. General-Purpose Timer 1 Registers

CPU Word Address	Acronym	Register Description	Section
1850h	TCR	Timer 1 Control Register	Section 6.9
1852h	TIMPRD1	Timer 1 Period Register 1	Section 6.10
1853h	TIMPRD2	Timer 1 Period Register 2	Section 6.11
1854h	TIMCNT1	Timer 1 Counter Register 1	Section 6.12
1855h	TIMCNT2	Timer 1 Counter Register 2	Section 6.13

Table 5. General-Purpose Timer 2 Registers

CPU Word Address	Acronym	Register Description	Section
1890h	TCR	Timer 2 Control Register	Section 6.9
1892h	TIMPRD1	Timer 2 Period Register 1	Section 6.10
1893h	TIMPRD2	Timer 2 Period Register 2	Section 6.11
1894h	TIMCNT1	Timer 2 Counter Register 1	Section 6.12
1895h	TIMCNT2	Timer 2 Counter Register 2	Section 6.13

Table 6. Timer Interrupt Aggregation Register

CPU Word Address	Acronym	Register Description	Section
1C14h	TIAFR	Timer Interrupt Aggregation Flag Register	Section 6.14

6.1 Watchdog Kick Lock Register (WDKCKLK)

The watchdog kick lock register (WDKCKLK) is shown in Figure 3 and described in Table 7.

Figure 3. Watchdog Kick Lock Register (WDKCKLK)

15	0
KICKLOK	
RW-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 7. Watchdog Kick Lock Register (WDKCKLK) Field Descriptions

Bit	Field	Value	Description
15-0	KICKLOK	0-FFFFh	Used to unlock the Watchdog Kick Register. A 2 word key sequence must be written to this register. The following keys must be written in this order: Key 1 = 5555h and Key 2 = AAAAh. When this is written, the Kick register can now be written. When reading back the WDKCKLK register, the value that is returned in bits [1:0] give the current state of the lock state machine where 00 = Idle/waiting for Key 1; 01 = Waiting for key 2; 11 = unlocked.

6.2 Watchdog Kick Register (WDKICK)

The watchdog kick register (WDKICK) is shown in Figure 4 and described in Table 8.

Figure 4. Watchdog Kick Register (WDKICK)

15	0
KICK	
RW-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 8. Watchdog Kick Register (WDKICK) Field Descriptions

Bit	Field	Value	Description
15-0	KICK	0-FFFFh	A write to the kick register when it is unlocked causes the Watchdog counter to be reloaded with the value in the WD Start Value register and start counting down again. It does not matter what value is written. Reading the register returns the current value of the counter.

6.3 Watchdog Start Value Lock Register (WDSVLR)

The watchdog start value lock register (WDSVLR) is shown in Figure 5 and described in Table 9.

Figure 5. Watchdog Start Value Lock Register (WDSVLR)

15	0
STVALLOK	
RW-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9. Watchdog Start Value Lock Register (WDSVLR) Field Descriptions

Bit	Field	Value	Description
15-0	STVALLOK	0-FFFFh	Used to unlock the Watchdog Start Value Register. A 2 word key sequence must be written to this register. The following keys must be written in this order: Key 1 = 6666h and Key 2 = BBBBh. When this is written, the WD Start Value register can now be input. When reading back the WDSVLR register, the value that is returned in bits [1:0] give the current state of the lock state machine where 00 = Idle/waiting for Key 1; 01 = Waiting for key 2; 11 = unlocked.

6.4 Watchdog Start Value Register (WDSVR)

The watchdog start value register (WDSVR) is shown in Figure 6 and described in Table 10.

Figure 6. Watchdog Start Value Register (WDSVR)

15	0
STRTVAL	
RW-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10. Watchdog Start Value Register (WDSVR) Field Descriptions

Bit	Field	Value	Description
15-0	STRTVAL	0-FFFFh	The value written to this register is what is loaded into the WD counter when the kick register is written to. A read of this register will return the Start Value for the counter.

6.5 Watchdog Enable Lock Register (WDENLOK)

The watchdog enable lock register (WDENLOK) is shown in Figure 7 and described in Table 11.

Figure 7. Watchdog Enable Lock Register (WDENLOK)

15	0
ENLOK	
RW-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11. Watchdog Enable Lock Register (WDENLOK) Field Descriptions

Bit	Field	Value	Description
15-0	ENLOK	0-FFFFh	Used to unlock the Watchdog Enable Register. A 3 word key sequence must be written to this register. The following keys must be written in this order: Key 1 = 7777h, Key 2 = CCCCh, and Key 3 = DDDDh. When this is written, the WDENLOK register can now be input. When reading back the WDENLOK register, the value that is returned in bits [1:0] give the current state of the lock state machine where 00 = Idle/waiting for Key 1; 01 = Waiting for key 2; 10 = Waiting for Key 3; 11 = unlocked.

6.6 Watchdog Enable Register (WDEN)

The watchdog enable register (WDEN) is shown in Figure 8 and described in Table 12.

Figure 8. Watchdog Enable Register (WDEN)

15	1	0
Reserved		EN
R-0		RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

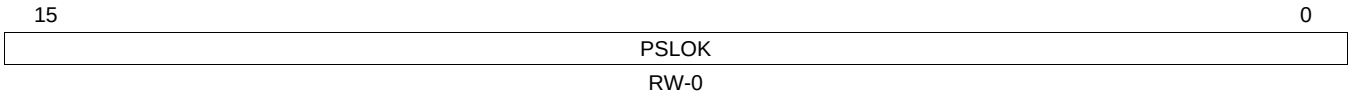
Table 12. Watchdog Enable Register (WDEN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved
0	EN		used to enable/disable the WD timer. When enabled, the counter begins counting down when the Watchdog Kick register is written, if the counter is allowed to reach 0 the chip will be reset.
		0	Watchdog Timer is disabled
		1	Watchdog Timer is enabled.

6.7 Watchdog Prescaler Lock Register (WDPSLR)

The watchdog prescaler lock register (WDPSLR) is shown in Figure 9 and described in Table 13.

Figure 9. Watchdog Prescaler Lock Register (WDPSLR)



LEGEND: R/W = Read/Write; -*n* = value after reset

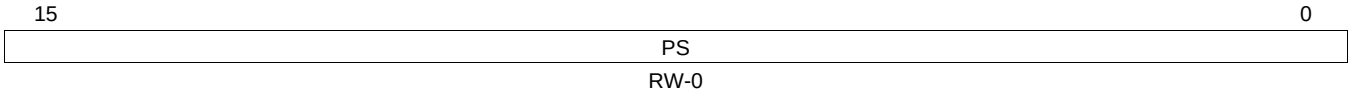
Table 13. Watchdog Prescaler Lock Register (WDPSLR) Field Descriptions

Bit	Field	Value	Description
15-0	PSLOK	0-FFFFh	Used to unlock the Watchdog Prescaler Register. A 2 word key sequence must be written to this register. The following keys must be written in this order: Key 1 = 5A5Ah and Key 2 = A5A5h. When this is written, the WDPSLR register can now be loaded. When reading back the WDPSLR register, the value that is returned in bits [1:0] give the current state of the lock state machine where 00 = Idle/waiting for Key 1; 01 = Waiting for key 2; 11 = unlocked.

6.8 Watchdog Prescaler Register (WDPS)

The watchdog prescaler register (WDPS) is shown in Figure 10 and described in Table 14.

Figure 10. Watchdog Prescaler Register (WDPS)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 14. Watchdog Prescaler Register (WDPS) Field Descriptions

Bit	Field	Value	Description
15-0	PS	0-FFFFh	The WD Prescaler register stores the start value for the WD Prescaler. Each time the PS register counts down to 0 the WD counter is decremented by 1. A read will return the last value written to this register (the Prescaler start value)

6.9 Timer n Control Register (TCR)

The timer *n* control register (TCR) is shown in Figure 11 and described in Table 15.

Figure 11. Timer *n* Control Register (TCR)

15	14 6	5 2	1	0
TIMEN	Reserved	PSCDIV	AUTORELOAD	START
RW-0	R-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

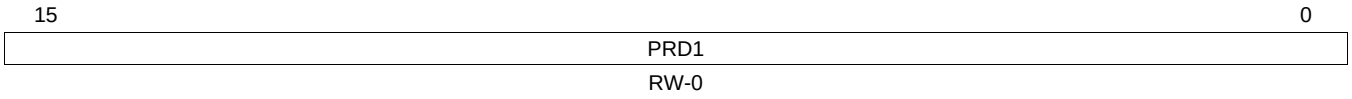
Table 15. Timer *n* Control Register (TCR) Field Descriptions

Bit	Field	Value	Description
15	TIMEN		This enables/disables both the Prescaler and the main counter.
		0	Timer counters are disabled
		1	Timer counters and prescaler are enabled
14-6	Reserved	0	Reserved.
5-2	PSCDIV	0-Fh	Prescaler divider. The range is 0000 = divide by 2 to 1100 = divide by 8192
1	AUTORELOAD		automatically reloads the counter when it reaches 0
		0	Auto Reload is disabled
		1	Auto Reload is enabled
0	START	0	When written to this bit loads and starts the counter.
		0	Stops the countdown
		1	Loads and starts the counter to counting down

6.10 Timer n Period Register 1 (TIMPRD1)

The timer *n* period register 1 (TIMPRD1) is shown in Figure 12 and described in Table 16.

Figure 12. Timer *n* Period Register 1 (TIMPRD1)



LEGEND: R/W = Read/Write; -*n* = value after reset

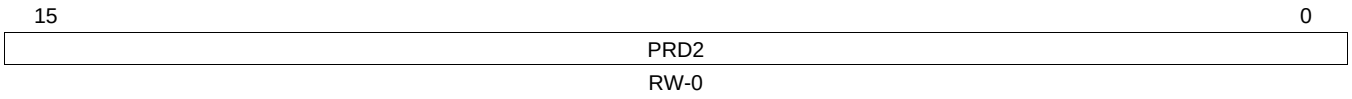
Table 16. Timer *n* Period Register 1 (TIMPRD1) Field Descriptions

Bit	Field	Value	Description
15-0	PRD1	0-FFFFh	The Timer period register is 32 bits wide. This is the LSW for the Timer period.

6.11 Timer n Period Register 2 (TIMPRD2)

The timer *n* period register 2 (TIMPRD2) is shown in Figure 13 and described in Table 17.

Figure 13. Timer *n* Period Register 2 (TIMPRD2)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 17. Timer *n* Period Register 2 (TIMPRD2) Field Descriptions

Bit	Field	Value	Description
15-0	PRD2	0-FFFFh	The Timer period register is 32 bits wide. This is the MSW for the Timer period.

6.12 Timer n Counter Register 1 (TIMCNT1)

The timer *n* counter register 1 (TIMCNT1) is shown in Figure 14 and described in Table 18.

Figure 14. Timer *n* Counter Register 1 (TIMCNT1)

15	0
TIM1	
RW-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 18. Timer *n* Counter Register 1 (TIMCNT1) Field Descriptions

Bit	Field	Value	Description
15-0	TIM1	0-FFFFh	The timer is 32bits wide. This is the LSW for the timer counter

6.13 Timer n Counter Register 2 (TIMCNT2)

The timer *n* counter register (TIMCNT2) is shown in Figure 15 and described in Table 19.

Figure 15. Timer *n* Counter Register (TIMCNT2)

15	0
TIM2	
RW-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 19. Timer *n* Counter Register (TIMCNT2) Field Descriptions

Bit	Field	Value	Description
15-0	TIM2	0-FFFFh	The timer is 32bits wide. This is the MSW for the timer counter

6.14 Timer Interrupt Aggregation Flag Register (TIAFR)

The timer interrupt aggregation flag register latches each timer (Timer0, Timer1, and Timer2) interrupt signal when the timer counter expires. Using this register, the programmer can determine which Timer generated the single Timer CPU interrupt signal. Each Timer flag needs to be cleared by the CPU with a write of '1' to the corresponding flag bit. Note that the corresponding Timer Interrupt Register must also be cleared.

The Timer Interrupt Aggregation Flag Register (TIAFR) is shown in Figure 16 and described in Table 20.

Figure 16. Timer Interrupt Aggregation Flag Register (TIAFR)

15	3	2	1	0
Reserved		TIM2FLAG	TIM1FLAG	TIM0FLAG
R-0		R/W1C	R/W1C	R/W1C

LEGEND: R/W1C = Read/Write 1 to Clear; R = Read only; *-n* = value after reset

Table 20. Timer Interrupt Aggregation Flag Register (TIAFR) Field Description

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2	TIM2FLAG		Timer 2 interrupt flag bit. This bit latches the timer interrupt signal when the timer counter expires. You can clear this flag bit by writing a 1 to it.
		0	Timer has not generated an interrupt.
		1	Timer interrupt has occurred.
1	TIM1FLAG		Timer 1 interrupt flag bit. This bit latches the timer interrupt signal when the timer counter expires. You can clear this flag bit by writing a 1 to it.
		0	Timer has not generated an interrupt.
		1	Timer interrupt has occurred.
0	TIM0FLAG		Timer 0 interrupt flag bit. This bit latches the timer interrupt signal when the timer counter expires. You can clear this flag bit by writing a 1 to it.
		0	Timer has not generated an interrupt.
		1	Timer interrupt has occurred.

6.15 Clock Gating

Each timer has an individual clock gating control bit in Peripheral Clock Gating Configuration LSW Register (PCGCR) [0x1C02]. Timer0 is bit 10, Timer1 is bit 12 and Timer3 is bit 13. All timers are defaulted to active with value equals to "0".

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