MMWCAS-DSP-EVM

The MMWCAS-DSP-EVM is an evaluation platform utilizing the TDA2x high performance, multimedia application processor based on enhance OMAP architecture implemented with 28-nm technology. The MMWCAS-RF-EVM is a 4-device, cascaded, array of AWR1243P mmWave devices. This user guide references the MMWCAS-RF-EVM and Radar Board as the same items. Both boards together provide a full Radar system evaluation.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The MMWCAS-DSP-EVM is an evaluation platform utilizing the TDA2x high performance, multimedia application processor based on enhance OMAP architecture implemented with 28-nm technology.

The MMWCAS-DSP-EVM provides a processing foundation for a cascaded imaging radar system. Cascade radar devices can support front, long-range(LRR) beam-forming applications as well as corner and side-cascade radar and sensor fusion platforms. The EVM supports SSD storage for longer term capture scenarios and 1 Gigabit Ethernet connectivity for control and offloading captured data. The MMWCAS-DSP-EVM may also be referred to as DSP Board throughout this guide.

The EVM interfaces with a companion Cascade Radar EVM (MMWCAS-RF-EVM). The MMWCAS-RF-EVM is a 4-device, cascaded, array of AWR1243P mmWave devices. This user guide references the MMWCAS-RF-EVM and Radar Board as the same items. Both boards together provide a full Radar system evaluation.

1.1 Key Features

The key features of the MMWCAS-DSP-EVM are:

- TDA2SX ADAS SoC (23 mm × 23 mm)
- Four Lattice Crosslink Automotive Grade FPGAs
- 2GByte of DDR3L device
- PCIe 2.0 m.2 connector(m-keyed)
- MicroSD™ Card interface
- JTAG interface through FTDI FT2232HL Chip
- USB interface to provide UART, and I2C interfaces through the onboard FTDI device. This is used for mmWave Studio.
- User LEDs, 3 push-button switches, and 1×6DIP switches for user BOOT configurations
- 1Gb/s RGMII Ethernet interface with RJ45 jack
- Video- one HDMI Out
- Two HiRose 120-pin Automotive Rated Board-to-Board connectors
- 12-V DC input (Wall supply not included in kit)
- Optimized Power Management IC (PMIC) Solution
- Dimension (L × W): 160 mm × 136 mm
- Expansion connector to support AWR Cascade Radar EVM

1.2 Kit Contents

The following items are included with the MMWCAS-DSP-EVM kit. Unbox the board and identify various components and connectors as detailed in the user guide.

- MMWCAS-DSP-EVM Board
- 512GB NVMe PCIE m.2 2280 SSD(assembled on EVM)
- 16GB microSD Card
- Ethernet cable
- Power Cable assembly
- USBA to miniB Cable
- Mounting standoffs and screws

1.3 Thermal Compliance

There is elevated heat on the processor/heatsink; use caution at elevated ambient temperature. Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink.

Figure 1. Caution Hot Surface Warning located on EVM

2 Hardware Specifications

2.1 Functional Block Diagram

The functional block diagram of the MMWCAS-DSP-EVM is shown in Figure 2.

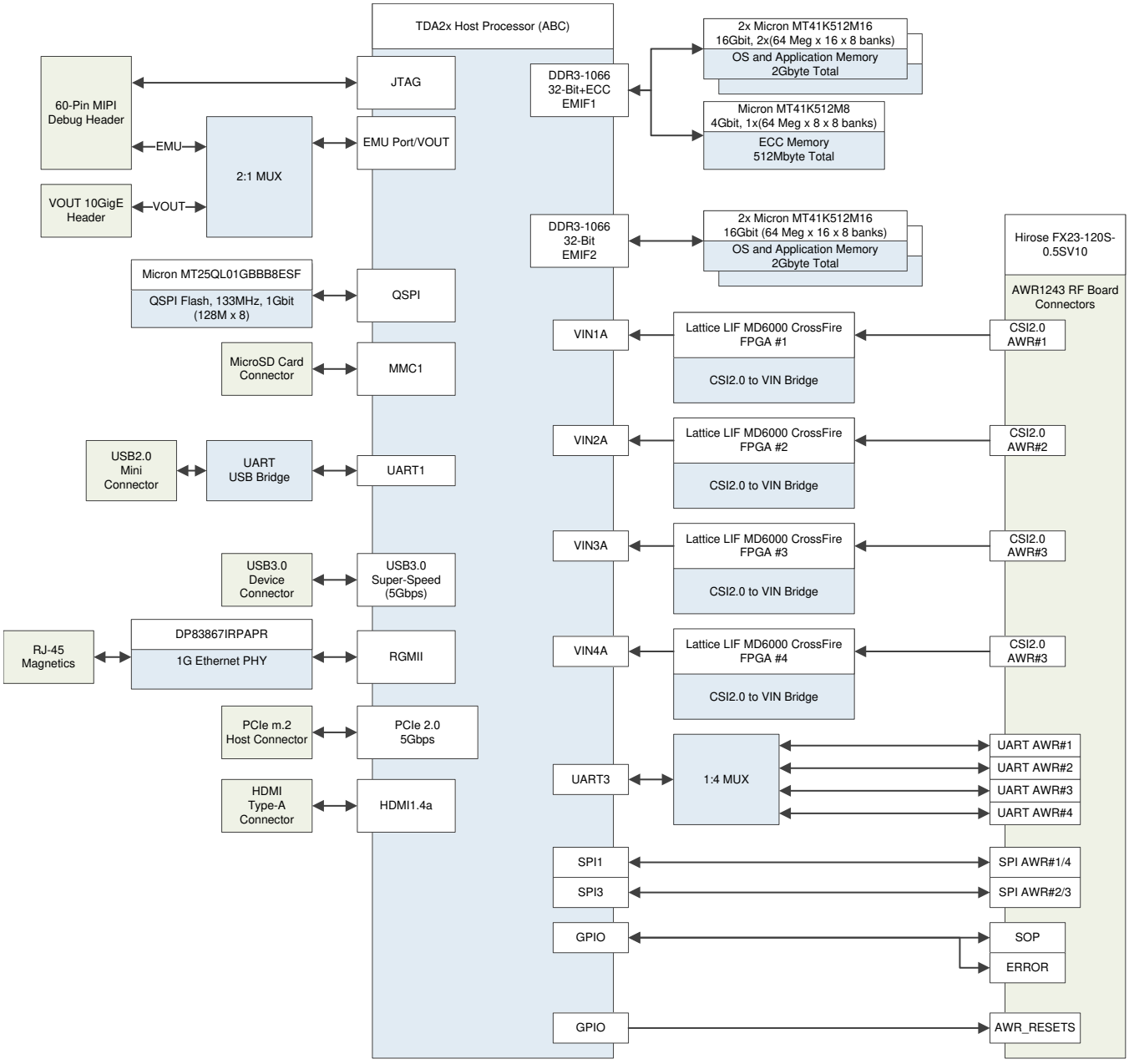

Figure 2. MMWCAS-DSP-EVM Functional Block Diagram

2.2 Board Dimensions & Description

The MMWCAS-DSP-EVM dimensions are 160 mm × 136 mm. It is a 22-layer board fabricated with epoxy fiberglass (UL94V-0 Certified). Figure 3 and Figure 4 show the top and bottom layers with key components identified.

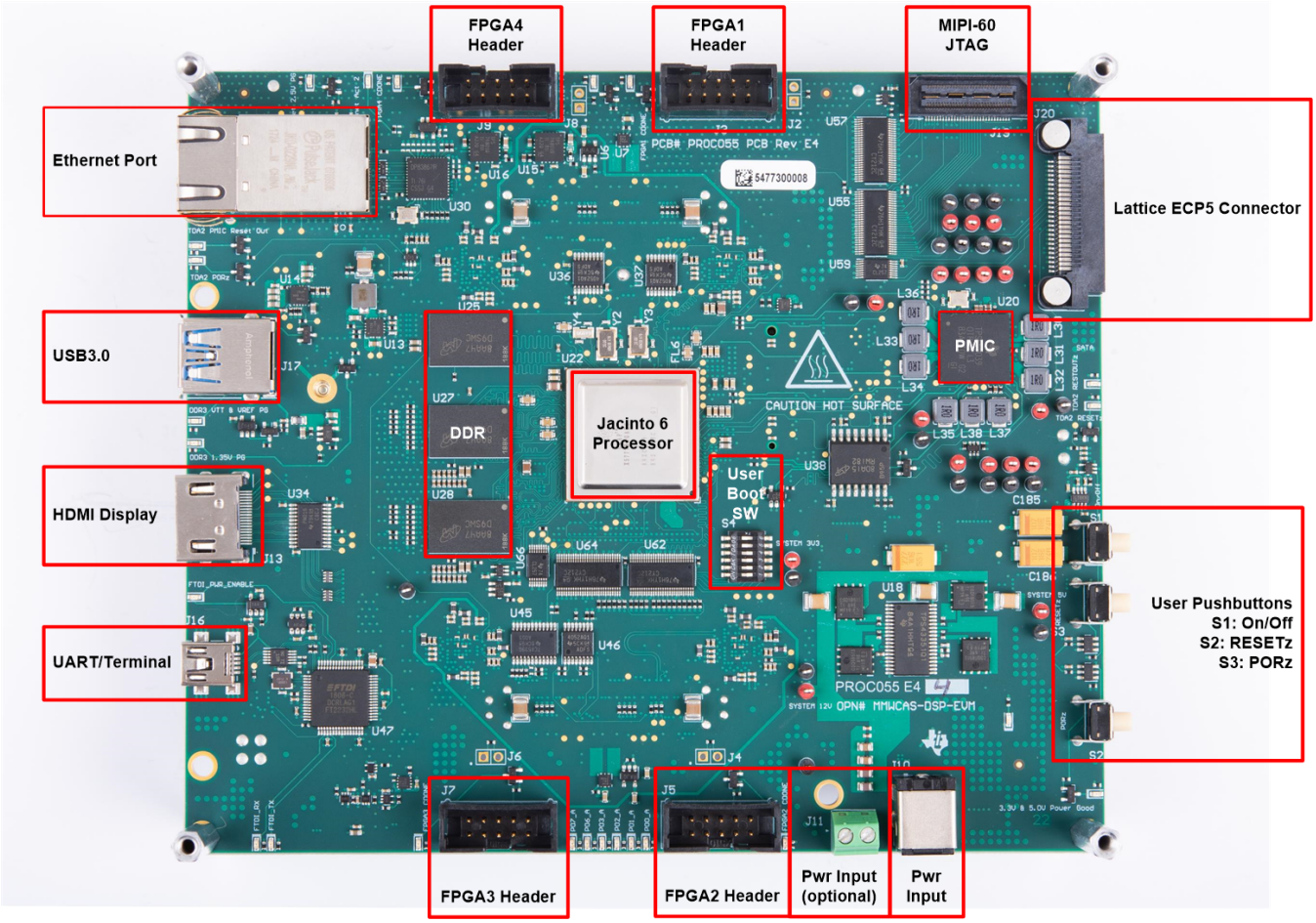

Figure 3. MMWCAS-DSP-EVM - Front

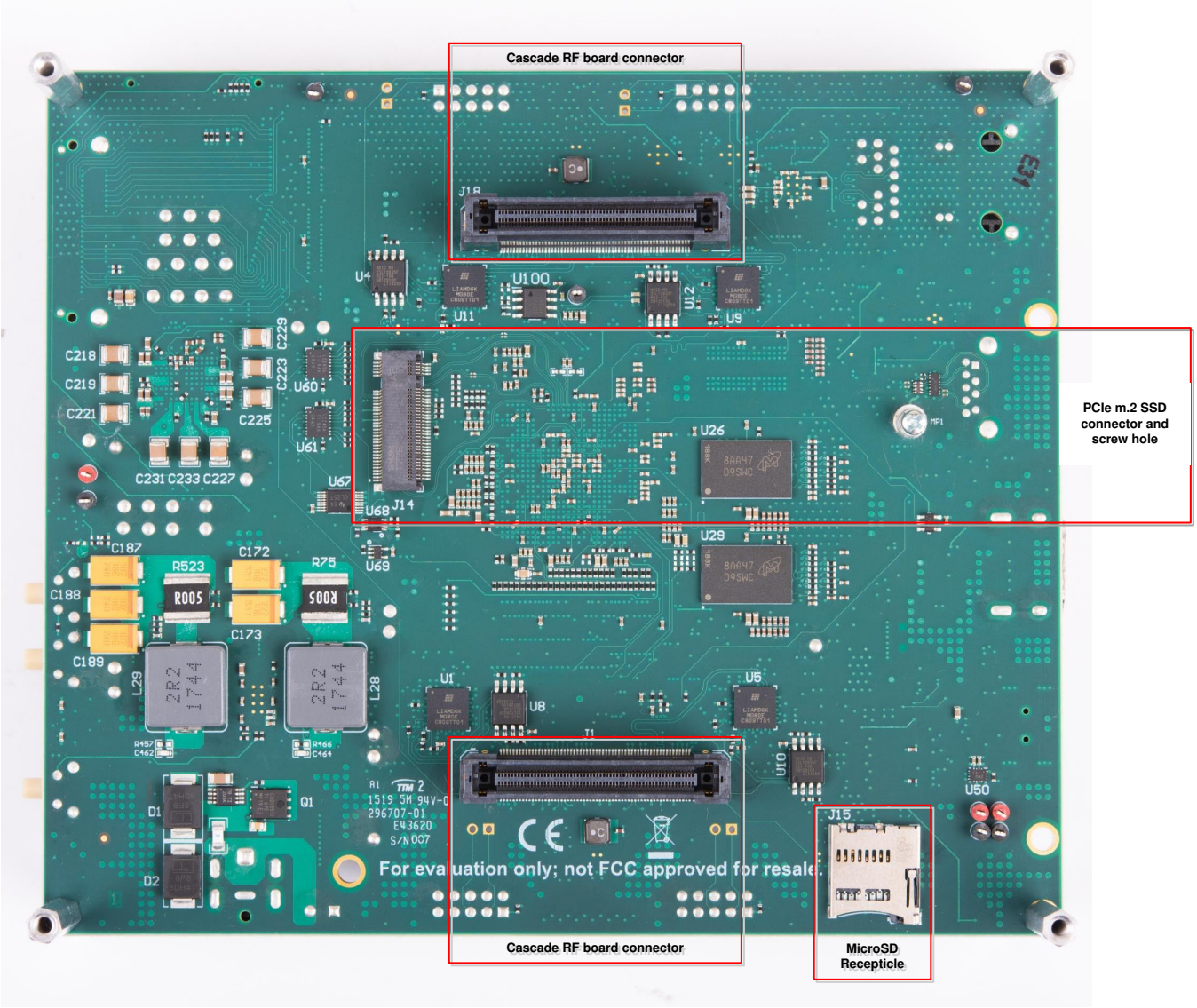

Figure 4. MMWCAS-DSP-EVM – Back

2.3 Attaching MMWCAS-DSP-EVM to MMWCAS-RF-EVM

The MMWCAS-DSP-EVM is designed to have a companion RF board attached to capture radar data. The EVM provides 5-V power and necessary control to the RF board upon connecting.

The boards align and attach through the board to board connectors (J1 and J18) on the EVM. The connectors are keyed to prevent incorrect, 180 degree, opposite orientation. The four corner mounting holes align the boards as well to outline the match. Depressing the RF board connectors into the EVM connectors connects the boards together. Use the included standoffs to secure a single assembly of the boards. Refer to Figure 5 for reference.

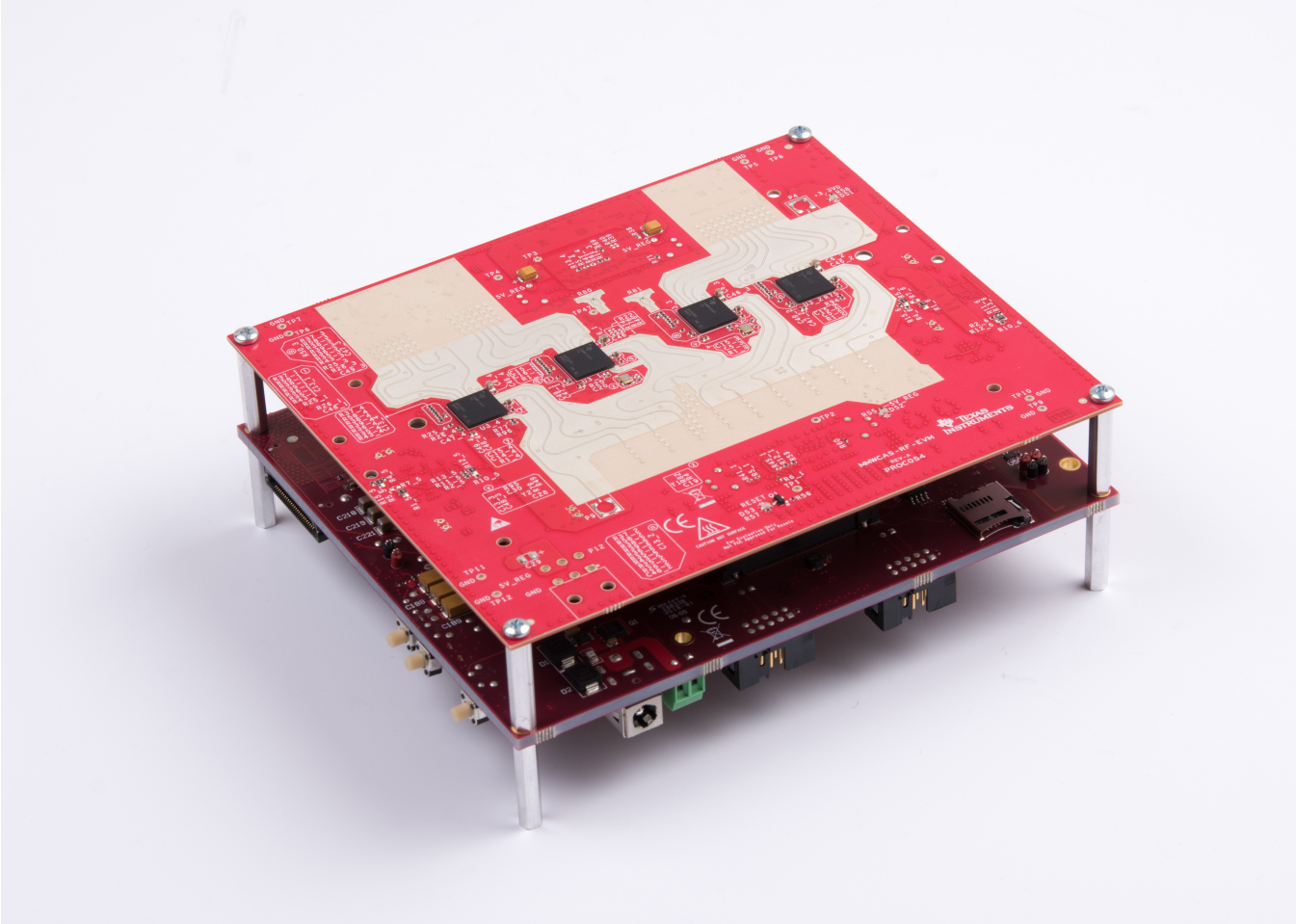

Figure 5. MMWCAS-DSP-EVM (bottom) and MMWCAS-RF-EVM (top) Board Alignment

2.4 Power

The MMWCAS-DSP-EVM is powered by 12-V power, either from a DC barrel connector (J10) or screw terminal (J11). A wall DC power source or a bench power source can be used to power the EVM. The power source should be rated at least 3 A. The typical power source is 12-V, 5-A Advantech Power supply P/N: 96PSA-A60W12V1-1.

When power is provided, various LEDs around the edge of the board light up, indicating the proper interfaces have the adequate power. Refer to the block diagram to see location of key status LEDs.

The companion power management IC (PMIC) for the SOC is TPS659039EP-Q1. A step-down 12-V to 3.3-V and 5-V converter is available in order to provide a 3.3-V and 5-V DC input to the PMIC as well as 3.3-V and 5-V power rails at the board level. Figure 6 shows the complete power supply tree.

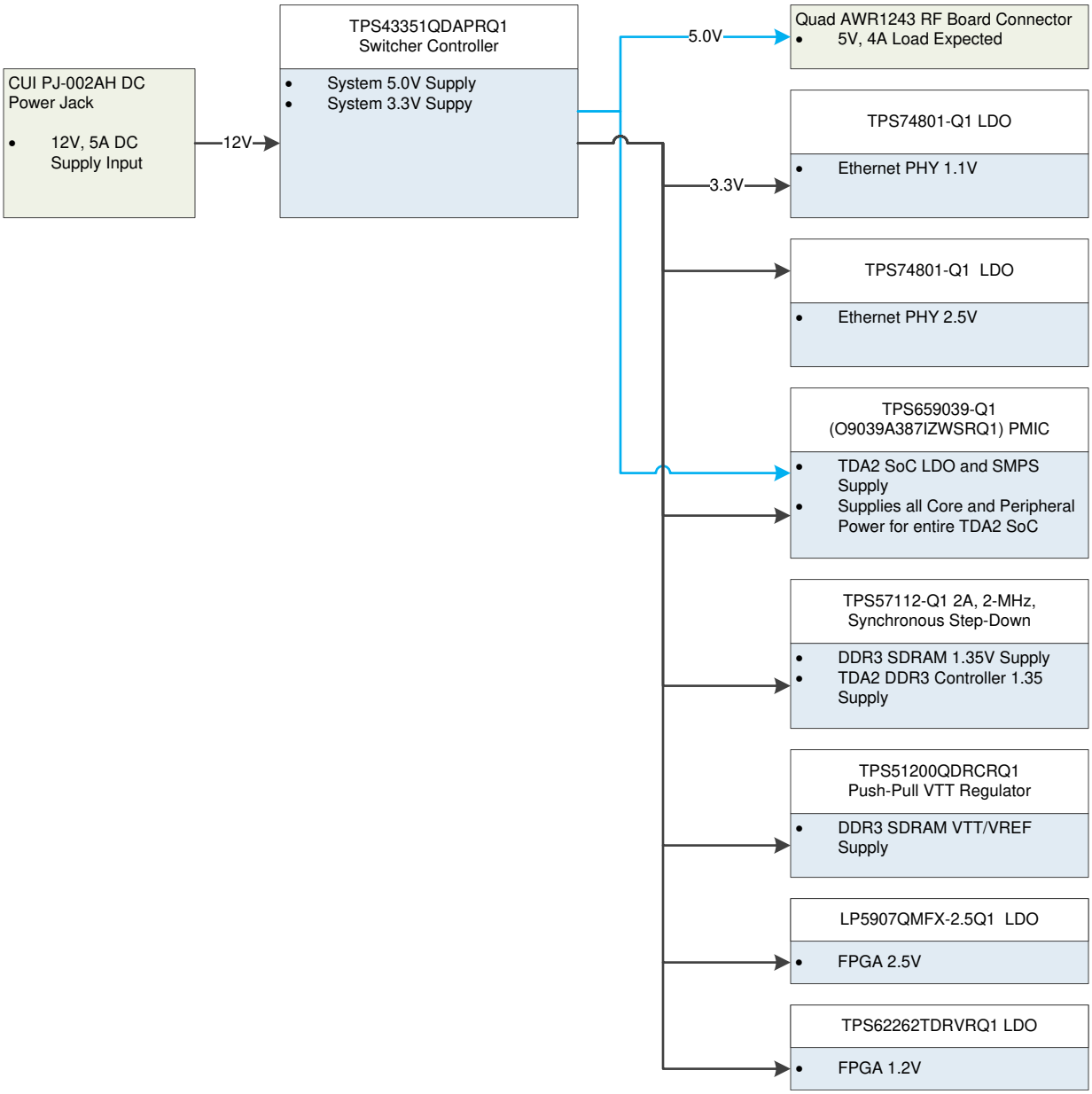

Figure 6. System Power Distribution Network

2.5 Connectors

2.5.1 RF Board Connectors (J1, J18)

The primary board to board connectors on the EVM (J1 and J18) are used to connect the board to MMWCAS-RF-EVM. These connectors are each implemented with a Hirose FX23-120S-0.5SV10 receptacle. J1 contains all the reset, boot, digital control, and CSI2.0 data paths for AWR1243P #1 and AWR1243P #2. J18 contains the same but for AWR1243P #3 and AWR1243P #4. Both connectors share common 5-V and GND return paths.

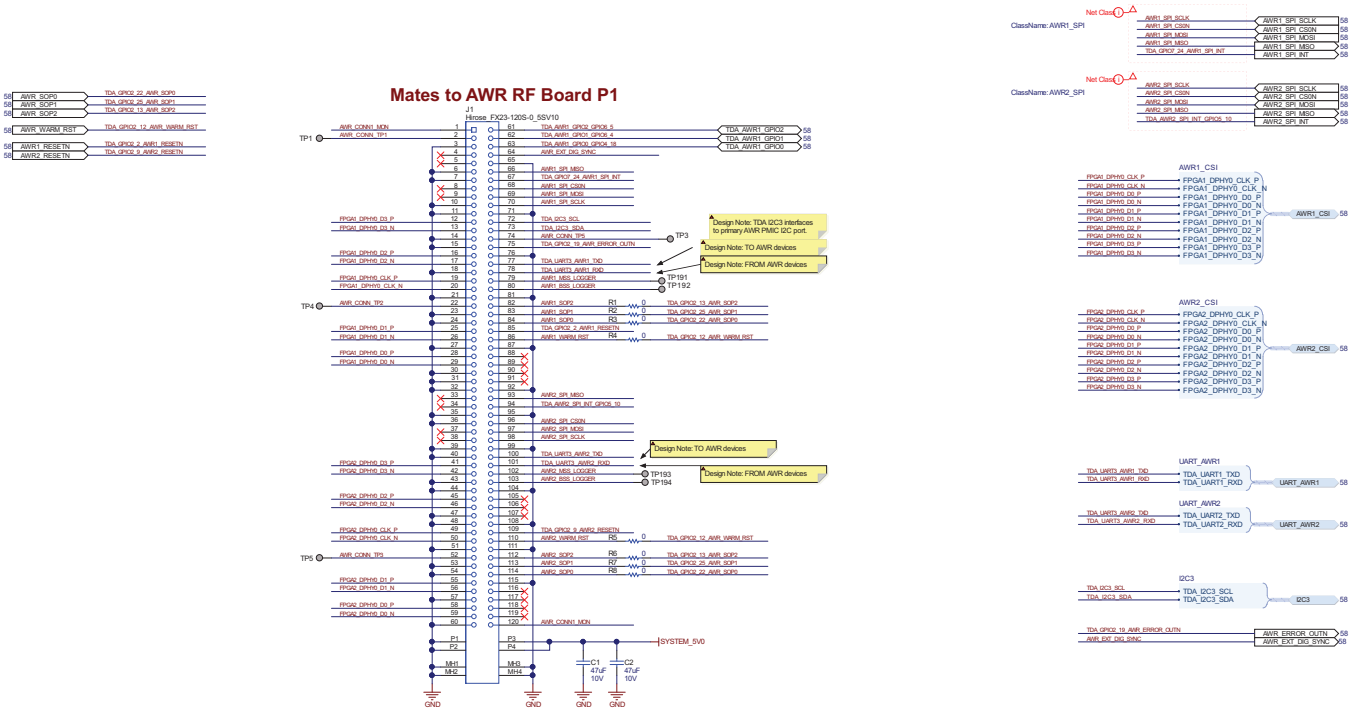

Figure 7. DSP Host to RF Board Connector #1 (J1)

Table 1. DSP Host to RF Board Connector Pin Table (J1)

Host Board Connector 1 (J1) - Mated to RF Board P1			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
1	CONN_MON	Passive	Connector monitor
2	TP1	Passive	Test Point
3	GND	Power	System ground return
4	NC	None	Unused
5	NC	None	Unused
6	GND	Power	System ground return
7	GND	Power	System ground return
8	NC	None	Unused
9	NC	None	Unused
10	GND	Power	System ground return
11	GND	Power	System ground return
12	AWR1_D3_P	Input	AWR #1 CSI2 TX3
13	AWR1_D3_N	Input	AWR #1 CSI2 TX3
14	GND	Power	System ground return
15	GND	Power	System ground return
16	AWR1_D2_P	Input	AWR #1 CSI2 TX2
17	AWR1_D2_N	Input	AWR #1 CSI2 TX2
18	GND	Power	System ground return
19	AWR1_CLK_P	Input	AWR #1 CSI2 Clock
20	AWR1_CLK_N	Input	AWR #1 CSI2 Clock
21	GND	Power	System ground return
22	TP4	Passive	Test point
23	GND	Power	System ground return

Table 1. DSP Host to RF Board Connector Pin Table (J1) (continued)

Host Board Connector 1 (J1) - Mated to RF Board P1			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
24	GND	Power	System ground return
25	AWR1_D1_P	Input	AWR #1 CSI2 TX1
26	AWR1_D1_N	Input	AWR #1 CSI2 TX1
27	GND	Power	System ground return
28	AWR1_D0_P	Input	AWR #1 CSI2 TX0
29	AWR1_D0_N	Input	AWR #1 CSI2 TX0
30	GND	Power	System ground return
31	GND	Power	System ground return
32	GND	Power	System ground return
33	NC	Passive	Unused
34	NC	Passive	Unused
35	GND	Power	System ground return
36	GND	Power	System ground return
37	NC	Passive	Unused
38	NC	Passive	Unused
39	GND	Power	System ground return
40	GND	Power	System ground return
41	AWR2_D3_P	Input	AWR #2 CSI2 TX3
42	AWR2_D3_N	Input	AWR #2 CSI2 TX3
43	GND	Power	System ground return
44	GND	Power	System ground return
45	AWR2_D2_P	Input	AWR #2 CSI2 TX2
46	AWR2_D2_N	Input	AWR #2 CSI2 TX2
47	GND	Power	System ground return
48	GND	Power	System ground return
49	AWR2_CLK_P	Input	AWR #2 CSI2 Clock
50	AWR2_CLK_N	Input	AWR #2 CSI2 Clock
51	GND	Power	System ground return
52	TP5	Passive	
53	GND	Power	System ground return
54	GND	Power	System ground return
55	AWR2_D1_P	Input	AWR #2 CSI2 TX1
56	AWR2_D1_N	Input	AWR #2 CSI2 TX1
57	GND	Power	System ground return
58	AWR2_D0_P	Input	AWR #2 CSI2 TX0
59	AWR2_D0_N	Input	AWR #2 CSI2 TX0
60	GND	Power	System ground return
61	AWR1_GPIO2	Bidirectional	AWR #1 GPIO2
62	AWR1_GPIO1	Bidirectional	AWR #1 GPIO1
63	AWR1_GPIO0	Bidirectional	AWR #1 GPIO0
64	TP_FSync	Input	Connected to EXT_DIG_SYNC fanout buffer on RF card
65	GND	Power	System ground return
66	SPI1_MISO	Input	AWR#1 SPI Slave MISO
67	AWR1_SPI_INT	Input	AWR#1 SPI Slave Interrupt
68	AWR1_CS0n	Output	AWR#1 SPI Slave CS0N
69	SPI1_MOSI	Output	AWR#1 SPI Slave MOSI

Table 1. DSP Host to RF Board Connector Pin Table (J1) (continued)

Host Board Connector 1 (J1) - Mated to RF Board P1			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
70	SPI1_SCLK	Output	AWR#1 SPI Slave SCLK
71	GND	Power	System ground return
72	I2C3_SCL	Output	E_PMIC_SCL - Primary LP87524-Q1 PMIC I2C
73	I2C3_SDA	Bidirectional	E_PMIC_SDA - Primary LP87524-Q1 PMIC I2C
74	TP3	Output	EXT_40MHZ_CLK_1V8
75	ERROR_OUTn	Input	Open-Drain OR'd ERROR_OUT from AWR#1, 2, 3 and 4
76	GND	Power	System ground return
77	AWR1_UART_TxD	Output	AWR#1 UART RX - TDA2x TX to AWR RX
78	AWR1_UART_RxD	Output	AWR#1 UART TX - AWR TX to TDA2x RX
79	TP191	Passive	
80	TP192	Passive	
81	GND	Power	System ground return
82	AWR_SOP_PMICCLKOUT	Output	AWR#1 PMICCLKOUT/SOP2
83	AWR_SOP_SYNCOUT	Output	AWR#1 SYNCOUT/SOP1 signal
84	AWR_SOP_TDO	Output	AWR#1 TDO/SOP0 signal
85	AWR1_RESETn	Output	AWR#1 NRESET signal
86	AWR_WARM_RST	Output	AWR#1 WARM_RESET signal
87	GND	Power	System ground return
88	NC	Passive	
89	NC	Passive	
90	NC	Passive	
91	NC	Passive	
92	GND	Power	System ground return
93	SPI3_MISO	Input	AWR#2 SPI Slave MISO
94	AWR2_SPI_INT		AWR#2 SPI Slave Interrupt
95	GND	Power	System ground return
96	AWR2_CS0n	Output	AWR#2 SPI Slave CS0N
97	SPI3_MOSI	Output	AWR#2 SPI Slave MOSI
98	SPI3_SCLK	Output	AWR#2 SPI Slave SCLK
99	GND	Power	System ground return
100	AWR2_UART_TxD	Output	AWR#2 UART RX - TDA2x TX to AWR RX
101	AWR2_UART_RxD	Input	AWR#2 UART TX - AWR TX to TDA2x RX
102	TP192	Passive	
103	TP194	Passive	
104	GND	Power	System ground return
105	NC	Passive	
106	NC	Passive	
107	NC	Passive	
108	GND	Power	System ground return
109	AWR2_RESETn	Output	AWR#2 NRESET signal
110	AWR_WARM_RST	Output	AWR#2 WARM_RESET signal
111	GND	Power	System ground return
112	AWR_SOP_PMICCLKOUT	Output	AWR#2 PMICCLKOUT/SOP2
113	AWR_SOP_SYNCOUT	Output	AWR#2 SYNCOUT/SOP1 signal
114	AWR_SOP_TDO	Output	AWR#2 TDO/SOP0 signal
115	GND	Power	System ground return

Table 1. DSP Host to RF Board Connector Pin Table (J1) (continued)

Host Board Connector 1 (J1) - Mated to RF Board P1			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
116	NC	Passive	
117	NC	Passive	
118	NC	Passive	
119	NC	Passive	
120	CONN_MON	Passive	Connector connection monitor - unused
121	GND	Power	System ground return
122	GND	Power	System ground return
123	EVM_5V0	Power	
124	EVM_5V0	Power	
125	GND	Power	System ground return
126	GND	Power	System ground return
127	GND	Power	System ground return
128	GND	Power	System ground return

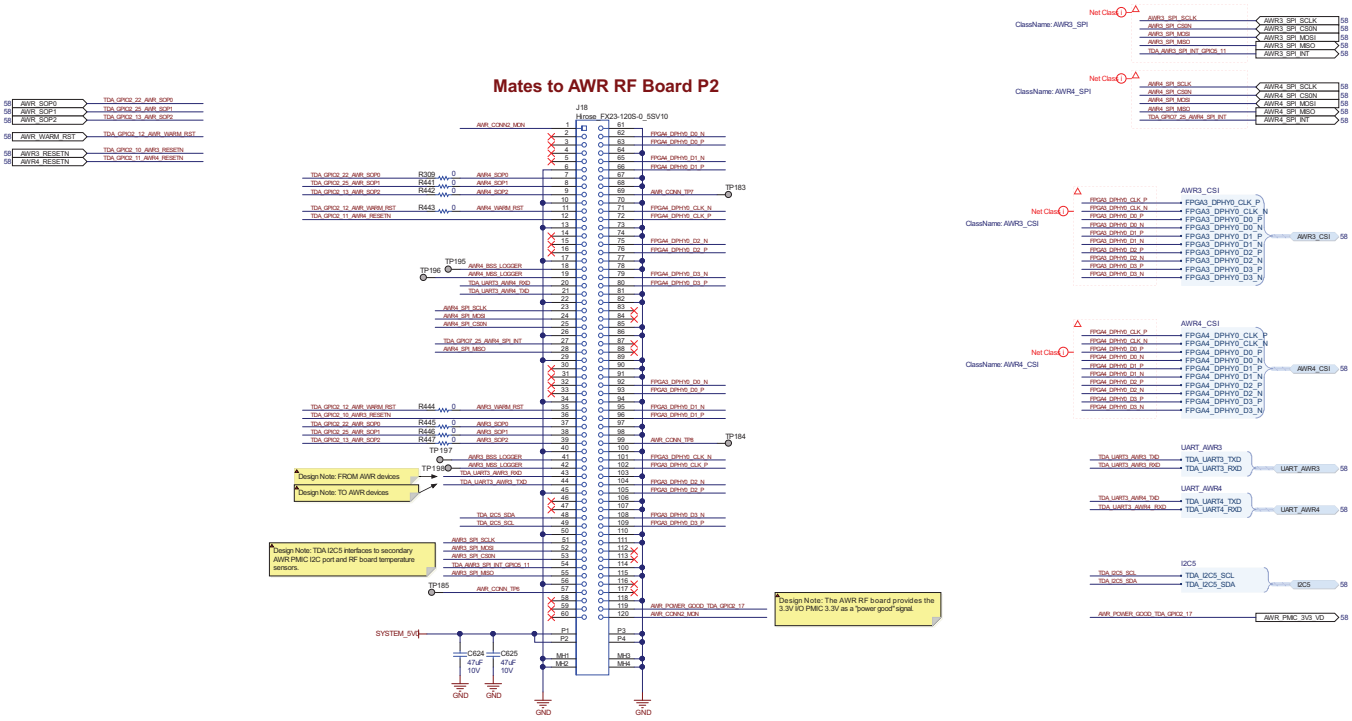

Figure 8. DSP Host to RF Board Connector #2 (J18)

Table 2. DSP Host to RF Board Connector Pin Table (J18)

Host Board Connector 1(J18) - Mated to RF Board P2			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
1	CONN2_MON	Passive	Connection Monitor
2	NC	Passive	
3	NC	Passive	
4	NC	Passive	
5	NC	Passive	
6	GND	Power	System ground return

Table 2. DSP Host to RF Board Connector Pin Table (J18) (continued)

Host Board Connector 1(J18) - Mated to RF Board P2			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
7	AWR_SOP_TDO	Output	AWR#4 TDO/SOP0 signal
8	AWR_SOP_SYNCOUT	Output	AWR#4 SYNCOUT/SOP1 signal
9	AWR_SOP_PMICCLKOUT	Output	AWR#4 PMICCLKOUT/SOP2
10	GND	Power	System ground return
11	AWR_WARM_RST	Output	AWR#4 WARM_RESET signal
12	AWR4_RESETn	Output	AWR#4 NRESET signal
13	GND	Power	System ground return
14	NC	Passive	
15	NC	Passive	
16	NC	Passive	
17	GND	Power	System ground return
18	NC	Passive	Test Point 195
19	NC	Passive	Test Point 196
20	AWR4_UART_RxD	Input	AWR4_UART_TxD-AWR TX to TDA2x RX
21	AWR4_UART_TxD	Output	AWR4_UART_RxD-AWR TX to TDA2x RX
22	GND	Power	System ground return
23	SPI1_SCLK	Output	AWR#4 SPI Slave SCLK
24	SPI1_MOSI	Output	AWR#4 SPI Slave MOSI
25	AWR4_CS1n	Output	AWR#4 SPI Slave SCLK
26	GND	Power	System ground return
27	AWR4_SPI_INT	Input	AWR#4 SPI Slave Interrupt
28	SPI1_MISO	Input	AWR#4 SPI Slave MISO
29	GND	Power	System ground return
30	NC	Passive	
31	NC	Passive	
32	NC	Passive	
33	NC	Passive	
34	GND	Power	System ground return
35	AWR_WARM_RST	Output	AWR#3 WARM_RESET signal
36	AWR3_RESETn	Output	AWR#3 NRESET signal
37	AWR_SOP_TDO	Output	AWR#3 TDO/SOP0 signal
38	AWR_SOP_SYNCOUT	Output	AWR#3 SYNCOUT/SOP1 signal
39	AWR_SOP_PMICCLKOUT	Output	AWR#3 PMICCLKOUT/SOP2
40	GND	Power	System ground return
41	NC	Passive	Test Point 197
42	NC	Passive	Test Point 198
43	AWR3_UART_TxD	Input	AWR3_UART_RxD-AWR TX to TDA2x RX
44	AWR3_UART_RxD	Output	AWR3_UART_TxD-AWR TX to TDA2x RX
45	GND	Power	System ground return
46	NC	Passive	
47	NC	Passive	
48	I2C5_SDA	Bidirectional	E_PMIC_SDA - Primary LP87524-Q1 PMIC I2C
49	I2C5_SCL	Output	E_PMIC_SCL - Primary LP87524-Q1 PMIC I2C
50	GND	Power	System ground return
51	SPI3_SCLK	Output	AWR#3 SPI Slave SCLK
52	SPI3_MOSI	Output	AWR#3 SPI Slave MOSI

Table 2. DSP Host to RF Board Connector Pin Table (J18) (continued)

Host Board Connector 1(J18) - Mated to RF Board P2			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
53	AWR3_CS1n	Output	AWR#3 SPI Slave SCLK
54	AWR3_SPI_INT	Input	AWR#3 SPI Slave Interrupt
55	SPI3_MISO	Input	AWR#3 SPI Slave MISO
56	GND	Power	
57	TP_tmp_al	Input	Test Point 185
58	NC	Passive	
59	NC	Passive	
60	NC	Passive	
61	GND	Power	System ground return
62	AWR4_D0_N	Input	AWR #4 CSI2 TX0
63	AWR4_D0_P	Input	AWR #4 CSI2 TX0
64	GND	Power	System ground return
65	AWR4_D1_N	Input	AWR #4 CSI2 TX1
66	AWR4_D1_P	Input	AWR #4 CSI2 TX1
67	GND	Power	System ground return
68	GND	Power	System ground return
69	TP_SP1	Passive	Test Point 183
70	GND	Power	System ground return
71	AWR4_CLK_N	Input	AWR #4 CSI2 Clock
72	AWR4_CLK_P	Input	AWR #4 CSI2 Clock
73	GND	Power	System ground return
74	GND	Power	System ground return
75	AWR4_D2_N	Input	AWR #4 CSI2 TX2
76	AWR4_D2_P	Input	AWR #4 CSI2 TX2
77	GND	Power	System ground return
78	GND	Power	System ground return
79	AWR4_D3_N	Input	AWR #4 CSI2 TX3
80	AWR4_D3_P	Input	AWR #4 CSI2 TX3
81	GND	Power	System ground return
82	GND	Power	System ground return
83	NC	Passive	
84	NC	Passive	
85	GND	Power	System ground return
86	GND	Power	System ground return
87	NC	Passive	
88	NC	Passive	
89	GND	Power	System ground return
90	GND	Power	System ground return
91	GND	Power	System ground return
92	AWR3_D0_N	Input	AWR #3 CSI2 TX0
93	AWR3_D0_P	Input	AWR #3 CSI2 TX0
94	GND	Power	System ground return
95	AWR3_D1_N	Input	AWR #3 CSI2 TX1
96	AWR3_D1_P	Input	AWR #3 CSI2 TX1
97	GND	Power	System ground return
98	GND	Power	System ground return

Table 2. DSP Host to RF Board Connector Pin Table (J18) (continued)

Host Board Connector 1(J18) - Mated to RF Board P2			
Pin Number	**Net Name**	**Pin Type**	**Function/Description**
99	TP_SP2	Passive	Test Point 184
100	GND	Power	System ground return
101	AWR3_CLK_N	Input	AWR #3 CSI2 Clock
102	AWR3_CLK_P	Input	AWR #3 CSI2 Clock
103	GND	Power	System ground return
104	AWR3_D2_N	Input	AWR #3 CSI2 TX2
105	AWR3_D2_P	Input	AWR #3 CSI2 TX2
106	GND	Power	System ground return
107	GND	Power	System ground return
108	AWR3_D3_N	Input	AWR #3 CSI2 TX3
109	AWR3_D3_P	Input	AWR #3 CSI2 TX3
110	GND	Power	System ground return
111	GND	Power	System ground return
112	NC	Passive	
113	NC	Passive	
114	GND	Power	System ground return
115	GND	Power	System ground return
116	NC	Passive	
117	NC	Passive	
118	GND	Power	
119	PWR_GOOD	Input	Power good from RF
120	CONN2_MON	Passive	Connector connection monitor - unused
121	EVM_5V0	Power	
122	EVM_5V0	Power	
123	GND	Power	System ground return
124	GND	Power	System ground return
125	GND	Power	System ground return
126	GND	Power	System ground return
127	GND	Power	System ground return
128	GND	Power	System ground return

2.5.2 USB Connector (J16)

The MMWCAS-DSP-EVM has one USB2.0 mini connector. Connector J16 allows access to the EVM through UART, SPI, or I2C through the FTDI chip.

Table 3 provides the J16 connector pin information.

Table 3. USB Connector Pin Table (J16)

Pin No	Signal Name	Description
1	FTDI_USB_VBUS_5V0	5-V power from PC machine
2	FTDI_USB_D_CONN_N	USB Data Signal Negative
3	FTDI_USB_D_CONN_P	USB Data Signal Positive
4	No Connect	No Connect
5	GND	Ground

2.5.3 Ethernet Jack (J12)

The MMWCAS-DSP-EVM supports a Gigabit Ethernet port to provide the connection to the network. The Ethernet port is interfaced to the TDA2 through the Ethernet PHY DP83867, and is used to stream the captured data over the network to the host PC.

The DP83867 device is a robust, low power, fully featured physical layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2(direct contact)

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

2.5.4 PCIe m.2 socket(m-keyed) (J14)

The DSP EVM supports PCIe 2.0 through an m.2 connector. Out of the box, a 512 GB SSD is assembled on the EVM. The connector is a JAE Electronics SM3ZS067U410AMR1000 PCI express m.2 connector. The SSD drive provides 3.3 V through the connector, and the data lanes have been length and impedance matched through the PCIE spec document. The EVM has a notch with a small standoff that allows a size 2280 SSD card to be securely attached with the provided machine screw. The recommended SSD is a single-sided card, but a double-sided card can be used if the SSD components do not touch the board components, due to height.

2.5.5 Lattice FPGA Headers (J3,J5,J7,J9)

The EVM contains four programming headers for the on board FPGA and flash devices. Out of the box, the FPGAs are flashed so they are ready to use. If the FPGAs must be flashed, refer to Figure 9 for proper cable assembly. Lattice Diamond 3.10 (not included) and Lattice HW-USBN-2B Programmer (not included) must be used. Along with each FPGA, there is a small NOR flash device used to hold the image on power cycle.

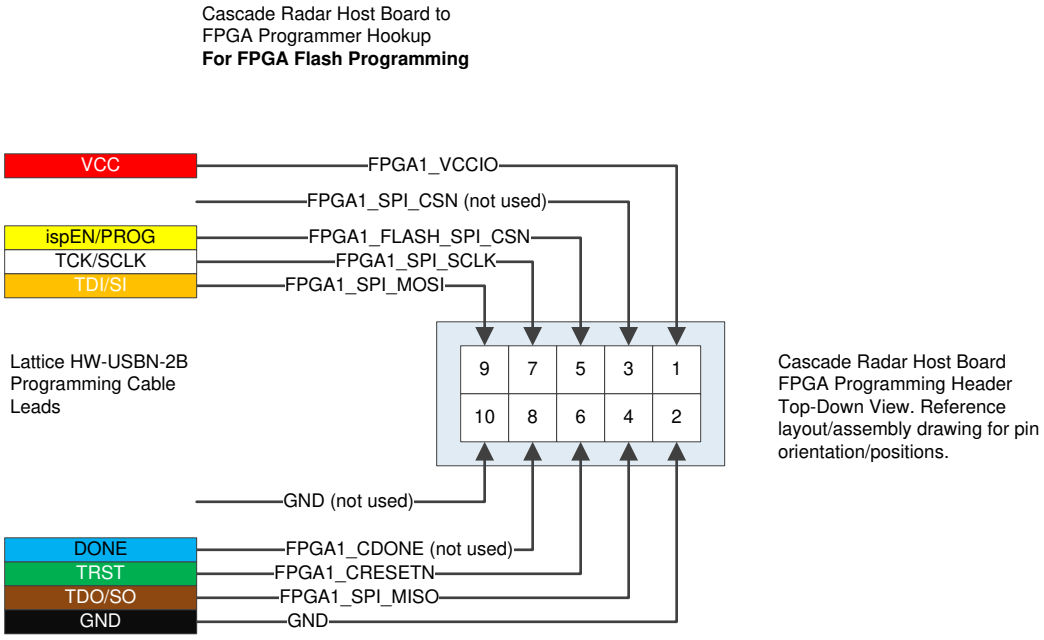

Figure 9. FPGA Flash Programming Header Pinout

2.5.6 JTAG and Emulator (J19)

The EVM has support of the following JTAG emulation headers:

- 60-pin MIPI Connector
- Standard 14-pin to 60-pin MIPI adapter
- 20-pin CTI to 60-pin MIPI adapter

2.5.7 Lattice ECP5 FPGA Prototyping Header (J20)

Included on the EVM is a Lattice Prototyping connector. The interface brings out the VOUT1 interface, I2C5, and two I2C GPIO expander pins to allow for interfacing to a separate Lattice ECP5 FPGA card, which performs VOUT to 10GBase-KR bridging.

2.6 GPIO, Switches, Push Buttons, and LEDs

2.6.1 GPIO List

The MMWCAS-DSP-EVM supports a number of GPIOs, some of which can be user controlled. Table 4 shows the GPIO list.

Table 4. GPIO List and Description

GPIO for EVM	Function/Description
TDA_GPIO1_15_ALERT#	PCIe SSD Alert notification to master. Active Low. Open-Drain with pullup on board. '0' - Active '1' - Inactive(Default)
GPIO_EXP_P13(PERST#)	PCIe Reset - functional reset to the card '0' - Hold in reset until stable(Default) '1' - Release from reset
GPIO_EXP_P14(CLKREQ#)	PCIe Reference Clock Request '0' - Request for clock '1' - Not Active(Default)
GPIO6_8	Selects between AWR and FPGA/Flash for SPI1 '0' - Selects AWR(Default) '1' - Selects FPGA/Flash
GPIO6_6	When ganged. Controls FPGA1/2/3/4 CRESETN signals '0' - Holds FPGA in Reset(Default) '1' - released FPGA from Reset
GPIO7_31	Controls FPGA1 CRESETN signals '0' - Holds FPGA1 in Reset(Default) '1' - released FPGA1 from Reset
GPIO7_30	Controls FPGA2 CRESETN signals '0' - Holds FPGA2 in Reset(Default) '1' - released FPGA2 from Reset
GPIO5_13	Controls FPGA3 CRESETN signals '0' - Holds FPGA3 in Reset(Default) '1' - released FPGA3 from Reset
GPIO5_14	Controls FPGA4 CRESETN signals '0' - Holds FPGA4 in Reset(Default) '1' - released FPGA4 from Reset
GPIO1_14	Control FPGA1/2/3/4 Flash RESETn Signals '0' - Hold in Reset '1' - Release from Reset (Default)
GPIO7_27	AWR Extern SYNC
SMB_CLK	SMBus Clock. I2C1 SCL for PCIe
SMB_DATA	SMBus Data. I2C1 SDA for PCIe
I2C1 SCL	EEPROM(U100) Serial Clock Address: 0x50
I2C1 SDA	EEPROM(U100) Serial Data Address: 0x50

2.6.2 Switches

The MMWCAS-DSP-EVM has a 1×6 DIP(S4) switch for boot selection (as shown in Table 5). Out of the box, the EVM has S4.5 and S4.6 "ON" so that it boots from the SD card.

Table 5. User Configurable Supported Boot Modes

Boot Mode	S4 Configuration[5:0]
USB boot	010000
UART boot	010011
eMMC boot	111000
eMMC boot partition	111011
SD boot	110000 **(Default)**

2.6.3 Push Buttons

The MMWCAS-DSP-EVM supports three push buttons for POR reset, SoC Reset, and an ON/OFF button. By default, the ON/OFF button is disabled. Refer to SCH for resistor options for ON/OFF functionality.

Table 6. Push Button Functionality Information

Reference	Usage	Description
S1	ON/OFF	Turns the EVM on and off with each push. By default, the switch is disabled so that the EVM powers up when power is applied. Refer to the SCH for resistor options in order to toggle ON/OFF functionality.
S2	PORz Reset	Generates a PORz reset upon pushing.
S3	SoC Reset	Generates a reset on the SoC.

2.6.4 LEDs

The MMWCAS-DSP-EVM supports LEDs for user indications, as listed in Table 7.

Table 7. User and Status LED Reference Designator and Description

Reference	Usage	Description	Color
D3	Status	Ethernet Activity	Green
D4	Status	TPS74801 - Ethernet 1.0V Power Good	Green
D5	Status	FTDI Power Enable – 5V	Green
D6	Status	FTDI RX	Green
D7	Status	FTDI TX	Green
D9	User GPIO	User programmable	Green
D10	Status	Ethernet 2.5V Power Good	Green
D11	Status	TDA2 Reset out	Green
D12	Status	12V Input	Green
D13	User GPIO	User programmable	Green
D14	User GPIO	User programmable	Green
D15	User GPIO	User programmable	Green
D16	Status	TDA2 PORz – Power On Reset	Green
D17	Status	FPGA1 LED	Green
D18	User GPIO	User programmable	Green
D19	User GPIO	User programmable	Green
D20	Status	TDA2 Reset – Reset based on status of VDD_MPU	Green
D21	Status	TDA2 PMIC Reset out	Green
D22	Status	FPGA2 LED	Green
D23	Status	TPS43351 - 3.3V and 5V Power Good	Green

Table 7. User and Status LED Reference Designator and Description (continued)

Reference	Usage	Description	Color
D24	Status	TPS57112 DDR3 1.35V Power Good	Green
D25	Status	FPGA3 LED	Green
D26	Status	TPS51200 DDR3 VTT and VREF Power Good	Green
D27	Status	FPGA4 LED	Green

3 mmWave Studio and Matlab Post Processing

TI provides the following evaluation software to get started with the Cascade DSP evaluation module:

- mmWave Studio GUI and Lua scriptable configuration environment
- TDA2x ADC IF data capture application running on the MMWCAS-DSP-EVM
- Matlab post processing sample codes for reading captured ADC IQ sample datasets and example TDMA-MIMO and TX-Beamforming use modes

For details on getting started with these demos, see the mmWave Studio User Guide

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