EVM User's Guide: AWR2944EVM, AWR2944PEVM

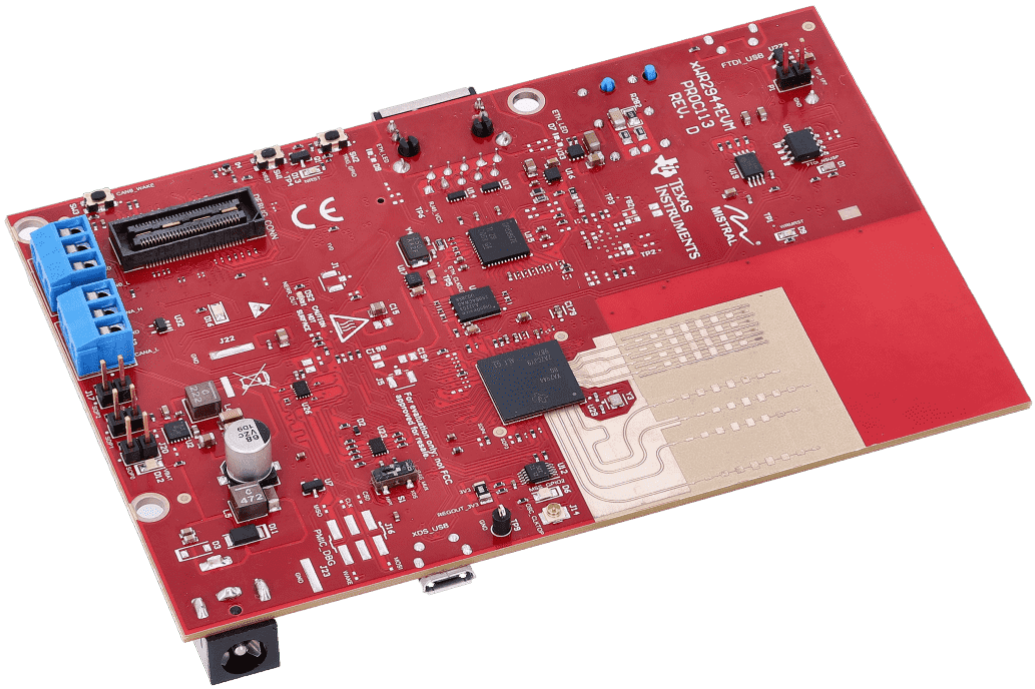
AWR2944/AWR2944P Evaluation Module

Description

The AWR2944/AWR2944P evaluation module (EVM) is an easy-to-use platform for evaluating the AWR2944/AWR2944P mmWave system-on-chip (SoC) radar sensor, which has direct connectivity to the DCA1000EVM (sold separately). The AWR2944EVM/AWR2944PEVM kit contains everything required to start developing software for the on-chip C66x digital signal processor (DSP), ARM® Cortex®-R5F controller, and hardware accelerator (HWA 2.0 in AWR2944, HWA 2.1 in AWR2944P). Also included is onboard emulation for programming and debugging, as well as onboard buttons and LEDs for quick integration of a simple user interface.

Features

- 76GHz to 81GHz mmWave radar sensor
- Onboard four-transmit four-receive (4TX/4RX) antenna
- On-chip C66x DSP core and Arm Cortex-R5F controller
- On-chip hardware accelerator (HWA 2.0)
- Direct interface with DCA1000EVM



AWR2944EVM

1 Evaluation Module Overview

1.1 Introduction

The AWR2944EVM and AWR2944PEVM are easy-to-use evaluation boards for the AWR294x mmWave sensing device, with direct connectivity to the DCA1000 EVM.This EVM kit contains everything needed to start developing software for the on-chip C66x DSP, ARM® Cortex®-R5F controller, and hardware accelerator (HWA 2.0). Also included is on-board emulation for programming and debugging as well as on-board buttons and LEDs for quick integration of a simple user interface.

1.2 Key Features

- Onboard antenna
- XDS110 based JTAG emulation with serial port for onboard 64-bit QSPI flash programming
- UART to USB Debug port for terminal access using FT4232H
- 60-pin, high-density (HD) connector for external JTAG/emulator interface with TRACE and CSI2 support
- 60-pin, high-density (HD) connector for debug, SPI, I2C and LVDS
- RJ45 connector to stream the captured data over the network to the host PC
- MATEnet Ethernet® interface to stream the captured data over the network to an automotive host
- Dual onboard CAN-FD transceiver
- One button and LED for basic user interface
- 12V power jack to power the board

1.3 What's Included

1.3.1 Kit Contents

- AWR2944EVM or AWR2944PEVM
- Micro USB cable
- Ethernet Cable
- Mounting brackets, screws, spacers and nuts, to allow placing the PCB vertical

Note

A 12V, > 2.5A supply brick with a 2.1mm barrel jack (center positive) is not included. TI recommends using an external power supply that complies with applicable regional safety standards, such as UL, CSA, VDE, CCC, PSE, and more. The length of the power cable needs to be < 3m.

The following power supply has been tested to work with the AWR2944EVM: SDI65-12-U-P5.

1.3.2 mmWave Out-of-Box (OOB) Demo

TI provides sample demo codes to easily get started with the AWR2944 evaluation module (EVM) and to experience the functionality of the AWR2944 radar sensor. For details on getting started with these demos, see www.ti.com/tool/mmwave-sdk.

2 Hardware

CAUTION HOT SURFACE
CONTACT MAY CAUSE BURN
DO NOT TOUCH

Note

During operation, a minimum separation distance of 20 centimeters must be maintained between the user and the EVM.

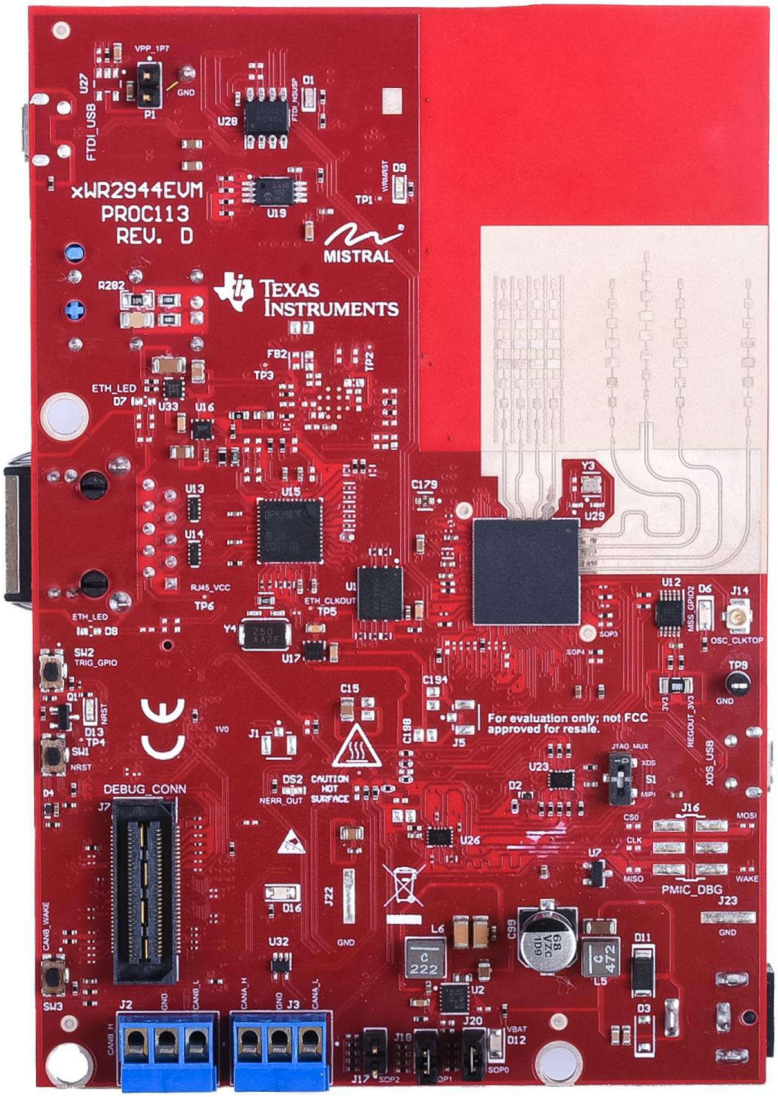


Figure 2-1. AWR2944EVM Front View

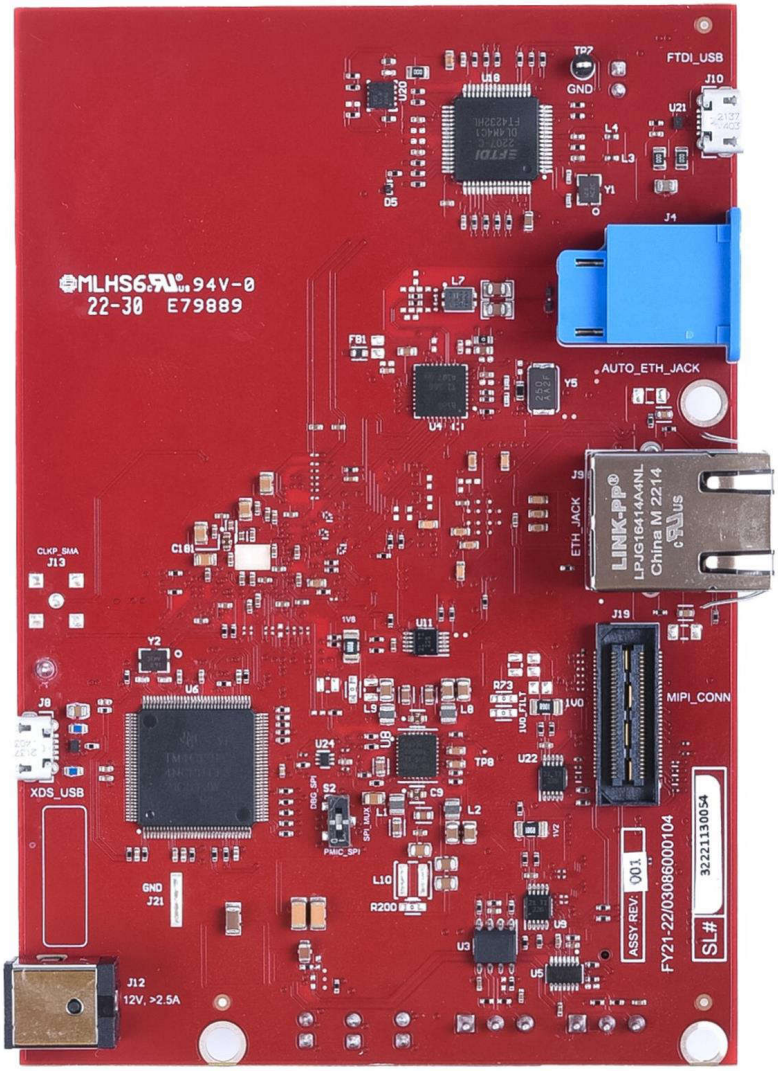


Figure 2-2. AWR2944EVM Back View

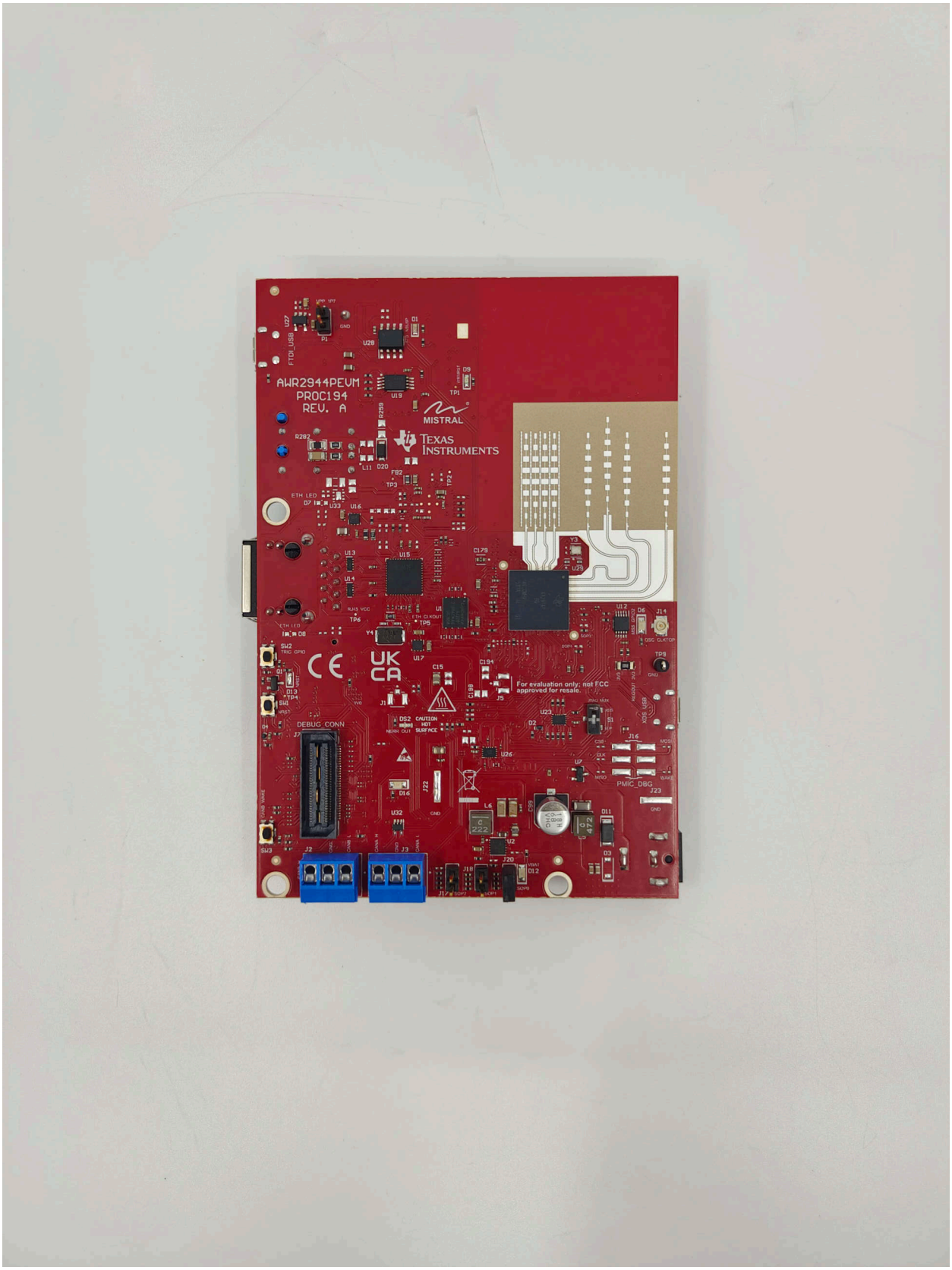


Figure 2-3. AWR2944PEVM Front View

Figure 2-4. AWR2944PEVM Back View

2.1 Block Diagram

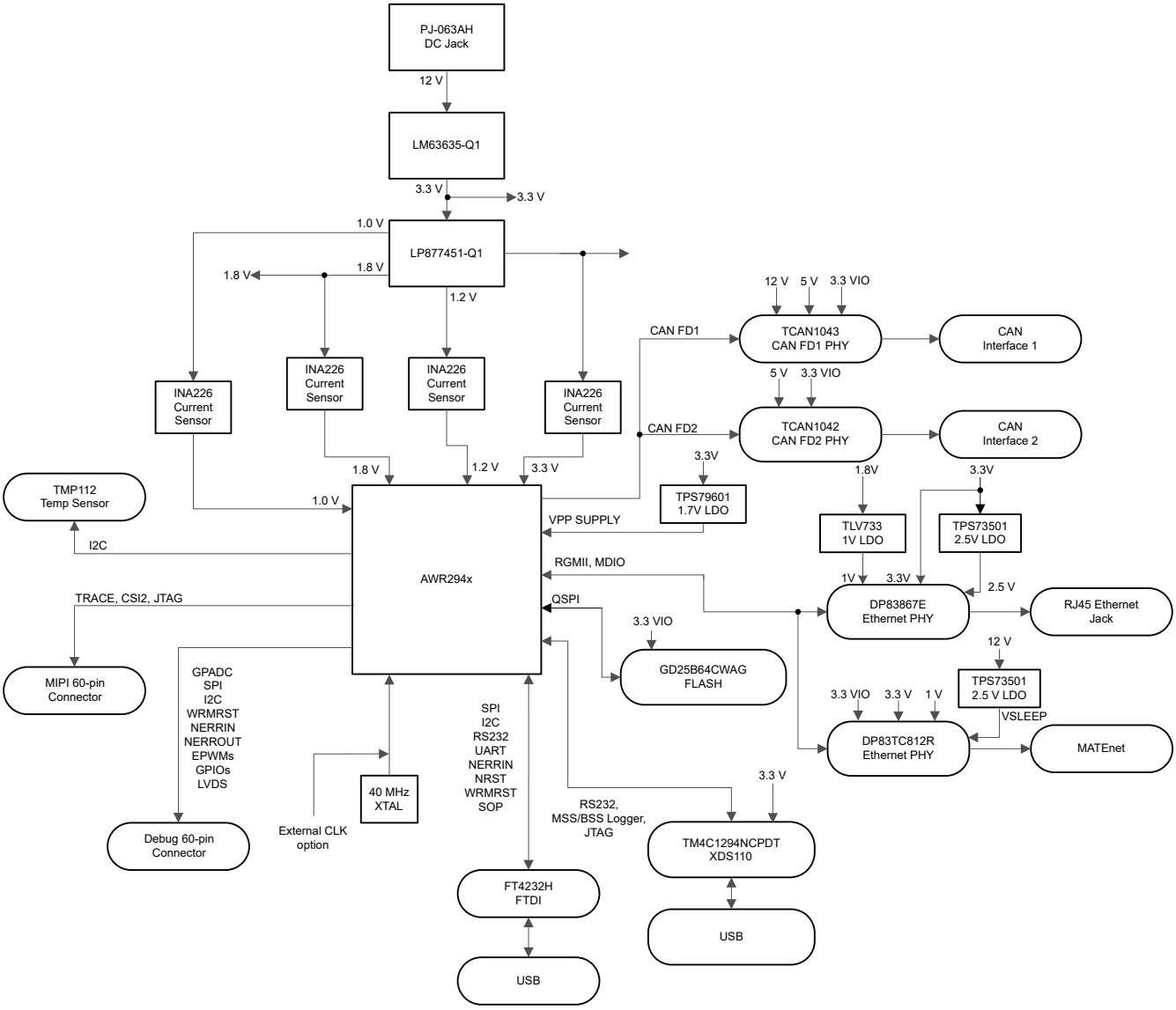


Figure 2-5. AWR2944EVM Block Diagram

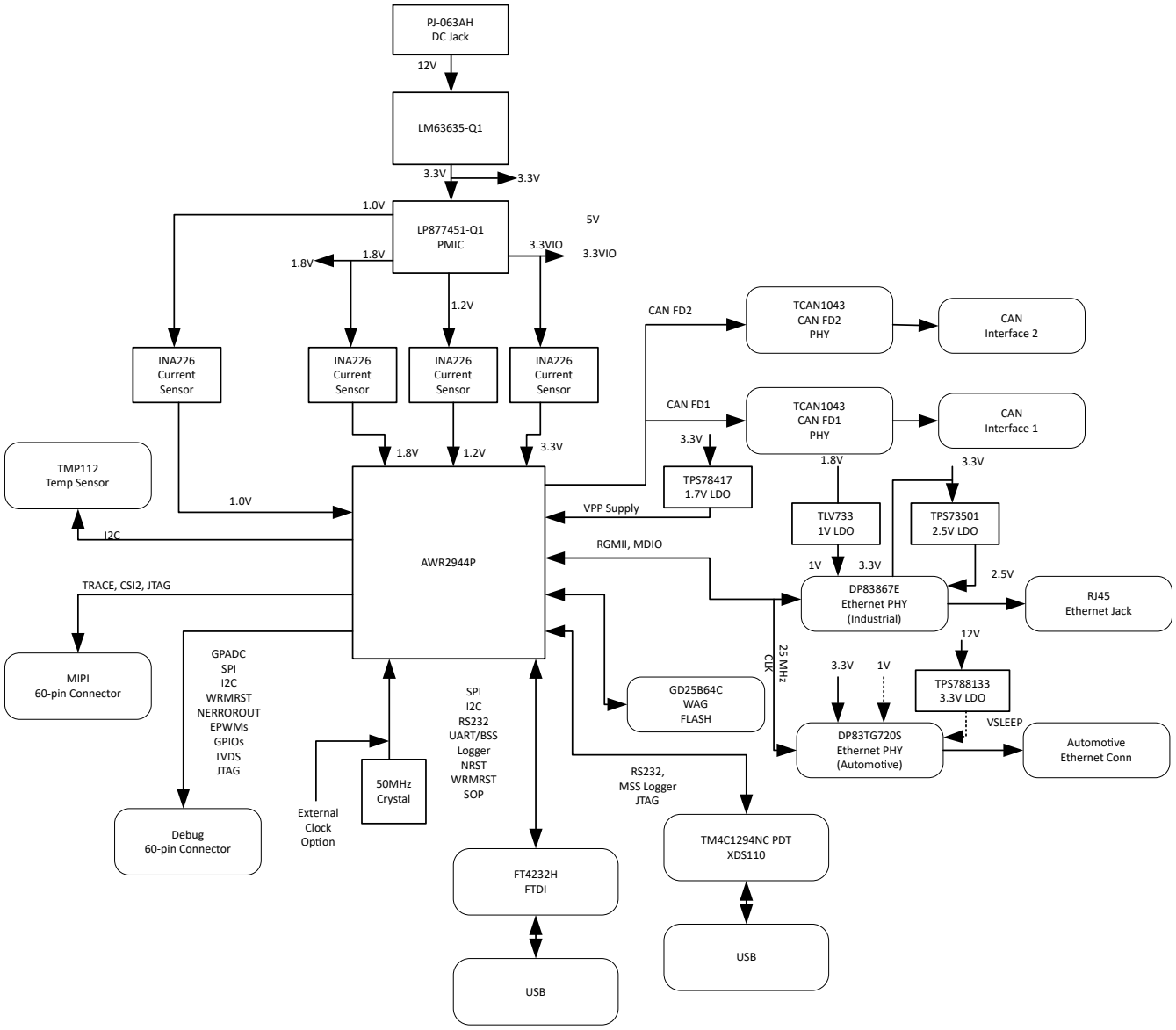


Figure 2-6. AWR2944PEVM Block Diagram

2.2 PCB Handling Recommendations

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in the supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA010A.

2.3 Power Connections

The AWR2944EVM/AWR2944PEVM is powered by the 12V power jack (>2.5A current capability). When power is provided the AR_NRST, VBAT_INT, and 5V0 LEDs glow, indicating that the board is powered up.

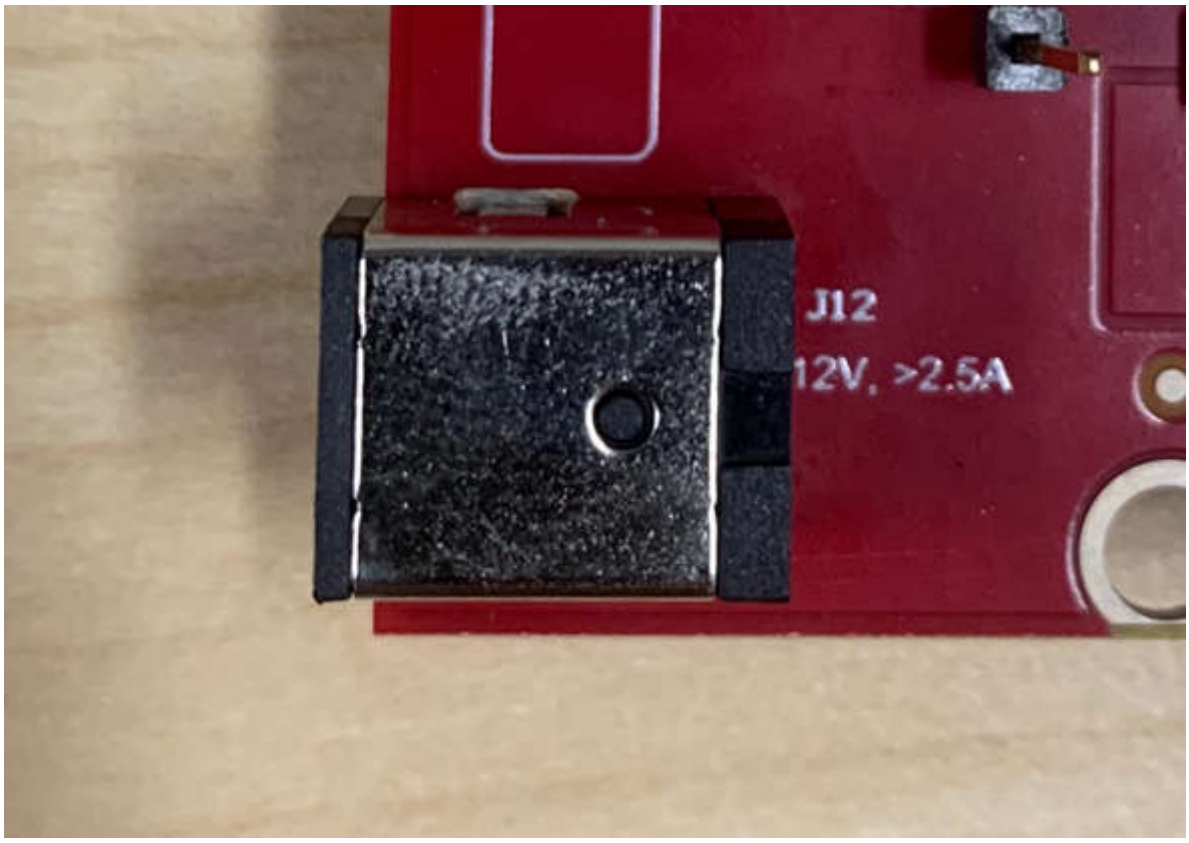


Figure 2-7. 12V Power Connector

Note

After the 12V power supply is provided to the EVM, TI recommends to press the NRST switch (SW1) one time to provide for a reliable boot-up state.

2.4 Connectors

2.4.1 MIPI 60-Pin Connector (J19)

This connector provides the standard MIPI 60-pin interface, as shown in Figure 5, for JTAG, CSI2 and trace capability through emulators such as the XDS560pro. Further information on the emulation and trace header can be found in the Emulation and Trace Headers Technical Reference Manual.This connector also provides access to the CSI_RX lanes which allow for playback or feeding external data and bypassing the RF front end, which enables testing and algorithm development on a known dataset.

To use this interface, the JTAG lines from the AWR2944EVM/AWR2944PEVM needs to be muxed to MIPI 60-pin connector. Refer to Section 2.8.1 for more details.

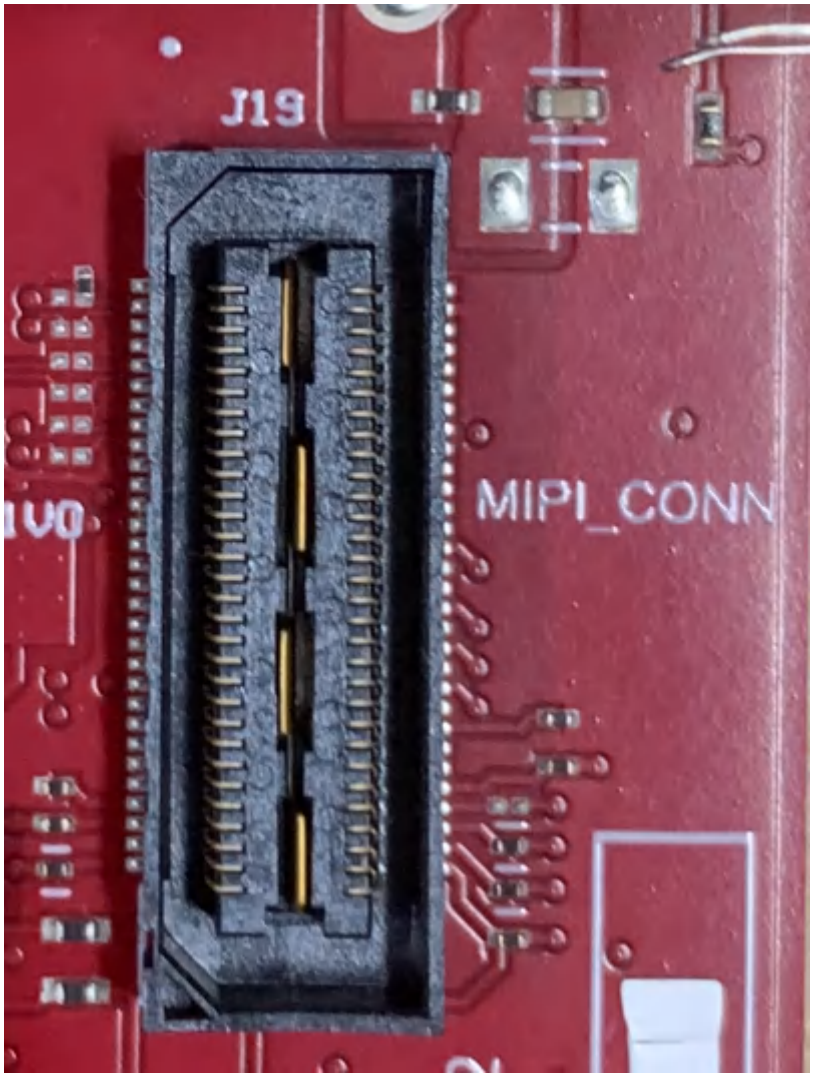


Figure 2-8. 60-pin MIPI Connector

Table 2-1 provides the pin assignment details for the MIPI 60-pin connector.

Table 2-1. J19 Pin Assignment

Pin Number	Description	Pin Number	Description
1	MIPI_VREF_DEBUG	2	MIPI_TMS
3	MIPI_TCK	4	MIPI_TDO
5	MIPI_TDI	6	MIPI_NRST
7	MIPI_RTCK	8	MIPI_TRSTPD
9	MIPI_JTAG_NRST	10	NC
11	NC	12	MIPI_VREF_DEBUG
13	TRACE_CLK	14	NC
15	MIPI_DBG_DETECT	16	GND
17	TRACE_CTL	18	NC
19	TRACE_DATA0	20	NC
21	TRACE_DATA1	22	NC
23	TRACE_DATA2	24	NC
25	TRACE_DATA3	26	NC
27	TRACE_DATA4	28	NC

Table 2-1. J19 Pin Assignment (continued)

Pin Number	Description	Pin Number	Description
29	TRACE_DATA5	30	NC
31	TRACE_DATA6	32	NC
33	TRACE_DATA7	34	NC
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC
41	NC	42	GND
43	NC	44	CSI2_CLK_P
45	NC	46	CSI2_CLK_N
47	NC	48	GND
49	NC	50	CSI2_1_P
51	NC	52	CSI2_1_N
53	NC	54	GND
55	NC	56	CSI2_0_P
57	GND	58	CSI2_0_N
59	NC	60	GND

2.4.2 Debug Connector-60 pin (J7)

This connector enables interfacing of LVDS signals to the DCA1000 EVM for data capturing purposes.

Also, the connector has SPI, I2C, JTAG, GPADC, WRMRST, NRROUT, EPWM, and other control signals from AWR2944EVM/AWR2944PEVM for debug purpose.

The SPI is multiplexed to the Debug Connector. For more details refer to Section 2.8.1.

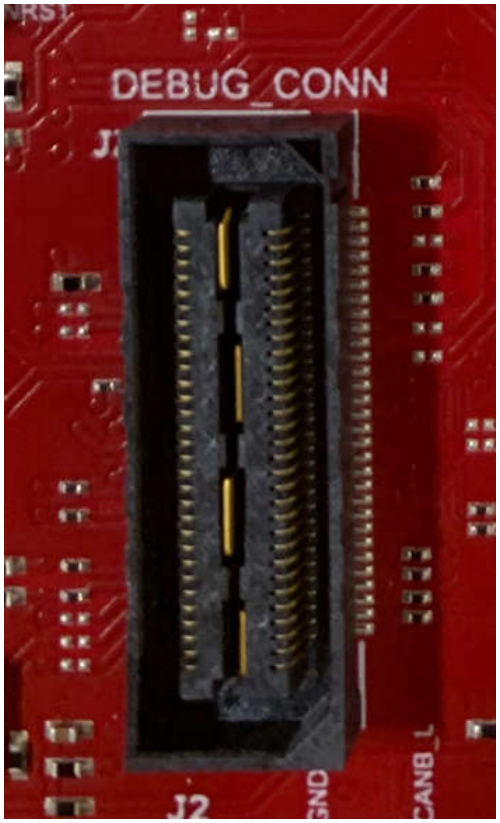


Figure 2-9. 60-pin Debug Connector

Table 2-2 provides the pin assignment details for the Debug 60-pin connector.

Table 2-2. J7 Pin Assignment

Pin Number	Description	Pin Number	Description
1	NC	2	NC
3	NC	4	XREF_CLK0
5	GND	6	MSS_EPWMA0
7	DBG_SPI_CS0	8	GND
9	DBG_SPI_CLK	10	MSS_SPIA_HOSTIRQ
11	DBG_SPI_PICO	12	DBG_SPI_POCI
13	3.3V PULL_UP	14	XREF_CLK1
15	EMU_TCK	16	MCU_CLKOUT
17	EMU_TDI	18	GND
19	GPADC1	20	EMU_TMS
21	GPADC2	22	EMU_TDO
23	GPADC3	24	GND
25	GPADC4	26	LVDS_TX3_FRCLK_P
27	GPADC5	28	LVDS_TX3_FRCLK_N
29	GPADC6	30	GND
31	GPADC7	32	NC
33	GPADC8	34	NC
35	GPADC9	36	GND
37	MSS_SPIB_CS1	38	NC
39	SOP1_MSS_SPIB_CS2	40	NC
41	MSS_GPIO_0	42	GND
43	MSS_GPIO_1	44	LVDS_TX2_CLK_P
45	AR_WRMRST	46	LVDS_TX2_CLK_N
47	NC	48	GND
49	AR_NERROUT	50	LVDS_TX1_P
51	MSS_I2CA_SCL	52	LVDS_TX1_N
53	MSS_I2CA_SDA	54	
55	MSS_EPWMB0	56	LVDS_TX0_P
57	MSS_EPWMA1	58	LVDS_TX0_N
59	MSS_GPIO_3	60	GND

2.4.3 CAN-A Interface Connector (J3)

The J3 connector provides the CANA_L and CANA_H signals from the onboard can CAN-FD transceiver (TCAN1042HGVDRQ1). These can be directly wired to the CAN bus.

Figure 2-10. CAN_A Connector

Table 2-3 provides the pin assignment details for the CAN_A connector.

Table 2-3. J3 Pin Assignment

Pin Number	Description
1	CAN_L
2	GND
3	CAN_H

2.4.4 CAN-B Interface Connector (J2)

The J2 connector provides the CANB_L and CANB_H signals from the onboard can CAN-FD transceiver (TCAN1043ADYYRQ1). These can be directly wired to the CAN bus.

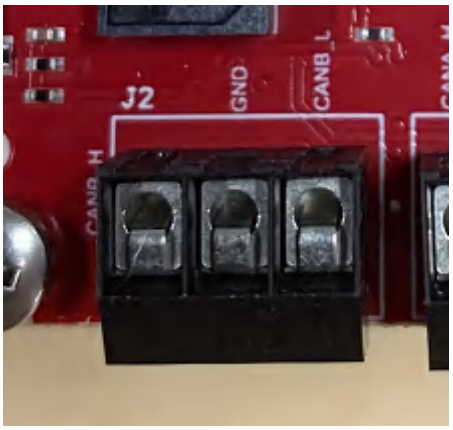


Figure 2-11. CAN_B Connector

Table 2-4 provides the pin assignment details for the CAN_B connector.

Table 2-4. J2 Pin Assignment

Pin Number	Description
1	CAN_L
2	GND
3	CAN_H

2.4.5 Ethernet Ports (J4 and J9)

The AWR2944EVM/AWR2944PEVM support two RGMII Ethernet ports to provide the connection to the network. The J4 connector provides access over a MATEnet port (9-2304372-9 connector) via a DP83TC812R-Q1 PHY. The J9 port provides access over an RJ45 port via a DP83867ERGZR PHY. By default, the RGMII interfaces are connected to the J9 port only. To access the RGMII interface over the J4 connector, several resistors must be populated. For more details please see Section 2.4.5.1 and refer to the Schematic, BOM, and Assembly and Database and Layout sections.

This RGMII interface is intended to operate primarily as a 100Mbps ECU interface and can also be used as an Instrumentation Interface.

The RGMII interface supports following features:

- Full Duplex 10Mbps/100Mbps wire rate Interface to Ethernet PHY over RGMII, parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support

The Ethernet port is interfaced to the AWR2944 through the Ethernet PHY and is used to stream the captured data over the network to the host PC.

The AWR2944PEVM is similar to the AWR2944EVM, except that the DP83TC812R-Q1 is replaced by a DP83TG720S 1Gbps Ethernet PHY device that can be interfaced with via the J4 connector. This allows for higher data rate Ethernet PHY testing. The AWR2944PEVM also allows resistors R385 and R212 to be populated while depopulating crystal Y5, in order to test sourcing a 25MHz clock directly from the AWR2944P device to the DP83TG720S.

Figure 2-12 shows the Ethernet RJ45 Mag-Jack connector, and Table 2-5 provides the connector pin details.

Table 2-5. J9 Pin Assignment

Pin Number	Description	Pin Number	Description
1	GND	2	Test point
3	ETH_D4P	4	ETH_D4N
5	ETH_D3P	6	ETH_D3N
7	ETH_D2P	8	ETH_D2N
9	ETH_D1P	10	ETH_D1N
11	LED_ACTn	12	GND
13	GND	14	LED_LINKn
15	ETH_GND	16	ETH_GND

Figure 2-12. RJ45 Connector

Figure 2-13 shows the Ethernet MATEnet connector, and Table 2-6 provides the connector pin details.

Table 2-6. J4 Pin Assignment

Pin Number	Description	Pin Number	Description
1	TRD_P	2	TRD_M
S1	GND	S2	GND
S3	GND	S4	GND
S5	GND	S6	GND

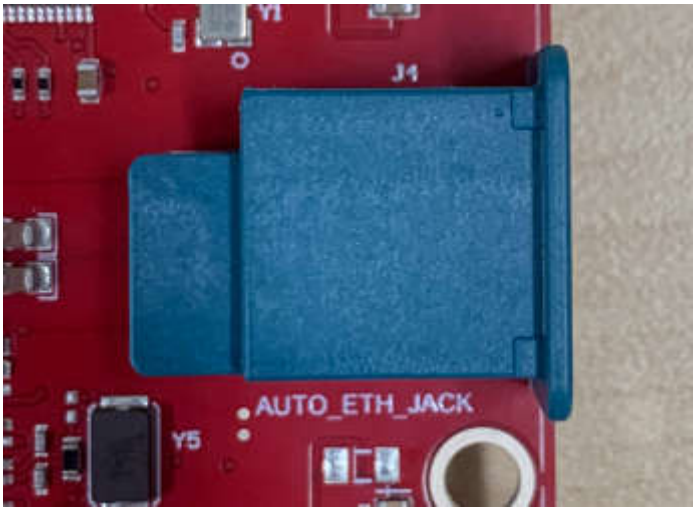


Figure 2-13. MATEnet Connector

2.4.5.1 ECOs to Enable the DP83TC812R (AWR2944EVM) or DP83TG720S (AWR2944PEVM) PHY

By default, the board is designed to be used with the DP83867E PHY with the RJ45 connector. To enable the DP83TC812R PHY with the MATEnet connector, the following hardware changes must be made. For help with locating these components on the PCB, refer to the provided Schematic, BOM, and assembly files.

1. Remove R98 and populate on R74
2. Remove R101 and populate on R230
3. Remove R103 and populate on R96
4. Remove R105 and populate on R100
5. Remove R121 and populate on R178
6. Remove R122 and populate on R225
7. Remove R195 and populate on R245
8. Remove R290 and populate on R234
9. Remove R325 and populate on R237
10. Remove R336 and populate on R238
11. Remove R338 and populate on R239
12. Remove R339 and populate on R240
13. Remove R413 and populate on R247
14. Remove R369 and populate on R249
15. Populate D18 and D19 ESD diodes
16. Populate C55
17. The bootstrap configuration pins can be populated/removed as needed depending on the use case

Note

The automotive Ethernet PHY (U4) and port (J4) on the AWR2944EVM have not been tested by Texas Instruments to be compliant with any regional standards such as Radio Equipment Directive 2014/53/EU. If the user wishes to populate the components necessary to utilize this port, then users can do any necessary testing to verify that the port is compliant with all applicable regional standards before use. Any modifications done to enable the J4 port invalidates the existing RED 2014/53/EU certification of the AWR2944EVM.

2.4.5.1.1 ECO needed to source 25MHz clock from AWR2944P to DP83TG720S

1. Populate R385
2. Populate R212
3. Remove crystal Y5

2.4.6 USB Connectors (J8, J10)

Note

The EVM must be powered on before the USB cables are connected. Plugging in the USB cables before powering on the board can cause the board to get stuck in a permanent reset state. In the event that this occurs, just unplug the USB cables, power cycle the EVM, and plug in the USB cables to resolve the issue.

The AWR2944EVM/AWR2944PEVM has two standard micro USB connectors.

Micro USB Connector J10 provides access to the AWR2944 UART, SPI, I2C, RS232, and SOP interfaces through the FTDI chip.

Table 2-7. J10 Pin Assignment

Pin Number	Description	Pin Number	Description
1	FTDI_VBUS	2	FTDI_USBD_N
3	FTDI_USBD_P	4	FTDI_USBID
5	GND	6	GND
7	GND	8	GND
9	GND	10	GND
11	GND		

Figure 2-14. FTDI USB Port

Micro USB connector J8 provides access to the JTAG, MSS_UARTA, and MSS_UARTB interfaces of the AWR2944 via the XDS110 emulator.

This is the UART interface used to flash the binary to the onboard serial flash and for Out-of-box (OOB) demo.

Note

The OOB demo requires only J8 to be connected to the PC. J10 is not used for the OOB demo.

Table 2-8. J8 Pin Assignment

Pin Number	Description	Pin Number	Description
1	XDSET_VBUS	2	XDSET_D_N
3	XDSET_D_P	4	XDSET_ID
5	GND	6	GND
7	NC	8	NC
9	GND	10	GND
11	GND		

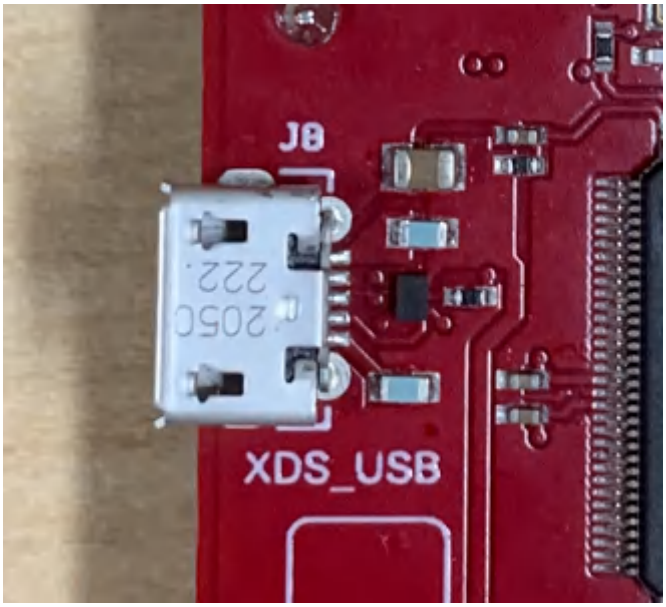


Figure 2-15. XDS USB Port

2.4.7 OSC_CLKOUT Connector (J14)

Connector J14 provides access to measure oscillator clock out signal from the AWR2944 device.

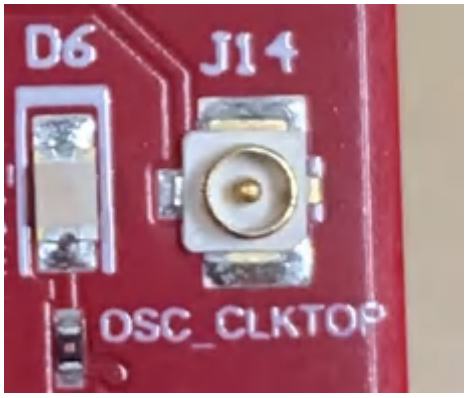


Figure 2-16. OSC Clock Port

2.4.8 PMIC SPI Connector (J16) (DNP)

Connector J16 provides access to the SPI and enable pins on the PMIC (U8). This part is not populated by default. To populate this connector with the appropriate part, please refer to the Schematic, BOM, and assembly files.

Table 2-9. J8 Pin Assignment

Pin Number	Description	Pin Number	Description
1	PMIC SPI_CS	2	PMIC SPI_PICO
3	PMIC SPI_CLK	4	NC
5	PMIC SPI_POCI	6	PMIC ENABLE

2.4.9 Voltage Rails Ripple Measurement Connectors (J1, J5) (DNP)

J1 provides access to measure ripple on 1V0_FILTERED (1.0 analog RF supply for AWR2944) voltage rail.

J5 provides access to measure ripple on 1V8_FILTERED (1.8V analog supply for AWR2944) voltage rail.

These connectors are not populated on the board by default. To populate these connectors with the appropriate part, please refer to the schematic, BOM, and assembly files.

2.5 Antenna

The AWR2944EVM/AWR2944PEVM includes etched antennas onboard for the four receivers and four transmitters, which enables tracking multiple objects with the distance and angle information. This antenna design enables estimation of both azimuth and elevation angles, which enables object detection in a 3D plane (see Figure 2-17).

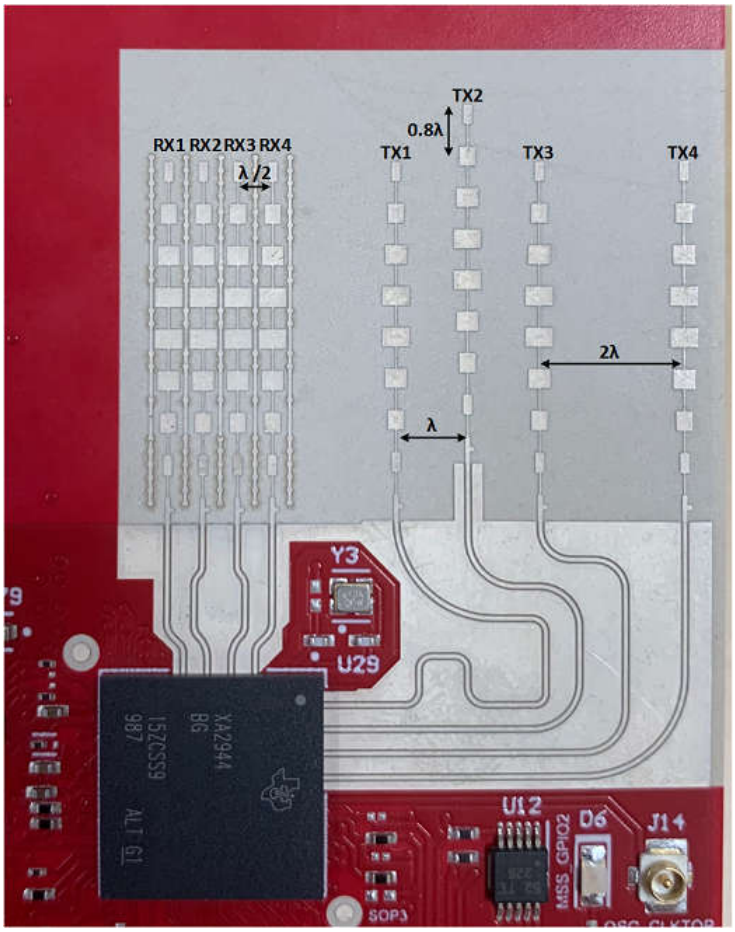


Figure 2-17. AWR2944EVM Antenna Design

The antenna placement shown in Figure 2-17 results in the virtual antenna array shown in Figure 2-18.

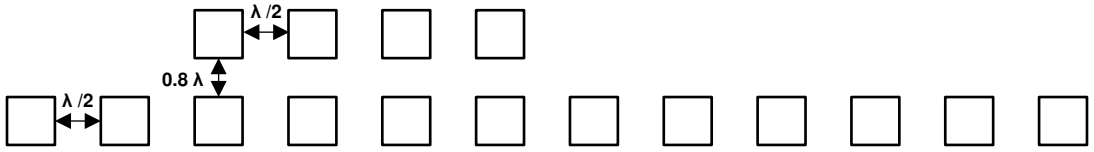


Figure 2-18. Virtual Antenna Array

The antenna peak gain is 13dBi across the frequency band of 76 to 81GHz. The radiation pattern of the antenna in the horizontal plan (H-plane) and elevation plan (E-plane) is as shown in Figure 2-19 and Figure 2-20, respectively.

The beamwidth of the antenna design can be determined from the radiation patterns provided below. For example, based on 3dB drop in the gain as compared to bore sight, the horizontal 3dB-beamwidth is approximately ±30 degrees (see Figure 2-19), and elevation 3dB-beamwidth is approximately ±3 degrees (see Figure 2-20). Similarly, the horizontal 6dB beamwidth is approximately ±45 degrees (see Figure 2-19) and the elevation 6dB-beamwidth is approximately ±5 degrees (see Figure 2-20).

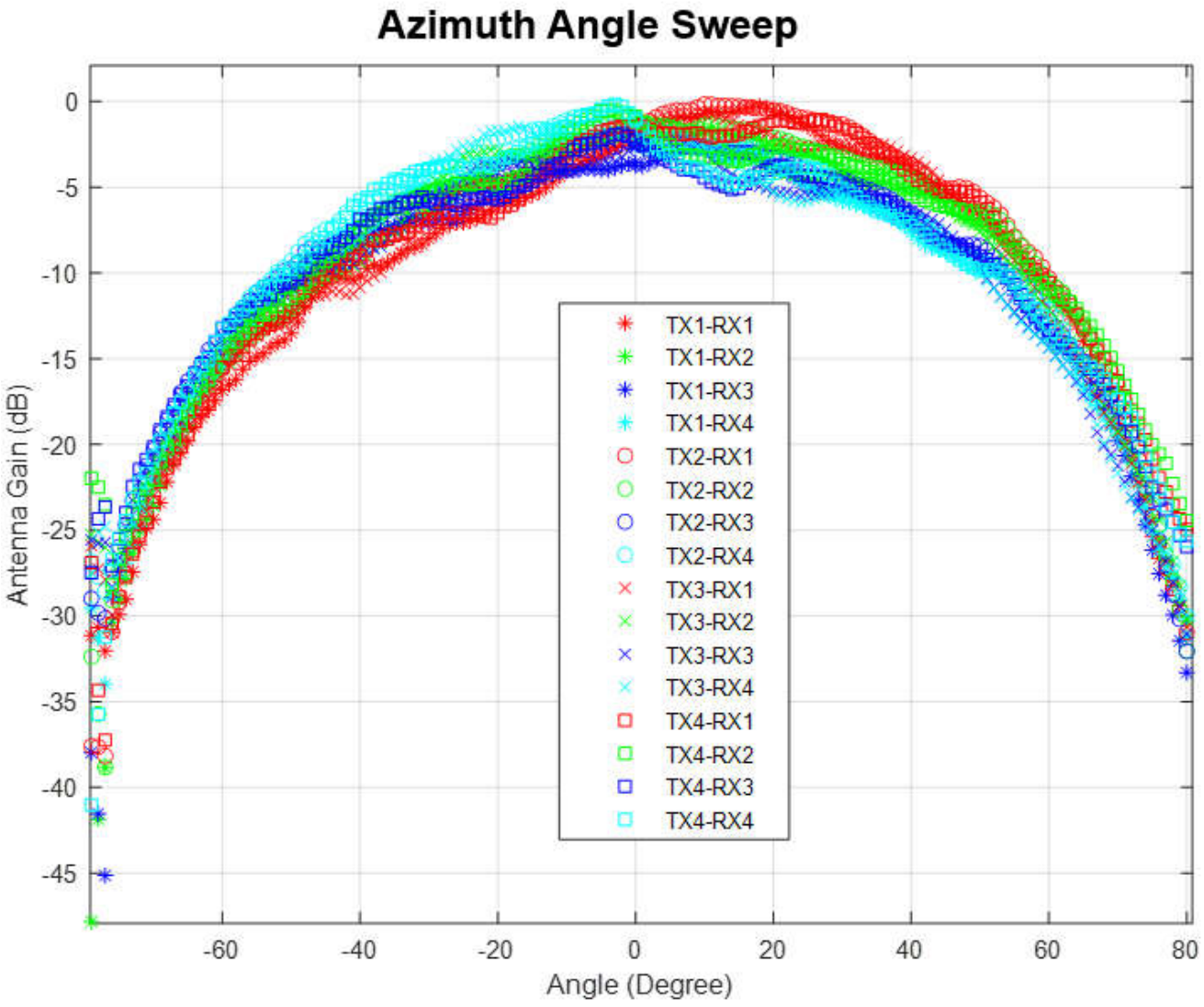


Figure 2-19. Azimuth Radiation Pattern

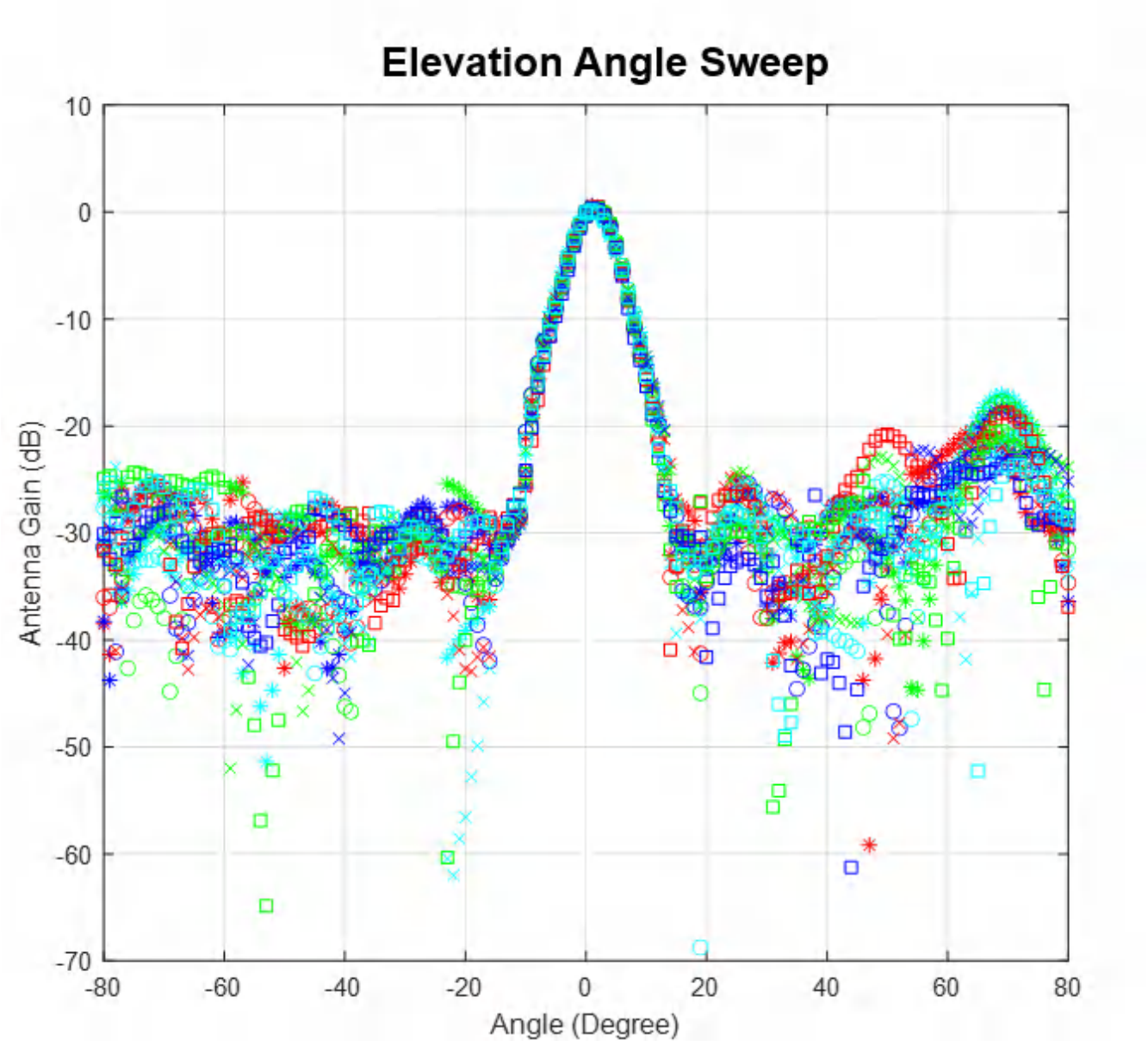


Figure 2-20. Elevation Radiation Pattern

2.6 PMIC

Power to the AWR2944 is provided by the LP877451-Q1 PMIC. This is a functional safety compliant PMIC that supports ASIL-C/SIL-2 applications. For more details, visit the LP87745-Q1 product page (https://www.ti.com/product/LP87745-Q1).

2.7 On-Board Sensors

The AWR2944EVM/AWR2944PEVM provides access to an on-board temperature sensor (TMP112AQDRLRQ1) and four on-board current sensors (INA228AIDGST). These sensors can be controlled by the radar via I2C.

The current sensors are designed to measure the current being supplied to the various power rails of the xWRL6432AOP device. For details on the supply rails that can be measured using the current sensors, refer to Table 2-10.

Table 2-10. Current Sensor Supply Details

Reference Designator	Supply Node	PCB Net Name
U6	1.8V Supply	REG_1V8
U7	3.3V Supply	VCC_3V3
U8	1.2V Supply	REG_1V2
U25	1.2V RF Supply	REG_RF_1V2

2.8 PC Connection

The PC connectivity is provided via two micro USB connectors, J8 and J10.

2.8.1 XDS110 Interface

J8 provides access to the onboard XDS110 (TM4C1294NCPDT) emulator. This connection provides the following interfaces to the PC:

- JTAG for CCS connectivity
- MSS logger UART (can be used to get MSS code logs on the PC)

When the J8 USB is connected to the PC, the device manager recognizes two XDS110 COM ports under Ports (COM and LPT).

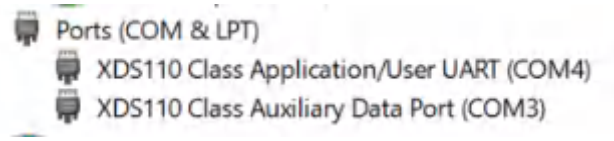


Figure 2-21. XDS110 COM Ports

XDS110 debug probe and data port are detected under Texas Instruments Debug Probes.

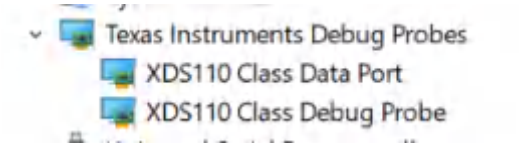


Figure 2-22. TI Debug Probes

If the PC is unable to recognize the above COM ports, then install the latest EMUpack.

2.8.2 FTDI Interface

J10 provides access to the onboard FTDI ports. This provides the following interfaces to the PC:

- FTDI Port A -> SPI.
- FTDI Port B-> Host INTR signal.
- FTDI Port C -> NRESET control signal.
- FTDI Port D -> SOP0, SOP1 control signals.

When the USB is connected for the first time to the PC, a possibility is that Windows® does not recognize the device. This is indicated in the device manager with yellow exclamation marks, as shown in Figure 2-23.

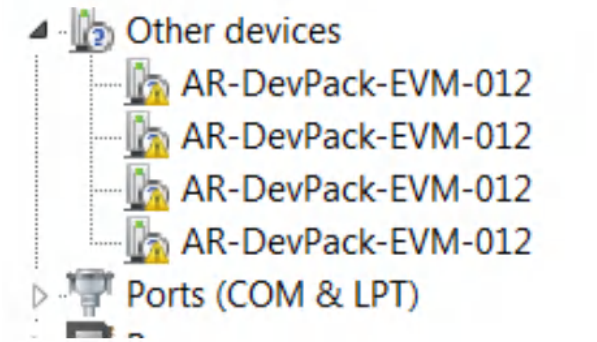


Figure 2-23. Uninstalled FTDI Drivers

To install the devices, download the latest FTDI drivers available in the mmwave SDK package. Right click on these devices, and update the drivers by pointing to the location where the FTDI drivers were installed (C:\ti\mmwave_sdk_<version_number>\tools\ftdi). This must be done for all four COM ports. When all four COM ports are installed, the device manager recognizes these devices and indicates the COM port numbers, as shown in Figure 2-24.

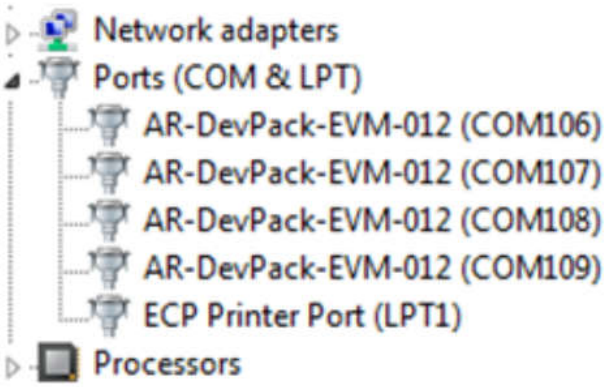


Figure 2-24. Installed FTDI Drivers

2.9 Connecting the AWR2944EVM/AWR2944PEVM to the DCA1000 EVM

The AWR2944EVM/AWR2944PEVM can be connected to the DCA1000 EVM platform to allow for LVDS data streaming. Figure 2-25 shows the AWR2944EVM/AWR2944PEVM interfaced to the DCA1000 EVM.

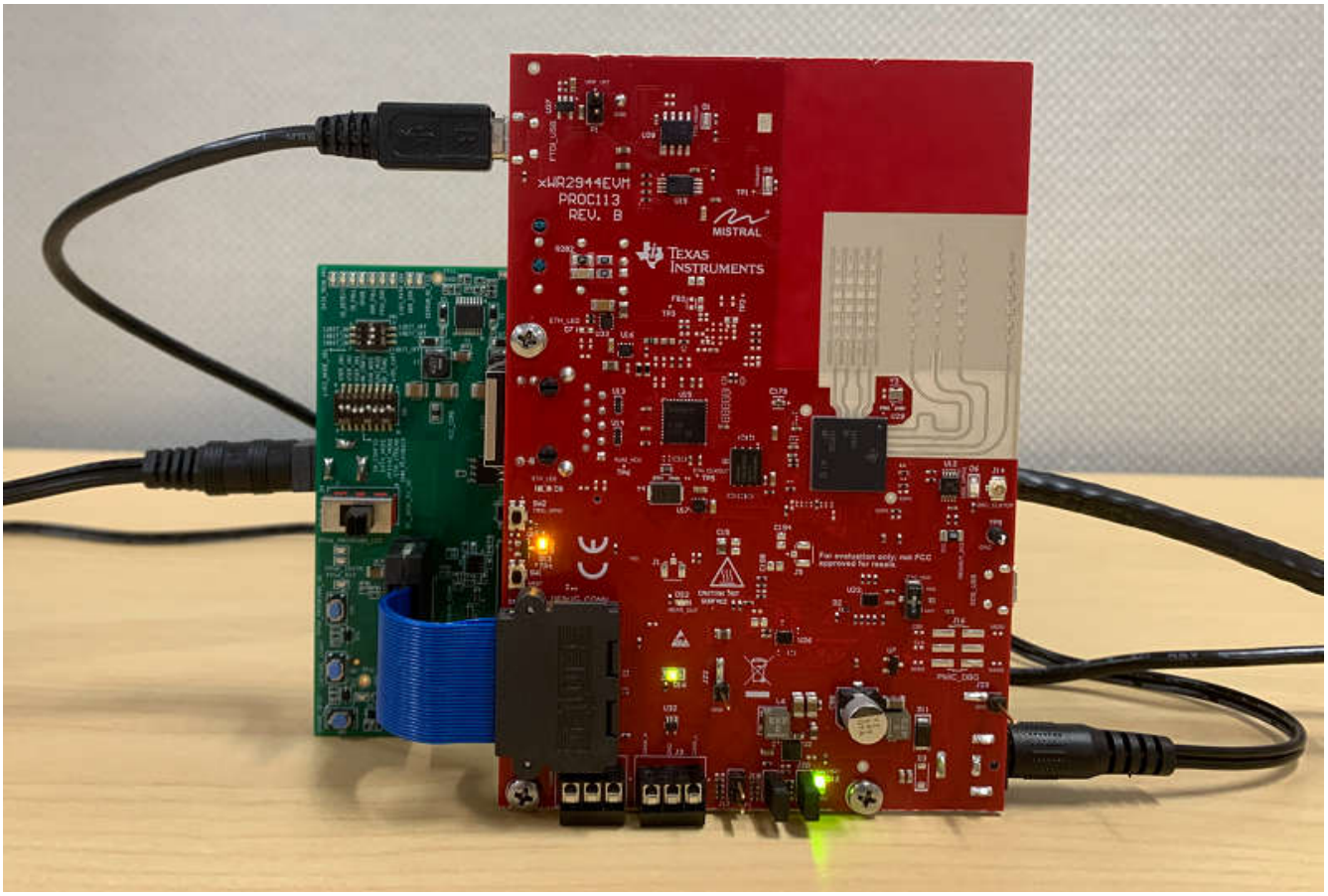


Figure 2-25. AWR2944EVM and DCA1000 EVM

When using the AWR2944EVM/AWR2944PEVM with the DCA1000 EVM, the following settings must be used.

1. Set the AWR2944EVM/AWR2944PEVM to SOP2 mode.

Figure 2-26. SOP2 Mode

2. Set the DCA1000 EVM switches to the following configuration.

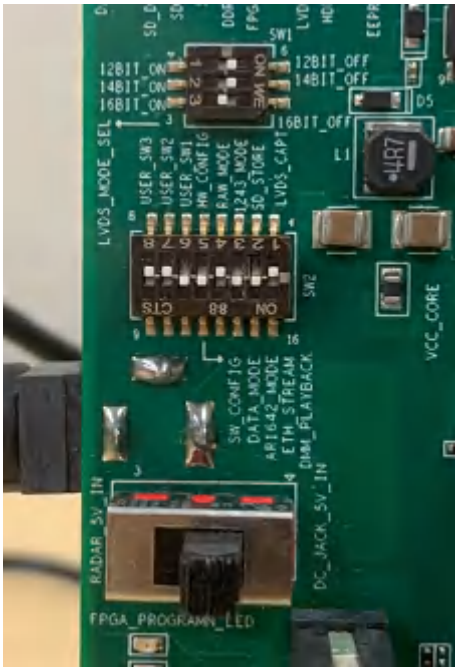


Figure 2-27. DCA1000 Switch Settings

3. The 12V supply must be connected to J12 on the AWR2944EVM/AWR2944PEVM.
4. A 5V supply must be connected to J2 on the DCA1000 EVM.
5. A micro USB cable must be connected to the FTDI port on the AWR2944EVM/AWR2944PEVM (J10).
6. The Samtec ribbon cable must be connected to J7 on the AWR2944EVM/AWR2944PEVM and J3 on the DCA1000 EVM.
7. An RJ45 cable must be connected to J6 on the DCA1000 EVM.

2.10 Jumpers, Switches, and LEDs

2.10.1 Switches

The AWR2944EVM contains two switches to mux various interfaces to different connectors on the EVM.

Table 2-11. MUX Switches

Reference	Usage	Comments	Image
S1	JTAG	When set to 'MIPI' position, the JTAG interface is routed to the MIPI 60-pin connector (J19). When set to 'XDS' position, the JTAG interface is routed to the XDS110 USB interface (J8)	

Table 2-11. MUX Switches (continued)

Reference	Usage	Comments	Image
S2	SPI	When set to 'PMIC_SPI' position, the MSS_SPIB interface is routed to the PMIC and to the J16 header. 1 When set to 'DBG_SPI', the MSS_SPIB interface is routed to the 60-pin debug header (J7)	

1. DNP resistors R5, R61, R167, and R176 must be populated to bring the MSS_SPIB interface out to the J16 header.

2.10.2 Sense On Power (SOP) Jumpers (J17, J18, J20)

The AWR2944EVM/AWR2944PEVM can be set to operate in different modes based on the state of the SOP [2:0] lines. These lines are sensed ONLY during boot up of the AWR2944 device. The state of the device is described in Table 2-12.

A closed jumper refers to a '1' and open the jumper refers to a '0' state of the SOP signal going to the AWR2944 device.

Note

The SOP[2:0] pins can also be controlled via the onboard FTDI. In this case, the FTDI settings override the jumper settings.

Table 2-12. SOP[0:2] Modes

Reference	Usage	Comments
J17 (SOP 2), J18 (SOP 1), J20 (SOP 0)	SOP[2:0]	101 (SOP mode 5) = Flashing mode 001 (SOP mode 4) = Functional mode 000 (SOP mode 3) = Reserved 011 (SOP mode 2) = Development mode 010 (SOP mode 1) = Reserved

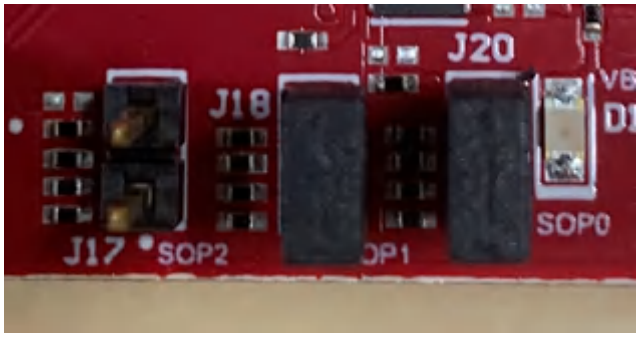


Figure 2-28. SOP Jumpers

Additionally, the SOP[4:3] signals defines the XTAL clock input as per the below configurations provided in Table 2-13.

Table 2-13. SOP[4:3] Modes

Reference	Usage	Comments
R303, R312 Populated. R301,R309 unpopulated	SOP[4:3]	00 = 40MHz (Default state)
R301, R312 Populated. R303,R319 unpopulated		01 = 45.1584MHz
R303, R309 Populated. R301,R312 unpopulated		10 = 49.152MHz
R301, R309 Populated. R303,R312 unpopulated		11 = 50MHz

2.10.3 I2C Connections

The board features temperature sensor for measuring onboard temperature, current sensors for current measurement for 1.2V, 1.8V, 3.3V, 1V0_RF1, and 1V0_RF2 AWR2944 supply rails and EEPROM for storing board ID. These are connected to the AWR2944EVM/AWR2944PEVM through I2C bus.

Table 2-14 shows the list of I2C devices available in AWR2944EVM/AWR2944PEVM board and the address.

Table 2-14. I2C Device Addresses

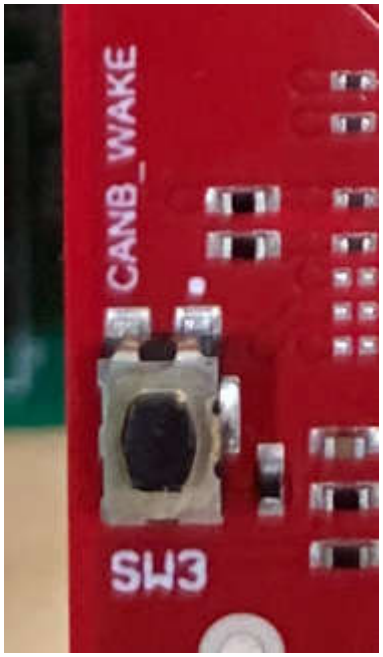
Sensor Type	Reference Designator	Part Number	Target Address
Temp sensor	U24	TMP112AIDRLR	0x49
Current sensor for 3.3V rail	U12	INA226AIDGSR	0x44
Current sensor for 1.8V rail	U11	INA226AIDGSR	0x41
Current sensor for 1.2V digital rail	U9	INA226AIDGSR	0x40
Current sensor for 1.0V RF1 rail	U22	INA226AIDGSR	0x42
Current sensor for 1.0V RF2 rail	U30	INA226AIDGSR	0x43
EEPROM	U28	CAV24C02WE-GT3	0x50

2.10.4 Push Buttons

Table 2-15. Push Button Switches

Reference	Usage	Comments	Image
SW1	RESET	This Switch is used to RESET the AWR2944, PMIC, XDS110 and FTDI device.	

Table 2-15. Push Button Switches (continued)

Reference	Usage	Comments	Image
SW2	GPIO_28	When pushed, the GPIO_28 shall be pulled to High.	
SW3	CANB_WAKE	Used to Wake up the CANB Transceiver	

2.10.5 LEDs

Table 2-16. On Board LEDs

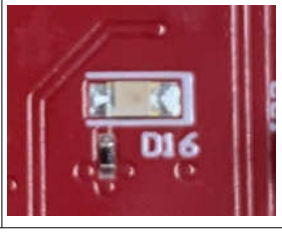
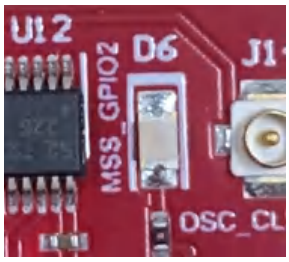
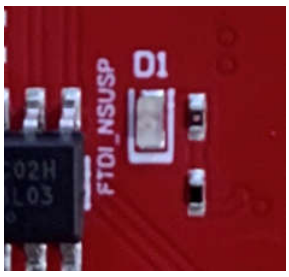
Ref	Color	Usage	Comments	Image
D12	Green	12V supply indication	This LED indicates the presence of 12V supply input.	
D16	Green	5V Supply	This LED indicates the presence of 5V supply output.	

Table 2-16. On Board LEDs (continued)

Ref	Color	Usage	Comments	Image
D13	Yellow	NRST	This LED is used to indicate the state of NRST pin. If this LED is glowing, then the device is out of reset.	
DS2	Red	NERROUT	Glows if there is any HW error in the AWR2944 device.	
D9	Yellow	WRMRST	Open drain fail safe warm reset signal.	
D6	Green	GPIO_2	Glows when the GPIO_2 is logic-1.	
D1	Yellow	FTDI_SUSPEND_N	Glows when FTDI is in suspend state.	

3 Software

3.1 Software, Development Tools, and Example Code

To enable quick development of end applications on the on-chip C66x DSP, ARM® Cortex®-R5F controller, and hardware accelerator (HWA 2.1), TI provides a software development kit (SDK) that includes demo codes, software drivers, emulation packages for debug, and more. These can be found at mmwave-sdk.

4 Hardware Design Files

4.1 Design Files

To view the schematics, assembly drawings, and BOM, see AWR2944EVM Schematic, Assembly Files, and BOM.

To view the design database and layout details, see AWR2944EVM Database and Layout Files.

To view the schematics, assembly drawings, and BOM, see AWR2944PEVM Schematic, Assembly Files, and BOM.

5 Compliance Information

5.1 Requirements for Operating in the EU and UK regions

The following requirements must be met when operating the AWR2944EVM in the EU and UK.

- The tested operating bandwidths for Radio Equipment Directive 2014/53/EU and UKCA compliance are 900MHz (77.45GHz center frequency) and 3900MHz (78.95GHz center frequency). The maximum peak EIRP is approximately 37dBm for the 900MHz bandwidth and 34dBm for the 3900MHz bandwidth.
  1. If users choose to operate the EVM outside of the specified operating bandwidth and operating power as described above, then the EVM must be operated inside a shielded chamber.
- When operating in the 77GHz to 81GHz region, users must not enable more than one simultaneous TX for 0dB backoff or enable a minimum of 10dB TX backoff for multiple simultaneous TX to meet the -3 dBm limit for mean power spectral density.
- The automotive Ethernet PHY (U4) and port (J4) on the AWR2944EVM have not been tested by Texas Instruments to be compliant with any regional standards such as Radio Equipment Directive 2014/53/EU. If users wish to populate the components necessary to utilize this port, then users can do any necessary testing to verify that the port is compliant with all applicable regional standards before use. Any modifications done to enable the J4 port invalidate the existing RED 2014/53/EU certification of the AWR2944EVM.
- The RJ45 port (J9) has been tested to be compliant with the Radio Equipment Directive 2014/53/EU and UKCA requirements using an unshielded, symmetrical indoor CAT5 or higher Ethernet cable with a maximum length of 3 meters. If users wish to operate the AWR2944EVM with an Ethernet cable that does not meet these specifications, then users can do any necessary testing to verify that the AWR2944EVM and Ethernet cable is compliant with all applicable regional standards before use.
- The AWR2944EVM has been tested to be compliant with the Radio Equipment Directive 2014/53/EU and UKCA requirements using a DC power cable with a maximum length of 3 meters. If users wish to operate the AWR2944EVM with a longer DC power cable length, then users can do any necessary testing to verify that the AWR2944EVM and DC power cable is compliant with all applicable regional standards before use.
- The AWR2944EVM has been tested to be compliant with the Radio Equipment Directive 2014/53/EU and UKCA requirements using a USB cable with a maximum length of 3 meters. If users wish to operate the AWR2944EVM with a longer USB cable length, then users can do any necessary testing to verify that the AWR2944EVM and USB cable is compliant with all applicable regional standards before use.
- The AWR2944EVM has not been assessed for the interactive control of a vehicle and any such use requires an additional assessment of applicable functional safety of the vehicle’s control systems.

6 Additional Information

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7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2023) to Revision C (September 2024) **Page**

Changes from Revision A (March 2023) to Revision B (August 2023) **Page**

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