Technical Article

Can a Clock Generator Act as a Jitter Cleaner?

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I'm excited to have the opportunity to address clock generators and jitter cleaners. My goal is that after reading this post, you will not stereotype a clock generator as a device that can't also perform jitter cleaning. I will discuss the difference between clock generators and jitter cleaners, cover some key points about phase-locked loops (PLLs), and discuss the performance characteristics of wide- and narrow-loop bandwidth PLL phase-noise plots as applied to clock generators and jitter cleaners.

Definitions

Clock generators can produce at least two output frequencies that are locked to the input clock. At least one frequency does not divide evenly into the input clock frequency. Clock generators typically consist of a single PLL, which often performs frequency multiplication (Figure 1). Jitter cleaners can produce at least one output frequency that is locked to the input clock and has lower jitter. Dual loop jitter cleaners consist of two cascaded PLLs (Figure 2). The first PLL is responsible for the jitter cleaning and the second PLL performs the frequency multiplication.

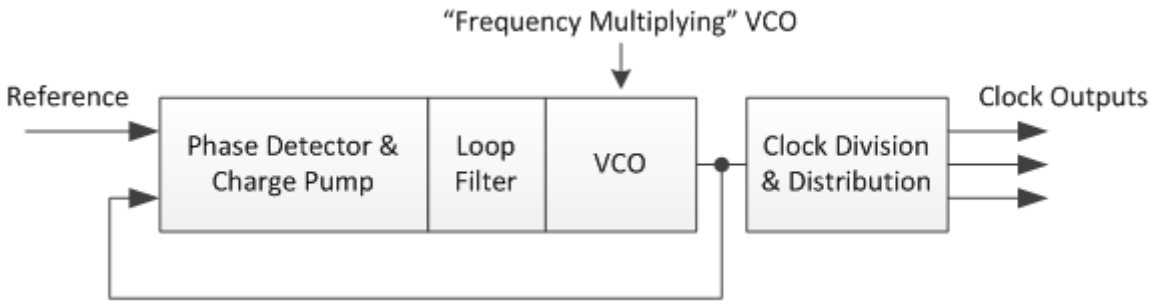

Figure 1. Single-loop Clock Generator

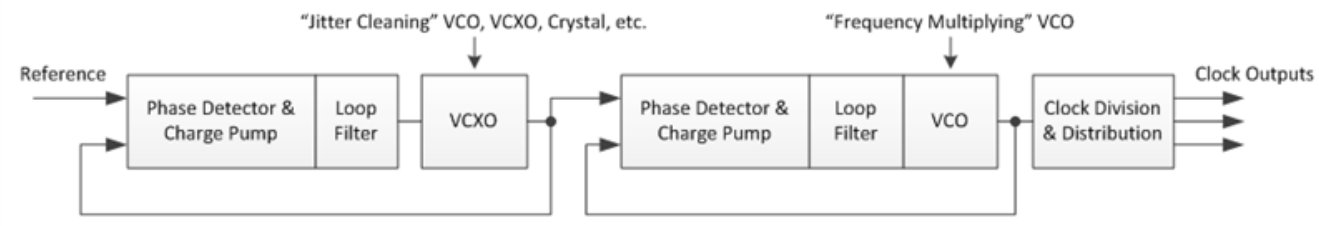

Figure 2. Dual-loop Jitter Cleaner

Key Points about PLLs

Three things to understand about PLLs:

- Every PLL is a jitter cleaner or a jitter dirtier depending on the relative performance of the reference, the PLL and the voltage-controlled oscillator (VCO).
- It is the VCO that does the "jitter cleaning," but in some cases the VCO could actually be adding noise, depending on the VCO phase-noise performance and the PLL's loop bandwidth relative to the noise of the reference.

- PLL performance typically improves with a higher phase-detector frequency and charge-pump current. You could consider PLL noise (meaning noise related to the phase detector and charge pump) to be the “noise cost” to lock the reference to the VCO.

It’s important to understand the impact of the VCO in a PLL system. The PLL’s loop filter serves as a low-pass filter to the reference and PLL noise and as a high-pass filter to the VCO noise. VCOs that use a quartz crystal (VCXO) have relatively high quality factors (Q), giving them excellent phase-noise performance compared to VCOs that use an LC tank with relatively low Q. Depending on the VCO technology, like surface acoustic wave (SAW) or coaxial-resonator oscillator (CRO), the Q associated with the design of the VCO will determine its phase-noise performance. Although high-Q VCXOs have good phase-noise performance, they also have limited maximum frequency, whereas other technologies enable multi-gigahertz VCOs that allow clock generators to provide many different output frequencies using clock output dividers. On-chip VCOs today have performance comparable to external-module VCOs.

Performance Characteristics of Clock Generators and Jitter Cleaners

The typical use case of a clock generator is to accept a clean reference into the PLL, which operates with a wide-loop bandwidth to attenuate the low offset phase noise of a VCO, especially VCOs with a low Q. Because the reference is clean the output has jitter/phase noise limited only by the specifications of the clock generator. Ideally a reference frequency is chosen to allow close to maximum phase detector frequency operation for best PLL performance.

Figure 3 shows a typical PLL phase-noise plot with a wide-loop bandwidth showing the noise contribution of reference, PLL and VCO. If the reference is noisy, it could exceed the PLL noise at offsets below the loop bandwidth and even bleed into the VCO region.

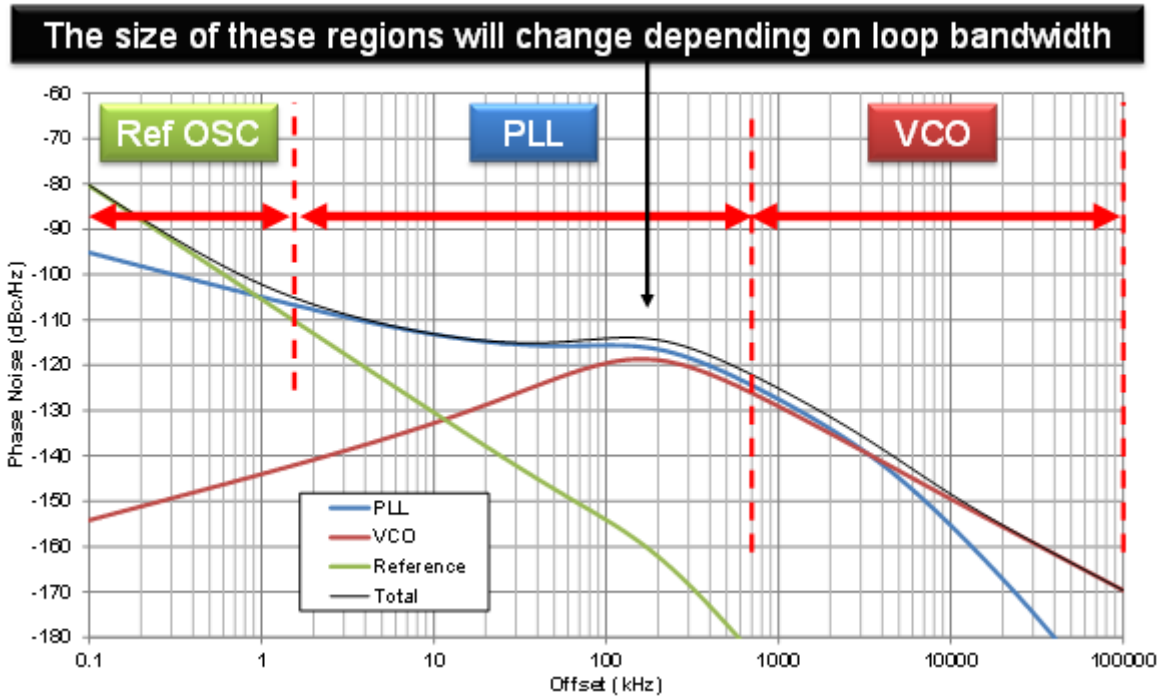

Figure 3. Typical Phase Noise of a PLL with a Wide Loop Bandwidth

The typical use case of a dual loop jitter cleaner is to accept a dirty or low-frequency reference into the first PLL, which operates with a very narrow-loop bandwidth to attenuate reference and PLL noise. This makes the VCO, or a high-Q VCXO, dominate reference noise to the second PLL which behaves as a clock generator described above. Figure 4 shows a typical PLL phase-noise plot with a narrow-loop bandwidth. The VCO is capable of “cleaning” both the reference oscillator and PLL noise. In a dual loop jitter cleaner, Figure 4 is the output of the first PLL used as a clean reference to the second PLL. In a single loop jitter cleaner, this cleaned output is

at or higher than the frequency required by the application and a second stage frequency multiplication is not required.

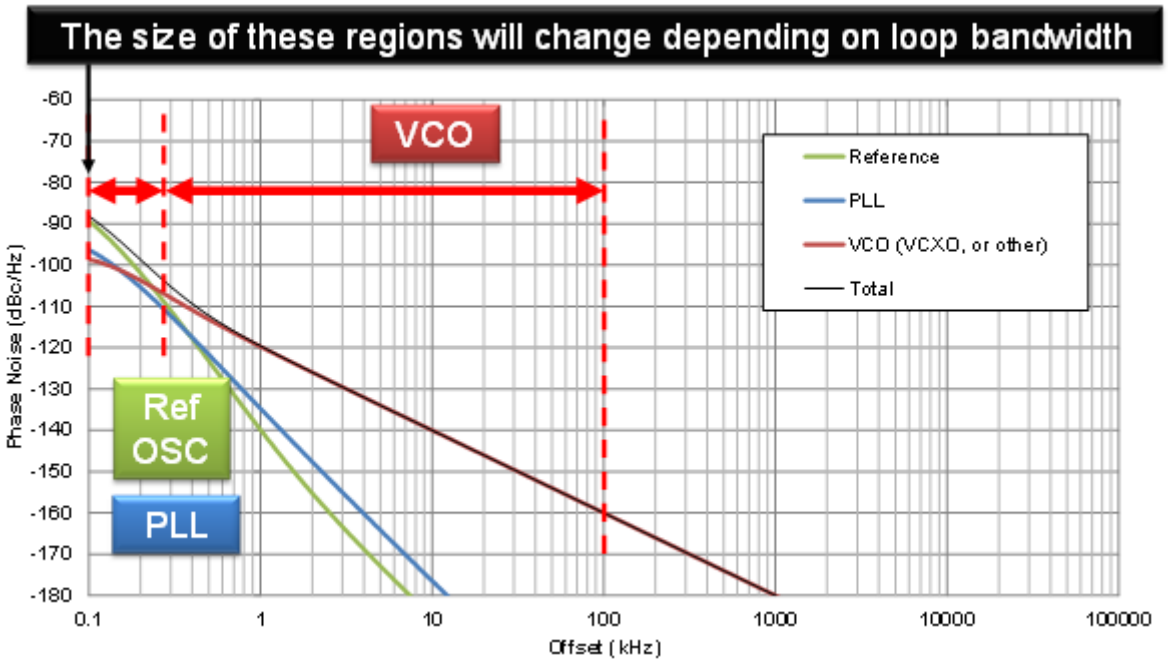

Figure 4. Typical Phase Noise of a PLL with a Narrow-loop Bandwidth

Take-aways

For your application which requires jitter cleaning, a single loop clock generator with an integrated VCO configured with a narrow-loop bandwidth loop filter can clean jitter. If the clock generator has a low-Q VCO, its phase-noise performance won't be quite as good as a high-Q VCXO, but may "clean" the jitter on the reference to meet the application phase noise or jitter requirements. This is more likely true when the jitter integration range is above 10 kHz offset. Using a single-loop clock generator with an integrated VCO reduces the total number of system components required for jitter cleaning.

When you begin designing, consider the WEBENCH® Clock Architect or PLLatinum™ simulator tool for simulating phase-noise performance of TI clock generators and jitter cleaners. By loading these tools with the phase noise of your reference and any external VCO/VCXOs, you can simulate system phase noise. The tools also enable custom jitter integration ranges to determine jitter for any given integration bandwidth.

Additional Resources

- Get started now with the LMK03328 ultra-low-jitter clock generator evaluation module (EVM).
- Download the app notes:
  - Using the LMK03000C to Clean Recovered Clocks.
  - CPRI Repeater System.

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