Technical Article

Biasing an SR Controller IC in USB Smartphone Charging Applications

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With the increased interest in energy efficiency and energy conservation, a synchronous rectifier (SR) helps boost efficiency when converting offline AC power into 5V for USB smartphone battery charging. During this conversion, an SR controller integrated circuit (IC) needs proper biasing in order to provide the adequate drive to the SR MOSFET. The bias voltage is typically above 4V in USB applications. Because the BC1.2 USB battery-charging standard specifies a power adapter output in the range of 4.1V to 6V, you can bias SR controller ICs from that output, as shown in Figure 1.

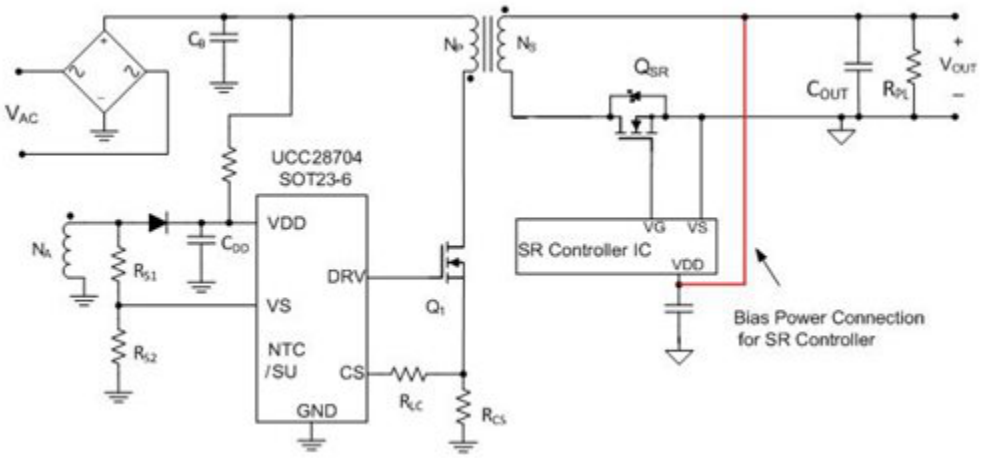

Figure 1. Flyback Converter with the SR Controller Biased from the Output Voltage

What If the Output Voltage Drops below UVLO?

This biasing approach is simple, easy and has almost no additional cost. It works well when the output voltage is above 4V, but at <4V on VDD, the SR controller IC enters undervoltage lockout off (UVLO). The issue here is that the SR still needs to be operational when the output drops below 4V. In fact, it still needs to be operational before the output drops to 3V in USB smartphone applications. This is because battery-charging operations require constant-current operation, where an adapter keeps delivering constant current while its output voltage falls to help operations such as battery charging during dynamic power management (DPM).

Figure 2 illustrates typical 5V-3A power adapter output characteristics. Operation ceases when the output drops to 3V because at 3V, the lithium-ion battery cannot charge; thus, no bias power is necessary for the SR. As a matter of fact, a fault is actually identified when high current is present at ≤3V.

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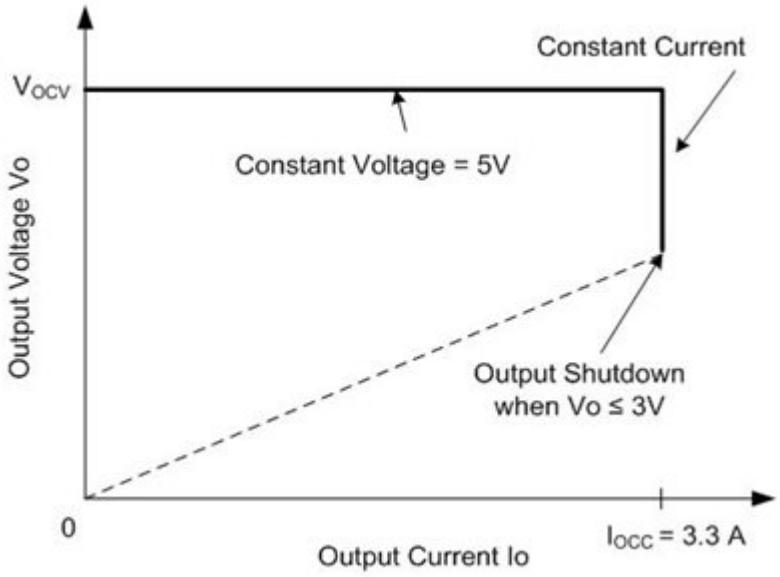

Figure 2. Typical 5V-3A Power Adapter Output Characteristics

When the output drops below 4V, the SR turns off, which causes undesired performance. First, the SR turn-off causes a constant current shift due to the voltage increase from the body-diode conduction, leading to unnecessary transients. Second, the current flowing through the SR MOSFET (Q_{SR}) channel now flows through its body diode. The resulting higher-power losses may cause a temperature rise that could cause thermal runaway and damage. Therefore, you need alternative approaches to keep the SR on before the output drops to 3V.

Biasing an SR Controller Using a Charge Pump

One alternative is to use a charge-pump circuit. Figure 3 explains the operation of a charge pump with the circuit. The VDD voltage on capacitor C2 is brought up to 2x Vp by switching S1 and S2 will alternate switching on/off, when the Vp pin is connected to the adapter output after the detected output voltage drops below 4V. As the output is between 3V and 4V, the SR bias voltage VDD is maintained at 6V to 8V, thus achieving the desired SR bias voltage.

This approach needs additional components and control functions to set up proper timing for S1 and S2. You can integrate these components and control functions inside an IC to simplify application designs, but you will still need three dedicated pins and a capacitor (C1) to fulfill the function.

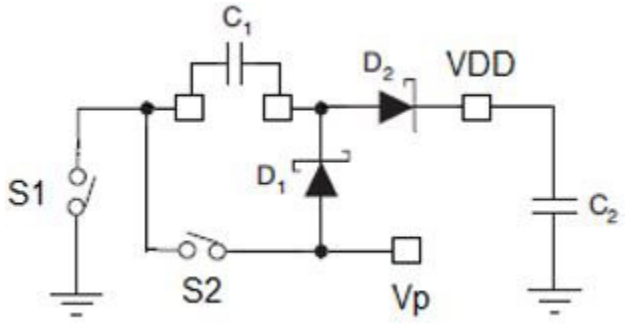

Figure 3. Charge-pump Biasing

Biasing an SR Controller Using a Linear Regulator

The SR MOSFET drain pin is applied with a pulse train during flyback converter operation. The pulse magnitude is well above 4V in USB smartphone power adapter designs. Figure 4 shows a linear regulator that can be used

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to regulate the linear regulator output to 5V which is connected to the SR controller VDD pin. But because you have to add four additional components, this approach becomes less attractive due to the increase of both cost and board space.

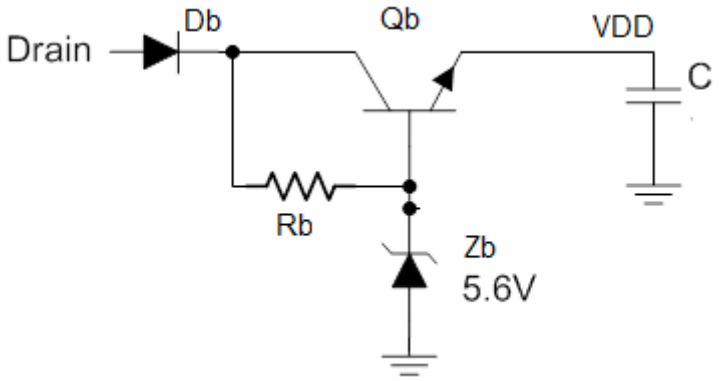

Figure 4. Pulse Linear-regulator Biasing

Biasing an SR Controller Using a Simple Regulator

As these first two approaches are generally not preferable in USB smartphone charging applications given their cost and complexity, newly developed SR controller ICs such as the UCC24636 accept a simpler bias approach using a “simple regulator,” as shown in Figure 5.

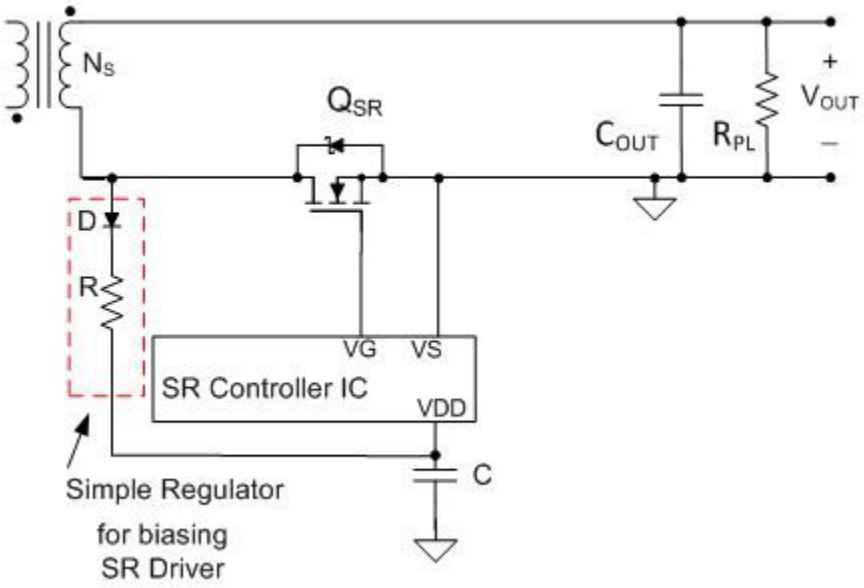

Figure 5. Simple Regulation Bias

The bias VDD pin accepts a wide voltage range from 4V to 30V – and the driver output is internally clamped to the MOSFET’s gate-voltage level, 10V. These features enable a simple regulator (placed externally with a diode and a resistor) to charge the VDD capacitor to a proper level across the input and load range. When the drain pin voltage is pulsing, the diode (D) rectifies the pulses, while the resistor (R) and capacitor (C) average out the pulses to deliver DC voltage and power to VDD.

Table 1 provides biasing results based on the TI Designs Universal AC Input to 5V/3A Output Reference Design, which employs the UCC28704 and UCC24636, a universal offline input, and a 5V-3A output flyback converter.

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Table 1. Simple Regulator Biasing Results

Vin	Vo condition	VDD (V)
80 to 85Vac	No Load SR VDD	8.78
	Vo = 3V SR VDD	4.57
230Vac	Vo = Vo(max) Iocc SR VDD	21.8
	Vo =3V SR VDD	18.2
265Vac	Vo = Vo(max) Iocc SR VDD	25.3

R = 309Ω C = 1.0µF

The results depict a minimum controller VDD voltage above 4.57V even if the converter output drops to 3V, thus maintaining plenty of bias voltage to keep the UCC24636 in operation.

When converting offline AC power into 5V for USB smartphone battery charging, an SR controller can help boost efficiency when biased properly.

Additional Resources:

- Read the blog post: USB Type-C: charging a new world
- Discover more about the UCC28704:
  - UCC28704 user guide
  - Get to know the design tools for the UCC28704, including a SPICE model, WEBENCH® Designer calculator, Excel calculator, MathCAD calculator

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