Application Report
SWCA286A–October 2014–Revised March 2017

TPS659038-Q1 and TPS659039-Q1 Operation With Higher Capacitive Loading

Frank Dehmelt

ABSTRACT

This application report addresses use-cases where external components demand a higher capacitive loading than the rating of the TPS659038-Q1 and TPS659039-Q1 SMPS-outputs (57-µF maximum per phase). The specification of the device with a rating of nominal 47 µF and maximum of 57 µF holds true. Exceeding these values is at the risk of the user and requires thorough validation in the system. This report is solely intended to provide guidelines on reasonable loading.

Contents

List of Figures

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The TPS65903x-Q1 device has been designed to drive processors such as OMAP5, Jacinto-6, and similar processors. The supply-domains of these processors have decoupling requirements that can be met with the rating of 47 µF typical (57 µF maximum) per phase, two times this value for dual-phase-operation, and three times this value for triple-phase operation.

The demand for higher decoupling capacitance is mainly driven by external components other than the processor, such as an external memory or physical-layer parts (Ethernet-Phys, Serializers, Deserializers, and other components).

With the number of SMPSs offered by the TPS65903x-Q1 device and with the limited power-consumption of the processors, the rails of the TPS65903x-Q1 device can be freed to supply external components in many use-cases. In such cases, it is possible that the decoupling requirements of those external components exceed the rating of the TPS65903x-Q1 device.

This report addresses the circumstances that may allow for a higher capacitive loading.

CAUTION

This application report only provides guidelines. Operating the device outside of the recommended operating conditions is at the customer's own risk.

2 Device Versions

This document applies to any variant of the TPS659038-Q1 and TPS659039-Q1 devices such as orderable part-numbers, O9038A3xxIZWSRQ1 and O9039A3xxIZWSRQ1, where *xx* designates the OTP-revision (one-time programmable memory).

3 Platform Connection Example

Figure 1 shows an example for the detailed connections between a processor and the TPS659039-Q1 device. SMPS7 and SMPS9 are entirely available to drive loads other than the processor, while SMPS3 drives the memory-supply of the processor plus the external memory. SMPS8 shares the power for the processor and external I/Os as well.

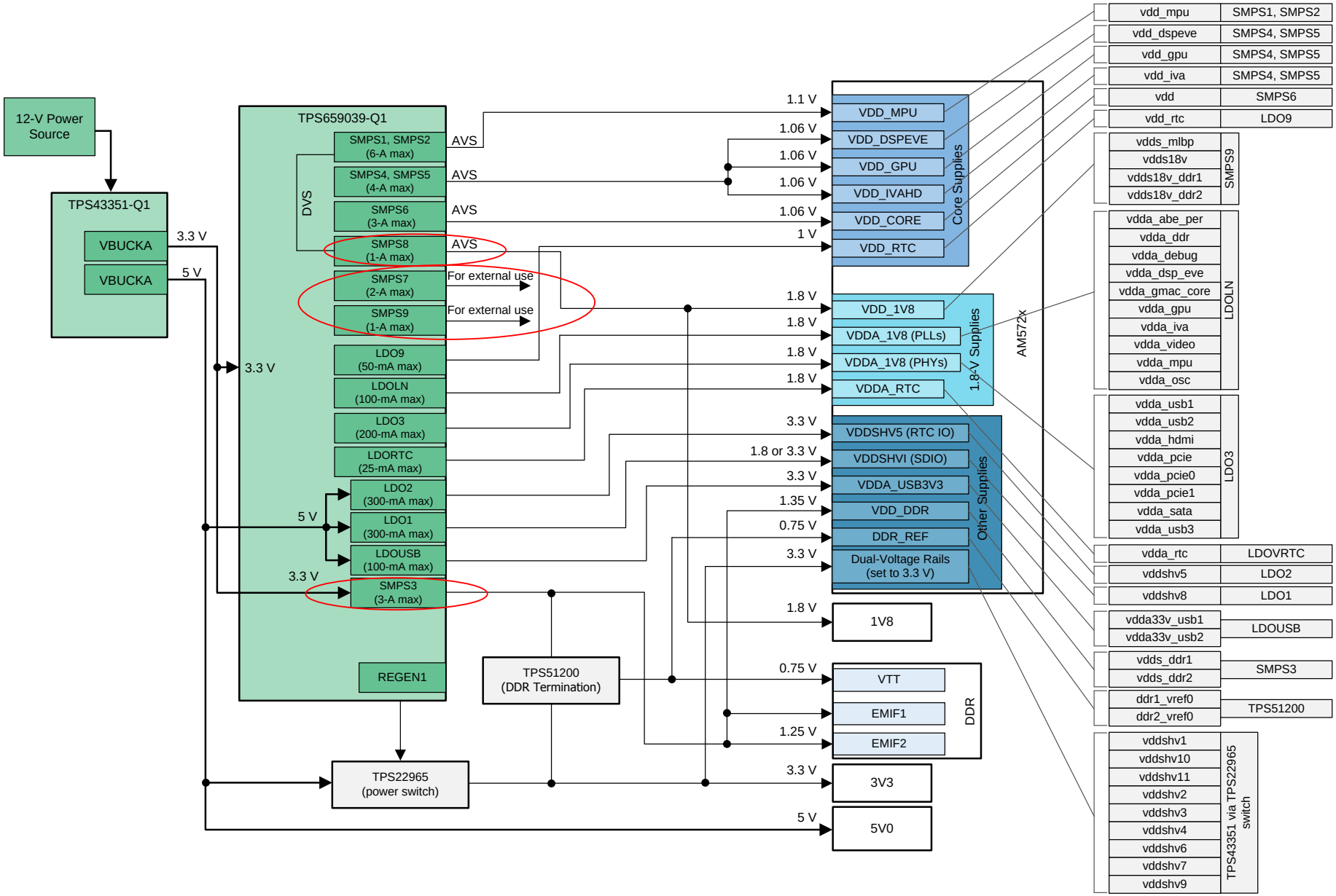

Figure 1. Processor Connection With TPS659039-Q1

4 Specification

The device is rated for an output capacitance of 47 µF typical (57 µF maximum). The following lists several reasons for the limited range:

- Internal compensation and therefore no option to adapt to external components
- Wide range of input voltage, output voltages, switching frequencies, loading, and other parameters
- The capacitance must cover temperature-range, process-variation, aging, and others (to a smaller extent)

A wider range of output capacitance can potentially be supported if some of the previously listed reasons are narrowed down. Because additional parameters, such as the ESR of capacitors and parasitics of the layout, have an effect and load-step response and inrush-current is affected, thorough investigation and validation of the user's design is essential.

5 Approach

A higher output-capacitance is most critical at low output voltages. The device supports output voltages down to 0.7 V, while the majority of applications demand an output voltage of at least 1 V. The external components with high decoupling-capacitance needs require an even higher output voltage (1.8 V, 1.5 V or 1.35 V for DDR-Memory and typically 1.8 V or 3.3 V for I/Os and physical layers).

While various input voltages, temperatures, and load conditions are being used, process variation has little effect on the acceptable range of output capacitance. For the purpose of this application report, the focus is on output voltages of 1 V or higher, across the entire supply-voltage range, temperature range, and load conditions.

Because of the similarities between the various SMPSs, SMPS7 was used as a representative for single-phase rails. SMPS12 was used as representation of the second dual-phase supply, SMPS45. Because the triple-phase operation of SMPS123 already allows for three times the single-phase loading (3 × 47 µH = 141 µH) and, is in all known cases used for a processor domain with limited decoupling needs, SMPS123 was not further evaluated.

Initially, simulations on actual silicon schematics were performed to get an overview of the acceptable capacitance, phase-margins, distribution over process, temperature, inductor-tolerance, and loading with various input and output voltages.

The results confirmed that with an output voltage of 0.7 V, only slight increases in output capacitance are possible. Therefore, no further evaluation with higher loading was tested for this output voltage. The results also determined that at output voltages of 1 V and higher, the potential increase in capacitance was limited. Similarly, the supply voltage had a stronger effect for single-phase. Therefore, a 3.3-V supply versus a 4.2-V supply and 5-V supply was distinguished. Because no significant impact was observed for multiphase, the evaluation was focused on the same capacitive loading (194 µF) for all supply-voltages (3.3 V , 4.2 V, and 5 V) for dual-phase operation.

The evaluation was conducted using gain-phase analysis with combinations of the following parameters:

- Supply voltage (VSYS)
- Output voltage
- Output voltage
- Load capacitance for single-phase (SMPS7) and dual-phase (SMPS12)

With a correlation between simulation and measurements, load-step-analysis was performed with all combinations of the following parameters:

- Supply voltage (VSYS)
- Output voltage
- Load-step: 800 mA to 2 A to 800 mA
- Load capacitance for single-phase (SMPS7) and dual-phase (SMPS12)
- Various temperatures: cold, room-temperature, and hot

6 Test Results

Based on the performed tests, single-phase rails could support up to 90-µF total capacitive loading (COUT of the SMPS plus all decoupling at the point of load) at a 3.3-V supply and a minimum output voltage of 1 V. At a 4-V supply or higher and minimum output voltage of 1 V, up to 130-µF capacitance can be supported. In any case, such a high capacitance would present an operation outside of the specification and thorough testing within the environment of the user is essential.

Notes:

- Load-step-responses showed stable behavior with 130 µF even at a 3.3-V supply, however the phase-margin is reduced. Therefore, TI recommends not to exceed 90 µF with such low supply voltages.
- The additional capacitance was soldered directly onto the output capacitor. This placement results in drops or overshoots on VOUT that potentially exceed the transient response-specification. In an actual design with distributed loads and capacitance, the behavior at the actual load is expected to be better, but demands thorough evaluation by the user in the specific design. Similarly, the additional ESR introduced by traces to the load capacitance change the gain-phase-plot. Therefore using the previously listed values as guidelines only is essential but the system behavior must be adequately validated in the actual design by the user.

Figure 2 shows the frequency band down to 1 Hz, proving no additional poles or zeroes at low frequencies. The following plots focus on the relevant region above 100 Hz.

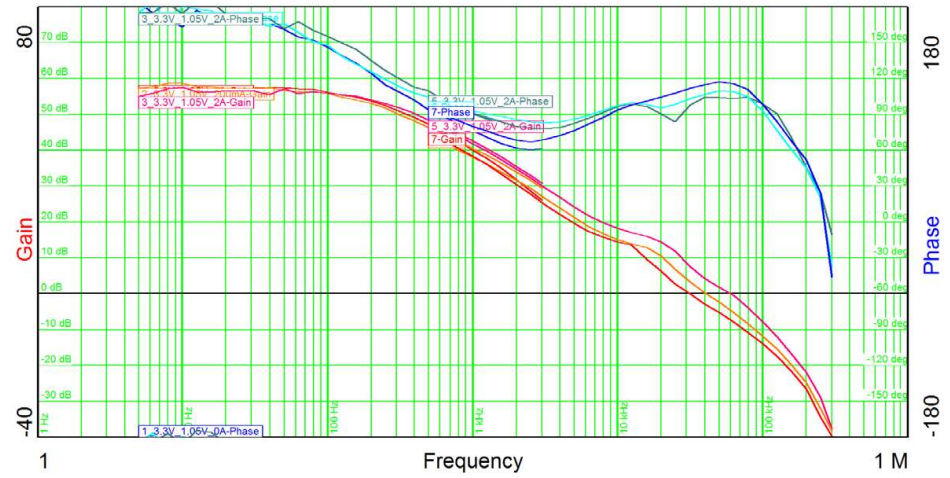

Figure 2. Single-Phase Gain-Phase-Plot With 3.3-V Input, 1.05-V Output, 94 µF

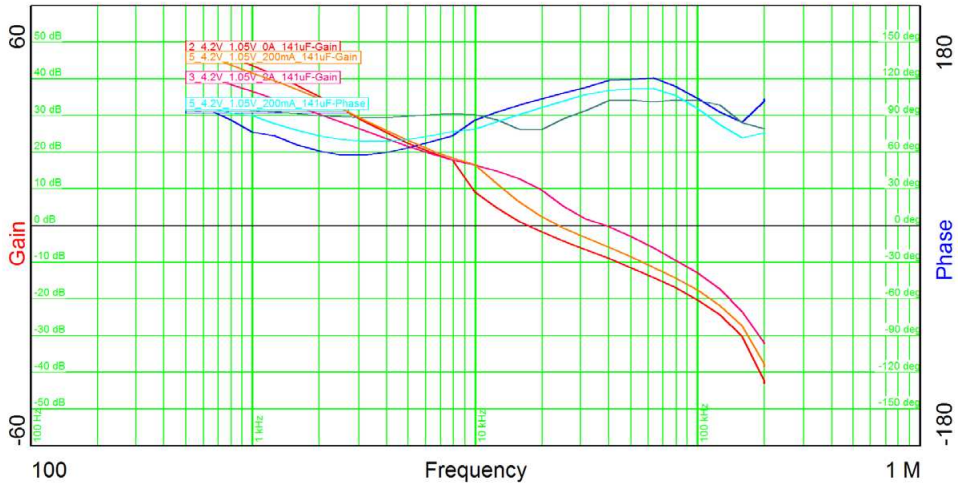

Figure 3. Single-Phase Gain-Phase-Plot With 4.2-V Input, 1.05-V Output, 141 µF

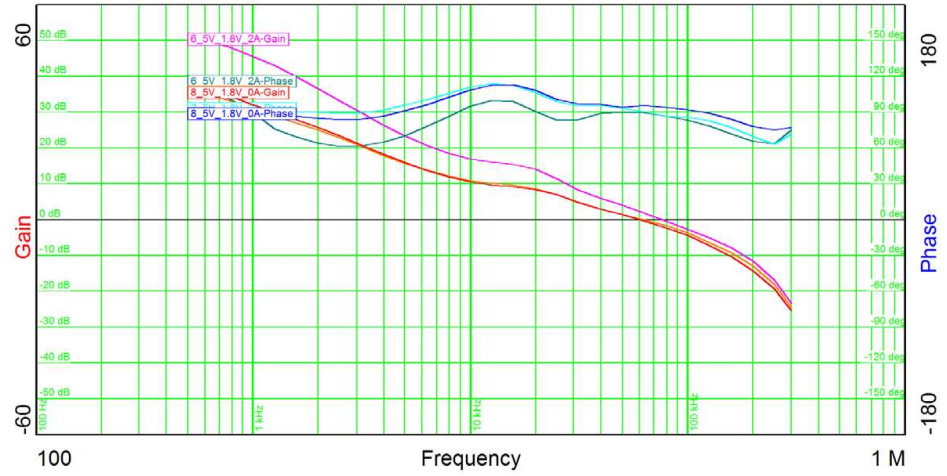

Figure 4. Single-Phase Gain-Phase-Plot With 5-V Input, 1.8-V Output, 94 µF

For dual-phase operation, load-step responses show stability to double the nominal output capacitance and a total capacitive output load of up to 180 µF can be supported for output voltages of 1 V or above.

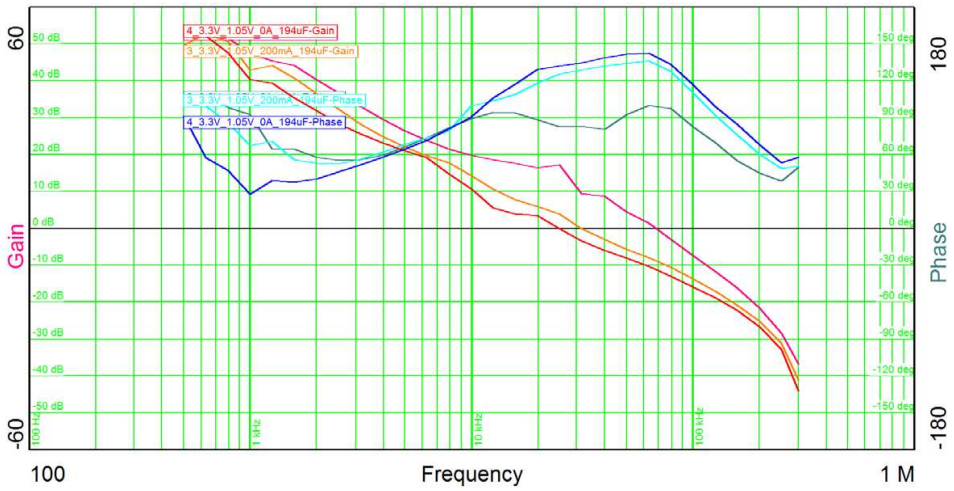

Figure 5. Dual-Phase Gain-Phase-Plot With 3.3-V Input, 1.05-V Output, 194 µF

6.1 Load-Step Response

The various scenarios were proven by the load-step-response tests, which were performed over temperature. The following figures show the previously used example-conditions and were taken at high temperature (hot), which represents the worst case condition. The figures show overshoots and undershoots in the < 30-mV range for load steps of 800 mA to 2 A to 800-mA with very fast transients (approximately 7 A/µs). The magenta curve shows the output current (50 mV/Div over a 100-mΩ shunt resulting in 500 mA/Div). The yellow curve shows the output voltage which is DC-coupled (20 mV/Div). The timescale is 100 ns/Div.

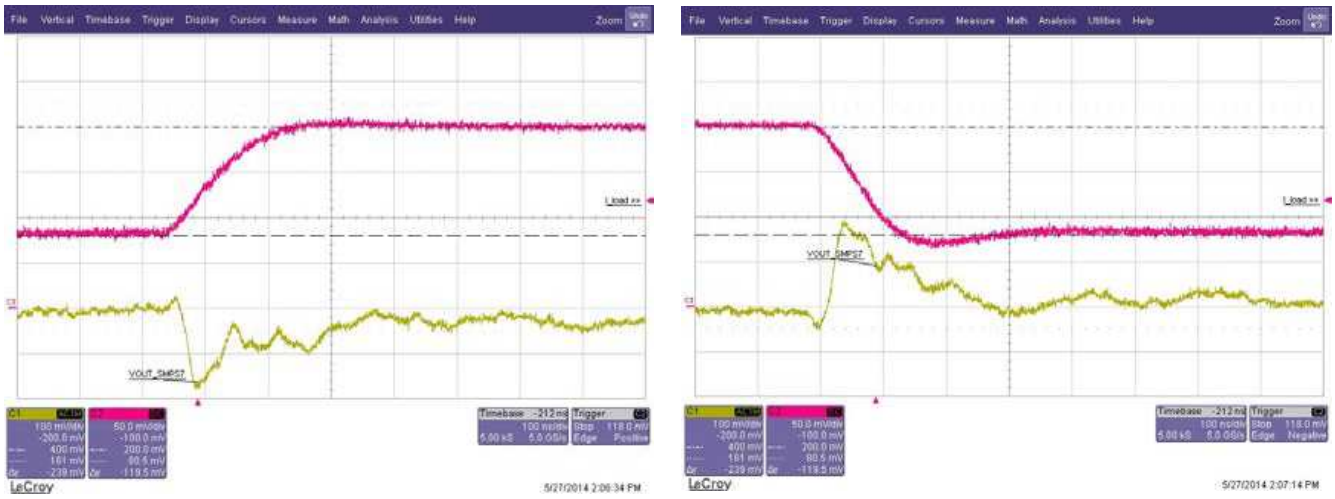

Figure 6. Single-Phase Load-Step Response 3.3-V Input, 1.05-V Output, 94 µF, Hot

Figure 7. Single-Phase Load-Step Response 3.3-V Input, 1.8-V Output, 94 µF, Hot

Figure 8. Single-Phase Load-Step Response 5-V Input, 1.05-V Output, 94 µF, Hot

Figure 9. Single-Phase Load-Step Response 5-V Input, 1.8-V Output, 94 µF, Hot

Figure 10. Single-Phase Load-Step Response 5-V Input, 3.3-V Output, 94 µF, Hot

The multiphase rail shows even less overshoots or undershoots which takes advantage of the multi-phase approach.

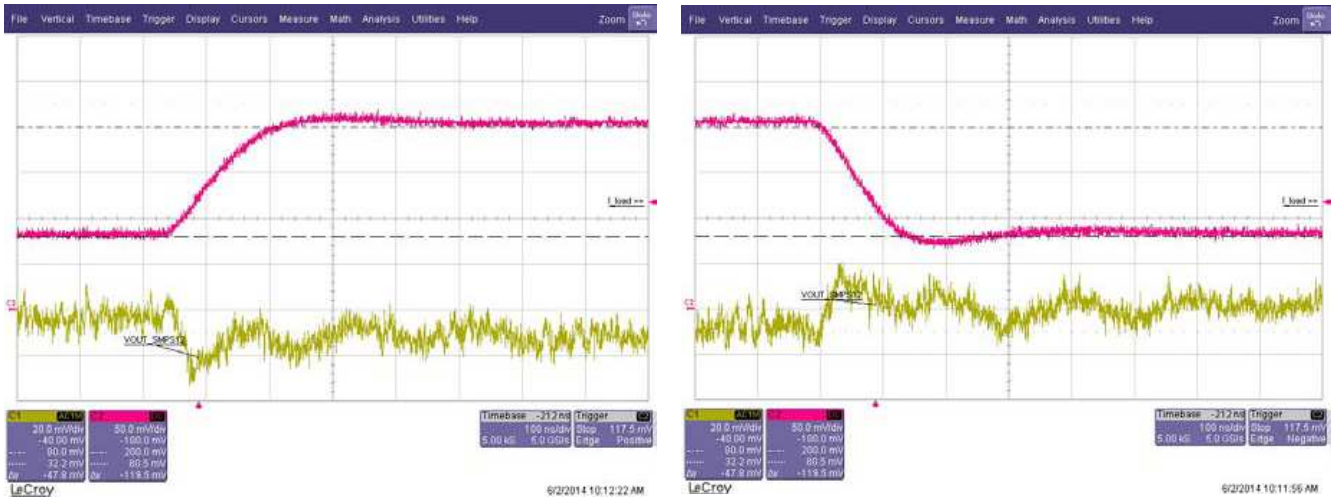

Figure 11. Dual-Phase Load-Step Response 3.3-V Input, 1.05-V Output, 194 µF, Hot

Figure 12. Dual-Phase Load-Step Response 3.3-V Input, 1.8-V Output, 194 µF, Hot

Figure 13. Dual-Phase Load-Step Response 5-V Input, 1.05-V Output, 194 µF, Hot

Figure 14. Dual-Phase Load-Step Response 5-V Input, 1.8-V Output, 194 µF, Hot

Figure 15. Dual-Phase Load-Step Response 5-V Input, 3.3-V Output, 194 µF, Hot

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2014) to A Revision	Page
• First public release of document	2

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265