CC27xx SimpleLink™ Wireless MCU

Technical Reference Manual

Literature Number: SWCU195
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About This Manual

This document is organized into sections that correspond to each major feature; it explains the features and functionality of each module, and it also explains how to use them. For each feature, references are given to the documentation for the driver of the corresponding operating systems. This document does not contain performance characteristics of the device or modules, which are gathered in the corresponding device data sheets. This manual is intended for system software developers, hardware designers, and application developers.

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Devices

The CC27xx device platform features different memory sizes, peripherals, and package options. All devices are centered around an Arm® Cortex®-M33 series processor that handles the application layer and protocol stack.

Register, Field, and Bit Calls

The naming convention applied for a call consists of:

- For a register call: *<Module name>.<Register name>*; for example: UART.UASR
- For a bit field call:
  - *<Module name>.<Register name>[End:Start] <Field name> field*; for example, UART.UASR[4:0] SPEED bit field
  - *<Field name> field <Module name>.<Register name>[End:Start]*; for example, SPEED bit field UART.UASR[4:0]
- For a bit call:
  - *<Module name>.<Register name>[pos] <Bit name> bit*; for example, UART.UASR[5] BIT_BY_CHAR bit
  - *<Bit name> bit <Module name>.<Register name>[pos]*; for example, BIT_BY_CHAR bit UART.UASR[5]

Related Documentation

The following related documents are available on the CC27xx device product pages at www.ti.com:

1. CC2745R10-Q1:
   - CC2745R10-Q1 data sheet and errata (Technical Documents)

Note

This list of documents was current as of publication date. Check the website for additional documentation, application notes, and white papers.

Additional, related documentation follows:

1. The Institute of Electrical and Electronic Engineers, Inc., *IEEE Standard Test Access Port and Boundary Scan Architecture, IEEE Std 1149.1a 1993 and Supplement Std. 1149.1b 1994* (see IEEExplore.ieee.org)
2. The Institute of Electrical and Electronic Engineers, Inc., *IEEE 1149.7 Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture* (see IEEExplore.ieee.org)
3. National Institute of Standards and Technology, *NIST Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation Methods and Techniques* (see NIST.gov)
4. National Institute of Standards and Technology, *NIST Special Publication 800-38D, Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC* (see NIST.gov)
5. National Institute of Standards and Technology, *FIPS 197, Advanced Encryption Standard (AES)* (see NIST.gov)
6. Bluetooth SIG, Inc., *Bluetooth* Specification versions 4.0, 4.1, 4.2, and 5.3 (see Bluetooth.com)
7. Cortex-M33 Devices Generic User Guide (see documentation at Arm.com)
8. Cortex-M33 Technical Reference Manual (see documentation at Arm.com)
9. *Arm®v6-M Architecture Reference Manual* (see documentation at Arm.com)
10. *Arm® Debug Interface V5 Architecture Specification* (see documentation at Arm.com)

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Chapter 1

Architectural Overview

The CC27xx SimpleLink™ low-power wireless and high-performance MCUs provide solutions for a wide range of applications. To help the user develop these applications, this user's guide focuses on the use of the different building blocks of the devices. For detailed device descriptions, complete feature lists, and electrical specifications, see the data sheet for the specific device. The following subsections provide easy access to relevant information and guide the reader to the different chapters in this document.

The CC27xx SimpleLink low-power and high-performance MCUs are optimized for low power, while providing fast and capable MCU systems to enable short processing times and high integration. The combination of an Arm® Cortex®-M33 processing core at 96MHz, flash memory, and a wide selection of peripherals makes the CC27xx specifically designed for single-chip implementation or network processor implementations of lower-power RF nodes. A hardware security module and implementation of TrustZone™ enables hardening of the device against security challenges.

1.1 Target Applications

The device is positioned for low-power wireless applications, such as:

- Automotive
  - Car access and security systems
    - Passive entry passive start (PEPS)
    - Phone as a key (Paak)
    - Remote keyless entry (RKE)
  - Advanced driver assistance systems (ADAS)
- Home and building automation
- Consumer electronics
- Mobile phone accessories
- Sports and fitness equipment
- HID applications
- Grid infrastructure
  - Solar inverter
  - E-meter
- Lighting control
- Alarm and security
- Electronic shelf labeling
- Proximity tags
- Medical electronics
  - Glucose monitor
  - Heart rate sensor
- Remote controls
- Smart metering
- Asset tracking
- Wireless sensor networks

1.2 Introduction

The block diagram shows the building blocks of the CC27xx platform. The following sections provide an overview of the features of the CC27xx.

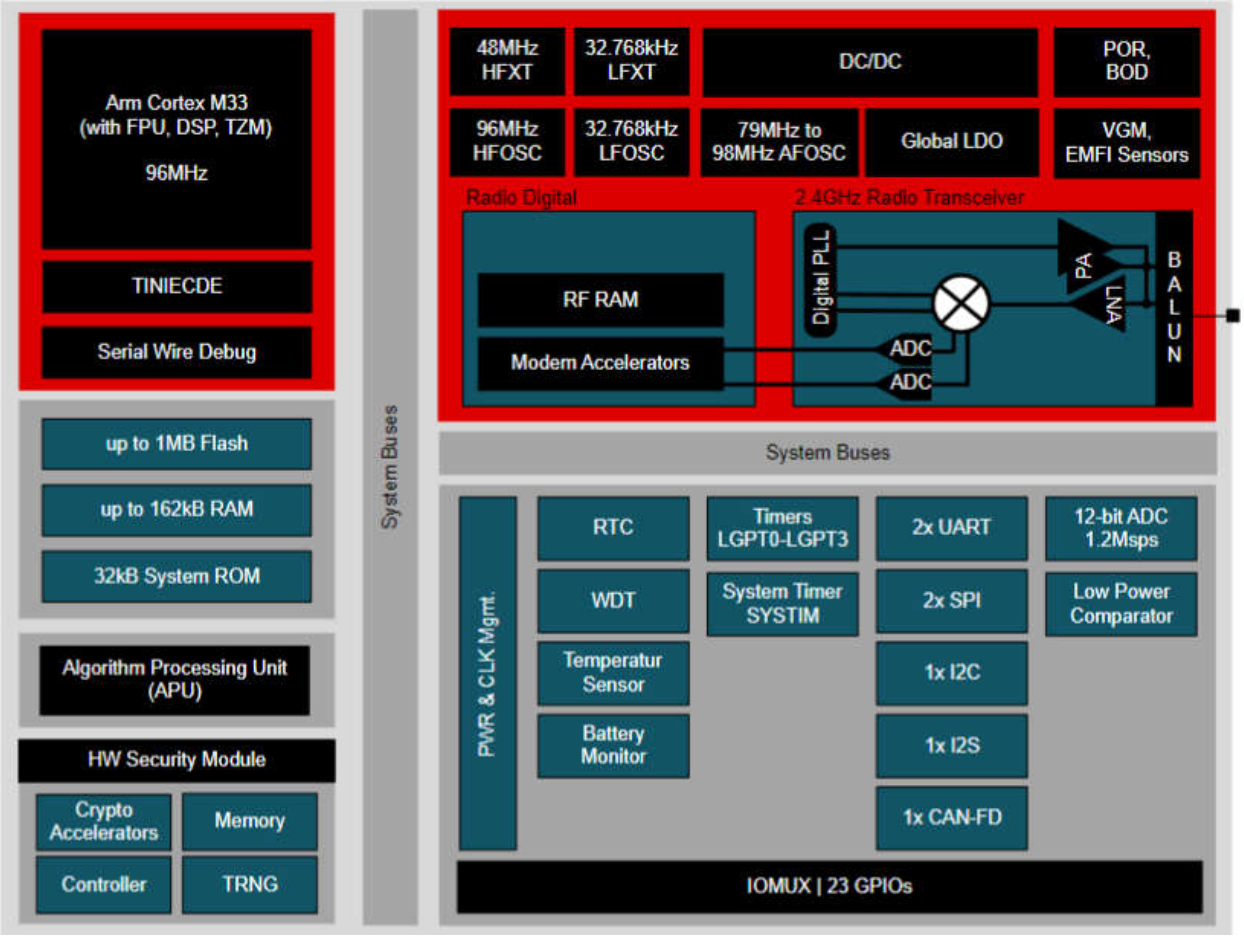

Figure 1-1. CC27xx Block Diagram

CC27xx devices have the following features:

- Arm® Cortex® M33 processor core
  - Arm® Cortex® SysTick timer
  - Nested Vectored Interrupt Controller (NVIC)
  - TrustZone ™
  - AI instruction extensions (TINIECDE)
- Clocks
  - 96MHz RC oscillator and 48MHz crystal oscillator with internal doubler to 96MHz
  - 32kHz crystal oscillator and 32kHz RC oscillator
  - 79MHz to 98MHz tunable RC oscillator for audio and CAN-FD applications
- On-chip memory
  - Up to 1MB of in-system programmable flash
  - Up to 162KB of ultra-low leakage SRAM, optionally with parity (up to 144KB) Retained in standby mode.
- Power Management
  - Wide supply voltage range
  - Efficient on-chip DC/DC converter for reduced power consumption
  - Flexible low-power modes allowing low energy consumption in duty-cycled applications

- Advanced Serial Integration
  - Universal asynchronous receiver-transmitter (UART)
  - Inter-Integrated Circuit (I^2C)
  - Serial peripheral interface (SPI)
  - CAN-FD
  - Inter-Integrated Circuit Sound (I^2S)
- System Integration
  - Direct memory access controller (µDMA)
  - Up to four general-purpose timers capable of pulse width modulation (PWM), synchronization, capture, counting, and quadrature decoding
  - 32kHz real-time clock (RTC)
  - Watchdog timer
  - System Timer (SYSTIM) with the same time base as RTC but down to 250ns resolution
  - Battery Monitor: On-chip temperature and supply voltage sensing
  - GPIO with normal or high-drive capabilities
  - GPIO with analog capability for ADC and comparator
  - GPIO split rail support
  - Configurable pin multiplexing
  - Low power comparator
  - 12bit ADC, 1.2Mbps with external reference, 260kbps with internal reference, up to 8 external ADC inputs
  - 1× Algorithm Processing Unit (APU) for applications such as Bluetooth channel sounding post-processing or ML feature extraction or digital signal processing like FFT, and so on
  - Hardware Security Module (HSM) with proprietary controller and dedicated memories supporting accelerated cryptographic operations and secure key storage:
    - AES 128- or 256-bit crypto accelerator
    - ECC (up to 521 bits), RSA (up to 3072 bits) public key accelerator
    - SHA-2 (up to 512 bits) accelerator
    - True random number generator
    - HSM firmware update support
    - DPA (Differential Power Analysis) countermeasures (AES, ECDSA)
    - Separate AES 128-bit crypto accelerator (LAES) for latency critical link-layer crypto operations
    - Secure boot and secure firmware updates
    - Cortex®-M33 TrustZone-M™, MPU, memory firewalls for software isolation
    - Voltage glitch monitor (VGM), Electromagnetic fault injection (EMFI) sensors
    - ISO21434 Automotive Cybersecurity Compliant
    - Global Platform SESIP (Security Evaluation Standard for IoT Platforms) Level 3 and Arm® PSA (Platform Security Architecture) Level 3 Certification
- Arm® SWD debug interface
- Instrumentation Trace Macrocell (ITM) and Data Trace and Watchpoint Unit (DWT) support
- 2.4GHz RF transceiver compatible with Bluetooth® 5.4 Low Energy and IEEE 802.15.4 PHY and MAC
- Integrated Balun
- Output power up to +20dBm with temperature compensation and integrated RF switch
- Wireless protocol support:
  - Bluetooth® 5.4 Low Energy
  - Ready for upcoming Bluetooth® Channel Sounding (High Accuracy Distance Measurement)
  - Thread, Zigbee®, Matter
  - Proprietary systems
- For packaging options see the device-specific data sheet

For applications requiring extreme conservation of power, the CC27xx device features a power-management system to efficiently power down the device to a low-power state during extended periods of inactivity. A power-up and power-down sequencer, a 32-bit sleep timer (an RTC) with interrupt capabilities, and ultra-low-leakage

(ULL) RAM with retention in all power modes (except device shutdown mode) positions the MCU for battery applications. The CC27xx device platform offers the advantages of the widely available development tools of Arm® , SoC infrastructure IP applications, and a large user community. Additionally, the microcontroller uses Arm® Thumb®-compatible Thumb-2 instruction set to reduce memory requirements.

TI offers a complete support package to assist in getting to market quickly, with evaluation and development boards, white papers and application notes, an easy-to-use peripheral driver library, a Software Development Kit (SDK) with qualified wireless protocols, and a strong support, sales, and distributor network.

1.3 Arm® Cortex® M33

The following subsections provide an overview of the Arm® Cortex® M33 , the integrated system timer (SysTick), and the NVIC.

1.3.1 Processor Core

The CC27xx device is designed around an Arm® Cortex® M33 processor core.

Features of the processor core are as follows:

- Arm®v8-M architecture with mainline extension
- Thumb/Thumb-2 subset instruction support
- 3-stage pipeline
- Software security:
  - TrustZone™ for Arm®v8-M, with a Security Attribution Unit of up to eight regions
  - Stack limit boundaries and checking
- DSP extension: including all the V8.1-M DSP/SIMD instructions.
- Floating Point Unit (FPU): single precision floating point unit, IEEE 754 compliant
- Memory Protection Unit (MPU) with eight regions for the secure state (MPU_S) and eight regions for the non-secure state (MPU_NS)
- Eight regions of Security Attribute Unit (SAU)
- 24-bit SysTick timer for each security domain
- Integrated Nested Vectored Interrupt Controller (NVIC) supporting Non-Maskable Interrupt (NMI)
- Low-power sleep modes
  - Arm® SLEEP maps to the device's idle power mode.
  - Arm® DEEPSLEEP maps to the device's standby power mode.
- Serial Wire Debug ports with up to eight breakpoints and four watchpoints
- Data Watchpoint and Trace Unit (DWT) and Instrumentation Trace Macrocell (ITM)
- CDE instruction extensions for Neural Network processing

1.3.2 SysTick Timer

The Arm® Cortex® M33 processor includes an integrated Sytick Timer. SysTick provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter
- A simple counter used to measure time to completion and time used
- An internal clock-source control based on missing or meeting durations

1.3.3 Nested Vectored Interrupt Controller

The CC27xx device controller includes the Arm® NVIC. The NVIC and Arm® Cortex® M33 prioritize and handle all exceptions in handler mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the interrupt service routine (ISR). The processor supports tail-chaining, that is, back-to-back interrupts can be performed without the overhead of state saving and restoration. Software can set priority/preemption grouping in eight levels on internal CPU exceptions and interrupts.

Features of the NVIC include:

- Deterministic, fast interrupt processing
- External non-maskable interrupt (NMI) signal available for immediate execution of NMI handler
- Dynamically reprioritizable interrupts
- Exceptional interrupt handling through hardware implementation of required register manipulations
- TrustZone ™ security attribution

1.3.4 System Control Block (SCB)

The system control block (SCB) provides system implementation information and system control (configuration, control, and reporting of system exceptions).

1.3.5 TI Machine Learning Instruction Extensions

The M33 core has extended neural net instructions to support TINIE. There are implemented Custom Datapath Extensions (CDE) in the Cortex-M33 to accelerate machine learning algorithms to support TI (New Product Update) NPU-APIs. Please see Section 2.4.4 for more information on TI-specific CDE implementations.

1.4 On-Chip Memory

The following subsections describe the on-chip memory modules.

1.4.1 SRAM

The CC27xx devices have up to 162KB of low-leakage, on-chip SRAM with retention in all power modes except Shutdown. Data can be transferred to and from the SRAM using the micro DMA (µDMA) controller. The ultra-low leakage system static RAM (SRAM) can be used for both the storage of data and execution of code. System SRAM is always initialized to zeroes upon code execution during boot. The memory can be configured to use parity for soft error mitigation, in which case up to 144KB SRAM can be used.

1.4.2 FLASH

The flash block provides an in-circuit programmable, nonvolatile program memory for the device. Up to 1MB of flash memory is organized as a set of 2KB sectors that can be individually erased. Erasing a sector causes the entire contents of the sector to be reset to all 1s. These sectors can be read-only protected. Write/erase protected sectors cannot be erased or programmed, protecting the contents of those sectors from being modified. In addition to holding program code and constants, the nonvolatile memory allows the application to save data that must be preserved so that the data is available after restarting the device. Using this feature lets the user use saved network-specific data and avoids the need for a full start-up and network find-and-join process.

The HSM will reserve a section of flash memory (64-128KB)

The flash memory is organized in two banks of 512KB each. The device supports continued reading/executing from one bank while a write or erase operation is underway in the other.

1.4.3 ROM

The ROM is preprogrammed with a boot sequence, hardware APIs (HAPI), and a serial bootloader (SPI or UART).

1.5 Power Supply System

There are multiple voltage levels in use on the CC27xx to effectively optimize the power consumption of various modules operating in different power modes. Figure 1-2 shows an overview of the supply system.

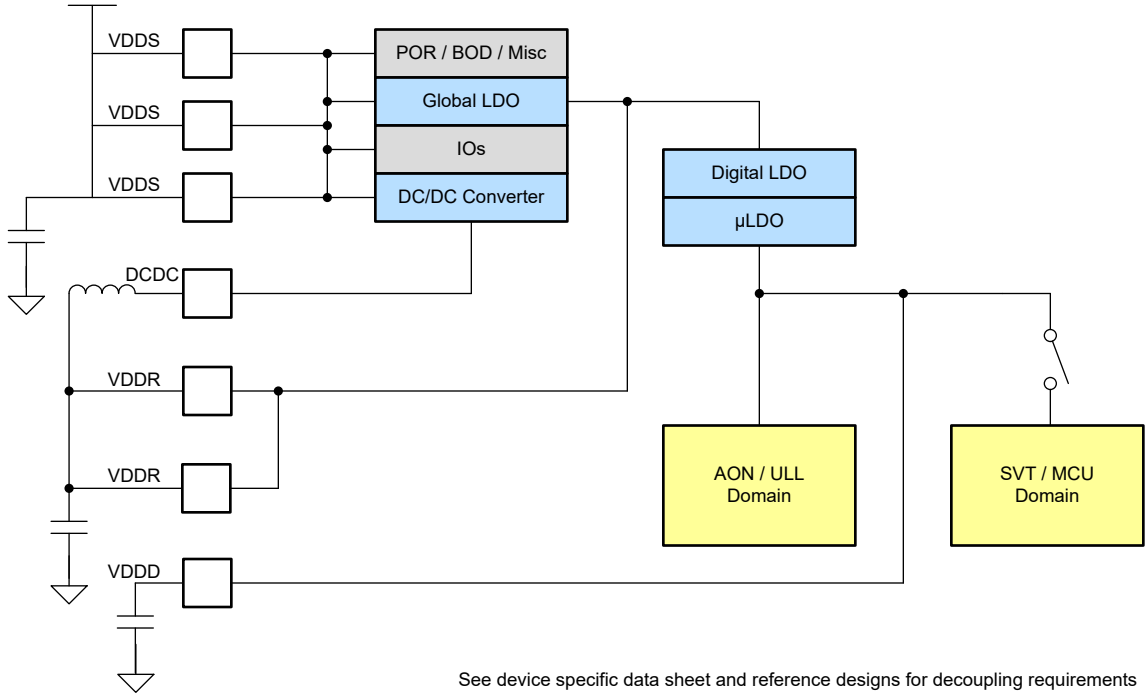

Figure 1-2. Supply System

1.5.1 VDDS

The battery voltage on the CC27xx device is called VDDS (supply).

Note

All VDDS pins must be at the same voltage level.

1.5.2 VDDIO

This VDDIO supply powers the split rail IO supply for some GPIOs.

VDDIO split rail I/O supply enables using a different I/O supply rail compared to the main VDDS supply rail. This enables applications to interface with other system components at a different voltage level compared to the main VDDS power supply level. GPIOs supplied by VDDIO and VDDS supplies are listed in orange or blue respectively in ***Figure 6.1 RHA Pinout*** in the data sheet. The voltage rails supplied on VDDS and VDDIO pins can ramp up and down in any order, independent of each other, and any combination of VDDS and VDDIO supplies being unpowered can be supported indefinitely. This simplifies the system-level power supply design, where it is not needed to control the availability or ramp up or down the sequence of these supplies at the VDDIO and VDDS pins.

1.5.3 VDDR

The two VDDR (regulated) pins are normally powered by one of the internal regulators. VDDR operates at 1.5V. For the lowest power, TI recommends using the internal DC/DC regulator. Using the Global LDO is also an option. See Section 6.3.1 for further details on this configuration.

Note

The VDDR pins cannot be used to supply external circuitry.

1.5.4 VDDD Digital Core Supply

The digital core of the CC27xx device is supplied by a 1.32V regulator connected to VDDR. The output of this regulator requires an external decoupling capacitor for proper operation. this capacitor must be connected to the VDDD pin.

Note

The VDDD pin cannot be used to supply external circuitry.

When the device is in standby, a small low-power regulator (µLDO) with limited current capacity supplies the digital domain to ensure enabled modules still have power.

1.5.5 DC/DC Converter

The on-chip buck-mode DC/DC converter provides a simple way to reduce the power consumption of the device. The DC/DC converter is integrated into the supply system and handles bias and clocks automatically through the system controller. The DC/DC converter is controlled through the PMCTL.VDDRCTL register. To enable the DC/DC converter when the system is active, the PMCTL.VDDRCTL[0] SELECT bit must be set. The DC/DC converter is also used periodically when the device is in Standby mode to maintain voltage on the VDDR domain. The output voltage of the DC/DC regulator is trimmed to 1.5V. The voltage level is controlled automatically by the device and cannot be changed by the user.

Note

The DC/DC regulator output cannot be used to supply external circuitry.

1.6 Radio

The CC27xx device provides a highly integrated low-power 2.4GHz radio transceiver with support for multiple modulations and packet formats. The radio subsystem provides an interface between the MCU and the radio transceiver, which makes it possible to issue commands, read status, and automate and sequence radio events. The RF path incorporates a balun to reduce system component count and simplify the design process.

1.7 Hardware Security Module

The CC27xx devices have an integrated hardware security module (HSM) supporting an isolated environment for cryptographic operations, key management, secure counters, and random number generation operations. AES and SHA-2 algorithms are protected from differential power analysis (DPA) side-channel attacks.

The HSM also contains a FIPS-compliant True Random Number Generator (TRNG) and nonvolatile monotonic counters. The HSM also supports HSM firmware validation by HSM ROM and secure HSM firmware updates.

1.8 AES 128-Bit Cryptographic Accelerator

The CC27xx devices also integrate an AES-128 cryptography hardware accelerator (separate from the HSM), to support latency critical link-layer encryption/decryption operations prescribed by the wireless protocols. This AES accelerator can get keys commissioned from the HSM or be used fully independently of the HSM. The AES hardware accelerator supports the following block cipher modes and message authentication codes:

- AES ECB encrypt
- AES CBC encrypt
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)
- Software implementation of AES GCM cipher mode using LAES for low-level cryptographic operations is supported.

1.9 System Timer (SYSTIM)

The SYSTIM is a 34-bit, 6-channel wrap-around timer with a per-channel selectable 32b slice with either a 1µs resolution and 1h11m35s range or 250ns resolution and 17m 54s range. All channels support both capture and

single-shot compare (posting an event) operation. One channel is reserved for system software, three channels are reserved for radio software and two channels are freely available to user applications.

For software convenience, there is a hardware synchronization mechanism that automatically ensures that the RTC and SYSTIM share a common time base (albeit with different resolutions/spans). For software convenience, a hardware synchronization mechanism automatically ensures that the RTC and SYSTIM share a common time base. Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel immediately triggers if the submitted event is in the immediate past (4.294s with 1µs resolution and 1.049s with 250ns resolution).

1.10 General Purpose Timers (LGPT)

General-purpose timers can be used to count or time external events that drive the timer-input pins.

The general-purpose timer module (LGPT) contains up to four LGPT blocks with the following functional options. To determine which timers support which functions see the device specific data sheet:

- 16-bit or 32-bit bit counter width
- Three Capture/Compare channels per timer
- One-shot or periodic counting
- Time counting between edges and edge counting
- Input filter on each of the channels for all timers
- 15 different channel Capture/Compare actions
- PWM Generation with programmable dead-band insertion and park on fault mode
- IR Signal generation
- Quadrature decoding (QDEC)
- Timer synchronization and chaining
- Efficient transfers using the µDMA controller

1.11 Always-ON (AON) or Ultra-Low Leakage (ULL) Domain

The AON/ULL domain contains circuitry that is always enabled, except for in the shutdown power state (where the digital supply is off). For more information on power states, see Chapter 6.

This domain includes the following:

1.11.1 Watchdog Timer

The watchdog timer is used to regain control when the system fails because of a software error or when an external device fails to respond properly. The watchdog timer can generate a reset when a predefined time-out value is reached.

The watchdog timer runs on a 32kHz clock rate and operates in device active, idle, and standby modes and cannot be stopped once enabled.

1.11.2 Battery and Temperature Monitor

A battery voltage monitor is available in the CC27xx device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when supply voltage or temperature go beyond defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (ULL/AON) event fabric.

1.11.3 Voltage Glitch Monitor (VGM)

A Voltage Glitch Monitor is present in the system to trigger a system reset if very fast voltage changes on the digital voltage supply occur as such changes can cause localized corruption of digital state.

The CC27xx devices supports the VGM on-chip to mitigate security risks from low-cost and low-effort physical non-invasive fault attacks. The VGM is enabled by default during device boot time operation and can be configured to be operational during application runtime operations based on application security needs.

1.11.4 Real-time Clock (RTC)

The RTC can be used to wake the CC27xx device from any state where the RTC is active. The RTC contains one capture and one compare channel. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32 kHz RC oscillator or the 32 kHz crystal oscillator. The RTC has a recovery mechanism to keep the clock through software initiated resets.

1.11.5 Low Power Comparator

The low power comparator is an ultra low-power clocked (on CLKLF) comparator that can be used for medium accuracy, low speed operations where power consumption is the main concern. Typical applications are wake-up on analog events like power supply monitoring or external transducers that generate analog output signals. The comparator includes input multiplexers on both signal (positive) side and reference (negative) side, a capacitive divider for low-power division of either the reference signal or the input signal, and programmable hysteresis that can be configured to trigger on both low and high comparator output. The low power comparator is also active in Standby mode.

1.12 Direct Memory Access

The CC27xx device includes a DMA controller, known as µDMA. The µDMA controller provides a way to offload data transfer tasks from the Arm Cortex M33 processor, allowing more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfers between memory-and-memory or between memory-and-peripherals. Channels in the µDMA are multiplexed between each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

1.13 System Control and Clock

System control determines the overall operation of the CC27xx device. System control provides information about the devices, controls power-saving features, controls the clocking of the devices and individual peripherals, and handles reset detection and reporting.

- Power Control:
  - On-chip fixed DC/DC converter and Global low drop-out (GLDO) voltage regulators
  - Handles the power-up sequencing, power-down sequencing, and control for the core digital-logic and analog circuits
  - Low-power options for on-chip modules:
    - Software controls shutdown of individual peripherals and memory
    - SRAM is retained in all power modes except shutdown
  - Configurable wake up from standby by RTC or any IOC interrupt
  - Voltage supervision circuitry
- Multiple clock sources for microcontroller system clock:
  - High Frequency Clock:
    - Clock doubler: Provides 96 MHz clcok to core digital functions
    - RC oscillator (HFOSC): on-chip 48 MHz RC oscillator.
    - External oscillator (HFXT): external 48MHz crystal oscillator connected across the X48P input and X48N output pins.
    - Radio operation requires the external oscillator.
    - Auxiliary Frequency Oscillator (AFOSC): The 80/90.3168/98.304MHz AFOSC is used as the high-frequency clock for generating needed frequencies to support for CAN-FD and audio I2S operations. The AFOSC tracks the HFOSC which in turn, tracks its accuracy against the external 48MHz crystal (HFXT). AFOSC can generate 79, 80, 86, 90.3168, and 98.304MHz clock frequencies with a 10ppb tracking accuracy from HFOSC.
  - Low Frequency Clock:
    - RC oscillator (LFOSC): on-chip 32kHz RC oscillator.

- External oscillator (LFXT): external 32.768kHz crystal oscillator connected across the X32P input and X32N output pins.
- Designed for accurate RTC operation or synchronous network timing.
- Used during power-saving modes and for RTC.

1.14 Communication Peripherals

The CC27xx device platform supports both asynchronous and synchronous serial communication including:

- UART module
- I^2C module
- SPI module
- CAN-FD module
- I^2S module

The following subsections provide more detail on each of the communication modules.

1.14.1 UART

A UART is an integrated circuit used for TTL serial communications. A UART contains a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter).

The CC27xx device includes a fully programmable UART. The UART can generate individually masked interrupts from the receive (RX), transmit (TX), modem flow control, and error conditions. The module generates one combined interrupt when any of the interrupts are asserted and are unmasked.

The UART has the following features:

- Programmable baud rate generator allowing speeds up to 3Mbps
- Separate 8 × 8 transmit (TX) and 8 × 12 receive (RX) first-in first-out (FIFO) buffers to reduce CPU interrupt service loading
- RX/TX FIFOs can be reconfigured to a 16x8b TX FIFO for unidirectional output
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of ¼, ½, ¾
- Line-break generation and detection
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity bit generation and detection
  - 1 or 2 stop-bit generation
- FIFO, RX FIFO RX time-out, modem status, and error conditions
- Standard FIFO-level and end-of- transmission interrupts.
- Efficient transfers using micro direct memory access controller (µDMA):
- Separate µDMA channels for transmit and receive.
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level.
  - Transmit single request is asserted when there is space in the FIFO; burst request is asserted at programmed FIFO level.
- Programmable hardware flow control
- Support for standard Infrared Data Association (IrDA) and low power IrDA protocols
- Provision to combine both TX and RX FIFOs in transmit mode

1.14.2 I^2C

The I^2C bus provides bidirectional data transfer through a 2-wire design (a serial data line SDA and a serial clock line SCL). The I^2C bus interfaces to external I^2C devices such as serial memory (RAM and ROM), networking devices, LCDs, tone generators, and so on. The I^2C bus can also be used for system testing and diagnostic purposes in product development and manufacturing.

The CC27xx device includes an I^2C module with the following features:

- Devices on the I^2C bus can be designated as either a controller or target:
  - Supports both transmitting and receiving data as either a controller or a target
  - Supports simultaneous controller and target operation
- Four I^2C modes:
  - Controller transmit
  - Controller receive
  - Target transmit
  - Target receive
- Two transmission speeds:
  - Standard (100 kbps)
  - Fast (400 kbps)
- Controller and target interrupt generation:
  - Controller generates interrupts when a TX or RX operation completes (or aborts due to an error)
  - Target generates interrupts when data is transferred or requested by a controller or when a START or STOP condition is detected
  - Controller with arbitration and clock synchronization, multi-controller support, and 7-bit addressing mode

1.14.3 SPI

The SPI module is a 3-wire or 4-wire bidirectional communication interface that converts data between parallel and serial formats. The SPI performs serial-to-parallel conversion on data received from a target device and performs parallel-to-serial conversion on data transmitted to a target device. The SPI can be configured as either a controller or peripheral device. As a peripheral device, the SPI can be configured to disable the SPI output, which allows coupling of a controller device with multiple peripheral devices. The TX and RX paths are buffered with separate internal FIFOs.

The SPI also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the input clock of the SPI. Bit rates are generated based on the input clock, see the device specific data sheet for maximum bit rates.

The SPI module supports the following features:

- Programmable interface operation for Motorola SPI (3-wire and 4-wire), MICROWIRE, or TI Synchronous Serial format
- Configurable as a controller or a peripheral on the interface
- Programmable clock bit rate and prescaler
- CRC8-CCITT or CRC16-CCITT CRC capability and auto insertion in TX upon underflow
- Separate transmit (TX) and receive (RX) first-in first-out buffers (FIFOs)
  - If Data Size Select (DSS) is 4 to 8 bits FIFOs are 16 locations deep and 8 bits wide
  - If Data Size Select (DSS) is 9 to 16 bits FIFOS are 8 locations deep and 16 bits wide
- Programmable data frame size from 4 bits to 16 bits (controller mode) or 7 to 16 bits (peripheral mode)
- Internal loop-back test mode for diagnostic and debug testing
- Interrupts for transmit and receive FIFOs, overrun and time-out interrupts, and DMA done interrupts
- Efficient transfers using micro direct memory access controller (µDMA):
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains a configurable number of entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when FIFO contains a configurable number of entries

1.14.4 CAN-FD

The Controller Area Network Flexible Data-Rate (CAN-FD) module supports both CAN, CAN 2.0 and CAN-FD protocols

- Conforms w/ CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)

- AUTOSAR and J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt, two interrupt lines
- ECC check for Message RAM
- Power-down and wakeup support
- Timestamp Counter

1.14.5 I^2S

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation (PDM) microphones. An I^2S module enables the CC27xx device to communicate with external devices like codecs, DAC, ADCs, or DSPs. The devices only support audio streaming formats like I^2S, RJF, LJF, and DSP; the devices do not support configuration of external devices. The CC27xx device platform supports both external and internally generated bit clock and word clock (BCLK and WCLK).

1.15 Programmable I/Os

I/O pins offer flexibility for a variety of connections. The CC27xx device supports configurable I/O pins that can be multiplexed to digital and analog peripherals through the I/O Controller. For information on what pins can be multiplexed to what peripherals see the device specific data sheet.

- Up to 23 GPIO (6x6 package)
- Up to 6 high drive strength pins, drive strength is configurable for high drive I/Os. Drive strength be set to AUTO where I/Os automatically use the drive strength required to support a 12 MHz toggle rate based on measured VDDS voltage
- Up to 8 analog capable IOs
- Support for split rail application, some IOs are driven by VDDS and some by VDDIO
- Programmable control for GPIO interrupts:
  - Interrupt generation masking per pin
  - Edge-triggered on rising or falling edges
- Can initiate a µDMA transfer
- Pin state can be retained during all sleep modes
- Wake-up from IOC supported on all pins in all power modes
- Pins configured as digital inputs are Schmitt-triggered
- Programmable control for DIO configuration:
  - Weak pull-up or pull-down resistors
  - Digital input buffer enable controls

1.16 Algorithm Processing Unit (APU)

The APU is a generic mathematical acceleration module that is able to operate with single-precision floating point numbers (IEEE 754 format) and is optimized to work with complex numbers.

The APU operates autonomously from the main CPU in the system and can be used to offload numerically intensive operations. This module handles efficient vector (and matrix) operations and sustains a complex Multiply-and-Add operation per clock cycle.

The APU has an 8kB local data memory (separate from the system RAM) and a core to handle advanced APIs developed for the APU hardware accelerator sub-modules. This core is controlled by the RAM-based local program memory (separate from the system RAM and APU data RAM) where the APU APIs are loaded. TI provides the APU APIs that shall be executed by the APU programmable core.

The APU supports algorithms including: FFT, Eigenvalue decomposition, Matrix factorization, Sorting, Matrix Frobenius Normalization. These are also useful for the upcoming Bluetooth Channel Sounding post-processing operations to perform precise ranging over RF.

1.17 Serial Wire Debug (SWD)

SWD is an industry standard 2-pin Arm® SWD interface used for device programming, configuration and in-circuit debugging. The 2-wire (SWDIO, SWCLK) debug interface is compatible with both TI and 3rd party debug probes and features:

- On-chip pull-up/pull-down resistors for SWDIO and SWCLK, respectively, enabled by default
- Support for disabling SWD functions to use SWD pins as general purpose input/output pins
- Capability of waking the device from SHUTDOWN mode upon valid SWD activity

The Cortex M33 core supports advanced debugging features including DWT (Data Watchpoint and Trace unit) that supports watchpoints and system profiling for the CM33 processor and ITM (Instrumentation Trace Macrocell) that supports printf style debugging to trace Operating System (OS) and application events, and emits diagnostic system information.

Chapter 2

Arm® Cortex®-M33 Processor

The Arm® Cortex®-M33 core brings high-performance 32- bit computing to cost-sensitive embedded microcontroller applications, such as factory automation and control, industrial control power devices, building and home automation, and stepper motor control.

This chapter provides information on the Arm® Cortex®-M33 processor.

For technical details on the instruction set, see section 3.4 – 3.13 of the document.

Arm®Cortex® -M33 Devices Generic User Guide, Revision r1p0

2.1 Arm® Cortex®-M33 Processor Introduction

The Cortex-M33 processor is a high performance, low gate count, highly configurable, and energy efficient processor. It is intended for microcontroller and embedded applications that require an efficient mix of control capability and signal processing instructions. The processor is based on the Arm®v8-M architecture and is primarily for use in environments where security is an important consideration.

The following features are included:

- 96 MHz Operation
- Arm® TrustZone® technology, using the Arm® v8-M Security Extension supporting Secure and Nonsecure states
- Floating-point Extension
- *Digital Signal Processing* (DSP) Extension
- *Custom Datapath Extension* (CDE)
- Memory Protection Unit (MPU) Extension
- Programmable Security Attribution Unit (SAU)
- A *Nested Vectored Interrupt Controller* (NVIC) that is closely integrated with the processor
- Passing on-chip data through a *Trace Port Interface Unit* (TPIU) to a *Trace Port Analyzer* (TPA) using *Serial Wire Output* (SWO) mode
- A ROM table to allow debuggers to determine which components are implemented in the Cortex-M33 processor
- It's an in-order pipeline processor
- It incorporates the Thumb-2 technology
- Harvard architecture characterized by separate buses for instruction and data
- Saturating arithmetic and dedicated hardware division
- Standard trace support
  - Instruction Trace Macrocell (ITM) Extension
  - Trace Port Interface Unit (TPIU) with a Trace Port Analyzer (TPA) including Serial Wire Output (SWO) mode
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace (DWT) and Breakpoint Unit (BPU)
  - SWD (Serial Wire Debug) port
  - Enhanced system debug with up to 4 watchpoints and 8 breakpoints

2.2 M33 instantiation parameters

For more info in Cortex M33, please refer to Arm®'s documentation for TEAL r1p0d.

Other important parameters of CPUSS:

Parameter	Value
JEPID	0010111b
JEPCONT	0000b
PARTNUM	000h
MCU ROM table address	E00FE000h
Processor Rom Table address	E00FF000h
TPIU Base address	E0040000h
VTOR address (Both secure and Non-secure)	01E0000h

2.3 Arm® Cortex®-M33 System Peripheral Details

The Arm® Cortex®-M33 includes the following system components:

2.3.1 Floating Point Unit (FPU)

The Cortex-M33 FPU is an implementation of the single precision variant of the Arm®v8-M Floating point extension, FPv5 architecture. It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

The FPU supports all single-precision data-processing instructions and data types described in the *Arm®v8-M Architecture Reference Manual*.

2.3.2 Memory Protection Unit (MPU)

The MPU improves system reliability by defining the memory attributes for different memory regions. There can be two MPUs, one Secure and one Non-secure. Each MPU can define memory attributes independently. There are 8 secure and 8 non-secure memory regions.

2.3.3 Digital Signal Processing (DSP)

The DSP adds the ability to perform digital-signal processing such as Fast-Fourier Transform (FFT), Discrete Transform (DCT) and Multiply-Accummulate (MAC) by enabling capabilities such as saturating arithmetic, SIMD (Single Instruction, Multiple Data) and others.

2.3.4 Security Attribution Unit (SAU)

The Security Attribution Unit (SAU) determines the security of an address accessed by the processor. For instructions, the SAU returns the security attribute (Secure or Non-secure) and identifies whether the instruction address is in a Non-secure callable region. For data, the SAU returns the security attribute (Secure or Non-secure). When a memory access is performed, the security of the address is verified by the SAU. Any address that matches multiple SAU regions is marked with the most secure attribute of the matching regions. There are 8regions for which security can be defined. The SAU is used with the IDAU and other security configuration settings to fully specify addresses as Secure, Non-secure, or Non-secure callable.

2.3.5 System timer (SysTick)

The processor has two 24-bit system timers, a Non-secure SysTick timer and a Secure SysTick timer. When enabled, each timer counts down from the reload value to zero, reloads (wraps to) the value in the SYST_RVR on the next clock cycle, then decrements on subsequent clock cycles. When the processor is halted for debugging, the counter does not decrement.

2.3.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an embedded interrupt controller (INTC) that supports low-latency interrupt processing. A programmable priority level of 0-255. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority. There is also an external non-maskable interrupt.

2.3.7 System Control Block (SCB)

The SCB is an address region in the System Control Space. The *System Control Block* (SCB) provides system implementation information and system control that includes configuration, control, and reporting of system exceptions.

2.3.8 System Control Space (SCS)

The System Control Space (SCS) is the programmer's model interface to the processor. It provides system implementation information and system control. The processor provides debug through registers in the SCS.

2.4 CPU Sub-System Peripheral Details

The CPU Sub System (CPUSS) encompasses the Arm® Cortex® M33 along with the following external peripherals:

1. Arm® Cortex® M33
2. Trace Port Interface Unit (TPIU)
3. DAP Bridge and Debug Authentication
4. Implementation Defined Attribution Unit (IDAU)

5. Custom Datapath Extension (CDE) instructions

2.4.1 Trace Port Interface Unit (TPIU)

The Trace Port Interface Unit (TPIU) drives trace data to external pins on a target, so that the Trace Port Analyzer (TPA), which is often part of a debug unit, can capture the trace data. The figure below shows the TPIU block diagram (main blocks of the TPIU and the clock domains).

The TPIU:

- Coordinates the stopping of trace capture when it receives a trigger
- Inserts source identification information into the trace stream so that trace data can be re-associated with its trace source
- Outputs the trace data over trace port pins
- Outputs patterns over the trace port. This pattern output is often referred to as TPIU pattern generation. This allows a TPA to tune its capture logic to the trace port, which maximizes the trace data output frequency on the trace port.

TPIU implementation details are found in the Arm® CoreSight System-on-Chip SoC-600 Technical Reference Manual.

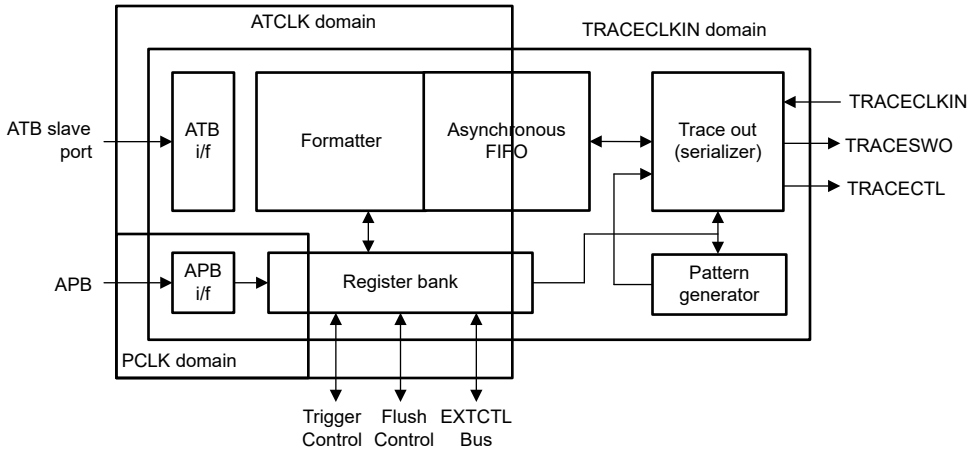

Figure 2-1. TPIU Block Diagram

2.4.2 DAP Bridge and Debug Authentication

The DAP bridge serves as a connection between Serial Wire (SW) Debug Port and AHB-AP Access Port.

There are 4 debug authentication control signals driven from DEBUGSS to CPUSS:-

1. DBGEN (Invasive debug enable)
2. NIDEN (Non-Invasive debug enable)
3. SPNIDEN (Secure Peripheral Non-Invasive Debug Enable)
4. SPIDEN (Secure Peripheral Invasive Debug Enable)

- SPNIDEN and SPIDEN can be overwritten by CPUSS by writing to the DAUTHCTRL MMR of M33.
- For invasive debug enable, DBGEN must be set by configuring the appropriate DEBUGSS MMR using CCFG copy list. For non-invasive debug enable, NIDEN must be set by configuring the appropriate DEBUGSS MMR using CCFG copy list.
- For TPIU to function, NIDEN must be set. Only single wire trace is enabled for TPIU. 4 wire trace is not supported.

Table 2-1. Invasive Debug Access Control

DBGEN	SPIDEN	Invasive Debug Status	Invasive debug permitted states
LOW	X	DISABLED	None
HIGH	LOW	ENABLED	All Non Secure States
HIGH	HIGH	ENABLED	All States

Table 2-2. Non Invasive Debug Access Control

NIDEN	SPNIDEN	States in which non-invasive debug is permitted
LOW	X	None
HIGH	LOW	All Non Secure States
HIGH	HIGH	All States

2.4.3 Implementation Defined Attribution Unit (IDAU)

IDAU along with SAU determines the security attribution of the M33 core. The watermark registers determine which parts of SRAM and Flash are considered Secure, Non-secure callable, or Non-secure. From base address and counting up, these registers define three regions which are first Secure, then Non-secure callable, then Non-secure.

The IDAU region ID for the entire Memory Map is mentioned below:

Address [31:0]	IDAU Region	Region Type
0000_0000h-0FFF_FFFF h	0	Non-secure callable
1000_0000h - 1FFF_FFFFh	1	Non-secure
2000_0000h - 2FFF_FFFFh	2	Non-secure callable
3000_0000h - 3FFF_FFFFh	3	Non-secure
4000_0000h - 4FFF_FFFFh	4	Non-secure callable
5000_0000h - 5FFF_FFFFh	5	Non-secure
6000_0000h - 6FFF_FFFFh	6	Non-secure callable
7000_0000h - 7FFF_FFFFh	7	Non-secure
8000_0000h - 8FFF_FFFFh	8	Non-secure callable
9000_0000h - 9FFF_FFFFh	9	Non-secure
A000_0000h - AFFF_FFFFh	10	Non-secure callable
B000_0000h - BFFF_FFFFh	11	Non-secure
C000_0000h - CFFF_FFFFh	12	Non-secure callable
D000_0000h - DFFF_FFFFh	13	Non-secure
E000_0000h - EFFF_FFFFh	14	Non-secure callable
F000_0000h - FFFF_FFFFh	15	Non-secure

2.4.4 Custom Datapath Extension (CDE)

Four custom instructions have been added as a part of CDE. These are the common instructions supported by HW acceleration leveraging CDE feature of CM33. Ternary MAC and BNN are special types with weight quantization supported to 2 bits and 1 bit respectively therefore enabling multiple operations, such as multiply and accumulate, in single clock cycle. Similarly, MMA (8x8 MAC) supports better throughput than using core

instructions of ARM CPU. Batch normalization layer is also an integral part of CNN and could be repeated depending on the network topology. This helps to speed up the training process and hence instruction support for BN is important for overall performance of typical network.

1. Matrix Multiplication - TMA
2. Matrix Multiply and Accumulate - MMA
3. Batch Normalization - BN
4. Support for Binary Neural Network - BNN

The custom instruction will be of the format:

1. CX3{A} {cond}, <coproc>, <Rd>, <Rn>, <Rm>, #<imm>
2. CX3D{A} {cond}, <coproc>, <Rd>, <Rd+1>, <Rn>, <Rm>, #<imm>

Which of the 4 instructions to execute is decided by the **#<imm>**field. And the opcodes are given below:

1. #imm=0 TMA (Signed)
2. #imm=1 BNORM
3. #imm=2 BNN
4. #imm=3 TMA (Unsigned)
5. #imm=4 MMA (Signed)
6. #imm=5 MMA (Unsigned)

The pseudocode for each of the instructions is mentioned below:

```
#define COPROC 0
#define imm_TMA4X4S 0
#define imm_BNORM4 1
#define imm_BNN16X4 2
#define imm_TMA4X4U 3
#define imm_MMA2X2S 4
#define imm_MMA2X2U 5
uint64_t Rd;
uint64_t Y;
uint32_t Rn, Rm;
```

Ternary Matrix Multiply and Accumulate (TMA)

Y = __arm_cx3da(COPROC, Rd, Rn, Rm, imm_TMA4X4S); //Y is 64 bit result

Y = {Rd+1(t+1), Rd(t+1)}

Rd(t+1) = {Y[1], Y[0]}

Rd+1(t+1) = {Y[3], Y[2]}

*Y[3] = Saturate (sign_extend(Rd+1[31:16]) + Rm[7:6] * sign_extend(Rn[31:24]) + Rm[5:4] * sign_extend(Rn[23:16]) + Rm[3:2] * sign_extend(Rn[15:8]) + Rm[1:0] * sign_extend(Rn[7:0]))*

*Y[2] = Saturate (sign_extend(Rd+1[15:0]) + Rm[7:6] * sign_extend(Rn[31:24]) + Rm[5:4] * sign_extend(Rn[23:16]) + Rm[3:2] * sign_extend(Rn[15:8]) + Rm[1:0] * sign_extend(Rn[7:0]))*

*Y[1] = Saturate (sign_extend(Rd[31:16]) + Rm[7:6] * sign_extend(Rn[31:24]) + Rm[5:4] * sign_extend(Rn[23:16]) + Rm[3:2] * sign_extend(Rn[15:8]) + Rm[1:0] * sign_extend(Rn[7:0]))*

*Y[0] = Saturate (sign_extend(Rd[15:0]) + Rm[7:6] * sign_extend(Rn[31:24]) + Rm[5:4] * sign_extend(Rn[23:16]) + Rm[3:2] * sign_extend(Rn[15:8]) + Rm[1:0] * sign_extend(Rn[7:0]))*

Y = __arm_cx3da(COPROC, Rd, Rn, Rm, imm_TMA4X4U); //Y is 64 bit result

Y = {Rd+1(t+1), Rd(t+1)}

Rd(t+1) = {Y[1], Y[0]}

Rd+1(t+1) = {Y[3], Y[2]}

*Y[3] = Saturate (sign_extend(Rd+1[31:16]) + Rm[7:6] * Rn[31:24] + Rm[5:4] * Rn[23:16] + Rm[3:2] * Rn[15:8] + Rm[1:0] * Rn[7:0])*

*Y[2] = Saturate (sign_extend(Rd+1[15:0]) + Rm[7:6] * Rn[31:24] + Rm[5:4] * Rn[23:16] + Rm[3:2] * Rn[15:8] + Rm[1:0] * Rn[7:0])*

*Y[1] = Saturate (sign_extend(Rd[31:16]) + Rm[7:6] * Rn[31:24] + Rm[5:4] * Rn[23:16] + Rm[3:2] * Rn[15:8] + Rm[1:0] * Rn[7:0])*

*Y[0] = Saturate (sign_extend(Rd[15:0]) + Rm[7:6] * Rn[31:24] + Rm[5:4] * Rn[23:16] + Rm[3:2] * Rn[15:8] + Rm[1:0] * Rn[7:0])*

Binary Neural Network (BNN)

Y = __arm_cx3da(COPROC, Rd, Rn, Rm, imm_BNN16X4); //Y is 64 bit result

Y = {Rd+1(t+1), Rd(t+1)}

Rd(t+1) = {Y[1], Y[0]}

Rd+1(t+1) = {Y[3], Y[2]}

Y[3] = sign_extend(Rd+1[31:16]) + sign_extend(POPCOUNT(Rn[31:16] XNOR Rm[31:16]))

Y[2] = sign_extend(Rd+1[15:0]) + sign_extend(POPCOUNT(Rn[31:16] XNOR Rm[15:0]))

Y[1] = sign_extend(Rd[31:16]) + sign_extend(POPCOUNT(Rn[15:0] XNOR Rm[31:16]))

Y[0] = sign_extend(Rd[15:0]) + sign_extend(POPCOUNT(Rn[15:0] XNOR Rm[15:0]))

Matrix Multiply and Accumulate (MMA)

Y = __arm_cx3da(COPROC, Rd, Rn, Rm, imm_MMA2X2S); //Y is 64 bit result

Y = {Rd+1(t+1), Rd(t+1)}

Rd(t+1) = {Y[1], Y[0]}

Rd+1(t+1) = {Y[3], Y[2]}

{Y[1], Y[0]} = Saturate(sign_extend(Rd) + { sign_extend(Rn[7:0]) sign_extend(Rm[7:0]) + sign_extend(Rn[15:8])* sign_extend(Rm[15:8])})*

{Y[3], Y[2]} = Saturate(sign_extend(Rd+1) + { sign_extend(Rn[23:16]) sign_extend(Rm[23:16]) + sign_extend(Rn[31:24])* sign_extend(Rm[31:24])})*

Y = __arm_cx3da(COPROC, Rd, Rn, Rm, imm_MMA2X2U); //Y is 64 bit result

Y = {Rd+1(t+1), Rd(t+1)}

Rd(t+1) = {Y[1], Y[0]}

Rd+1(t+1) = {Y[3], Y[2]}

*{Y[1], Y[0]} = Saturate(sign_extend(Rd) + {Rn[7:0] * sign_extend(Rm[7:0]) + Rn[15:8] * sign_extend(Rm[15:8])})*

*{Y[3], Y[2]} = Saturate(sign_extend(Rd+1) + {Rn[23:16] * sign_extend(Rm[23:16]) + Rn[31:24] * sign_extend(Rm[31:24])})*

Batch Normalization (BN)

Y = __arm_cx3da(COPROC, Rd, Rn, Rm, imm_BNORM4); //Y is 32 bit result

Y = Rd(t+1)

Cycle 1

Rd(t+1)[15:8] = clamp([((Rd[31:24] sign_extend(Rn[15:8]))<<8) + (Rd[23:16]* sign_extend(Rn[15:8]))] >> Rm[21:17])*

Rd(t+1)[7:0] = clamp([((Rd[15:8] sign_extend(Rn[7:0]))<<8) + (Rd[7:0]* sign_extend(Rn[7:0]))] >> Rm[16:12])*

Cycle 2

Rd(t+1)[31:24] = clamp([((Rd+1[31:24] sign_extend(Rn[31:24]))<<8) + (Rd+1[23:16]* sign_extend(Rn[31:24]))) >> Rm[31:27])*

Rd(t+1)[23:16] = clamp([((Rd+1[15:8] sign_extend(Rn[23:16]))<<8) + (Rd+1[7:0]* sign_extend(Rn[23:16]))] >> Rm[26:22])*

Other important points:

1. **<coproc>** has to be 0
2. 2x32 bit registers (Rd, Rd+1) represent 4x16 bit data, each 16-bit data to be treated as **signed** and Rd, Rd+1 individually are ***not*** signed 32 bit numbers. Applicable for instructions **#imm - 0, 1, 2, 3**
3. 2x32 bit registers (Rd, Rd+1) represent 2x32 bit data, each to be treated as **signed**. Applicable for instructions **#imm - 4,5**
4. Additional decodes from instruction opcodes - **Applicable only for BN**
    a. Clamp High - Use upper 9 bit value (11:3) as signed value directly as clamp high value
    b. Clamp Low - Use lower 3 bits to decode i.e. (2:0) : 000 → 0, 001 → -2, 010 → -4, 011 → -8, 100 → -16, 101 → -32, 110 → -64, 111 → -128
5. Some SCB registers that might need to be programmed based on security state of the processor:
    a. SCB -->CPACR (Coprocessor Access Control Register) - The CPACR register specifies the access privileges for coprocessors.
    b. SCB -->NSACR (Non secure Access Control Register) - The NSACR register defines the Non-secure access permissions for both the FPU and coprocessors CP
    c. SCB -->CPPWR (Coprocessor Power Control Register) - Applicable for co-processor and not for CDE logic since CDE logic shares its power domain with the CPU
6. The 'popcount' block in the data flow diagram of **BN** operation calculates the number of 1s in the 16 bit signal which is input to the block.

2.5 Programming Model

The Cortex-M33 programmer's model is an implementation of the Arm®v8-M Main Extension architecture. For a complete description of the programmer's model, refer to the *Arm®v8-M Architecture Reference Manual*, which also contains the Arm®v8-M Thumb® instructions.

2.5.1 Modes of operation and execution

The Cortex-M33 processor supports Secure and Non-secure security states, Thread and Handler operating modes, and can run in either Thumb or Debug operating states. In addition, the processor can limit or exclude access to some resources by executing code in privileged or unprivileged mode. See the *Arm®v8-M Architecture Reference Manual* for more information about the modes of operation and execution.

2.5.1.1 Security states

The programmers model includes two orthogonal security states, Secure state and Non-secure state. When the Security Extension is implemented, the processor always resets into Secure state. When the security state is not implemented, the processor resets into Non-secure state. Each security state includes a set of independent operating modes and supports both privileged and unprivileged user access. Registers in the System Control Space are banked across Secure and Non-secure state, with the Non-secure register view available at an aliased address to Secure state.

2.5.1.2 Operating modes

For each security state, the processor can operate in Thread or Handler mode. The conditions which cause the processor to enter Thread or Handler mode are as follows:

- The processor enters Thread mode on reset, or as a result of an exception return to Thread mode. Privileged and Unprivileged code can run in Thread mode.
- The processor enters Handler mode as a result of an exception. All code is privileged in Handler mode.

The processor can change security state on taking an exception, for example when a Secure exception is taken from Non-secure state, the Thread mode enters the Secure state Handler mode. The processor can also call Secure functions from Non-secure state and Non-secure functions from Secure state. The Security Extension includes requirements for these calls to prevent secure data from being accessed in Non-secure state.

2.5.1.3 Operating states

The processor can operate in Thumb or Debug state:

- Thumb state is the state of normal execution running 16-bit and 32-bit halfword-aligned Thumb instructions.
- Debug state is the state when the processor is in Halting debug.

2.5.1.4 Privileged access and unprivileged user access

Code can execute as privileged or unprivileged. Unprivileged execution limits or excludes access to some resources appropriate to the current security state. Privileged execution has access to all resources available to the security state. Handler mode is always privileged. Thread mode can be privileged or unprivileged.

2.5.2 Instruction set summary

The processor implements the following instruction from Arm®v8-M:

- All base instructions.
- All instructions in the Main Extension.
- Optionally all instructions in the Security Extension.
- Optionally all instructions in the DSP Extension.
- Optionally all single-precision instructions and double precision load and store instructions in the

Floating-point Extension.

For more information about Arm® v8-M instructions, see the *Arm ®v8-M Architecture Reference Manual*.

2.5.3 Memory model

The processor contains a bus matrix that arbitrates instruction fetches and memory accesses from the processor core between the external memory system and the internal *System Control Space* (SCS) and debug components. Priority is usually given to the processor to ensure that any debug accesses are as non-intrusive as possible. The system memory map is Arm®v8-M Main Extension compliant, and is common both to the debugger and processor accesses. The default memory map provides user and privileged access to all regions except for the *Private Peripheral Bus* (PPB). The PPB space is privileged access only.

The following table shows the default memory map.

Address Range	Region	Interface
0x00000000-0x1FFFFFFF	Code	Instruction and data accesses performed on C-AHB.
0x20000000-0x3FFFFFFF	SRAM	Instruction and data accesses performed on S-AHB. Any attempt to execute instructions from the peripheral and external device region results in a MemManage fault.
0x40000000-0x5FFFFFFF	Peripheral	
0x60000000-0x9FFFFFFF	External RAM	
0xA0000000-0xDFFFFFFF	External device	

Address Range	Region	Interface
0xE0000000-0xE00FFFFF	PPB	Reserved for system control and debug. Cannot be used for exception vector tables. Data accesses are either performed internally or on EPPB. Accesses in the range: **0xE0000000-0xE0043FFF** Are handled within the processor. **0xE0044000-0xE00FFFFF** Appear as APB transactions on the EPPB interface of the processor. Any attempt to execute instructions from the region results in a MemManage fault.
0xE0100000-0xFFFFFFFF	Vendor_SYS	Partly reserved for future processor feature expansion. Any attempt to execute instructions from the region results in a MemManage fault. Data accesses are performed on S-AHB

The security level associated with an address is determined by either the internal *Secure Attribution Unit* (SAU) or an external *Implementation Defined Attribution Unit* (IDAU) in the system. Some internal peripherals have memory-mapped registers in the PPB region which are banked between Secure and Non-secure state. When the processor is in Secure state, software can access both the Secure and Non-secure versions of these registers. The Non-secure versions are accessed using an aliased address. See the *Arm®v8-M Architecture Reference Manual* for more information about the memory model.

2.5.3.1 Private Peripheral Bus

The *Private Peripheral Bus* (PPB) memory region provides access to internal and external processor resources.

The internal PPB provides access to:

- The *System Control Space* (SCS), including the *Memory Protection Unit* (MPU), *Secure Attribution Unit* (SAU), and the *Nested Vectored Interrupt Controller* (NVIC).
- The *Data Watchpoint and Trace* (DWT)
- The *Breakpoint Unit* (BPU)
- The ROM table

The *external PPB* (EPPB) provides access to implementation-specific external areas of the PPB memory map.

2.5.3.2 Unaligned accesses

The Cortex-M33 processor supports unaligned accesses. They are converted into two or more aligned AHB transactions on the C-AHB or S-AHB master ports on the processor. Unaligned support is only available for load/store singles (LDR, LDRH, STR, STRH, TBH) to addresses in Normal memory. Load/store double and load/store multiple instructions already support word aligned accesses, but do not permit other unaligned accesses, and generate a fault if this is attempted. Unaligned accesses in Device memory are not permitted and fault. Unaligned accesses that cross memory map boundaries are architecturally UNPREDICTABLE.

Note

If CCR.UNALIGN_TRP for the current Security state is set, any unaligned accesses generate a fault.

2.5.4 Processor core registers summary

The following table shows the processor core register set summary. Each of these registers is 32 bits wide. Some of the registers are banked. The Secure view of these registers is available when the Cortex-M33 processor is in Secure state and the Non-secure view when Cortex-M33 processor is in Non-secure state.

Name	Description
R0-R12	R0-R12 are general-purpose registers for data operations.

Name	Description
MSP (R13) PSP (R13)	The *Stack Pointer* (SP) is register R13. In Thread mode, the CONTROL register indicates the stack pointer to use, *Main Stack Pointer* (MSP) or *Process Stack Pointer* (PSP). There are two MSP registers in the Cortex-M33 processor: • MSP_NS for the Non-secure state. • MSP_S for the Secure state. There are two PSP registers in the Cortex-M33 processor: • PSP_NS for the Non-secure state. • PSP_S for the Secure state.
MSPLIM PSPLIM	The stack limit registers limit the extent to which the MSP and PSP registers can descend respectively. There are two MSPLIM registers in the Cortex-M33 processor: • MSPLIM_NS for the Non-secure state. • MSPLIM_S for the Secure state. There are two PSPLIM registers in the Cortex-M33 processor: • PSPLIM_NS for the Non-secure state. • PSPLIM_S for the Secure state.
LR (R14)	The *Link Register* (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions.
PC (R15)	The *Program Counter* (PC) is register R15. It contains the current program address.
PSR	The *Program Status Register* (PSR) combines: • *Application Program Status Register* (APSR). • *Interrupt Program Status Register* (IPSR). • *Execution Program Status Register* (EPSR). These registers provide different views of the PSR.
PRIMASK	The PRIMASK register prevents activation of exceptions with configurable priority. There are two PRIMASK registers in the Cortex-M33 processor: • PRIMASK_NS for the Non-secure state. • PRIMASK_S for the Secure state.
BASEPRI	The BASEPRI register defines the minimum priority for exception processing. There are two BASEPRI registers in the Cortex-M33 processor: • BASEPRI_NS for the Non-secure state. • BASEPRI_S for the Secure state.
FAULTMASK	The FAULTMASK register prevents activation of all exceptions except for NON-MASKABLE INTERRUPT (NMI) and optionally Secure HardFault. There are two FAULTMASK registers in the Cortex-M33 processor: • FAULTMASK_NS for the Non-secure state. • FAULTMASK_S for the Secure state.
CONTROL	The CONTROL register controls the stack used, and optionally the privilege level, when the processor is in Thread mode. There are two CONTROL registers in the Cortex-M33 processor: • CONTROL_NS for the Non-secure state. • CONTROL_S for the Secure state.

Note

See the *Arm®v8-M Architecture Reference Manual* for information about the processor core registers and their addresses, access types, and reset values.

2.5.5 Exceptions

Exceptions are handled and prioritized by the processor and the NVIC. In addition to architecturally defined behavior, the processor implements advanced exception and interrupt handling that reduces interrupt latency and includes implementation defined behavior.

2.5.5.1 Exception handling and prioritization

The processor core and the *Nested Vectored Interrupt Controller* (NVIC) together prioritize and handle all exceptions.

When handling exceptions:

- All exceptions are handled in Handler mode.
- Processor state is automatically stored to the stack on an exception, and automatically restored from the stack at the end of the *Interrupt Service Routine* (ISR).
- The vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining that enables back-to-back interrupts without the overhead of state saving and restoration.

Software can configure the priorities of these interrupts.

Exceptions can be specified as either Secure or Nonsecure. When an exception is taken the processor switches to the associated security state. The priority of Secure and Non-secure exceptions can be programmed independently. It is possible to deprioritize Nonsecure configurable exceptions using the AIRCR.PRIS bit field to enable Secure interrupts to take priority.

When taking and returning from an exception, the register state is always stored using the stack pointer associated with the background security state. When taking a Non-secure exception from Secure state, all the register state is stacked and then registers are cleared to prevent Secure data being available to the Non-secure handler. The vector base address is banked between Secure and Non-secure state. VTOR_S contains the Secure vector base address, and VTOR_NS contains the Non-secure vector base address. These registers can be programmed by software, and also initialized at reset by the system.

Note

Vector table entries are compatible with interworking between Arm® and Thumb instructions. This causes bit[0] of the vector value to load into the *Execution Program Status Register* (EPSR) T-bit on exception entry. All populated vectors in the vector table entries must have bit[0] set. Creating a table entry with bit[0] clear generates an INVSTATE fault on the first instruction of the handler corresponding to this vector.

2.6 TrustZone-M

The system implements a Arm® Cortex® M33 with security extensions, Secure and Non-secure MPU with 8 regions each and SAU with 8 regions.

TCM provides flash and SRAM memory watermark inputs to flash controller and SRAM controller. This watermark defines the secure memory address range from the base address of flash and SRAM respectively.

The watermark configuration resolution is 1kB for SRAM and 8kB for flash.

Access permissions to the memory address range is as below.

- When secure access is made to watermarked address range, write and read accesses are allowed.
- Secure accesses to memory outside watermarked address range are not allowed with write ignored and read returning 0.

- When non-secure access is made outside watermarked address range, write and read accesses are allowed.
- Non-secure accesses to watermarked address range are not allowed with write ignored and read returning 0.

Writes to memory addresses beyond the physical size of available memory are ignored and read returns 0 for both secure as well as non-secure accesses.

2.6.1 Overview

The TrustZone-M consist of the following elements:

- IDAU configuration of background security memory attribution
- Trustzone Control Module (TCM), holding registers to control other TrustZone related features
- Periphery and control gaskets to enforce restrictions and enable selectable attribution of memory mapped registers
- Structures in memories to allocated memory to Secure and Non Secure memory region

2.6.2 M33 Configuration

M33 configuration:

- Floating Point Unit (FPU)
- Digital signal processing instructions
- Security extensions (Trustzone)
- NS MPU regions: 8
- S MPU regions 8
- SAU regions: 8
- IRQ priority levels: 16 (4 bits)
- 2 software interrupts
- Debug
  - 4 watchpoints
  - 8 breakpoint comparators
  - Data watchpoint and instrumentation trace (DWT/ITM)
  - ETM trace

2.6.3 Description of elements

2.6.3.1 IDAU (Implementation Defined Attribution Unit)

The IDAU defines a background memory map as follows:

If Address bit 28 (hereafter A[28]) is 0 then the address is attributed Non-Secure Callable (NSC).

Note

NSC attributed addresses are also Secure addresses

If A[28]=1 then the address is attributed Non-Secure (NS).

2.6.3.1.1 Expected use

The IDAU does not attribute any region directly as secure (S) because it is not allowed to change a S region to NSC. For addresses attributed Execute-never (XN) the distinction does not matter but for executable memory the user is responsible to use the SAU to mark regions not intended to be NSC as S. Best practice is to mark all Flash and SRAM that does not explicitly hold the SG (Secure Gateway) instructions as S or NS. I.e. mark all but a region of the Flash and SRAM NSC regions as S where the remaining region holds all the SG instructions. If you do not execute secure code with SG calls from NS in SRAM mark all of SRAM NSC region as S.

2.6.3.2 Gaskets

Peripheries and controllers other than the CPU are equipped with bus gaskets that control their interaction with the TrustZone-M system.

The TCM and flash subsystems do not have periphery gaskets. These are always mapped to NSC marked memory and cannot be moved into NS memory space.

2.6.3.2.1 Periphery gasket

Peripheries are by default mapped in the NSC marked region 0x4000 0000 - 0x4FFF FFFF. Each periphery has a gasket that can move it into the 0x5000 0000 0x5FFF FFFF range which is marked NS. This happens when a control signal is sent to the gasket from the TCM. The gaskets shall only be configured at boot. Run-time reconfiguration outside of TI delivered code is not supported and may lead to malfunctions. The new address is given by the old address + 0x1000 0000.

Note

An access to a region where the periphery is NOT mapped will not result in a BusFault, instead you will read zero/ignored write.

2.6.3.2.2 Controller gasket

Controllers (devices that generate bus transactions) other than the main CPU have a gasket that may block transactions from the controller to NSC marked memory. By default controllers are not blocked. If this gasket is enabled through a signal from TCM then transactions where A[28]=0 are blocked. A blocked read transaction will cause an error indication to the controller and will return data as 0x0. A blocked write transaction will cause an error to the controller. Blocked transactions do not propagate on the bus past the gasket.

Note

Non-CPU controllers will also have a periphery port for control. This periphery port is secured independently from the controller port and has a gasket just like any other periphery.

2.6.3.3 Memories

Memories (Flash and SRAM) has each a watermark feature where a boundary can be set in the TCM. Memory past this boundary is remapped to a new address equal to the old address + 0x1000 0000. Thus memory past the watermark now exist in NS memory space and can be accessed by a NS context.

2.6.3.4 TCM

The Trustzone Control Module (TCM) holds protected registers intended to configure the system outside the CPU.

Each register has the following form:

- 31: Parity covering bits 23:16
- 30: Parity covering bits 15:8
- 29: Parity covering bits 7:0
- 28:24: 0
- 23:0: Data

The data field contains either control bits for all gaskets or sets the watermark for memories.

If the parity is wrong at the time of writing or at any time during operation, the device will perform a security reset as this is evidence of external tampering with security features.

Watermark has a limited resolution, providing a granularity of 1024 bytes for SRAM and 8kB for Flash.

If the TCM is not reconfigured from its initial state then the entire system is operating in Secure mode. This is the correct backwards compatible mode of operation with non TrustZone-M systems, and is the expected mode if no TrustZone-M features are needed.

Bootcode can configure TCM securely based on user configuration.

As the TCM changes the system address map, special precautions must be taken to ensure no data corruption occurs when it is modified. Please refer to TI provided code or code already deployed in the system in ROM to reconfigure TCM safely.

2.6.4 TCM Registers

Table 2-3 lists the memory-mapped registers for the TCM registers. All register offset addresses not listed in Table 2-3 should be considered as reserved locations and the register contents should not be modified.

Table 2-3. TCM Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 2.6.4.1
4h	DESCEX	Extended Module Description	Section 2.6.4.2
8h	REGWEN	Register Write Enable	Section 2.6.4.3
Ch	WMCFG	VIMS and SRAM watermark configurations	Section 2.6.4.4
10h	GSKEN0	Gasket configuration	Section 2.6.4.5
14h	GSKEN1	Gasket configuration	Section 2.6.4.6

Complex bit access types are encoded to fit into small table cells. Table 2-4 shows the codes that are used for access types in this section.

Table 2-4. TCM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.6.4.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 2-5.

Return to the Summary Table.

This register identifies the peripheral and its exact version. ;This register is strictly read-only. Any write to this register will trigger chip reset.

Table 2-5. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6F44h	Module identification contains a unique peripheral identification number.
15-12	STDIPOFF	R	0h	Standard IP registers offset. Value 0 indicates Standard IP registers are not present. Any other value between 1 to 15 indicates standard IP registers start from address offset 64 * STDIPOFF from base address.
11-8	INSTIDX	R	0h	Instance Index within the device. This will be a parameter to the RTL for modules that can have multiple instances.
7-4	MAJREV	R	1h	Major rev of the IP
3-0	MINREV	R	0h	Minor rev of the IP

2.6.4.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 2-6.

Return to the Summary Table.

This register identifies the peripheral and its exact version.;This register is strictly read-only. Any write to this register will trigger chip reset.

Table 2-6. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	GSKCNT	R	29h	Number of gaskets

2.6.4.3 REGWEN Register (Offset = 8h) [Reset = 00000000h]

REGWEN is shown in Table 2-7.

Return to the Summary Table.

This register blocks writes to all the MMR of TCM once set. This register is protected by odd parity bit. It is sticky 1.

Table 2-7. REGWEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-29	PAR	R/W	1h	Parity bit. Bit 29 stores the odd parity for bits 0 to 7. Bit 30 stores the odd parity of bits 8 to 15.;PAR[29] = ~WEN;PAR[30] = ~SYNC
28-9	RESERVED	R	0h	Reserved
8	SYNC	R/W	1h	Program this bit to 0 before writing to WMCFG or any of the gasket enable MMR i.e. GSKEN0, GSKEN1 etc.;Once the MMR writes are done, program this bit to 1 again.;Then WEN can be programmed 1 to lock the configuration.;Note:;Do not toggle SYNC and WEN in the same cycle 0h = Set 1h = Reset
7-1	RESERVED	R	0h	Reserved
0	WEN	R/W	0h	Write enable 0h = Enable writes 1h = Disable writes

2.6.4.4 WMCFG Register (Offset = Ch) [Reset = 00000000h]

WMCFG is shown in Table 2-8.

Return to the Summary Table.

This register is used to configure SRAM and VIMS watermark. This register is protected by odd parity bits.

Table 2-8. WMCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PAR	R/W	6h	Parity bits. Bit 29 stores the odd parity for bits 0 to 7. Bit 30 stores the odd parity of bits 8 to 15. Bit 31 stores the odd parity of bits 23 to 16.;PAR[29] = ~XOR(VIMSWM[7:0]);PAR[30] = ~XOR({[VIMSWM[9:8]], SRAMWM[15:12]});PAR[31] = ~XOR(SRAMWM[21:16])
28-20	RESERVED	R	0h	Reserved
19-12	SRAMWM	R/W	FFh	SRAM Watermark.;The address from (SRAM Base Address) to (SRAM Base Address + (SRAMWM + 1)<<10 - 1) is considered secure.;The address from (SRAM Base Address + (SRAMWM + 1) <<10) to (SRAM Last Address) is considered Non-secure.
11-7	RESERVED	R	0h	Reserved
6-0	VIMSWM	R/W	7Fh	VIMS Watermark;The address from (Flash Main Base Address) to (Flash Main Base Address + (VIMSWM + 1)<<13 - 1) is considered secure.;The address from (Flash Main Base Address + (VIMSWM + 1)<<13) to (Flash Main Last Address) is considered Non-secure.

2.6.4.5 GSKEN0 Register (Offset = 10h) [Reset = 00000000h]

GSKEN0 is shown in Table 2-9.

Return to the Summary Table.

This register is used to store gasket configuration. This register is protected by odd parity bits.

Table 2-9. GSKEN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PAR	R/W	6h	Parity bits. Bit 29 stores the odd parity for bits 0 to 7. Bit 30 stores the odd parity of bits 8 to 15. Bit 31 stores the odd parity of bits 23 to 16.;PAR[29] = ~XOR(GSKEN0[7:0]);PAR[30] = ~XOR(GSKEN0[15:8]);PAR[31] = ~XOR(GSKEN0[23:16])
28-24	RESERVED	R	0h	Reserved
23-0	EN	R/W	00FFFFF8h	Gasket enable. The gasket bit to IP mapping is given as follows :-;[0] = DMA initiator gasket enable;[1] = I2S initiator gasket enable;[2] = HSM initiator gasket enable;[3] = Radio target gasket enable;[4] = AES target gasket enable;[5] = I2S target gasket enable;[6] = PDM target gasket enable;[7] = AFA target gasket enable;[8] = DMA target gasket enable;[9] = CANFD target gasket enable;[10] = APU target gasket enable;[11] = APURAM target gasket enable;[12] = GPIO target gasket enable;[13] = SYSTIMER target gasket enable;[14] = UART0 target gasket enable;[15] = UART1 target gasket enable;[16] = SPI0 target gasket enable;[17] = SPI1 target gasket enable;[18] = I2C0 target gasket enable;[19] = EVTSVT target gasket enable;[20] = ADC target gasket enable;[21] = MICADC target gasket enable;[22] = MICPGA target gasket enable;[23] = CLKCTRL target gasket enable

2.6.4.6 GSKEN1 Register (Offset = 14h) [Reset = 00000000h]

GSKEN1 is shown in Table 2-10.

Return to the Summary Table.

This register is used to store gasket configuration. This register is protected by odd parity bits.

Table 2-10. GSKEN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PAR	R/W	3h	Parity bits. Bit 29 stores the odd parity for bits 0 to 7. Bit 30 stores the odd parity of bits 8 to 15. Bit 31 stores the odd parity of bits 23 to 16.;PAR[29] = ~XOR(GSKEN1[7:0]);PAR[30] = ~XOR(GSKEN1[15:8]);PAR[31] = ~XOR(GSKEN1[23:16])
28-17	RESERVED	R	0h	Reserved
16-0	EN	R/W	0001FFFFh	Gasket enable. The gasket bit to IP mapping is given as follows :-;[0] = LGPT target gasket enable;[1] = FLASH target gasket enable;[2] = VIMS target gasket enable;[3] = HSM target gasket enable;[4] = PMC target gasket enable;[5] = CKMDIG target gasket enable;[6] = RTC target gasket enable;[7] = IOC target gasket enable;[8] = SYS0 target gasket enable;[9] = EVTULL target gasket enable;[10] = PMUDIG target gasket enable;[11] = DEBUGSS target gasket enable;[12] = HSM mailbox 1 target gasket enable;[13] = HSM mailbox 2 target gasket enable;[14] = HSM mailbox 3 target gasket enable;[15] = HSM mailbox 4 target gasket enable;[16] = HSM config target gasket enable;[17] = Flash BANK 2 Trim read gasket enable;[18] = Flash BANK 2 Non main region 0 read gasket enable;[19] = Flash BANK 2 Non main region 1 read gasket enable;[20] = Flash BANK 3 Trim read gasket enable;[21] = Flash BANK 3 Non main region 0 read gasket enable;[22] = Flash BANK 3 Non main region 1 read gasket enable

2.7 Arm® Cortex®-M33 Registers

2.7.1 CPU_ROM_TABLE Registers

Table 2-11 lists the memory-mapped registers for the CPU_ROM_TABLE registers. All register offset addresses not listed in Table 2-11 should be considered as reserved locations and the register contents should not be modified.

Table 2-11. CPU_ROM_TABLE Registers

Offset	Acronym	Register Name	Section
0h	SCS_ENTRY	SCS component	Section 2.7.1.1
4h	DWT_ENTRY	Data watchpoint unit	Section 2.7.1.2
8h	FPB_ENTRY	Flash Patch and Breakpoint unit	Section 2.7.1.3
Ch	ITM_ENTRY	never implemented	Section 2.7.1.4
10h	TPIU_ENTRY	Trace Port Interface unit	Section 2.7.1.5
14h	ETM_ENTRY	Embedded Trace Macrocell	Section 2.7.1.6
18h	CTI_ENTRY	Cross Trigger Interface	Section 2.7.1.7
1Ch	MTB_ENTRY	Micro Trace Buffer	Section 2.7.1.8
20h	END_MARKER	end of the rom for discovery	Section 2.7.1.9
FCCh	SYSTEM_ACCESS_ENTRY	SYSTEM ACCESS	Section 2.7.1.10
FD0h	PIDR4	CoreSight Peripheral ID4	Section 2.7.1.11
FD4h	PIDR5	CoreSight Peripheral ID5	Section 2.7.1.12
FD8h	PIDR6	CoreSight Peripheral ID6	Section 2.7.1.13
FDCh	PIDR7	CoreSight Peripheral ID7	Section 2.7.1.14
FE0h	PIDR0	CoreSight Peripheral ID0	Section 2.7.1.15
FE4h	PIDR1	CoreSight Peripheral ID1	Section 2.7.1.16
FE8h	PIDR2	CoreSight Peripheral ID2	Section 2.7.1.17
FECh	PIDR3	CoreSight Peripheral ID3	Section 2.7.1.18
FF0h	CIDR0	CoreSight Component ID0	Section 2.7.1.19
FF4h	CIDR1	CoreSight Component ID1	Section 2.7.1.20
FF8h	CIDR2	CoreSight Component ID2	Section 2.7.1.21
FFCh	CIDR3	CoreSight Component ID3	Section 2.7.1.22

Complex bit access types are encoded to fit into small table cells. Table 2-12 shows the codes that are used for access types in this section.

Table 2-12. CPU_ROM_TABLE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

2.7.1.1 SCS_ENTRY Register (Offset = 0h) [Reset = 00000000h]

SCS_ENTRY is shown in Table 2-13.

Return to the Summary Table.

SCS component

Table 2-13. SCS_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF0Fh	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

2.7.1.2 DWT_ENTRY Register (Offset = 4h) [Reset = 00000000h]

DWT_ENTRY is shown in Table 2-14.

Return to the Summary Table.

Data watchpoint unit

Table 2-14. DWT_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF02h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

2.7.1.3 FPB_ENTRY Register (Offset = 8h) [Reset = 00000000h]

FPB_ENTRY is shown in Table 2-15.

Return to the Summary Table.

Flash Patch and Breakpoint unit

Table 2-15. FPB_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF03h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

2.7.1.4 ITM_ENTRY Register (Offset = Ch) [Reset = 00000000h]

ITM_ENTRY is shown in Table 2-16.

Return to the Summary Table.

never implemented

Table 2-16. ITM_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF01h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	1h	Indicates whether there is a valid ROM entry at this location.

2.7.1.5 TPIU_ENTRY Register (Offset = 10h) [Reset = 00000000h]

TPIU_ENTRY is shown in Table 2-17.

Return to the Summary Table.

Trace Port Interface unit

Table 2-17. TPIU_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF41h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

2.7.1.6 ETM_ENTRY Register (Offset = 14h) [Reset = 00000000h]

ETM_ENTRY is shown in Table 2-18.

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Embedded Trace Macrocell

Table 2-18. ETM_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF42h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

2.7.1.7 CTI_ENTRY Register (Offset = 18h) [Reset = 00000000h]

CTI_ENTRY is shown in Table 2-19.

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Cross Trigger Interface

Table 2-19. CTI_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF43h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

2.7.1.8 MTB_ENTRY Register (Offset = 1Ch) [Reset = 00000000h]

MTB_ENTRY is shown in Table 2-20.

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Micro Trace Buffer

Table 2-20. MTB_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BASE_ADDR	R	000FFF44h	Base address for master interface 0. Bit[31] is always 0.
11-9	RES0_1	R	0h	Reserved, RES0
8-4	POWER_DOMAIN_ID	R	0h	Indicates the power domain ID of the component. This field is only valid when bit[2] of this register is 0b1. Otherwise this field is 0b1.
3	RES0_0	R	0h	Reserved, RES0
2	POWER_DOMAIN_ID_VALID	R	0h	Indicates whether there is a power domain ID specified in the ROM Table entry
1	FORMAT	R	1h	Indicates the ROM table entry format
0	ENTRY_PRESENT	R	0h	Indicates whether there is a valid ROM entry at this location.

2.7.1.9 END_MARKER Register (Offset = 20h) [Reset = 00000000h]

END_MARKER is shown in Table 2-21.

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end of the rom for discovery

Table 2-21. END_MARKER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.1.10 SYSTEM_ACCESS_ENTRY Register (Offset = FCCh) [Reset = 00000000h]

SYSTEM_ACCESS_ENTRY is shown in Table 2-22.

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SYSTEM ACCESS

Table 2-22. SYSTEM_ACCESS_ENTRY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	1h	Reserved, RES0

2.7.1.11 PIDR4 Register (Offset = FD0h) [Reset = 00000000h]

PIDR4 is shown in Table 2-23.

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CoreSight Peripheral ID4

Table 2-23. PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SIZE	R	0h	Always 0b0000. Indicates that the device only occupies 4KB of memory
3-0	DES_2	R	4h	Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component.

2.7.1.12 PIDR5 Register (Offset = FD4h) [Reset = 00000000h]

PIDR5 is shown in Table 2-24.

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CoreSight Peripheral ID5

Table 2-24. PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.1.13 PIDR6 Register (Offset = FD8h) [Reset = 00000000h]

PIDR6 is shown in Table 2-25.

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CoreSight Peripheral ID6

Table 2-25. PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.1.14 PIDR7 Register (Offset = FDCh) [Reset = 00000000h]

PIDR7 is shown in Table 2-26.

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CoreSight Peripheral ID7

Table 2-26. PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.1.15 PIDR0 Register (Offset = FE0h) [Reset = 00000000h]

PIDR0 is shown in Table 2-27.

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CoreSight Peripheral ID0

Table 2-27. PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PART_0	R	C9h	Bits[7:0] of the 12-bit part number of the component. The designer of the component assigns this part number.

2.7.1.16 PIDR1 Register (Offset = FE4h) [Reset = 00000000h]

PIDR1 is shown in Table 2-28.

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CoreSight Peripheral ID1

Table 2-28. PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	DES_0	R	Bh	Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component.
3-0	PART_1	R	4h	Bits[11:8] of the 12-bit part number of the component. The designer of the component assigns this part number.

2.7.1.17 PIDR2 Register (Offset = FE8h) [Reset = 00000000h]

PIDR2 is shown in Table 2-29.

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CoreSight Peripheral ID2

Table 2-29. PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVISION	R	0h	This device is at r1p0
3	JEDEC	R	1h	Always 1. Indicates that the JEDEC-assigned designer ID is used.
2-0	DES_1	R	3h	Together, PIDR1.DES_0, PIDR2.DES_1, and PIDR4.DES_2 identify the designer of the component.

2.7.1.18 PIDR3 Register (Offset = FECh) [Reset = 00000000h]

PIDR3 is shown in Table 2-30.

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CoreSight Peripheral ID3

Table 2-30. PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVAND	R	0h	Indicates minor errata fixes specific to the revision of the component being used, for example metal fixes after implementation. In most cases, this field is 0b0000. ARM recommends that the component designers ensure that a metal fix can change this field if required, for example, by driving it from registers that reset to 0b0000.
3-0	CMOD	R	0h	Customer Modified. Indicates whether the customer has modified the behavior of the component. In most cases, this field is 0b0000. Customers change this value when they make authorized modifications to this component.

2.7.1.19 CIDR0 Register (Offset = FF0h) [Reset = 00000000h]

CIDR0 is shown in Table 2-31.

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CoreSight Component ID0

Table 2-31. CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_0	R	Dh	Preamble[0]. Contains bits[7:0] of the component identification code

2.7.1.20 CIDR1 Register (Offset = FF4h) [Reset = 00000000h]

CIDR1 is shown in Table 2-32.

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CoreSight Component ID1

Table 2-32. CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	CLASS	R	1h	Class of the component, for example, whether the component is a ROM table or a generic CoreSight component. Contains bits[15:12] of the component identification code.
3-0	PRMBL_1	R	0h	Preamble[1]. Contains bits[11:8] of the component identification code.

2.7.1.21 CIDR2 Register (Offset = FF8h) [Reset = 00000000h]

CIDR2 is shown in Table 2-33.

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CoreSight Component ID2

Table 2-33. CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_2	R	5h	Preamble[2]. Contains bits[23:16] of the component identification code.

2.7.1.22 CIDR3 Register (Offset = FFCh) [Reset = 00000000h]

CIDR3 is shown in Table 2-34.

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CoreSight Component ID3

Table 2-34. CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_3	R	B1h	Preamble[3]. Contains bits[31:24] of the component identification code.

2.7.2 TPIU Registers

Table 2-35 lists the memory-mapped registers for the TPIU registers. All register offset addresses not listed in Table 2-35 should be considered as reserved locations and the register contents should not be modified.

Table 2-35. TPIU Registers

Offset	Acronym	Register Name	Section
0h	SSPSR	Supported Sync Port Sizes	Section 2.7.2.1
4h	CSPSR	Current Sync Port Size	Section 2.7.2.2
10h	ACPR	Async Clock Prescaler	Section 2.7.2.3
F0h	SPPR	Selected Pin Protocol	Section 2.7.2.4
300h	FFSR	Formatter and Flush Status	Section 2.7.2.5
304h	FFCR	Formatter and Flush Control	Section 2.7.2.6
308h	PSCR	Formatter Synchronization Counter	Section 2.7.2.7
FA0h	CLAIMMASK	Claim Tag Mask	Section 2.7.2.8
FA0h	CLAIMSET	Claim Tag Set	Section 2.7.2.9
FA4h	CLAIMTAG	Current Claim Tag	Section 2.7.2.10
FA4h	CLAIMCLR	Claim Tag Clear	Section 2.7.2.11
FC8h	DEVID	Device ID	Section 2.7.2.12

Complex bit access types are encoded to fit into small table cells. Table 2-36 shows the codes that are used for access types in this section.

Table 2-36. TPIU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.2.1 SSPSR Register (Offset = 0h) [Reset = 00000000h]

SSPSR is shown in Table 2-37.

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Supported Sync Port Sizes;This register represents a single port size that is supported on the device, that is, 4, 2 or 1. This is to ensure that tools do not attempt to select a port width that an attached TPA cannot capture.

Table 2-37. SSPSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	FOUR	R	1h	4-bit port size support;0x0: Not supported;0x1: Supported
2	THREE	R	0h	3-bit port size support;0x0: Not supported;0x1: Supported
1	TWO	R	1h	2-bit port size support;0x0: Not supported;0x1: Supported
0	ONE	R	1h	1-bit port size support;0x0: Not supported;0x1: Supported

2.7.2.2 CSPSR Register (Offset = 4h) [Reset = 00000000h]

CSPSR is shown in Table 2-38.

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Current Sync Port Size;This register has the same format as SSPSR but only one bit can be set, and all others must be zero. Writing values with more than one bit set, or setting a bit that is not indicated as supported can cause Unpredictable behavior. On reset this defaults to the smallest possible port size, 1 bit.

Table 2-38. CSPSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	FOUR	R/W	0h	4-bit port enable;Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.
2	THREE	R/W	0h	3-bit port enable;Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.
1	TWO	R/W	0h	2-bit port enable;Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.
0	ONE	R/W	1h	1-bit port enable;Writing values with more than one bit set in CSPSR, or setting a bit that is not indicated as supported in SSPSR can cause Unpredictable behavior.

2.7.2.3 ACPR Register (Offset = 10h) [Reset = 00000000h]

ACPR is shown in Table 2-39.

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Async Clock Prescaler;This register scales the baud rate of the asynchronous output.

Table 2-39. ACPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
12-0	PRESCALER	R/W	0h	Divisor for input trace clock is (PRESCALER + 1).

2.7.2.4 SPPR Register (Offset = F0h) [Reset = 00000000h]

SPPR is shown in Table 2-40.

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Selected Pin Protocol;This register selects the protocol to be used for trace output. ;Note: If this register is changed while trace data is being output, data corruption occurs.

Table 2-40. SPPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1-0	PROTOCOL	R/W	1h	Trace output protocol 0h = TracePort mode 1h = SerialWire Output (Manchester). This is the reset value. 2h = SerialWire Output (NRZ)

2.7.2.5 FFSR Register (Offset = 300h) [Reset = 00000000h]

FFSR is shown in Table 2-41.

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Formatter and Flush Status

Table 2-41. FFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	FTNONSTOP	R	1h	0: Formatter can be stopped;1: Formatter cannot be stopped
2-0	RESERVED	R	0h	This field always reads as zero

2.7.2.6 FFCR Register (Offset = 304h) [Reset = 00000000h]

FFCR is shown in Table 2-42.

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Formatter and Flush Control;When one of the two single wire output (SWO) modes is selected, ENFCONT enables the formatter to be bypassed. If the formatter is bypassed, only the ITM/DWT trace source (ATDATA2) passes through. The TPIU accepts and discards data that is presented on the ETM port (ATDATA1). This function is intended to be used when it is necessary to connect a device containing an ETM to a trace capture device that is only able to capture Serial Wire Output (SWO) data. Enabling or disabling the formatter causes momentary data corruption. ;Note: If the selected pin protocol register (SPPR.PROTOCOL) is set to 0x00 (TracePort mode), this register always reads 0x102, because the formatter is automatically enabled. If one of the serial wire modes is then selected, the register reverts to its previously programmed value.

Table 2-42. FFCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
8	TRIGIN	R/W	1h	Indicates that triggers are inserted when a trigger pin is asserted.
7-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
1	ENFCONT	R/W	1h	Enable continuous formatting:;0: Continuous formatting disabled;1: Continuous formatting enabled
0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

2.7.2.7 PSCR Register (Offset = 308h) [Reset = 00000000h]

PSCR is shown in Table 2-43.

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Periodic Synchronization Control Registers

Table 2-43. PSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4-0	PSCOUNT	R/W	0h	Periodic Synchronization Count. Determines the reload value of the Periodic Synchronization Counter. The reload value takes effect the next time the counter reaches zero. Reads from this register return the reload value programmed into this register;0b00000 Synchronization disabled.;0b00111 128 bytes;0b01000 256 bytes;0b11111 2^{31} bytes

2.7.2.8 CLAIMMASK Register (Offset = FA0h) [Reset = 00000000h]

CLAIMMASK is shown in Table 2-44.

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Claim Tag Mask

Table 2-44. CLAIMMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMMASK	R	Fh	This register forms one half of the Claim Tag value. When reading this register returns the number of bits that can be set (each bit is considered separately):;0: This claim tag bit is not implemented;1: This claim tag bit is not implemented;The behavior when writing to this register is described in CLAIMSET.

2.7.2.9 CLAIMSET Register (Offset = FA0h) [Reset = 00000000h]

CLAIMSET is shown in Table 2-45.

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Claim Tag Set

Table 2-45. CLAIMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMSET	W	Fh	This register forms one half of the Claim Tag value. Writing to this location allows individual bits to be set (each bit is considered separately):;0: No effect;1: Set this bit in the claim tag;The behavior when reading from this location is described in CLAIMMASK.

2.7.2.10 CLAIMTAG Register (Offset = FA4h) [Reset = 00000000h]

CLAIMTAG is shown in Table 2-46.

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Current Claim Tag

Table 2-46. CLAIMTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMTAG	R	0h	This register forms one half of the Claim Tag value. Reading this register returns the current Claim Tag value. ;Reading CLAIMMASK determines how many bits from this register must be used.;The behavior when writing to this register is described in CLAIMCLR.

2.7.2.11 CLAIMCLR Register (Offset = FA4h) [Reset = 00000000h]

CLAIMCLR is shown in Table 2-47.

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Claim Tag Clear

Table 2-47. CLAIMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAIMCLR	W	0h	This register forms one half of the Claim Tag value. Writing to this location enables individual bits to be cleared (each bit is considered separately):;0: No effect;1: Clear this bit in the claim tag.;The behavior when reading from this location is described in CLAIMTAG.

2.7.2.12 DEVID Register (Offset = FC8h) [Reset = 00000000h]

DEVID is shown in Table 2-48.

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Device ID

Table 2-48. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEVID	R	CA0h	This field returns: 0xCA1 if there is an ETM present. 0xCA0 if there is no ETM present.

2.7.3 DCB Registers

Table 2-49 lists the memory-mapped registers for the DCB registers. All register offset addresses not listed in Table 2-49 should be considered as reserved locations and the register contents should not be modified.

Table 2-49. DCB Registers

Offset	Acronym	Register Name	Section
10h	DHCSR	Controls halting debug	Section 2.7.3.1
14h	DCRSR	With the DCRDR, provides debug access to the general-purpose registers, special-purpose registers, and the FP extension registers. A write to the DCRSR specifies the register to transfer, whether the transfer is a read or write, and starts the transfer	Section 2.7.3.2
18h	DCRDR	With the DCRSR, provides debug access to the general-purpose registers, special-purpose registers, and the FP Extension registers. If the Main Extension is implemented, it can also be used for message passing between an external debugger and a debug agent running on the PE	Section 2.7.3.3
1Ch	DEMCR	Manages vector catch behavior and DebugMonitor handling when debugging	Section 2.7.3.4
24h	DAUTHCTRL	This register allows the external authentication interface to be overridden from software.	Section 2.7.3.5
28h	DSCSR	Provides control and status information for Secure debug	Section 2.7.3.6

Complex bit access types are encoded to fit into small table cells. Table 2-50 shows the codes that are used for access types in this section.

Table 2-50. DCB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.3.1 DHCSR Register (Offset = 10h) [Reset = 00000000h]

DHCSR is shown in Table 2-51.

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Controls halting debug

Table 2-51. DHCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RES0	R	0h	Reserved, RES0
26	S_RESTART_ST	R	0h	Indicates the PE has processed a request to clear DHCSR.C_HALT to 0. That is, either a write to DHCSR that clears DHCSR.C_HALT from 1 to 0, or an External Restart Request
25	S_RESET_ST	R	0h	Indicates whether the PE has been reset since the last read of the DHCSR
24	S_RETIRE_ST	R	0h	Set to 1 every time the PE retires one of more instructions
23-21	RES0_1	R	0h	Reserved, RES0
20	S_SDE	R	0h	Indicates whether Secure invasive debug is allowed
19	S_LOCKUP	R	0h	Indicates whether the PE is in Lockup state
18	S_SLEEP	R	0h	Indicates whether the PE is sleeping
17	S_HALT	R	0h	Indicates whether the PE is in Debug state
31-16	DBGKEY	W	0h	A debugger must write 0xA05F to this field to enable write access to the remaining bits, otherwise the PE ignores the write access
16	S_REGRDY	R	0h	Handshake flag to transfers through the DCRDR
15-6	RES0_2	R	0h	Reserved, RES0
5	C_SNAPSTALL	R/W	0h	Allow imprecise entry to Debug state
4	RES0_3	R	0h	Reserved, RES0
3	C_MASKINTS	R/W	0h	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts
2	C_STEP	R/W	0h	Enable single instruction step
1	C_HALT	R/W	0h	PE enter Debug state halt request
0	C_DEBUGEN	R/W	0h	Enable Halting debug

2.7.3.2 DCRSR Register (Offset = 14h) [Reset = 00000000h]

DCRSR is shown in Table 2-52.

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With the DCRDR, provides debug access to the general-purpose registers, special-purpose registers, and the FP extension registers. A write to the DCRSR specifies the register to transfer, whether the transfer is a read or write, and starts the transfer

Table 2-52. DCRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES0	R	0h	Reserved, RES0
16	REGWnR	W	0h	Specifies the access type for the transfer
15-7	RES0_1	R	0h	Reserved, RES0
6-0	REGSEL	W	0h	Specifies the general-purpose register, special-purpose register, or FP register to transfer

2.7.3.3 DCRDR Register (Offset = 18h) [Reset = 00000000h]

DCRDR is shown in Table 2-53.

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With the DCRSR, provides debug access to the general-purpose registers, special-purpose registers, and the FP Extension registers. If the Main Extension is implemented, it can also be used for message passing between an external debugger and a debug agent running on the PE

Table 2-53. DCRDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DBGTMP	R/W	0h	Provides debug access for reading and writing the general-purpose registers, special-purpose registers, and Floating-point Extension registers

2.7.3.4 DEMCR Register (Offset = 1Ch) [Reset = 00000000h]

DEMCR is shown in Table 2-54.

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Manages vector catch behavior and DebugMonitor handling when debugging

Table 2-54. DEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RES0	R	0h	Reserved, RES0
24	TRCENA	R/W	0h	Global enable for all DWT and ITM features
23-21	RES0_1	R	0h	Reserved, RES0
20	SDME	R	0h	Indicates whether the DebugMonitor targets the Secure or the Non-secure state and whether debug events are allowed in Secure state
19	MON_REQ	R/W	0h	DebugMonitor semaphore bit
18	MON_STEP	R/W	0h	Enable DebugMonitor stepping
17	MON_PEND	R/W	0h	Sets or clears the pending state of the DebugMonitor exception
16	MON_EN	R/W	0h	Enable the DebugMonitor exception
15-12	RES0_2	R	0h	Reserved, RES0
11	VC_SFERR	R/W	0h	SecureFault exception halting debug vector catch enable
10	VC_HARDERR	R/W	0h	HardFault exception halting debug vector catch enable
9	VC_INTERR	R/W	0h	Enable halting debug vector catch for faults during exception entry and return
8	VC_BUSERR	R/W	0h	BusFault exception halting debug vector catch enable
7	VC_STATERR	R/W	0h	Enable halting debug trap on a UsageFault exception caused by a state information error, for example an Undefined Instruction exception
6	VC_CHKERR	R/W	0h	Enable halting debug trap on a UsageFault exception caused by a checking error, for example an alignment check error
5	VC_NOCPERR	R/W	0h	Enable halting debug trap on a UsageFault caused by an access to a coprocessor
4	VC_MMERR	R/W	0h	Enable halting debug trap on a MemManage exception
3-1	RES0_3	R	0h	Reserved, RES0
0	VC_CORERESET	R/W	0h	Enable Reset Vector Catch. This causes a warm reset to halt a running system

2.7.3.5 DAUTHCTRL Register (Offset = 24h) [Reset = 00000000h]

DAUTHCTRL is shown in Table 2-55.

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This register allows the external authentication interface to be overridden from software.

Table 2-55. DAUTHCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	INTSPNIDEN	R/W	0h	Internal Secure non-invasive debug enable. Overrides the external Secure non-invasive debug authentication interface
2	SPNIDENSEL	R/W	0h	Secure non-invasive debug enable select. Selects between DAUTHCTRL and the external authentication interface for control of Secure non-invasive debug
1	INTSPIDEN	R/W	0h	Internal Secure invasive debug enable. Overrides the external Secure invasive debug authentication Interfaces.
0	SPIDENSEL	R/W	0h	Secure invasive debug enable select. Selects between DAUTHCTRL and the external authentication interface for control of Secure invasive debug.

2.7.3.6 DSCSR Register (Offset = 28h) [Reset = 00000000h]

DSCSR is shown in Table 2-56.

Return to the Summary Table.

Provides control and status information for Secure debug

Table 2-56. DSCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RES0	R	0h	Reserved, RES0
17	CDSKEY	R/W	0h	Writes to the CDS bit are ignored unless CDSKEY is concurrently written to zero
16	CDS	R/W	0h	This field indicates the current Security state of the processor
15-2	RES0_1	R	0h	Reserved, RES0
1	SBRSEL	R/W	0h	If SBRSELEN is 1 this bit selects whether the Non-secure or the Secure version of the memory-mapped Banked registers are accessible to the debugger
0	SBRSELEN	R/W	0h	Controls whether the SBRSEL field or the current Security state of the processor selects which version of the memory-mapped Banked registers are accessed to the debugger

2.7.4 DIB Registers

Table 2-57 lists the memory-mapped registers for the DIB registers. All register offset addresses not listed in Table 2-57 should be considered as reserved locations and the register contents should not be modified.

Table 2-57. DIB Registers

Offset	Acronym	Register Name	Section
0h	DLAR	Provides CoreSight discovery information for the SCS	Section 2.7.4.1
4h	DLSR	Provides CoreSight discovery information for the SCS	Section 2.7.4.2
8h	DAUTHSTATUS	Provides CoreSight discovery information for the SCS	Section 2.7.4.3
Ch	DDEVARCH	Provides CoreSight discovery information for the SCS	Section 2.7.4.4
1Ch	DDEVTYPE	Provides CoreSight discovery information for the SCS	Section 2.7.4.5
20h	DPIDR4	Provides CoreSight discovery information for the SCS	Section 2.7.4.6
24h	DPIDR5	Provides CoreSight discovery information for the SCS	Section 2.7.4.7
28h	DPIDR6	Provides CoreSight discovery information for the SCS	Section 2.7.4.8
2Ch	DPIDR7	Provides CoreSight discovery information for the SCS	Section 2.7.4.9
30h	DPIDR0	Provides CoreSight discovery information for the SCS	Section 2.7.4.10
34h	DPIDR1	Provides CoreSight discovery information for the SCS	Section 2.7.4.11
38h	DPIDR2	Provides CoreSight discovery information for the SCS	Section 2.7.4.12
3Ch	DPIDR3	Provides CoreSight discovery information for the SCS	Section 2.7.4.13
40h	DCIDR0	Provides CoreSight discovery information for the SCS	Section 2.7.4.14
44h	DCIDR1	Provides CoreSight discovery information for the SCS	Section 2.7.4.15
48h	DCIDR2	Provides CoreSight discovery information for the SCS	Section 2.7.4.16
4Ch	DCIDR3	Provides CoreSight discovery information for the SCS	Section 2.7.4.17

Complex bit access types are encoded to fit into small table cells. Table 2-58 shows the codes that are used for access types in this section.

Table 2-58. DIB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

2.7.4.1 DLAR Register (Offset = 0h) [Reset = 00000000h]

DLAR is shown in Table 2-59.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-59. DLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	KEY	R	0h	Indicates whether Non-secure invasive debug is allowed

2.7.4.2 DLSR Register (Offset = 4h) [Reset = 00000000h]

DLSR is shown in Table 2-60.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-60. DLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	08EE0540h	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
2	nTT	R	1h	Indicates whether Secure invasive debug is implemented and allowed
1	SLK	R	0h	Indicates whether Non-secure non-invasive debug is allowed
0	SLI	R	0h	Indicates whether Non-secure invasive debug is allowed

2.7.4.3 DAUTHSTATUS Register (Offset = 8h) [Reset = 00000000h]

DAUTHSTATUS is shown in Table 2-61.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-61. DAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	047702A0h	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
3	SNID	R	0h	Indicates whether Secure non-invasive debug is implemented and allowed
2	SID	R	1h	Indicates whether Secure invasive debug is implemented and allowed
1	NSNID	R	0h	Indicates whether Non-secure non-invasive debug is allowed
0	NSID	R	0h	Indicates whether Non-secure invasive debug is allowed

2.7.4.4 DDEVARCH Register (Offset = Ch) [Reset = 00000000h]

DDEVARCH is shown in Table 2-62.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-62. DDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	ARCHITECT	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	PRESENT	R	1h	Defines that the DEVARCH register is present
19-16	REVISION	R	0h	Defines the architecture revision of the component
15-12	ARCHVER	R	2h	Defines the architecture version of the component
11-0	ARCHPART	R	A04h	Defines the architecture of the component

2.7.4.5 DDEVTYPE Register (Offset = 1Ch) [Reset = 00000000h]

DDEVTYPE is shown in Table 2-63.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-63. DDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SUB	R	0h	Component sub-type
3-0	MAJOR	R	0h	CoreSight major type

2.7.4.6 DPIDR4 Register (Offset = 20h) [Reset = 00000000h]

DPIDR4 is shown in Table 2-64.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-64. DPIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SIZE	R	0h	See CoreSight Architecture Specification
3-0	DES_2	R	4h	See CoreSight Architecture Specification

2.7.4.7 DPIDR5 Register (Offset = 24h) [Reset = 00000000h]

DPIDR5 is shown in Table 2-65.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-65. DPIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.4.8 DPIDR6 Register (Offset = 28h) [Reset = 00000000h]

DPIDR6 is shown in Table 2-66.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-66. DPIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.4.9 DPIDR7 Register (Offset = 2Ch) [Reset = 00000000h]

DPIDR7 is shown in Table 2-67.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-67. DPIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.4.10 DPIDR0 Register (Offset = 30h) [Reset = 00000000h]

DPIDR0 is shown in Table 2-68.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-68. DPIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PART_0	R	21h	See CoreSight Architecture Specification

2.7.4.11 DPIDR1 Register (Offset = 34h) [Reset = 00000000h]

DPIDR1 is shown in Table 2-69.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-69. DPIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	DES_0	R	Bh	See CoreSight Architecture Specification
3-0	PART_1	R	Dh	See CoreSight Architecture Specification

2.7.4.12 DPIDR2 Register (Offset = 38h) [Reset = 00000000h]

DPIDR2 is shown in Table 2-70.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-70. DPIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVISION	R	0h	See CoreSight Architecture Specification
3	JEDEC	R	1h	See CoreSight Architecture Specification
2-0	DES_1	R	3h	See CoreSight Architecture Specification

2.7.4.13 DPIDR3 Register (Offset = 3Ch) [Reset = 00000000h]

DPIDR3 is shown in Table 2-71.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-71. DPIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVAND	R	0h	See CoreSight Architecture Specification
3-0	CMOD	R	0h	See CoreSight Architecture Specification

2.7.4.14 DCIDR0 Register (Offset = 40h) [Reset = 00000000h]

DCIDR0 is shown in Table 2-72.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-72. DCIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_0	R	Dh	See CoreSight Architecture Specification

2.7.4.15 DCIDR1 Register (Offset = 44h) [Reset = 00000000h]

DCIDR1 is shown in Table 2-73.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-73. DCIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	CLASS	R	9h	See CoreSight Architecture Specification
3-0	PRMBL_1	R	0h	See CoreSight Architecture Specification

2.7.4.16 DCIDR2 Register (Offset = 48h) [Reset = 00000000h]

DCIDR2 is shown in Table 2-74.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-74. DCIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_2	R	5h	See CoreSight Architecture Specification

2.7.4.17 DCIDR3 Register (Offset = 4Ch) [Reset = 00000000h]

DCIDR3 is shown in Table 2-75.

Return to the Summary Table.

Provides CoreSight discovery information for the SCS

Table 2-75. DCIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_3	R	B1h	See CoreSight Architecture Specification

2.7.5 DWT Registers

Table 2-76 lists the memory-mapped registers for the DWT registers. All register offset addresses not listed in Table 2-76 should be considered as reserved locations and the register contents should not be modified.

Table 2-76. DWT Registers

Offset	Acronym	Register Name	Section
0h	DWT Control Register	Provides configuration and status information for the DWT unit, and used to control features of the unit	Section 2.7.5.1
4h	DWT Cycle Count Register	Shows or sets the value of the processor cycle counter, CYCCNT	Section 2.7.5.2
8h	DWT CPI Count Register	Counts additional cycles required to execute multicycle instructions and instruction fetch stalls.	Section 2.7.5.3
Ch	DWT Exception Overhead Count Register	Counts the total cycles spent in exception processing	Section 2.7.5.4
10h	DWT Sleep Count Register	Counts the total number of cycles that the processor is sleeping.	Section 2.7.5.5
14h	DWT LSU Count Register	Increments on the additional cycles required to execute all load or store instructions	Section 2.7.5.6
18h	DWT Folded Instruction Count Register	Increments on the additional cycles required to execute all load or store instructions	Section 2.7.5.7
1Ch	DWT Program Counter Sample Register	Samples the current value of the Program Counter.	Section 2.7.5.8
20h	DWT Comparator Register 0	Provides a reference value for use by watchpoint comparator 0	Section 2.7.5.9
28h	DWT Comparator Function Register 0	Controls the operation of watchpoint comparator 0	Section 2.7.5.10
30h	DWT Comparator Register 1	Provides a reference value for use by watchpoint comparator 1	Section 2.7.5.11
38h	DWT Comparator Function Register 1	Controls the operation of watchpoint comparator 1	Section 2.7.5.12
40h	DWT Comparator Register 2	Provides a reference value for use by watchpoint comparator 2	Section 2.7.5.13
48h	DWT Comparator Function Register 2	Controls the operation of watchpoint comparator 2	Section 2.7.5.14
50h	DWT Comparator Register 3	Provides a reference value for use by watchpoint comparator 3	Section 2.7.5.15
58h	DWT Comparator Function Register 3	Controls the operation of watchpoint comparator 3	Section 2.7.5.16
FBCh	DWT Device Architecture Register	Provides CoreSight discovery information for the DWT	Section 2.7.5.17
FCCh	DWT Device Type Register	Provides CoreSight discovery information for the DWT	Section 2.7.5.18
FD0h	DWT Peripheral Identification Register 4	Provides CoreSight discovery information for the DWT	Section 2.7.5.19
FD4h	DWT Peripheral Identification Register 5	Provides CoreSight discovery information for the DWT	Section 2.7.5.20
FD8h	DWT Peripheral Identification Register 6	Provides CoreSight discovery information for the DWT	Section 2.7.5.21
FDCh	DWT Peripheral Identification Register 7	Provides CoreSight discovery information for the DWT	Section 2.7.5.22
FE0h	DWT Peripheral Identification Register 0	Provides CoreSight discovery information for the DWT	Section 2.7.5.23
FE4h	DWT Peripheral Identification Register 1	Provides CoreSight discovery information for the DWT	Section 2.7.5.24
FE8h	DWT Peripheral Identification Register 2	Provides CoreSight discovery information for the DWT	Section 2.7.5.25
FECh	DWT Peripheral Identification Register 3	Provides CoreSight discovery information for the DWT	Section 2.7.5.26
FF0h	DWT Component Identification Register 0	Provides CoreSight discovery information for the DWT	Section 2.7.5.27
FF4h	DWT Component Identification Register 1	Provides CoreSight discovery information for the DWT	Section 2.7.5.28
FF8h	DWT Component Identification Register 2	Provides CoreSight discovery information for the DWT	Section 2.7.5.29
FFCh	DWT Component Identification Register 3	Provides CoreSight discovery information for the DWT	Section 2.7.5.30

Complex bit access types are encoded to fit into small table cells. Table 2-77 shows the codes that are used for access types in this section.

Table 2-77. DWT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.5.1 DWT Control Register (Offset = 0h) [Reset = 02000000h]

DWT Control Register is shown in Table 2-78.

Return to the Summary Table.

Provides configuration and status information for the DWT unit, and used to control features of the unit

Table 2-78. DWT Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Number of comparators	R	0h	Number of DWT comparators implemented
27	No trace packets	R	0h	Indicates whether the implementation does not support trace
26	RESERVED	R	0h	Reserved, RAZ
25	No cycle count	R	1h	Indicates whether the implementation does not include a cycle counter
24	No profile counters	R	0h	Indicates whether the implementation does not include the profiling counters
23	Cycle counter disabled secure	R/W	0h	Controls whether the cycle counter is disabled in Secure state
22	Cycle event enable	R/W	0h	Enables Event Counter packet generation on POSTCNT underflow
21	Fold event enable	R/W	0h	Enables DWT_FOLDCNT counter
20	LSU event enable	R/W	0h	Enables DWT_LSUCNT counter
19	Sleep event enable	R/W	0h	Enable DWT_SLEEPCNT counter
18	Exception event enable	R/W	0h	Enables DWT_EXCCNT counter
17	CPI event enable	R/W	0h	Enables DWT_CPICNT counter
16	Exception trace enable	R/W	0h	Enables generation of Exception Trace packets
15-13	RESERVED	R	0h	Reserved, RES0
12	PC sample enable	R/W	0h	Enables use of POSTCNT counter as a timer for Periodic PC Sample packet generation
11-10	Synchronization tap	R/W	0h	Selects the position of the synchronization packet counter tap on the CYCCNT counter. This determines the Synchronization packet rate
9	Cycle count tap	R/W	0h	Selects the position of the POSTCNT tap on the CYCCNT counter
8-5	POSTCNT initial	R/W	0h	Initial value for the POSTCNT counter
4-1	POSTCNT preset	R/W	0h	Reload value for the POSTCNT counter
0	CYCCNT enable	R/W	0h	Enables CYCCNT

2.7.5.2 DWT Cycle Count Register (Offset = 4h) [Reset = 00000000h]

DWT Cycle Count Register is shown in Table 2-79.

Return to the Summary Table.

Shows or sets the value of the processor cycle counter, CYCCNT

Table 2-79. DWT Cycle Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Incrementing cycle counter value	R/W	0h	Increments one on each processor clock cycle when DWT_CTRL.CYCCNTENA == 1 and DEMCR.TRCENA == 1. On overflow, CYCCNT wraps to zero

2.7.5.3 DWT CPI Count Register (Offset = 8h) [Reset = 00000000h]

DWT CPI Count Register is shown in Table 2-80.

Return to the Summary Table.

Counts additional cycles required to execute multicycle instructions and instruction fetch stalls.

Table 2-80. DWT CPI Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Base instruction overhead counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.CPIEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed. - No load-store operation is in progress, see DWT_LSUCNT. - No exception-entry or exception-exit operation is in progress, see DWT_EXCCNT. - The PE is not in a power saving mode, see DWT_SLEEPCNT. - Either SecureNoninvasiveDebugAllowed() == TRUE, or the PE is in Non-secure state and NoninvasiveDebugAllowed() == TRUE.

2.7.5.4 DWT Exception Overhead Count Register (Offset = Ch) [Reset = 00000000h]

DWT Exception Overhead Count Register is shown in Table 2-81.

Return to the Summary Table.

Counts the total cycles spent in exception processing

Table 2-81. DWT Exception Overhead Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	The exception overhead counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.EXCEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed, see DWT_CPICNT. - An exception-entry or exception-exit related operation is in progress. - Either SecureNoninvasiveDebugAllowed() == TRUE, or NS-Req for the operation is set to Non-secure and NoninvasiveDebugAllowed() == TRUE.

2.7.5.5 DWT Sleep Count Register (Offset = 10h) [Reset = 00000000h]

DWT Sleep Count Register is shown in Table 2-82.

Return to the Summary Table.

Counts the total number of cycles that the processor is sleeping.

Table 2-82. DWT Sleep Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Sleep counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.SLEEPEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed, see DWT_CPICNT. - No load-store operation is in progress, see DWT_LSUCNT. - No exception-entry or exception-exit operation is in progress, see DWT_EXCCNT. - The PE is in a power saving mode. - Either SecureNoninvasiveDebugAllowed() == TRUE, or the PE is in Non-secure state and NoninvasiveDebugAllowed() == TRUE.

2.7.5.6 DWT LSU Count Register (Offset = 14h) [Reset = 00000000h]

DWT LSU Count Register is shown in Table 2-83.

Return to the Summary Table.

Increments on the additional cycles required to execute all load or store instructions

Table 2-83. DWT LSU Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Load-store overhead counter	R/W	0h	Counts one on each cycle when all of the following are true: - DWT_CTRL.LSUEVTENA == 1 and DEMCR.TRCENA == 1. - No instruction is executed, see DWT_CPICNT. - No exception-entry or exception-exit operation is in progress, see DWT_EXCCNT. - A load-store operation is in progress. - Either SecureNoninvasiveDebugAllowed() == TRUE, or NS-Req for the operation is set to Non-secure and NoninvasiveDebugAllowed() == TRUE.

2.7.5.7 DWT Folded Instruction Count Register (Offset = 18h) [Reset = 00000000h]

DWT Folded Instruction Count Register is shown in Table 2-84.

Return to the Summary Table.

Increments on the additional cycles required to execute all load or store instructions

Table 2-84. DWT Folded Instruction Count Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Folded instruction counter	R/W	0h	Counts on each cycle when all of the following are true: - DWT_CTRL.FOLDEVTENA == 1 and DEMCR.TRCENA == 1. - At least two instructions are executed, see DWT_CPICNT. - Either SecureNoninvasiveDebugAllowed() == TRUE, or the PE is in Non-secure state and NoninvasiveDebugAllowed() == TRUE. The counter is incremented by the number of instructions executed, minus one

2.7.5.8 DWT Program Counter Sample Register (Offset = 1Ch) [Reset = 00000000h]

DWT Program Counter Sample Register is shown in Table 2-85.

Return to the Summary Table.

Samples the current value of the Program Counter.

Table 2-85. DWT Program Counter Sample Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Executed instruction address sample. Recently executed instruction address sample value	R	0h	The possible values of this field are: 0xFFFFFFFF One of the following is true: - The PE is halted in Debug state. - The Security Extension is implemented, the sampled instruction was executed in Secure state, and SecureNoninvasiveDebugAllowed() == FALSE. - NoninvasiveDebugAllowed() == FALSE. - DEMCR.TRCENA == 0. - The address of a recently-executed instruction is not available. Not 0xFFFFFFFF Instruction address of a recently executed instruction. Bit [0] of the sample instruction address is 0.

2.7.5.9 DWT Comparator Register 0 (Offset = 20h) [Reset = 00000000h]

DWT Comparator Register 0 is shown in Table 2-86.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 0

Table 2-86. DWT Comparator Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

2.7.5.10 DWT Comparator Function Register 0 (Offset = 28h) [Reset = 58000000h]

DWT Comparator Function Register 0 is shown in Table 2-87.

Return to the Summary Table.

Controls the operation of watchpoint comparator 0

Table 2-87. DWT Comparator Function Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	Bh	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

2.7.5.11 DWT Comparator Register 1 (Offset = 30h) [Reset = 00000000h]

DWT Comparator Register 1 is shown in Table 2-88.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 1

Table 2-88. DWT Comparator Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

2.7.5.12 DWT Comparator Function Register 1 (Offset = 38h) [Reset = D0000000h]

DWT Comparator Function Register 1 is shown in Table 2-89.

Return to the Summary Table.

Controls the operation of watchpoint comparator 1

Table 2-89. DWT Comparator Function Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	1Ah	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

2.7.5.13 DWT Comparator Register 2 (Offset = 40h) [Reset = 00000000h]

DWT Comparator Register 2 is shown in Table 2-90.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 2

Table 2-90. DWT Comparator Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

2.7.5.14 DWT Comparator Function Register 2 (Offset = 48h) [Reset = 50000000h]

DWT Comparator Function Register 2 is shown in Table 2-91.

Return to the Summary Table.

Controls the operation of watchpoint comparator 2

Table 2-91. DWT Comparator Function Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	Ah	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

2.7.5.15 DWT Comparator Register 3 (Offset = 50h) [Reset = 00000000h]

DWT Comparator Register 3 is shown in Table 2-92.

Return to the Summary Table.

Provides a reference value for use by watchpoint comparator 3

Table 2-92. DWT Comparator Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Cycle, PC, address or data value	R/W	0h	Reference value for comparison. Behaviour depends on the value of DWT_FUNCTIONn.MATCH

2.7.5.16 DWT Comparator Function Register 3 (Offset = 58h) [Reset = 50000000h]

DWT Comparator Function Register 3 is shown in Table 2-93.

Return to the Summary Table.

Controls the operation of watchpoint comparator 3

Table 2-93. DWT Comparator Function Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Identify capability	R	Ah	Identifies the capabilities for MATCH for comparator *n
26-25	RESERVED	R	0h	Reserved, RES0
24	Comparator matched	RC	0h	Set to 1 when the comparator matches
23-12	RESERVED	R	0h	Reserved, RES0
11-10	Data value size	R/W	0h	Defines the size of the object being watched for by Data Value and Data Address comparators
9-6	RESERVED	R	0h	Reserved, RES0
5-4	Action on match	R/W	0h	Defines the action on a match. This field is ignored and the comparator generates no actions if it is disabled by MATCH
3-0	Match type	R/W	0h	Controls the type of match generated by this comparator

2.7.5.17 DWT Device Architecture Register (Offset = FBCh) [Reset = 47701A02h]

DWT Device Architecture Register is shown in Table 2-94.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-94. DWT Device Architecture Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	Architect	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	DEVARCH Present	R	1h	Defines that the DEVARCH register is present
19-16	Revision	R	0h	Defines the architecture revision of the component
15-12	Architecture Version	R	1h	Defines the architecture version of the component
11-0	Architecture Part	R	A02h	Defines the architecture of the component

2.7.5.18 DWT Device Type Register (Offset = FCCh) [Reset = 00000000h]

DWT Device Type Register is shown in Table 2-95.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-95. DWT Device Type Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Sub-type	R	0h	Component sub-type
3-0	Major type	R	0h	Component major type

2.7.5.19 DWT Peripheral Identification Register 4 (Offset = FD0h) [Reset = 00000004h]

DWT Peripheral Identification Register 4 is shown in Table 2-96.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-96. DWT Peripheral Identification Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	4KB count	R	0h	See CoreSight Architecture Specification
3-0	JEP106 continuation code	R	4h	See CoreSight Architecture Specification

2.7.5.20 DWT Peripheral Identification Register 5 (Offset = FD4h) [Reset = 00000000h]

DWT Peripheral Identification Register 5 is shown in Table 2-97.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-97. DWT Peripheral Identification Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

2.7.5.21 DWT Peripheral Identification Register 6 (Offset = FD8h) [Reset = 00000000h]

DWT Peripheral Identification Register 6 is shown in Table 2-98.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-98. DWT Peripheral Identification Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

2.7.5.22 DWT Peripheral Identification Register 7 (Offset = FDCh) [Reset = 00000000h]

DWT Peripheral Identification Register 7 is shown in Table 2-99.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-99. DWT Peripheral Identification Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

2.7.5.23 DWT Peripheral Identification Register 0 (Offset = FE0h) [Reset = 00000021h]

DWT Peripheral Identification Register 0 is shown in Table 2-100.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-100. DWT Peripheral Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Part number bits [7:0]	R	21h	See CoreSight Architecture Specification

2.7.5.24 DWT Peripheral Identification Register 1 (Offset = FE4h) [Reset = 000000BDh]

DWT Peripheral Identification Register 1 is shown in Table 2-101.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-101. DWT Peripheral Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	JEP106 identification code bits [3:0]	R	Bh	See CoreSight Architecture Specification
3-0	Part number bits [11:8]	R	Dh	See CoreSight Architecture Specification

2.7.5.25 DWT Peripheral Identification Register 2 (Offset = FE8h) [Reset = 0000000Bh]

DWT Peripheral Identification Register 2 is shown in Table 2-102.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-102. DWT Peripheral Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Component revision	R	0h	See CoreSight Architecture Specification
3	JEDEC assignee value is used	R	1h	See CoreSight Architecture Specification
2-0	JEP106 identification code bits [6:4]	R	3h	See CoreSight Architecture Specification

2.7.5.26 DWT Peripheral Identification Register 3 (Offset = FECh) [Reset = 00000000h]

DWT Peripheral Identification Register 3 is shown in Table 2-103.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-103. DWT Peripheral Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	RevAnd	R	0h	See CoreSight Architecture Specification
3-0	Customer Modified	R	0h	See CoreSight Architecture Specification

2.7.5.27 DWT Component Identification Register 0 (Offset = FF0h) [Reset = 0000000Dh]

DWT Component Identification Register 0 is shown in Table 2-104.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-104. DWT Component Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	Dh	See CoreSight Architecture Specification

2.7.5.28 DWT Component Identification Register 1 (Offset = FF4h) [Reset = 00000090h]

DWT Component Identification Register 1 is shown in Table 2-105.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-105. DWT Component Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	CoreSight component class	R	9h	See CoreSight Architecture Specification
3-0	CoreSight component identification preamble	R	0h	See CoreSight Architecture Specification

2.7.5.29 DWT Component Identification Register 2 (Offset = FF8h) [Reset = 00000005h]

DWT Component Identification Register 2 is shown in Table 2-106.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-106. DWT Component Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	5h	See CoreSight Architecture Specification

2.7.5.30 DWT Component Identification Register 3 (Offset = FFCh) [Reset = 000000B1h]

DWT Component Identification Register 3 is shown in Table 2-107.

Return to the Summary Table.

Provides CoreSight discovery information for the DWT

Table 2-107. DWT Component Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	B1h	See CoreSight Architecture Specification

2.7.6 FPB Registers

Table 2-108 lists the memory-mapped registers for the FPB registers. All register offset addresses not listed in Table 2-108 should be considered as reserved locations and the register contents should not be modified.

Table 2-108. FPB Registers

Offset	Acronym	Register Name	Section
0h	FP_CTRL	Provides FPB implementation information, and the global enable for the FPB unit	Section 2.7.6.1
4h	FP_REMAP	Indicates whether the implementation supports Flash Patch remap and, if it does, holds the target address for remap	Section 2.7.6.2
8h	FP_COMP0	Holds an address for comparison.	Section 2.7.6.3
Ch	FP_COMP1	Holds an address for comparison.	Section 2.7.6.4
10h	FP_COMP2	Holds an address for comparison.	Section 2.7.6.5
14h	FP_COMP3	Holds an address for comparison.	Section 2.7.6.6
18h	FP_COMP4	Holds an address for comparison.	Section 2.7.6.7
1Ch	FP_COMP5	Holds an address for comparison.	Section 2.7.6.8
20h	FP_COMP6	Holds an address for comparison.	Section 2.7.6.9
24h	FP_COMP7	Holds an address for comparison.	Section 2.7.6.10
FBCh	FP_DEVARCH	Provides CoreSight discovery information for the FPB	Section 2.7.6.11
FCCh	FP_DEVTYPE	Provides CoreSight discovery information for the FPB	Section 2.7.6.12
FD0h	FP_PIDR4	Provides CoreSight discovery information for the FP	Section 2.7.6.13
FD4h	FP_PIDR5	Provides CoreSight discovery information for the FP	Section 2.7.6.14
FD8h	FP_PIDR6	Provides CoreSight discovery information for the FP	Section 2.7.6.15
FDCh	FP_PIDR7	Provides CoreSight discovery information for the FP	Section 2.7.6.16
FE0h	FP_PIDR0	Provides CoreSight discovery information for the FP	Section 2.7.6.17
FE4h	FP_PIDR1	Provides CoreSight discovery information for the FP	Section 2.7.6.18
FE8h	FP_PIDR2	Provides CoreSight discovery information for the FP	Section 2.7.6.19
FECh	FP_PIDR3	Provides CoreSight discovery information for the FP	Section 2.7.6.20
FF0h	FP_CIDR0	Provides CoreSight discovery information for the FP	Section 2.7.6.21
FF4h	FP_CIDR1	Provides CoreSight discovery information for the FP	Section 2.7.6.22
FF8h	FP_CIDR2	Provides CoreSight discovery information for the FP	Section 2.7.6.23
FFCh	FP_CIDR3	Provides CoreSight discovery information for the FP	Section 2.7.6.24

Complex bit access types are encoded to fit into small table cells. Table 2-109 shows the codes that are used for access types in this section.

Table 2-109. FPB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.6.1 FP_CTRL Register (Offset = 0h) [Reset = 00000000h]

FP_CTRL is shown in Table 2-110.

Return to the Summary Table.

Provides FPB implementation information, and the global enable for the FPB unit

Table 2-110. FP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REV	R	1h	Flash Patch and Breakpoint Unit architecture revision
27-15	RES0	R	0h	Reserved, RES0
14-12	NUM_CODE_14_12_	R	0h	Indicates the number of implemented instruction address comparators. Zero indicates no Instruction Address comparators are implemented. The Instruction Address comparators are numbered from 0 to NUM_CODE - 1
11-8	NUM_LIT	R	0h	Indicates the number of implemented literal address comparators. The Literal Address comparators are numbered from NUM_CODE to NUM_CODE + NUM_LIT - 1
7-4	NUM_CODE_7_4_	R	8h	Indicates the number of implemented instruction address comparators. Zero indicates no Instruction Address comparators are implemented. The Instruction Address comparators are numbered from 0 to NUM_CODE - 1
3-2	RES0_1	R	0h	Reserved, RES0
1	KEY	R/W	0h	Writes to the FP_CTRL are ignored unless KEY is concurrently written to one
0	ENABLE	R/W	0h	Enables the FPB

2.7.6.2 FP_REMAP Register (Offset = 4h) [Reset = 00000000h]

FP_REMAP is shown in Table 2-111.

Return to the Summary Table.

Indicates whether the implementation supports Flash Patch remap and, if it does, holds the target address for remap

Table 2-111. FP_REMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RES0	R	0h	Reserved, RES0
29	RMPSPT	R	0h	Indicates whether the FPB unit supports the Flash Patch remap function
28-5	REMAP	R	Xh	Holds the bits[28:5] of the Flash Patch remap address
4-0	RES0_1	R	0h	Reserved, RES0

2.7.6.3 FP_COMP0 Register (Offset = 8h) [Reset = 00000000h]

FP_COMP0 is shown in Table 2-112.

Return to the Summary Table.

Holds an address for comparison.

Table 2-112. FP_COMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.4 FP_COMP1 Register (Offset = Ch) [Reset = 00000000h]

FP_COMP1 is shown in Table 2-113.

Return to the Summary Table.

Holds an address for comparison.

Table 2-113. FP_COMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.5 FP_COMP2 Register (Offset = 10h) [Reset = 00000000h]

FP_COMP2 is shown in Table 2-114.

Return to the Summary Table.

Holds an address for comparison.

Table 2-114. FP_COMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.6 FP_COMP3 Register (Offset = 14h) [Reset = 00000000h]

FP_COMP3 is shown in Table 2-115.

Return to the Summary Table.

Holds an address for comparison.

Table 2-115. FP_COMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.7 FP_COMP4 Register (Offset = 18h) [Reset = 00000000h]

FP_COMP4 is shown in Table 2-116.

Return to the Summary Table.

Holds an address for comparison.

Table 2-116. FP_COMP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.8 FP_COMP5 Register (Offset = 1Ch) [Reset = 00000000h]

FP_COMP5 is shown in Table 2-117.

Return to the Summary Table.

Holds an address for comparison.

Table 2-117. FP_COMP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.9 FP_COMP6 Register (Offset = 20h) [Reset = 00000000h]

FP_COMP6 is shown in Table 2-118.

Return to the Summary Table.

Holds an address for comparison.

Table 2-118. FP_COMP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.10 FP_COMP7 Register (Offset = 24h) [Reset = 00000000h]

FP_COMP7 is shown in Table 2-119.

Return to the Summary Table.

Holds an address for comparison.

Table 2-119. FP_COMP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	BPADDR	R/W	0h	Specifies bits[31:1] of the breakpoint instruction address
0	BE	R/W	0h	Selects between remapping and breakpoint functionality

2.7.6.11 FP_DEVARCH Register (Offset = FBCh) [Reset = 00000000h]

FP_DEVARCH is shown in Table 2-120.

Return to the Summary Table.

Provides CoreSight discovery information for the FPB

Table 2-120. FP_DEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	ARCHITECT	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	PRESENT	R	1h	Defines that the DEVARCH register is present
19-16	REVISION	R	0h	Defines the architecture revision of the component
15-12	ARCHVER	R	1h	Defines the architecture version of the component
11-0	ARCHPART	R	A03h	Defines the architecture of the component

2.7.6.12 FP_DEVTYPE Register (Offset = FCCh) [Reset = 00000000h]

FP_DEVTYPE is shown in Table 2-121.

Return to the Summary Table.

Provides CoreSight discovery information for the FPB

Table 2-121. FP_DEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SUB	R	0h	Component sub-type
3-0	MAJOR	R	0h	Component major type

2.7.6.13 FP_PIDR4 Register (Offset = FD0h) [Reset = 00000000h]

FP_PIDR4 is shown in Table 2-122.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-122. FP_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	SIZE	R	0h	See CoreSight Architecture Specification
3-0	DES_2	R	4h	See CoreSight Architecture Specification

2.7.6.14 FP_PIDR5 Register (Offset = FD4h) [Reset = 00000000h]

FP_PIDR5 is shown in Table 2-123.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-123. FP_PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.6.15 FP_PIDR6 Register (Offset = FD8h) [Reset = 00000000h]

FP_PIDR6 is shown in Table 2-124.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-124. FP_PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.6.16 FP_PIDR7 Register (Offset = FDCh) [Reset = 00000000h]

FP_PIDR7 is shown in Table 2-125.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-125. FP_PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.6.17 FP_PIDR0 Register (Offset = FE0h) [Reset = 00000000h]

FP_PIDR0 is shown in Table 2-126.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-126. FP_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PART_0	R	21h	See CoreSight Architecture Specification

2.7.6.18 FP_PIDR1 Register (Offset = FE4h) [Reset = 00000000h]

FP_PIDR1 is shown in Table 2-127.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-127. FP_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	DES_0	R	Bh	See CoreSight Architecture Specification
3-0	PART_1	R	Dh	See CoreSight Architecture Specification

2.7.6.19 FP_PIDR2 Register (Offset = FE8h) [Reset = 00000000h]

FP_PIDR2 is shown in Table 2-128.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-128. FP_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVISION	R	0h	See CoreSight Architecture Specification
3	JEDEC	R	1h	See CoreSight Architecture Specification
2-0	DES_1	R	3h	See CoreSight Architecture Specification

2.7.6.20 FP_PIDR3 Register (Offset = FECh) [Reset = 00000000h]

FP_PIDR3 is shown in Table 2-129.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-129. FP_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	REVAND	R	0h	See CoreSight Architecture Specification
3-0	CMOD	R	0h	See CoreSight Architecture Specification

2.7.6.21 FP_CIDR0 Register (Offset = FF0h) [Reset = 00000000h]

FP_CIDR0 is shown in Table 2-130.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-130. FP_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_0	R	Dh	See CoreSight Architecture Specification

2.7.6.22 FP_CIDR1 Register (Offset = FF4h) [Reset = 00000000h]

FP_CIDR1 is shown in Table 2-131.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-131. FP_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	CLASS	R	9h	See CoreSight Architecture Specification
3-0	PRMBL_1	R	0h	See CoreSight Architecture Specification

2.7.6.23 FP_CIDR2 Register (Offset = FF8h) [Reset = 00000000h]

FP_CIDR2 is shown in Table 2-132.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-132. FP_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_2	R	5h	See CoreSight Architecture Specification

2.7.6.24 FP_CIDR3 Register (Offset = FFCh) [Reset = 00000000h]

FP_CIDR3 is shown in Table 2-133.

Return to the Summary Table.

Provides CoreSight discovery information for the FP

Table 2-133. FP_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	PRMBL_3	R	B1h	See CoreSight Architecture Specification

2.7.7 FPE Registers

Table 2-134 lists the memory-mapped registers for the FPE registers. All register offset addresses not listed in Table 2-134 should be considered as reserved locations and the register contents should not be modified.

Table 2-134. FPE Registers

Offset	Acronym	Register Name	Section
4h	FPCCR	Holds control data for the Floating-point extension	Section 2.7.7.1
8h	FPCAR	Holds the location of the unpopulated floating-point register space allocated on an exception stack frame	Section 2.7.7.2
Ch	FPDSCR	Holds the default values for the floating-point status control data that the PE assigns to the FPSCR when it creates a new floating-point context	Section 2.7.7.3
10h	MVFR0	Describes the features provided by the Floating-point Extension	Section 2.7.7.4
14h	MVFR1	Describes the features provided by the Floating-point Extension	Section 2.7.7.5
18h	MVFR2	Describes the features provided by the Floating-point Extension	Section 2.7.7.6

Complex bit access types are encoded to fit into small table cells. Table 2-135 shows the codes that are used for access types in this section.

Table 2-135. FPE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.7.1 FPCCR Register (Offset = 4h) [Reset = 00000000h]

FPCCR is shown in Table 2-136.

Return to the Summary Table.

Holds control data for the Floating-point extension

Table 2-136. FPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ASPEN	R/W	1h	When this bit is set to 1, execution of a floating-point instruction sets the CONTROL.FPCA bit to 1
30	LSPEN	R/W	1h	Enables lazy context save of floating-point state
29	LSPENS	R/W	0h	This bit controls whether the LSPEN bit is writeable from the Non-secure state
28	CLRONRET	R/W	0h	Clear floating-point caller saved registers on exception return
27	CLRONRETS	R/W	0h	This bit controls whether the CLRONRET bit is writeable from the Non-secure state
26	TS	R/W	0h	Treat floating-point registers as Secure enable
25-11	RES0	R	0h	Reserved, RES0
10	UFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the UsageFault exception to pending
9	SPLIMVIOL	R/W	0h	This bit is banked between the Security states and indicates whether the floating-point context violates the stack pointer limit that was active when lazy state preservation was activated. SPLIMVIOL modifies the lazy floating-point state preservation behavior
8	MONRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the DebugMonitor exception to pending
7	SFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the SecureFault exception to pending. This bit is only present in the Secure version of the register, and behaves as RAZ/WI when accessed from the Non-secure state
6	BFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the BusFault exception to pending
5	MMRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the MemManage exception to pending
4	HFRDY	R/W	0h	Indicates whether the software executing when the PE allocated the floating-point stack frame was able to set the HardFault exception to pending
3	THREAD	R/W	0h	Indicates the PE mode when it allocated the floating-point stack frame
2	S	R/W	0h	Security status of the floating-point context. This bit is only present in the Secure version of the register, and behaves as RAZ/WI when accessed from the Non-secure state. This bit is updated whenever lazy state preservation is activated, or when a floating-point instruction is executed
1	USER	R/W	0h	Indicates the privilege level of the software executing when the PE allocated the floating-point stack frame
0	LSPACT	R/W	0h	Indicates whether lazy preservation of the floating-point state is active

2.7.7.2 FPCAR Register (Offset = 8h) [Reset = 00000000h]

FPCAR is shown in Table 2-137.

Return to the Summary Table.

Holds the location of the unpopulated floating-point register space allocated on an exception stack frame

Table 2-137. FPCAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	ADDRESS	R/W	0h	The location of the unpopulated floating-point register space allocated on an exception stack frame
2-0	RES0	R	0h	Reserved, RES0

2.7.7.3 FPDSCR Register (Offset = Ch) [Reset = 00000000h]

FPDSCR is shown in Table 2-138.

Return to the Summary Table.

Holds the default values for the floating-point status control data that the PE assigns to the FPSCR when it creates a new floating-point context

Table 2-138. FPDSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RES0	R	0h	Reserved, RES0
26	AHP	R/W	0h	Default value for FPSCR.AHP
25	DN	R/W	0h	Default value for FPSCR.DN
24	FZ	R/W	0h	Default value for FPSCR.FZ
23-22	RMode	R/W	0h	Default value for FPSCR.RMode
21-0	RES0_1	R	Xh	Reserved, RES0

2.7.7.4 MVFR0 Register (Offset = 10h) [Reset = 00000000h]

MVFR0 is shown in Table 2-139.

Return to the Summary Table.

Describes the features provided by the Floating-point Extension

Table 2-139. MVFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	FPRound	R	1h	Indicates the rounding modes supported by the FP Extension
27-24	RES0	R	0h	Reserved, RES0
23-20	FPSqrt	R	1h	Indicates the support for FP square root operations
19-16	FPDivide	R	1h	Indicates the support for FP divide operations
15-12	RES0_1	R	0h	Reserved, RES0
11-8	FPDP	R	0h	Indicates support for FP double-precision operations
7-4	FPSP	R	2h	Indicates support for FP single-precision operations
3-0	SIMDReg	R	1h	Indicates size of FP register file

2.7.7.5 MVFR1 Register (Offset = 14h) [Reset = 00000000h]

MVFR1 is shown in Table 2-140.

Return to the Summary Table.

Describes the features provided by the Floating-point Extension

Table 2-140. MVFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	FMAC	R	1h	Indicates whether the FP Extension implements the fused multiply accumulate instructions
27-24	FPHP	R	1h	Indicates whether the FP Extension implements half-precision FP conversion instructions
23-8	RES0	R	0h	Reserved, RES0
7-4	FPDNaN	R	1h	Indicates whether the FP hardware implementation supports NaN propagation
3-0	FPFtZ	R	1h	Indicates whether subnormals are always flushed-to-zero

2.7.7.6 MVFR2 Register (Offset = 18h) [Reset = 00000000h]

MVFR2 is shown in Table 2-141.

Return to the Summary Table.

Describes the features provided by the Floating-point Extension

Table 2-141. MVFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	FPMisc	R	4h	Indicates support for miscellaneous FP features
3-0	RES0_1	R	0h	Reserved, RES0

2.7.8 ICB Registers

Table 2-142 lists the memory-mapped registers for the ICB registers. All register offset addresses not listed in Table 2-142 should be considered as reserved locations and the register contents should not be modified.

Table 2-142. ICB Registers

Offset	Acronym	Register Name	Section
4h	ICTR	Provides information about the interrupt controller	Section 2.7.8.1
8h	ACTLR	Provides IMPLEMENTATION DEFINED configuration and control options	Section 2.7.8.2

Complex bit access types are encoded to fit into small table cells. Table 2-143 shows the codes that are used for access types in this section.

Table 2-143. ICB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.8.1 ICTR Register (Offset = 4h) [Reset = 00000000h]

ICTR is shown in Table 2-144.

Return to the Summary Table.

Provides information about the interrupt controller

Table 2-144. ICTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES0	R	Xh	Reserved, RES0
3-0	INTLINESNUM	R	0h	Indicates the number of the highest implemented register in each of the NVIC control register sets, or in the case of NVIC_IPR*n, 4×INTLINESNUM

2.7.8.2 ACTLR Register (Offset = 8h) [Reset = 00000000h]

ACTLR is shown in Table 2-145.

Return to the Summary Table.

Provides IMPLEMENTATION DEFINED configuration and control options

Table 2-145. ACTLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RES0	R	0h	Reserved, RES0
29	EXTEXCLALL	R/W	0h	External Exclusives Allowed with no MPU
28-14	RES0_1	R	0h	Reserved, RES0
13	SBIST	R/W	0h	Bit used internally by Software Test Library (STL)
12	DISITMATBFLUSH	R/W	0h	Disable ATB Flush
11	RES0_2	R	0h	Reserved, RES0
10	FPEXCODIS	R/W	0h	Disable FPU exception outputs
9	DISOOFP	R/W	0h	Disable out-of-order FP instruction completion
8-3	RES0_3	R	0h	Reserved, RES0
2	DISFOLD	R/W	0h	Disable dual-issue.
1	RES0_4	R	0h	Reserved, RES0
0	DISMCYCINT	R/W	0h	Disable dual-issue.

2.7.9 ITM Registers

Table 2-146 lists the memory-mapped registers for the ITM registers. All register offset addresses not listed in Table 2-146 should be considered as reserved locations and the register contents should not be modified.

Table 2-146. ITM Registers

Offset	Acronym	Register Name	Section
0h	ITM Stimulus Port Register 0	Provides the interface for generating Instrumentation packets	Section 2.7.9.1
4h	ITM Stimulus Port Register 1	Provides the interface for generating Instrumentation packets	Section 2.7.9.2
8h	ITM Stimulus Port Register 2	Provides the interface for generating Instrumentation packets	Section 2.7.9.3
Ch	ITM Stimulus Port Register 3	Provides the interface for generating Instrumentation packets	Section 2.7.9.4
10h	ITM Stimulus Port Register 4	Provides the interface for generating Instrumentation packets	Section 2.7.9.5
14h	ITM Stimulus Port Register 5	Provides the interface for generating Instrumentation packets	Section 2.7.9.6
18h	ITM Stimulus Port Register 6	Provides the interface for generating Instrumentation packets	Section 2.7.9.7
1Ch	ITM Stimulus Port Register 7	Provides the interface for generating Instrumentation packets	Section 2.7.9.8
20h	ITM Stimulus Port Register 8	Provides the interface for generating Instrumentation packets	Section 2.7.9.9
24h	ITM Stimulus Port Register 9	Provides the interface for generating Instrumentation packets	Section 2.7.9.10
28h	ITM Stimulus Port Register 10	Provides the interface for generating Instrumentation packets	Section 2.7.9.11
2Ch	ITM Stimulus Port Register 11	Provides the interface for generating Instrumentation packets	Section 2.7.9.12
30h	ITM Stimulus Port Register 12	Provides the interface for generating Instrumentation packets	Section 2.7.9.13
34h	ITM Stimulus Port Register 13	Provides the interface for generating Instrumentation packets	Section 2.7.9.14
38h	ITM Stimulus Port Register 14	Provides the interface for generating Instrumentation packets	Section 2.7.9.15
3Ch	ITM Stimulus Port Register 15	Provides the interface for generating Instrumentation packets	Section 2.7.9.16
40h	ITM Stimulus Port Register 16	Provides the interface for generating Instrumentation packets	Section 2.7.9.17
44h	ITM Stimulus Port Register 17	Provides the interface for generating Instrumentation packets	Section 2.7.9.18
48h	ITM Stimulus Port Register 18	Provides the interface for generating Instrumentation packets	Section 2.7.9.19
4Ch	ITM Stimulus Port Register 19	Provides the interface for generating Instrumentation packets	Section 2.7.9.20
50h	ITM Stimulus Port Register 20	Provides the interface for generating Instrumentation packets	Section 2.7.9.21
54h	ITM Stimulus Port Register 21	Provides the interface for generating Instrumentation packets	Section 2.7.9.22
58h	ITM Stimulus Port Register 22	Provides the interface for generating Instrumentation packets	Section 2.7.9.23
5Ch	ITM Stimulus Port Register 23	Provides the interface for generating Instrumentation packets	Section 2.7.9.24

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
60h	ITM Stimulus Port Register 24	Provides the interface for generating Instrumentation packets	Section 2.7.9.25
64h	ITM Stimulus Port Register 25	Provides the interface for generating Instrumentation packets	Section 2.7.9.26
68h	ITM Stimulus Port Register 26	Provides the interface for generating Instrumentation packets	Section 2.7.9.27
6Ch	ITM Stimulus Port Register 27	Provides the interface for generating Instrumentation packets	Section 2.7.9.28
70h	ITM Stimulus Port Register 28	Provides the interface for generating Instrumentation packets	Section 2.7.9.29
74h	ITM Stimulus Port Register 29	Provides the interface for generating Instrumentation packets	Section 2.7.9.30
78h	ITM Stimulus Port Register 30	Provides the interface for generating Instrumentation packets	Section 2.7.9.31
7Ch	ITM Stimulus Port Register 31	Provides the interface for generating Instrumentation packets	Section 2.7.9.32
80h	ITM Stimulus Port Register 32	Provides the interface for generating Instrumentation packets	Section 2.7.9.33
84h	ITM Stimulus Port Register 33	Provides the interface for generating Instrumentation packets	Section 2.7.9.34
88h	ITM Stimulus Port Register 34	Provides the interface for generating Instrumentation packets	Section 2.7.9.35
8Ch	ITM Stimulus Port Register 35	Provides the interface for generating Instrumentation packets	Section 2.7.9.36
90h	ITM Stimulus Port Register 36	Provides the interface for generating Instrumentation packets	Section 2.7.9.37
94h	ITM Stimulus Port Register 37	Provides the interface for generating Instrumentation packets	Section 2.7.9.38
98h	ITM Stimulus Port Register 38	Provides the interface for generating Instrumentation packets	Section 2.7.9.39
9Ch	ITM Stimulus Port Register 39	Provides the interface for generating Instrumentation packets	Section 2.7.9.40
A0h	ITM Stimulus Port Register 40	Provides the interface for generating Instrumentation packets	Section 2.7.9.41
A4h	ITM Stimulus Port Register 41	Provides the interface for generating Instrumentation packets	Section 2.7.9.42
A8h	ITM Stimulus Port Register 42	Provides the interface for generating Instrumentation packets	Section 2.7.9.43
ACh	ITM Stimulus Port Register 43	Provides the interface for generating Instrumentation packets	Section 2.7.9.44
B0h	ITM Stimulus Port Register 44	Provides the interface for generating Instrumentation packets	Section 2.7.9.45
B4h	ITM Stimulus Port Register 45	Provides the interface for generating Instrumentation packets	Section 2.7.9.46
B8h	ITM Stimulus Port Register 46	Provides the interface for generating Instrumentation packets	Section 2.7.9.47
BCh	ITM Stimulus Port Register 47	Provides the interface for generating Instrumentation packets	Section 2.7.9.48
C0h	ITM Stimulus Port Register 48	Provides the interface for generating Instrumentation packets	Section 2.7.9.49
C4h	ITM Stimulus Port Register 49	Provides the interface for generating Instrumentation packets	Section 2.7.9.50

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
C8h	ITM Stimulus Port Register 50	Provides the interface for generating Instrumentation packets	Section 2.7.9.51
CCh	ITM Stimulus Port Register 51	Provides the interface for generating Instrumentation packets	Section 2.7.9.52
D0h	ITM Stimulus Port Register 52	Provides the interface for generating Instrumentation packets	Section 2.7.9.53
D4h	ITM Stimulus Port Register 53	Provides the interface for generating Instrumentation packets	Section 2.7.9.54
D8h	ITM Stimulus Port Register 54	Provides the interface for generating Instrumentation packets	Section 2.7.9.55
DCh	ITM Stimulus Port Register 55	Provides the interface for generating Instrumentation packets	Section 2.7.9.56
E0h	ITM Stimulus Port Register 56	Provides the interface for generating Instrumentation packets	Section 2.7.9.57
E4h	ITM Stimulus Port Register 57	Provides the interface for generating Instrumentation packets	Section 2.7.9.58
E8h	ITM Stimulus Port Register 58	Provides the interface for generating Instrumentation packets	Section 2.7.9.59
ECh	ITM Stimulus Port Register 59	Provides the interface for generating Instrumentation packets	Section 2.7.9.60
F0h	ITM Stimulus Port Register 60	Provides the interface for generating Instrumentation packets	Section 2.7.9.61
F4h	ITM Stimulus Port Register 61	Provides the interface for generating Instrumentation packets	Section 2.7.9.62
F8h	ITM Stimulus Port Register 62	Provides the interface for generating Instrumentation packets	Section 2.7.9.63
FCh	ITM Stimulus Port Register 63	Provides the interface for generating Instrumentation packets	Section 2.7.9.64
100h	ITM Stimulus Port Register 64	Provides the interface for generating Instrumentation packets	Section 2.7.9.65
104h	ITM Stimulus Port Register 65	Provides the interface for generating Instrumentation packets	Section 2.7.9.66
108h	ITM Stimulus Port Register 66	Provides the interface for generating Instrumentation packets	Section 2.7.9.67
10Ch	ITM Stimulus Port Register 67	Provides the interface for generating Instrumentation packets	Section 2.7.9.68
110h	ITM Stimulus Port Register 68	Provides the interface for generating Instrumentation packets	Section 2.7.9.69
114h	ITM Stimulus Port Register 69	Provides the interface for generating Instrumentation packets	Section 2.7.9.70
118h	ITM Stimulus Port Register 70	Provides the interface for generating Instrumentation packets	Section 2.7.9.71
11Ch	ITM Stimulus Port Register 71	Provides the interface for generating Instrumentation packets	Section 2.7.9.72
120h	ITM Stimulus Port Register 72	Provides the interface for generating Instrumentation packets	Section 2.7.9.73
124h	ITM Stimulus Port Register 73	Provides the interface for generating Instrumentation packets	Section 2.7.9.74
128h	ITM Stimulus Port Register 74	Provides the interface for generating Instrumentation packets	Section 2.7.9.75
12Ch	ITM Stimulus Port Register 75	Provides the interface for generating Instrumentation packets	Section 2.7.9.76

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
130h	ITM Stimulus Port Register 76	Provides the interface for generating Instrumentation packets	Section 2.7.9.77
134h	ITM Stimulus Port Register 77	Provides the interface for generating Instrumentation packets	Section 2.7.9.78
138h	ITM Stimulus Port Register 78	Provides the interface for generating Instrumentation packets	Section 2.7.9.79
13Ch	ITM Stimulus Port Register 79	Provides the interface for generating Instrumentation packets	Section 2.7.9.80
140h	ITM Stimulus Port Register 80	Provides the interface for generating Instrumentation packets	Section 2.7.9.81
144h	ITM Stimulus Port Register 81	Provides the interface for generating Instrumentation packets	Section 2.7.9.82
148h	ITM Stimulus Port Register 82	Provides the interface for generating Instrumentation packets	Section 2.7.9.83
14Ch	ITM Stimulus Port Register 83	Provides the interface for generating Instrumentation packets	Section 2.7.9.84
150h	ITM Stimulus Port Register 84	Provides the interface for generating Instrumentation packets	Section 2.7.9.85
154h	ITM Stimulus Port Register 85	Provides the interface for generating Instrumentation packets	Section 2.7.9.86
158h	ITM Stimulus Port Register 86	Provides the interface for generating Instrumentation packets	Section 2.7.9.87
15Ch	ITM Stimulus Port Register 87	Provides the interface for generating Instrumentation packets	Section 2.7.9.88
160h	ITM Stimulus Port Register 88	Provides the interface for generating Instrumentation packets	Section 2.7.9.89
164h	ITM Stimulus Port Register 89	Provides the interface for generating Instrumentation packets	Section 2.7.9.90
168h	ITM Stimulus Port Register 90	Provides the interface for generating Instrumentation packets	Section 2.7.9.91
16Ch	ITM Stimulus Port Register 91	Provides the interface for generating Instrumentation packets	Section 2.7.9.92
170h	ITM Stimulus Port Register 92	Provides the interface for generating Instrumentation packets	Section 2.7.9.93
174h	ITM Stimulus Port Register 93	Provides the interface for generating Instrumentation packets	Section 2.7.9.94
178h	ITM Stimulus Port Register 94	Provides the interface for generating Instrumentation packets	Section 2.7.9.95
17Ch	ITM Stimulus Port Register 95	Provides the interface for generating Instrumentation packets	Section 2.7.9.96
180h	ITM Stimulus Port Register 96	Provides the interface for generating Instrumentation packets	Section 2.7.9.97
184h	ITM Stimulus Port Register 97	Provides the interface for generating Instrumentation packets	Section 2.7.9.98
188h	ITM Stimulus Port Register 98	Provides the interface for generating Instrumentation packets	Section 2.7.9.99
18Ch	ITM Stimulus Port Register 99	Provides the interface for generating Instrumentation packets	Section 2.7.9.100
190h	ITM Stimulus Port Register 100	Provides the interface for generating Instrumentation packets	Section 2.7.9.101
194h	ITM Stimulus Port Register 101	Provides the interface for generating Instrumentation packets	Section 2.7.9.102

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
198h	ITM Stimulus Port Register 102	Provides the interface for generating Instrumentation packets	Section 2.7.9.103
19Ch	ITM Stimulus Port Register 103	Provides the interface for generating Instrumentation packets	Section 2.7.9.104
1A0h	ITM Stimulus Port Register 104	Provides the interface for generating Instrumentation packets	Section 2.7.9.105
1A4h	ITM Stimulus Port Register 105	Provides the interface for generating Instrumentation packets	Section 2.7.9.106
1A8h	ITM Stimulus Port Register 106	Provides the interface for generating Instrumentation packets	Section 2.7.9.107
1ACh	ITM Stimulus Port Register 107	Provides the interface for generating Instrumentation packets	Section 2.7.9.108
1B0h	ITM Stimulus Port Register 108	Provides the interface for generating Instrumentation packets	Section 2.7.9.109
1B4h	ITM Stimulus Port Register 109	Provides the interface for generating Instrumentation packets	Section 2.7.9.110
1B8h	ITM Stimulus Port Register 110	Provides the interface for generating Instrumentation packets	Section 2.7.9.111
1BCh	ITM Stimulus Port Register 111	Provides the interface for generating Instrumentation packets	Section 2.7.9.112
1C0h	ITM Stimulus Port Register 112	Provides the interface for generating Instrumentation packets	Section 2.7.9.113
1C4h	ITM Stimulus Port Register 113	Provides the interface for generating Instrumentation packets	Section 2.7.9.114
1C8h	ITM Stimulus Port Register 114	Provides the interface for generating Instrumentation packets	Section 2.7.9.115
1CCh	ITM Stimulus Port Register 115	Provides the interface for generating Instrumentation packets	Section 2.7.9.116
1D0h	ITM Stimulus Port Register 116	Provides the interface for generating Instrumentation packets	Section 2.7.9.117
1D4h	ITM Stimulus Port Register 117	Provides the interface for generating Instrumentation packets	Section 2.7.9.118
1D8h	ITM Stimulus Port Register 118	Provides the interface for generating Instrumentation packets	Section 2.7.9.119
1DCh	ITM Stimulus Port Register 119	Provides the interface for generating Instrumentation packets	Section 2.7.9.120
1E0h	ITM Stimulus Port Register 120	Provides the interface for generating Instrumentation packets	Section 2.7.9.121
1E4h	ITM Stimulus Port Register 121	Provides the interface for generating Instrumentation packets	Section 2.7.9.122
1E8h	ITM Stimulus Port Register 122	Provides the interface for generating Instrumentation packets	Section 2.7.9.123
1ECh	ITM Stimulus Port Register 123	Provides the interface for generating Instrumentation packets	Section 2.7.9.124
1F0h	ITM Stimulus Port Register 124	Provides the interface for generating Instrumentation packets	Section 2.7.9.125
1F4h	ITM Stimulus Port Register 125	Provides the interface for generating Instrumentation packets	Section 2.7.9.126
1F8h	ITM Stimulus Port Register 126	Provides the interface for generating Instrumentation packets	Section 2.7.9.127
1FCh	ITM Stimulus Port Register 127	Provides the interface for generating Instrumentation packets	Section 2.7.9.128

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
200h	ITM Stimulus Port Register 128	Provides the interface for generating Instrumentation packets	Section 2.7.9.129
204h	ITM Stimulus Port Register 129	Provides the interface for generating Instrumentation packets	Section 2.7.9.130
208h	ITM Stimulus Port Register 130	Provides the interface for generating Instrumentation packets	Section 2.7.9.131
20Ch	ITM Stimulus Port Register 131	Provides the interface for generating Instrumentation packets	Section 2.7.9.132
210h	ITM Stimulus Port Register 132	Provides the interface for generating Instrumentation packets	Section 2.7.9.133
214h	ITM Stimulus Port Register 133	Provides the interface for generating Instrumentation packets	Section 2.7.9.134
218h	ITM Stimulus Port Register 134	Provides the interface for generating Instrumentation packets	Section 2.7.9.135
21Ch	ITM Stimulus Port Register 135	Provides the interface for generating Instrumentation packets	Section 2.7.9.136
220h	ITM Stimulus Port Register 136	Provides the interface for generating Instrumentation packets	Section 2.7.9.137
224h	ITM Stimulus Port Register 137	Provides the interface for generating Instrumentation packets	Section 2.7.9.138
228h	ITM Stimulus Port Register 138	Provides the interface for generating Instrumentation packets	Section 2.7.9.139
22Ch	ITM Stimulus Port Register 139	Provides the interface for generating Instrumentation packets	Section 2.7.9.140
230h	ITM Stimulus Port Register 140	Provides the interface for generating Instrumentation packets	Section 2.7.9.141
234h	ITM Stimulus Port Register 141	Provides the interface for generating Instrumentation packets	Section 2.7.9.142
238h	ITM Stimulus Port Register 142	Provides the interface for generating Instrumentation packets	Section 2.7.9.143
23Ch	ITM Stimulus Port Register 143	Provides the interface for generating Instrumentation packets	Section 2.7.9.144
240h	ITM Stimulus Port Register 144	Provides the interface for generating Instrumentation packets	Section 2.7.9.145
244h	ITM Stimulus Port Register 145	Provides the interface for generating Instrumentation packets	Section 2.7.9.146
248h	ITM Stimulus Port Register 146	Provides the interface for generating Instrumentation packets	Section 2.7.9.147
24Ch	ITM Stimulus Port Register 147	Provides the interface for generating Instrumentation packets	Section 2.7.9.148
250h	ITM Stimulus Port Register 148	Provides the interface for generating Instrumentation packets	Section 2.7.9.149
254h	ITM Stimulus Port Register 149	Provides the interface for generating Instrumentation packets	Section 2.7.9.150
258h	ITM Stimulus Port Register 150	Provides the interface for generating Instrumentation packets	Section 2.7.9.151
25Ch	ITM Stimulus Port Register 151	Provides the interface for generating Instrumentation packets	Section 2.7.9.152
260h	ITM Stimulus Port Register 152	Provides the interface for generating Instrumentation packets	Section 2.7.9.153
264h	ITM Stimulus Port Register 153	Provides the interface for generating Instrumentation packets	Section 2.7.9.154

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
268h	ITM Stimulus Port Register 154	Provides the interface for generating Instrumentation packets	Section 2.7.9.155
26Ch	ITM Stimulus Port Register 155	Provides the interface for generating Instrumentation packets	Section 2.7.9.156
270h	ITM Stimulus Port Register 156	Provides the interface for generating Instrumentation packets	Section 2.7.9.157
274h	ITM Stimulus Port Register 157	Provides the interface for generating Instrumentation packets	Section 2.7.9.158
278h	ITM Stimulus Port Register 158	Provides the interface for generating Instrumentation packets	Section 2.7.9.159
27Ch	ITM Stimulus Port Register 159	Provides the interface for generating Instrumentation packets	Section 2.7.9.160
280h	ITM Stimulus Port Register 160	Provides the interface for generating Instrumentation packets	Section 2.7.9.161
284h	ITM Stimulus Port Register 161	Provides the interface for generating Instrumentation packets	Section 2.7.9.162
288h	ITM Stimulus Port Register 162	Provides the interface for generating Instrumentation packets	Section 2.7.9.163
28Ch	ITM Stimulus Port Register 163	Provides the interface for generating Instrumentation packets	Section 2.7.9.164
290h	ITM Stimulus Port Register 164	Provides the interface for generating Instrumentation packets	Section 2.7.9.165
294h	ITM Stimulus Port Register 165	Provides the interface for generating Instrumentation packets	Section 2.7.9.166
298h	ITM Stimulus Port Register 166	Provides the interface for generating Instrumentation packets	Section 2.7.9.167
29Ch	ITM Stimulus Port Register 167	Provides the interface for generating Instrumentation packets	Section 2.7.9.168
2A0h	ITM Stimulus Port Register 168	Provides the interface for generating Instrumentation packets	Section 2.7.9.169
2A4h	ITM Stimulus Port Register 169	Provides the interface for generating Instrumentation packets	Section 2.7.9.170
2A8h	ITM Stimulus Port Register 170	Provides the interface for generating Instrumentation packets	Section 2.7.9.171
2ACh	ITM Stimulus Port Register 171	Provides the interface for generating Instrumentation packets	Section 2.7.9.172
2B0h	ITM Stimulus Port Register 172	Provides the interface for generating Instrumentation packets	Section 2.7.9.173
2B4h	ITM Stimulus Port Register 173	Provides the interface for generating Instrumentation packets	Section 2.7.9.174
2B8h	ITM Stimulus Port Register 174	Provides the interface for generating Instrumentation packets	Section 2.7.9.175
2BCh	ITM Stimulus Port Register 175	Provides the interface for generating Instrumentation packets	Section 2.7.9.176
2C0h	ITM Stimulus Port Register 176	Provides the interface for generating Instrumentation packets	Section 2.7.9.177
2C4h	ITM Stimulus Port Register 177	Provides the interface for generating Instrumentation packets	Section 2.7.9.178
2C8h	ITM Stimulus Port Register 178	Provides the interface for generating Instrumentation packets	Section 2.7.9.179
2CCh	ITM Stimulus Port Register 179	Provides the interface for generating Instrumentation packets	Section 2.7.9.180

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
2D0h	ITM Stimulus Port Register 180	Provides the interface for generating Instrumentation packets	Section 2.7.9.181
2D4h	ITM Stimulus Port Register 181	Provides the interface for generating Instrumentation packets	Section 2.7.9.182
2D8h	ITM Stimulus Port Register 182	Provides the interface for generating Instrumentation packets	Section 2.7.9.183
2DCh	ITM Stimulus Port Register 183	Provides the interface for generating Instrumentation packets	Section 2.7.9.184
2E0h	ITM Stimulus Port Register 184	Provides the interface for generating Instrumentation packets	Section 2.7.9.185
2E4h	ITM Stimulus Port Register 185	Provides the interface for generating Instrumentation packets	Section 2.7.9.186
2E8h	ITM Stimulus Port Register 186	Provides the interface for generating Instrumentation packets	Section 2.7.9.187
2ECh	ITM Stimulus Port Register 187	Provides the interface for generating Instrumentation packets	Section 2.7.9.188
2F0h	ITM Stimulus Port Register 188	Provides the interface for generating Instrumentation packets	Section 2.7.9.189
2F4h	ITM Stimulus Port Register 189	Provides the interface for generating Instrumentation packets	Section 2.7.9.190
2F8h	ITM Stimulus Port Register 190	Provides the interface for generating Instrumentation packets	Section 2.7.9.191
2FCh	ITM Stimulus Port Register 191	Provides the interface for generating Instrumentation packets	Section 2.7.9.192
300h	ITM Stimulus Port Register 192	Provides the interface for generating Instrumentation packets	Section 2.7.9.193
304h	ITM Stimulus Port Register 193	Provides the interface for generating Instrumentation packets	Section 2.7.9.194
308h	ITM Stimulus Port Register 194	Provides the interface for generating Instrumentation packets	Section 2.7.9.195
30Ch	ITM Stimulus Port Register 195	Provides the interface for generating Instrumentation packets	Section 2.7.9.196
310h	ITM Stimulus Port Register 196	Provides the interface for generating Instrumentation packets	Section 2.7.9.197
314h	ITM Stimulus Port Register 197	Provides the interface for generating Instrumentation packets	Section 2.7.9.198
318h	ITM Stimulus Port Register 198	Provides the interface for generating Instrumentation packets	Section 2.7.9.199
31Ch	ITM Stimulus Port Register 199	Provides the interface for generating Instrumentation packets	Section 2.7.9.200
320h	ITM Stimulus Port Register 200	Provides the interface for generating Instrumentation packets	Section 2.7.9.201
324h	ITM Stimulus Port Register 201	Provides the interface for generating Instrumentation packets	Section 2.7.9.202
328h	ITM Stimulus Port Register 202	Provides the interface for generating Instrumentation packets	Section 2.7.9.203
32Ch	ITM Stimulus Port Register 203	Provides the interface for generating Instrumentation packets	Section 2.7.9.204
330h	ITM Stimulus Port Register 204	Provides the interface for generating Instrumentation packets	Section 2.7.9.205
334h	ITM Stimulus Port Register 205	Provides the interface for generating Instrumentation packets	Section 2.7.9.206

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
338h	ITM Stimulus Port Register 206	Provides the interface for generating Instrumentation packets	Section 2.7.9.207
33Ch	ITM Stimulus Port Register 207	Provides the interface for generating Instrumentation packets	Section 2.7.9.208
340h	ITM Stimulus Port Register 208	Provides the interface for generating Instrumentation packets	Section 2.7.9.209
344h	ITM Stimulus Port Register 209	Provides the interface for generating Instrumentation packets	Section 2.7.9.210
348h	ITM Stimulus Port Register 210	Provides the interface for generating Instrumentation packets	Section 2.7.9.211
34Ch	ITM Stimulus Port Register 211	Provides the interface for generating Instrumentation packets	Section 2.7.9.212
350h	ITM Stimulus Port Register 212	Provides the interface for generating Instrumentation packets	Section 2.7.9.213
354h	ITM Stimulus Port Register 213	Provides the interface for generating Instrumentation packets	Section 2.7.9.214
358h	ITM Stimulus Port Register 214	Provides the interface for generating Instrumentation packets	Section 2.7.9.215
35Ch	ITM Stimulus Port Register 215	Provides the interface for generating Instrumentation packets	Section 2.7.9.216
360h	ITM Stimulus Port Register 216	Provides the interface for generating Instrumentation packets	Section 2.7.9.217
364h	ITM Stimulus Port Register 217	Provides the interface for generating Instrumentation packets	Section 2.7.9.218
368h	ITM Stimulus Port Register 218	Provides the interface for generating Instrumentation packets	Section 2.7.9.219
36Ch	ITM Stimulus Port Register 219	Provides the interface for generating Instrumentation packets	Section 2.7.9.220
370h	ITM Stimulus Port Register 220	Provides the interface for generating Instrumentation packets	Section 2.7.9.221
374h	ITM Stimulus Port Register 221	Provides the interface for generating Instrumentation packets	Section 2.7.9.222
378h	ITM Stimulus Port Register 222	Provides the interface for generating Instrumentation packets	Section 2.7.9.223
37Ch	ITM Stimulus Port Register 223	Provides the interface for generating Instrumentation packets	Section 2.7.9.224
380h	ITM Stimulus Port Register 224	Provides the interface for generating Instrumentation packets	Section 2.7.9.225
384h	ITM Stimulus Port Register 225	Provides the interface for generating Instrumentation packets	Section 2.7.9.226
388h	ITM Stimulus Port Register 226	Provides the interface for generating Instrumentation packets	Section 2.7.9.227
38Ch	ITM Stimulus Port Register 227	Provides the interface for generating Instrumentation packets	Section 2.7.9.228
390h	ITM Stimulus Port Register 228	Provides the interface for generating Instrumentation packets	Section 2.7.9.229
394h	ITM Stimulus Port Register 229	Provides the interface for generating Instrumentation packets	Section 2.7.9.230
398h	ITM Stimulus Port Register 230	Provides the interface for generating Instrumentation packets	Section 2.7.9.231
39Ch	ITM Stimulus Port Register 231	Provides the interface for generating Instrumentation packets	Section 2.7.9.232

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
3A0h	ITM Stimulus Port Register 232	Provides the interface for generating Instrumentation packets	Section 2.7.9.233
3A4h	ITM Stimulus Port Register 233	Provides the interface for generating Instrumentation packets	Section 2.7.9.234
3A8h	ITM Stimulus Port Register 234	Provides the interface for generating Instrumentation packets	Section 2.7.9.235
3ACh	ITM Stimulus Port Register 235	Provides the interface for generating Instrumentation packets	Section 2.7.9.236
3B0h	ITM Stimulus Port Register 236	Provides the interface for generating Instrumentation packets	Section 2.7.9.237
3B4h	ITM Stimulus Port Register 237	Provides the interface for generating Instrumentation packets	Section 2.7.9.238
3B8h	ITM Stimulus Port Register 238	Provides the interface for generating Instrumentation packets	Section 2.7.9.239
3BCh	ITM Stimulus Port Register 239	Provides the interface for generating Instrumentation packets	Section 2.7.9.240
3C0h	ITM Stimulus Port Register 240	Provides the interface for generating Instrumentation packets	Section 2.7.9.241
3C4h	ITM Stimulus Port Register 241	Provides the interface for generating Instrumentation packets	Section 2.7.9.242
3C8h	ITM Stimulus Port Register 242	Provides the interface for generating Instrumentation packets	Section 2.7.9.243
3CCh	ITM Stimulus Port Register 243	Provides the interface for generating Instrumentation packets	Section 2.7.9.244
3D0h	ITM Stimulus Port Register 244	Provides the interface for generating Instrumentation packets	Section 2.7.9.245
3D4h	ITM Stimulus Port Register 245	Provides the interface for generating Instrumentation packets	Section 2.7.9.246
3D8h	ITM Stimulus Port Register 246	Provides the interface for generating Instrumentation packets	Section 2.7.9.247
3DCh	ITM Stimulus Port Register 247	Provides the interface for generating Instrumentation packets	Section 2.7.9.248
3E0h	ITM Stimulus Port Register 248	Provides the interface for generating Instrumentation packets	Section 2.7.9.249
3E4h	ITM Stimulus Port Register 249	Provides the interface for generating Instrumentation packets	Section 2.7.9.250
3E8h	ITM Stimulus Port Register 250	Provides the interface for generating Instrumentation packets	Section 2.7.9.251
3ECh	ITM Stimulus Port Register 251	Provides the interface for generating Instrumentation packets	Section 2.7.9.252
3F0h	ITM Stimulus Port Register 252	Provides the interface for generating Instrumentation packets	Section 2.7.9.253
3F4h	ITM Stimulus Port Register 253	Provides the interface for generating Instrumentation packets	Section 2.7.9.254
3F8h	ITM Stimulus Port Register 254	Provides the interface for generating Instrumentation packets	Section 2.7.9.255
3FCh	ITM Stimulus Port Register 255	Provides the interface for generating Instrumentation packets	Section 2.7.9.256
E00h	ITM Trace Enable Register 0	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.257
E04h	ITM Trace Enable Register 1	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.258

Table 2-146. ITM Registers (continued)

Offset	Acronym	Register Name	Section
E08h	ITM Trace Enable Register 2	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.259
E0Ch	ITM Trace Enable Register 3	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.260
E10h	ITM Trace Enable Register 4	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.261
E14h	ITM Trace Enable Register 5	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.262
E18h	ITM Trace Enable Register 6	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.263
E1Ch	ITM Trace Enable Register 7	Provide an individual enable bit for each ITM_STIM register	Section 2.7.9.264
E40h	ITM Trace Privilege Register	Controls which stimulus ports can be accessed by unprivileged code	Section 2.7.9.265
E80h	ITM Trace Control Register	Configures and controls transfers through the ITM interface	Section 2.7.9.266
EF0h	INT_ATREADY	Integration Mode: Read ATB Ready	Section 2.7.9.267
EF8h	INT_ATVALID	Integration Mode: Write ATB Valid	Section 2.7.9.268
F00h	ITM_ITCTRL	Integration Mode Control Register	Section 2.7.9.269
FBCh	ITM Device Architecture Register	Provides CoreSight discovery information for the ITM	Section 2.7.9.270
FCCh	ITM Device Type Register	Provides CoreSight discovery information for the ITM	Section 2.7.9.271
FD0h	ITM Peripheral Identification Register 4	Provides CoreSight discovery information for the ITM	Section 2.7.9.272
FD4h	ITM Peripheral Identification Register 5	Provides CoreSight discovery information for the ITM	Section 2.7.9.273
FD8h	ITM Peripheral Identification Register 6	Provides CoreSight discovery information for the ITM	Section 2.7.9.274
FDCh	ITM Peripheral Identification Register 7	Provides CoreSight discovery information for the ITM	Section 2.7.9.275
FE0h	ITM Peripheral Identification Register 0	Provides CoreSight discovery information for the ITM	Section 2.7.9.276
FE4h	ITM Peripheral Identification Register 1	Provides CoreSight discovery information for the ITM	Section 2.7.9.277
FE8h	ITM Peripheral Identification Register 2	Provides CoreSight discovery information for the ITM	Section 2.7.9.278
FECh	ITM Peripheral Identification Register 3	Provides CoreSight discovery information for the ITM	Section 2.7.9.279
FF0h	ITM Component Identification Register 0	Provides CoreSight discovery information for the ITM	Section 2.7.9.280
FF4h	ITM Component Identification Register 1	Provides CoreSight discovery information for the ITM	Section 2.7.9.281
FF8h	ITM Component Identification Register 2	Provides CoreSight discovery information for the ITM	Section 2.7.9.282
FFCh	ITM Component Identification Register 3	Provides CoreSight discovery information for the ITM	Section 2.7.9.283

Complex bit access types are encoded to fit into small table cells. Table 2-147 shows the codes that are used for access types in this section.

Table 2-147. ITM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.9.1 ITM Stimulus Port Register 0 (Offset = 0h) [Reset = 00000002h]

ITM Stimulus Port Register 0 is shown in Table 2-148.

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Table 2-148. ITM Stimulus Port Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.2 ITM Stimulus Port Register 1 (Offset = 4h) [Reset = 00000002h]

ITM Stimulus Port Register 1 is shown in Table 2-149.

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Table 2-149. ITM Stimulus Port Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.3 ITM Stimulus Port Register 2 (Offset = 8h) [Reset = 00000002h]

ITM Stimulus Port Register 2 is shown in Table 2-150.

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Table 2-150. ITM Stimulus Port Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.4 ITM Stimulus Port Register 3 (Offset = Ch) [Reset = 00000002h]

ITM Stimulus Port Register 3 is shown in Table 2-151.

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Table 2-151. ITM Stimulus Port Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.5 ITM Stimulus Port Register 4 (Offset = 10h) [Reset = 00000002h]

ITM Stimulus Port Register 4 is shown in Table 2-152.

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Table 2-152. ITM Stimulus Port Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.6 ITM Stimulus Port Register 5 (Offset = 14h) [Reset = 00000002h]

ITM Stimulus Port Register 5 is shown in Table 2-153.

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Table 2-153. ITM Stimulus Port Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.7 ITM Stimulus Port Register 6 (Offset = 18h) [Reset = 00000002h]

ITM Stimulus Port Register 6 is shown in Table 2-154.

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Table 2-154. ITM Stimulus Port Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.8 ITM Stimulus Port Register 7 (Offset = 1Ch) [Reset = 00000002h]

ITM Stimulus Port Register 7 is shown in Table 2-155.

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Table 2-155. ITM Stimulus Port Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.9 ITM Stimulus Port Register 8 (Offset = 20h) [Reset = 00000002h]

ITM Stimulus Port Register 8 is shown in Table 2-156.

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Table 2-156. ITM Stimulus Port Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.10 ITM Stimulus Port Register 9 (Offset = 24h) [Reset = 00000002h]

ITM Stimulus Port Register 9 is shown in Table 2-157.

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Table 2-157. ITM Stimulus Port Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.11 ITM Stimulus Port Register 10 (Offset = 28h) [Reset = 00000002h]

ITM Stimulus Port Register 10 is shown in Table 2-158.

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Table 2-158. ITM Stimulus Port Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.12 ITM Stimulus Port Register 11 (Offset = 2Ch) [Reset = 00000002h]

ITM Stimulus Port Register 11 is shown in Table 2-159.

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Table 2-159. ITM Stimulus Port Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.13 ITM Stimulus Port Register 12 (Offset = 30h) [Reset = 00000002h]

ITM Stimulus Port Register 12 is shown in Table 2-160.

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Table 2-160. ITM Stimulus Port Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.14 ITM Stimulus Port Register 13 (Offset = 34h) [Reset = 00000002h]

ITM Stimulus Port Register 13 is shown in Table 2-161.

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Table 2-161. ITM Stimulus Port Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.15 ITM Stimulus Port Register 14 (Offset = 38h) [Reset = 00000002h]

ITM Stimulus Port Register 14 is shown in Table 2-162.

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Table 2-162. ITM Stimulus Port Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.16 ITM Stimulus Port Register 15 (Offset = 3Ch) [Reset = 00000002h]

ITM Stimulus Port Register 15 is shown in Table 2-163.

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Table 2-163. ITM Stimulus Port Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.17 ITM Stimulus Port Register 16 (Offset = 40h) [Reset = 00000002h]

ITM Stimulus Port Register 16 is shown in Table 2-164.

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Table 2-164. ITM Stimulus Port Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.18 ITM Stimulus Port Register 17 (Offset = 44h) [Reset = 00000002h]

ITM Stimulus Port Register 17 is shown in Table 2-165.

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Table 2-165. ITM Stimulus Port Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.19 ITM Stimulus Port Register 18 (Offset = 48h) [Reset = 00000002h]

ITM Stimulus Port Register 18 is shown in Table 2-166.

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Table 2-166. ITM Stimulus Port Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.20 ITM Stimulus Port Register 19 (Offset = 4Ch) [Reset = 00000002h]

ITM Stimulus Port Register 19 is shown in Table 2-167.

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Table 2-167. ITM Stimulus Port Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.21 ITM Stimulus Port Register 20 (Offset = 50h) [Reset = 00000002h]

ITM Stimulus Port Register 20 is shown in Table 2-168.

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Table 2-168. ITM Stimulus Port Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.22 ITM Stimulus Port Register 21 (Offset = 54h) [Reset = 00000002h]

ITM Stimulus Port Register 21 is shown in Table 2-169.

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Table 2-169. ITM Stimulus Port Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.23 ITM Stimulus Port Register 22 (Offset = 58h) [Reset = 00000002h]

ITM Stimulus Port Register 22 is shown in Table 2-170.

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Table 2-170. ITM Stimulus Port Register 22 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.24 ITM Stimulus Port Register 23 (Offset = 5Ch) [Reset = 00000002h]

ITM Stimulus Port Register 23 is shown in Table 2-171.

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Table 2-171. ITM Stimulus Port Register 23 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.25 ITM Stimulus Port Register 24 (Offset = 60h) [Reset = 00000002h]

ITM Stimulus Port Register 24 is shown in Table 2-172.

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Table 2-172. ITM Stimulus Port Register 24 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.26 ITM Stimulus Port Register 25 (Offset = 64h) [Reset = 00000002h]

ITM Stimulus Port Register 25 is shown in Table 2-173.

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Table 2-173. ITM Stimulus Port Register 25 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.27 ITM Stimulus Port Register 26 (Offset = 68h) [Reset = 00000002h]

ITM Stimulus Port Register 26 is shown in Table 2-174.

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Table 2-174. ITM Stimulus Port Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.28 ITM Stimulus Port Register 27 (Offset = 6Ch) [Reset = 00000002h]

ITM Stimulus Port Register 27 is shown in Table 2-175.

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Table 2-175. ITM Stimulus Port Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.29 ITM Stimulus Port Register 28 (Offset = 70h) [Reset = 00000002h]

ITM Stimulus Port Register 28 is shown in Table 2-176.

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Table 2-176. ITM Stimulus Port Register 28 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.30 ITM Stimulus Port Register 29 (Offset = 74h) [Reset = 00000002h]

ITM Stimulus Port Register 29 is shown in Table 2-177.

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Table 2-177. ITM Stimulus Port Register 29 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.31 ITM Stimulus Port Register 30 (Offset = 78h) [Reset = 00000002h]

ITM Stimulus Port Register 30 is shown in Table 2-178.

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Table 2-178. ITM Stimulus Port Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.32 ITM Stimulus Port Register 31 (Offset = 7Ch) [Reset = 00000002h]

ITM Stimulus Port Register 31 is shown in Table 2-179.

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Table 2-179. ITM Stimulus Port Register 31 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	1h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	2h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.33 ITM Stimulus Port Register 32 (Offset = 80h) [Reset = 00000000h]

ITM Stimulus Port Register 32 is shown in Table 2-180.

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Table 2-180. ITM Stimulus Port Register 32 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.34 ITM Stimulus Port Register 33 (Offset = 84h) [Reset = 00000000h]

ITM Stimulus Port Register 33 is shown in Table 2-181.

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Table 2-181. ITM Stimulus Port Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.35 ITM Stimulus Port Register 34 (Offset = 88h) [Reset = 00000000h]

ITM Stimulus Port Register 34 is shown in Table 2-182.

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Table 2-182. ITM Stimulus Port Register 34 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.36 ITM Stimulus Port Register 35 (Offset = 8Ch) [Reset = 00000000h]

ITM Stimulus Port Register 35 is shown in Table 2-183.

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Table 2-183. ITM Stimulus Port Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.37 ITM Stimulus Port Register 36 (Offset = 90h) [Reset = 00000000h]

ITM Stimulus Port Register 36 is shown in Table 2-184.

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Table 2-184. ITM Stimulus Port Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.38 ITM Stimulus Port Register 37 (Offset = 94h) [Reset = 00000000h]

ITM Stimulus Port Register 37 is shown in Table 2-185.

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Table 2-185. ITM Stimulus Port Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.39 ITM Stimulus Port Register 38 (Offset = 98h) [Reset = 00000000h]

ITM Stimulus Port Register 38 is shown in Table 2-186.

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Table 2-186. ITM Stimulus Port Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.40 ITM Stimulus Port Register 39 (Offset = 9Ch) [Reset = 00000000h]

ITM Stimulus Port Register 39 is shown in Table 2-187.

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Table 2-187. ITM Stimulus Port Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.41 ITM Stimulus Port Register 40 (Offset = A0h) [Reset = 00000000h]

ITM Stimulus Port Register 40 is shown in Table 2-188.

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Table 2-188. ITM Stimulus Port Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.42 ITM Stimulus Port Register 41 (Offset = A4h) [Reset = 00000000h]

ITM Stimulus Port Register 41 is shown in Table 2-189.

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Table 2-189. ITM Stimulus Port Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.43 ITM Stimulus Port Register 42 (Offset = A8h) [Reset = 00000000h]

ITM Stimulus Port Register 42 is shown in Table 2-190.

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Table 2-190. ITM Stimulus Port Register 42 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.44 ITM Stimulus Port Register 43 (Offset = ACh) [Reset = 00000000h]

ITM Stimulus Port Register 43 is shown in Table 2-191.

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Table 2-191. ITM Stimulus Port Register 43 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.45 ITM Stimulus Port Register 44 (Offset = B0h) [Reset = 00000000h]

ITM Stimulus Port Register 44 is shown in Table 2-192.

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Table 2-192. ITM Stimulus Port Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.46 ITM Stimulus Port Register 45 (Offset = B4h) [Reset = 00000000h]

ITM Stimulus Port Register 45 is shown in Table 2-193.

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Table 2-193. ITM Stimulus Port Register 45 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.47 ITM Stimulus Port Register 46 (Offset = B8h) [Reset = 00000000h]

ITM Stimulus Port Register 46 is shown in Table 2-194.

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Table 2-194. ITM Stimulus Port Register 46 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.48 ITM Stimulus Port Register 47 (Offset = BCh) [Reset = 00000000h]

ITM Stimulus Port Register 47 is shown in Table 2-195.

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Table 2-195. ITM Stimulus Port Register 47 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.49 ITM Stimulus Port Register 48 (Offset = C0h) [Reset = 00000000h]

ITM Stimulus Port Register 48 is shown in Table 2-196.

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Table 2-196. ITM Stimulus Port Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.50 ITM Stimulus Port Register 49 (Offset = C4h) [Reset = 00000000h]

ITM Stimulus Port Register 49 is shown in Table 2-197.

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Table 2-197. ITM Stimulus Port Register 49 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.51 ITM Stimulus Port Register 50 (Offset = C8h) [Reset = 00000000h]

ITM Stimulus Port Register 50 is shown in Table 2-198.

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Table 2-198. ITM Stimulus Port Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.52 ITM Stimulus Port Register 51 (Offset = CCh) [Reset = 00000000h]

ITM Stimulus Port Register 51 is shown in Table 2-199.

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Table 2-199. ITM Stimulus Port Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.53 ITM Stimulus Port Register 52 (Offset = D0h) [Reset = 00000000h]

ITM Stimulus Port Register 52 is shown in Table 2-200.

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Table 2-200. ITM Stimulus Port Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.54 ITM Stimulus Port Register 53 (Offset = D4h) [Reset = 00000000h]

ITM Stimulus Port Register 53 is shown in Table 2-201.

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Table 2-201. ITM Stimulus Port Register 53 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.55 ITM Stimulus Port Register 54 (Offset = D8h) [Reset = 00000000h]

ITM Stimulus Port Register 54 is shown in Table 2-202.

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Table 2-202. ITM Stimulus Port Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.56 ITM Stimulus Port Register 55 (Offset = DCh) [Reset = 00000000h]

ITM Stimulus Port Register 55 is shown in Table 2-203.

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Table 2-203. ITM Stimulus Port Register 55 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.57 ITM Stimulus Port Register 56 (Offset = E0h) [Reset = 00000000h]

ITM Stimulus Port Register 56 is shown in Table 2-204.

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Table 2-204. ITM Stimulus Port Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.58 ITM Stimulus Port Register 57 (Offset = E4h) [Reset = 00000000h]

ITM Stimulus Port Register 57 is shown in Table 2-205.

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Table 2-205. ITM Stimulus Port Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.59 ITM Stimulus Port Register 58 (Offset = E8h) [Reset = 00000000h]

ITM Stimulus Port Register 58 is shown in Table 2-206.

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Table 2-206. ITM Stimulus Port Register 58 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.60 ITM Stimulus Port Register 59 (Offset = ECh) [Reset = 00000000h]

ITM Stimulus Port Register 59 is shown in Table 2-207.

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Table 2-207. ITM Stimulus Port Register 59 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.61 ITM Stimulus Port Register 60 (Offset = F0h) [Reset = 00000000h]

ITM Stimulus Port Register 60 is shown in Table 2-208.

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Table 2-208. ITM Stimulus Port Register 60 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.62 ITM Stimulus Port Register 61 (Offset = F4h) [Reset = 00000000h]

ITM Stimulus Port Register 61 is shown in Table 2-209.

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Table 2-209. ITM Stimulus Port Register 61 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.63 ITM Stimulus Port Register 62 (Offset = F8h) [Reset = 00000000h]

ITM Stimulus Port Register 62 is shown in Table 2-210.

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Table 2-210. ITM Stimulus Port Register 62 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.64 ITM Stimulus Port Register 63 (Offset = FCh) [Reset = 00000000h]

ITM Stimulus Port Register 63 is shown in Table 2-211.

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Table 2-211. ITM Stimulus Port Register 63 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.65 ITM Stimulus Port Register 64 (Offset = 100h) [Reset = 00000000h]

ITM Stimulus Port Register 64 is shown in Table 2-212.

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Table 2-212. ITM Stimulus Port Register 64 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.66 ITM Stimulus Port Register 65 (Offset = 104h) [Reset = 00000000h]

ITM Stimulus Port Register 65 is shown in Table 2-213.

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Table 2-213. ITM Stimulus Port Register 65 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.67 ITM Stimulus Port Register 66 (Offset = 108h) [Reset = 00000000h]

ITM Stimulus Port Register 66 is shown in Table 2-214.

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Table 2-214. ITM Stimulus Port Register 66 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.68 ITM Stimulus Port Register 67 (Offset = 10Ch) [Reset = 00000000h]

ITM Stimulus Port Register 67 is shown in Table 2-215.

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Table 2-215. ITM Stimulus Port Register 67 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.69 ITM Stimulus Port Register 68 (Offset = 110h) [Reset = 00000000h]

ITM Stimulus Port Register 68 is shown in Table 2-216.

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Table 2-216. ITM Stimulus Port Register 68 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.70 ITM Stimulus Port Register 69 (Offset = 114h) [Reset = 00000000h]

ITM Stimulus Port Register 69 is shown in Table 2-217.

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Table 2-217. ITM Stimulus Port Register 69 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.71 ITM Stimulus Port Register 70 (Offset = 118h) [Reset = 00000000h]

ITM Stimulus Port Register 70 is shown in Table 2-218.

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Table 2-218. ITM Stimulus Port Register 70 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.72 ITM Stimulus Port Register 71 (Offset = 11Ch) [Reset = 00000000h]

ITM Stimulus Port Register 71 is shown in Table 2-219.

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Table 2-219. ITM Stimulus Port Register 71 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.73 ITM Stimulus Port Register 72 (Offset = 120h) [Reset = 00000000h]

ITM Stimulus Port Register 72 is shown in Table 2-220.

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Table 2-220. ITM Stimulus Port Register 72 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.74 ITM Stimulus Port Register 73 (Offset = 124h) [Reset = 00000000h]

ITM Stimulus Port Register 73 is shown in Table 2-221.

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Table 2-221. ITM Stimulus Port Register 73 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.75 ITM Stimulus Port Register 74 (Offset = 128h) [Reset = 00000000h]

ITM Stimulus Port Register 74 is shown in Table 2-222.

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Table 2-222. ITM Stimulus Port Register 74 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.76 ITM Stimulus Port Register 75 (Offset = 12Ch) [Reset = 00000000h]

ITM Stimulus Port Register 75 is shown in Table 2-223.

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Table 2-223. ITM Stimulus Port Register 75 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.77 ITM Stimulus Port Register 76 (Offset = 130h) [Reset = 00000000h]

ITM Stimulus Port Register 76 is shown in Table 2-224.

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Table 2-224. ITM Stimulus Port Register 76 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.78 ITM Stimulus Port Register 77 (Offset = 134h) [Reset = 00000000h]

ITM Stimulus Port Register 77 is shown in Table 2-225.

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Table 2-225. ITM Stimulus Port Register 77 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.79 ITM Stimulus Port Register 78 (Offset = 138h) [Reset = 00000000h]

ITM Stimulus Port Register 78 is shown in Table 2-226.

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Table 2-226. ITM Stimulus Port Register 78 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.80 ITM Stimulus Port Register 79 (Offset = 13Ch) [Reset = 00000000h]

ITM Stimulus Port Register 79 is shown in Table 2-227.

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Table 2-227. ITM Stimulus Port Register 79 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.81 ITM Stimulus Port Register 80 (Offset = 140h) [Reset = 00000000h]

ITM Stimulus Port Register 80 is shown in Table 2-228.

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Table 2-228. ITM Stimulus Port Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.82 ITM Stimulus Port Register 81 (Offset = 144h) [Reset = 00000000h]

ITM Stimulus Port Register 81 is shown in Table 2-229.

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Table 2-229. ITM Stimulus Port Register 81 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.83 ITM Stimulus Port Register 82 (Offset = 148h) [Reset = 00000000h]

ITM Stimulus Port Register 82 is shown in Table 2-230.

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Table 2-230. ITM Stimulus Port Register 82 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.84 ITM Stimulus Port Register 83 (Offset = 14Ch) [Reset = 00000000h]

ITM Stimulus Port Register 83 is shown in Table 2-231.

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Table 2-231. ITM Stimulus Port Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.85 ITM Stimulus Port Register 84 (Offset = 150h) [Reset = 00000000h]

ITM Stimulus Port Register 84 is shown in Table 2-232.

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Table 2-232. ITM Stimulus Port Register 84 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.86 ITM Stimulus Port Register 85 (Offset = 154h) [Reset = 00000000h]

ITM Stimulus Port Register 85 is shown in Table 2-233.

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Table 2-233. ITM Stimulus Port Register 85 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.87 ITM Stimulus Port Register 86 (Offset = 158h) [Reset = 00000000h]

ITM Stimulus Port Register 86 is shown in Table 2-234.

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Table 2-234. ITM Stimulus Port Register 86 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.88 ITM Stimulus Port Register 87 (Offset = 15Ch) [Reset = 00000000h]

ITM Stimulus Port Register 87 is shown in Table 2-235.

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Table 2-235. ITM Stimulus Port Register 87 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.89 ITM Stimulus Port Register 88 (Offset = 160h) [Reset = 00000000h]

ITM Stimulus Port Register 88 is shown in Table 2-236.

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Table 2-236. ITM Stimulus Port Register 88 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.90 ITM Stimulus Port Register 89 (Offset = 164h) [Reset = 00000000h]

ITM Stimulus Port Register 89 is shown in Table 2-237.

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Table 2-237. ITM Stimulus Port Register 89 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.91 ITM Stimulus Port Register 90 (Offset = 168h) [Reset = 00000000h]

ITM Stimulus Port Register 90 is shown in Table 2-238.

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Table 2-238. ITM Stimulus Port Register 90 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.92 ITM Stimulus Port Register 91 (Offset = 16Ch) [Reset = 00000000h]

ITM Stimulus Port Register 91 is shown in Table 2-239.

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Table 2-239. ITM Stimulus Port Register 91 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.93 ITM Stimulus Port Register 92 (Offset = 170h) [Reset = 00000000h]

ITM Stimulus Port Register 92 is shown in Table 2-240.

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Table 2-240. ITM Stimulus Port Register 92 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.94 ITM Stimulus Port Register 93 (Offset = 174h) [Reset = 00000000h]

ITM Stimulus Port Register 93 is shown in Table 2-241.

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Table 2-241. ITM Stimulus Port Register 93 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.95 ITM Stimulus Port Register 94 (Offset = 178h) [Reset = 00000000h]

ITM Stimulus Port Register 94 is shown in Table 2-242.

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Table 2-242. ITM Stimulus Port Register 94 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.96 ITM Stimulus Port Register 95 (Offset = 17Ch) [Reset = 00000000h]

ITM Stimulus Port Register 95 is shown in Table 2-243.

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Table 2-243. ITM Stimulus Port Register 95 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.97 ITM Stimulus Port Register 96 (Offset = 180h) [Reset = 00000000h]

ITM Stimulus Port Register 96 is shown in Table 2-244.

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Table 2-244. ITM Stimulus Port Register 96 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.98 ITM Stimulus Port Register 97 (Offset = 184h) [Reset = 00000000h]

ITM Stimulus Port Register 97 is shown in Table 2-245.

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Table 2-245. ITM Stimulus Port Register 97 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.99 ITM Stimulus Port Register 98 (Offset = 188h) [Reset = 00000000h]

ITM Stimulus Port Register 98 is shown in Table 2-246.

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Table 2-246. ITM Stimulus Port Register 98 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.100 ITM Stimulus Port Register 99 (Offset = 18Ch) [Reset = 00000000h]

ITM Stimulus Port Register 99 is shown in Table 2-247.

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Table 2-247. ITM Stimulus Port Register 99 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.101 ITM Stimulus Port Register 100 (Offset = 190h) [Reset = 00000000h]

ITM Stimulus Port Register 100 is shown in Table 2-248.

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Table 2-248. ITM Stimulus Port Register 100 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.102 ITM Stimulus Port Register 101 (Offset = 194h) [Reset = 00000000h]

ITM Stimulus Port Register 101 is shown in Table 2-249.

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Table 2-249. ITM Stimulus Port Register 101 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.103 ITM Stimulus Port Register 102 (Offset = 198h) [Reset = 00000000h]

ITM Stimulus Port Register 102 is shown in Table 2-250.

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Table 2-250. ITM Stimulus Port Register 102 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.104 ITM Stimulus Port Register 103 (Offset = 19Ch) [Reset = 00000000h]

ITM Stimulus Port Register 103 is shown in Table 2-251.

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Table 2-251. ITM Stimulus Port Register 103 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.105 ITM Stimulus Port Register 104 (Offset = 1A0h) [Reset = 00000000h]

ITM Stimulus Port Register 104 is shown in Table 2-252.

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Table 2-252. ITM Stimulus Port Register 104 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.106 ITM Stimulus Port Register 105 (Offset = 1A4h) [Reset = 00000000h]

ITM Stimulus Port Register 105 is shown in Table 2-253.

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Table 2-253. ITM Stimulus Port Register 105 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.107 ITM Stimulus Port Register 106 (Offset = 1A8h) [Reset = 00000000h]

ITM Stimulus Port Register 106 is shown in Table 2-254.

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Table 2-254. ITM Stimulus Port Register 106 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.108 ITM Stimulus Port Register 107 (Offset = 1ACh) [Reset = 00000000h]

ITM Stimulus Port Register 107 is shown in Table 2-255.

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Table 2-255. ITM Stimulus Port Register 107 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.109 ITM Stimulus Port Register 108 (Offset = 1B0h) [Reset = 00000000h]

ITM Stimulus Port Register 108 is shown in Table 2-256.

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Table 2-256. ITM Stimulus Port Register 108 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.110 ITM Stimulus Port Register 109 (Offset = 1B4h) [Reset = 00000000h]

ITM Stimulus Port Register 109 is shown in Table 2-257.

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Table 2-257. ITM Stimulus Port Register 109 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.111 ITM Stimulus Port Register 110 (Offset = 1B8h) [Reset = 00000000h]

ITM Stimulus Port Register 110 is shown in Table 2-258.

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Table 2-258. ITM Stimulus Port Register 110 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.112 ITM Stimulus Port Register 111 (Offset = 1BCh) [Reset = 00000000h]

ITM Stimulus Port Register 111 is shown in Table 2-259.

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Table 2-259. ITM Stimulus Port Register 111 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.113 ITM Stimulus Port Register 112 (Offset = 1C0h) [Reset = 00000000h]

ITM Stimulus Port Register 112 is shown in Table 2-260.

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Table 2-260. ITM Stimulus Port Register 112 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.114 ITM Stimulus Port Register 113 (Offset = 1C4h) [Reset = 00000000h]

ITM Stimulus Port Register 113 is shown in Table 2-261.

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Table 2-261. ITM Stimulus Port Register 113 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.115 ITM Stimulus Port Register 114 (Offset = 1C8h) [Reset = 00000000h]

ITM Stimulus Port Register 114 is shown in Table 2-262.

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Table 2-262. ITM Stimulus Port Register 114 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.116 ITM Stimulus Port Register 115 (Offset = 1CCh) [Reset = 00000000h]

ITM Stimulus Port Register 115 is shown in Table 2-263.

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Table 2-263. ITM Stimulus Port Register 115 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.117 ITM Stimulus Port Register 116 (Offset = 1D0h) [Reset = 00000000h]

ITM Stimulus Port Register 116 is shown in Table 2-264.

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Table 2-264. ITM Stimulus Port Register 116 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.118 ITM Stimulus Port Register 117 (Offset = 1D4h) [Reset = 00000000h]

ITM Stimulus Port Register 117 is shown in Table 2-265.

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Table 2-265. ITM Stimulus Port Register 117 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.119 ITM Stimulus Port Register 118 (Offset = 1D8h) [Reset = 00000000h]

ITM Stimulus Port Register 118 is shown in Table 2-266.

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Table 2-266. ITM Stimulus Port Register 118 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.120 ITM Stimulus Port Register 119 (Offset = 1DCh) [Reset = 00000000h]

ITM Stimulus Port Register 119 is shown in Table 2-267.

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Table 2-267. ITM Stimulus Port Register 119 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.121 ITM Stimulus Port Register 120 (Offset = 1E0h) [Reset = 00000000h]

ITM Stimulus Port Register 120 is shown in Table 2-268.

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Table 2-268. ITM Stimulus Port Register 120 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.122 ITM Stimulus Port Register 121 (Offset = 1E4h) [Reset = 00000000h]

ITM Stimulus Port Register 121 is shown in Table 2-269.

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Table 2-269. ITM Stimulus Port Register 121 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.123 ITM Stimulus Port Register 122 (Offset = 1E8h) [Reset = 00000000h]

ITM Stimulus Port Register 122 is shown in Table 2-270.

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Table 2-270. ITM Stimulus Port Register 122 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.124 ITM Stimulus Port Register 123 (Offset = 1ECh) [Reset = 00000000h]

ITM Stimulus Port Register 123 is shown in Table 2-271.

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Table 2-271. ITM Stimulus Port Register 123 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.125 ITM Stimulus Port Register 124 (Offset = 1F0h) [Reset = 00000000h]

ITM Stimulus Port Register 124 is shown in Table 2-272.

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Table 2-272. ITM Stimulus Port Register 124 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.126 ITM Stimulus Port Register 125 (Offset = 1F4h) [Reset = 00000000h]

ITM Stimulus Port Register 125 is shown in Table 2-273.

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Table 2-273. ITM Stimulus Port Register 125 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.127 ITM Stimulus Port Register 126 (Offset = 1F8h) [Reset = 00000000h]

ITM Stimulus Port Register 126 is shown in Table 2-274.

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Table 2-274. ITM Stimulus Port Register 126 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.128 ITM Stimulus Port Register 127 (Offset = 1FCh) [Reset = 00000000h]

ITM Stimulus Port Register 127 is shown in Table 2-275.

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Table 2-275. ITM Stimulus Port Register 127 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.129 ITM Stimulus Port Register 128 (Offset = 200h) [Reset = 00000000h]

ITM Stimulus Port Register 128 is shown in Table 2-276.

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Table 2-276. ITM Stimulus Port Register 128 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.130 ITM Stimulus Port Register 129 (Offset = 204h) [Reset = 00000000h]

ITM Stimulus Port Register 129 is shown in Table 2-277.

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Table 2-277. ITM Stimulus Port Register 129 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.131 ITM Stimulus Port Register 130 (Offset = 208h) [Reset = 00000000h]

ITM Stimulus Port Register 130 is shown in Table 2-278.

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Table 2-278. ITM Stimulus Port Register 130 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.132 ITM Stimulus Port Register 131 (Offset = 20Ch) [Reset = 00000000h]

ITM Stimulus Port Register 131 is shown in Table 2-279.

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Table 2-279. ITM Stimulus Port Register 131 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.133 ITM Stimulus Port Register 132 (Offset = 210h) [Reset = 00000000h]

ITM Stimulus Port Register 132 is shown in Table 2-280.

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Table 2-280. ITM Stimulus Port Register 132 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.134 ITM Stimulus Port Register 133 (Offset = 214h) [Reset = 00000000h]

ITM Stimulus Port Register 133 is shown in Table 2-281.

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Table 2-281. ITM Stimulus Port Register 133 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.135 ITM Stimulus Port Register 134 (Offset = 218h) [Reset = 00000000h]

ITM Stimulus Port Register 134 is shown in Table 2-282.

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Table 2-282. ITM Stimulus Port Register 134 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.136 ITM Stimulus Port Register 135 (Offset = 21Ch) [Reset = 00000000h]

ITM Stimulus Port Register 135 is shown in Table 2-283.

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Table 2-283. ITM Stimulus Port Register 135 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.137 ITM Stimulus Port Register 136 (Offset = 220h) [Reset = 00000000h]

ITM Stimulus Port Register 136 is shown in Table 2-284.

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Table 2-284. ITM Stimulus Port Register 136 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.138 ITM Stimulus Port Register 137 (Offset = 224h) [Reset = 00000000h]

ITM Stimulus Port Register 137 is shown in Table 2-285.

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Table 2-285. ITM Stimulus Port Register 137 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.139 ITM Stimulus Port Register 138 (Offset = 228h) [Reset = 00000000h]

ITM Stimulus Port Register 138 is shown in Table 2-286.

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Table 2-286. ITM Stimulus Port Register 138 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.140 ITM Stimulus Port Register 139 (Offset = 22Ch) [Reset = 00000000h]

ITM Stimulus Port Register 139 is shown in Table 2-287.

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Table 2-287. ITM Stimulus Port Register 139 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.141 ITM Stimulus Port Register 140 (Offset = 230h) [Reset = 00000000h]

ITM Stimulus Port Register 140 is shown in Table 2-288.

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Table 2-288. ITM Stimulus Port Register 140 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.142 ITM Stimulus Port Register 141 (Offset = 234h) [Reset = 00000000h]

ITM Stimulus Port Register 141 is shown in Table 2-289.

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Table 2-289. ITM Stimulus Port Register 141 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.143 ITM Stimulus Port Register 142 (Offset = 238h) [Reset = 00000000h]

ITM Stimulus Port Register 142 is shown in Table 2-290.

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Table 2-290. ITM Stimulus Port Register 142 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.144 ITM Stimulus Port Register 143 (Offset = 23Ch) [Reset = 00000000h]

ITM Stimulus Port Register 143 is shown in Table 2-291.

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Table 2-291. ITM Stimulus Port Register 143 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.145 ITM Stimulus Port Register 144 (Offset = 240h) [Reset = 00000000h]

ITM Stimulus Port Register 144 is shown in Table 2-292.

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Table 2-292. ITM Stimulus Port Register 144 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.146 ITM Stimulus Port Register 145 (Offset = 244h) [Reset = 00000000h]

ITM Stimulus Port Register 145 is shown in Table 2-293.

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Table 2-293. ITM Stimulus Port Register 145 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.147 ITM Stimulus Port Register 146 (Offset = 248h) [Reset = 00000000h]

ITM Stimulus Port Register 146 is shown in Table 2-294.

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Table 2-294. ITM Stimulus Port Register 146 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.148 ITM Stimulus Port Register 147 (Offset = 24Ch) [Reset = 00000000h]

ITM Stimulus Port Register 147 is shown in Table 2-295.

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Table 2-295. ITM Stimulus Port Register 147 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.149 ITM Stimulus Port Register 148 (Offset = 250h) [Reset = 00000000h]

ITM Stimulus Port Register 148 is shown in Table 2-296.

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Table 2-296. ITM Stimulus Port Register 148 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.150 ITM Stimulus Port Register 149 (Offset = 254h) [Reset = 00000000h]

ITM Stimulus Port Register 149 is shown in Table 2-297.

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Table 2-297. ITM Stimulus Port Register 149 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.151 ITM Stimulus Port Register 150 (Offset = 258h) [Reset = 00000000h]

ITM Stimulus Port Register 150 is shown in Table 2-298.

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Table 2-298. ITM Stimulus Port Register 150 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.152 ITM Stimulus Port Register 151 (Offset = 25Ch) [Reset = 00000000h]

ITM Stimulus Port Register 151 is shown in Table 2-299.

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Table 2-299. ITM Stimulus Port Register 151 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.153 ITM Stimulus Port Register 152 (Offset = 260h) [Reset = 00000000h]

ITM Stimulus Port Register 152 is shown in Table 2-300.

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Table 2-300. ITM Stimulus Port Register 152 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.154 ITM Stimulus Port Register 153 (Offset = 264h) [Reset = 00000000h]

ITM Stimulus Port Register 153 is shown in Table 2-301.

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Table 2-301. ITM Stimulus Port Register 153 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.155 ITM Stimulus Port Register 154 (Offset = 268h) [Reset = 00000000h]

ITM Stimulus Port Register 154 is shown in Table 2-302.

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Table 2-302. ITM Stimulus Port Register 154 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.156 ITM Stimulus Port Register 155 (Offset = 26Ch) [Reset = 00000000h]

ITM Stimulus Port Register 155 is shown in Table 2-303.

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Table 2-303. ITM Stimulus Port Register 155 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.157 ITM Stimulus Port Register 156 (Offset = 270h) [Reset = 00000000h]

ITM Stimulus Port Register 156 is shown in Table 2-304.

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Table 2-304. ITM Stimulus Port Register 156 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.158 ITM Stimulus Port Register 157 (Offset = 274h) [Reset = 00000000h]

ITM Stimulus Port Register 157 is shown in Table 2-305.

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Table 2-305. ITM Stimulus Port Register 157 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.159 ITM Stimulus Port Register 158 (Offset = 278h) [Reset = 00000000h]

ITM Stimulus Port Register 158 is shown in Table 2-306.

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Table 2-306. ITM Stimulus Port Register 158 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.160 ITM Stimulus Port Register 159 (Offset = 27Ch) [Reset = 00000000h]

ITM Stimulus Port Register 159 is shown in Table 2-307.

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Table 2-307. ITM Stimulus Port Register 159 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.161 ITM Stimulus Port Register 160 (Offset = 280h) [Reset = 00000000h]

ITM Stimulus Port Register 160 is shown in Table 2-308.

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Table 2-308. ITM Stimulus Port Register 160 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.162 ITM Stimulus Port Register 161 (Offset = 284h) [Reset = 00000000h]

ITM Stimulus Port Register 161 is shown in Table 2-309.

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Table 2-309. ITM Stimulus Port Register 161 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.163 ITM Stimulus Port Register 162 (Offset = 288h) [Reset = 00000000h]

ITM Stimulus Port Register 162 is shown in Table 2-310.

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Table 2-310. ITM Stimulus Port Register 162 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.164 ITM Stimulus Port Register 163 (Offset = 28Ch) [Reset = 00000000h]

ITM Stimulus Port Register 163 is shown in Table 2-311.

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Table 2-311. ITM Stimulus Port Register 163 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.165 ITM Stimulus Port Register 164 (Offset = 290h) [Reset = 00000000h]

ITM Stimulus Port Register 164 is shown in Table 2-312.

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Table 2-312. ITM Stimulus Port Register 164 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.166 ITM Stimulus Port Register 165 (Offset = 294h) [Reset = 00000000h]

ITM Stimulus Port Register 165 is shown in Table 2-313.

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Table 2-313. ITM Stimulus Port Register 165 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.167 ITM Stimulus Port Register 166 (Offset = 298h) [Reset = 00000000h]

ITM Stimulus Port Register 166 is shown in Table 2-314.

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Table 2-314. ITM Stimulus Port Register 166 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.168 ITM Stimulus Port Register 167 (Offset = 29Ch) [Reset = 00000000h]

ITM Stimulus Port Register 167 is shown in Table 2-315.

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Table 2-315. ITM Stimulus Port Register 167 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.169 ITM Stimulus Port Register 168 (Offset = 2A0h) [Reset = 00000000h]

ITM Stimulus Port Register 168 is shown in Table 2-316.

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Table 2-316. ITM Stimulus Port Register 168 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.170 ITM Stimulus Port Register 169 (Offset = 2A4h) [Reset = 00000000h]

ITM Stimulus Port Register 169 is shown in Table 2-317.

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Table 2-317. ITM Stimulus Port Register 169 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.171 ITM Stimulus Port Register 170 (Offset = 2A8h) [Reset = 00000000h]

ITM Stimulus Port Register 170 is shown in Table 2-318.

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Table 2-318. ITM Stimulus Port Register 170 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.172 ITM Stimulus Port Register 171 (Offset = 2ACh) [Reset = 00000000h]

ITM Stimulus Port Register 171 is shown in Table 2-319.

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Table 2-319. ITM Stimulus Port Register 171 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.173 ITM Stimulus Port Register 172 (Offset = 2B0h) [Reset = 00000000h]

ITM Stimulus Port Register 172 is shown in Table 2-320.

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Table 2-320. ITM Stimulus Port Register 172 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.174 ITM Stimulus Port Register 173 (Offset = 2B4h) [Reset = 00000000h]

ITM Stimulus Port Register 173 is shown in Table 2-321.

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Table 2-321. ITM Stimulus Port Register 173 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.175 ITM Stimulus Port Register 174 (Offset = 2B8h) [Reset = 00000000h]

ITM Stimulus Port Register 174 is shown in Table 2-322.

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Table 2-322. ITM Stimulus Port Register 174 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.176 ITM Stimulus Port Register 175 (Offset = 2BCh) [Reset = 00000000h]

ITM Stimulus Port Register 175 is shown in Table 2-323.

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Table 2-323. ITM Stimulus Port Register 175 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.177 ITM Stimulus Port Register 176 (Offset = 2C0h) [Reset = 00000000h]

ITM Stimulus Port Register 176 is shown in Table 2-324.

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Table 2-324. ITM Stimulus Port Register 176 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.178 ITM Stimulus Port Register 177 (Offset = 2C4h) [Reset = 00000000h]

ITM Stimulus Port Register 177 is shown in Table 2-325.

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Table 2-325. ITM Stimulus Port Register 177 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.179 ITM Stimulus Port Register 178 (Offset = 2C8h) [Reset = 00000000h]

ITM Stimulus Port Register 178 is shown in Table 2-326.

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Table 2-326. ITM Stimulus Port Register 178 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.180 ITM Stimulus Port Register 179 (Offset = 2CCh) [Reset = 00000000h]

ITM Stimulus Port Register 179 is shown in Table 2-327.

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Table 2-327. ITM Stimulus Port Register 179 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.181 ITM Stimulus Port Register 180 (Offset = 2D0h) [Reset = 00000000h]

ITM Stimulus Port Register 180 is shown in Table 2-328.

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Table 2-328. ITM Stimulus Port Register 180 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.182 ITM Stimulus Port Register 181 (Offset = 2D4h) [Reset = 00000000h]

ITM Stimulus Port Register 181 is shown in Table 2-329.

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Table 2-329. ITM Stimulus Port Register 181 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.183 ITM Stimulus Port Register 182 (Offset = 2D8h) [Reset = 00000000h]

ITM Stimulus Port Register 182 is shown in Table 2-330.

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Table 2-330. ITM Stimulus Port Register 182 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.184 ITM Stimulus Port Register 183 (Offset = 2DCh) [Reset = 00000000h]

ITM Stimulus Port Register 183 is shown in Table 2-331.

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Table 2-331. ITM Stimulus Port Register 183 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.185 ITM Stimulus Port Register 184 (Offset = 2E0h) [Reset = 00000000h]

ITM Stimulus Port Register 184 is shown in Table 2-332.

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Table 2-332. ITM Stimulus Port Register 184 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.186 ITM Stimulus Port Register 185 (Offset = 2E4h) [Reset = 00000000h]

ITM Stimulus Port Register 185 is shown in Table 2-333.

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Table 2-333. ITM Stimulus Port Register 185 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.187 ITM Stimulus Port Register 186 (Offset = 2E8h) [Reset = 00000000h]

ITM Stimulus Port Register 186 is shown in Table 2-334.

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Table 2-334. ITM Stimulus Port Register 186 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.188 ITM Stimulus Port Register 187 (Offset = 2ECh) [Reset = 00000000h]

ITM Stimulus Port Register 187 is shown in Table 2-335.

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Table 2-335. ITM Stimulus Port Register 187 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.189 ITM Stimulus Port Register 188 (Offset = 2F0h) [Reset = 00000000h]

ITM Stimulus Port Register 188 is shown in Table 2-336.

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Table 2-336. ITM Stimulus Port Register 188 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.190 ITM Stimulus Port Register 189 (Offset = 2F4h) [Reset = 00000000h]

ITM Stimulus Port Register 189 is shown in Table 2-337.

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Table 2-337. ITM Stimulus Port Register 189 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.191 ITM Stimulus Port Register 190 (Offset = 2F8h) [Reset = 00000000h]

ITM Stimulus Port Register 190 is shown in Table 2-338.

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Table 2-338. ITM Stimulus Port Register 190 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.192 ITM Stimulus Port Register 191 (Offset = 2FCh) [Reset = 00000000h]

ITM Stimulus Port Register 191 is shown in Table 2-339.

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Table 2-339. ITM Stimulus Port Register 191 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.193 ITM Stimulus Port Register 192 (Offset = 300h) [Reset = 00000000h]

ITM Stimulus Port Register 192 is shown in Table 2-340.

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Table 2-340. ITM Stimulus Port Register 192 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.194 ITM Stimulus Port Register 193 (Offset = 304h) [Reset = 00000000h]

ITM Stimulus Port Register 193 is shown in Table 2-341.

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Table 2-341. ITM Stimulus Port Register 193 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.195 ITM Stimulus Port Register 194 (Offset = 308h) [Reset = 00000000h]

ITM Stimulus Port Register 194 is shown in Table 2-342.

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Table 2-342. ITM Stimulus Port Register 194 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.196 ITM Stimulus Port Register 195 (Offset = 30Ch) [Reset = 00000000h]

ITM Stimulus Port Register 195 is shown in Table 2-343.

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Table 2-343. ITM Stimulus Port Register 195 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.197 ITM Stimulus Port Register 196 (Offset = 310h) [Reset = 00000000h]

ITM Stimulus Port Register 196 is shown in Table 2-344.

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Table 2-344. ITM Stimulus Port Register 196 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.198 ITM Stimulus Port Register 197 (Offset = 314h) [Reset = 00000000h]

ITM Stimulus Port Register 197 is shown in Table 2-345.

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Table 2-345. ITM Stimulus Port Register 197 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.199 ITM Stimulus Port Register 198 (Offset = 318h) [Reset = 00000000h]

ITM Stimulus Port Register 198 is shown in Table 2-346.

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Table 2-346. ITM Stimulus Port Register 198 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.200 ITM Stimulus Port Register 199 (Offset = 31Ch) [Reset = 00000000h]

ITM Stimulus Port Register 199 is shown in Table 2-347.

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Table 2-347. ITM Stimulus Port Register 199 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.201 ITM Stimulus Port Register 200 (Offset = 320h) [Reset = 00000000h]

ITM Stimulus Port Register 200 is shown in Table 2-348.

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Table 2-348. ITM Stimulus Port Register 200 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.202 ITM Stimulus Port Register 201 (Offset = 324h) [Reset = 00000000h]

ITM Stimulus Port Register 201 is shown in Table 2-349.

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Table 2-349. ITM Stimulus Port Register 201 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.203 ITM Stimulus Port Register 202 (Offset = 328h) [Reset = 00000000h]

ITM Stimulus Port Register 202 is shown in Table 2-350.

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Table 2-350. ITM Stimulus Port Register 202 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.204 ITM Stimulus Port Register 203 (Offset = 32Ch) [Reset = 00000000h]

ITM Stimulus Port Register 203 is shown in Table 2-351.

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Provides the interface for generating Instrumentation packets

Table 2-351. ITM Stimulus Port Register 203 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.205 ITM Stimulus Port Register 204 (Offset = 330h) [Reset = 00000000h]

ITM Stimulus Port Register 204 is shown in Table 2-352.

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Table 2-352. ITM Stimulus Port Register 204 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.206 ITM Stimulus Port Register 205 (Offset = 334h) [Reset = 00000000h]

ITM Stimulus Port Register 205 is shown in Table 2-353.

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Table 2-353. ITM Stimulus Port Register 205 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.207 ITM Stimulus Port Register 206 (Offset = 338h) [Reset = 00000000h]

ITM Stimulus Port Register 206 is shown in Table 2-354.

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Table 2-354. ITM Stimulus Port Register 206 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.208 ITM Stimulus Port Register 207 (Offset = 33Ch) [Reset = 00000000h]

ITM Stimulus Port Register 207 is shown in Table 2-355.

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Table 2-355. ITM Stimulus Port Register 207 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.209 ITM Stimulus Port Register 208 (Offset = 340h) [Reset = 00000000h]

ITM Stimulus Port Register 208 is shown in Table 2-356.

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Provides the interface for generating Instrumentation packets

Table 2-356. ITM Stimulus Port Register 208 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.210 ITM Stimulus Port Register 209 (Offset = 344h) [Reset = 00000000h]

ITM Stimulus Port Register 209 is shown in Table 2-357.

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Table 2-357. ITM Stimulus Port Register 209 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.211 ITM Stimulus Port Register 210 (Offset = 348h) [Reset = 00000000h]

ITM Stimulus Port Register 210 is shown in Table 2-358.

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Table 2-358. ITM Stimulus Port Register 210 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.212 ITM Stimulus Port Register 211 (Offset = 34Ch) [Reset = 00000000h]

ITM Stimulus Port Register 211 is shown in Table 2-359.

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Provides the interface for generating Instrumentation packets

Table 2-359. ITM Stimulus Port Register 211 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.213 ITM Stimulus Port Register 212 (Offset = 350h) [Reset = 00000000h]

ITM Stimulus Port Register 212 is shown in Table 2-360.

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Table 2-360. ITM Stimulus Port Register 212 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.214 ITM Stimulus Port Register 213 (Offset = 354h) [Reset = 00000000h]

ITM Stimulus Port Register 213 is shown in Table 2-361.

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Table 2-361. ITM Stimulus Port Register 213 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.215 ITM Stimulus Port Register 214 (Offset = 358h) [Reset = 00000000h]

ITM Stimulus Port Register 214 is shown in Table 2-362.

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Provides the interface for generating Instrumentation packets

Table 2-362. ITM Stimulus Port Register 214 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.216 ITM Stimulus Port Register 215 (Offset = 35Ch) [Reset = 00000000h]

ITM Stimulus Port Register 215 is shown in Table 2-363.

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Provides the interface for generating Instrumentation packets

Table 2-363. ITM Stimulus Port Register 215 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.217 ITM Stimulus Port Register 216 (Offset = 360h) [Reset = 00000000h]

ITM Stimulus Port Register 216 is shown in Table 2-364.

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Table 2-364. ITM Stimulus Port Register 216 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.218 ITM Stimulus Port Register 217 (Offset = 364h) [Reset = 00000000h]

ITM Stimulus Port Register 217 is shown in Table 2-365.

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Table 2-365. ITM Stimulus Port Register 217 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.219 ITM Stimulus Port Register 218 (Offset = 368h) [Reset = 00000000h]

ITM Stimulus Port Register 218 is shown in Table 2-366.

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Table 2-366. ITM Stimulus Port Register 218 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.220 ITM Stimulus Port Register 219 (Offset = 36Ch) [Reset = 00000000h]

ITM Stimulus Port Register 219 is shown in Table 2-367.

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Provides the interface for generating Instrumentation packets

Table 2-367. ITM Stimulus Port Register 219 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.221 ITM Stimulus Port Register 220 (Offset = 370h) [Reset = 00000000h]

ITM Stimulus Port Register 220 is shown in Table 2-368.

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Provides the interface for generating Instrumentation packets

Table 2-368. ITM Stimulus Port Register 220 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.222 ITM Stimulus Port Register 221 (Offset = 374h) [Reset = 00000000h]

ITM Stimulus Port Register 221 is shown in Table 2-369.

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Provides the interface for generating Instrumentation packets

Table 2-369. ITM Stimulus Port Register 221 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.223 ITM Stimulus Port Register 222 (Offset = 378h) [Reset = 00000000h]

ITM Stimulus Port Register 222 is shown in Table 2-370.

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Provides the interface for generating Instrumentation packets

Table 2-370. ITM Stimulus Port Register 222 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.224 ITM Stimulus Port Register 223 (Offset = 37Ch) [Reset = 00000000h]

ITM Stimulus Port Register 223 is shown in Table 2-371.

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Provides the interface for generating Instrumentation packets

Table 2-371. ITM Stimulus Port Register 223 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.225 ITM Stimulus Port Register 224 (Offset = 380h) [Reset = 00000000h]

ITM Stimulus Port Register 224 is shown in Table 2-372.

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Provides the interface for generating Instrumentation packets

Table 2-372. ITM Stimulus Port Register 224 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.226 ITM Stimulus Port Register 225 (Offset = 384h) [Reset = 00000000h]

ITM Stimulus Port Register 225 is shown in Table 2-373.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-373. ITM Stimulus Port Register 225 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.227 ITM Stimulus Port Register 226 (Offset = 388h) [Reset = 00000000h]

ITM Stimulus Port Register 226 is shown in Table 2-374.

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Provides the interface for generating Instrumentation packets

Table 2-374. ITM Stimulus Port Register 226 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.228 ITM Stimulus Port Register 227 (Offset = 38Ch) [Reset = 00000000h]

ITM Stimulus Port Register 227 is shown in Table 2-375.

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Provides the interface for generating Instrumentation packets

Table 2-375. ITM Stimulus Port Register 227 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.229 ITM Stimulus Port Register 228 (Offset = 390h) [Reset = 00000000h]

ITM Stimulus Port Register 228 is shown in Table 2-376.

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Provides the interface for generating Instrumentation packets

Table 2-376. ITM Stimulus Port Register 228 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.230 ITM Stimulus Port Register 229 (Offset = 394h) [Reset = 00000000h]

ITM Stimulus Port Register 229 is shown in Table 2-377.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-377. ITM Stimulus Port Register 229 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.231 ITM Stimulus Port Register 230 (Offset = 398h) [Reset = 00000000h]

ITM Stimulus Port Register 230 is shown in Table 2-378.

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Provides the interface for generating Instrumentation packets

Table 2-378. ITM Stimulus Port Register 230 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.232 ITM Stimulus Port Register 231 (Offset = 39Ch) [Reset = 00000000h]

ITM Stimulus Port Register 231 is shown in Table 2-379.

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Provides the interface for generating Instrumentation packets

Table 2-379. ITM Stimulus Port Register 231 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.233 ITM Stimulus Port Register 232 (Offset = 3A0h) [Reset = 00000000h]

ITM Stimulus Port Register 232 is shown in Table 2-380.

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Provides the interface for generating Instrumentation packets

Table 2-380. ITM Stimulus Port Register 232 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.234 ITM Stimulus Port Register 233 (Offset = 3A4h) [Reset = 00000000h]

ITM Stimulus Port Register 233 is shown in Table 2-381.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-381. ITM Stimulus Port Register 233 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.235 ITM Stimulus Port Register 234 (Offset = 3A8h) [Reset = 00000000h]

ITM Stimulus Port Register 234 is shown in Table 2-382.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-382. ITM Stimulus Port Register 234 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.236 ITM Stimulus Port Register 235 (Offset = 3ACh) [Reset = 00000000h]

ITM Stimulus Port Register 235 is shown in Table 2-383.

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Provides the interface for generating Instrumentation packets

Table 2-383. ITM Stimulus Port Register 235 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.237 ITM Stimulus Port Register 236 (Offset = 3B0h) [Reset = 00000000h]

ITM Stimulus Port Register 236 is shown in Table 2-384.

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Provides the interface for generating Instrumentation packets

Table 2-384. ITM Stimulus Port Register 236 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.238 ITM Stimulus Port Register 237 (Offset = 3B4h) [Reset = 00000000h]

ITM Stimulus Port Register 237 is shown in Table 2-385.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-385. ITM Stimulus Port Register 237 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.239 ITM Stimulus Port Register 238 (Offset = 3B8h) [Reset = 00000000h]

ITM Stimulus Port Register 238 is shown in Table 2-386.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-386. ITM Stimulus Port Register 238 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.240 ITM Stimulus Port Register 239 (Offset = 3BCh) [Reset = 00000000h]

ITM Stimulus Port Register 239 is shown in Table 2-387.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-387. ITM Stimulus Port Register 239 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.241 ITM Stimulus Port Register 240 (Offset = 3C0h) [Reset = 00000000h]

ITM Stimulus Port Register 240 is shown in Table 2-388.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-388. ITM Stimulus Port Register 240 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.242 ITM Stimulus Port Register 241 (Offset = 3C4h) [Reset = 00000000h]

ITM Stimulus Port Register 241 is shown in Table 2-389.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-389. ITM Stimulus Port Register 241 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.243 ITM Stimulus Port Register 242 (Offset = 3C8h) [Reset = 00000000h]

ITM Stimulus Port Register 242 is shown in Table 2-390.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-390. ITM Stimulus Port Register 242 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.244 ITM Stimulus Port Register 243 (Offset = 3CCh) [Reset = 00000000h]

ITM Stimulus Port Register 243 is shown in Table 2-391.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-391. ITM Stimulus Port Register 243 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.245 ITM Stimulus Port Register 244 (Offset = 3D0h) [Reset = 00000000h]

ITM Stimulus Port Register 244 is shown in Table 2-392.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-392. ITM Stimulus Port Register 244 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.246 ITM Stimulus Port Register 245 (Offset = 3D4h) [Reset = 00000000h]

ITM Stimulus Port Register 245 is shown in Table 2-393.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-393. ITM Stimulus Port Register 245 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.247 ITM Stimulus Port Register 246 (Offset = 3D8h) [Reset = 00000000h]

ITM Stimulus Port Register 246 is shown in Table 2-394.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-394. ITM Stimulus Port Register 246 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.248 ITM Stimulus Port Register 247 (Offset = 3DCh) [Reset = 00000000h]

ITM Stimulus Port Register 247 is shown in Table 2-395.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-395. ITM Stimulus Port Register 247 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.249 ITM Stimulus Port Register 248 (Offset = 3E0h) [Reset = 00000000h]

ITM Stimulus Port Register 248 is shown in Table 2-396.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-396. ITM Stimulus Port Register 248 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.250 ITM Stimulus Port Register 249 (Offset = 3E4h) [Reset = 00000000h]

ITM Stimulus Port Register 249 is shown in Table 2-397.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-397. ITM Stimulus Port Register 249 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.251 ITM Stimulus Port Register 250 (Offset = 3E8h) [Reset = 00000000h]

ITM Stimulus Port Register 250 is shown in Table 2-398.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-398. ITM Stimulus Port Register 250 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.252 ITM Stimulus Port Register 251 (Offset = 3ECh) [Reset = 00000000h]

ITM Stimulus Port Register 251 is shown in Table 2-399.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-399. ITM Stimulus Port Register 251 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.253 ITM Stimulus Port Register 252 (Offset = 3F0h) [Reset = 00000000h]

ITM Stimulus Port Register 252 is shown in Table 2-400.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-400. ITM Stimulus Port Register 252 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.254 ITM Stimulus Port Register 253 (Offset = 3F4h) [Reset = 00000000h]

ITM Stimulus Port Register 253 is shown in Table 2-401.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-401. ITM Stimulus Port Register 253 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.255 ITM Stimulus Port Register 254 (Offset = 3F8h) [Reset = 00000000h]

ITM Stimulus Port Register 254 is shown in Table 2-402.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-402. ITM Stimulus Port Register 254 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.256 ITM Stimulus Port Register 255 (Offset = 3FCh) [Reset = 00000000h]

ITM Stimulus Port Register 255 is shown in Table 2-403.

Return to the Summary Table.

Provides the interface for generating Instrumentation packets

Table 2-403. ITM Stimulus Port Register 255 Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	Disabled	R	0h	Indicates whether the Stimulus Port is enabled or disabled
0	FIFO ready	R	0h	Indicates whether the Stimulus Port can accept data
31-0	Stimulus data	W	0h	Data to write to the Stimulus Port FIFO, for forwarding as an Instrumentation packet. The size of write access determines the type of Instrumentation packet generated.

2.7.9.257 ITM Trace Enable Register 0 (Offset = E00h) [Reset = 00000000h]

ITM Trace Enable Register 0 is shown in Table 2-404.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-404. ITM Trace Enable Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.258 ITM Trace Enable Register 1 (Offset = E04h) [Reset = 00000000h]

ITM Trace Enable Register 1 is shown in Table 2-405.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-405. ITM Trace Enable Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.259 ITM Trace Enable Register 2 (Offset = E08h) [Reset = 00000000h]

ITM Trace Enable Register 2 is shown in Table 2-406.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-406. ITM Trace Enable Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.260 ITM Trace Enable Register 3 (Offset = E0Ch) [Reset = 00000000h]

ITM Trace Enable Register 3 is shown in Table 2-407.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-407. ITM Trace Enable Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.261 ITM Trace Enable Register 4 (Offset = E10h) [Reset = 00000000h]

ITM Trace Enable Register 4 is shown in Table 2-408.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-408. ITM Trace Enable Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.262 ITM Trace Enable Register 5 (Offset = E14h) [Reset = 00000000h]

ITM Trace Enable Register 5 is shown in Table 2-409.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-409. ITM Trace Enable Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.263 ITM Trace Enable Register 6 (Offset = E18h) [Reset = 00000000h]

ITM Trace Enable Register 6 is shown in Table 2-410.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-410. ITM Trace Enable Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.264 ITM Trace Enable Register 7 (Offset = E1Ch) [Reset = 00000000h]

ITM Trace Enable Register 7 is shown in Table 2-411.

Return to the Summary Table.

Provide an individual enable bit for each ITM_STIM register

Table 2-411. ITM Trace Enable Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Stimulus enable	R/W	0h	For STIMENA[m] in ITM_TER*n, controls whether ITM_STIM(32*n + m) is enabled

2.7.9.265 ITM Trace Privilege Register (Offset = E40h) [Reset = 00000000h]

ITM Trace Privilege Register is shown in Table 2-412.

Return to the Summary Table.

Controls which stimulus ports can be accessed by unprivileged code

Table 2-412. ITM Trace Privilege Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved, RES0
3-0	Privilege mask	R/W	0h	Bit mask to enable tracing on ITM stimulus ports

2.7.9.266 ITM Trace Control Register (Offset = E80h) [Reset = 00000000h]

ITM Trace Control Register is shown in Table 2-413.

Return to the Summary Table.

Configures and controls transfers through the ITM interface

Table 2-413. ITM Trace Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved, RES0
23	ITM busy	R	0h	Indicates whether the ITM is currently processing events
22-16	Trace bus identity	R/W	0h	Identifier for multi-source trace stream formatting. If multi-source trace is in use, the debugger must write a unique non-zero trace ID value to this field
15-12	RESERVED	R	0h	Reserved, RES0
11-10	Global timestamp frequency	R/W	0h	Defines how often the ITM generates a global timestamp, based on the global timestamp clock frequency, or disables generation of global timestamps
9-8	Timestamp prescale	R/W	0h	Local timestamp prescaler, used with the trace packet reference clock
7-6	RESERVED	R	0h	Reserved, RES0
5	Stall enable	R/W	0h	Stall the PE to guarantee delivery of Data Trace packets.
4	SWO enable	R/W	0h	Enables asynchronous clocking of the timestamp counter
3	Transmit enable	R/W	0h	Enables forwarding of hardware event packet from the DWT unit to the ITM for output to the TPIU
2	Synchronization enable	R/W	0h	Enables Synchronization packet transmission for a synchronous TPIU
1	Timestamp enable	R/W	0h	Enables Local timestamp generation
0	ITM enable	R/W	0h	Enables the ITM

2.7.9.267 INT_ATREADY Register (Offset = EF0h) [Reset = 00000000h]

INT_ATREADY is shown in Table 2-414.

Return to the Summary Table.

Integration Mode: Read ATB Ready

Table 2-414. INT_ATREADY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	AFVALID	R	0h	A read of this bit returns the value of AFVALID
0	ATREADY	R	0h	A read of this bit returns the value of ATREADY

2.7.9.268 INT_ATVALID Register (Offset = EF8h) [Reset = 00000000h]

INT_ATVALID is shown in Table 2-415.

Return to the Summary Table.

Integration Mode: Write ATB Valid

Table 2-415. INT_ATVALID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved, RES0
1	AFREADY	W	0h	A write to this bit gives the value of AFREADY
0	ATVALID	W	0h	A write to this bit gives the value of ATVALID

2.7.9.269 ITM_ITCTRL Register (Offset = F00h) [Reset = 00000000h]

ITM_ITCTRL is shown in Table 2-416.

Return to the Summary Table.

Integration Mode Control Register

Table 2-416. ITM_ITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved, RES0
0	Integration mode enable bit	R/W	0h	Integration mode enable bit - The possible values are: 0 - The trace unit is not in integration mode. 1 - The trace unit is in integration mode. This mode enables: A debug agent to perform topology detection. SoC test software to perform integration testing.

2.7.9.270 ITM Device Architecture Register (Offset = FBCh) [Reset = 47701A01h]

ITM Device Architecture Register is shown in Table 2-417.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-417. ITM Device Architecture Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	Architect	R	23Bh	Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.
20	DEVARCH Present	R	1h	Defines that the DEVARCH register is present
19-16	Revision	R	0h	Defines the architecture revision of the component
15-12	Architecture Version	R	1h	Defines the architecture version of the component
11-0	Architecture Part	R	A01h	Defines the architecture of the component

2.7.9.271 ITM Device Type Register (Offset = FCCh) [Reset = 00000043h]

ITM Device Type Register is shown in Table 2-418.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-418. ITM Device Type Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Sub-type	R	4h	Component sub-type
3-0	Major type	R	3h	Component major type

2.7.9.272 ITM Peripheral Identification Register 4 (Offset = FD0h) [Reset = 00000004h]

ITM Peripheral Identification Register 4 is shown in Table 2-419.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-419. ITM Peripheral Identification Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	4KB count	R	0h	See CoreSight Architecture Specification
3-0	JEP106 continuation code	R	4h	See CoreSight Architecture Specification

2.7.9.273 ITM Peripheral Identification Register 5 (Offset = FD4h) [Reset = 00000000h]

ITM Peripheral Identification Register 5 is shown in Table 2-420.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-420. ITM Peripheral Identification Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

2.7.9.274 ITM Peripheral Identification Register 6 (Offset = FD8h) [Reset = 00000000h]

ITM Peripheral Identification Register 6 is shown in Table 2-421.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-421. ITM Peripheral Identification Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

2.7.9.275 ITM Peripheral Identification Register 7 (Offset = FDCh) [Reset = 00000000h]

ITM Peripheral Identification Register 7 is shown in Table 2-422.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-422. ITM Peripheral Identification Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved, RES0

2.7.9.276 ITM Peripheral Identification Register 0 (Offset = FE0h) [Reset = 00000021h]

ITM Peripheral Identification Register 0 is shown in Table 2-423.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-423. ITM Peripheral Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	Part number bits [7:0]	R	21h	See CoreSight Architecture Specification

2.7.9.277 ITM Peripheral Identification Register 1 (Offset = FE4h) [Reset = 000000BDh]

ITM Peripheral Identification Register 1 is shown in Table 2-424.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-424. ITM Peripheral Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	JEP106 identification code bits [3:0]	R	Bh	See CoreSight Architecture Specification
3-0	Part number bits [11:8]	R	Dh	See CoreSight Architecture Specification

2.7.9.278 ITM Peripheral Identification Register 2 (Offset = FE8h) [Reset = 0000000Bh]

ITM Peripheral Identification Register 2 is shown in Table 2-425.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-425. ITM Peripheral Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	Component revision	R	0h	See CoreSight Architecture Specification
3	JEDEC assignee value is used	R	1h	See CoreSight Architecture Specification
2-0	JEP106 identification code bits [6:4]	R	3h	See CoreSight Architecture Specification

2.7.9.279 ITM Peripheral Identification Register 3 (Offset = FECh) [Reset = 00000000h]

ITM Peripheral Identification Register 3 is shown in Table 2-426.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-426. ITM Peripheral Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	RevAnd	R	0h	See CoreSight Architecture Specification
3-0	Customer Modified	R	0h	See CoreSight Architecture Specification

2.7.9.280 ITM Component Identification Register 0 (Offset = FF0h) [Reset = 0000000Dh]

ITM Component Identification Register 0 is shown in Table 2-427.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-427. ITM Component Identification Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	Dh	See CoreSight Architecture Specification

2.7.9.281 ITM Component Identification Register 1 (Offset = FF4h) [Reset = 00000090h]

ITM Component Identification Register 1 is shown in Table 2-428.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-428. ITM Component Identification Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-4	CoreSight component class	R	9h	See CoreSight Architecture Specification
3-0	CoreSight component identification preamble	R	0h	See CoreSight Architecture Specification

2.7.9.282 ITM Component Identification Register 2 (Offset = FF8h) [Reset = 00000005h]

ITM Component Identification Register 2 is shown in Table 2-429.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-429. ITM Component Identification Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	5h	See CoreSight Architecture Specification

2.7.9.283 ITM Component Identification Register 3 (Offset = FFCh) [Reset = 000000B1h]

ITM Component Identification Register 3 is shown in Table 2-430.

Return to the Summary Table.

Provides CoreSight discovery information for the ITM

Table 2-430. ITM Component Identification Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved, RES0
7-0	CoreSight component identification preamble	R	B1h	See CoreSight Architecture Specification

2.7.10 MPU Registers

Table 2-431 lists the memory-mapped registers for the MPU registers. All register offset addresses not listed in Table 2-431 should be considered as reserved locations and the register contents should not be modified.

Table 2-431. MPU Registers

Offset	Acronym	Register Name	Section
0h	MPU_TYPE	The MPU Type Register indicates how many regions the MPU `FTSSS supports	Section 2.7.10.1
4h	MPU_CTRL	Enables the MPU and, when the MPU is enabled, controls whether the default memory map is enabled as a background region for privileged accesses, and whether the MPU is enabled for HardFaults, NMIs, and exception handlers when FAULTMASK is set to 1	Section 2.7.10.2
8h	MPU_RNR	Selects the region currently accessed by MPU_RBAR and MPU_RLAR	Section 2.7.10.3
Ch	MPU_RBAR	Provides indirect read and write access to the base address of the currently selected MPU region `FTSSS	Section 2.7.10.4
10h	MPU_RLAR	Provides indirect read and write access to the limit address of the currently selected MPU region `FTSSS	Section 2.7.10.5
14h	MPU_RBAR_A1	Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]:(1[1:0]) `FTSSS	Section 2.7.10.6
18h	MPU_RLAR_A1	Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(1[1:0]) `FTSSS	Section 2.7.10.7
1Ch	MPU_RBAR_A2	Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]:(2[1:0]) `FTSSS	Section 2.7.10.8
20h	MPU_RLAR_A2	Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(2[1:0]) `FTSSS	Section 2.7.10.9
24h	MPU_RBAR_A3	Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]:(3[1:0]) `FTSSS	Section 2.7.10.10
28h	MPU_RLAR_A3	Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(3[1:0]) `FTSSS	Section 2.7.10.11
30h	MPU_MAIR0	Along with MPU_MAIR1, provides the memory attribute encodings corresponding to the AttrIndex values	Section 2.7.10.12
34h	MPU_MAIR1	Along with MPU_MAIR0, provides the memory attribute encodings corresponding to the AttrIndex values	Section 2.7.10.13

Complex bit access types are encoded to fit into small table cells. Table 2-432 shows the codes that are used for access types in this section.

Table 2-432. MPU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.10.1 MPU_TYPE Register (Offset = 0h) [Reset = 00000000h]

MPU_TYPE is shown in Table 2-433.

Return to the Summary Table.

The MPU Type Register indicates how many regions the MPU `FTSSS supports

Table 2-433. MPU_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RES0	R	0h	Reserved, RES0
15-8	DREGION	R	8h	Number of regions supported by the MPU
7-1	RES0_1	R	0h	Reserved, RES0
0	SEPARATE	R	0h	Indicates support for separate instructions and data address regions

2.7.10.2 MPU_CTRL Register (Offset = 4h) [Reset = 00000000h]

MPU_CTRL is shown in Table 2-434.

Return to the Summary Table.

Enables the MPU and, when the MPU is enabled, controls whether the default memory map is enabled as a background region for privileged accesses, and whether the MPU is enabled for HardFaults, NMIs, and exception handlers when FAULTMASK is set to 1

Table 2-434. MPU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RES0	R	0h	Reserved, RES0
2	PRIVDEFENA	R/W	0h	Controls whether the default memory map is enabled for privileged software
1	HFNMIENA	R/W	0h	Controls whether handlers executing with priority less than 0 access memory with the MPU enabled or disabled. This applies to HardFaults, NMIs, and exception handlers when FAULTMASK is set to 1
0	ENABLE	R/W	0h	Enables the MPU

2.7.10.3 MPU_RNR Register (Offset = 8h) [Reset = 00000000h]

MPU_RNR is shown in Table 2-435.

Return to the Summary Table.

Selects the region currently accessed by MPU_RBAR and MPU_RLAR

Table 2-435. MPU_RNR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES0	R	Xh	Reserved, RES0
3	RES0_3	R	0h	Reserved, RES0
2-0	REGION	R/W	0h	Indicates the memory region accessed by MPU_RBAR and MPU_RLAR

2.7.10.4 MPU_RBAR Register (Offset = Ch) [Reset = 00000000h]

MPU_RBAR is shown in Table 2-436.

Return to the Summary Table.

Provides indirect read and write access to the base address of the currently selected MPU region `FTSSS

Table 2-436. MPU_RBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

2.7.10.5 MPU_RLAR Register (Offset = 10h) [Reset = 00000000h]

MPU_RLAR is shown in Table 2-437.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region `FTSSS

Table 2-437. MPU_RLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

2.7.10.6 MPU_RBAR_A1 Register (Offset = 14h) [Reset = 00000000h]

MPU_RBAR_A1 is shown in Table 2-438.

Return to the Summary Table.

Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]: (1[1:0]) `FTSSS

Table 2-438. MPU_RBAR_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

2.7.10.7 MPU_RLAR_A1 Register (Offset = 18h) [Reset = 00000000h]

MPU_RLAR_A1 is shown in Table 2-439.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(1[1:0]) `FTSSS

Table 2-439. MPU_RLAR_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

2.7.10.8 MPU_RBAR_A2 Register (Offset = 1Ch) [Reset = 00000000h]

MPU_RBAR_A2 is shown in Table 2-440.

Return to the Summary Table.

Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]: (2[1:0]) `FTSSS

Table 2-440. MPU_RBAR_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

2.7.10.9 MPU_RLAR_A2 Register (Offset = 20h) [Reset = 00000000h]

MPU_RLAR_A2 is shown in Table 2-441.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(2[1:0]) `FTSSS

Table 2-441. MPU_RLAR_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

2.7.10.10 MPU_RBAR_A3 Register (Offset = 24h) [Reset = 00000000h]

MPU_RBAR_A3 is shown in Table 2-442.

Return to the Summary Table.

Provides indirect read and write access to the base address of the MPU region selected by MPU_RNR[7:2]: (3[1:0]) `FTSSS

Table 2-442. MPU_RBAR_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BASE	R/W	Xh	Contains bits [31:5] of the lower inclusive limit of the selected MPU memory region. This value is zero extended to provide the base address to be checked against
4-3	SH	R/W	0h	Defines the Shareability domain of this region for Normal memory
2-1	AP	R/W	0h	Defines the access permissions for this region
0	XN	R/W	0h	Defines whether code can be executed from this region

2.7.10.11 MPU_RLAR_A3 Register (Offset = 28h) [Reset = 00000000h]

MPU_RLAR_A3 is shown in Table 2-443.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected MPU region selected by MPU_RNR[7:2]:(3[1:0]) `FTSSS

Table 2-443. MPU_RLAR_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LIMIT	R/W	Xh	Contains bits [31:5] of the upper inclusive limit of the selected MPU memory region. This value is postfixed with 0x1F to provide the limit address to be checked against
4	RES0	R	0h	Reserved, RES0
3-1	AttrIndx	R/W	0h	Associates a set of attributes in the MPU_MAIR0 and MPU_MAIR1 fields
0	EN	R/W	0h	Region enable

2.7.10.12 MPU_MAIR0 Register (Offset = 30h) [Reset = 00000000h]

MPU_MAIR0 is shown in Table 2-444.

Return to the Summary Table.

Along with MPU_MAIR1, provides the memory attribute encodings corresponding to the AttrIndex values

Table 2-444. MPU_MAIR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Attr3	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 3
23-16	Attr2	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 2
15-8	Attr1	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 1
7-0	Attr0	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 0

2.7.10.13 MPU_MAIR1 Register (Offset = 34h) [Reset = 00000000h]

MPU_MAIR1 is shown in Table 2-445.

Return to the Summary Table.

Along with MPU_MAIR0, provides the memory attribute encodings corresponding to the AttrIndex values

Table 2-445. MPU_MAIR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Attr7	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 7
23-16	Attr6	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 6
15-8	Attr5	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 5
7-0	Attr4	R/W	0h	Memory attribute encoding for MPU regions with an AttrIndex of 4

2.7.11 NVIC Registers

Table 2-446 lists the memory-mapped registers for the NVIC registers. All register offset addresses not listed in Table 2-446 should be considered as reserved locations and the register contents should not be modified.

Table 2-446. NVIC Registers

Offset	Acronym	Register Name	Section
0h	NVIC_ISER0	Enables or reads the enabled state of each group of 32 interrupts	Section 2.7.11.1
4h	NVIC_ISER1	Enables or reads the enabled state of each group of 32 interrupts	Section 2.7.11.2
80h	NVIC_ICER0	Clears or reads the enabled state of each group of 32 interrupts	Section 2.7.11.3
84h	NVIC_ICER1	Clears or reads the enabled state of each group of 32 interrupts	Section 2.7.11.4
100h	NVIC_ISPR0	Enables or reads the pending state of each group of 32 interrupts	Section 2.7.11.5
104h	NVIC_ISPR1	Enables or reads the pending state of each group of 32 interrupts	Section 2.7.11.6
180h	NVIC_ICPR0	Clears or reads the pending state of each group of 32 interrupts	Section 2.7.11.7
184h	NVIC_ICPR1	Clears or reads the pending state of each group of 32 interrupts	Section 2.7.11.8
200h	NVIC_IABR0	For each group of 32 interrupts, shows the active state of each interrupt	Section 2.7.11.9
204h	NVIC_IABR1	For each group of 32 interrupts, shows the active state of each interrupt	Section 2.7.11.10
280h	NVIC_ITNS0	For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state	Section 2.7.11.11
284h	NVIC_ITNS1	For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state	Section 2.7.11.12
300h	NVIC_IPR0	Sets or reads interrupt priorities	Section 2.7.11.13
304h	NVIC_IPR1	Sets or reads interrupt priorities	Section 2.7.11.14
308h	NVIC_IPR2	Sets or reads interrupt priorities	Section 2.7.11.15
30Ch	NVIC_IPR3	Sets or reads interrupt priorities	Section 2.7.11.16
310h	NVIC_IPR4	Sets or reads interrupt priorities	Section 2.7.11.17
314h	NVIC_IPR5	Sets or reads interrupt priorities	Section 2.7.11.18
318h	NVIC_IPR6	Sets or reads interrupt priorities	Section 2.7.11.19
31Ch	NVIC_IPR7	Sets or reads interrupt priorities	Section 2.7.11.20
320h	NVIC_IPR8	Sets or reads interrupt priorities	Section 2.7.11.21

Complex bit access types are encoded to fit into small table cells. Table 2-447 shows the codes that are used for access types in this section.

Table 2-447. NVIC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.11.1 NVIC_ISER0 Register (Offset = 0h) [Reset = 00000000h]

NVIC_ISER0 is shown in Table 2-448.

Return to the Summary Table.

Enables or reads the enabled state of each group of 32 interrupts

Table 2-448. NVIC_ISER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETENA	R	0h	For SETENA[m] in NVIC_ISER*n, indicates whether interrupt 32*n + m is enabled

2.7.11.2 NVIC_ISER1 Register (Offset = 4h) [Reset = 00000000h]

NVIC_ISER1 is shown in Table 2-449.

Return to the Summary Table.

Enables or reads the enabled state of each group of 32 interrupts

Table 2-449. NVIC_ISER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETENA	R	0h	For SETENA[m] in NVIC_ISER*n, indicates whether interrupt 32*n + m is enabled

2.7.11.3 NVIC_ICER0 Register (Offset = 80h) [Reset = 00000000h]

NVIC_ICER0 is shown in Table 2-450.

Return to the Summary Table.

Clears or reads the enabled state of each group of 32 interrupts

Table 2-450. NVIC_ICER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRENA	R	0h	For CLRENA[m] in NVIC_ICER*n, indicates whether interrupt 32*n + m is enabled

2.7.11.4 NVIC_ICER1 Register (Offset = 84h) [Reset = 00000000h]

NVIC_ICER1 is shown in Table 2-451.

Return to the Summary Table.

Clears or reads the enabled state of each group of 32 interrupts

Table 2-451. NVIC_ICER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRENA	R	0h	For CLRENA[m] in NVIC_ICER*n, indicates whether interrupt 32*n + m is enabled

2.7.11.5 NVIC_ISPR0 Register (Offset = 100h) [Reset = 00000000h]

NVIC_ISPR0 is shown in Table 2-452.

Return to the Summary Table.

Enables or reads the pending state of each group of 32 interrupts

Table 2-452. NVIC_ISPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETPEND	R	0h	For SETPEND[m] in NVIC_ISPR*n, indicates whether interrupt 32*n + m is pending

2.7.11.6 NVIC_ISPR1 Register (Offset = 104h) [Reset = 00000000h]

NVIC_ISPR1 is shown in Table 2-453.

Return to the Summary Table.

Enables or reads the pending state of each group of 32 interrupts

Table 2-453. NVIC_ISPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SETPEND	R	0h	For SETPEND[m] in NVIC_ISPR*n, indicates whether interrupt 32*n + m is pending

2.7.11.7 NVIC_ICPR0 Register (Offset = 180h) [Reset = 00000000h]

NVIC_ICPR0 is shown in Table 2-454.

Return to the Summary Table.

Clears or reads the pending state of each group of 32 interrupts

Table 2-454. NVIC_ICPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRPEND	R	0h	For CLRPEND[m] in NVIC_ICPR*n, indicates whether interrupt 32*n + m is pending

2.7.11.8 NVIC_ICPR1 Register (Offset = 184h) [Reset = 00000000h]

NVIC_ICPR1 is shown in Table 2-455.

Return to the Summary Table.

Clears or reads the pending state of each group of 32 interrupts

Table 2-455. NVIC_ICPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLRPEND	R	0h	For CLRPEND[m] in NVIC_ICPR*n, indicates whether interrupt 32*n + m is pending

2.7.11.9 NVIC_IABR0 Register (Offset = 200h) [Reset = 00000000h]

NVIC_IABR0 is shown in Table 2-456.

Return to the Summary Table.

For each group of 32 interrupts, shows the active state of each interrupt

Table 2-456. NVIC_IABR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ACTIVE	R	0h	For ACTIVE[m] in NVIC_IABR*n, indicates the active state for interrupt 32*n+m

2.7.11.10 NVIC_IABR1 Register (Offset = 204h) [Reset = 00000000h]

NVIC_IABR1 is shown in Table 2-457.

Return to the Summary Table.

For each group of 32 interrupts, shows the active state of each interrupt

Table 2-457. NVIC_IABR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ACTIVE	R	0h	For ACTIVE[m] in NVIC_IABR*n, indicates the active state for interrupt 32*n+m

2.7.11.11 NVIC_ITNS0 Register (Offset = 280h) [Reset = 00000000h]

NVIC_ITNS0 is shown in Table 2-458.

Return to the Summary Table.

For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state

Table 2-458. NVIC_ITNS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ITNS	R/W	0h	For ITNS[m] in NVIC_ITNS*n, `IAAMO the target Security state for interrupt 32*n+m

2.7.11.12 NVIC_ITNS1 Register (Offset = 284h) [Reset = 00000000h]

NVIC_ITNS1 is shown in Table 2-459.

Return to the Summary Table.

For each group of 32 interrupts, determines whether each interrupt targets Non-secure or Secure state

Table 2-459. NVIC_ITNS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ITNS	R/W	0h	For ITNS[m] in NVIC_ITNS*n, `IAAMO the target Security state for interrupt 32*n+m

2.7.11.13 NVIC_IPR0 Register (Offset = 300h) [Reset = 00000000h]

NVIC_IPR0 is shown in Table 2-460.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-460. NVIC_IPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.14 NVIC_IPR1 Register (Offset = 304h) [Reset = 00000000h]

NVIC_IPR1 is shown in Table 2-461.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-461. NVIC_IPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.15 NVIC_IPR2 Register (Offset = 308h) [Reset = 00000000h]

NVIC_IPR2 is shown in Table 2-462.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-462. NVIC_IPR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.16 NVIC_IPR3 Register (Offset = 30Ch) [Reset = 00000000h]

NVIC_IPR3 is shown in Table 2-463.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-463. NVIC_IPR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.17 NVIC_IPR4 Register (Offset = 310h) [Reset = 00000000h]

NVIC_IPR4 is shown in Table 2-464.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-464. NVIC_IPR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.18 NVIC_IPR5 Register (Offset = 314h) [Reset = 00000000h]

NVIC_IPR5 is shown in Table 2-465.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-465. NVIC_IPR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.19 NVIC_IPR6 Register (Offset = 318h) [Reset = 00000000h]

NVIC_IPR6 is shown in Table 2-466.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-466. NVIC_IPR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.20 NVIC_IPR7 Register (Offset = 31Ch) [Reset = 00000000h]

NVIC_IPR7 is shown in Table 2-467.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-467. NVIC_IPR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	PRI_N3	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
23-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.11.21 NVIC_IPR8 Register (Offset = 320h) [Reset = 00000000h]

NVIC_IPR8 is shown in Table 2-468.

Return to the Summary Table.

Sets or reads interrupt priorities

Table 2-468. NVIC_IPR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	PRI_N2	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+2, or is RES0 if the PE does not implement this interrupt
15-11	RESERVED	R	0h	Reserved
10-8	PRI_N1	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+1, or is RES0 if the PE does not implement this interrupt
7-3	RESERVED	R	0h	Reserved
2-0	PRI_N0	R	0h	For register NVIC_IPR*n, `IAAMO the priority of interrupt number 4*n+0, or is RES0 if the PE does not implement this interrupt

2.7.12 SAU Registers

Table 2-469 lists the memory-mapped registers for the SAU registers. All register offset addresses not listed in Table 2-469 should be considered as reserved locations and the register contents should not be modified.

Table 2-469. SAU Registers

Offset	Acronym	Register Name	Section
0h	SAU_CTRL	Allows enabling of the Security Attribution Unit	Section 2.7.12.1
4h	SAU_TYPE	Indicates the number of regions implemented by the Security Attribution Unit	Section 2.7.12.2
8h	SAU_RNR	Selects the region currently accessed by SAU_RBAR and SAU_RLAR	Section 2.7.12.3
Ch	SAU_RBAR	Provides indirect read and write access to the base address of the currently selected SAU region	Section 2.7.12.4
10h	SAU_RLAR	Provides indirect read and write access to the limit address of the currently selected SAU region	Section 2.7.12.5
14h	SFSR	Provides information about any security related faults	Section 2.7.12.6
18h	SFAR	Shows the address of the memory location that caused a Security violation	Section 2.7.12.7

Complex bit access types are encoded to fit into small table cells. Table 2-470 shows the codes that are used for access types in this section.

Table 2-470. SAU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.12.1 SAU_CTRL Register (Offset = 0h) [Reset = 00000000h]

SAU_CTRL is shown in Table 2-471.

Return to the Summary Table.

Allows enabling of the Security Attribution Unit

Table 2-471. SAU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RES0	R	0h	Reserved, RES0
1	ALLNS	R/W	0h	When SAU_CTRL.ENABLE is 0 this bit controls if the memory is marked as Non-secure or Secure
0	ENABLE	R/W	0h	Enables the SAU

2.7.12.2 SAU_TYPE Register (Offset = 4h) [Reset = 00000000h]

SAU_TYPE is shown in Table 2-472.

Return to the Summary Table.

Indicates the number of regions implemented by the Security Attribution Unit

Table 2-472. SAU_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	SREGION	R	4h	The number of implemented SAU regions

2.7.12.3 SAU_RNR Register (Offset = 8h) [Reset = 00000000h]

SAU_RNR is shown in Table 2-473.

Return to the Summary Table.

Selects the region currently accessed by SAU_RBAR and SAU_RLAR

Table 2-473. SAU_RNR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-0	REGION	R/W	0h	Indicates the SAU region accessed by SAU_RBAR and SAU_RLAR

2.7.12.4 SAU_RBAR Register (Offset = Ch) [Reset = 00000000h]

SAU_RBAR is shown in Table 2-474.

Return to the Summary Table.

Provides indirect read and write access to the base address of the currently selected SAU region

Table 2-474. SAU_RBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	BADDR	R/W	Xh	Holds bits [31:5] of the base address for the selected SAU region
4-0	RES0	R	0h	Reserved, RES0

2.7.12.5 SAU_RLAR Register (Offset = 10h) [Reset = 00000000h]

SAU_RLAR is shown in Table 2-475.

Return to the Summary Table.

Provides indirect read and write access to the limit address of the currently selected SAU region

Table 2-475. SAU_RLAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	LADDR	R/W	Xh	Holds bits [31:5] of the limit address for the selected SAU region
4-2	RES0	R	0h	Reserved, RES0
1	NSC	R/W	0h	Controls whether Non-secure state is permitted to execute an SG instruction from this region
0	ENABLE	R/W	0h	SAU region enable

2.7.12.6 SFSR Register (Offset = 14h) [Reset = 00000000h]

SFSR is shown in Table 2-476.

Return to the Summary Table.

Provides information about any security related faults

Table 2-476. SFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7	LSERR	R/W	0h	Sticky flag indicating that an error occurred during lazy state activation or deactivation
6	SFARVALID	R/W	0h	This bit is set when the SFAR register contains a valid value. As with similar fields, such as BFSR.BFARVALID and MMFSR.MMARVALID, this bit can be cleared by other exceptions, such as BusFault
5	LSPERR	R/W	0h	Stick flag indicating that an SAU or IDAU violation occurred during the lazy preservation of floating-point state
4	INVTRAN	R/W	0h	Sticky flag indicating that an exception was raised due to a branch that was not flagged as being domain crossing causing a transition from Secure to Non-secure memory
3	AUVIOL	R/W	0h	Sticky flag indicating that an attempt was made to access parts of the address space that are marked as Secure with NS-Req for the transaction set to Non-secure. This bit is not set if the violation occurred during lazy state preservation. See LSPERR
2	INVER	R/W	0h	This can be caused by EXC_RETURN.DCRS being set to 0 when returning from an exception in the Non-secure state, or by EXC_RETURN.ES being set to 1 when returning from an exception in the Non-secure state
1	INVIS	R/W	0h	This bit is set if the integrity signature in an exception stack frame is found to be invalid during the unstacking operation
0	INVEP	R/W	0h	This bit is set if a function call from the Non-secure state or exception targets a non-SG instruction in the Secure state. This bit is also set if the target address is a SG instruction, but there is no matching SAU/IDAU region with the NSC flag set

2.7.12.7 SFAR Register (Offset = 18h) [Reset = 00000000h]

SFAR is shown in Table 2-477.

Return to the Summary Table.

Shows the address of the memory location that caused a Security violation

Table 2-477. SFAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	The address of an access that caused a attribution unit violation. This field is only valid when SFSR.SFARVALID is set. This allows the actual flip flops associated with this register to be shared with other fault address registers. If an implementation chooses to share the storage in this way, care must be taken to not leak Secure address information to the Non-secure state. One way of achieving this is to share the SFAR register with the MMFAR_S register, which is not accessible to the Non-secure state

2.7.13 SCB Registers

Table 2-478 lists the memory-mapped registers for the SCB registers. All register offset addresses not listed in Table 2-478 should be considered as reserved locations and the register contents should not be modified.

Table 2-478. SCB Registers

Offset	Acronym	Register Name	Section
0h	REVIDR	Provides implementation-specific minor revision information	Section 2.7.13.1
4h	CPUID	Provides identification information for the PE, including an implementer code for the device and a device ID number	Section 2.7.13.2
8h	ICSR	Controls and provides status information for NMI, PendSV, SysTick and interrupts	Section 2.7.13.3
Ch	VTOR	Indicates the offset of the vector table base address from memory address 0x00000000	Section 2.7.13.4
10h	AIRCR	This register is used to determine data endianness, clear all active state information for debug or to recover from a hard failure, execute a system reset, alter the priority grouping position (binary point).	Section 2.7.13.5
14h	SCR	This register is used for power-management functions, i.e., signaling to the system when the processor can enter a low power state, controlling how the processor enters and exits low power states.	Section 2.7.13.6
18h	CCR	Sets or returns configuration and control data	Section 2.7.13.7
1Ch	SHPR1	Sets or returns priority for system handlers 4 - 7	Section 2.7.13.8
20h	SHPR2	Sets or returns priority for system handlers 8 - 11	Section 2.7.13.9
24h	SHPR3	Sets or returns priority for system handlers 12 - 15	Section 2.7.13.10
28h	SHCSR	Provides access to the active and pending status of system exceptions	Section 2.7.13.11
2Ch	CFSR	Contains the three Configurable Fault Status Registers	Section 2.7.13.12
30h	HFSR	Shows the cause of any HardFaults	Section 2.7.13.13
34h	DFSR	Shows which debug event occurred	Section 2.7.13.14
38h	MMFAR	Shows the address of the memory location that caused an MPU fault	Section 2.7.13.15
3Ch	BFAR	Shows the address associated with a precise data access BusFault	Section 2.7.13.16
40h	AFSR	This register is used to determine additional system fault information to software. Single-cycle high level on an auxiliary faults is latched as one. The bit can only be cleared by writing a one to the corresponding bit. Auxiliary fault inputs to the **CPU** are tied to 0.	Section 2.7.13.17
44h	ID_PFR0	Gives top-level information about the instruction set supported by the PE	Section 2.7.13.18
48h	ID_PFR1	Gives information about the programmers' model and Extensions support	Section 2.7.13.19
4Ch	ID_DFR0	Provides top level information about the debug system	Section 2.7.13.20
50h	ID_AFR0	Provides information about the IMPLEMENTATION DEFINED features of the PE	Section 2.7.13.21
54h	ID_MMFR0	Provides information about the implemented memory model and memory management support	Section 2.7.13.22
58h	ID_MMFR1	Provides information about the implemented memory model and memory management support	Section 2.7.13.23
5Ch	ID_MMFR2	Provides information about the implemented memory model and memory management support	Section 2.7.13.24
60h	ID_MMFR3	Provides information about the implemented memory model and memory management support	Section 2.7.13.25

Table 2-478. SCB Registers (continued)

Offset	Acronym	Register Name	Section
64h	ID_ISAR0	Provides information about the instruction set implemented by the PE	Section 2.7.13.26
68h	ID_ISAR1	Provides information about the instruction set implemented by the PE	Section 2.7.13.27
6Ch	ID_ISAR2	Provides information about the instruction set implemented by the PE	Section 2.7.13.28
70h	ID_ISAR3	Provides information about the instruction set implemented by the PE	Section 2.7.13.29
74h	ID_ISAR4	Provides information about the instruction set implemented by the PE	Section 2.7.13.30
78h	ID_ISAR5	Provides information about the instruction set implemented by the PE	Section 2.7.13.31
7Ch	CLIDR	Identifies the type of caches implemented and the level of coherency and unification	Section 2.7.13.32
80h	CTR	The CTR provides information about the architecture of the currently selected cache	Section 2.7.13.33
84h	CCSIDR	Provides information about the architecture of the caches. CCSIDR is RES0 if CLIDR is zero.	Section 2.7.13.34
88h	CSSELR	Selects the current Cache Size ID Register, CCSIDR, by specifying the required cache level and the cache	Section 2.7.13.35
8Ch	CPACR	Specifies the access privileges for coprocessors and the FP Extension	Section 2.7.13.36
90h	NSACR	Defines the Non-secure access permissions for both the FP Extension and coprocessors CP0 to CP7	Section 2.7.13.37

Complex bit access types are encoded to fit into small table cells. Table 2-479 shows the codes that are used for access types in this section.

Table 2-479. SCB Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.13.1 REVIDR Register (Offset = 0h) [Reset = 00000000h]

REVIDR is shown in Table 2-480.

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Provides implementation-specific minor revision information

Table 2-480. REVIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IMPLEMENTAION_DEFINED	R	411FD210h	The contents of this field are IMPLEMENTATION DEFINED

2.7.13.2 CPUID Register (Offset = 4h) [Reset = 00000000h]

CPUID is shown in Table 2-481.

Return to the Summary Table.

Provides identification information for the PE, including an implementer code for the device and a device ID number

Table 2-481. CPUID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Implementer	R	41h	This field must hold an implementer code that has been assigned by ARM
23-20	Variant	R	1h	IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product
19-16	Architecture	R	Fh	Defines the Architecture implemented by the PE
15-4	PartNo	R	D21h	IMPLEMENTATION DEFINED primary part number for the device
3-0	Revision	R	0h	IMPLEMENTATION DEFINED revision number for the device

2.7.13.3 ICSR Register (Offset = 8h) [Reset = 00000000h]

ICSR is shown in Table 2-482.

Return to the Summary Table.

Controls and provides status information for NMI, PendSV, SysTick and interrupts

Table 2-482. ICSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PENDNMISET	R	0h	Indicates whether the NMI exception is pending
30	PENDNMICLR	W	0h	Allows the NMI exception pend state to be cleared
29	RES0	R	0h	Reserved, RES0
28	PENDSVSET	R	0h	Indicates whether the PendSV `FTSSS exception is pending
27	PENDSVCLR	W	0h	Allows the PendSV exception pend state to be cleared `FTSSS
26	PENDSTSET	R	0h	Indicates whether the SysTick `FTSSS exception is pending
25	PENDSTCLR	W	0h	Allows the SysTick exception pend state to be cleared `FTSSS
24	STTNS	R/W	0h	Controls whether in a single SysTick implementation, the SysTick is Secure or Non-secure
23	ISRPREEMPT	R	0h	Indicates whether a pending exception will be serviced on exit from debug halt state
22	ISRPENDING	R	0h	Indicates whether an external interrupt, generated by the NVIC, is pending
21	RES0_1	R	0h	Reserved, RES0
20-12	VECTPENDING	R	0h	The exception number of the highest priority pending and enabled interrupt
11	RETTOBASE	R	0h	In Handler mode, indicates whether there is more than one active exception
10-9	RES0_2	R	0h	Reserved, RES0
8-0	VECTACTIVE	R	0h	The exception number of the current executing exception

2.7.13.4 VTOR Register (Offset = Ch) [Reset = 00000000h]

VTOR is shown in Table 2-483.

Return to the Summary Table.

Indicates the offset of the vector table base address from memory address 0x00000000

Table 2-483. VTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	TBLOFF	R	00823FA4h	Bits 31 down to 7 of the vector table base offset.
6-0	RES0	R	10h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

2.7.13.5 AIRCR Register (Offset = 10h) [Reset = 00000000h]

AIRCR is shown in Table 2-484.

Return to the Summary Table.

This register is used to determine data endianness, clear all active state information for debug or to recover from a hard failure, execute a system reset, alter the priority grouping position (binary point).

Table 2-484. AIRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VECTKEY	R/W	FA05h	Register key. Writing to this register (AIRCR) requires 0x05FA in VECTKEY. Otherwise the write value is ignored. Read always returns 0xFA05.
15	ENDIANESS	R	0h	Data endianness bit;0 Little-endian.;1 Big-endian.
14	PRIS	R	0h	Prioritize Secure exceptions. The value of this bit defines whether Secure exception priority boosting is;enabled.
13	BFHFNMINS	R/W	0h	BusFault, HardFault, and NMI Non-secure enable. The value of this bit defines whether BusFault and NMI;exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception;0x0 BusFault, HardFault, and NMI are Secure.;0x1 BusFault and NMI are Non-secure and exceptions can target Non-secure HardFault.
12-11	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
10-8	PRIGROUP	R/W	0h	Interrupt priority grouping field. This field determines the split of group priority from;subpriority
7-4	RES4	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	SYSRESETREQS	R/W	0h	System reset request Secure only. The value of this bit defines whether the SYSRESETREQ bit is functional;for Non-secure use
2	SYSRESETREQ	W	0h	System reset request. This bit allows software or a debugger to request a system reset:;0 Do not request a system reset.;1 Request a system reset.;This bit is not banked between Security states.
1	VECTCLRACTIVE	W	0h	Reserved for Debug use. This bit reads as 0. When writing to the register you must write;0 to this bit, otherwise behavior is UNPREDICTABLE.
1	RESERVED	R	0h	Reserved
0	RES0	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

2.7.13.6 SCR Register (Offset = 14h) [Reset = 00000000h]

SCR is shown in Table 2-485.

Return to the Summary Table.

This register is used for power-management functions, i.e., signaling to the system when the processor can enter a low power state, controlling how the processor enters and exits low power states.

Table 2-485. SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
4	SEVONPEND	R/W	0h	Send Event on Pending bit:;0 Only enabled interrupts or events can wakeup the processor, disabled interrupts are excluded.;1 Enabled events and all interrupts, including disabled interrupts, can wakeup the processor.;When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the;processor is not waiting for an event, the event is registered and affects the next WFE.;The processor also wakes up on execution of an SEV instruction or an external event.;This bit is banked between Security states.
3	SLEEPDEEPS	R/W	0h	Controls whether the SLEEPDEEP bit is only accessible from the Secure state:;0 The SLEEPDEEP bit accessible from both Security states.;1 The SLEEPDEEP bit behaves as RAZ/WI when accessed from the Non-secure state.;This bit in only accessible from the Secure state, and behaves as RAZ/WI when accessed from the Nonsecure;state.;This bit is not banked between Security states.
2	SLEEPDEEP	R/W	0h	Controls whether the processor uses sleep or deep sleep as its low power mode.;0 Sleep.;1 Deep sleep.;This bit is not banked between Security states.
1	SLEEPONEXIT	R/W	0h	Indicates sleep-on-exit when returning from Handler mode to Thread mode:;0 Do not sleep when returning to Thread mode.;1 Enter sleep, or deep sleep, on return from an ISR.;Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.;This bit is banked between Security states.
0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.

2.7.13.7 CCR Register (Offset = 18h) [Reset = 00000000h]

CCR is shown in Table 2-486.

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Sets or returns configuration and control data

Table 2-486. CCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RES0	R	0h	Reserved, RES0
18	BP	R	0h	Enables program flow prediction `FTSSS
17	IC	R	0h	This is a global enable bit for instruction caches in the selected Security state
16	DC	R	0h	Enables data caching of all data accesses to Normal memory `FTSSS
15-11	RES0_1	R	0h	Reserved, RES0
10	STKOFHFNMIGN	R/W	0h	Controls the effect of a stack limit violation while executing at a requested priority less than 0
9	RES1	R	1h	Reserved, RES1
8	BFHFNMIGN	R/W	0h	Determines the effect of precise BusFaults on handlers running at a requested priority less than 0
7-5	RES0_2	R	0h	Reserved, RES0
4	DIV_0_TRP	R/W	0h	Controls the generation of a DIVBYZERO UsageFault when attempting to perform integer division by zero
3	UNALIGN_TRP	R/W	0h	Controls the trapping of unaligned word or halfword accesses
2	RES0_3	R	0h	Reserved, RES0
1	USERSETMPEND	R/W	0h	Determines whether unprivileged accesses are permitted to pend interrupts via the STIR
0	RES1_1	R	1h	Reserved, RES1

2.7.13.8 SHPR1 Register (Offset = 1Ch) [Reset = 00000000h]

SHPR1 is shown in Table 2-487.

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Sets or returns priority for system handlers 4 - 7

Table 2-487. SHPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI_7	R/W	0h	Priority of system handler 7, SecureFault
23-16	PRI_6	R/W	0h	Priority of system handler 6, UsageFault
15-8	PRI_5	R/W	0h	Priority of system handler 5, BusFault
7-0	PRI_4	R/W	0h	Priority of system handler 4, MemManage

2.7.13.9 SHPR2 Register (Offset = 20h) [Reset = 00000000h]

SHPR2 is shown in Table 2-488.

Return to the Summary Table.

Sets or returns priority for system handlers 8 - 11

Table 2-488. SHPR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI_11	R/W	0h	Priority of system handler 11, SVCall
23-0	RES0	R	Xh	Reserved, RES0

2.7.13.10 SHPR3 Register (Offset = 24h) [Reset = 00000000h]

SHPR3 is shown in Table 2-489.

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Sets or returns priority for system handlers 12 - 15

Table 2-489. SHPR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI_15	R/W	0h	Priority of system handler 15, SysTick
23-16	PRI_14	R/W	0h	Priority of system handler 14, PendSV
15-0	RES0_0	R	0h	Reserved, RES0

2.7.13.11 SHCSR Register (Offset = 28h) [Reset = 00000000h]

SHCSR is shown in Table 2-490.

Return to the Summary Table.

Provides access to the active and pending status of system exceptions

Table 2-490. SHCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RES0	R	0h	Reserved, RES0
21	HARDFAULTPENDED	R/W	0h	`IAAMO the pending state of the HardFault exception `CTTSSS
20	SECUREFAULTPENDED	R/W	0h	`IAAMO the pending state of the SecureFault exception
19	SECUREFAULTENA	R/W	0h	`DW the SecureFault exception is enabled
18	USGFAULTENA	R/W	0h	`DW the UsageFault exception is enabled `FTSSS
17	BUSFAULTENA	R/W	0h	`DW the BusFault exception is enabled
16	MEMFAULTENA	R/W	0h	`DW the MemManage exception is enabled `FTSSS
15	SVCALLPENDED	R/W	0h	`IAAMO the pending state of the SVCall exception `FTSSS
14	BUSFAULTPENDED	R/W	0h	`IAAMO the pending state of the BusFault exception
13	MEMFAULTPENDED	R/W	0h	`IAAMO the pending state of the MemManage exception `FTSSS
12	USGFAULTPENDED	R/W	0h	The UsageFault exception is banked between Security states, `IAAMO the pending state of the UsageFault exception `FTSSS
11	SYSTICKACT	R/W	0h	`IAAMO the active state of the SysTick exception `FTSSS
10	PENDSVACT	R/W	0h	`IAAMO the active state of the PendSV exception `FTSSS
9	RES0_1	R	0h	Reserved, RES0
8	MONITORACT	R/W	0h	`IAAMO the active state of the DebugMonitor exception
7	SVCALLACT	R/W	0h	`IAAMO the active state of the SVCall exception `FTSSS
6	RES0_2	R	0h	Reserved, RES0
5	NMIACT	R/W	0h	`IAAMO the active state of the NMI exception
4	SECUREFAULTACT	R/W	0h	`IAAMO the active state of the SecureFault exception
3	USGFAULTACT	R/W	0h	`IAAMO the active state of the UsageFault exception `FTSSS
2	HARDFAULTACT	R/W	0h	Indicates and allows limited modification of the active state of the HardFault exception `FTSSS
1	BUSFAULTACT	R/W	0h	`IAAMO the active state of the BusFault exception
0	MEMFAULTACT	R/W	0h	`IAAMO the active state of the MemManage exception `FTSSS

2.7.13.12 CFSR Register (Offset = 2Ch) [Reset = 00000000h]

CFSR is shown in Table 2-491.

Return to the Summary Table.

Contains the three Configurable Fault Status Registers

Table 2-491. CFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES0_3	R	0h	Reserved, RES0
25	DIVBYZERO	R/W	0h	Sticky flag indicating whether an integer division by zero error has occurred
24	UNALIGNED	R/W	0h	Sticky flag indicating whether an unaligned access error has occurred
23-21	RES0_1_2	R	0h	Reserved, RES0
20	STKOF	R/W	0h	Sticky flag indicating whether a stack overflow error has occurred
19	NOCP	R/W	0h	Sticky flag indicating whether a coprocessor disabled or not present error has occurred
18	INVPC	R/W	0h	Sticky flag indicating whether an integrity check error has occurred
17	INVSTATE	R/W	0h	Sticky flag indicating whether an EPSR.T or EPSR.IT validity error has occurred
16	UNDEFINSTR	R/W	0h	Sticky flag indicating whether an undefined instruction error has occurred
15	BFARVALID	R/W	0h	Indicates validity of the contents of the BFAR register
14	RES0_2	R	0h	Reserved, RES0
13	LSPERR	R/W	0h	Records whether a BusFault occurred during FP lazy state preservation
12	STKERR	R/W	0h	Records whether a derived BusFault occurred during exception entry stacking
11	UNSTKERR	R/W	0h	Records whether a derived BusFault occurred during exception return unstacking
10	IMPRECISERR	R/W	0h	Records whether an imprecise data access error has occurred
9	PRECISERR	R/W	0h	Records whether a precise data access error has occurred
8	IBUSERR	R/W	0h	Records whether a BusFault on an instruction prefetch has occurred
7	MMARVALID	R/W	0h	Indicates validity of the MMFAR register
6	RES0	R	0h	Reserved, RES0
5	MLSPERR	R/W	0h	Records whether a MemManage fault occurred during FP lazy state preservation
4	MSTKERR	R/W	0h	Records whether a derived MemManage fault occurred during exception entry stacking
3	MUNSTKERR	R/W	0h	Records whether a derived MemManage fault occurred during exception return unstacking
2	RES0_1	R	0h	Reserved, RES0
1	DACCVIOL	R/W	0h	Records whether a data access violation has occurred
0	IACCVIOL	R/W	0h	Records whether an instruction related memory access violation has occurred

2.7.13.13 HFSR Register (Offset = 30h) [Reset = 00000000h]

HFSR is shown in Table 2-492.

Return to the Summary Table.

Shows the cause of any HardFaults

Table 2-492. HFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DEBUGEVT	R/W	0h	Indicates when a Debug event has occurred
30	FORCED	R/W	0h	Indicates that a fault with configurable priority has been escalated to a HardFault exception, because it could not be made active, because of priority, or because it was disabled
29-2	RES0	R	Xh	Reserved, RES0
1	VECTTBL	R/W	0h	Indicates when a fault has occurred because of a vector table read error on exception processing
0	RES0_1	R	0h	Reserved, RES0

2.7.13.14 DFSR Register (Offset = 34h) [Reset = 00000000h]

DFSR is shown in Table 2-493.

Return to the Summary Table.

Shows which debug event occurred

Table 2-493. DFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RES0	R	Xh	Reserved, RES0
4	EXTERNAL	R/W	0h	Sticky flag indicating whether an External debug request debug event has occurred
3	VCATCH	R/W	0h	Sticky flag indicating whether a Vector catch debug event has occurred
2	DWTTRAP	R/W	0h	Sticky flag indicating whether a Watchpoint debug event has occurred
1	BKPT	R/W	0h	Sticky flag indicating whether a Breakpoint debug event has occurred
0	HALTED	R/W	0h	Sticky flag indicating that a Halt request debug event or Step debug event has occurred

2.7.13.15 MMFAR Register (Offset = 38h) [Reset = 00000000h]

MMFAR is shown in Table 2-494.

Return to the Summary Table.

Shows the address of the memory location that caused an MPU fault

Table 2-494. MMFAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	This register is updated with the address of a location that produced a MemManage fault. The MMFSR shows the cause of the fault, and whether this field is valid. This field is valid only when MMFSR.MMARVALID is set, otherwise it is UNKNOWN

2.7.13.16 BFAR Register (Offset = 3Ch) [Reset = 00000000h]

BFAR is shown in Table 2-495.

Return to the Summary Table.

Shows the address associated with a precise data access BusFault

Table 2-495. BFAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R/W	0h	This register is updated with the address of a location that produced a BusFault. The BFSR shows the reason for the fault. This field is valid only when BFSR.BFARVALID is set, otherwise it is UNKNOWN

2.7.13.17 AFSR Register (Offset = 40h) [Reset = 00000000h]

AFSR is shown in Table 2-496.

Return to the Summary Table.

This register is used to determine additional system fault information to software. Single-cycle high level on an auxiliary faults is latched as one. The bit can only be cleared by writing a one to the corresponding bit. Auxiliary fault inputs to the CPU are tied to 0.

Table 2-496. AFSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	IMPDEF	R/W	0h	Implementation defined. The bits map directly onto the signal assignment to the auxiliary fault inputs. Tied to 0

2.7.13.18 ID_PFR0 Register (Offset = 44h) [Reset = 00000000h]

ID_PFR0 is shown in Table 2-497.

Return to the Summary Table.

Gives top-level information about the instruction set supported by the PE

Table 2-497. ID_PFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RES0	R	Xh	Reserved, RES0
7-4	State1	R	3h	T32 instruction set support
3-0	State0	R	0h	A32 instruction set support

2.7.13.19 ID_PFR1 Register (Offset = 48h) [Reset = 00000000h]

ID_PFR1 is shown in Table 2-498.

Return to the Summary Table.

Gives information about the programmers' model and Extensions support

Table 2-498. ID_PFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RES0	R	Xh	Reserved, RES0
11-8	MProgMod	R	2h	Identifies support for the M-Profile programmers' model support
7-4	Security	R	1h	Identifies whether the Security Extension is implemented
3-0	RES0_1	R	0h	Reserved, RES0

2.7.13.20 ID_DFR0 Register (Offset = 4Ch) [Reset = 00000000h]

ID_DFR0 is shown in Table 2-499.

Return to the Summary Table.

Provides top level information about the debug system

Table 2-499. ID_DFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES0	R	0h	Reserved, RES0
23-20	MProfDbg	R	2h	Indicates the supported M-profile debug architecture
19-0	RES0_1	R	Xh	Reserved, RES0

2.7.13.21 ID_AFR0 Register (Offset = 50h) [Reset = 00000000h]

ID_AFR0 is shown in Table 2-500.

Return to the Summary Table.

Provides information about the IMPLEMENTATION DEFINED features of the PE

Table 2-500. ID_AFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RES0	R	0h	Reserved, RES0
15-12	IMPDEF3	R	0h	IMPLEMENTATION DEFINED meaning
11-8	IMPDEF2	R	0h	IMPLEMENTATION DEFINED meaning
7-4	IMPDEF1	R	0h	IMPLEMENTATION DEFINED meaning
3-0	IMPDEF0	R	0h	IMPLEMENTATION DEFINED meaning

2.7.13.22 ID_MMFR0 Register (Offset = 54h) [Reset = 00000000h]

ID_MMFR0 is shown in Table 2-501.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 2-501. ID_MMFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES0	R	0h	Reserved, RES0
23-20	AuxReg	R	1h	Indicates support for Auxiliary Control Registers
19-16	TCM	R	0h	Indicates support for tightly coupled memories (TCMs)
15-12	ShareLvl	R	1h	Indicates the number of shareability levels implemented
11-8	OuterShr	R	Fh	Indicates the outermost shareability domain implemented
7-4	PMSA	R	4h	Indicates support for the protected memory system architecture (PMSA)
3-0	RES0_1	R	0h	Reserved, RES0

2.7.13.23 ID_MMFR1 Register (Offset = 58h) [Reset = 00000000h]

ID_MMFR1 is shown in Table 2-502.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 2-502. ID_MMFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.13.24 ID_MMFR2 Register (Offset = 5Ch) [Reset = 00000000h]

ID_MMFR2 is shown in Table 2-503.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 2-503. ID_MMFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	WFIStall	R	1h	Indicates the support for Wait For Interrupt (WFI) stalling
23-0	RES0_1	R	Xh	Reserved, RES0

2.7.13.25 ID_MMFR3 Register (Offset = 60h) [Reset = 00000000h]

ID_MMFR3 is shown in Table 2-504.

Return to the Summary Table.

Provides information about the implemented memory model and memory management support

Table 2-504. ID_MMFR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RES0	R	Xh	Reserved, RES0
11-8	BPMaint	R	0h	Indicates the supported branch predictor maintenance
7-4	CMaintSW	R	0h	Indicates the supported cache maintenance operations by set/way
3-0	CMaintVA	R	0h	Indicates the supported cache maintenance operations by address

2.7.13.26 ID_ISAR0 Register (Offset = 64h) [Reset = 00000000h]

ID_ISAR0 is shown in Table 2-505.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 2-505. ID_ISAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	Divide	R	1h	Indicates the supported Divide instructions
23-20	Debug	R	1h	Indicates the implemented Debug instructions
19-16	Coproc	R	4h	Indicates the supported Coprocessor instructions
15-12	CmpBranch	R	1h	Indicates the supported combined Compare and Branch instructions
11-8	BitField	R	1h	Indicates the supported bit field instructions
7-4	BitCount	R	1h	Indicates the supported bit count instructions
3-0	RES0_1	R	0h	Reserved, RES0

2.7.13.27 ID_ISAR1 Register (Offset = 68h) [Reset = 00000000h]

ID_ISAR1 is shown in Table 2-506.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 2-506. ID_ISAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	Interwork	R	2h	Indicates the implemented Interworking instructions
23-20	Immediate	R	2h	Indicates the implemented for data-processing instructions with long immediates
19-16	IfThen	R	1h	Indicates the implemented If-Then instructions
15-12	Extend	R	2h	Indicates the implemented Extend instructions
11-0	RES0_1	R	0h	Reserved, RES0

2.7.13.28 ID_ISAR2 Register (Offset = 6Ch) [Reset = 00000000h]

ID_ISAR2 is shown in Table 2-507.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 2-507. ID_ISAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reversal	R	2h	Indicates the implemented Reversal instructions
27-24	RES0	R	0h	Reserved, RES0
23-20	MultU	R	2h	Indicates the implemented advanced unsigned Multiply instructions
19-16	MultS	R	3h	Indicates the implemented advanced signed Multiply instructions
15-12	Mult	R	2h	Indicates the implemented additional Multiply instructions
11-8	MultiAccessInt	R	2h	Indicates the support for interruptible multi-access instructions
7-4	MemHint	R	3h	Indicates the implemented Memory Hint instructions
3-0	LoadStore	R	2h	Indicates the implemented additional load/store instructions

2.7.13.29 ID_ISAR3 Register (Offset = 70h) [Reset = 00000000h]

ID_ISAR3 is shown in Table 2-508.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 2-508. ID_ISAR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	TrueNOP	R	1h	Indicates the implemented true NOP instructions
23-20	T32Copy	R	1h	Indicates the support for T32 non flag-setting MOV instructions
19-16	TabBranch	R	1h	Indicates the implemented Table Branch instructions
15-12	SynchPrim	R	1h	Used in conjunction with ID_ISAR4.SynchPrim_frac to indicate the implemented Synchronization Primitive instructions
11-8	SVC	R	1h	Indicates the implemented SVC instructions
7-4	SIMD	R	3h	Indicates the implemented SIMD instructions
3-0	Saturate	R	1h	Indicates the implemented saturating instructions

2.7.13.30 ID_ISAR4 Register (Offset = 74h) [Reset = 00000000h]

ID_ISAR4 is shown in Table 2-509.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 2-509. ID_ISAR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES0	R	0h	Reserved, RES0
27-24	PSR_M	R	1h	Indicates the implemented M profile instructions to modify the PSRs
23-20	SyncPrim_frac	R	3h	Used in conjunction with ID_ISAR3.SynchPrim to indicate the implemented Synchronization Primitive instructions
19-16	Barrier	R	1h	Indicates the implemented Barrier instructions
15-12	RES0_1	R	0h	Reserved, RES0
11-8	Writeback	R	1h	Indicates the support for writeback addressing modes
7-4	WithShifts	R	3h	Indicates the support for writeback addressing modes
3-0	Unpriv	R	2h	Indicates the implemented unprivileged instructions

2.7.13.31 ID_ISAR5 Register (Offset = 78h) [Reset = 00000000h]

ID_ISAR5 is shown in Table 2-510.

Return to the Summary Table.

Provides information about the instruction set implemented by the PE

Table 2-510. ID_ISAR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES0	R	0h	Reserved, RES0

2.7.13.32 CLIDR Register (Offset = 7Ch) [Reset = 00000000h]

CLIDR is shown in Table 2-511.

Return to the Summary Table.

Identifies the type of caches implemented and the level of coherency and unification

Table 2-511. CLIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	ICB	R	0h	This field indicates the boundary between inner and outer domain 0h = Not disclosed in this mechanism 1h = L1 cache is the highest inner level 2h = L2 cache is the highest inner level 3h = L3 cache is the highest inner level
29-27	LoUU	R	0h	This field indicates the Level of Unification Uniprocessor for the cache;hierarchy
26-24	LoC	R	0h	This field indicates the Level of Coherence for the cache hierarchy
23-21	LoUIS	R	0h	Enables Non-secure access to coprocessor CP0
20-18	Ctype7	R	0h	Cache type field 7. Indicates the type of cache implemented at level 7. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
17-15	Ctype6	R	0h	Cache type field 6. Indicates the type of cache implemented at level 6. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
14-12	Ctype5	R	0h	Cache type field 5. Indicates the type of cache implemented at level 5. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
11-9	Ctype4	R	0h	Cache type field 4. Indicates the type of cache implemented at level 4. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
8-6	Ctype3	R	0h	Cache type field 3. Indicates the type of cache implemented at level 3. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache
5-3	Ctype2	R	0h	Cache type field 2. Indicates the type of cache implemented at level 2. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache

Table 2-511. CLIDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	Ctype1	R	0h	Cache type field 1. Indicates the type of cache implemented at level 1. 0h = No cache 1h = Instruction cache only 2h = Data cache only 3h = Separate instruction and data caches 4h = Unified cache

2.7.13.33 CTR Register (Offset = 80h) [Reset = 00000000h]

CTR is shown in Table 2-512.

Return to the Summary Table.

The CTR provides information about the architecture of the currently selected cache

Table 2-512. CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES1	R	1h	Reserved, RES1
30-28	RES0	R	0h	Reserved, RES0
27-24	CWG	R	0h	Log2 of the number of words of the maximum size of memory that can be overwritten as a result of the eviction of a cache entry that has had a memory location in it modified
23-20	ERG	R	0h	Log2 of the number of words of the maximum size of the reservation granule that has been implemented for the Load-Exclusive and Store-Exclusive instructions
19-16	DminLine	R	0h	Log2 of the number of words in the smallest cache line of all the data caches and unified caches that are controlled by the PE
15-14	RES1_1	R	3h	Reserved, RES1
13-4	RES0_1	R	0h	Reserved, RES0
3-0	IminLine	R	0h	Log2 of the number of words in the smallest cache line of all the instruction caches that are controlled by the PE

2.7.13.34 CCSIDR Register (Offset = 84h) [Reset = 00000000h]

CCSIDR is shown in Table 2-513.

Return to the Summary Table.

Provides information about the architecture of the caches. CCSIDR is RES0 if CLIDR is zero.

Table 2-513. CCSIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WT	R	1h	Indicates whether the currently selected cache level supports Write-Through 0h = Not supported 1h = Supported
30	WB	R	0h	Indicates whether the currently selected cache level supports Write-Back 0h = Not supported 1h = Supported
29	RA	R	0h	Indicates whether the currently selected cache level supports read-allocation 0h = Not supported 1h = Supported
28	WA	R	0h	Indicates whether the currently selected cache level supports write-allocation 0h = Not supported 1h = Supported
27-13	NumSets	R	6h	Indicates (Number of sets in the currently selected cache) - 1. Therefore, a value of 0;indicates that 1 is set in the cache. The number of sets does not have to be a power of 2
12-3	Associativity	R	0h	Indicates (Associativity of cache) - 1. A value of 0 indicates an associativity of 1. The;associativity does not have to be a power of 2
2-0	LineSize	R	0h	Indicates (Log2(Number of words per line in the currently selected cache)) - 2.

2.7.13.35 CSSELR Register (Offset = 88h) [Reset = 00000000h]

CSSELR is shown in Table 2-514.

Return to the Summary Table.

Selects the current Cache Size ID Register, CCSIDR, by specifying the required cache level and the cache;type (either instruction or data cache)

Table 2-514. CSSELR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	Res0	R	08000C00h	Reserved,Res0
3-1	Level	R	0h	Selects which cache level is to be identified. Permitted values are from 0b000, indicating Level;1 cache, to 0b110 indicating Level 7 cache 0h = Level 1 cache 1h = Level 2 cache 2h = Level 3 cache 3h = Level 4 cache 4h = Level 5 cache 5h = Level 6 cache 6h = Level 7 cache
0	InD	R	0h	Selects whether the instruction or the data cache is to be identified 0h = Data or unified cache 1h = Instruction cache

2.7.13.36 CPACR Register (Offset = 8Ch) [Reset = 00000000h]

CPACR is shown in Table 2-515.

Return to the Summary Table.

Specifies the access privileges for coprocessors and the FP Extension

Table 2-515. CPACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES0	R	0h	Reserved, RES0
23-22	CP11	R/W	0h	The value in this field is ignored. If the implementation does not include the FP Extension, this field is RAZ/WI. If the value of this bit is not programmed to the same value as the CP10 field, then the value is UNKNOWN
21-20	CP10	R/W	0h	Defines the access rights for the floating-point functionality
19-16	RES0_1	R	0h	Reserved, RES0
15-14	CP7	R/W	0h	Controls access privileges for coprocessor 7
13-12	CP6	R/W	0h	Controls access privileges for coprocessor 6
11-10	CP5	R/W	0h	Controls access privileges for coprocessor 5
9-8	CP4	R/W	0h	Controls access privileges for coprocessor 4
7-6	CP3	R/W	0h	Controls access privileges for coprocessor 3
5-4	CP2	R/W	0h	Controls access privileges for coprocessor 2
3-2	CP1	R/W	0h	Controls access privileges for coprocessor 1
1-0	CP0	R/W	0h	Controls access privileges for coprocessor 0

2.7.13.37 NSACR Register (Offset = 90h) [Reset = 00000000h]

NSACR is shown in Table 2-516.

Return to the Summary Table.

Defines the Non-secure access permissions for both the FP Extension and coprocessors CP0 to CP7

Table 2-516. NSACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RES0	R	Xh	Reserved, RES0
11	CP11	R/W	0h	Enables Non-secure access to the Floating-point Extension
10	CP10	R/W	0h	Enables Non-secure access to the Floating-point Extension
9-8	RES0_1	R	0h	Reserved, RES0
7	CP7	R/W	0h	Enables Non-secure access to coprocessor CP7
6	CP6	R/W	0h	Enables Non-secure access to coprocessor CP6
5	CP5	R/W	0h	Enables Non-secure access to coprocessor CP5
4	CP4	R/W	0h	Enables Non-secure access to coprocessor CP4
3	CP3	R/W	0h	Enables Non-secure access to coprocessor CP3
2	CP2	R/W	0h	Enables Non-secure access to coprocessor CP2
1	CP1	R/W	0h	Enables Non-secure access to coprocessor CP1
0	CP0	R/W	0h	Enables Non-secure access to coprocessor CP0

2.7.14 SYSTIMER Registers

Table 2-517 lists the memory-mapped registers for the SYSTIMER registers. All register offset addresses not listed in Table 2-517 should be considered as reserved locations and the register contents should not be modified.

Table 2-517. SYSTIMER Registers

Offset	Acronym	Register Name	Section
0h	SysTick Control and Status Register	Controls and provides status date for the SysTick timer	Section 2.7.14.1
4h	SysTick Reload Value Register	Specifies the SysTick timer counter reload value	Section 2.7.14.2
8h	SysTick Current Value Register	Contains the current value of the SysTick counter	Section 2.7.14.3
Ch	SysTick Calibration Value Register	Indicates the SysTick calibration value and parameters for the selected security state	Section 2.7.14.4

Complex bit access types are encoded to fit into small table cells. Table 2-518 shows the codes that are used for access types in this section.

Table 2-518. SYSTIMER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.14.1 SysTick Control and Status Register (Offset = 0h) [Reset = 00000000h]

SysTick Control and Status Register is shown in Table 2-519.

Return to the Summary Table.

Controls and provides status date for the SysTick timer

Table 2-519. SysTick Control and Status Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES17	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
16	COUNTFLAG	R/W	0h	Indicates whether the counter has counted to zero since the last read of this register
15-3	RES3	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	CLKSOURCE	R/W	0h	Indicates the SysTick clock source
1	TICKINT	R/W	0h	Indicates whether counting to 0 causes the status of the SysTick exception to change to pending
0	ENABLE	R/W	0h	Indicates the enabled status of the SysTick counter

2.7.14.2 SysTick Reload Value Register (Offset = 4h) [Reset = 00000000h]

SysTick Reload Value Register is shown in Table 2-520.

Return to the Summary Table.

Specifies the SysTick timer counter reload value

Table 2-520. SysTick Reload Value Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	RELOAD	R/W	0h	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0

2.7.14.3 SysTick Current Value Register (Offset = 8h) [Reset = 00000000h]

SysTick Current Value Register is shown in Table 2-521.

Return to the Summary Table.

Contains the current value of the SysTick counter

Table 2-521. SysTick Current Value Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	CURRENT	W	0h	Reads the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.

2.7.14.4 SysTick Calibration Value Register (Offset = Ch) [Reset = 00000000h]

SysTick Calibration Value Register is shown in Table 2-522.

Return to the Summary Table.

Indicates the SysTick calibration value and parameters for the selected security state

Table 2-522. SysTick Calibration Value Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES24_2	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
30	SKEW	R	0h	Indicates whether the TENMS value is exact
29-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	TENMS	R	0h	Reload value for 10ms (100Hz) timing, subject to system clock skew errors. If the value reads as zero, the calibration value is not known.

2.7.15 SYSTICK Registers

Table 2-523 lists the memory-mapped registers for the SYSTICK registers. All register offset addresses not listed in Table 2-523 should be considered as reserved locations and the register contents should not be modified.

Table 2-523. SYSTICK Registers

Offset	Acronym	Register Name	Section
0h	SYST_CSR	Controls and provides status date for the SysTick timer	Section 2.7.15.1
4h	SYST_RVR	Specifies the SysTick timer counter reload value	Section 2.7.15.2
8h	SYST_CVR	Contains the current value of the SysTick counter	Section 2.7.15.3
Ch	SYST_CALIB	Indicates the SysTick calibration value and parameters for the selected security state	Section 2.7.15.4

Complex bit access types are encoded to fit into small table cells. Table 2-524 shows the codes that are used for access types in this section.

Table 2-524. SYSTICK Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

2.7.15.1 SYST_CSR Register (Offset = 0h) [Reset = 00000000h]

SYST_CSR is shown in Table 2-525.

Return to the Summary Table.

Controls and provides status date for the SysTick timer

Table 2-525. SYST_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES17	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
16	COUNTFLAG	R/W	0h	Indicates whether the counter has counted to zero since the last read of this register
15-3	RES3	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	CLKSOURCE	R/W	0h	Indicates the SysTick clock source
1	TICKINT	R/W	0h	Indicates whether counting to 0 causes the status of the SysTick exception to change to pending
0	ENABLE	R/W	0h	Indicates the enabled status of the SysTick counter

2.7.15.2 SYST_RVR Register (Offset = 4h) [Reset = 00000000h]

SYST_RVR is shown in Table 2-526.

Return to the Summary Table.

Specifies the SysTick timer counter reload value

Table 2-526. SYST_RVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	RELOAD	R/W	Xh	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0

2.7.15.3 SYST_CVR Register (Offset = 8h) [Reset = 00000000h]

SYST_CVR is shown in Table 2-527.

Return to the Summary Table.

Contains the current value of the SysTick counter

Table 2-527. SYST_CVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	CURRENT	W	Xh	Reads the current value of the SysTick counter.;A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.

2.7.15.4 SYST_CALIB Register (Offset = Ch) [Reset = 00000000h]

SYST_CALIB is shown in Table 2-528.

Return to the Summary Table.

Indicates the SysTick calibration value and parameters for the selected security state

Table 2-528. SYST_CALIB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES24_2	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
30	SKEW	R	0h	Indicates whether the TENMS value is exact
29-24	RES24	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
23-0	TENMS	R	Xh	Reload value for 10ms (100Hz) timing, subject to system clock skew errors. If the value reads as zero, the;calibration value is not known.

2.7.16 Clock Control

CPUSS is a single clock domain IP. The clock gating diagram is provided in the CPUSS implementation spec page:

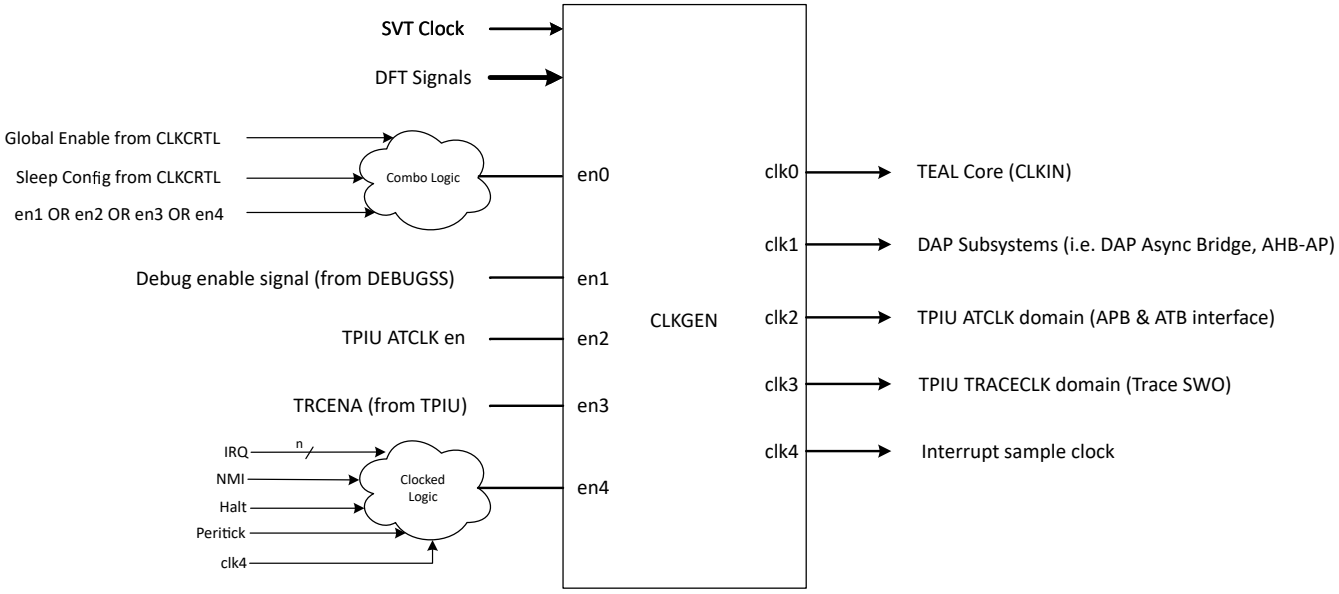

Figure 2-2. CPUSS Clock Control

There are 5 levels of clock gating in CPUSS which are explained below:

1. Clock gate 0

   It's the highest level of clock gate. This clock gate has to be enabled for the other clock gates to be functional. This clock gating is disabled when the SOC is in STANDBY. This clock gating is controlled by CLKCTRL IP.
2. Clock gate 1

   Based on debug connection, it will be used for clock gating the DAP subsystem. This involved the DAP bridge.
3. Clock gate 2

   This is used to clock gate the AT clock domain of TPIU. This is controlled by the debug authentication signals SPNIDEN & NIDEN and read or write to TPIU MMR.

4. Clock gate 3

   This is used to clock gate the TRACECLK domain of TPIU on which the SWO clock runs.
5. Clock gate 4

   This is used to enable the interrupt sampling circuitry present in the CPUSS.

2.7.17 Protocol Descriptions

CKM uses ARM's AMBA AHB protocol. Internally the SOC supports only AHB lite.

2.7.18 Reset Considerations

2.7.18.1 Hardware Reset Considerations

CPUSS has 2 resets nSYSRESET and nPORESET. nPORESET is the higher level reset among the 2. Hence when nSYSRESET is asserted, it must be ensured that clock to CPUSS is gated.

2.7.19 Initialization

Describe the initialization issues and information that are not related to a specific supported mode or use case, such as how to bring the peripheral out of reset. Put any information specific to one of the supported use cases (such as the proper configuration for that use case) in the use case section.

2.7.20 Interrupt and Event Support

2.7.20.1 Connection to Event Fabric

2.7.21 Power Management

Most parts of the design are clock-gated when not in use. The core M33 logic inside CPUSS will be clock gated only in standby (or DEEPSLEEP state of M33). When SOC is in idle state (or SLEEP state of M33), clock to M33 won't be gated so that systick timer inside M33 can keep on running.

This section describes the Memory Map.

3.1 Memory Map

All CC27XX devices share a common platform memory map. Peripherals are assigned a fixed address space and have the same address space on all devices within the family. The memory map is compliant with the standard Arm® Cortex® -M memory regions.

Table 3-1. Memory Map

Module	Module Name	Base Address
FLASHMEM	Program Flash Memory	0x0000 0000
ROM	System ROM	0x0F00 0000
SRAM	Static RAM	0x2000 0000
PMCTL	Power Mode Controller	0x4000 0000
CKMD	Clock Manager	0x4000 1000
RTC	Real-Time Clock	0x4000 2000
IOC	I/O Controller	0x4000 3000
SYS0	LPCOMP (Low Power Comparator), System Control and Trim	0x4000 4000
EVTULL	AON (Always On)/ULL (Ultra-Low Leakage) Event Fabric	0x4000 5000
PMUD	Power Management (BATMON and DCDC)	0x4000 6000
TCM	TrustZone Firewall Control Module	0x4000 7000
DBGSS	Debug Subsystem	0x4000 F000
CLKCTL	IP Clock Control	0x4002 0000
FLASH	Flash Subsystem Controller	0x4002 1000
SYSTIM	System Timer	0x4002 2000
GPIO	General Purpose I/O	0x4002 3000
VIMS	Versatile Instruction Memory System	0x4002 4000
EVTSVT	SVT (Standard Threshold Voltage)/MCU Event Fabric	0x4002 5000
DMA	µDMA (Direct Memory Access) Controller	0x400C 4000
SPI0	Serial Peripheral Interface (SPI) 0	0x4003 0000
SPI1	Serial Peripheral Interface (SPI) 1	0x4003 1000
UART0	Universal Asynchronous Receiver Transmitter (UART) 0	0x4003 4000
UART1	Universal Asynchronous Receiver Transmitter (UART) 1	0x4003 5000
I2C0	Inter-Integrated Circuit (I^2C) 0	0x4003 8000
ADC	Analog-to-Digital Converter	0x4005 0000
HSM	HSM wrapper	0x4005 3000
LGPT0	General Purpose Timer 0	0x4006 0000
LGPT1	General Purpose Timer 1	0x4006 1000
LGPT2	General Purpose Timer 2	0x4006 2000

Table 3-1. Memory Map (continued)

Module	Module Name	Base Address
LGPT3	General Purpose Timer 3	0x4006 3000
LRFD	Low-power Radio	0x4008 0000
PBERAM	Radio PBE RAM	0x4009 0000
BUFRAM	Radio BUF RAM	0x4009 2000
MCERAM	Radio MCE RAM	0x4009 4000
RFERAM	Radio RFE RAM	0x4009 6000
S2RRAM	Radio S2R RAM	0x4009 8000
AES	AES Accelerator	0x400C 0000
I^2S	I^2S interface	0x400C 1000
SRAMCTL	SRAM controller	0x400C 5000
CAN-FD	CAN-FD (Controller Area Network Flexible Data-Rate) interface	0x400D 0000
APU	Algorithm Processing Unit program memory and control	0x400D 2000
APURAM	Algorithm Processing Unit data memory	0x400E 0000
HSM	HSM (Hardware Security Module) security subsystem	0x400F 0000
FCFG	Factory Configuration	0x4E00 0000
CCFG	Customer Configuration	0x4E02 0000
HSMOTP0	Contains the memory sectors used by HSM as OTP storage	0x4E02 0800
SCFG	Contains Security Configuration	0x4E04 0000
VLOG	Version Log	0x4E06 0000
HSMOTP1	Used by HSM as OTP storage	0x4E06 0800
ITM	Cortex-M's Instrumentation Trace Macrocell (ITM)	0xE000 0000
DWT	Cortex-M's Data watchpoint and Trace (DWT)	0xE000 1000
FPB	Cortex-M's Flash Patch and Breakpoint (FPB)	0xE000 2000
ICB	Cortex-M's Implementation Control Block (ICB)	0xE000 E000
SYSTICK	Cortex-M's System Timer (SYSTICK)	0xE000 E010
NVIC	Cortex-M's Nested Vectored Interrupt Controller (NVIC)	0xE000 E100
SCB	Cortex-M's System Control Block (SCB)	0xE000 ED00
MPU	Cortex-M's Memory Protection Unit (MPU)	0xE000 ED90
SAU	Cortex-M's Security Attribution Unit (SAU)	0xE000 EDD0
DCB	Cortex-M's Debug Control Block	0xE000 EDE0
SIG	Cortex-M's Software Interrupt Generator (SIG)	0xE000 EF00
FPU	Cortex-M's Floating Point Unit (FPU)	0xE000 EF30
DIB	Cortex-M's CoreSight discovery information for the SCS	0xE000 EFB0
TPIU	Cortex-M's Trace Port Interface Unit (TPIU)	0xE004 0000
CPU_ROM_TABLE	Cortex-M ROM Table	0xE00F F000

Chapter 4

Interrupts and Events

This chapter describes interrupts and events for the CC27XX device platform and the different Arm® documentation listed in Chapter 2 are used as reference.

4.1 Exception Model

The Arm®Cortex®-M33 processor and the nested vectored interrupt controller (NVIC) prioritize and handle all exceptions in handler mode. The state of the processor is automatically stored to the stack on an exception and automatically restored from the stack at the end of the interrupt service routine (ISR). The vector is fetched in parallel to state saving, thus enabling efficient interrupt entry. The processor supports tail-chaining, which enables performance of back-to-back interrupts without the overhead of state saving and restoration.

Exception Types lists all exception types. Software can set eight priority levels on all the exceptions except reset and hard fault.

Internally, the highest user-programmable priority (0) is treated as third priority, after a reset, and a hard fault, in that order.

Note

The default priority is 0 for all the programmable priorities.

CAUTION

After a write to clear an interrupt source, it can take several processor cycles for the NVIC to detect the interrupt source de-assertion due to the write buffer. Thus, if the interrupt clear is done as the last action in an interrupt handler, it is possible for the interrupt handler to complete while the NVIC detects the interrupt as still asserted, causing the interrupt handler to be re-entered errantly. This situation can be avoided by either clearing the interrupt source at the beginning of the interrupt handler or by performing a read from the same address after the write to clear the interrupt source (and flush the write buffer).

4.1.1 Exception States

Each exception is in one of the following states:

- **Inactive**: The exception is not active and not pending.
- **Pending**: The exception is waiting to be serviced by the processor. An interrupt request from a peripheral or from software can change the state of the corresponding interrupt to pending.
- **Active**: An exception is being serviced by the processor but has not completed. An exception handler can interrupt the execution of another exception handler. In this case, both exceptions are in the active state.
- **Active and Pending**: The exception is being serviced by the processor, and there is a pending exception from the same source

4.1.2 Exception Types

The exception types are:

- **Reset**: The exception model treats reset as a special form of exception. When reset is asserted, the operation of the processor stops, potentially at any point in an instruction. When either power-on or warm reset is de-asserted, execution restarts from the address provided by the reset entry in the ROM vector table. Execution restarts as privileged execution in Secure state in Thread mode. This exception is not banked between security states.
- **NMI**: A Non-Maskable Interrupt (NMI) can be signaled by a peripheral or triggered by software. It is permanently enabled and has a fixed priority of -2. NMI can only be preempted by reset and, when it is Non-secure, by a Secure HardFault. If SCB:AIRCR.BFHFNMINS = 0, then the NMI is Secure. If SCB:AIRCR.BFHFNMINS = 1, then NMI is Non-secure.
- **HardFault**: A HardFault is an exception that occurs because of an error during normal or exception processing. HardFaults have a fixed priority of at least -1, meaning they have higher priority than any exception with configurable priority. This exception is not banked between security states.

  If SCB:AIRCR.BFHFNMINS = 0, HardFault handles all faults that are unable to preempt the current execution. The HardFault handler is always Secure.

If SCB:AIRCR.BFHFNMINS = 1, HardFault handles faults that target Non-secure state that are unable to preempt the current execution.
HardFaults that specifically target the Secure state when SCB:AIRCR.BFHFNMINS is set to 1 have a priority of -3 to ensure they can preempt any execution. A Secure HardFault at priority -3 is only enabled when SCB:AIRCR.BFHFNMINS is set to 1. Secure HardFault handles Secure faults that are unable to preempt current execution.

- **MemManage**: A MemManage fault is an exception that occurs because of a memory protection violation, compared to the MPU or the fixed memory protection constraints, for both instruction and data memory transactions. This fault is always used to abort instruction accesses to Execute Never (XN) memory regions. This exception is banked between security states.
- **BusFault**: A BusFault is an exception that occurs because of a memory-related violation for an instruction or data memory transaction. This might be from an error that is detected on a bus in the memory system. This exception is not banked between security states.

  If SCB:AIRCR.BFHFNMINS = 0, BusFaults target the Secure state.
  If SCB:AIRCR.BFHFNMINS = 1, BusFaults target the Non-secure state.

- **UsageFault**: A UsageFault is an exception that occurs because of a fault related to instruction execution. This includes:
  – An undefined instruction
  – An illegal unaligned access
  – Invalid state on instruction execution
  – An error on exception return

  The following can cause a usage fault:
  – An unaligned address on word and halfword memory access
  – Division by zero

  This exception is banked between security states.
- **SecureFault**: This exception is triggered by the various security checks that are performed. It is triggered, for example, when jumping from Non-secure code to an address in Secure code that is not marked as a valid entry point. Most systems choose to treat a Secure fault as a terminal condition that either halts or restarts the system. Any other handling of the SecureFault must be checked carefully to make sure that it does not inadvertently introduce a security vulnerability. SecureFaults always target the Secure state.
- **SVCall**: A Supervisor Call (SVC) is an exception that is triggered by the SVC instruction. In an OS environment, applications can use SVC instructions to access OS kernel functions and device drivers. This exception is banked between security states.
- **DebugMonitor:** A DebugMonitor exception. If halting debug is disabled and the debug monitor is enabled, a debug event causes a debug monitor exception when the group priority of the debug monitor exception is greater than the current execution priority.
- **PendSV**: PendSV is an asynchronous request for system-level service. In an OS environment, use PendSV for context switching when no other exception is active. This exception is banked between Security states.
- **SysTick**: A SysTick exception is an exception the system timer generates when it reaches zero. Software can also generate a SysTick exception. In an OS environment, the processor can use this exception as a system tick. This exception is banked between Security states.
- **Interrupt (IRQ)**: An interrupt, or IRQ, is an exception signaled by a peripheral, or generated by a software request. All interrupts are asynchronous to instruction execution. In the system, peripherals use interrupts to communicate with the processor. This exception is not banked between security states. Secure code can assign each interrupt to Secure or Non-secure state. By default, all interrupts are assigned to Secure state.

For an asynchronous exception, other than reset, the processor can execute extra instructions between the moment the exception is triggered and the moment the processor enters the exception handler. Privileged software can disable the exceptions that have configurable priority, as shown in the table above. An exception that targets Secure state cannot be disabled by Non-secure code.

Table 4-1. Exception Types

Exception Number	IRQ Number	Exception Type	Priority	Vector Address	Activation
1	-	Reset	-4, the highest	0x00000004	Asynchronous
2	-14	NMI	-2	0x00000008	Asynchronous
3	-13	Secure HardFault when SCB:AIRCR.BFHFNMINS is 1	-3	0x0000000C	Synchronous
		Secure HardFault when SCB:AIRCR.BFHFNMINS is 0	-1		
		HardFault	-1		
4	-12	MemManage	Configurable	0x00000010	Synchronous
5	-11	BusFault	Configurable	0x00000014	Synchronous
6	-10	UsageFault	Configurable	0x00000018	Synchronous
7	-9	SecureFault	Configurable	0x0000001C	Synchronous
8-10	-	Reserved	-	-	-
11	-5	SVCall	Configurable	0x0000002C	Synchronous
12	-4	DebugMonitor	Configurable	0x00000030	Synchronous
13	-	Reserved	-	-	-
14	-2	PendSV	Configurable	0x00000038	Asynchronous
15	-1	SysTick	Configurable	0x0000003C	Asynchronous
16 and above	0 and above	Interrupt (IRQ)	Configurable	0x00000040 and above (increasing in steps of 4)	Asynchronous

Note

To simplify the software layer, the CMSIS only uses IRQ numbers. It uses negative values for exceptions other than interrupts. The IPSR returns the Exception number.

4.1.3 Exception Handlers

The exception handlers are the following:

- **Interrupt Service Routine (ISRs)**: Interrupts IRQ0-IRQ46 are the exceptions that are handled by ISRs. Each interrupt is configured by Secure software in Secure or Non-secure state, using CPU_NVIC:ITNS0 and CPU_NVIC:ITNS1.
- **Fault Handler**: The fault handler handles the following exceptions:
  - HardFault
  - MemManage
  - BusFault
  - UsageFault
  - SecureFault

  There can be separate MemManage and UsageFault handlers in Secure and Non-secure state. The SCB:AIRCR.BFHFNMINS bit controls the target state for HardFault and BusFault. SecureFault always targets Secure state.

- **System Handlers**: The system handlers handle the following system exceptions:
  - NMI
  - PendSV
  - SVCall
  - SysTick

  Most system handlers can be banked with separate handlers between Secure and Non-secure state. The SCB:AIRCR.BFHFNMINS bit controls the target state for NMI.

4.1.4 Vector Table

The Vector Table Offset Register (SCB:VTOR) in the System Control Block (SCB) determines the starting address of the vector table. The VTOR is banked so there is a VTOR_S and a VTOR_NS. The initial values of VTOR_S and VTOR_NS are 0. The vector table used depends on the target state of the exception. For exceptions targeting the Secure state, VTOR_S is used. For exceptions targeting the Non-secure state, VTOR_NS is used.

Table 4-2 shows the order of the exception vectors in the Secure and Non-secure vector tables. The least-significant bit of each vector is 1, indicating that the exception handler is written in Thumb® code.

Table 4-2. Vector Table With Security Extension

Exception Number	IRQ Number	Secure Vector	Non-secure Vector	Offset
62	46	IRQ46		0xF8
.		.		.
.		.		.
.		.		.
18	2	IRQ2	IRQ2	0x48
17	1	IRQ1	IRQ1	0x44
16	0	IRQ0	IRQ0	0x40
15	-1	SysTick_S	SysTick_NS	0x3C
14	-2	PendSV_S	PendSV_NS	0x38
13		Reserved	Reserved	0x30
12	-3	DebugMonitor	DebugMonitor	
11	-5	SVCall_S	SVCall_NS	0x2C
10		Reserved	Reserved	
9				
8				
7	-9	SecureFault	Reserved	0x1C
6	-11	UsageFault_S	UsageFault_NS	0x18
5	-12	BusFault_S	BusFault_NS	0x14
4	-13	MemManage_S	MemManage_NS	0x10
3	-13	HardFault_S	HardFault_NS	0x0C
2	-14	NMI_S	NMI_NS	0x08
1		Reset	Reset	0x04
		Initial SP Value	Initial SP Value	0x00

Because reset always targets Secure state, the Non-secure reset and Non-secure initial SP value are ignored by the hardware.

4.1.5 Exception Priorities

All exceptions have an assigned priority that is used to control both pre-emption and prioritization between pending exceptions. A lower priority value indicates a higher priority. You can configure priorities for all exceptions except Reset, HardFault, and NMI.

If software does not configure any priorities, then all exceptions with a configurable priority have a priority of 0.

Note

Configurable priorities are in the range 0-255. The Reset, HardFault, and NMI exceptions, with fixed negative priority values always have higher priority than any other exception.

For configurable priority exceptions, the target Security state also affects the programmed priority. Depending on the value of SCB:AIRCR.PRIS, the priority can be extended.

Extended Priority, the values in columns 2 and 3 must match, and increase from zero in increments of 32. The values in column 4 start from 128 and increase in increments of 16.

Table 4-3. Extended Priority

Priority Value [7:5]	Secure Priority	Non-secure priority when SCB:AIRCR.PRIS = 0	Non-secure priority when SCB:AIRCR.PRIS = 1
0	0	0	128
1	32	32	144
2	64	64	160
3	96	96	176
4	128	128	192
5	160	160	208
6	192	192	224
7	224	224	240

Assigning a higher priority value to IRQ[0] and a lower priority value to IRQ[1] means that IRQ[1] has higher priority than IRQ[0]. If both IRQ[1] and IRQ[0] are asserted, IRQ[1] is processed before IRQ[0].

If multiple pending exceptions have the same priority, the pending exception with the lowest exception number takes precedence. For example, if both IRQ[0] and IRQ[1] are pending and have the same priority, then IRQ[0] is processed before IRQ[1].

When the processor is executing an exception handler, the exception handler is preempted if a higher priority exception occurs. If an exception occurs with the same priority as the exception being handled, the handler is not preempted, irrespective of the exception number. However, the status of the new interrupt changes to pending.

4.1.6 Interrupt Priority Grouping

The NVIC supports software assigned priority levels. A priority level from 0 to 8 can be assign to an interrupt by writing to the most significant bits of the PRI_N field in the NVIC:IPRn register corresponding to the interrupt, see Section 2.7.11.

Only the group priority determines pre-emption of interrupt exceptions. When the processor is executing an interrupt exception handler, another interrupt with the same group priority as the interrupt being handled does not pre-empt the handler.

If multiple pending interrupts have the same group priority, the subpriority field determines the order in which the interrupts are processed. If multiple pending interrupts have the same group priority and subpriority, the interrupt with the lowest IRQ number is processed first.

If a pending Secure exception and a pending Non-secure exception both have the same group priority field value, the same subpriority field value, and the same exception number, the Secure exception takes precedence.

4.1.7 Exception Entry and Return

Descriptions of exception handling use the following terms.

- **Preemption**: An exception can preempt the current execution if its priority is higher than the current execution priority. When one exception preempts another, the exceptions are called nested exceptions.
- **Return**: This occurs when the exception handler is completed. The processor pops the stack and restores the processor state to the state it had before the interrupt occurred.
- **Tail-Chaining**: This mechanism speeds up exception servicing. On completion of an exception handler or during the return operation, if there is a pending exception that meets the requirements for exception entry, then the stack pop is skipped and control transfers directly to the new exception handler.
- **Late Arriving Interrupts**: This mechanism speeds up preemption. If a higher priority exception occurs during state saving for a previous exception, the processor switches to handle the higher priority exception and initiates the vector fetch for that exception. State saving may be affected by the late arrival depending on the stacking requirements of the original exception and the late-arriving exception. On return from the exception handler of the late-arriving exception, the normal tail-chaining rules apply.

4.1.7.1 Exception Entry

Exception entry occurs when there is a pending exception with sufficient priority and either the processor is in Thread mode, or the new exception is of higher priority than the exception being handled, in which case the new exception preempts the original exception.

When one exception preempts another, the exceptions are nested.

Sufficient priority means that the exception has higher priority than any limits set by the mask registers. An exception with lower priority than this is pending but is not handled by the processor.

When the processor takes an exception, unless the exception is a tail-chained or a late-arriving exception, the processor pushes information onto the current stack. This operation is referred to as stacking and the structure of the data stacked is referred as the stack frame.

The Cortex-M33 processor can automatically stack the architected floating-point state on exception entry.

4.1.7.2 Exception Return

Exception return occurs when the processor is in Handler mode and execution of one of the following instructions attempts to set the PC to an EXC_RETURN value:

- A POP or LDM instruction that loads the PC
- An LDR instruction that loads the PC
- A BX instruction using any register

The processor saves an EXC_RETURN value to the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. When the processor loads a value matching this pattern to the PC it detects that the operation is not a normal branch operation and, instead, that the exception is complete. As a result, it starts the exception return sequence. Bits[6:0] of the EXC_RETURN value indicate the required return stack, processor mode, Security state, and stack frame as shown in Table 4-4.

Table 4-4. Exception Return Behavior

Bits	Name	Description
[31:24]	PREFIX	Indicates that this is an EXC_RETURN value. This field reads as 0b11111111
[23:7]	-	Reserved, RES1
[6]	S	Indicates whether registers have been pushed to a Secure or Non-secure stack. 0: Non-secure stack used 1: Secure stack used.

Table 4-4. Exception Return Behavior (continued)

Bits	Name	Description
[5]	DCRS	Indicates whether the default stacking rules apply, or whether the called registers are already on the stack. 0: Stacking of the called saved registers is skipped 1: Default rules for stacking the called registers are followed
[4]	FType	In a PE with the Main and Floating-point Extensions: 0: The PE allocated space on the stack for FP context 1: The PE did not allocate space on the stack for FP context. In a PE without the Floating-point Extension, this bit is Reserved, RES1
[3]	Mode	Indicates the mode that was stacked from. 0: Handler mode 1: Thread mode
[2]	SPSEL	Indicates which stack contains the exception stack frame. 0: Main stack pointer 1: Process stack pointer
[1]	-	Reserved, RES0
[0]	ES	Indicates the Security state the exception was taken to. 0: Non-secure 1: Secure

4.2 Fault Handling

Faults can occur on instruction fetches, instruction execution, and data accesses. When a fault occurs, information about the cause of the fault is recorded in various registers, according to the type of fault. Faults are a subset of the exceptions.

Faults are generated by:

- A bus error on:
  - An instruction fetches or vector table load
  - A data access
- An internally-detected error such as an undefined instruction
- Attempting to execute an instruction from a memory region marked as Execute Never (XN)
- A privilege violation or an attempt to access an unmanaged region causing an MPU fault
- A security violation

4.2.1 Fault Types

Table 4-5 shows the types of fault, the handler used for the fault, the corresponding fault status register, and the register bit that indicates that the fault has occurred.

Table 4-5. Fault Types

Fault	Handler	Bit Name	Fault Status Register
Bus error on a vector read	HardFault	VECTTBL	HardFault Status Register
Fault escalated to a hard fault		FORCED	

Table 4-5. Fault Types (continued)

Fault	Handler	Bit Name	Fault Status Register
MPU or default memory map mismatch:	MemManage	-	MemManage Fault Status Register (MMFSR)
On instruction access		IACCVIOL	
On data access		DACCVIOL	
During exception stacking		MSTKERR	
During exception unstacking		MUNSKERR	
During lazy floating-point state preservation		MLSPERR	
Bus error:	BusFault	-	-
During exception stacking		STKERR	BusFault Status Register (BFSR)
During exception unstacking		UNSTKERR	
During instruction prefetch		IBUSERR	
During lazy floating-point state preservation		LSPERR	
Precise data bus error		PRECISERR	
Imprecise data bus error		IMPRECISERR	
Attempt to access a coprocessor	UsageFault	NOCP	UsageFault Status Register (UFSR)
Undefined instruction		UNDEFINSTR	
Attempt to enter an invalid instruction set state		INVSTATE	
Invalid EXC_RETURN value		INVPC	
Illegal unaligned load or store		UNALIGNED	
Stack overflow flag		STKOF	
Divide By 0		DIVBYZERO	
Lazy state error flag	SecureFault	LSERR	SecureFault Status Register (SFSR)
Lazy state preservation error flag		LSPERR	
Invalid transition flag		INVTRAN	
Attribution unit violation flag		AUVIOL	
Invalid exception return flag		INVER	
Invalid integrity signature flag		INVIS	
Invalid integrity signature flag		INVEP	

4.2.2 Fault Escalation to HardFault

All fault exceptions other than HardFault have configurable exception priority. Software can disable execution of the handlers for these faults.

Usually, the exception priority and the values of the exception mask registers determine whether the processor enters the fault handler. They also determine if one fault handler can preempt another.

In some situations, a fault with configurable priority is treated as a HardFault. This is called priority escalation, and the fault is described as escalated to HardFault. Escalation to HardFault occurs when:

- A fault handler causes the same kind of fault as the one it is servicing. This escalation to HardFault occurs because a fault handler cannot preempt itself; it must have the same priority as the current execution priority level.
- A fault handler causes a fault with the same or lower priority as the fault it is servicing. This is because the handler for the new fault cannot preempt the currently executing fault handler.
- An exception handler causes a fault for which the priority is the same as or lower than the currently executing exception.
- A fault occurs and the handler for that fault is not enabled.

If a BusFault occurs during a stack push when entering a BusFault handler, the BusFault does not escalate to a HardFault. This means that if a corrupted stack causes a fault, the fault handler executes even though the stack push for the handler failed. The fault handler operates but the stack contents are corrupted.

BusFaults and fixed priority exceptions can be designated as Secure or Non-secure under the control of SCB:AIRCR.BFHFNMINS. When AIRCR.BFHFMNINS is set to:

- 0: BusFaults and fixed priority exceptions are designated as Secure. The exceptions retain the prioritization of HardFault at -1 and NMI at -2.
- 1: BusFaults and fixed priority exceptions are designated as Non-secure. In this case, Secure HardFault is introduced at priority -3 to ensure that faults that target Secure state are recognized.

The Non-secure state cannot inhibit BusFaults and fixed priority exceptions which target Secure state. Therefore when faults and fixed priority exceptions are Secure, Non-secure FAULTMASK (FAULTMASK_NS) only inhibits programmable priority exceptions, making it equivalent to Non-secure PRIMASK (PRIMASK_NS).

Non-secure programmable priority exceptions are mapped to the regular priority range 0-255, if SCB:AIRCR.PRIS is clear. Non-secure programmable priority exceptions are mapped to the bottom half the regular priority range, 128-255, if AIRCR.PRIS is set to 1. Therefore, the FAULTMASK_NS sets the execution priority to 0x0 or 0x80, according to AIRCR.PRIS, to mask the Non-secure programmable priority exception only.

When BusFaults and fixed priority exceptions are Secure, FAULTMASK_S sets execution priority to -1 to inhibit everything up to and including HardFault.

When BusFaults and fixed priority exceptions are designated as Non-secure, FAULTMASK_NS boosts priority to -1 to inhibit everything up to Non-secure HardFault at priority -1, while FAULTMASK_S boosts priority to -3 to inhibit all faults and fixed priority exceptions including the Secure HardFault at priority -3.

Note

Only Reset can preempt the fixed priority Secure HardFault when SCB:AIRCR.BFHFNMINS is set to 1. A Secure HardFault when AIRCR.BFHFNMINS is set to 1 can preempt any exception other than Reset.

A Secure HardFault when AIRCR.BFHFNMINS is set to 0 can preempt any exception other than Reset, NMI, or another HardFault.

4.2.3 Fault Status Registers and Fault Address Registers

The fault status registers indicate the cause of a fault. For BusFaults, MemManage faults, and SecureFaults, the fault address register indicates the address that is accessed by the operation that caused the fault.

The processor has two physical fault address registers. One shared between the MMFAR_S (SCB:MMFAR), CPU_SAU:SFAR, and SCB:BFAR (only if AIRCR.BFHFNMINS is set to 0), and the other shared between the MMFAR_NS (SCB:MMFAR) and SCB:BFAR (only if AIRCR.BFHFNMINS is set to 1). These are targeted by Secure and Non-secure faults respectively.

For each physical fault address register, it is only possible to report the address of one fault at a time.

Each fault address register is updated when one of the *FARVALID bits is set for their respective faults in the associated *FSR register. BFARVALID is located in SCB:CFSR and SFARVALID is located in CPU_SAU:SFSR.

Any fault that targets a fault address register with one of its *FARVALID bits already set does not update the fault address. The *FARVALID bits must be cleared before another fault address can be reported.

4.2.4 Lockup

The processor enters a lockup state if a fault occurs when it cannot be serviced or escalated. When the processor is in lockup state, it does not execute any instructions.

The processor remains in lockup state until either:

- It is reset
- Preemption by a higher priority exception occurs
- It is halted by a debugger

Note

If lockup state occurs from a Secure HardFault when AIRCR.BFHFNMINS is set to 1 or the NMI handler, a subsequent NMI does not cause the processor to leave lockup state.

4.3 Security State Switches

Security State Transitions presents the possible security transitions, the instructions that can cause them, and any faults that may be generated.

Table 4-6. Security State Transitions

Current Security State	Security Attribute of the Branch Target Address	Security State Change
Secure	Non-secure	Change to Non-secure state if the branch was a BXNS or BLXNS instruction with the LSB of the target address set to 0. Otherwise, a SecureFault is generated.
Non-secure	Secure and Non-secure callable	Change to Secure state if the branch target address contains an SG instruction. If the target address does not contain an SG a SecureFault is generated.
Non-Secure	Secure and not Non-secure callable	A SecureFault is generated.

Secure software can call a Non-secure function using the BLXNS instruction. When this happens, the LR is set to a special value called FNC_RETURN, and the return address and XPSR is saved onto the Secure stack. Return from Non-secure state to Secure state is triggered when one of the following instructions attempts to set the PC to an FNC_RETURN value:

- A POP or LDM instruction that loads the PC
- An LDR instruction that loads the PC
- A BX instruction using any register

When a return from Non-secure state to Secure state occurs the processor restores the program counter and XPSR from the Secure stack.

Any scenario not listed in the table triggers a SecureFault. For example:

- Sequential instructions that cross security attributes from Secure to Non-secure.
  - A 32-bit instruction fetch that crosses regions with different security attributes.

4.4 Event Fabric

4.4.1 Introduction

The event fabric is a combinational router between event sources/publishers and event subscribers. The event inputs are routed to a central event-bus where a subscriber can select the appropriate events and output those as inputs to peripherals.

Several of the events (signals) are statically routed, and a small number of configurable output lines go to the event subscribers. A configurable output line from a subscriber can choose from a list of several input events available to the specific subscriber in question.

Subscribers output event signaling is identical to input signaling. That is, events are simply passed through the event fabric as presented to the input ports. Possible event types include system hardware interrupts and DMA triggers.

All ULL/AON event inputs are considered level-triggered events active high. SVT/MCU event inputs can be either active high level or pulse triggered events. Events like DMA triggers can be level-type signals. The event fabric is not a peripheral in itself, but rather a block of routing between the peripherals and more. The lines that have configurable inputs are controlled by selection registers that are connected to a MUX, which forward the selected input in the subscriber to the peripherals.

Figure 4-1 shows a simple illustration of the event fabric concept

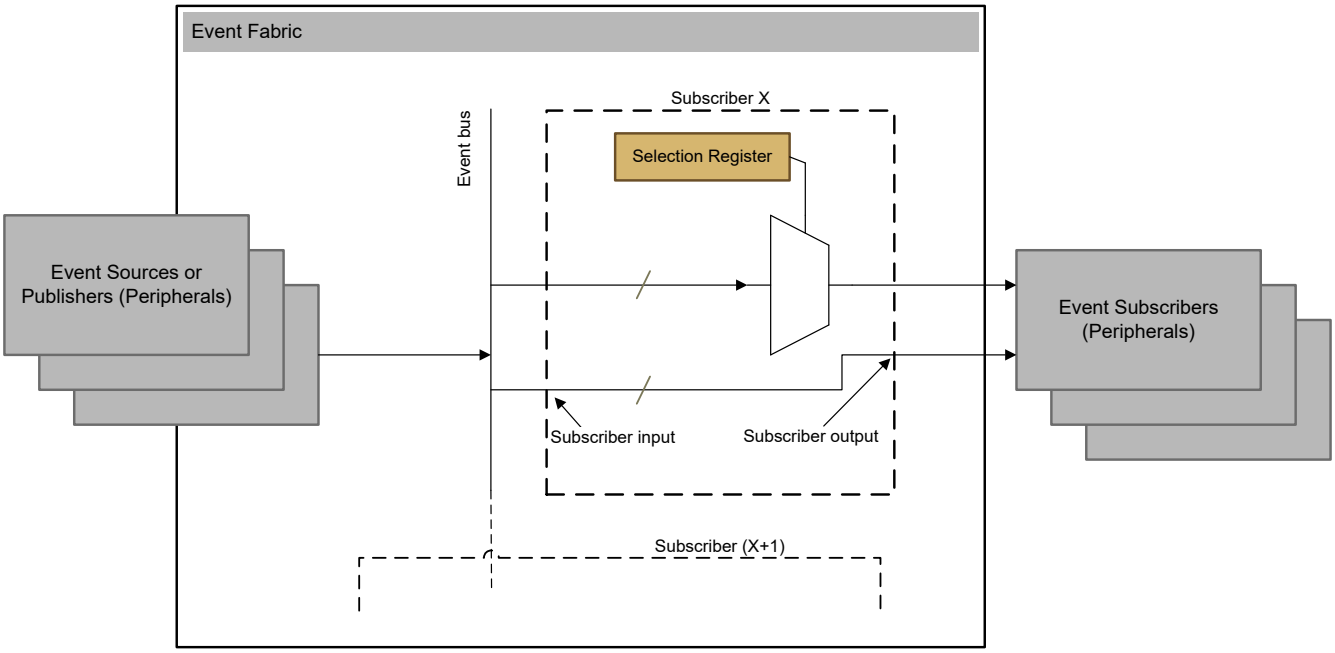

Figure 4-1. Event Fabric Concept

4.4.2 Overview

There are two main event fabric blocks. The MCU event fabric and the AON event fabric. The MCU event fabric is in the SVT/MCU power domain and is configured with the EVTSVT registers. The AON event fabric is in the ULL/AON domain and is configured with the EVTULL registers.

Figure 4-2 shows a simplified overview of the two modules together. The MCU event fabric is one of the subscribers to the AON event fabric.

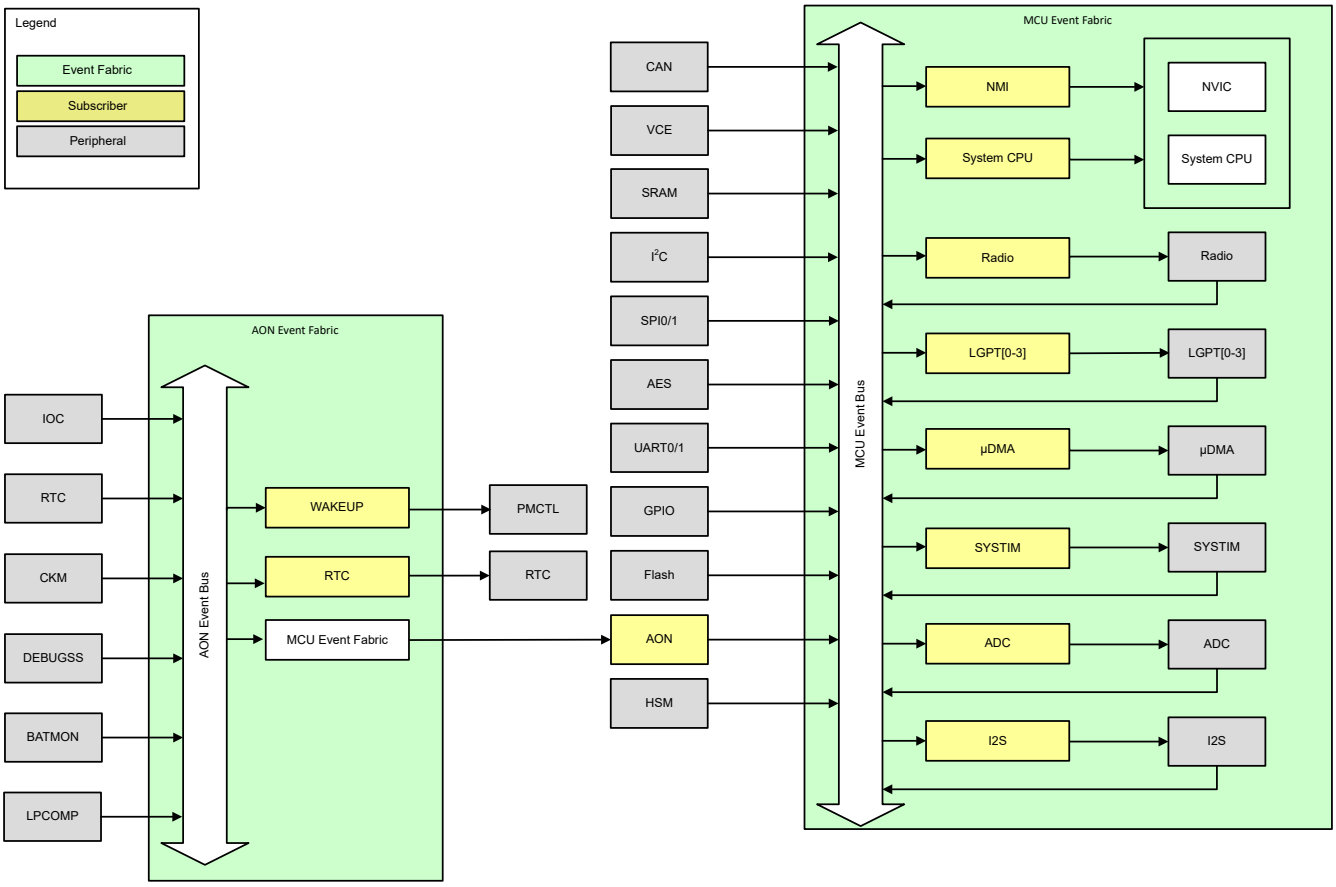

Figure 4-2. Event Fabric Overview (Simplified)

4.4.3 Registers

The event fabric has two types of registers. The first type, a configuration register, is used to control and report the selection settings for a subscriber output. For each subscriber output, an address is mapped for a read register that contains a value representing the selection of the input event currently set for that subscriber output. For nonconfigurable outputs, only a read-only register is implemented. A read to that address returns the static, predefined value. The second type of register in the event fabric are description registers and one register that can be used for observation of event signals on the pads.

4.4.4 AON Event Fabric

The AON event fabric resides in the AON voltage domain.

4.4.4.1 AON Common Input Events List

Table 4-7 lists the input events for the AON event fabric (event numbers 0x2 to 0x7). The sources for these events are considered level-triggered active high.

4.4.4.2 AON Event Subscribers

There are three subscribers in the AON event fabric as can be seen in Figure 4-2. The first subscriber is the MCU event fabric, which resides in the MCU power domain. The other two subscribers, the PMCTL and RTC, are presented in the following subsections.

4.4.4.3 Power Management Controller (PMCTL)

The PMCTL subscriber has 6 programmable events in AON event fabric, which are ORed together to form a single wake-up event to PMCTL configurable via the EVTULL.WKUPMASK register. This wake-up event is used to trigger the wakeup of the MCU power domain from Standby mode. Any of the events listed in Table 4-7 can

be chosen as input by selecting the appropriate event publisher or publishers. By default, this register is set to 0, meaning that no publishers are selected to drive the wake-up event towards PMCTL.

4.4.4.4 Real Time Clock (RTC)

The RTC has a programmable event, which can be configured in the EVTULL.RTCCPTSEL register. This register can be used to choose between 6 programmable sources within AON.

4.4.4.5 AON to MCU Event Fabric

The 6 AON events are also exported separately as a bus to MCU Event Fabric and can be used as publishers within MCU peripherals.

Note

Since the events from AON are double synchronized within MCU event fabric before being used as publishers, care must be taken to make sure that when the AON events are cleared, a subsequent event does not get set immediately (within four CLKSVT clock cycles). This is so that a separate rising edge is generated for the second event. Otherwise the second event can get missed if the cleared AON event pulse does not get synchronized within MCU event fabric before getting set again.

4.4.5 MCU Event Fabric

The MCU event fabric resides in the MCU power domain and routes signals between most of the peripherals and different internal blocks. Only a few of the subscribers in the MCU event fabric are described in this section. For more information on the remaining subscribers, refer to the specific peripheral chapters for the appropriate consumer (peripheral) for that specific subscriber.

4.4.5.1 Common Input Event List

Table 4-7 lists the input events for the MCU event fabric.

Table 4-7. Common Input Event List

Event Number	Name	Description
0x0	NONE	Always inactive
0x2	AON_PMU_COMB	PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD.EVENT
0x3	AON_CKM_COMB	CKMD combined interrupt request, interrupt flags can be found here CKMD.MIS
0x4	AON_RTC_COMB	AON_RTC event, controlled by the RTC.IMASK setting
0x5	AON_DBG_COMB	DebugSS combined interrupt, interrupt flags can be found here DBGSS.MIS
0x6	AON_LPMCMP_IRQ	AON LPCMP interrupt, controlled by SYS0.LPCMPCFG
0x7	AON_IOC_COMB	IOC synchronous combined event, controlled by IOC.EVTCFG
0x10	SYSTIM_COMB	SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS
0x11	GPIO_COMB	GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS
0x12	GPIO_EVT0	GPIO generic published event 0, controlled by GPIO:EVTCFG
0x13	FLASH_IRQ	NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS
0x14	LRFD_IRQ0	LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0
0x15	LRFD_IRQ1	LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1
0x16	LRFD_IRQ2	LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2
0x17	SPI0_COMB	SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS
0x18	ADC_COMB	ADC combined interrupt request, interrupt flags can be found here ADC:MIS0
0x19	ADC_EVT	ADC general published event, interrupt flags can be found here ADC:MIS1
0x1A	LGPT0_COMB	LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS

Table 4-7. Common Input Event List (continued)

Event Number	Name	Description
0x1B	LGPT1_COMB	LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS
0x1C	DMA_DONE_COMB	DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE
0x1D	DMA_ERR	DMA bus error, corresponds to DMA:ERROR.STATUS
0x1E	AES_COMB	AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS
0x1F	UART0_COMB	UART0 combined interrupt, interrupt flags are found here UART0:MIS
0x20	I2C0_IRQ	Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS
0x21	SYSTIM_HB	SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT
0x22	SYSTIM_LT	SYSTIM interrupt driven by synchronizing LFTICK signal to SVT clock
0x23	SYSTIM0	SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0
0x24	SYSTIM1	SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1
0x25	SYSTIM2	SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2
0x26	SYSTIM3	SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3
0x27	SYSTIM4	SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4
0x28	LGPT0C0	LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting
0x29	LGPT0C1	LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting
0x2A	LGPT0C2	LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting
0x2B	LGPT0_DMA	LGPT0 DMA request event, controlled by LGPT0:DMA settingd
0x2C	LGPT0_ADC	LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting
0x2D	LGPT1C0	LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting
0x2E	LGPT1C1	LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting
0x2F	LGPT1C2	LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting
0x30	LGPT1_DMA	LGPT1 DMA request event, controlled by LGPT1:DMA setting
0x31	LGPT1_ADC	LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting
0x32	LRFD_EVT0	LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0
0x33	LRFD_EVT1	LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1
0x34	LRFD_EVT2	LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2
0x35	UART1_COMB	UART1 combined interrupt, interrupt flags are found here UART0:MIS
0x36	LGPT2C0	LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting
0x37	LGPT2C1	LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting
0x38	LGPT2C2	LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting
0x39	LGPT2_COMB	LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS
0x3A	LGPT2_DMA	LGPT2 DMA request event, controlled by LGPT2:DMA setting
0x3B	LGPT2_ADC	LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting
0x3C	LGPT3C0	LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting
0x3D	LGPT3C1	LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting
0x3E	LGPT3C2	LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting
0x3F	LGPT3_COMB	LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS
0x40	LGPT3_DMA	LGPT3 DMA request event, controlled by LGPT3:DMA setting
0x41	LGPT3_ADC	LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting
0x42	I2S_IRQ	I2S interrupt event, controlled by I2S:IRQMASK

Table 4-7. Common Input Event List (continued)

Event Number	Name	Description
0x43	CAN_IRQ	MCAN interrupt event, interrupt flags can be found here MCAN:MIS0
0x44	CAN_EVT	MCAN general event, interrupt flags can be found here MCAN:MIS1
0x45	SPI1_COMB	SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS
0x46	APU_IRQ	APU combined interrupt, interrupt flags can be found in APU:MIS
0x4B	GPIO_EVT1	GPIO generic published event 1, controlled by GPIO:EVTCFG
0x4C	SYSTIM5	SYSTIM Channel 5 event, event flag is SYSTIM:MIS.EVT5

4.4.5.2 MCU Event Subscribers

There are six peripheral subscribers for the MCU event fabric. These subscribers are different peripherals that must be configured differently according to the purpose of those specific peripherals. The following subscribers are not described in this chapter, but rather in each of the corresponding peripheral chapters:

- Micro Direct Memory Access (µDMA) - Chapter 19
- Four Low Power General-Purpose Timers - Chapter 12
- System Timer - Chapter 15
- Radio - Chapter 28
- ADC - Chapter 21
- I^2S - Chapter 26

The following two subscribers are described below:

- System CPU
- Non-maskable Interrupt (NMI) to System CPU

4.4.5.2.1 System CPU

Interrupts with vectors numbered from 16 to 76 (58 total) are sourced by the events routed in the MCU event fabric to the system CPU.

Seven of the interrupts are configurable out from the sources present in Table 4-7, and the other interrupts are fixed routes from system peripherals to the CPU. For information on the available routing see the EVTSVT.CPUIRQnSEL descriptions.

4.4.5.2.2 Non-Maskable Interrupt (NMI)

The NMI subscriber is driven by SRAM parity error output.

EVTSVT.NMI.SRAM_EVT_STA provides information about the current parity error state when read. When written to 1, this field can be cleared. For debug purposes, EVTSVT.NMI.SRAM_EVT_SET field can be written to 1, to force an NMI event to the CPU.

4.5 Digital Test Bus (DTB)

Both MCU and AON event fabric structures include a feature to enable porting a set of selected internal signals to the pads for observation purposes.

The signals are grouped into several 16-bit buses, which can be selected via DTB.SEL register. A value of zero within DTB.SEL disables this feature and only zeros are exported.

The signals that can be observed from within EVTULL are:

Table 4-8. EVTULL Signals

EVTULL.DTB[0] SEL bit	Bits	Observed signal
0	[15:0]	All zeros

Table 4-8. EVTULL Signals (continued)

1	[15:7]	All zeros
	[6]	AON_PMU_COMB event
	[5]	AON_CKM_COMB event
	[4]	AON_RTC_COMB event
	[3]	AON_DBG_COMB event
	[2]	AON_LPMCMP_IRQ event
	[1]	AON_IOC_COMB event
	[0]	Event selected for wakeup via EVTULL.WKUPMASK

The signals that can be observed from within EVTSVT are:

Table 4-9. EVTSVT Signals

EVTSVT.DTB[1:0] SEL bit field	Bits	Observed signal
0	[15:0]	All zeros
1	[15]	SYSTIM_COMB event
	[14]	GPIO_COMB event
	[13]	FLASH_IRQ event
	[12]	LRFD_EVT0 event
	[11]	LRFD_EVT1 event
	[10]	LRFD_EVT2 event
	[9]	SPI0_COMB event
	[8]	ADC_COMB event
	[7]	LGPT0_COMB event
	[6]	LGPT1_COMB event
	[5]	DMA_DONE_COMB event
	[4]	AES_COMB event
	[3]	UART0_COMB event
	[2]	I2C0_IRQ event
	[1]	UART1_COMB event
	[0]	LGPT2_COMB event
2	[15]	LGPT3_COMB event
	[14]	I2S_IRQ event
	[13]	CAN_IRQ event
	[12]	SPI1_COMB event
	[11]	APU_IRQ event
	[10]	Event selected via EVTSVT.CPUIRQ0SEL
	[9]	Event selected via EVTSVT.CPUIRQ2SEL
	[8]	Event selected via EVTSVT.SYSTIMC1SEL
	[7]	DMA burst request selected via EVTSVT.DMACH0SEL
	[6]	DMA single request selected via EVTSVT.DMACH0SEL
	[5]	DMA burst request selected via EVTSVT.DMACH1SEL
	[4]	DMA single request selected via EVTSVT.DMACH1SEL
	[3]	DMA burst request selected via EVTSVT.DMACH2SEL
	[2]	DMA single request selected via EVTSVT.DMACH2SEL
	[1]	DMA burst request selected via EVTSVT.DMACH3SEL
	[0]	DMA single request selected via EVTSVT.DMACH3SEL

Table 4-9. EVTSVT Signals (continued)

3	[15]	DMA burst request selected via EVTSVT.DMACH4SEL
	[14]	DMA single request selected via EVTSVT.DMACH4SEL
	[13]	DMA burst request selected via EVTSVT.DMACH5SEL
	[12]	DMA single request selected via EVTSVT.DMACH5SEL
	[11]	DMA burst request selected via EVTSVT.DMACH6SEL
	[10]	DMA single request selected via EVTSVT.DMACH6SEL
	[9]	DMA burst request selected via EVTSVT.DMACH7SEL
	[8]	DMA single request selected via EVTSVT.DMACH7SEL
	[7]	DMA burst request selected via EVTSVT.DMACH8SEL
	[6]	DMA single request selected via EVTSVT.DMACH8SEL
	[5]	DMA burst request selected via EVTSVT.DMACH9SEL
	[4]	DMA single request selected via EVTSVT.DMACH9SEL
	[3]	DMA burst request selected via EVTSVT.DMACH10SEL
	[2]	DMA single request selected via EVTSVT.DMACH10SEL
	[1]	DMA burst request selected via EVTSVT.DMACH11SEL
	[0]	DMA single request selected via EVTSVT.DMACH11SEL

Further details about routing these set of signals to the pads can be found in Chapter 22.

4.6 EVTSVT Registers

Table 4-10 lists the memory-mapped registers for the EVTSVT registers. All register offset addresses not listed in Table 4-10 should be considered as reserved locations and the register contents should not be modified.

Table 4-10. EVTSVT Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.	Section 4.6.1
4h	DESCEX	Extended Description Register. This register provides configuration details of the IP to software drivers and end users.	Section 4.6.2
64h	DTB	Digital test bus control register. This register can be used to bring out IP internal signals to the pads for observation. 16 signals can be observed per select value.	Section 4.6.3
400h	NMI	CPU NMI Interrupt Register	Section 4.6.4
404h	CPUIRQ0SEL	Output Selection for CPU Interrupt CPUIRQ0	Section 4.6.5
408h	CPUIRQ1SEL	Output Selection for CPU Interrupt CPUIRQ1	Section 4.6.6
40Ch	CPUIRQ2SEL	Output Selection for CPU Interrupt CPUIRQ2	Section 4.6.7
410h	CPUIRQ3SEL	Output Selection for CPU Interrupt CPUIRQ3	Section 4.6.8
414h	CPUIRQ4SEL	Output Selection for CPU Interrupt CPUIRQ4	Section 4.6.9
418h	CPUIRQ5SEL	Output Selection for CPU Interrupt CPUIRQ5	Section 4.6.10
41Ch	CPUIRQ6SEL	Output Selection for CPU Interrupt CPUIRQ6	Section 4.6.11
420h	CPUIRQ7SEL	Output Selection for CPU Interrupt CPUIRQ7	Section 4.6.12
424h	CPUIRQ8SEL	Output Selection for CPU Interrupt CPUIRQ8	Section 4.6.13
428h	CPUIRQ9SEL	Output Selection for CPU Interrupt CPUIRQ9	Section 4.6.14
42Ch	CPUIRQ10SEL	Output Selection for CPU Interrupt CPUIRQ10	Section 4.6.15
430h	CPUIRQ11SEL	Output Selection for CPU Interrupt CPUIRQ11	Section 4.6.16
434h	CPUIRQ12SEL	Output Selection for CPU Interrupt CPUIRQ12	Section 4.6.17
438h	CPUIRQ13SEL	Output Selection for CPU Interrupt CPUIRQ13	Section 4.6.18
43Ch	CPUIRQ14SEL	Output Selection for CPU Interrupt CPUIRQ14	Section 4.6.19
440h	CPUIRQ15SEL	Output Selection for CPU Interrupt CPUIRQ15	Section 4.6.20
444h	CPUIRQ16SEL	Output Selection for CPU Interrupt CPUIRQ16	Section 4.6.21
448h	CPUIRQ17SEL	Output Selection for CPU Interrupt CPUIRQ17	Section 4.6.22
44Ch	CPUIRQ18SEL	Output Selection for CPU Interrupt CPUIRQ18	Section 4.6.23
450h	CPUIRQ19SEL	Output Selection for CPU Interrupt CPUIRQ19	Section 4.6.24
454h	CPUIRQ20SEL	Output Selection for CPU Interrupt CPUIRQ20	Section 4.6.25
458h	CPUIRQ21SEL	Output Selection for CPU Interrupt CPUIRQ21	Section 4.6.26
45Ch	CPUIRQ22SEL	Output Selection for CPU Interrupt CPUIRQ22	Section 4.6.27
460h	CPUIRQ23SEL	Output Selection for CPU Interrupt CPUIRQ23	Section 4.6.28
464h	CPUIRQ24SEL	Output Selection for CPU Interrupt CPUIRQ24	Section 4.6.29
468h	CPUIRQ25SEL	Output Selection for CPU Interrupt CPUIRQ25	Section 4.6.30
46Ch	CPUIRQ26SEL	Output Selection for CPU Interrupt CPUIRQ26	Section 4.6.31
470h	CPUIRQ27SEL	Output Selection for CPU Interrupt CPUIRQ27	Section 4.6.32
474h	CPUIRQ28SEL	Output Selection for CPU Interrupt CPUIRQ28	Section 4.6.33
478h	CPUIRQ29SEL	Output Selection for CPU Interrupt CPUIRQ29	Section 4.6.34
47Ch	CPUIRQ30SEL	Output Selection for CPU Interrupt CPUIRQ30	Section 4.6.35
480h	CPUIRQ31SEL	Output Selection for CPU Interrupt CPUIRQ31	Section 4.6.36
484h	CPUIRQ32SEL	Output Selection for CPU Interrupt CPUIRQ32	Section 4.6.37

Table 4-10. EVTSVT Registers (continued)

Offset	Acronym	Register Name	Section
488h	SYSTIMC0SEL	Output Selection for SYSTIMC0	Section 4.6.38
48Ch	SYSTIMC1SEL	Output Selection for SYSTIMC1	Section 4.6.39
490h	SYSTIMC2SEL	Output Selection for SYSTIMC2	Section 4.6.40
494h	SYSTIMC3SEL	Output Selection for SYSTIMC3	Section 4.6.41
498h	SYSTIMC4SEL	Output Selection for SYSTIMC4	Section 4.6.42
49Ch	SYSTIMC5SEL	Output Selection for SYSTIMC5	Section 4.6.43
4A0h	ADCTRGSEL	Output Selection for ADCTRG	Section 4.6.44
4A4h	LGPTSYNCSEL	Output Selection for LGPTSYNC	Section 4.6.45
4A8h	LGPT0IN0SEL	Output Selection for LGPT0IN0	Section 4.6.46
4ACh	LGPT0IN1SEL	Output Selection for LGPT0IN1	Section 4.6.47
4B0h	LGPT0IN2SEL	Output Selection for LGPT0IN2	Section 4.6.48
4B4h	LGPT0TENSEL	Output Selection for LGPT0TEN	Section 4.6.49
4B8h	LGPT1IN0SEL	Output Selection for LGPT1IN0	Section 4.6.50
4BCh	LGPT1IN1SEL	Output Selection for LGPT1IN1	Section 4.6.51
4C0h	LGPT1IN2SEL	Output Selection for LGPT1IN2	Section 4.6.52
4C4h	LGPT1TENSEL	Output Selection for LGPT1TEN	Section 4.6.53
4C8h	LGPT2IN0SEL	Output Selection for LGPT2IN0	Section 4.6.54
4CCh	LGPT2IN1SEL	Output Selection for LGPT2IN1	Section 4.6.55
4D0h	LGPT2IN2SEL	Output Selection for LGPT2IN2	Section 4.6.56
4D4h	LGPT2TENSEL	Output Selection for LGPT2TEN	Section 4.6.57
4D8h	LGPT3IN0SEL	Output Selection for LGPT3IN0	Section 4.6.58
4DCh	LGPT3IN1SEL	Output Selection for LGPT3IN1	Section 4.6.59
4E0h	LGPT3IN2SEL	Output Selection for LGPT3IN2	Section 4.6.60
4E4h	LGPT3TENSEL	Output Selection for LGPT3TEN	Section 4.6.61
4E8h	LRFDIN0SEL	Output Selection for LRFDIN0	Section 4.6.62
4ECh	LRFDIN1SEL	Output Selection for LRFDIN1	Section 4.6.63
4F0h	LRFDIN2SEL	Output Selection for LRFDIN2	Section 4.6.64
4F4h	I2SSTMPSEL	Output Selection for I2SSTMP	Section 4.6.65
C00h	DMACH0SEL	Output Selection for DMA CH0	Section 4.6.66
C04h	DMACH1SEL	Output Selection for DMA CH1	Section 4.6.67
C08h	DMACH2SEL	Output Selection for DMA CH2	Section 4.6.68
C0Ch	DMACH3SEL	Output Selection for DMA CH3	Section 4.6.69
C10h	DMACH4SEL	Output Selection for DMA CH4	Section 4.6.70
C14h	DMACH5SEL	Output Selection for DMA CH5	Section 4.6.71
C18h	DMACH6SEL	Output Selection for DMA CH6	Section 4.6.72
C1Ch	DMACH7SEL	Output Selection for DMA CH7	Section 4.6.73
C20h	DMACH10SEL	Output Selection for DMA CH10	Section 4.6.74
C24h	DMACH11SEL	Output Selection for DMA CH11	Section 4.6.75
C28h	DMACH8SEL	Output Selection for DMA CH8	Section 4.6.76
C2Ch	DMACH9SEL	Output Selection for DMA CH9	Section 4.6.77

Complex bit access types are encoded to fit into small table cells. Table 4-11 shows the codes that are used for access types in this section.

Table 4-11. EVTSVT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

4.6.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 4-12.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 4-12. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	3045h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

4.6.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 4-13.

Return to the Summary Table.

Extended Description Register. This register provides configuration details of the IP to software drivers and end users.

Table 4-13. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	IDMA	R	Eh	Number of DMA input channels
21-17	NDMA	R	10h	Number of DMA output channels
16	PD	R	0h	Power Domain.;0 : SVT; 1 : ULL
15-8	NSUB	R	3Dh	Number of Subscribers
7-0	NPUB	R	39h	Number of Publishers

4.6.3 DTB Register (Offset = 64h) [Reset = 00000000h]

DTB is shown in Table 4-14.

Return to the Summary Table.

Digital test bus control register. This register can be used to bring out IP internal signals to the pads for observation. 16 signals can be observed per select value.

Table 4-14. DTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
1-0	SEL	R/W	0h	Digital test bus selection mux control.;Non-zero select values output a 16 bit selected group of signals per value.

4.6.4 NMI Register (Offset = 400h) [Reset = 00000000h]

NMI is shown in Table 4-15.

Return to the Summary Table.

CPU NMI Interrupt Register

Table 4-15. NMI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
16	SRAM_EVT_SET	W	0h	Writing a value of 1'b1 sets the corresponding NMI status flag
15-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
0	SRAM_EVT_STA	R/W	0h	Read value indicates the current state of NMI flops. ;Writing a value of 1'b1 clears the NMI status when set.

4.6.5 CPUIRQ0SEL Register (Offset = 404h) [Reset = 00000000h]

CPUIRQ0SEL is shown in Table 4-16.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ0

Table 4-16. CPUIRQ0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-16. CPUIRQ0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-16. CPUIRQ0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.6 CPUIRQ1SEL Register (Offset = 408h) [Reset = 00000000h]

CPUIRQ1SEL is shown in Table 4-17.

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Output Selection for CPU Interrupt CPUIRQ1

Table 4-17. CPUIRQ1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-17. CPUIRQ1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-17. CPUIRQ1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.7 CPUIRQ2SEL Register (Offset = 40Ch) [Reset = 00000000h]

CPUIRQ2SEL is shown in Table 4-18.

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Output Selection for CPU Interrupt CPUIRQ2

Table 4-18. CPUIRQ2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-18. CPUIRQ2SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-18. CPUIRQ2SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.8 CPUIRQ3SEL Register (Offset = 410h) [Reset = 00000000h]

CPUIRQ3SEL is shown in Table 4-19.

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Output Selection for CPU Interrupt CPUIRQ3

Table 4-19. CPUIRQ3SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-19. CPUIRQ3SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-19. CPUIRQ3SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.9 CPUIRQ4SEL Register (Offset = 414h) [Reset = 00000000h]

CPUIRQ4SEL is shown in Table 4-20.

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Output Selection for CPU Interrupt CPUIRQ4

Table 4-20. CPUIRQ4SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-20. CPUIRQ4SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-20. CPUIRQ4SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.10 CPUIRQ5SEL Register (Offset = 418h) [Reset = 00000000h]

CPUIRQ5SEL is shown in Table 4-21.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ5

Table 4-21. CPUIRQ5SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	11h	Read only selection value 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS

4.6.11 CPUIRQ6SEL Register (Offset = 41Ch) [Reset = 00000000h]

CPUIRQ6SEL is shown in Table 4-22.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ6

Table 4-22. CPUIRQ6SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	14h	Read only selection value 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0

4.6.12 CPUIRQ7SEL Register (Offset = 420h) [Reset = 00000000h]

CPUIRQ7SEL is shown in Table 4-23.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ7

Table 4-23. CPUIRQ7SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	15h	Read only selection value 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1

4.6.13 CPUIRQ8SEL Register (Offset = 424h) [Reset = 00000000h]

CPUIRQ8SEL is shown in Table 4-24.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ8

Table 4-24. CPUIRQ8SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	1Ch	Read only selection value 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE

4.6.14 CPUIRQ9SEL Register (Offset = 428h) [Reset = 00000000h]

CPUIRQ9SEL is shown in Table 4-25.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ9

Table 4-25. CPUIRQ9SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	1Eh	Read only selection value 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS

4.6.15 CPUIRQ10SEL Register (Offset = 42Ch) [Reset = 00000000h]

CPUIRQ10SEL is shown in Table 4-26.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ10

Table 4-26. CPUIRQ10SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	17h	Read only selection value 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS

4.6.16 CPUIRQ11SEL Register (Offset = 430h) [Reset = 00000000h]

CPUIRQ11SEL is shown in Table 4-27.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ11

Table 4-27. CPUIRQ11SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	1Fh	Read only selection value 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS

4.6.17 CPUIRQ12SEL Register (Offset = 434h) [Reset = 00000000h]

CPUIRQ12SEL is shown in Table 4-28.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ12

Table 4-28. CPUIRQ12SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	20h	Read only selection value 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS

4.6.18 CPUIRQ13SEL Register (Offset = 438h) [Reset = 00000000h]

CPUIRQ13SEL is shown in Table 4-29.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ13

Table 4-29. CPUIRQ13SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	1Ah	Read only selection value 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS

4.6.19 CPUIRQ14SEL Register (Offset = 43Ch) [Reset = 00000000h]

CPUIRQ14SEL is shown in Table 4-30.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ14

Table 4-30. CPUIRQ14SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	1Bh	Read only selection value 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS

4.6.20 CPUIRQ15SEL Register (Offset = 440h) [Reset = 00000000h]

CPUIRQ15SEL is shown in Table 4-31.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ15

Table 4-31. CPUIRQ15SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	18h	Read only selection value 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0

4.6.21 CPUIRQ16SEL Register (Offset = 444h) [Reset = 00000000h]

CPUIRQ16SEL is shown in Table 4-32.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ16

Table 4-32. CPUIRQ16SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-32. CPUIRQ16SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-32. CPUIRQ16SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.22 CPUIRQ17SEL Register (Offset = 448h) [Reset = 00000000h]

CPUIRQ17SEL is shown in Table 4-33.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ17

Table 4-33. CPUIRQ17SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-33. CPUIRQ17SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-33. CPUIRQ17SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.23 CPUIRQ18SEL Register (Offset = 44Ch) [Reset = 00000000h]

CPUIRQ18SEL is shown in Table 4-34.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ18

Table 4-34. CPUIRQ18SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	39h	Read only selection value 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS

4.6.24 CPUIRQ19SEL Register (Offset = 450h) [Reset = 00000000h]

CPUIRQ19SEL is shown in Table 4-35.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ19

Table 4-35. CPUIRQ19SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	3Fh	Read only selection value 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS

4.6.25 CPUIRQ20SEL Register (Offset = 454h) [Reset = 00000000h]

CPUIRQ20SEL is shown in Table 4-36.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ20

Table 4-36. CPUIRQ20SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	42h	Read only selection value 42h = I2S interrupt event, controlled by I2S:IRQMASK

4.6.26 CPUIRQ21SEL Register (Offset = 458h) [Reset = 00000000h]

CPUIRQ21SEL is shown in Table 4-37.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ21

Table 4-37. CPUIRQ21SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	43h	Read only selection value 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0

4.6.27 CPUIRQ22SEL Register (Offset = 45Ch) [Reset = 00000000h]

CPUIRQ22SEL is shown in Table 4-38.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ22

Table 4-38. CPUIRQ22SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	35h	Read only selection value 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS

4.6.28 CPUIRQ23SEL Register (Offset = 460h) [Reset = 00000000h]

CPUIRQ23SEL is shown in Table 4-39.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ23

Table 4-39. CPUIRQ23SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	45h	Read only selection value 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS

4.6.29 CPUIRQ24SEL Register (Offset = 464h) [Reset = 00000000h]

CPUIRQ24SEL is shown in Table 4-40.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ24

Table 4-40. CPUIRQ24SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	46h	Read only selection value 46h = APU IRQ

4.6.30 CPUIRQ25SEL Register (Offset = 468h) [Reset = 00000000h]

CPUIRQ25SEL is shown in Table 4-41.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ25

Table 4-41. CPUIRQ25SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	47h	Read only selection value 47h = HSM Secure IRQ

4.6.31 CPUIRQ26SEL Register (Offset = 46Ch) [Reset = 00000000h]

CPUIRQ26SEL is shown in Table 4-42.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ26

Table 4-42. CPUIRQ26SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	48h	Read only selection value 48h = HSM Non-secure IRQ

4.6.32 CPUIRQ27SEL Register (Offset = 470h) [Reset = 00000000h]

CPUIRQ27SEL is shown in Table 4-43.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ27

Table 4-43. CPUIRQ27SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	49h	Read only selection value 49h = HSM OTP IRQ

4.6.33 CPUIRQ28SEL Register (Offset = 474h) [Reset = 00000000h]

CPUIRQ28SEL is shown in Table 4-44.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ28

Table 4-44. CPUIRQ28SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	2h	Read only selection value 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT

4.6.34 CPUIRQ29SEL Register (Offset = 478h) [Reset = 00000000h]

CPUIRQ29SEL is shown in Table 4-45.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ29

Table 4-45. CPUIRQ29SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	3h	Read only selection value 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS

4.6.35 CPUIRQ30SEL Register (Offset = 47Ch) [Reset = 00000000h]

CPUIRQ30SEL is shown in Table 4-46.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ30

Table 4-46. CPUIRQ30SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	4h	Read only selection value 4h = AON_RTC event, controlled by the RTC:IMASK setting

4.6.36 CPUIRQ31SEL Register (Offset = 480h) [Reset = 00000000h]

CPUIRQ31SEL is shown in Table 4-47.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ31

Table 4-47. CPUIRQ31SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	6h	Read only selection value 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG

4.6.37 CPUIRQ32SEL Register (Offset = 484h) [Reset = 00000000h]

CPUIRQ32SEL is shown in Table 4-48.

Return to the Summary Table.

Output Selection for CPU Interrupt CPUIRQ32

Table 4-48. CPUIRQ32SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	7h	Read only selection value 7h = IOC synchronous combined event, controlled by IOC:EVTCFG

4.6.38 SYSTIMC0SEL Register (Offset = 488h) [Reset = 00000000h]

SYSTIMC0SEL is shown in Table 4-49.

Return to the Summary Table.

Output Selection for SYSTIMC0

Table 4-49. SYSTIMC0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	4h	Read only selection value 4h = AON_RTC event, controlled by the RTC:IMASK setting

4.6.39 SYSTIMC1SEL Register (Offset = 48Ch) [Reset = 00000000h]

SYSTIMC1SEL is shown in Table 4-50.

Return to the Summary Table.

Output Selection for SYSTIMC1

Table 4-50. SYSTIMC1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-50. SYSTIMC1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-50. SYSTIMC1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.40 SYSTIMC2SEL Register (Offset = 490h) [Reset = 00000000h]

SYSTIMC2SEL is shown in Table 4-51.

Return to the Summary Table.

Output Selection for SYSTIMC2

Table 4-51. SYSTIMC2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	32h	Read only selection value 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0

4.6.41 SYSTIMC3SEL Register (Offset = 494h) [Reset = 00000000h]

SYSTIMC3SEL is shown in Table 4-52.

Return to the Summary Table.

Output Selection for SYSTIMC3

Table 4-52. SYSTIMC3SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	33h	Read only selection value 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1

4.6.42 SYSTIMC4SEL Register (Offset = 498h) [Reset = 00000000h]

SYSTIMC4SEL is shown in Table 4-53.

Return to the Summary Table.

Output Selection for SYSTIMC4

Table 4-53. SYSTIMC4SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	34h	Read only selection value 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2

4.6.43 SYSTIMC5SEL Register (Offset = 49Ch) [Reset = 00000000h]

SYSTIMC5SEL is shown in Table 4-54.

Return to the Summary Table.

Output Selection for SYSTIMC5

Table 4-54. SYSTIMC5SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-54. SYSTIMC5SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-54. SYSTIMC5SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.44 ADCTRGSEL Register (Offset = 4A0h) [Reset = 00000000h]

ADCTRGSEL is shown in Table 4-55.

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Output Selection for ADCTRG

Table 4-55. ADCTRGSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-55. ADCTRGSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-55. ADCTRGSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.45 LGPTSYNCSEL Register (Offset = 4A4h) [Reset = 00000000h]

LGPTSYNCSEL is shown in Table 4-56.

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Output Selection for LGPTSYNC

Table 4-56. LGPTSYNCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-56. LGPTSYNCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-56. LGPTSYNCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.46 LGPT0IN0SEL Register (Offset = 4A8h) [Reset = 00000000h]

LGPT0IN0SEL is shown in Table 4-57.

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Output Selection for LGPT0IN0

Table 4-57. LGPT0IN0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-57. LGPT0IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-57. LGPT0IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.47 LGPT0IN1SEL Register (Offset = 4ACh) [Reset = 00000000h]

LGPT0IN1SEL is shown in Table 4-58.

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Output Selection for LGPT0IN1

Table 4-58. LGPT0IN1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-58. LGPT0IN1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.48 LGPT0IN2SEL Register (Offset = 4B0h) [Reset = 00000000h]

LGPT0IN2SEL is shown in Table 4-59.

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Output Selection for LGPT0IN2

Table 4-59. LGPT0IN2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-59. LGPT0IN2SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.49 LGPT0TENSEL Register (Offset = 4B4h) [Reset = 00000000h]

LGPT0TENSEL is shown in Table 4-60.

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Output Selection for LGPT0TEN

Table 4-60. LGPT0TENSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-60. LGPT0TENSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.50 LGPT1IN0SEL Register (Offset = 4B8h) [Reset = 00000000h]

LGPT1IN0SEL is shown in Table 4-61.

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Output Selection for LGPT1IN0

Table 4-61. LGPT1IN0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-61. LGPT1IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-61. LGPT1IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.51 LGPT1IN1SEL Register (Offset = 4BCh) [Reset = 00000000h]

LGPT1IN1SEL is shown in Table 4-62.

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Output Selection for LGPT1IN1

Table 4-62. LGPT1IN1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-62. LGPT1IN1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.52 LGPT1IN2SEL Register (Offset = 4C0h) [Reset = 00000000h]

LGPT1IN2SEL is shown in Table 4-63.

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Output Selection for LGPT1IN2

Table 4-63. LGPT1IN2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-63. LGPT1IN2SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.53 LGPT1TENSEL Register (Offset = 4C4h) [Reset = 00000000h]

LGPT1TENSEL is shown in Table 4-64.

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Output Selection for LGPT1TEN

Table 4-64. LGPT1TENSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-64. LGPT1TENSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.54 LGPT2IN0SEL Register (Offset = 4C8h) [Reset = 00000000h]

LGPT2IN0SEL is shown in Table 4-65.

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Output Selection for LGPT2IN0

Table 4-65. LGPT2IN0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-65. LGPT2IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-65. LGPT2IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.55 LGPT2IN1SEL Register (Offset = 4CCh) [Reset = 00000000h]

LGPT2IN1SEL is shown in Table 4-66.

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Output Selection for LGPT2IN1

Table 4-66. LGPT2IN1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-66. LGPT2IN1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.56 LGPT2IN2SEL Register (Offset = 4D0h) [Reset = 00000000h]

LGPT2IN2SEL is shown in Table 4-67.

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Output Selection for LGPT2IN2

Table 4-67. LGPT2IN2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-67. LGPT2IN2SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.57 LGPT2TENSEL Register (Offset = 4D4h) [Reset = 00000000h]

LGPT2TENSEL is shown in Table 4-68.

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Output Selection for LGPT2TEN

Table 4-68. LGPT2TENSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-68. LGPT2TENSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.58 LGPT3IN0SEL Register (Offset = 4D8h) [Reset = 00000000h]

LGPT3IN0SEL is shown in Table 4-69.

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Output Selection for LGPT3IN0

Table 4-69. LGPT3IN0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-69. LGPT3IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-69. LGPT3IN0SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.59 LGPT3IN1SEL Register (Offset = 4DCh) [Reset = 00000000h]

LGPT3IN1SEL is shown in Table 4-70.

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Output Selection for LGPT3IN1

Table 4-70. LGPT3IN1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-70. LGPT3IN1SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.60 LGPT3IN2SEL Register (Offset = 4E0h) [Reset = 00000000h]

LGPT3IN2SEL is shown in Table 4-71.

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Output Selection for LGPT3IN2

Table 4-71. LGPT3IN2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-71. LGPT3IN2SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.61 LGPT3TENSEL Register (Offset = 4E4h) [Reset = 00000000h]

LGPT3TENSEL is shown in Table 4-72.

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Output Selection for LGPT3TEN

Table 4-72. LGPT3TENSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-72. LGPT3TENSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting 2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.62 LRFDIN0SEL Register (Offset = 4E8h) [Reset = 00000000h]

LRFDIN0SEL is shown in Table 4-73.

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Output Selection for LRFDIN0

Table 4-73. LRFDIN0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	25h	Read only selection value 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2

4.6.63 LRFDIN1SEL Register (Offset = 4ECh) [Reset = 00000000h]

LRFDIN1SEL is shown in Table 4-74.

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Output Selection for LRFDIN1

Table 4-74. LRFDIN1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	26h	Read only selection value 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3

4.6.64 LRFDIN2SEL Register (Offset = 4F0h) [Reset = 00000000h]

LRFDIN2SEL is shown in Table 4-75.

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Output Selection for LRFDIN2

Table 4-75. LRFDIN2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R	27h	Read only selection value 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4

4.6.65 I2SSTMPSEL Register (Offset = 4F4h) [Reset = 00000000h]

I2SSTMPSEL is shown in Table 4-76.

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Output Selection for I2SSTMP

Table 4-76. I2SSTMPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-76. I2SSTMPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-76. I2SSTMPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.66 DMACH0SEL Register (Offset = C00h) [Reset = 00000000h]

DMACH0SEL is shown in Table 4-77.

Return to the Summary Table.

Output Selection for DMA CH0

Table 4-77. DMACH0SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Selects spi0txtrg as channel source Dh = Selects uart1rxtrg as channel source

4.6.67 DMACH1SEL Register (Offset = C04h) [Reset = 00000000h]

DMACH1SEL is shown in Table 4-78.

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Output Selection for DMA CH1

Table 4-78. DMACH1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 1h = Selects spi0rxtrg as channel source Ch = Selects uart1txtrg as channel source

4.6.68 DMACH2SEL Register (Offset = C08h) [Reset = 00000000h]

DMACH2SEL is shown in Table 4-79.

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Output Selection for DMA CH2

Table 4-79. DMACH2SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 2h = Selects lrfdtrg as channel source 6h = Selects uart0txtrg as channel source

4.6.69 DMACH3SEL Register (Offset = C0Ch) [Reset = 00000000h]

DMACH3SEL is shown in Table 4-80.

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Output Selection for DMA CH3

Table 4-80. DMACH3SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 5h = Selects adc0trg as channel source 7h = Selects uart0rxtrg as channel source

4.6.70 DMACH4SEL Register (Offset = C10h) [Reset = 00000000h]

DMACH4SEL is shown in Table 4-81.

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Output Selection for DMA CH4

Table 4-81. DMACH4SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 2h = Selects lrfdtrg as channel source 3h = Selects laestrga as channel source

4.6.71 DMACH5SEL Register (Offset = C14h) [Reset = 00000000h]

DMACH5SEL is shown in Table 4-82.

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Output Selection for DMA CH5

Table 4-82. DMACH5SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 4h = Selects laestrgb as channel source 5h = Selects adc0trg as channel source

4.6.72 DMACH6SEL Register (Offset = C18h) [Reset = 00000000h]

DMACH6SEL is shown in Table 4-83.

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Output Selection for DMA CH6

Table 4-83. DMACH6SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 8h = Selects cantrga as channel source Ah = Selects spi1txtrg as channel source

4.6.73 DMACH7SEL Register (Offset = C1Ch) [Reset = 00000000h]

DMACH7SEL is shown in Table 4-84.

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Output Selection for DMA CH7

Table 4-84. DMACH7SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
3-0	IPID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 9h = Selects cantrgb as channel source Bh = Selects spi1rxtrg as channel source

4.6.74 DMACH10SEL Register (Offset = C20h) [Reset = 00000000h]

DMACH10SEL is shown in Table 4-85.

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Output Selection for DMA CH10

Table 4-85. DMACH10SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
16	EDGDETDIS	R/W	0h	Edge detect disable.;0: Enabled.;1: Disabled
15-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-85. DMACH10SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-85. DMACH10SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.75 DMACH11SEL Register (Offset = C24h) [Reset = 00000000h]

DMACH11SEL is shown in Table 4-86.

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Output Selection for DMA CH11

Table 4-86. DMACH11SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
16	EDGDETDIS	R/W	0h	Edge detect disable.;0: Enabled.;1: Disabled
15-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-86. DMACH11SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-86. DMACH11SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.76 DMACH8SEL Register (Offset = C28h) [Reset = 00000000h]

DMACH8SEL is shown in Table 4-87.

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Output Selection for DMA CH8

Table 4-87. DMACH8SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
16	EDGDETDIS	R/W	0h	Edge detect disable.;0: Enabled.;1: Disabled
15-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-87. DMACH8SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-87. DMACH8SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.6.77 DMACH9SEL Register (Offset = C2Ch) [Reset = 00000000h]

DMACH9SEL is shown in Table 4-88.

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Output Selection for DMA CH9

Table 4-88. DMACH9SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
16	EDGDETDIS	R/W	0h	Edge detect disable.;0: Enabled.;1: Disabled
15-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Table 4-88. DMACH9SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG 10h = SYSTIM combined interrupt, interrupt flags are found here SYSTIM:MIS 11h = GPIO combined wake up interrupt, interrupt flags can be found here GPIO:MIS 12h = GPIO generic published event 0, controlled by GPIO:EVTCFG 13h = NoWrapper Flash interrupt indicating that the flash operation has completed, interrupt flags can be found here FLASH:MIS 14h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS0 15h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS1 16h = LRFD combined event, interrupt flags can be found here LRFDDBELL:MIS2 17h = SPI0 combined interrupt request, interrupt flags can be found here SPI0:MIS 18h = ADC combined interrupt request, interrupt flags can be found here ADC:MIS0 19h = ADC general published event, interrupt flags can be found here ADC:MIS1 1Ah = LGPT0 combined interrupt, interrupt flags are found here LGPT0:MIS 1Bh = LGPT1 combined interrupt, interrupt flags are found here LGPT1:MIS 1Ch = DMA combined done interrupt, corresponding flags can be found here DMA:REQDONE 1Dh = DMA bus error, corresponds to DMA:ERROR.STATUS 1Eh = AES accelerator combined interrupt request, interrupt flags can be found here AES:MIS 1Fh = UART0 combined interrupt, interrupt flags are found here UART0:MIS 20h = Interrupt event from I2C0, interrupt flags can be found here I2C0:MIS 21h = SYSTIM heartbeat, can be set by SYSTIM:TIMEBIT 22h = SYSTIM interrupt driven by synchroinizing LFTICK signal to SVT clock 23h = SYSTIM Channel 0 event, event flag is SYSTIM:MIS.EVT0 24h = SYSTIM Channel 1 event, event flag is SYSTIM:MIS.EVT1 25h = SYSTIM Channel 2 event, event flag is SYSTIM:MIS.EVT2 26h = SYSTIM Channel 3 event, event flag is SYSTIM:MIS.EVT3 27h = SYSTIM Channel 4 event, event flag is SYSTIM:MIS.EVT4 28h = LGPT0 compare/capture output event 0, controlled by LGPT0:C0CFG setting 29h = LGPT0 compare/capture output event 1, controlled by LGPT0:C1CFG setting 2Ah = LGPT0 compare/capture output event 2, controlled by LGPT0:C2CFG setting 2Bh = LGPT0 DMA request event, controlled by LGPT0:DMA setting 2Ch = LGPT0 ADC trigger event, controlled by LGPT0:ADCTRG setting 2Dh = LGPT1 compare/capture output event 0, controlled by LGPT1:C0CFG setting 2Eh = LGPT1 compare/capture output event 1, controlled by LGPT1:C1CFG setting

Table 4-88. DMACH9SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Fh = LGPT1 compare/capture output event 2, controlled by LGPT1:C2CFG setting 30h = LGPT1 DMA request event, controlled by LGPT1:DMA setting 31h = LGPT1 ADC trigger event, controlled by LGPT1:ADCTRG setting 32h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC0 33h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC1 34h = LRFD interrupt to SYSTIM, controlled by LRFDDBELL:SYSTIMOEV.SRC2 35h = UART1 combined interrupt, interrupt flags are found here UART1:MIS 36h = LGPT2 compare/capture output event 0, controlled by LGPT2:C0CFG setting 37h = LGPT2 compare/capture output event 1, controlled by LGPT2:C1CFG setting 38h = LGPT0 compare/capture output event 2, controlled by LGPT2:C2CFG setting 39h = LGPT2 combined interrupt, interrupt flags are found here LGPT2:MIS 3Ah = LGPT2 DMA request event, controlled by LGPT2:DMA setting 3Bh = LGPT2 ADC trigger event, controlled by LGPT2:ADCTRG setting 3Ch = LGPT3 compare/capture output event 0, controlled by LGPT3:C0CFG setting 3Dh = LGPT3 compare/capture output event 1, controlled by LGPT3:C1CFG setting 3Eh = LGPT3 compare/capture output event 2, controlled by LGPT3:C2CFG setting 3Fh = LGPT3 combined interrupt, interrupt flags are found here LGPT3:MIS 40h = LGPT3 DMA request event, controlled by LGPT3:DMA setting 41h = LGPT3 ADC trigger event, controlled by LGPT3:ADCTRG setting 42h = I2S interrupt event, controlled by I2S:IRQMASK 43h = MCAN interrupt event, interrupt flags can be found here MCAN:MIS0 44h = MCAN general event, interrupt flags can be found here MCAN:MIS1 45h = SPI1 combined interrupt request, interrupt flags can be found here SPI1:MIS 46h = APU IRQ 4Bh = GPIO generic published event 1, controlled by GPIO:EVTCFG 4Ch = SYSTIM Channel 5 event

4.7 EVTULL Registers

Table 4-89 lists the memory-mapped registers for the EVTULL registers. All register offset addresses not listed in Table 4-89 should be considered as reserved locations and the register contents should not be modified.

Table 4-89. EVTULL Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.This register provides IP module ID, revision information, instance index and standard MMR registers offset.	Section 4.7.1
4h	DESCEX	Extended Description Register. This register provides configuration details of the IP to software drivers and end users.	Section 4.7.2
64h	DTB	Digital test bus control register. This register can be used to bring out IP internal signals to the pads for observation. 16 signals can be observed per select value.	Section 4.7.3
404h	RTCCPTSEL	Output Selection for RTCCPT Register.	Section 4.7.4
800h	WKUPMASK	WAKEUP Mask Register.	Section 4.7.5

Complex bit access types are encoded to fit into small table cells. Table 4-90 shows the codes that are used for access types in this section.

Table 4-90. EVTULL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

4.7.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 4-91.

Return to the Summary Table.

Description Register.This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 4-91. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	3045h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

4.7.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 4-92.

Return to the Summary Table.

Extended Description Register. This register provides configuration details of the IP to software drivers and end users.

Table 4-92. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	IDMA	R	0h	Number of DMA input channels
21-17	NDMA	R	0h	Number of DMA output channels
16	PD	R	1h	Power Domain.;0 : SVT; 1 : ULL
15-8	NSUB	R	1h	Number of Subscribers
7-0	NPUB	R	6h	Number of Publishers

4.7.3 DTB Register (Offset = 64h) [Reset = 00000000h]

DTB is shown in Table 4-93.

Return to the Summary Table.

Digital test bus control register. This register can be used to bring out IP internal signals to the pads for observation. 16 signals can be observed per select value.

Table 4-93. DTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
0	SEL	R/W	0h	Digital test bus selection mux control.;Non-zero select values output a 16 bit selected group of signals per value.

4.7.4 RTCCPTSEL Register (Offset = 404h) [Reset = 00000000h]

RTCCPTSEL is shown in Table 4-94.

Return to the Summary Table.

Output Selection for RTCCPT Register.

Table 4-94. RTCCPTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
6-0	PUBID	R/W	0h	Read/write selection value.;Writing any other value than values defined by a ENUM may result in undefined behavior. 0h = Always inactive 2h = PMU combined interrupt request for BATMON, interrupt flags can be found here PMUD:EVENT 3h = CKMD combined interrupt request, interrupt flags can be found here CKMD:MIS 4h = AON_RTC event, controlled by the RTC:IMASK setting 5h = DebugSS combined interrupt, interrupt flags can be found here DBGSS:MIS 6h = AON LPCMP interrupt, controlled by SYS0:LPCMPCFG 7h = IOC synchronous combined event, controlled by IOC:EVTCFG

4.7.5 WKUPMASK Register (Offset = 800h) [Reset = 00000000h]

WKUPMASK is shown in Table 4-95.

Return to the Summary Table.

WAKEUP Mask Register.

Table 4-95. WKUPMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior
7	AON_IOC_COMB	R/W	0h	Wake-up mask for AON_IOC_COMB. 0h = Wakeup disabled 1h = Wakeup enabled
6	AON_LPMCMP_IRQ	R/W	0h	Wake-up mask for AON_LPCMP_IRQ. 0h = Wakeup disabled 1h = Wakeup enabled
5	AON_DBG_COMB	R/W	0h	Wake-up mask for AON_DBG_COMB. 0h = Wakeup disabled 1h = Wakeup enabled
4	AON_RTC_COMB	R/W	0h	Wake-up mask for AON_RTC_COMB. 0h = Wakeup disabled 1h = Wakeup enabled
3	AON_CKM_COMB	R/W	0h	Wake-up mask for AON_CKM_COMB. 0h = Wakeup disabled 1h = Wakeup enabled
2	AON_PMU_COMB	R/W	0h	Wake-up mask for AON_PMU_COMB. 0h = Wakeup disabled 1h = Wakeup enabled
1-0	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior

Chapter 5

Debug Subsystem

This chapter discussions the features of the debug subsystem (DEBUGSS).

5.1 Introduction

The debug subsystem (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. Debugging of processor execution and the device state are supported. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

Key features provided by the debug subsystem include:

- Two-wire (SWDIO, SWCLK) debug interface, compatible with both TI and 3rd party debug probes
  - On-chip pull-up/pull-down resistors for SWDIO and SWCLK, respectively, enabled by default
  - Support for disabling SWD functions to use SWD pins as general purpose input/output pins
  - Capability of waking the device from SHUTDOWN mode upon valid SWD activity
- Debug of the processor
  - Run, halt, and step debug support
  - 4 hardware breakpoints (BPU)
- Software-configurable peripheral behavior during processor debug
  - Ability to free run select peripherals through debug halt
  - Ability to halt select peripherals on a debug halt
  - Ability to request reset and mode changes to the Power Management Control (PMCTL)
- Debug subsystem mailbox (DSSM) for passing data and control signals between the SWD interface and boot ROM (as well as application software)
- Support for various security features, including authenticated debugging

5.2 Block Diagram

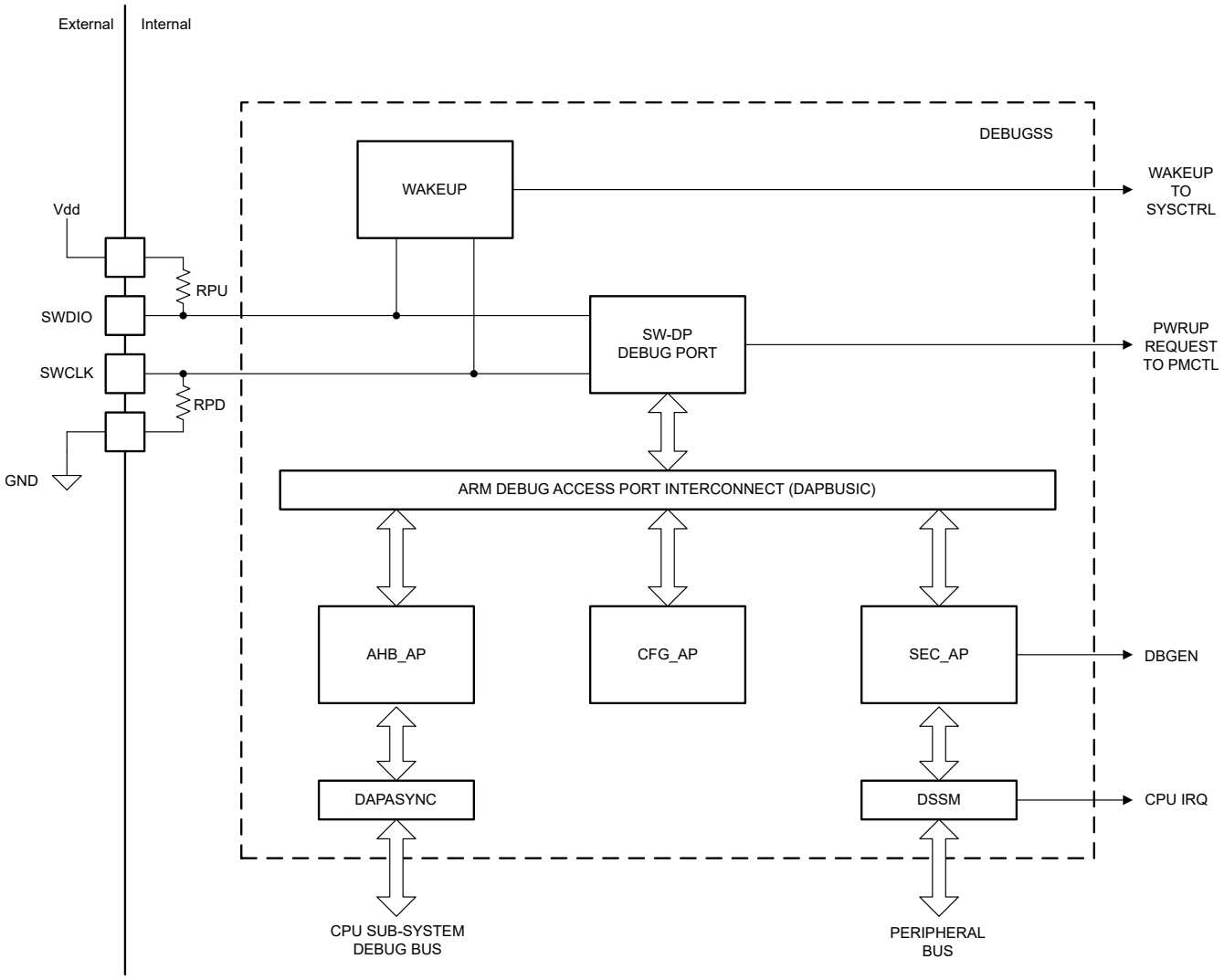

Figure 5-1. DEBUGSS Block Diagram

5.3 Overview

The SWD physical interface interacts with the Arm serial wire debug port (SW-DP) to gain access to the debug access port bus interconnect (DAPBUSIC) when the SW-DP is enabled. From TI, devices ship with the SW-DP enabled to allow SWD access to the device for development and production programming. The SW-DP can be configured to be permanently disabled through the boot configuration policy, see "debugCfg" in Section 10.3. The DAPBUSIC enables a debug probe to access one or more debug access ports. For a debug probe to be able to communicate with an access port, the SW-DP debug port must not be disabled by the boot configuration policy, and the target access port must also not be disabled by the boot configuration policy. The available access ports are given in Section 5.3.2.

5.3.1 Physical Interface

Debug connections to the device are supported through an Arm® serial wire debug (SWD) compliant interface. The SWD interface requires two connections:

- A bidirectional data line (SWDIO) used to send data to, and receive data from the device
- A unidirectional clock line (SWCLK) driven by the debug probe connecting to the device

The SWD interface uses the standard logic levels of the device for SWD communication. See the device-specific datasheet for input and output logic levels for a given supply voltage (VDDS). A SWCLK frequency of up to 10 MHz is supported by the DEBUGSS.

During SWD operation, the SWDIO line can be driven high or driven low by either the target device or the debug probe. As either device can drive the line, when ownership of the shared SWDIO line is switched between the device and the debug probe, undriven time slots are inserted as a part of the SWD protocol. The primary purpose of the pull-up resistor on the SWDIO line, and the pull-down resistor on the SWCLK line, is to place the SWD pins into a known state when no debug probe is attached. A minimum resistance of 100 kΩ is recommended by Arm®. The internal pull-up/pull-down resistors fulfill this requirement and external resistors are not required for correct operation of the SWD interface.

After a power-on reset (POR), the target device configures the SWD pins in SWD mode with an internal pull-up resistor enabled on the SWDIO line and an internal pull-down resistor enabled on the SWCLK line. If the device configuration has not permanently disabled all SWD access, then the SWD interface is enabled during the boot process and a debug probe can be connected to the DEBUGSS.

In the event that a device was configured by software to enter SHUTDOWN mode, and a debug probe is then connected to the SWD pins with SWCLK active, wake-up logic triggers an exit from SHUTDOWN mode. A debug connection can then be established to the DEBUGSS after the reset sequence completes.

Upon physical connection of a debug probe, a configuration sequence must be sent from the debug probe to the target device to initiate a valid SWD connection with the SW-DP. An invalid sequence doesn't wake the device from SHUTDOWN mode. Once the sequence is transmitted and the SWD connection is established, communication with enabled debug access points is possible and the bootcode is alerted through assertion of DBGSS.DBGCTL[1] SWDSEL bit which is continuously monitored in bootcode. The debug probe must be disconnected by sending disconnection sequence from the debug probe to target device.

Bootcode can disable the SWD interface in DEBUGSS, freeing the IOs to be used for general purpose IO functionality. Once Bootcode disables SWD functionality, SWD functionality cannot be re-enabled other than by triggering a POR. A POR automatically re-enables the SWD functionality and puts the SWD pins into SWD mode with pull-up/pull-down resistors enabled. To regain debug access to a device, hold the device in a reset state with the RSTN pin during a POR. This prevents the bootcode from starting and lets the debug probe gain access to the device.

5.3.2 Debug Access Ports

The debug access ports in the DEBUGSS are given in Table 5-1.

Table 5-1. DEBUGSS Access Port Listing

APSEL	AP	Port Description	Purpose
0x0	AHB-AP	CPUSS debug access port	Debug of the processor and peripherals
0x1	CFG-AP	Configuration access port	Access device type information
0x2	SEC-AP	Security access port	Access the debug mailbox

The AHB-AP provides the complete device debug functionality (processor debug, peripheral and memory bus access and processor state). See Section 5.4 for more information.

The CFG-AP provides device information to the debug probe so that the debug probe can identify device characteristics, including the device part number and the device revision.

The SEC-AP provides access to the mailbox for communicating with software running on the device through SWD. See Section 5.7 for more information.

5.4 Debug Features

The DEBUGSS supports processor debug and peripheral debug

5.4.1 Processor Debug

The Arm® Cortex® -M33 processor supports a wide range of features to simplify debugging of application software during development. Key features supported by CC27XX MCUs include:

- Ability to halt the processor through an assertion of a halt signal, a configured debug event (such as a hard fault entry or reset), or a BKPT instruction (for software breakpoints)
- Ability to step through instructions (with or without peripheral interrupts enabled)
- Ability to run through instructions (with or without peripheral interrupts enabled)
- Ability to read and write CPU registers when halted
- Ability to read exception information through the system control space (SCS)
- Support for 4 hardware breakpoints
- Support for accessing the device memory map

5.4.2 Breakpoint Unit (BPU)

The breakpoint unit (BPU) provides 4 comparators which can be used to generate a debug event when the address of an instruction fetch matches the address programmed into the one of the BPU comparators.

The BPU comparators match instruction fetches from the code memory region, meaning the comparators only operate on instruction read accesses. The comparators do not match data read or data write accesses.

Address matching is possible for half-word (16-bit) instructions and word (32-bit) instructions fetched from the CODE region (0x00000000 to 0x1FFFFFFF).

Hardware breakpoints are not available when debugging code in SRAM. When debugging code in SRAM, software breakpoints must be inserted by the debug probe.

5.4.3 Peripheral Debug

In addition to processor debug, the DEBUGSS can be used to access the device memory map from the perspective of the processor. Thus, a connected debug probe can be used to read and write memory-mapped peripheral registers, the system SRAM, and the flash memory.

Certain peripherals support advanced debug configuration options. These options are configured by application software (or optionally, the debug probe) by setting/clearing various debug control bits in the memory map of a given peripheral. In general, the debug behavior of a particular peripheral is specified in the EMU register of each peripheral. Many peripherals offer the option of halting the functional clock to the peripheral when the processor is halted for debug, thus pausing the peripheral together with the processor (default configuration), or letting the peripheral run even when the processor is halted for debug.

For example, the SYSTIM peripheral supports the RUN/STOP bits in the EMU register. Setting the RUN bit in EMU for a SYSTIM causes the SYSTIM to run even if the processor is halted for debug.

5.5 Behavior in Low Power Modes

The DEBUGSS supports maintaining a debug connection through SWD in all operating modes except SHUTDOWN.

Access to device memory and peripherals is possible in ACTIVE mode and IDLE mode, in which a debug probe can be actively connected to the AHB-AP access port to interface with the processor. In STANDBY mode, a debug connection can be established and/or maintained with the DEBUGSS, but not with the CPU debug access port.

While a debug connection to the DEBUGSS is not possible while the device is in SHUTDOWN mode, a debug probe can cause the device to exit SHUTDOWN mode by attempting to communicate with the SWD pins. The device detects attempted SWD communication even when the device is in SHUTDOWN. If any activity is detected, a SHUTDOWN exit is initiated and after which a debug connection can be made to the DEBUGSS through SWD. An active debug connection prohibits SHUTDOWN entry and device can enter SHUTDOWN mode only after debug disconnection.

The DEBUGSS functionality by operating mode is given in Table 5-2.

Table 5-2. DEBUGSS Functionality by Operating Mode

Capability	ACTIVE	IDLE	STANDBY	SHUTDOWN
Processor debug	Y	Y	N	N
Memory map access	Y	Y	N	N
Debug status through SW-DP	Y	Y	Y	N
Debug state maintained	Y	Y	Y	N
Wake from SWD	-	-	-	Y

5.6 Restricting Debug Access

The debug subsystem supports several methods for restricting access to the device through the SWD interface. The debug access policy is determined by the user configuration specified in the CCFG flash region. See Section 10.3 for a detailed description of debug access control through the CCFG flash region.

There are 3 levels of access control, given in Table 5-3. By default, products shipped from TI arrive in a "debug enabled" state where the device is fully open. This state is not recommended for production. For production, TI recommends changing the debug configuration to 'require authentication' or 'disabled'.

Table 5-3. Debug Access Control

DEBUGSS Function	Debug Configuration		
	Debug Enabled (default)	Debug Enabled with Authentication	Debug Disabled
SW-DP (Debug Port)	EN	EN	DIS
CFG-AP	EN	EN	DIS
SEC-AP	EN	EN	DIS
AHB-AP (CPU Debug)	EN	EN w/ Authentication	DIS

When debug is enabled with public key based authentication, the debug access commands implementing a secure challenge response sequence must be provided to the DEBUGSS mailbox by the debug probe.

When debug is disabled, the SW-DP is disabled during the boot process. Any commands previously sent to the mailbox are ignored during boot. Following boot, any attempt to connect to the SW-DP is ignored.

Debug access can be permanently locked by configuring the CCFG flash region to disable debug access while also configuring the CCFG flash region as statically write protected (locked). Locking the CCFG configuration has the added security of preventing the ROM serial bootloader and application code from changing the debug security policy.

5.7 Mailbox (DSSM)

The debug subsystem mailbox (DSSM) enables a debug probe to pass messages to the target device through the SWD interface, and for the target device to return data to the debug probe.

The DSSM supports the following functions:

- Transmission of commands to the device during boot, including authenticating the debug probe for public key authenticated debug, mass erase, and factory reset operations
- Communicating with application software running on the target device when no other communication interface is present

32-bit word data buffers are provided for transmit data (debug probe to target device) and receive data (target device to debug probe). These data buffers are implemented as the 32-bit memory-mapped registers DBGSS.TXD and DBGSS.RXD. The DBGSS.TXCTL and DBGSS.RXCTL registers are provided for enabling flow control and indicating status of the mailbox.

Table 5-4. DBGSS DSSM Register Functions

DBGSS Register	Description	Debug Probe	Target Device	Actions
TXD	Data buffer	RW	R	DBGSS.TXCTL[0] TXDSTA bit is set on write by the debug probe, and cleared on a read by the target device. DBGSS.RIS[0] TXIFG bit is also set on a write by the debug probe.
TXCTL	Flow control and status	RW	R	None. More information on SACI Communication Protocol
RXD	Data buffer	R	RW	DBGSS.RXCTL[0] RXDSTA bit is set on write by the target device, and cleared on a read by the debug probe. DBGSS.RIS[1] RXIFG bit is also set on a write by the target device
RXCTL	Flow control and status	R	RW	None. More information on SACI Communication Protocol

The DBGSS.TXCTL[0] TXD_FULL bit is set in the TXCTL register when a debug probe writes data to the DBGSS.TXD buffer register. The TXD_FULL flag remains set until the target device reads DBGSS.TXD or a POR occurs. The DBGSS.RXCTL[0] RXD_FULL bit is set when the target device writes data to the DBGSS.RXD buffer register. The RXD_FULL flag remains set until the debug probe or target device reads the data from DBGSS.RXD.

Software running on the target device cannot write to TXD, and software cannot clear the TXD_FULL flag other than by reading DGBSS.TXD. The DBGSS.TXCTL[7:1] bit field contains flag bits which can be set or cleared by the debug probe to implement a protocol if desired. Only the debug probe can write to the TXD_FULL_FLAGS field in TXCTL.

In a similar way, only the target device software can write to DBGSS.RXD and DBGSS.RXCTL. The debug probe cannot write to RXD and can only clear the DEBUGSS.RXCTL[0] RXD_FULL bit by reading DBGSS.RXD. DBGSS.RXCTL[7:1] FLAGS bit field contains flag bits. Software on the target device can set or clear bits in the DBGSS.RXCTL[7:1] FLAGS field to implement a protocol if desired. These flags can be read by the debug probe but can not be modified by the debug probe.

DBGSS.TXDPEEK and DBGSS.RXDPEEK registers can be read by the device to read DBGSS.TXD and DBGSS.RXD registers without affecting the FULL/EMPTY flag.

For a complete listing of commands which are supported by the boot configuration routine during device startup configuration, see Chapter 9.

5.8 Mailbox Events

The DSSM contains one event publisher and no event subscribers. One event publisher (INT_EVENT0) manages DSSM interrupt requests (IRQs) to the CPU subsystem via the AON event fabric.

The DSSM events are summarized in Table 5-5.

Table 5-5. DSSM Events

Event	Type	Source	Destination	Route	Configuration	Functionality
CPU Interrupt Event	Publisher	DEBUGSS	CPU Subsystem	Dynamic route	AON_DBG_COMB	DBGIRQ from DEBUGSS to CPU is a configurable IRQ

5.8.1 CPU Interrupt Event (AON_DBG_COMB)

The DSSM provides 4 interrupt sources which can be configured to source a CPU interrupt event. The CPU interrupt events from the DSSM are given in Table 5-6.

Table 5-6. DSSM CPU Interrupt Event Conditions (INT_EVENT0)

Name	Description
TXIFG	Indicates that the TX_DATA buffer in the DSSM has received data.
RXIFG	Indicates that the data in RX_DATA buffer in the DSSM was read.
PWRUPIFG	Indicates that the DEBUGSS was started due to a debug probe attaching to the device.
PWRDWNIFG	Indicates that the DEBUGSS was stopped due to a debug probe disconnecting from the device.

See Chapter 4 for guidance on configuring the DEBUGGSS event as a CPU interrupt.

5.9 Software Considerations

Enable the debug connection before connecting a debug probe by setting the DBGSS.DBGBCTRL[5] SWDCEN register bit and disable after the debug session is completed by clearing the bit.

The debug software override feature is a fail-safe approach for enabling a debug connection and is enabled by writing the DBGSS.DBGBCTRL[0] SWDOVR register bit. When this bit is set, the device does not wake up from shutdown due to a debug connection. This feature is used only for internal debugging purposes, if there are issues seen in establishing debug connection in standby/active modes.

5.10 DBGSS Registers

Table 5-7 lists the memory-mapped registers for the DBGSS registers. All register offset addresses not listed in Table 5-7 should be considered as reserved locations and the register contents should not be modified.

Table 5-7. DBGSS Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 5.10.1
44h	IMASK	Interrupt mask	Section 5.10.2
4Ch	RIS	Raw interrupt status	Section 5.10.3
54h	MIS	Masked interrupt status	Section 5.10.4
5Ch	ISET	Interrupt set	Section 5.10.5
64h	ICLR	Interrupt clear	Section 5.10.6
6Ch	IMSET	Set Interupt Mask in IMASK	Section 5.10.7
74h	IMCLR	Clear Interupt Mask in IMASK	Section 5.10.8
100h	TXD	Transmit data register	Section 5.10.9
104h	TXCTL	Transmit control register	Section 5.10.10
108h	RXD	Receive data register	Section 5.10.11
10Ch	RXCTL	Receive control register	Section 5.10.12
110h	TXDPEEK	Transmit Data Peek Register	Section 5.10.13
114h	RXDPEEK	Receive Data Peek Register	Section 5.10.14
200h	SPECIAL_AUTH	Special enable authorization register	Section 5.10.15
204h	SPECIAL_AUTH_SET	Special enable authorization set register	Section 5.10.16
208h	SPECIAL_AUTH_CLR	Special enable authorization clear register	Section 5.10.17
210h	APP_AUTH	Application authorization register	Section 5.10.18
214h	APP_AUTH_SET	Application authorization set register	Section 5.10.19
218h	APP_AUTH_CLR	Application authorization clear register	Section 5.10.20
21Ch	DBGCTL	Debug control register	Section 5.10.21

Complex bit access types are encoded to fit into small table cells. Table 5-8 shows the codes that are used for access types in this section.

Table 5-8. DBGSS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

5.10.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 5-9.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 5-9. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	B24Dh	Module identifier used to uniquely identify this IP. 0h = Minimum value FFFFh = Maximum possible value
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address);0: STDIP MMRs do not exist;0x1-0xF: These MMRs begin at offset 64*STDIPOFF from IP base address 0h = Minimum Value Fh = Maximum possible value
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15). 0h = Minimum Value Fh = Maximum possible value
7-4	MAJREV	R	1h	Major revision of IP (0-15). 0h = Minimum Value Fh = Maximum possible value
3-0	MINREV	R	0h	Minor revision of IP (0-15). 0h = Minimum Value Fh = Maximum possible value

5.10.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 5-10.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 5-10. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	R/W	0h	PWRDWNIFG interrupt mask 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set
2	PWRUPIFG	R/W	0h	PWRUPIFG interrupt mask 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set
1	RXIFG	R/W	0h	RXIFG interrupt mask 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set
0	TXIFG	R/W	0h	TXIFG interrupt mask 0h = Disable Interrupt Mask 1h = Enable Interrupt Mask

5.10.3 RIS Register (Offset = 4Ch) [Reset = 00000000h]

RIS is shown in Table 5-11.

Return to the Summary Table.

Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 5-11. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	R	0h	Raw interrupt status for PWRDWNIFG 0h = PWRDWNIFG did not occur 1h = PWRDWNIFG occurred
2	PWRUPIFG	R	0h	Raw interrupt status for PWRUPIFG 0h = PWRUPIFG did not occur 1h = PWRUPIFG occurred
1	RXIFG	R	0h	Raw interrupt status for RXIFG 0h = RXIFG did not occur 1h = RXIFG occurred
0	TXIFG	R	0h	Raw interrupt status for TXIFG 0h = TXIFG did not occur 1h = TXIFG occurred

5.10.4 MIS Register (Offset = 54h) [Reset = 00000000h]

MIS is shown in Table 5-12.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of IMASK and RIS registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 5-12. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	R	0h	Masked interrupt status for PWRDWNIFG 0h = PWRDWNIFG did not request an interrupt service routine 1h = PWRDWNIFG requests an interrupt service routine
2	PWRUPIFG	R	0h	Masked interrupt status for PWRUPIFG 0h = PWRUPIFG did not request an interrupt service routine 1h = PWRUPIFG requests an interrupt service routine
1	RXIFG	R	0h	Masked interrupt status for RXIFG 0h = RXIFG did not request an interrupt service routine 1h = RXIFG requests an interrupt service routine
0	TXIFG	R	0h	Masked interrupt status for TXIFG 0h = TXIFG did not request an interrupt service routine 1h = TXIFG requests an interrupt service routine

5.10.5 ISET Register (Offset = 5Ch) [Reset = 00000000h]

ISET is shown in Table 5-13.

Return to the Summary Table.

Interrupt set register. This register can be used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 5-13. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	W	0h	Sets PWRDWNIFG in RIS register 0h = Writing a 0 has no effect 1h = Set interrupt
2	PWRUPIFG	W	0h	Sets PWRUPIFG in RIS register 0h = Writing a 0 has no effect 1h = Set interrupt
1	RXIFG	W	0h	Sets RXIFG in RIS register 0h = Writing a 0 has no effect 1h = Set interrupt
0	TXIFG	W	0h	Sets TXIFG in RIS register 0h = Writing a 0 has no effect 1h = Set interrupt

5.10.6 ICLR Register (Offset = 64h) [Reset = 00000000h]

ICLR is shown in Table 5-14.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 5-14. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	W	0h	Clears PWRDWNIFG interrupt 0h = Writing a 0 has no effect 1h = Clear interrupt
2	PWRUPIFG	W	0h	Clears PWRUPIFG interrupt 0h = Writing a 0 has no effect 1h = Clear interrupt
1	RXIFG	W	0h	Clears RXIFG interrupt 0h = Writing a 0 has no effect 1h = Clear interrupt
0	TXIFG	W	0h	Clears TXIFG interrupt 0h = Writing a 0 has no effect 1h = Clear interrupt

5.10.7 IMSET Register (Offset = 6Ch) [Reset = 00000000h]

IMSET is shown in Table 5-15.

Return to the Summary Table.

Interrupt mask set register. Writing a 1 to a bit in this register will set the corresponding IMASK bit.;

Table 5-15. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	W	0h	Set PWRDWNIFG interrupt mask 0h = Writing a 0 has no effect 1h = Set interrupt mask
2	PWRUPIFG	W	0h	Set PWRUPIFG interrupt mask 0h = Writing a 0 has no effect 1h = Set interrupt mask
1	RXIFG	W	0h	Set RXIFG interrupt mask 0h = Writing a 0 has no effect 1h = Set interrupt mask
0	TXIFG	W	0h	Set TXIFG interrupt mask 0h = Writing a 0 has no effect 1h = Set interrupt mask

5.10.8 IMCLR Register (Offset = 74h) [Reset = 00000000h]

IMCLR is shown in Table 5-16.

Return to the Summary Table.

Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 5-16. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWRDWNIFG	W	0h	Clears PWRDWNIFG interrupt mask 0h = Writing a 0 has no effect 1h = IMASK bit corresponding to PWRDWNIFG is cleared
2	PWRUPIFG	W	0h	Clears PWRUPIFG interrupt mask 0h = Writing a 0 has no effect 1h = IMASK bit corresponding to PWRUPIFG is cleared
1	RXIFG	W	0h	Clears RXIFG interrupt mask 0h = Writing a 0 has no effect 1h = IMASK bit corresponding to RXIFG is cleared
0	TXIFG	W	0h	Clears TXIFG interrupt mask 0h = Writing a 0 has no effect 1h = IMASK bit corresponding to TXIFG is cleared

5.10.9 TXD Register (Offset = 100h) [Reset = 00000000h]

TXD is shown in Table 5-17.

Return to the Summary Table.

Transmit data register. This register is used for sending SACI (SECAP command interface) data from the host to the device.;The host (SWD interface) can write this register. This updates the value of TXD, and sets TXCTL.TXDSTA = FULL;The host should only write TXD while TXCTL.TXDSTA = EMPTY.;If the host incorrectly writes TXD while TXCTL.TXDSTA = FULL, this will just update the value of TXD.;The host (SWD interface) can read the TXD register. This does not affect TXCTL.TXDSTA.;The device (boot code) can only read the TXD register. This sets TXCTL.TXDSTA = EMPTY.;The device should only read TXD while TXCTL.TXDSTA = FULL.;If the device incorrectly reads TXD while TXCTL.TXDSTA = EMPTY, this will just return the value of TXD.;If the host writes TXD on the same clock cycle as the device reads TXD:;The device reads the old TXD value.;TXD is updated with the new value, and TXCTL.TXDSTA is set to FULL.

Table 5-17. TXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	SACI command/parameter word. Valid value when TXCTL.TXDSTA=1. TXCTL.TXDSTA gets automatically cleared upon read.

5.10.10 TXCTL Register (Offset = 104h) [Reset = 00000000h]

TXCTL is shown in Table 5-18.

Return to the Summary Table.

Transmit control register. This register contains status of the TXD register (full/empty), and also software defined flags that are used by the SACI protocol.;The host (SWD interface) can write the FLAGS field of the TXCTL register.;The host (SWD interface) can read the TXCTL register.;The device (boot code) can only read the TXCTL register.

Table 5-18. TXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-1	FLAGS	R	0h	Software defined flags that are used by the SACI protocol (host to device).
0	TXDSTA	R	0h	Indicates whether the host has written a word to the TXD register, which can be read by the device:;TXDSTA is automatically set upon write to TXD register in SECAP and automatically gets cleared upon read from TXD 0h = The TXD register does not contain a new SACI parameter word from the host, and should not be read by the device. 1h = The TXD register contains a new SACI parameter word from the host, which can be read by the device.

5.10.11 RXD Register (Offset = 108h) [Reset = 00000000h]

RXD is shown in Table 5-19.

Return to the Summary Table.

Receive data register. This register is used to send SACI command response data from the device to the host.;The device (boot code) can write the RXD register. This updates the value of RXD, and sets RXCTL.RXDSTA = FULL.;The device should only write RXD while RXCTL.RXDSTA = EMPTY.;If the device incorrectly writes RXD while RXCTL.RXDSTA = FULL, this will just update the value of RXD.;The device (boot code) can read the RXD register in order to flush it. This sets RXCTL.RXDSTA = EMPTY.;The host (SWD interface) can only read the RXD register. This sets RXCTL.RXDSTA = EMPTY.;The host should only read RXD while RXCTL.RXDSTA = FULL.;If the host incorrectly reads RXD while RXCTL.RXDSTA = EMPTY, this will just return the value of RXD.;If the device writes RXD on the same clock cycle as the host reads RXD:;The host reads the old RXD value.;RXD is updated with the new value, and RXCTL.RXDSTA is set to FULL.

Table 5-19. RXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	SACI command response word. RXCTL.RXDSTA automatically set upon write. RXCTL.RXDSTA automatically cleared upon read (flush operation).

5.10.12 RXCTL Register (Offset = 10Ch) [Reset = 00000000h]

RXCTL is shown in Table 5-20.

Return to the Summary Table.

Receive control register. This register contains status of the RXD register (full/empty), and also software defined flags that are used by the SACI protocol.;The device (boot code) can write the FLAGS field of the RXCTL register.;The device (boot code) can read the RXCTL register.;The host (SWD interface) can only read the RXCTL register

Table 5-20. RXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-1	FLAGS	R/W	0h	Software defined flags that are used by the SACI protocol (device to host).
0	RXDSTA	R	0h	Indicates whether the device has written a word to the RXD register, which can be read by the host:;RXDSTA is automatically set upon write to RXD and automatically cleared upon read from RXD register of SECAP or RXD. 0h = The RXD register does not contain a new SACI response word from the device, and should not be read by the host. 1h = The RXD register contains a new SACI response word from the device, which can be read by the host.

5.10.13 TXDPEEK Register (Offset = 110h) [Reset = 00000000h]

TXDPEEK is shown in Table 5-21.

Return to the Summary Table.

Transmit data peek register . This register is a read-only version of the TXD register that can be read by host and device without any side-effects.;This register is used to peek at the values in TXD without affecting the FULL/EMPTY flag.

Table 5-21. TXDPEEK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Transmit Data Peek Register. SACI command parameter word. TXCTL.TXDSTA not affected by read of TXDPEEK

5.10.14 RXDPEEK Register (Offset = 114h) [Reset = 00000000h]

RXDPEEK is shown in Table 5-22.

Return to the Summary Table.

Receive data peek register. The RXDPEEK register is a read-only version of the RXD register that can be read by host and device without any side-effects;This register is used to peek at the values in Receive Data Register without affecting the FULL/EMPTY flag.

Table 5-22. RXDPEEK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Receive Data Peek Register. SACI command response word. RXCTL.RXDSTA not affected by read of RXDPEEK

5.10.15 SPECIAL_AUTH Register (Offset = 200h) [Reset = 00000000h]

SPECIAL_AUTH is shown in Table 5-23.

Return to the Summary Table.

This register indicates the status of different AP firewalls.

Table 5-23. SPECIAL_AUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	DBGDIS	R	0h	Indicates status of DBGDIS. 0h = Enables debugging capability. 1h = Disables debugging capability
5	AHBAPEN	R	0h	Indicates status of AHBAPEN 0h = Disable AHB-AP 1h = Enable AHB-AP
4	CFGAPEN	R	1h	Indicates status of CFGAPEN 0h = Disable CFG-AP 1h = Enable CFG-AP
3	RESERVED	R	0h	Reserved
2	DFTAPEN	R	0h	Indicates status of DFTAPEN 0h = Disable DFT-TAP 1h = Enable DFT-TAP
1	RESERVED	R	0h	Reserved
0	SECAPEN	R	1h	Indicates status of SECAP 0h = Disable SEC-AP 1h = Enable SEC-AP

5.10.16 SPECIAL_AUTH_SET Register (Offset = 204h) [Reset = 00000000h]

SPECIAL_AUTH_SET is shown in Table 5-24.

Return to the Summary Table.

This register is used for setting bits in SPECIAL_AUTH register. ;This register is configured and locked during device boot.

Table 5-24. SPECIAL_AUTH_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	This field must be configured with 0xA5 in order to access this register. A5h = This field must be written with 0xA5 to be able to set any of the enable bits
23-7	RESERVED	R	0h	Reserved
6	DBGDIS	W	0h	This bit sets DBGDIS in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = SET DBGDIS
5	AHBAPEN	W	0h	This bit sets AHBAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = SET AHB-AP
4	CFGAPEN	W	1h	This bit sets CFGAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Set CFGAPEN
3	RESERVED	R	0h	Reserved
2	DFTAPEN	W	0h	This bit sets DFTAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Set DFTAPEN
1	RESERVED	R	0h	Reserved
0	SECAPEN	W	1h	This bit sets SECAPEN bit in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Set SECAPEN

5.10.17 SPECIAL_AUTH_CLR Register (Offset = 208h) [Reset = 00000000h]

SPECIAL_AUTH_CLR is shown in Table 5-25.

Return to the Summary Table.

This register is used for clearing bits in SPECIAL_AUTH register. ;This register is configured and locked during device boot.

Table 5-25. SPECIAL_AUTH_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	This field must be configured with 0x22 in order to access this register. 22h = This field must be written with 0x22 to be able to clear any of the enable bits
23-7	RESERVED	R	0h	Reserved
6	DBGDIS	W	0h	This bit clears DBGDIS in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Clear DBGDIS
5	AHBAPEN	W	0h	This bit clears AHBAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Clear AHBAPEN
4	CFGAPEN	W	0h	This bit clears CFGAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Clear CFGAPEN
3	RESERVED	R	0h	Reserved
2	DFTAPEN	W	0h	This bit clears DFTAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Clear DFTAPEN
1	RESERVED	R	0h	Reserved
0	SECAPEN	W	0h	This bit clears SECAPEN in SPECIAL_AUTH register. 0h = Writing 0 has no effect 1h = Clear SECAPEN

5.10.18 APP_AUTH Register (Offset = 210h) [Reset = 00000000h]

APP_AUTH is shown in Table 5-26.

Return to the Summary Table.

This register indicates the debug privileges of ARM Cortex CPU.

Table 5-26. APP_AUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	NIDEN	R	0h	Controls non-invasive debug enable. 0h = Non-invasive debug disabled 1h = Non-invasive debug enabled
0	DBGEN	R	0h	Controls invasive debug enable. 0h = Invasive debug disabled 1h = Invasive debug enabled

5.10.19 APP_AUTH_SET Register (Offset = 214h) [Reset = 00000000h]

APP_AUTH_SET is shown in Table 5-27.

Return to the Summary Table.

This register is used for setting bits in APP_AUTH register. ;This register is configured and locked during device boot.

Table 5-27. APP_AUTH_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	This field must be configured with 0x39 in order to access this register. 39h = Write this value 0x39 to unlock writing to the APP_AUTH_SET register
23-2	RESERVED	R	0h	Reserved
1	NIDEN	W	0h	Sets NIDEN bit in [APP_AUTH]register. 0h = Writing 0 has no effect 1h = Sets NIDEN
0	DBGEN	W	0h	Sets DBGEN bit in APP_AUTH register. 0h = Writing 0 has no effect 1h = Sets DBGEN

5.10.20 APP_AUTH_CLR Register (Offset = 218h) [Reset = 00000000h]

APP_AUTH_CLR is shown in Table 5-28.

Return to the Summary Table.

This register is used for clearing bits in APP_AUTH register. ;This register is configured and locked during device boot.

Table 5-28. APP_AUTH_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	This field must be configured with 0x7D in order to access this register. 7Dh = Write this value 0x7D to unlock writing to the APP_AUTH_CLR register
23-2	RESERVED	R	0h	Reserved
1	NIDEN	W	0h	Clears NIDEN bit in APP_AUTH register. 0h = Writing 0 has no effect 1h = Clears NIDEN
0	DBGEN	W	0h	Clears DBGEN bit in APP_AUTH register. 0h = Writing 0 has no effect 1h = Clears DBGEN

5.10.21 DBGCTL Register (Offset = 21Ch) [Reset = 00000000h]

DBGCTL is shown in Table 5-29.

Return to the Summary Table.

Debug control register. This register is used for controlling debug connection and read out debug status.

Table 5-29. DBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	SWDCEN	R/W	1h	This bit is used to enable connection between SWD pads and IceMelter (wakeup circuit used for detecting debug probe) 0h = Connection disabled 1h = Connection enabled
4	DBGPWRUPACK	R	0h	This bit field specifies the status of dbgpwrupack from pmctl. 0h = dbgpwrupreq is not acknowledged 1h = dbgpwrupreq is acknowledged.
3	SYSPWRUPACK	R	0h	This bit field specify the status of syspwrupack from pmctl. 0h = syspwrupreq is not acknowledged 1h = syspwrupreq is acknowledged
2	JTAGSEL	R	0h	This bit field specifies the status of JTAG MODE for TEST TAP. 0h = TEST TAP disabled 1h = TEST TAP enabled
1	SWDSEL	R	0h	This bit field specifies the status of SWD MODE for connection. 0h = debug connection disabled. 1h = debug connection enabled.
0	SWDOVR	R/W	0h	This bit is used for connecting to IO pads to SWCLK/IO on SW-DP through a software request and establish SWD connection without IceMelter trigger for debug purpose. 0h = Transparent mode in which SWD connection is established via IceMelter Sequence. 1h = Force 1 or debug enable mode in which SWD connection is established bypassing IceMelter sequence

Chapter 6

Power, Reset, and Clocking

This chapter describes the systems related to power, resets, and clocking.

6.1 Introduction

Power and clock management is flexible to facilitate low-power applications. The following sections describe details for clock and power control.

The features in this chapter are embedded and optimized in TI's Power Manager. Please see the SDK documentation for more details.

Figure 6-1 shows the hierarchy of power-saving features. Low-power consumption and cycling time for a power-saving mode has an inverse relationship. The power-saving mode with the lowest power consumption requires the longest time from initiation until that power-saving mode is enabled, as well as wake-up time back to active mode. Table 6-1 summarizes the power saving features (VD = Voltage Domain, PD = Power Domain).

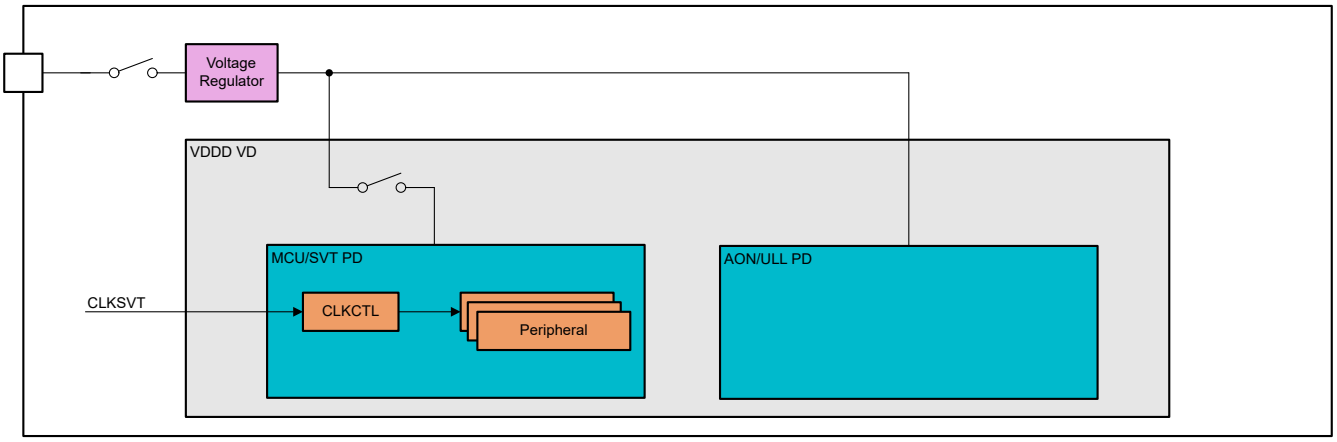

Figure 6-1. Power Hierarchy

Table 6-1. Power Saving Features

Power-Saving Feature	Description
Clock gating	Immediate response - no latency. This feature offers the least amount of power savings.
Power domain off (overrides clock gating)	Power cycling down and up takes longer time than clock gating. Modules in power domains without retention must be reinitialized before functionality can be resumed.
Voltage regulator off	Voltage cycling down and up takes longer time than power domain cycling. The device loses all configurations and boots at wake up. This feature offers the least possible current consumption.

Table 6-2 lists the four defined power modes for the power-saving features in TI's Power Manager listed in Table 6-1. Section 6.4 discusses the power modes in detail.

Table 6-2. Power Modes in the TI Power Manager

Power Mode	Description
Active mode	The system CPU is running. System infrastructure components such as system SRAM memory and system NVM memory are also running. Other MCU IP clocks are SW controlled through CLKCTL.
Idle mode	The system CPU clock is gated. Other MCU IP clocks are SW controlled through CLKCTL. System infrastructure components such as SRAM memory and system NVM memory are dependent on other MCU IPs' clock status.
Standby mode	MCU power domain is powered off, and the VDDD voltage domain is supplied by the µLDO.
Shutdown mode	Only I/Os maintain their state. All voltage regulators, voltage domains, and power domains are off.

6.2 System CPU Modes

The CPU modes, Run, Sleep, and Deep Sleep, are managed by the TI Power API and cannot be directly manipulated. Table 6-3 shows the CPU mode in each TI defined power mode.

Table 6-3. System CPU Modes

TI Power Mode	System CPU Mode
Active Mode	Run Mode
Idle Mode	Sleep Mode
Standby Mode	Deep Sleep Mode

6.3 Supply System

The device supply system is complex and controlled by hardware.

6.3.1 Internal DC/DC Converter and Global LDO

Normally, the VDDS supply pins are powered from a 1.8 V to 3.8 V supply (for example, batteries), and the VDDR supply pins are powered from the internal DC/DC regulator.

Alternatively, the internal Global LDO (GLDO) can be used instead of the DC/DC regulator, but this increases the current consumption of the device. If using the GLDO, disconnect the DCDC pin and remove the DC/DC regulator inductor. The GLDO is connected internally to VDDR. See the device specific data sheet for the GLDO decoupling capacitor requirements. More information on the DC/DC capability can be found in Chapter 18.

6.4 Power States

The following power states and power state transitions are used in the CC27XX device:

6.4.1 RESET

The lowest power state of the device, RESET is entered unconditionally when the reset pin is held low. In this state no oscillators are running, all voltage regulators are disabled and I/Os have both their input and output buffers disabled. There is no internal mechanism to allow software to enter RESET, nor any software mechanism to allow exit from RESET. Thermal shutdown functionality, after being explicitly triggered by software, holds the device in RESET state by pulling the RSTN pin low as long as temperature is above the set threshold. See the device specific data sheet for thermal threshold values.

6.4.2 SHUTDOWN

The lowest power state that can be deliberately entered by software. In this state no oscillators are running, all voltage regulators are disabled, but I/Os retain their state. Level-based wake-up can be configured individually for each I/O pin. The device goes through a full boot when exiting SHUTDOWN, but I/Os remain latched and software is able to discern that the reset cause is I/O wake-up from SHUTDOWN. POR is active in SHUTDOWN but no other voltage supervision is enabled.

6.4.3 ACTIVE

Once the reset pin is deasserted and the minimum supply voltage is supplied, the device enters the ACTIVE power state. HFOSC and the Global LDO are enabled. Once the digital supply is good, the cold boot sequence is performed, applying trims to analog circuitry (including oscillators and voltage regulators) and memories. The CPU boots into the user application at which point the application can configure and enable the DC/DC, low frequency crystal (LFXT) or low frequency oscillator (LFOSC) or high frequency reference clock (HFXT). For more information on the boot process see Chapter 9.

In the ACTIVE power state, both MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU.

6.4.4 IDLE

In IDLE the CPU is in sleep but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on state of the µDMA and debug subsystem.

In Idle mode, all modules are available and power consumption is highly application dependent.

6.4.5 STANDBY

STANDBY is the low power state of the device where LFCLK is running and RTC and Watchdog timer can be active. The MCU domain is powered off, but all logic in the AON power domain remains on and clocked by LFCLK. There are up to 6 wake-up sources for STANDBY to ACTIVE as described in Section 4.4.4.3. When in STANDBY, the DC/DC or GLDO is duty cycled to periodically recharge VDDR. On STANDBY exit, SVT is powered up again. MCU modules with retention will restore the state they had before STANDBY entry. See Figure 6-3 to see which modules have retention. Modules without retention are reset and need to be reconfigured when exiting STANDBY.

6.4.6 PMCTL Registers

Table 6-4 lists the memory-mapped registers for the PMCTL registers. All register offset addresses not listed in Table 6-4 should be considered as reserved locations and the register contents should not be modified.

Table 6-4. PMCTL Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 6.4.6.1
4h	DESCEX	Extended Description Register.	Section 6.4.6.2
8h	SHTDWN	Shutdown Register.	Section 6.4.6.3
Ch	SLPCTL	Sleep Control Register.	Section 6.4.6.4
10h	WUSTA	Wakeup Status Register	Section 6.4.6.5
14h	VDDRCTL	VDDR Control Register.	Section 6.4.6.6
20h	SYSFSET	Internal. Only to be used through TI provided API.	Section 6.4.6.7
24h	SYSFCLR	Internal. Only to be used through TI provided API.	Section 6.4.6.8
28h	SYSFSTA	Internal. Only to be used through TI provided API.	Section 6.4.6.9
2Ch	RSTCTL	Reset Control Register.	Section 6.4.6.10
30h	RSTSTA	Reset Status.	Section 6.4.6.11
34h	BOOTSTA	Internal. Only to be used through TI provided API.	Section 6.4.6.12
3Ch	AONRSTA1	AON Register Status 1.	Section 6.4.6.13
40h	AONRSET1	AON Register Set 1.	Section 6.4.6.14
44h	AONRCLR1	AON register clear 1	Section 6.4.6.15
4Ch	DELTA	Delta Time Register.	Section 6.4.6.16
50h	WUTIME	WakeUp Time Register.	Section 6.4.6.17
54h	PREPUCTL	Pre Power-Up Control Register.	Section 6.4.6.18
58h	SWSTMP	SW Time Stamp Register.	Section 6.4.6.19
64h	ETPP	Internal. Only to be used through TI provided API.	Section 6.4.6.20
7Ch	RETCFG0	Internal. Only to be used through TI provided API.	Section 6.4.6.21
80h	RETCFG1	Internal. Only to be used through TI provided API.	Section 6.4.6.22
84h	RETCFG2	Internal. Only to be used through TI provided API.	Section 6.4.6.23
88h	RETCFG3	Internal. Only to be used through TI provided API.	Section 6.4.6.24
8Ch	RETCFG4	Internal. Only to be used through TI provided API.	Section 6.4.6.25
90h	RETCFG5	Internal. Only to be used through TI provided API.	Section 6.4.6.26
94h	RETCFG6	Internal. Only to be used through TI provided API.	Section 6.4.6.27
98h	RETCFG7	Internal. Only to be used through TI provided API.	Section 6.4.6.28
A8h	HFXTCTL	HFXT Control Register.	Section 6.4.6.29
ACh	LFCAL	Low Frequency Calibration Register.	Section 6.4.6.30
B0h	VREFCFG	Internal. Only to be used through TI provided API.	Section 6.4.6.31
B4h	VREFSTA	VREF Status Register.	Section 6.4.6.32

Complex bit access types are encoded to fit into small table cells. Table 6-5 shows the codes that are used for access types in this section.

Table 6-5. PMCTL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

Table 6-5. PMCTL Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

6.4.6.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 6-6.

Return to the Summary Table.

Description Register.;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 6-6. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	D741h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	0h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	2h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

6.4.6.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 6-7.

Return to the Summary Table.

Extended Description Register.;This register shows ULL IP availability and memory size configuration.

Table 6-7. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	FLASHSZ	R	3h	System flash availability 0h = Flash size set to level 0 (Min size) 1h = Flash size set to level 1 2h = Flash size set to level 2 3h = Flash size set to level 3 (Max size)
29-28	SRAMSZ	R	3h	System SRAM availability 0h = SRAM size set to level 0 (Min size) 1h = SRAM size set to level 1 2h = SRAM size set to level 2 3h = SRAM size set to level 3 (Max size)
27	RESERVED	R	0h	Reserved
26	LPCMP	R	1h	LPCMP (low power comparator) IP status on device 0h = IP is unavailable 1h = IP is available
25-0	RESERVED	R	0h	Reserved

6.4.6.3 SHTDWN Register (Offset = 8h) [Reset = 00000000h]

SHTDWN is shown in Table 6-8.

Return to the Summary Table.

Shutdown Register.;This register controls SHUTDOWN mode entry.

Table 6-8. SHTDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	KEY	W	0h	Setting a valid key will trigger the device to enter SHUTDOWN mode. A5A5h = This is the only valid key value that will trigger SHUTDOWN mode.;All other values are invalid and will have no effect.

6.4.6.4 SLPCTL Register (Offset = Ch) [Reset = 00000000h]

SLPCTL is shown in Table 6-9.

Return to the Summary Table.

Sleep Control Register.;This register controls I/O pad sleep mode. When I/O pad sleep mode is enabled all I/O pad outputs and I/O pad configurations are latched. Inputs are transparent if I/O pad is configured as input.

Table 6-9. SLPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SLPN	R/W	0h	The boot code will set this bit field and disable sleep mode, automatically unless waking up from a SHUTDOWN RSTSTA.SDDET is set.;Application software must reconfigure the state for all IO's before setting this bit field upon waking up from a SHUTDOWN to avoid glitches on pins. 0h = I/O pad sleep mode is enabled 1h = I/O pad sleep mode is disabled

6.4.6.5 WUSTA Register (Offset = 10h) [Reset = 00000000h]

WUSTA is shown in Table 6-10.

Return to the Summary Table.

Wakeup Status Register;This register shows the device wakeup source. Used to distinguish between wakeup from STANDBY, SHUTDOWN and reset.

Table 6-10. WUSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SRC	R	1h	This field shows the device wakeup source. 1h = Wakeup from system reset / SHUTDOWN mode. ;See RSTSTA for more status information. 2h = Wakeup from STANDBY mode.

6.4.6.6 VDDRCTL Register (Offset = 14h) [Reset = 00000000h]

VDDRCTL is shown in Table 6-11.

Return to the Summary Table.

VDDR Control Register.;This register contains VDDR regulator settings for the device.

Table 6-11. VDDRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	STBY	R/W	0h	Select between continuous or duty-cycled VDDR regulation in STANDBY mode. 0h = Duty-cycled VDDR regulation in STANDBY mode. 1h = Continuous VDDR regulation in STANDBY mode.
0	SELECT	R/W	0h	Select between GLDO and DCDC as VDDR regulator (in ACTIVE, IDLE and STANDBY mode). 0h = GLDO enabled for regulation of VDDR voltage 1h = DCDC enabled for regulation of VDDR voltage

6.4.6.7 SYSFSET Register (Offset = 20h) [Reset = 00000000h]

SYSFSET is shown in Table 6-12.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-12. SYSFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	FLAG2	W	0h	Internal. Only to be used through TI provided API.
1	FLAG1	W	0h	Internal. Only to be used through TI provided API.
0	FLAG0	W	0h	Internal. Only to be used through TI provided API.

6.4.6.8 SYSFCLR Register (Offset = 24h) [Reset = 00000000h]

SYSFCLR is shown in Table 6-13.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-13. SYSFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	FLAG2	W	0h	Internal. Only to be used through TI provided API.
1	FLAG1	W	0h	Internal. Only to be used through TI provided API.
0	FLAG0	W	0h	Internal. Only to be used through TI provided API.

6.4.6.9 SYSFSTA Register (Offset = 28h) [Reset = 00000000h]

SYSFSTA is shown in Table 6-14.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-14. SYSFSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	FLAG2	R	0h	Internal. Only to be used through TI provided API.
1	FLAG1	R	0h	Internal. Only to be used through TI provided API.
0	FLAG0	R	0h	Internal. Only to be used through TI provided API.

6.4.6.10 RSTCTL Register (Offset = 2Ch) [Reset = 00000000h]

RSTCTL is shown in Table 6-15.

Return to the Summary Table.

Reset Control Register.;This register configures and controls system reset.

Table 6-15. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	VGMDLYN	R/W	0h	VDD glitch monitor delay.;This bit configures if exit out of STANDBY will be stalled until VGM has settled or not.;When bypassed the CPU execution will potentially start before the VGM is ready. 0h = Ensure that VGM has settled before we exit STANDBY. 1h = VGM settling will not stall exit out of STANDBY.
2	LFLOSS	R/W	0h	LF clock loss reset enable.;Trigger system reset when LF clock loss is detected, which reset the entire device and causes a reboot of the system.;The system reset event is captured as RSTSTA.RESETSRC set to SYSRESET and RSTSTA.SYSSRC set to LFLOSSEV. 0h = LF clock loss detection will not trigger a system reset. 1h = LF clock loss detection will trigger a system reset.
1	TSDEN	R/W	0h	TSD (Thermal Shutdown) enable. ;TSD will trigger an immediate system reset, which reset the entire device and causes a reboot of the system.;The device will be in reset until released by the TSD IP.;The system reset event is captured as RSTSTA.TSDEV flag set. 0h = No effect 1h = Temperature shutdown comparator enable. ;Note: If TSD IP not present, see DESCEX.TSD, enable will have no effect.
0	SYSRST	R/W	0h	Trigger system reset, which will reset the entire device and causes a reboot of the system.;The system reset event is captured as RSTSTA.RESETSRC set to SYSRESET and RSTSTA.SYSSRC set to SYSRSTEV. 0h = No effect 1h = Trigger a system reset.

6.4.6.11 RSTSTA Register (Offset = 30h) [Reset = 00000000h]

RSTSTA is shown in Table 6-16.

Return to the Summary Table.

Reset Status. ;This register contains the reset source and SHUTDOWN wakeup source for the system.;Check WUSTA.SRC first to ensure that wakeup from STANDBY is not set.;The capture feature is not rearmed until all of the possible reset sources have been released and the result has been copied to this register. ;During the copy and rearm process it is one 24MHz period in which an eventual new system reset will be reported as Power on reset regardless of the root cause.

Table 6-16. RSTSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	SDDET	R	0h	Wakeup from SHUTDOWN flag.;Note: This flag will be cleared when SLPCTL.SLPN is asserted. 0h = Wakeup from SHUTDOWN mode not triggered. 1h = Wakeup from SHUTDOWN mode
16	IOWUSD	R	0h	Wakeup from SHUTDOWN on an I/O event flag.;Note: This flag will be cleared when SLPCTL.SLPN is asserted. 0h = Wakeup from SHUTDOWN not triggered by an I/O event. 1h = Wakeup from SHUTDOWN triggered by an I/O event.
15	RTCSTA	R	0h	RTC TIME reset status.;This bit shows if the last system reset event cleared RTC TIME or not. 0h = System reset event cleared RTC TIME 1h = System reset event did not clear RTC TIME
14-8	RESERVED	R	0h	Reserved
7-4	SYSSRC	R	0h	Shows which reset event that triggered SYSRESET in RESETSRC. 0h = LF clock loss event 1h = CPU reset event 2h = CPU LOCKUP event 3h = Watchdog timeout event 4h = System reset event 5h = Serial Wire Debug reset event 6h = Analog FSM timeout event 7h = Electromagnetic sensor event 8h = Tamper event 9h = SRAM parity error event Eh = Analog Error reset event Fh = Digital Error reset event
3	TSDEV	R	0h	System reset triggered by TSD event 0h = TSD event not triggered 1h = System reset triggered by TSD event
2-0	RESETSRC	R	0h	Shows the root cause of the last system reset. More than one reported reset source can have been active during the last system reset, but only the root cause is reported.;If reset cause is SYSRESET or PINRESET, the other reset flags must be read to determine actual root cause. 0h = Power on reset 1h = Reset pin. TSD will also trigger a pin reset, so actual root cause is given by TSDEV reset flag status. 2h = Brown out detect on VDDS 4h = Brown out detect on VDDR 6h = Digital system reset. Actual root cause is given by SYSSRC. 7h = VDD glitch detection reset

6.4.6.12 BOOTSTA Register (Offset = 34h) [Reset = 00000000h]

BOOTSTA is shown in Table 6-17.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-17. BOOTSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	FLAG	R/W	0h	Internal. Only to be used through TI provided API.

6.4.6.13 AONRSTA1 Register (Offset = 3Ch) [Reset = 00000000h]

AONRSTA1 is shown in Table 6-18.

Return to the Summary Table.

AON Register Status 1.;This register contains the general purpose AON flags for SW, and is updated through AONRSET1.FLAG and AONRCLR1.FLAG.;The register is only reset on a POR event.

Table 6-18. AONRSTA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20	VDDIOPGIO	R	0h	VDDIO power good.;Controls the I/O pads on the VDDIO segment.
19-18	RESERVED	R	0h	Reserved
17-0	FLAG	R	Xh	State of the AON register flags

6.4.6.14 AONRSET1 Register (Offset = 40h) [Reset = 00000000h]

AONRSET1 is shown in Table 6-19.

Return to the Summary Table.

AON Register Set 1.;This register sets the AON flags that can be read through AONRSTA1.FLAG.

Table 6-19. AONRSET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20	VDDIOPGIO	W	0h	Write 1 to set AONRSTA1.VDDIOPGIO. 0h = No effect 1h = Set flag
19-18	RESERVED	R	0h	Reserved
17-0	FLAG	W	Xh	Write 1 to set AONRSTA1.FLAG 0h = No flags changed status 0003FFFFh = Set all flags

6.4.6.15 AONRCLR1 Register (Offset = 44h) [Reset = 00000000h]

AONRCLR1 is shown in Table 6-20.

Return to the Summary Table.

AON register clear 1;Clear the AON flags that can be read through AONRSTA1.FLAG

Table 6-20. AONRCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20	VDDIOPGIO	W	0h	Write 1 to clear AONRSTA1.VDDIOPGIO. 0h = No effect 1h = Clear flag
19-18	RESERVED	R	0h	Reserved
17-0	FLAG	W	Xh	Write 1 to clear AONRSTA1.FLAG 0h = No flags changed status 0003FFFFh = Clear all flags

6.4.6.16 DELTA Register (Offset = 4Ch) [Reset = 00000000h]

DELTA is shown in Table 6-21.

Return to the Summary Table.

Delta Time Register.;This register contains the measured delta time during wakeup from STANDBY mode.

Table 6-21. DELTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SLWP	R	0h	Slow part.;States which of HFXT ready or SW ready that completed first during wakeup from STANDBY mode. 0h = No valid measurement available 1h = HFXT ready set before SW ready (SWSTMP.SWRDY) 2h = HFXT ready set after SW ready (SWSTMP.SWRDY) 3h = No valid measurement available
29-12	RESERVED	R	0h	Reserved
11-0	TIME	R	0h	Delta time.;Measured time in us between SWSTMP.SWRDY and HFXT ready. ;This is a always a positive number, and SLWP is used to determine which event occurred first.;Measurement is enabled when PREPUCTL.WUTIMEN is set.

6.4.6.17 WUTIME Register (Offset = 50h) [Reset = 00000000h]

WUTIME is shown in Table 6-22.

Return to the Summary Table.

WakeUp Time Register.;This register contains the measured wakeup times from STANDBY mode.

Table 6-22. WUTIME Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	DIGWU	R	0h	Digital wakeup time. ;Gives the time (in us) from HFSOC is running until CPU execution starts.;Measurement is enabled when PREPUCTL.WUTIMEN is set.
15-8	RESERVED	R	0h	Reserved
7-0	HFXTWU	R	0h	HFXT wakeup time.;Gives the time (in us) from HFSOC is running until HFXT auto enable is triggered.;Measurement is enabled when PREPUCTL.WUTIMEN is set.

6.4.6.18 PREPUCTL Register (Offset = 54h) [Reset = 00000000h]

PREPUCTL is shown in Table 6-23.

Return to the Summary Table.

Pre Power-Up Control Register.;This register contains settings and control for pre-powerup, STANDBY and wakeup measurements.

Table 6-23. PREPUCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PREPUEN	R/W	0h	Pre powerup Enable.;When this bit is set, the device will start the wakeup process in advance of the RTC wakeup event.;This to start HFXT settling earlier, so that HFXT can be ready when SW is ready.;Note that HFXTCTL.AUTO must be enabled to turn on HFXT. 0h = Disable pre-powerup 1h = Enable pre-powerup
30	WUTIMEN	R/W	0h	Wakeup time measurement enable.;When set will enable WUTIME.DIGWU, WUTIME.HFXTWU and DELTA.TIME time measurements. 0h = Disable wakeup time measurement 1h = Enable wakeup time measurement
29-16	RESERVED	R	0h	Reserved
15-8	CONS	R/W	0h	Conservative pre-wakeup time.;When PREPUEN is set, the device will start the wakeup process in advance of the RTC wakeup event.;This field will give the conservative time in advance of a RTC event. Conservative value is used if a temperature change has been detected since STANDBY mode was entered.;The time unit for the value is 8us. 0h = Smallest value FEh = Highest possible value
7-0	NOM	R/W	0h	Nominal pre-wakeup time.;When PREPUEN is set, the device will start the wakeup process in advance of the RTC wakeup event.;This field will give the nominal time in advance of a RTC event. Nominal value is used if no temperature change has been detected since STANDBY mode was entered.;The time unit for the value is 8us. 0h = Smallest value FEh = Highest possible value

6.4.6.19 SWSTMP Register (Offset = 58h) [Reset = 00000000h]

SWSTMP is shown in Table 6-24.

Return to the Summary Table.

SW Time Stamp Register.;This register is used to set the SW time stamp for the delta time measurement.

Table 6-24. SWSTMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SWRDY	R/W	0h	SW ready.;Set by SW to indicate when SW is ready. Used to measure DELTA.TIME and DELTA.SLWP.;This bit is auto-cleared by HW. 0h = No effect 1h = Set SW ready time stamp. Auto-cleared by HW

6.4.6.20 ETPP Register (Offset = 64h) [Reset = 00000000h]

ETPP is shown in Table 6-25.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-25. ETPP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved

6.4.6.21 RETCFG0 Register (Offset = 7Ch) [Reset = 00000000h]

RETCFG0 is shown in Table 6-26.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-26. RETCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	Internal. Only to be used through TI provided API.

6.4.6.22 RETCFG1 Register (Offset = 80h) [Reset = 00000000h]

RETCFG1 is shown in Table 6-27.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-27. RETCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	Internal. Only to be used through TI provided API.

6.4.6.23 RETCFG2 Register (Offset = 84h) [Reset = 00000000h]

RETCFG2 is shown in Table 6-28.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-28. RETCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	Internal. Only to be used through TI provided API.

6.4.6.24 RETCFG3 Register (Offset = 88h) [Reset = 00000000h]

RETCFG3 is shown in Table 6-29.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-29. RETCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

6.4.6.25 RETCFG4 Register (Offset = 8Ch) [Reset = 00000000h]

RETCFG4 is shown in Table 6-30.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-30. RETCFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-3	RESERVED	R	0h	Reserved
2-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

6.4.6.26 RETCFG5 Register (Offset = 90h) [Reset = 00000000h]

RETCFG5 is shown in Table 6-31.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-31. RETCFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	1h	Internal. Only to be used through TI provided API.

6.4.6.27 RETCFG6 Register (Offset = 94h) [Reset = 00000000h]

RETCFG6 is shown in Table 6-32.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-32. RETCFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

6.4.6.28 RETCFG7 Register (Offset = 98h) [Reset = 00000000h]

RETCFG7 is shown in Table 6-33.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-33. RETCFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
30-3	RESERVED	R	0h	Reserved
2-0	VAL	R/W	1h	Internal. Only to be used through TI provided API.

6.4.6.29 HFXTCTL Register (Offset = A8h) [Reset = 00000000h]

HFXTCTL is shown in Table 6-34.

Return to the Summary Table.

HFXT Control Register.;This register controls features to turn on/off HFXT automatically.

Table 6-34. HFXTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	LFCAL	R/W	0h	LF Calibration Enable.;Turn on/off HFXT periodically to perform LF oscillator calibration. ;LF oscillator period and measurement time is configured through LFCAL. 0h = HFXT on/off periodically for LF calibration is disabled. 1h = HFXT on/off periodically for LF calibration is enabled.
0	AUTO	R/W	1h	Turn on/off HFXT during STANDBY entry/exit. 0h = HFXT is neither turned on/off during STANDBY entry/exit 1h = HFXT turned off when entring STANDBY and turned on when leaving STANDBY.

6.4.6.30 LFCAL Register (Offset = ACh) [Reset = 00000000h]

LFCAL is shown in Table 6-35.

Return to the Summary Table.

Low Frequency Calibration Register.;This register contains the period and measurement time setting used for LF oscillator calibration.;The LF calibartion feature is enabled through HFXTCTL.LFCAL.

Table 6-35. LFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	QUAL	R/W	0h	CKM qualifier configuration. ;Used to qualify that LF calibration is completed before HFXT is request off. 0h = Disable CKM qualifier 1h = Enable CKM qualifier
30-24	RESERVED	R	0h	Reserved
23-16	MEAS	R/W	0h	LFCAL measurment time, given in number of 32kHz periods. FFh = Maximum LFCAL measurment time
15-8	RESERVED	R	0h	Reserved
7-0	PER	R/W	0h	LFCAL period time, given in number of 256 * 32kHz periods. FFh = Maximum LFCAL period time

6.4.6.31 VREFCFG Register (Offset = B0h) [Reset = 00000000h]

VREFCFG is shown in Table 6-36.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-36. VREFCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	TIMEOUT	R/W	11h	Internal. Only to be used through TI provided API.

6.4.6.32 VREFSTA Register (Offset = B4h) [Reset = 00000000h]

VREFSTA is shown in Table 6-37.

Return to the Summary Table.

VREF Status Register.;This register contains VREF settling status.

Table 6-37. VREFSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	GOOD	R	0h	VREF settling / good status. 0h = VREF voltage is not good. 1h = VREF voltage is good.

6.5 Digital Power Partitioning

The device has a single voltage domain, VDDD. Within VDDD there are two power domains. The always-on AON domain and the switchable MCU domain. Throughout this documentation register mnemonics or descriptions can also reference the ULL domain, this is an alternative term for AON and is equivalent in all ways. Similarly the MCU domain can be described in register mnemonics or descriptions as SVT. See Figure 6-2 and Figure 6-3 for an overview of the voltage and power partitioning.

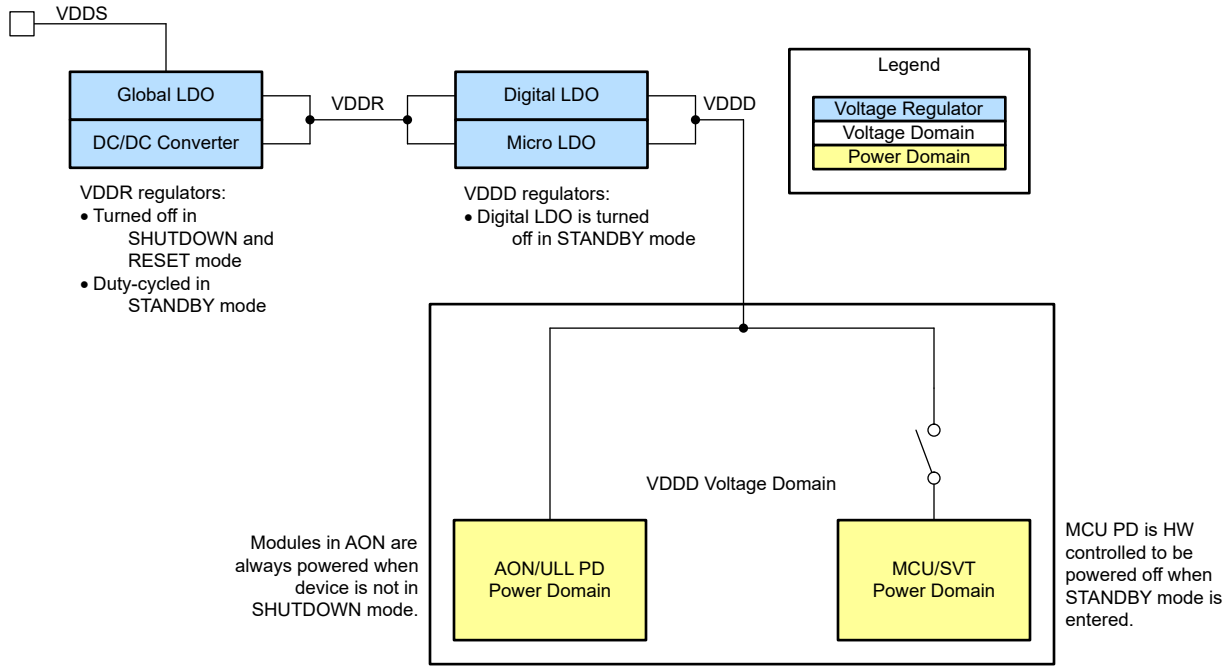

Figure 6-2. Power Supply System

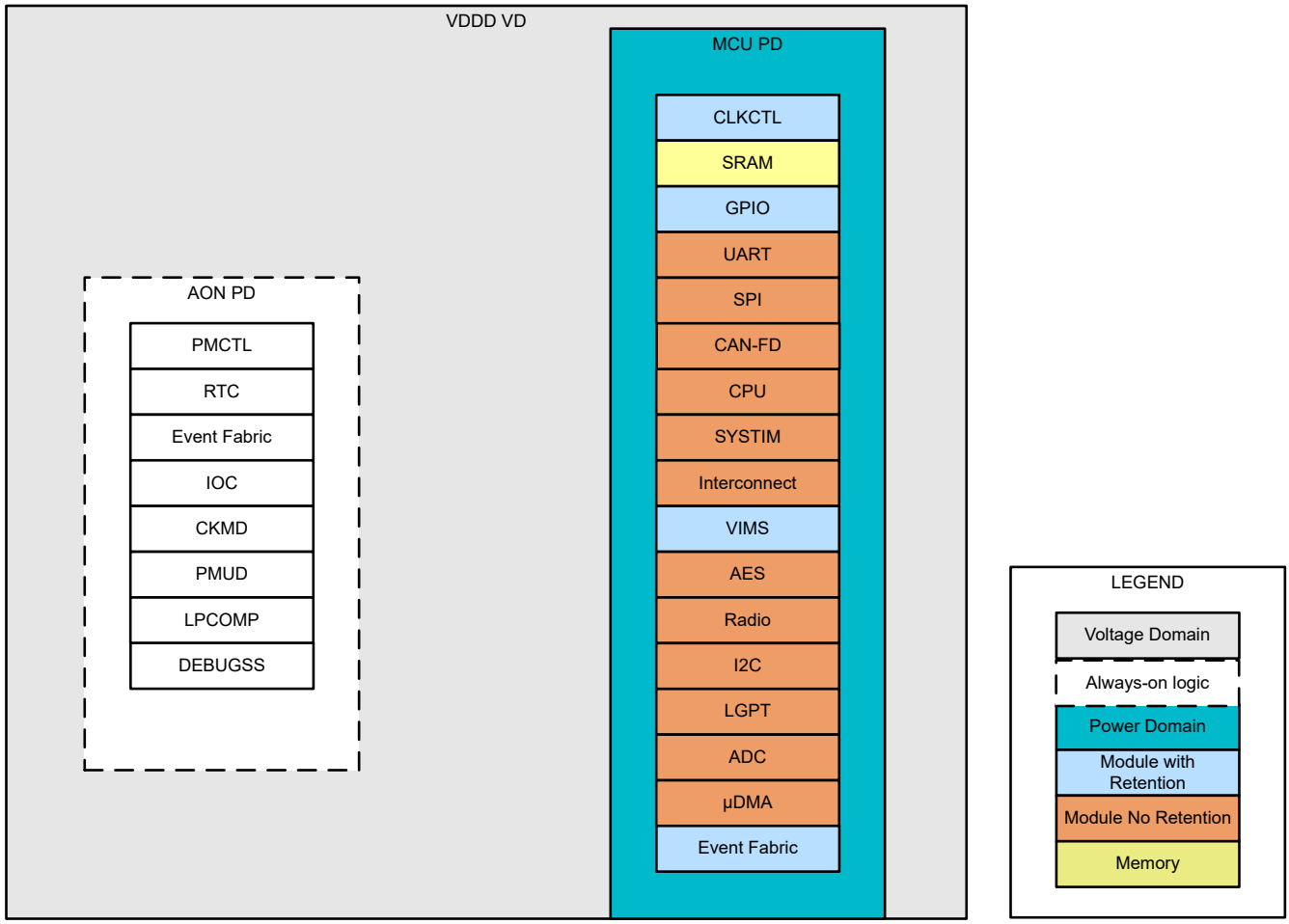

Figure 6-3. Power Partitioning

6.6 Clocks

CC27XX uses a single clock for the MCU domain (CLKSVT), and a single clock for the AON domain (CLKULL).

6.6.1 Block Diagram

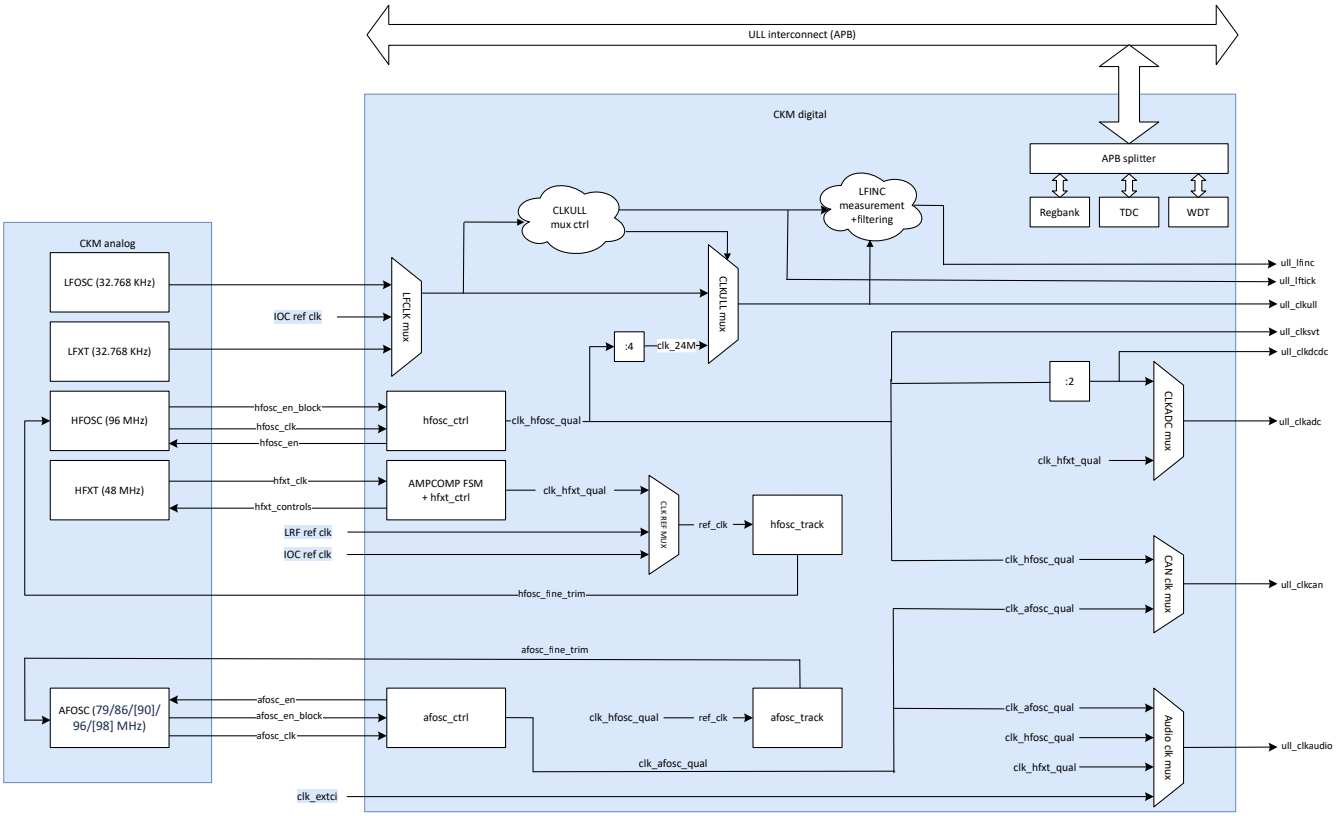

Figure 6-4. CKM Bock diagram

6.6.2 LF clock

We can choose the LF clock between the following 4 options using the MMR CKMD.LFCLKSEL.MAIN :

1. No LF clock
2. LFOSC
3. LFXT
4. External LF clock from DIO

The chosen LF clock is delayed in Analog. The delay is configurable through the MMR CKMD.TRIM1.LFDLY.

The delayed LF clock is used to increment RTC and also as a system clock in standby.

When the selected Low frequency clock is not running, HFOSC clock is used to generate a Fake LF clock. Hence Low frequency clock can be categorized into :

1. Real LF clock (Which can be from LFOSC or LFXT or External LF clock from DIO)
2. Fake LF clock (Which is generated using HFOSC, which can be tracked or untracked)

6.6.2.1 LFINC measurement mechanism

This mechanism calculates the time period of 1 LF clock (referred to as LFINC) and provides it to RTC to maintain the system time across standby entry exits.

The LFINC value is of format 6b.16b us and can be from any of the following 4 sources :

1. Fixed 0x1E8000 - This value corresponds to an LF period of 30.5us.
2. Filtered (average) value - This is the average value of LF clock's period measured till now
3. Direct measurement value - This is the live value of LF clock's period measured using the faster ULL clock (24 MHz)
4. MMR CKMD.LFINCOVR.LFINC - Override value when CKMD.LFINCOVR.OVERRIDE is set

There are a number of factors that determine which of the 1st three sources of LF period would be forwarded to RTC. These are mentioned below :

1. Whether the LF clock is running or not
2. Whether HFOSC tracking is active or not
3. Whether the LF filter has settled or not (read the read-only MMR LFCLKSTAT.FLTSETTLED)
4. Whether LFINCCTL.PREVENTSTBY MMR is set or not

The above 4 factors are also responsible for deciding whether the LF filter is getting updated or not. This is better explained using the truth table given below :

LFOSC running	Tracking Active	LF filter Settled	CKMD.LFINCCTL. PREVENTSTBY	LFINC Source	LFTICK Source	Filter Update
0	0	0	0	Constant (0x1E8000 i.e. 30.5us)	Untracked HFOSC/4	No
0	0	0	1	Constant (0x1E8000 i.e. 30.5us)	Untracked HFOSC/4	No
0	0	1	0	Constant (0x1E8000 i.e. 30.5us)	Untracked HFOSC/4	No
0	0	1	1	Constant (0x1E8000 i.e. 30.5us)	Untracked HFOSC/4	No
0	1	0	0	Constant (0x1E8000 i.e. 30.5us)	Tracked HFOSC/4	No
0	1	0	1	Constant (0x1E8000 i.e. 30.5us)	Tracked HFOSC/4	No
0	1	1	0	Constant (0x1E8000 i.e. 30.5us)	Tracked HFOSC/4	No
0	1	1	1	Constant (0x1E8000 i.e. 30.5us)	Tracked HFOSC/4	No
1	0	0	0	Filter	LFOSC	No
1	0	1	0	Filter	LFOSC	No
1	0	1	1	Filter	LFOSC	No
1	1	0	0	Live	LFOSC	Yes
1	1	0	1	Live	LFOSC	Yes
1	1	1	0	Live	LFOSC	Yes
1	1	1	1	Live	LFOSC	Yes

6.6.2.2 LFINC Filtering

LFINC is filtered using a proportional filter with automatic gearing. The filter is enabled only when the real LFCLK is available and the tracking loop is running (to provide a precise HFOSC).

If CKMD.LFINCCTL.PREVENTSTBY is set and the filter is not settled because the tracking is not active, the filter can still continue to run until it's settled.

- Gearing adjusts the K value to 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, (1/1024)
  - The final gear can be selected in MMR CKMD.LFINCCTL.STOPGEAR
- Gearing reduces K to the next value after 8 updates without too large of an error (configurable)
- Gearing increases K (in steps of two) whenever a large error is seen
  - This event is available as IRQ (LFGEARRSTRT)
- The filter indicates "settled" when the final gear is reached
  - This status is available as CKMD.LFCLKSTAT.FLTSETTLED (only when the filter is running)
  - The filter can optionally prevent STANDBY entry when not settled (CKMD.LFINCCTL.PREVENTSTBY)

Configuration of "too large of an error" for increasing K:

- The filter uses a "decaying error accumulator" with a decay rate configured in CKMD.LFINCCTL.ERRTHR
  - LARGE means "fastest decay" (actually no history at all)

large instantaneous errors (approximately 125ns) are needed to make the error accumulator cross the threshold
  - MIDLARGE means "fast decay"

    subsequent large errors in the same direction make the error accumulator cross the threshold
  - MIDSMALL means "slower decay"

    subsequent smaller errors in the same direction make the error accumulator cross the threshold
  - SMALL means "slowest decay"

    even smaller errors in the same direction required to make the error accumulator cross the threshold
- CKMD.LFINCCTL.GEARRSTRT decides when to increase K:
  - NEVER – used for "bad" clocks (high frequency variation), when the automatic gearing restarts prevents settling at all
  - ONETHR – increase K when the threshold is crossed once
  - TWOTHR – increase K when the threshold is crossed twice in a row in the same direction (positive/ negative)
- CKMD.LFINCCTL.SOFTRSTRT decides if K can also be increased for the first update after wakup / re-enabling the filter (to account for potential frequency changes during STANDBY / periods without tracking loop)

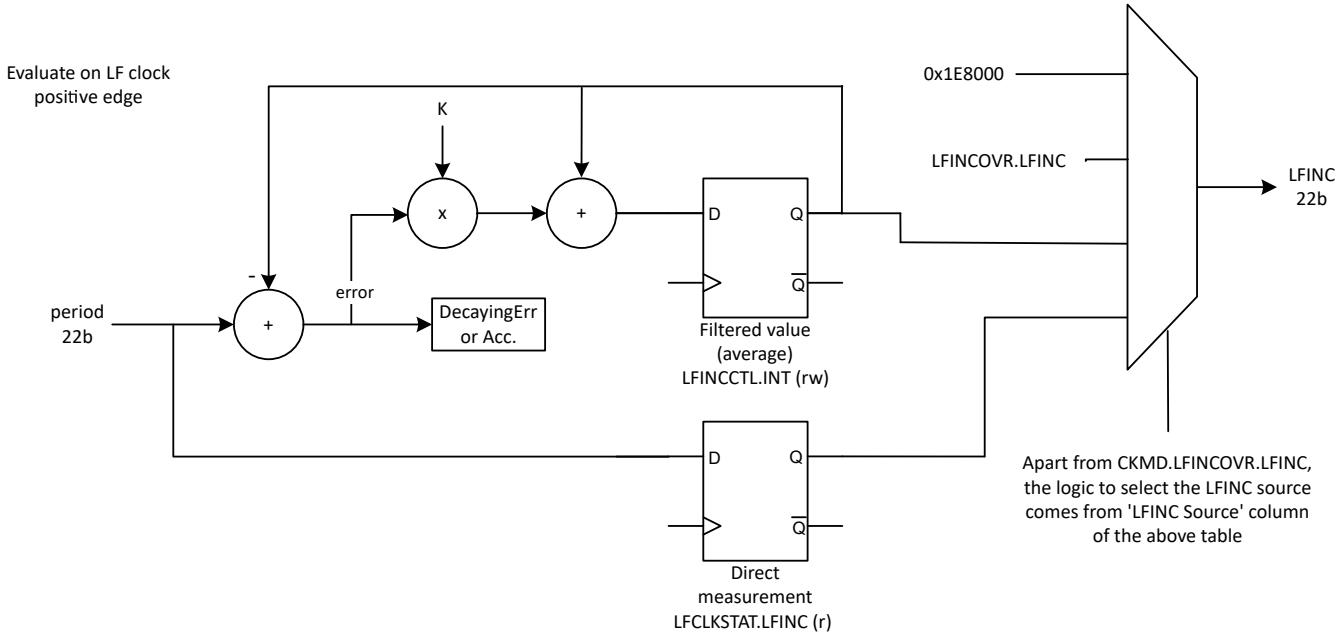

Figure 6-5. Block Diagram

Comparison of the filter transfer function for different values of K.

The transfer function of the filter can be written as:

$$TF = k^{*}z/(z + (k - 1)) \quad (1)$$

The filter bandwidth for different values of K is mentioned below :

Loop Bandwidth with k = 1/8: 674.6353Hz
Loop Bandwidth with k = 1/16: 337.3176Hz
Loop Bandwidth with k = 1/32: 166.2145Hz
Loop Bandwidth with k = 1/64: 81.92Hz
Loop Bandwidth with k = 1/128: 40.96Hz

Loop Bandwidth with k = 1/256: 20.4071Hz
Loop Bandwidth with k = 1/512: 10.2036Hz
Loop Bandwidth with k = 1/1024: 5.0995Hz

Higher values of Loop Bandwidth result in higher sensitivity to variations in LFOSC frequency. To ensure the filter reduces the effects of noise from the LFOSC frequency, the gearing mechanism is designed such that it starts with a larger value of 'k' to help the filter settle faster, and eventually settles on a small value of 'k' which reduces the noise of LFOSC.

6.6.3 HFOSC

HFOSC is an RC oscillator running at 96 MHz.

6.6.3.1 HFOSC control and qualification

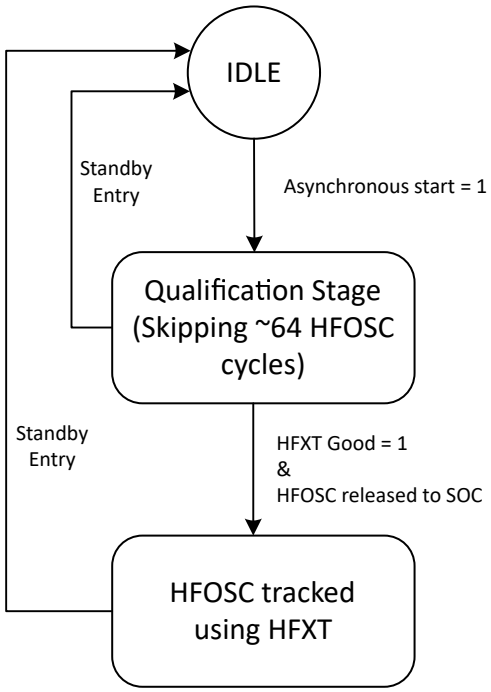

Figure 6-6. HFOSC qualification

The counter will skip a number of pulses when the clock is not stable enough.

6.6.3.2 HFOSC Tracking Loop

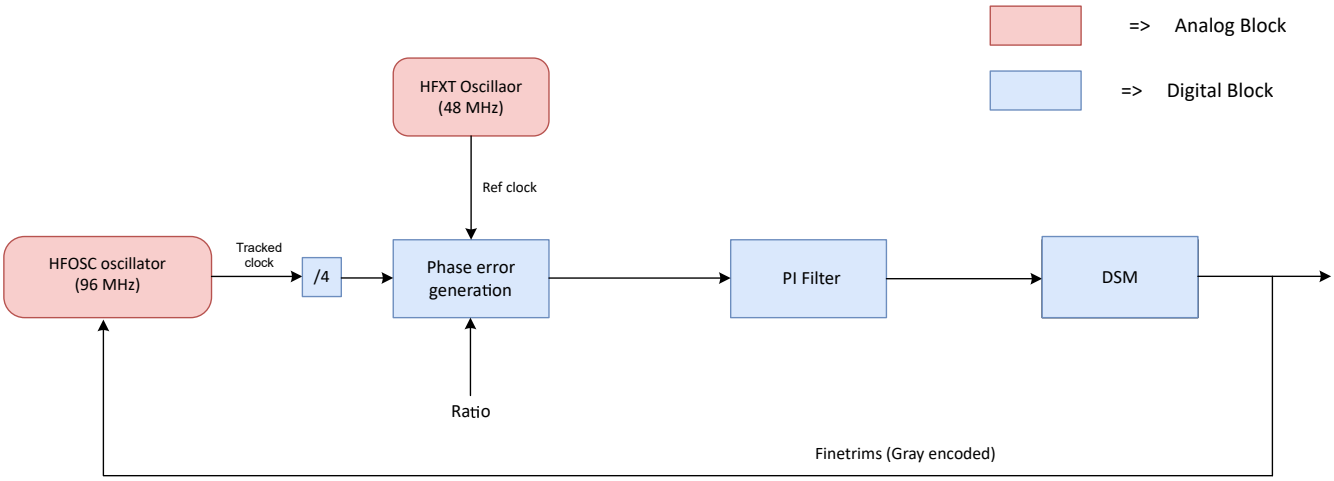

Figure 6-7. HFOSC Tracking Loop

1. HFOSC (internal RC oscillator) is tracked using HFXT (External crystal oscillator)
2. To enable this tracking loop, the following MMRs must be set :-
   a. CKMD.HFTRACKCTL.EN
   b. CKMD.HFXTCTL.EN
3. The Tracking loop ratio is adjusted using CKMD.HFTRACKCTL.RATIO MMR.

   The ratio is of format 2b.24b. i.e. there are 24 fractional bits.

   HFTRACKCTL.RATIO = [(ull_freq)/(2*HFXT freq)]*2^24 = [24/2*48]*2^24 = 0x400000

   Note

   Multiply by 2^24 because we want to shift the decimal by 24 bits, as the ratio format is 2.24b.
4. The KI and KP value of the loop filter is adjusted using the MMR CKMD.LOOPCFG.
5. The filter is designed to achieve <100ppm in ~250us and <1ppm in ~1s

6.6.4 AFOSC

AFOSC is an RC oscillator that can be run at the following frequencies by configuring the TRIMS and tracking loop ratios. The MMRs for configuration are as follows :

1. CKMD.ATTRACKCTL.RATIO
2. TRIM0.AFOSC_COARSE
3. TRIM0.AFOSC_MID
4. TRIM0.AFOSC_MODE

6.6.4.1 AFOSC control and qualification

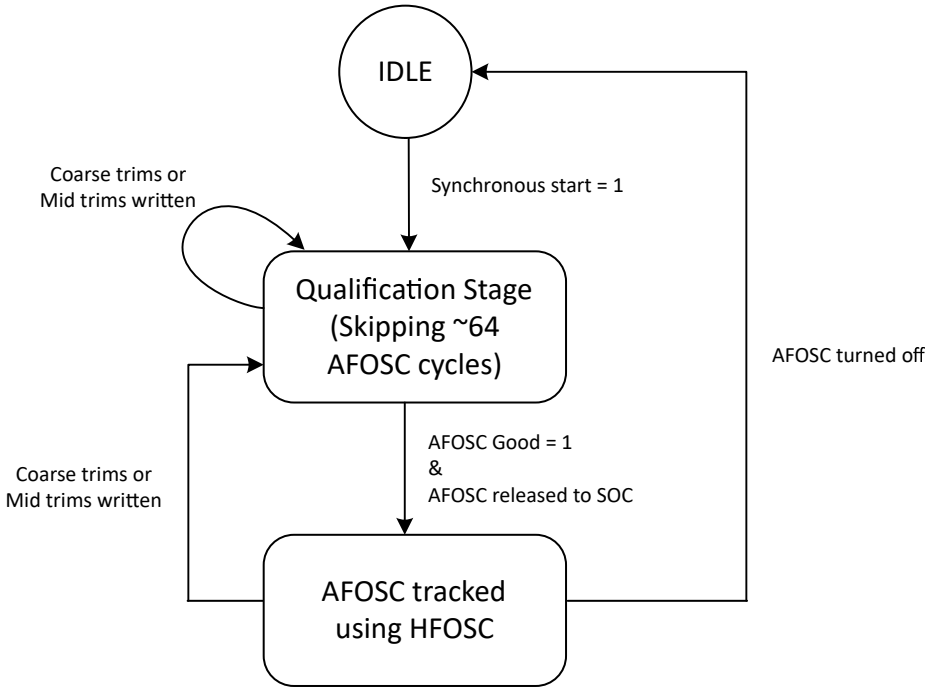

Figure 6-8. AFOSC qualification

1. Counter to skip a number of pulses when the clock might not be stable enough
   - Needs to be robust against unclean clock → ripple counter
   - Length hardcoded based on analog requirements
2. The AFOSC is enabled synchronously with CLK_ULL, using the MMR CKMD.AFOSCCTL.EN
3. For the AFOSC oscillator, we can change the COARSE and MID trims. Every time the trims are changed, the AFOSC clock is stopped and qualification is re-triggered.

6.6.4.2 AFOSC Tracking Loop

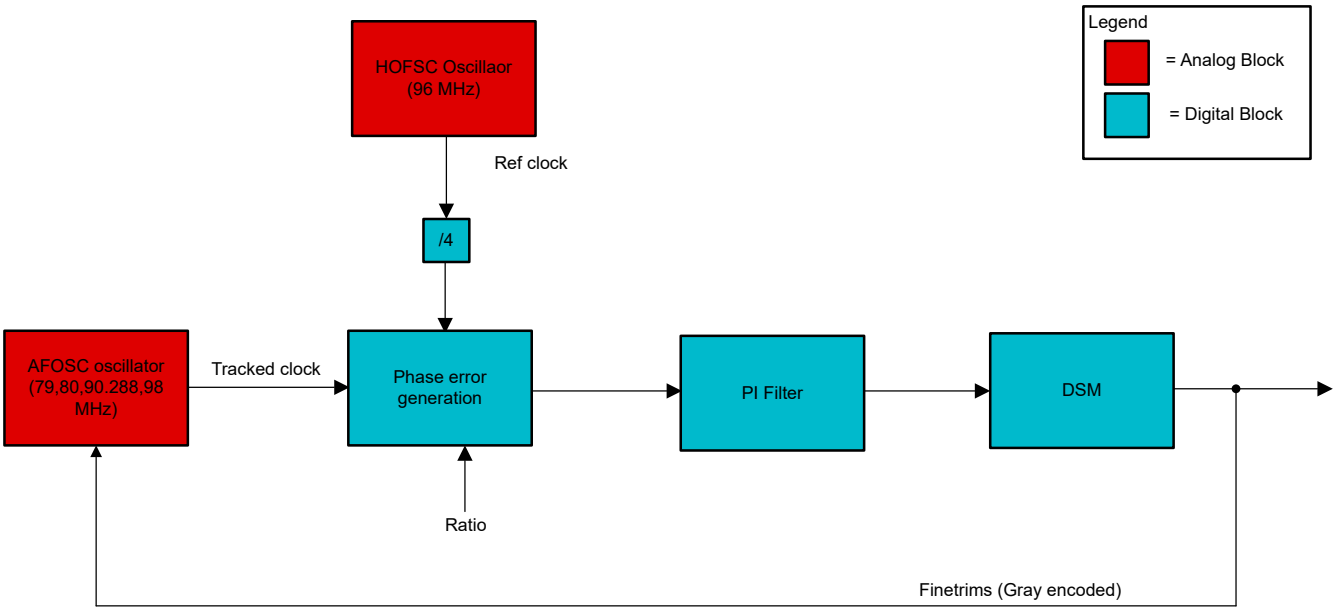

Figure 6-9. AFOSC Tracking Loop

1. AFOSC is indirectly tracked using HFOSC instead of HFXT

2. The Tracking loop ratio is adjusted using CKMD.HFTRACKCTL.RATIO MMR. The steps to compute the MMR values is mentioned in the AFOSC ratio section below.
3. The KI and KP value of the loop filter is adjusted using the MMR CKMD.LOOPCFGAF.
4. The filter is designed to achieve <100ppm in ~250us and ~10ppb in a couple of seconds.

6.6.4.3 AFOSC ratio

The AFOSC tracking loop ratio is stored in the MMR CKMD.AFTRACKCTL.RATIO. The ratio is of the format 2b.30b. i.e. there are 30 fractional bits.

There are 3 supported frequencies for AFOSC for which the ratio calculation has been shown. But the same can be extended to any other ratio.

- 80 MHz:

  CKMD.AFTRACKCTL.RATIO = [(ull_freq)/(2*AFOSC freq)] * 2^30 = [24/(2*80)]*2^30 = 0x0999999A
- 90.3168 MHz:

  CKMD.AFTRACKCTL.RATIO = [(ull_freq)/(2*AFOSC freq)] * 2^30 = [24/(2*90.3168)]*2^30 = 0x880DEE9
- 98.304 MHz:

  CKMD.AFTRACKCTL.RATIO = [(ull_freq)/(2*AFOSC freq)] * 2^30 = [24/(2*98.304)]*2^30 = 0x7D00000

6.6.5 CLKSVT

CLKSVT is a free running 96 MHz clock. Some CLKSVT peripherals run on 96 MHz and others on 48 MHz. Individual peripherals can be clock gated to reduce power consumption. Individual clock gating settings are configured in CLKCTL.

6.6.6 CLKULL

All AON modules receive a continuously running clock (CLKULL), which runs at 24 MHz when the CPU domain is powered (ACTIVE and IDLE power states) and runs at 32.768 kHz when the CPU domain is not powered (STANDBY power state).

6.6.7 CKM Registers

Table 6-38 lists the memory-mapped registers for the CKM registers. All register offset addresses not listed in Table 6-38 should be considered as reserved locations and the register contents should not be modified.

Table 6-38. CKM Registers

Offset	Acronym	Register Name	Section
0h	DESC	IP Description	Section 6.6.7.1
44h	IMASK	Interrupt mask. This register selects interrupt sources which are allowed to pass from [RIS.*] to [MIS.*] when the corresponding bit-fields are set to 1.	Section 6.6.7.2
48h	RIS	Raw interrupt flag register	Section 6.6.7.3
4Ch	MIS	Masked interrupt flag register	Section 6.6.7.4
50h	ISET	Interrupt flag set register	Section 6.6.7.5
54h	ICLR	Interrupt flag clear register	Section 6.6.7.6
58h	IMSET	Interrupt mask set register	Section 6.6.7.7
5Ch	IMCLR	Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding [IMASK.*] bit.	Section 6.6.7.8
80h	HFOSCCTL	High frequency oscillator control	Section 6.6.7.9
84h	HFXTCTL	High frequency crystal control	Section 6.6.7.10
8Ch	LFOSCCTL	Low frequency oscillator control	Section 6.6.7.11
90h	LFXTCTL	Low frequency crystal control	Section 6.6.7.12
94h	LFQUALCTL	Low frequency clock qualification control	Section 6.6.7.13
98h	LFINCCTL	Low frequency time increment control	Section 6.6.7.14
9Ch	LFINCOVR	Low frequency time increment override control	Section 6.6.7.15
A0h	AMPADCCTL	Amplitude ADC control	Section 6.6.7.16
A4h	HFTRACKCTL	High frequency tracking loop control	Section 6.6.7.17
A8h	LDOCTL	LDO control By default, the LDO is controlled by the HFXT Amplitude compensation. This register is used for software overrides.	Section 6.6.7.18
ACh	NABIASCTL	Nanoamp-bias control	Section 6.6.7.19
B0h	LFMONCTL	Low-frequency clock-monitor control	Section 6.6.7.20
B4h	LFINCCTL2	Low frequency time increment control-2	Section 6.6.7.21
C0h	LFCLKSEL	Low frequency clock selection	Section 6.6.7.22
C4h	TDCCLKSEL	TDC clock selection	Section 6.6.7.23
C8h	ADCCLKSEL	ADC clock selection	Section 6.6.7.24
E0h	LFCLKSTAT	Low-frequency clock status	Section 6.6.7.25
E4h	HFXTSTAT	HFXT status information	Section 6.6.7.26
E8h	AMPADCSTAT	HFXT Amplitude ADC Status	Section 6.6.7.27
ECh	TRACKSTAT	HF tracking loop status information	Section 6.6.7.28
F0h	AMPSTAT	HFXT Amplitude Compensation Status	Section 6.6.7.29
F4h	LFCLKSTAT2	Low-frequency clock status-2	Section 6.6.7.30
100h	ATBCTL0	Analog test bus controls All fields within this register are locked using the global-lock within SYS0.	Section 6.6.7.31
104h	ATBCTL1	Analog test bus controls All fields within this register are locked using the global-lock within SYS0.	Section 6.6.7.32
108h	DTBCTL	Digital test bus mux control	Section 6.6.7.33

Table 6-38. CKM Registers (continued)

Offset	Acronym	Register Name	Section
10Ch	DTBCTL2	Digital test bus mux control	Section 6.6.7.34
110h	TRIM0	Production Trim Register 0 Note: This register contains the HFOSC and AFOSC coarse trims. Changing it might result in frequency overshoots. To prevent these from reaching the system, the clock is gated off for some periods after writing this register.	Section 6.6.7.35
114h	TRIM1	Production Trim Register 1	Section 6.6.7.36
118h	HFXTINIT	Initial values for HFXT ramping	Section 6.6.7.37
11Ch	HFXTTARG	Target values for HFXT ramping	Section 6.6.7.38
120h	HFXTDYN	Alternative target values for HFXT configuration Software can change these values to dynamically transition the HFXT configuration while HFXT is running. Set [SEL] to select the alternative set of target values.	Section 6.6.7.39
124h	AMPCFG0	Amplitude Compensation Configuration 0	Section 6.6.7.40
128h	AMPCFG1	Amplitude Compensation Configuration 1	Section 6.6.7.41
12Ch	LOOPCFG	Configuration Register for the Tracking Loop	Section 6.6.7.42
130h	LOOPCFG1	Configuration Register for underclocking HFOSC	Section 6.6.7.43
140h	AFOSCCTL	Audio frequency oscillator control	Section 6.6.7.44
144h	AFTRACKCTL	Audio frequency tracking loop control	Section 6.6.7.45
148h	BANDGAPCTL	Configuration Register for the Tracking Loop	Section 6.6.7.46
150h	AFCLKSEL	Audio clock selection	Section 6.6.7.47
154h	CANCLKSEL	CAN clock selection	Section 6.6.7.48
160h	TRACKSTATAF	AF tracking loop status information	Section 6.6.7.49
164h	TRACKSTATAF1	AF tracking loop status information	Section 6.6.7.50
168h	TRACKSTATAF2	AF tracking loop status information	Section 6.6.7.51
170h	LOOPCFGAF	Configuration Register for the Audio frequency Tracking Loop	Section 6.6.7.52
200h	CTL	Control	Section 6.6.7.53
204h	STAT	Status	Section 6.6.7.54
208h	RESULT	Result Result of last **TDC** conversion.	Section 6.6.7.55
20Ch	SATCFG	Saturation Configuration	Section 6.6.7.56
210h	TRIGSRC	Trigger Source Select source and polarity for **TDC** start and stop events. See the Technical Reference Manual for event timing requirements.	Section 6.6.7.57
214h	TRIGCNT	Trigger Counter Stop-counter control and status.	Section 6.6.7.58
218h	TRIGCNTLOAD	Trigger Counter Load Stop-counter load.	Section 6.6.7.59
21Ch	TRIGCNTCFG	Trigger Counter Configuration Stop-counter configuration.	Section 6.6.7.60
220h	PRECTL	Prescaler Control The prescaler can be used to count events that are faster than the bus rate. It can be used to: - count pulses on a specified event from the asynchronous event bus. - prescale a specified event from the asynchronous event bus. To use the prescaler output as an event source in **TDC** measurements you must set both [TRIGSRC.START_SRC] and [TRIGSRC.STOP_SRC] to TDC_PRE. It is recommended to use the prescaler when the signal frequency to measure exceeds 1/10th of the bus rate.	Section 6.6.7.61

Table 6-38. CKM Registers (continued)

Offset	Acronym	Register Name	Section
224h	PRECNTR	Prescaler Counter	Section 6.6.7.62
300h	CNT	WDT counter value register	Section 6.6.7.63
304h	TEST	WDT test mode register	Section 6.6.7.64
308h	LOCK	WDT lock register	Section 6.6.7.65

Complex bit access types are encoded to fit into small table cells. Table 6-39 shows the codes that are used for access types in this section.

Table 6-39. CKM Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
WC	W C	Write to Clear
Reset or Default Value		
-n		Value after reset or the default value

6.6.7.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 6-40.

Return to the Summary Table.

IP Description

Table 6-40. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	0h	Module identifier
15-12	STDIPOFF	R	0h	Standard IP MMR block offset
11-8	RESERVED	R	0h	
7-4	MAJREV	R	0x0	Major revision
3-0	MINREV	R	0x0	Minor revision

6.6.7.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 6-41.

Return to the Summary Table.

Interrupt mask.
This register selects interrupt sources which are allowed to pass from [RIS.*] to [MIS.*] when the corresponding bit-fields are set to 1.

Table 6-41. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	R/W	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	R/W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	R/W	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	R/W	0h	AFOSC good indication.
18	TRACKREFAFOOR	R/W	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	R/W	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	R/W	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	R/W	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	R/W	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	R/W	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	R/W	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	R/W	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	R/W	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].

Table 6-41. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	LFINCUPD	R/W	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.
8	TDCDONE	R/W	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	R/W	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	R/W	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	R/W	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	R/W	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	R/W	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	R/W	0h	HFXT amplitude good indication.
1	HFXTFAULT	R/W	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	R/W	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 6-42.

Return to the Summary Table.

Raw interrupt flag register

Table 6-42. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	R	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	R	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	R	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	R	0h	AFOSC good indication.
18	TRACKREFAFOOR	R	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	R	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	R	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	R	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	R	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	R	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	R	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	R	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	R	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].
9	LFINCUPD	R	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.

Table 6-42. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TDCDONE	R	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	R	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	R	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	R	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	R	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	R	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	R	0h	HFXT amplitude good indication.
1	HFXTFAULT	R	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	R	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 6-43.

Return to the Summary Table.

Masked interrupt flag register

Table 6-43. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	R	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	R	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	R	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	R	0h	AFOSC good indication.
18	TRACKREFAFOOR	R	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	R	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	R	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	R	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	R	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	R	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	R	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	R	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	R	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].
9	LFINCUPD	R	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.

Table 6-43. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TDCDONE	R	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	R	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	R	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	R	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	R	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	R	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	R	0h	HFXT amplitude good indication.
1	HFXTFAULT	R	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	R	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 6-44.

Return to the Summary Table.

Interrupt flag set register

Table 6-44. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	W	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].
9	LFINCUPD	W	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.

Table 6-44. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TDCDONE	W	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 6-45.

Return to the Summary Table.

Interrupt flag clear register

Table 6-45. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	W	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].
9	LFINCUPD	W	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.

Table 6-45. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TDCDONE	W	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 6-46.

Return to the Summary Table.

Interrupt mask set register

Table 6-46. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	W	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].
9	LFINCUPD	W	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.

Table 6-46. IMSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TDCDONE	W	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 6-47.

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Interrupt mask clear register.
Writing a 1 to a bit in this register will clear the corresponding [IMASK.*] bit.

Table 6-47. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on SETTLED_TARGET
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than GEARRSTRTLIM
21	RESERVED	R	0h	
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop. Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT. Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart. Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state, and the controls configured in [HFXTTARG.*] or [HFXTDYN.*] are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target Indicates that the control values configured in [HFXTTARG.*] or [HFXTDYN.*] are reached. Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect. Indicates that a positive edge occured on the selected pre-LF clock [CLKSEL.PRELFCLK]' Can be used by software to confirm that a LF clock source is running and within the expected frequency, before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost. Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period). The system will automatically fall-back to generating LFTICK based on CLKULL, to avoid timing corruption. Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range. Indicates that a LF clock period was measured to be out-of-range, according to MAXERR.
10	LFCLKGOOD	W	0h	LF clock good. Indicates that the LF clock is good, according to the configuration in [LFQUALCTL.*].
9	LFINCUPD	W	0h	LFINC updated. Indicates that a new LFINC measurement value is available in LFINC.

Table 6-47. IMCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TDCDONE	W	0h	TDC done event. Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event. Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event. Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event. Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop. Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop. Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication. Indicates that HFXT did not start correctly, or its frequency is too low. HFXT will not recover from this fault and has to be restarted. This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication. Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation. This is only a one-time check at HFXT startup.

6.6.7.9 HFOSCCTL Register (Offset = 80h) [Reset = 00000000h]

HFOSCCTL is shown in Table 6-48.

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High frequency oscillator control

Table 6-48. HFOSCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PW	W	0h	Password protection for [QUALBYP] and FORCEOFF. Write this field to 0xA5 to accept writes to [QUALBYP] and FORCEOFF.
23-2	RESERVED	R	0h	
1	FORCEOFF	R/W	0x0	Force HFOSC off. Once this MMR is set, the system will stop. The only way to start the system again is system reset. This field is locked using the global-lock within SYS0.
0	QUALBYP	R/W	0x0	Clock qualification bypass. HFOSC qualification will skip a fixed number of clock cycles to prevent glitches or frequency overshoots from reaching the system. Setting this bit will bypass the qualification. This bit can be locked in SYS0. If unlocked, it is password protected with [PW].

6.6.7.10 HFXTCTL Register (Offset = 84h) [Reset = 00000000h]

HFXTCTL is shown in Table 6-49.

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High frequency crystal control

Table 6-49. HFXTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AMPOVR	R/W	0x0	Software override for the amplitude compensation FSM Directly use control values in [HFXTDYN.*]. Control injection and clock buffer using INJECT and LPBUFEN.
30-27	RESERVED	R	0h	
26	BIASEN	R/W	0x0	HFXT bias enable. Controls the biasing if AMPOVR is set. Otherwise, the biasing is controlled by the amplitude compensation FSM.
25	LPBUFEN	R/W	0x0	Low power clock buffer enable. Controls the clock buffer if AMPOVR is set. Otherwise, the buffer is controlled by the amplitude compensation FSM.
24	INJECT	R/W	0x0	Control HFXT injection if AMPOVR is set.
23	QUALBYP	R/W	0x0	Bypass HFXT clock qualification. Enables HFXT propagation to the system without waiting for the qualification circuit.
22-20	RESERVED	R	0h	
19-8	QUALDLY	R/W	0x0	Skip potentially unstable clock cycles after enabling HFXT. Number of cycles skipped is 8*QUALDLY.
7	TCXOMODE	R/W	0x0	Temperature compensated crystal oscillator mode. Set this bit if a TXCO is connected.
6	TCXOTYPE	R/W	0x0	Type of temperature compensated crystal used. Only has effect if TCXOMODE is set. 0h = Use with clipped-sine TCXO 1h = Use with CMOS TCXO
5-3	RESERVED	R	0h	
2	AUTOEN	R/W	0x0	Automatic HFXT enable. If this bit is set, [EN] will automatically be set at wakeup or before (using pre-wake mechanism in PMCTL).
1	HPBUFEN	R/W	0x0	High performance clock buffer enable. This bit controls the clock output for the RF PLL. It is required for radio operation.
0	EN	RH/W	0x0	HFXT enable. Setting this bit will enable HFXT. It will automatically be cleared upon STANDBY entry. If AUTOEN is set, this bit will be set automatically on wakeup or before (pre-wake mechanism in PMCTL).

6.6.7.11 LFOSCCTL Register (Offset = 8Ch) [Reset = 00000000h]

LFOSCCTL is shown in Table 6-50.

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Low frequency oscillator control

Table 6-50. LFOSCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	EN	R/W	0x0	LFOSC enable

6.6.7.12 LFXTCTL Register (Offset = 90h) [Reset = 00000000h]

LFXTCTL is shown in Table 6-51.

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Low frequency crystal control

Table 6-51. LFXTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	
14-13	LEAKCOMP	R/W	0x0	Leakage compensation control 0h = Full leakage compensation 1h = Half leakage compensation 3h = No leakage compensation
12	BUFBIAS	R/W	0x0	Control the BIAS current of the input amp in LP buffer 0h = Minimum bias current: 25nA 1h = Maximum bias current: 50nA
11-8	AMPBIAS	R/W	0x0	Adjust current mirror ratio into oscillator core. This value is depending on crystal and is set by FW. This field uses a 2's complement encoding.
7-6	BIASBOOST	R/W	0x0	Boost oscillator amplitude This value depends on the crystal and needs to be configured by Firmware.
5-4	REGBIAS	R/W	0x0	Regulation loop bias resistor value This value depends on the crystal and needs to be configured by Firmware.
3	RESERVED	R	0h	
2	HPBUFEN	R/W	0x0	Control the buffer used. In normal operation, low-power buffer is used in all device modes. The high-performance buffer is only used for test purposes.
1	AMPREGMODE	R/W	0x0	Amplitude regulation mode 0h = Amplitude control loop enabled 1h = Amplitude control loop disabled
0	EN	R/W	0x0	LFXT enable

6.6.7.13 LFQUALCTL Register (Offset = 94h) [Reset = 00000000h]

LFQUALCTL is shown in Table 6-52.

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Low frequency clock qualification control

Table 6-52. LFQUALCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	
13-8	MAXERR	R/W	0h	Maximum LFCLK period error. Value given in microseconds, 3 integer bits + 3 fractional bits.
7-0	CONSEC	R/W	0h	Number of consecutive times the LFCLK period error has to be smaller than MAXERR to be considered 'good'. Setting this value to 0 will bypass clock qualification, and the 'good' indicator will always be 1.

6.6.7.14 LFINCCTL Register (Offset = 98h) [Reset = 00000000h]

LFINCCTL is shown in Table 6-53.

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Low frequency time increment control

Table 6-53. LFINCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PREVENTSTBY	R/W	0h	Controls if the LFINC filter prevents STANBY entry until settled. 0h = Disable. Do not prevent STANDBY entry. 1h = Enable. Prevent STANDBY entry.
30	KEEPHFXTEN	R/W	0x0	Keeps the HFXT enabled till the LFINC filter settles 0h = Disable. Do not keep HFXT enabled. 1h = Enable. Keep HFXT enabled.
29-8	INT	RH/W	0h	Integral part of the LFINC filter. This value is updated by Hardware to reflect the current state of the filter. It can also be written to change the current state.
7	STOPGEAR	R/W	0x0	Controls the final gear of the LFINC filter. 0h = Lowest final gear. Best settling, but less dynamic frequency tracking. 1h = Highest final gear. Best dynamic frequency tracking, but higher variation in filter value.
6-5	ERRTHR	R/W	0x0	Controls the threshold for gearing restart of the LFINC filter. Only effective if GEARRSTRT is not ONETHR or TWOTHR. 0h = Restart gearing on large error. Fewer false restarts, slower response on small frequency shifts. 1h = Middle value towards LARGE. 2h = Middle value towards SMALL. 3h = Restart gearing on small error. Potentially more false restarts, faster response on small frequency shifts.
4-3	GEARRSTRT	R/W	0h	Controls gearing restart of the LFINC filter. 0h = Never restart gearing. Very stable filter value, but very slow response on frequency changes. 1h = Restart gearing when the error accumulator crosses the threshold once. 2h = Restart gearing when the error accumulator crosses the threshold twice in a row.
2	SOFTRSTRT	R/W	0h	Use a higher gear after re-enabling / wakeup. The filter will require 16-24 LFCLK periods to settle (depending on STOPGEAR), but may respond faster to frequency changes during STANDBY. 0h = Don't use soft gearing restarts 1h = Use soft gearing restarts
1-0	EN	R/W	0h	Enable LFINC filter. Programming with a value of 0x3 will disable the LFINC filter 0h = DISABLED 1h = ENABLED 2h = Enable based on HFOS getting settled. HFOSC gets settled after the tracking loop has updated equal to or more than SETTLED_TARGET times.

6.6.7.15 LFINCOVR Register (Offset = 9Ch) [Reset = 00000000h]

LFINCOVR is shown in Table 6-54.

Return to the Summary Table.

Low frequency time increment override control

Table 6-54. LFINCOVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVERRIDE	R/W	0x0	Override LF increment Use the value provided in [LFINC] instead of the value calculated by Hardware.
30-22	RESERVED	R	0h	
21-0	LFINC	R/W	0x0	LF increment value This value is used when OVERRIDE is set to 1. Otherwise the value is calculated automatically. The current LFINC value can be read from LFINC.

6.6.7.16 AMPADCCTL Register (Offset = A0h) [Reset = 00000000h]

AMPADCCTL is shown in Table 6-55.

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Amplitude ADC control

Table 6-55. AMPADCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SWOVR	R/W	0x0	Software override. Control Amplitude ADC from software
30-18	RESERVED	R	0h	
17	PEAKDETEN	R/W	0x0	Enable HFXT Peak Detector. If the peak detector is used by the AMPCOMP FSM, this bit can be used to keep the peak detector always enabled. If [SWOVR] is set, this bit directly controls the peak detector. 0h = Disable peak detector (unless requested by AMPCOMP FSM) 1h = Enable peak detector
16	ADCEN	R/W	0x0	Enable Amplitude ADC. If the ADC is used by the AMPCOMP FSM, this bit can be used to keep the ADC always enabled. If [SWOVR] is set, this bit directly controls the ADC. 0h = Disable ADC (unless requested by AMPCOMP FSM) 1h = Enable ADC
15	RESERVED	R	0h	
14-8	COMPVAL	R/W	0x0	Comparator reference input in compare mode This bitfield is only active if [SWOVR] is set. SRCSEL selects the source to be compared. Result will be available in COMPOUT.
7-5	RESERVED	R	0h	
4	SRCSEL	R/W	0x0	Select the input to the ADC Only active if [SWOVR] is set. 0h = Measure bias voltage 1h = Measure HFXT peak voltage
3-2	RESERVED	R	0h	
1	COMPSTRT	R/W	0x0	Start a comparison This bit is only active if [SWOVR] is set. SRCSEL selects the source to be measured. COMPVAL configures the threshold value. Result will be available in COMPOUT.
0	SARSTRT	R/W	0x0	Start a SAR conversion This bit is only active if [SWOVR] is set. SRCSEL selects the source to be measured. Result will be available in [AMPADCSTAT.*].

6.6.7.17 HFTRACKCTL Register (Offset = A4h) [Reset = 00000000h]

HFTRACKCTL is shown in Table 6-56.

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High frequency tracking loop control

Table 6-56. HFTRACKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0x0	Enable tracking loop.
30	DSMBYP	R/W	0x0	Bypass Delta-Sigma-Modulation of fine trim.
29-28	UNDERCLK	R/W	0x0	When the HFOSC tracking loop is not running, this bitfield can be used to set the condition to automatically lower the HFOSC frequency. This will prevent frequency drift that may lead to SOC instability. 0h = Disable 1h = Timer event 2h = Temperature event from Batmon 3h = Temperature event from Batmon or Timer event
27-26	REFCLK	R/W	0x0	Select the reference clock for the tracking loop. Change only while the tracking loop is disabled. 0h = Select HFXT as reference clock. 1h = Select LRF reference clock. 2h = Select GPI as reference clock.
25-0	RATIO	R/W	0h	Reference clock ratio. Ratio format is 2b.24b [RATIO] = 24MHz / (2*reference-frequency) * 2^{24} Commonly used reference clock frequencies are provided as enumerations.

6.6.7.18 LDOCTL Register (Offset = A8h) [Reset = 00000000h]

LDOCTL is shown in Table 6-57.

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LDO control
By default, the LDO is controlled by the HFXT Amplitude compensation.
This register is used for software overrides.

Table 6-57. LDOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SWOVR	R/W	0x0	Software override. Control LDO from software
30-5	RESERVED	R	0h	
4	HFXTLVLEN	R/W	0x0	Enable levelshifters from ULL to VCKM. Needs to be timer-based. Worst-case LDO startup time is 5us across PVT.
3	STARTCTL	R/W	0x0	Enable faster startup. This bit should be set together with [EN], and cleared after 5us.
2	START	R/W	0x0	Enable faster startup. This bit should be set together with [EN], and cleared after 5us.
1	BYPASS	R/W	0x0	Bypass LDO
0	EN	R/W	0x0	Enable LDO

6.6.7.19 NABIASCTL Register (Offset = ACh) [Reset = 00000000h]

NABIASCTL is shown in Table 6-58.

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Nanoamp-bias control

Table 6-58. NABIASCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	EN	R/W	0x0	Enable nanoamp-bias

6.6.7.20 LFMONCTL Register (Offset = B0h) [Reset = 00000000h]

LFMONCTL is shown in Table 6-59.

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Low-frequency clock-monitor control

Table 6-59. LFMONCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	EN	R/W	0x0	Enable LFMONITOR. Enable only after a LF clock source has been selected, enabled and is stable. If LFMONITOR detects a clock loss, the system will be reset.

6.6.7.21 LFINCCTL2 Register (Offset = B4h) [Reset = 00000000h]

LFINCCTL2 is shown in Table 6-60.

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Low frequency time increment control-2

Table 6-60. LFINCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ADJUSTLFINC	R/W	0h	Adjusts LFINC while transitioning from fake to real LF clock if necessary. For the adjustment to happen, tracking loop must be running.
30-10	RESERVED	R	0h	
9-4	GEARRSTRTLIM	R/W	0x0	Specifies the number of times gear could be restarted before raising an interrupt. It has no impact on the number of times gear can be reduced. A value of 0 indicates that the interrupt mechanism is disabled
3-0	GEARREDCNT	R/W	0h	Specifies the number by which gear should be reduced post standby exit

6.6.7.22 LFCLKSEL Register (Offset = C0h) [Reset = 00000000h]

LFCLKSEL is shown in Table 6-61.

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Low frequency clock selection

Table 6-61. LFCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3-2	PRE	R/W	0x0	Select low frequency clock source for the PRELFCLK interrupt. Can be used by Software to confirm that the clock is running and it's frequency is good, before selecting it in MAIN. 0h = No clock. Output will be tied low. 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = External LF clock through GPI.
1-0	MAIN	R/W	0x0	Select the main low frequency clock source. If running, this clock will be used to generate LFTICK and as CLKULL during STANDBY. If not running, LFTICK will be generated from HFOSC and STANDBY entry will be prevented. 0h = No LF clock selected. LFTICK will be generated from HFOSC, STANDBY entry will be prevented. 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = External LF clock through GPI.

6.6.7.23 TDCCLKSEL Register (Offset = C4h) [Reset = 00000000h]

TDCCLKSEL is shown in Table 6-62.

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TDC clock selection

Table 6-62. TDCCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2-0	REFCLK	R/W	0x0	Select reference clock for the TDC. 0h = No reference clock 1h = 96MHz HFOSC clock div by 2 2h = 24MHz CLKULL 3h = General purpose input signal 4h = AFOSC clock div by 2 5h = 48MHz HFXT

6.6.7.24 ADCCLKSEL Register (Offset = C8h) [Reset = 00000000h]

ADCCLKSEL is shown in Table 6-63.

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ADC clock selection

Table 6-63. ADCCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	SRC	R/W	0x0	Select ADC clock source Change only while ADC is disabled! 0h = 48MHz CLKSVT 1h = 48MHz HFXT

6.6.7.25 LFCLKSTAT Register (Offset = E0h) [Reset = 00000000h]

LFCLKSTAT is shown in Table 6-64.

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Low-frequency clock status

Table 6-64. LFCLKSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GOOD	R	0h	Low frequency clock good Note: This is only a coarse frequency check based on [LFQUALCTL.*]. The clock may not be accurate enough for timing purposes.
30-26	RESERVED	R	0h	
25	FLTSETTLED	R	0h	LFINC filter is running and settled.
24	LFTICKSRC	R	0h	Source of LFTICK. 0h = LFTICK generated from the selected LFCLK 1h = LFTICK generated from CLKULL (LFCLK not available)
23-22	LFINCSRC	R	0h	Source of LFINC used by the RTC. This value depends on OVERRIDE, LF clock availability, HF tracking loop status and the device state (ACTIVE/STANDBY). 0h = Using measured value. This value is updated by hardware and can be read from [LFINC]. 1h = Using filtered / average value. This value is updated by hardware and can be read and updated in INT. 2h = Using override value from LFINC 3h = Using FAKE LFTICKs with corresponding LFINC value.
21-0	LFINC	R	0h	Measured value of LFINC. Given in microseconds with 16 fractional bits. This value is calculated by Hardware. It is the LFCLK period according to CLKULL cycles.

6.6.7.26 HFXTSTAT Register (Offset = E4h) [Reset = 00000000h]

HFXTSTAT is shown in Table 6-65.

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HFXT status information

Table 6-65. HFXTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	
30-16	STARTUPTIME	R	0x0	HFXT startup time Can be used by software to plan starting HFXT ahead in time. Measured whenever HFXT is enabled in CLKULL periods (24MHz), from EN until the clock is good for radio operation (amplitude compensation is settled).
15-2	RESERVED	R	0h	
1	FAULT	R	0x0	HFXT clock fault Indicates a lower than expected HFXT frequency. HFXT will not recover from this fault, disabling and re-enabling HFXT is required.
0	GOOD	R	0x0	HFXT clock available. The frequency is not necessarily good enough for radio operation.

6.6.7.27 AMPADCSTAT Register (Offset = E8h) [Reset = 00000000h]

AMPADCSTAT is shown in Table 6-66.

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HFXT Amplitude ADC Status

Table 6-66. AMPADCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	COMPOUT	R	0x0	Most recent comparison output
23	RESERVED	R	0h	
22-16	PEAKRAW	R	0x0	Most recently measured peak voltage - raw This value is the raw output of the HFXT ADC. For the actual peak voltage use the value (PEAK + 0.0150)/0.74 + K, where 'K' is a function of process variation and is stored in FCFG1 register.
15-8	PEAK	R	0x0	Most recently measured peak voltage - bias corrected This value is computed as 2*PEAKRAW-BIAS Actual voltage = (2*PEAKRAW-BIAS - 0.015)/0.74 + K, where 'K' is a function of process variation and is stored in FCFG1 register.
7	RESERVED	R	0h	
6-0	BIAS	R	0x0	Most recently measured bias voltage

6.6.7.28 TRACKSTAT Register (Offset = ECh) [Reset = 00000000h]

TRACKSTAT is shown in Table 6-67.

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HF tracking loop status information

Table 6-67. TRACKSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOOPERRVLD	R	0x0	Current HFOSC tracking error valid This bit is one if the tracking loop is running and the error value is valid.
30	RESERVED	R	0h	
29-16	LOOPERR	R	0x0	Current HFOSC tracking error This field uses the internal fractional representation (sign, 9 integer bits, 4 fractional bits).
15-13	RESERVED	R	0h	
12-0	FINETRIM	R	0h	Current HFOSC Fine-trim value This field uses the internal fractional representation (sign, 5 integer bits, 7 fractional bits). The actual trim value applied to the oscillator is delta-sigma modulated 6 bits non-signed (inverted sign bit + integer bits). INTERNAL_NOTE: This field can be written by also writing a magic value (0xA5) into LOOPERR (bits 23:16)

6.6.7.29 AMPSTAT Register (Offset = F0h) [Reset = 00000000h]

AMPSTAT is shown in Table 6-68.

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HFXT Amplitude Compensation Status

Table 6-68. AMPSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28-25	STATE	R	0x0	Current AMPCOMP FSM state. 0h = FSM in idle state 1h = Starting LDO 2h = Second shutdown state 3h = Injecting HFOSC for fast startup 4h = Transition to [HFXTTARG.*] values 5h = Initial amplitude ramping with [HFXTINIT.*] values 6h = Amplitude down correction 7h = Post injection settle wait Ah = First shutdown state Ch = TCXO settled state Eh = Amplitude up correction Fh = Settled state
24-18	IDAC	R	0x0	Current IDAC control value.
17-14	IREF	R	0x0	Current IREF control value.
13-8	Q2CAP	R	0x0	Current Q2CAP control value.
7-2	Q1CAP	R	0x0	Current Q1CAP control value.
1	CTRLATTARGET	R	0x0	HFXT control values match target values. This applies to IREF, Q1CAP, Q2CAP values.
0	AMPGOOD	R	0x0	HFXT amplitude good

6.6.7.30 LFCLKSTAT2 Register (Offset = F4h) [Reset = 00000000h]

LFCLKSTAT2 is shown in Table 6-69.

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Low-frequency clock status-2

Table 6-69. LFCLKSTAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	
6-4	SUBGEAR	R	0x0	The value of sub gear in LF filter
3-0	MAINGEAR	R	0x0	The value of main gear in LF filter

6.6.7.31 ATBCTL0 Register (Offset = 100h) [Reset = 00000000h]

ATBCTL0 is shown in Table 6-70.

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Analog test bus controls
All fields within this register are locked using the global-lock within SYS0.

Table 6-70. ATBCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23-0	SEL	R/W	0x0	Testmux selection ALWAYS write this signal to 0 (OFF), before selecting another configuration! Not following this might result in device damage. 00000000h = No signal connected to ATB. All outputs high impedant 00000001h = vr_atb_hfxt_ana connected to vr_atb_ckmanatop_ana 00000002h = vr_atb_ckmldo_vddckm connected to vr_atb_ckmanatop_ana 00000008h = vr_atb_lfxt_ana connected to vr_atb_ckmanatop_ana 00000010h = vr_atb_hfxtadc_compout connected to vr_atb_ckmanatop_ana 00000020h = vr_atb_hfxtadc_compin connected to vr_atb_ckmanatop_ana 00000040h = vr_atb_hfxtadc_dacout connected to vr_atb_ckmanatop_ana 00000080h = vr_atb_nabias_itest_250n_dn connected to vr_atb_ckmanatop_ana 00000100h = vr_atb_hfosc_out connected to vr_atb_ckmanatop_ana 00001000h = vr_atb_lfmonitor_vtest connected to vr_atb_ckmanatop_ana 00004000h = vr_atb_afosc connected to vr_atb_ckmanatop_ana 00010000h = ull_ckm_hfosc_testclk connected to vr_atb_ckmanatop_clk 00030000h = ull_ckm_hfxt_testclk connected to vr_atb_ckmanatop_clk 00050000h = ull_ckm_lfosc_testclk connected to vr_atb_ckmanatop_clk 00070000h = ull_ckm_lfxt_testclk connected to vr_atb_ckmanatop_clk 00090000h = ull_ckm_afosc_testclk connected to vr_atb_ckmanatop_clk

6.6.7.32 ATBCTL1 Register (Offset = 104h) [Reset = 00000000h]

ATBCTL1 is shown in Table 6-71.

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Analog test bus controls
All fields within this register are locked using the global-lock within SYS0.

Table 6-71. ATBCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	
18	BGAP	R/W	0x0	Control bandgap test output signals
17-15	AFOSC	R/W	0x0	Control AFOSC test output signals
14-13	LFOSC	R/W	0x0	Control LFOSC test output signals 0h = No output signal selected 1h = LFOSC test clock 2h = LFOSC VDD LOCAL 3h = Both LFOSC test signals (TESTCLK, VDD LOCAL)
12	NABIAS	R/W	0x0	Enable NABIAS test mode.
11	RESERVED	R	0h	
10	LFXT	R/W	0x0	Control LFXT test output signals 0h = No output signal selected 1h = LFXT test clock
9-8	LFMON	R/W	0x0	Control LFMON test output signals 0h = No output signal selected 1h = Test signal 1 / in phase with LF clock 2h = Test signal 2 / in phase with inverted clock signal
7	HFXT	R/W	0x0	Enable HFXT test mode.
6-3	RESERVED	R	0h	
2-0	HFOSC	R/W	0x0	Enable HFOSC test clock output.

6.6.7.33 DTBCTL Register (Offset = 108h) [Reset = 00000000h]

DTBCTL is shown in Table 6-72.

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Digital test bus mux control

Table 6-72. DTBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	
22-18	DSEL2	R/W	0x0	Select data to output on DTB[15:11]
17-13	DSEL1	R/W	0x0	Select data to output on DTB[10:6]
12-8	DSEL0	R/W	0x0	Select data to output on DTB[5:1]
7-3	CLKSEL	R/W	0x0	Select clock to output on DTB[0] 0h = Select CLKULL (24 MHz during ACTIVE, 32kHz during STANDBY) 1h = Select CLKSVT (48 MHz) 2h = Select CLKADC (48 MHz) 3h = Select internal 24 MHz clock 4h = Select tracking loop reference clock 5h = Select TDC reference clock 6h = Select AMPCOMP FSM clock 7h = Select LFCLK (selected by MAIN) 8h = Select delayed version of LFCLK 9h = Select HFCLOCK before qualification Ah = Select HFOSC after qualification Bh = Select HFXT before qualification Ch = Select HFXT divided by 8 Dh = Select HFXT Eh = Select LFOSC Fh = Select LFXT 10h = Select AFCLOCK before qualification 11h = Select AFOSC after qualification 12h = HFOSC div by 2 clock
2-1	RESERVED	R	0h	
0	EN	R/W	0x0	Enable DTB output

6.6.7.34 DTBCTL2 Register (Offset = 10Ch) [Reset = 00000000h]

DTBCTL2 is shown in Table 6-73.

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Digital test bus mux control

Table 6-73. DTBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	
13-10	CLK2DTBSEL	R/W	0x0	Select a DTB other than DTB0 to route the clock. Value of 0 indicates that clock 2 won't be sent to DTB.
9-8	RESERVED	R	0h	
7-5	CLKSEL2	R/W	0x0	Select the clock that needs to be routed to a DTB other than DTB0 0h = Select CLKULL (24 MHz during ACTIVE, 32kHz during STANDBY) 1h = Select CLKSVT (48 MHz) 2h = Select delayed version of LFCLK 3h = Select HFXT before qualification 4h = Select AFCLOCK before qualification
4-3	RESERVED	R	0h	
2-1	CLK2DIVVAL	R/W	0x0	These bits are used to configure the divider value. 0h = Divide by 2 1h = Divide by 4 2h = Divide by 8 3h = Divide by 16
0	CLK2DIVEN	R/W	0x0	Enable divider on second clock path 0h = Disable 1h = Enable

6.6.7.35 TRIM0 Register (Offset = 110h) [Reset = 00000000h]

TRIM0 is shown in Table 6-74.

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Production Trim Register 0
Note: This register contains the HFOSC and AFOSC coarse trims.
Changing it might result in frequency overshoots.
To prevent these from reaching the system, the clock is gated off for some periods after writing this register.

Table 6-74. TRIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	
25	AFOSC_MODE	R/W	0x0	AFOSC mode trim
24-21	AFOSC_MID	R/W	0x0	AFOSC mid trim
20-16	AFOSC_COARSE	R/W	0x0	AFOSC coarse trim
15-10	RESERVED	R	0h	
9	HFOSC_MODE	R/W	0x0	HFOSC mode trim This field is locked using the global-lock within SYS0.
8-5	HFOSC_MID	R/W	0x0	HFOSC mid trim This field is locked using the global-lock within SYS0.
4-0	HFOSC_COARSE	R/W	0x0	HFOSC coarse trim This field is locked using the global-lock within SYS0.

6.6.7.36 TRIM1 Register (Offset = 114h) [Reset = 00000000h]

TRIM1 is shown in Table 6-75.

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Production Trim Register 1

Table 6-75. TRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	HFXTSLICER	R/W	0x0	Bias current trim for HFXT slicer.
29-28	PEAKIBIAS	R/W	0x0	IBIAS value for the HFXT peak detector
27	NABIAS_UDIGLDO	R/W	0h	Decrease uDIGLDO reference current by 25nA
26-24	LDOBW	R/W	0x0	HFXT LDO bandwidth trim
23-20	LDOFB	R/W	0h	HFXT LDO feedback trim
19-16	LFDLY	R/W	0h	LF delay cell trim
15	NABIAS_LFOSC	R/W	0h	Increase LFOSC reference current by 25nA
14-8	NABIAS_RES	R/W	0h	NABIAS resistor trim
7-0	LFOSC_CAP	R/W	0h	LFOSC cap trim. Note:- It's changing resistor inside LFOC, and not capacitor.

6.6.7.37 HFXTINIT Register (Offset = 118h) [Reset = 00000000h]

HFXTINIT is shown in Table 6-76.

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Initial values for HFXT ramping

Table 6-76. HFXTINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	
29-23	AMPTHR	R/W	0h	Amplitude threshold during HFXT ramping
22-16	IDAC	R/W	0h	Initial HFXT IDAC current
15-12	IREF	R/W	0h	Initial HFXT IREF current

Table 6-76. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	Q2CAP	R/W	0x0	Initial HFXT Q2 cap trim 0h = Nominal 25C = 2.57E-12 F Stong 25C = 1.50E-12 F Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F Stong 25C = 1.60E-12 F Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F Stong 25C = 1.69E-12 F Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F Stong 25C = 1.79E-12 F Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F Stong 25C = 1.89E-12 F Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F Stong 25C = 1.99E-12 F Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F Stong 25C = 2.09E-12 F Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F Stong 25C = 2.19E-12 F Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F Stong 25C = 2.29E-12 F Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F Stong 25C = 2.39E-12 F Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F Stong 25C = 2.49E-12 F Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F Stong 25C = 2.59E-12 F Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F Stong 25C = 2.69E-12 F Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F Stong 25C = 2.79E-12 F Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F Stong 25C = 2.89E-12 F Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F Stong 25C = 3.11E-12 F Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F Stong 25C = 3.23E-12 F Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F Stong 25C = 3.36E-12 F Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F Stong 25C = 3.48E-12 F Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F

Table 6-76. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Stong 25C = 3.60E-12 F Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F Stong 25C = 3.73E-12 F Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F Stong 25C = 3.85E-12 F Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F Stong 25C = 3.97E-12 F Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F Stong 25C = 4.09E-12 F Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F Stong 25C = 4.21E-12 F Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F Stong 25C = 4.32E-12 F Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F Stong 25C = 4.44E-12 F Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F Stong 25C = 4.56E-12 F Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F Stong 25C = 4.67E-12 F Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F Stong 25C = 4.79E-12 F Weak 25C = 6.12E-12 F 20h = Nominal 25C = 5.97E-12 F Stong 25C = 5.05E-12 F Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F Stong 25C = 5.20E-12 F Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F Stong 25C = 5.35E-12 F Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F Stong 25C = 5.49E-12 F Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F Stong 25C = 5.63E-12 F Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F Stong 25C = 5.78E-12 F Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F Stong 25C = 5.92E-12 F Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F Stong 25C = 6.06E-12 F Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F Stong 25C = 6.21E-12 F Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F Stong 25C = 6.35E-12 F Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F Stong 25C = 6.49E-12 F Weak 25C = 7.98E-12 F

Table 6-76. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Bh = Nominal 25C = 7.55E-12 F Stong 25C = 6.63E-12 F Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F Stong 25C = 6.77E-12 F Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F Stong 25C = 6.91E-12 F Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F Stong 25C = 7.05E-12 F Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F Stong 25C = 7.38E-12 F Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F Stong 25C = 7.57E-12 F Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F Stong 25C = 7.76E-12 F Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F Stong 25C = 7.94E-12 F Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F Stong 25C = 8.13E-12 F Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F Stong 25C = 8.32E-12 F Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F Stong 25C = 8.51E-12 F Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F Stong 25C = 8.70E-12 F Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F Stong 25C = 8.89E-12 F Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F Stong 25C = 9.07E-12 F Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F Stong 25C = 9.26E-12 F Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F Stong 25C = 9.45E-12 F Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F Stong 25C = 9.64E-12 F Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F Stong 25C = 9.82E-12 F Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F Stong 25C = 1.00E-11 F Weak 25C = 1.19E-11 F

Table 6-76. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Q1CAP	R/W	0x0	Initial HFXT Q1 cap trim 0h = Nominal 25C = 2.57E-12 F Stong 25C = 1.50E-12 F Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F Stong 25C = 1.60E-12 F Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F Stong 25C = 1.69E-12 F Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F Stong 25C = 1.79E-12 F Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F Stong 25C = 1.89E-12 F Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F Stong 25C = 1.99E-12 F Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F Stong 25C = 2.09E-12 F Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F Stong 25C = 2.19E-12 F Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F Stong 25C = 2.29E-12 F Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F Stong 25C = 2.39E-12 F Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F Stong 25C = 2.49E-12 F Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F Stong 25C = 2.59E-12 F Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F Stong 25C = 2.69E-12 F Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F Stong 25C = 2.79E-12 F Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F Stong 25C = 2.89E-12 F Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F Stong 25C = 3.11E-12 F Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F Stong 25C = 3.23E-12 F Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F Stong 25C = 3.36E-12 F Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F Stong 25C = 3.48E-12 F Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F

Table 6-76. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Stong 25C = 3.60E-12 F Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F Stong 25C = 3.73E-12 F Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F Stong 25C = 3.85E-12 F Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F Stong 25C = 3.97E-12 F Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F Stong 25C = 4.09E-12 F Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F Stong 25C = 4.21E-12 F Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F Stong 25C = 4.32E-12 F Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F Stong 25C = 4.44E-12 F Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F Stong 25C = 4.56E-12 F Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F Stong 25C = 4.67E-12 F Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F Stong 25C = 4.79E-12 F Weak 25C = 6.12E-12 F 20h = Nominal 25C = 5.97E-12 F Stong 25C = 5.05E-12 F Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F Stong 25C = 5.20E-12 F Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F Stong 25C = 5.35E-12 F Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F Stong 25C = 5.49E-12 F Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F Stong 25C = 5.63E-12 F Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F Stong 25C = 5.78E-12 F Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F Stong 25C = 5.92E-12 F Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F Stong 25C = 6.06E-12 F Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F Stong 25C = 6.21E-12 F Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F Stong 25C = 6.35E-12 F Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F Stong 25C = 6.49E-12 F Weak 25C = 7.98E-12 F

Table 6-76. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Bh = Nominal 25C = 7.55E-12 F Stong 25C = 6.63E-12 F Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F Stong 25C = 6.77E-12 F Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F Stong 25C = 6.91E-12 F Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F Stong 25C = 7.05E-12 F Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F Stong 25C = 7.38E-12 F Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F Stong 25C = 7.57E-12 F Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F Stong 25C = 7.76E-12 F Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F Stong 25C = 7.94E-12 F Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F Stong 25C = 8.13E-12 F Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F Stong 25C = 8.32E-12 F Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F Stong 25C = 8.51E-12 F Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F Stong 25C = 8.70E-12 F Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F Stong 25C = 8.89E-12 F Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F Stong 25C = 9.07E-12 F Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F Stong 25C = 9.26E-12 F Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F Stong 25C = 9.45E-12 F Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F Stong 25C = 9.64E-12 F Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F Stong 25C = 9.82E-12 F Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F Stong 25C = 1.00E-11 F Weak 25C = 1.19E-11 F

6.6.7.38 HFXTTARG Register (Offset = 11Ch) [Reset = 00000000h]

HFXTTARG is shown in Table 6-77.

Return to the Summary Table.

Target values for HFXT ramping

Table 6-77. HFXTTARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	AMPHYST	R/W	0h	ADC hysteresis used during IDAC updates. Every INTERVAL, IDAC will be regulated - up as long as ADC < [AMPTHR] - down as long as ADC > [AMPTHR]+AMPHYST
29-23	AMPTHR	R/W	0h	Minimum HFXT amplitude
22-16	IDAC	R/W	0h	Minimum IDAC current
15-12	IREF	R/W	0h	Target HFXT IREF current

Table 6-77. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	Q2CAP	R/W	0h	Target HFXT Q2 cap trim 0h = Nominal 25C = 2.57E-12 F Stong 25C = 1.50E-12 F Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F Stong 25C = 1.60E-12 F Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F Stong 25C = 1.69E-12 F Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F Stong 25C = 1.79E-12 F Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F Stong 25C = 1.89E-12 F Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F Stong 25C = 1.99E-12 F Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F Stong 25C = 2.09E-12 F Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F Stong 25C = 2.19E-12 F Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F Stong 25C = 2.29E-12 F Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F Stong 25C = 2.39E-12 F Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F Stong 25C = 2.49E-12 F Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F Stong 25C = 2.59E-12 F Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F Stong 25C = 2.69E-12 F Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F Stong 25C = 2.79E-12 F Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F Stong 25C = 2.89E-12 F Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F Stong 25C = 3.11E-12 F Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F Stong 25C = 3.23E-12 F Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F Stong 25C = 3.36E-12 F Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F Stong 25C = 3.48E-12 F Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F

Table 6-77. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Stong 25C = 3.60E-12 F Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F Stong 25C = 3.73E-12 F Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F Stong 25C = 3.85E-12 F Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F Stong 25C = 3.97E-12 F Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F Stong 25C = 4.09E-12 F Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F Stong 25C = 4.21E-12 F Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F Stong 25C = 4.32E-12 F Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F Stong 25C = 4.44E-12 F Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F Stong 25C = 4.56E-12 F Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F Stong 25C = 4.67E-12 F Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F Stong 25C = 4.79E-12 F Weak 25C = 6.12E-12 F 20h = Nominal 25C = 5.97E-12 F Stong 25C = 5.05E-12 F Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F Stong 25C = 5.20E-12 F Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F Stong 25C = 5.35E-12 F Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F Stong 25C = 5.49E-12 F Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F Stong 25C = 5.63E-12 F Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F Stong 25C = 5.78E-12 F Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F Stong 25C = 5.92E-12 F Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F Stong 25C = 6.06E-12 F Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F Stong 25C = 6.21E-12 F Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F Stong 25C = 6.35E-12 F Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F Stong 25C = 6.49E-12 F Weak 25C = 7.98E-12 F

Table 6-77. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Bh = Nominal 25C = 7.55E-12 F Stong 25C = 6.63E-12 F Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F Stong 25C = 6.77E-12 F Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F Stong 25C = 6.91E-12 F Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F Stong 25C = 7.05E-12 F Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F Stong 25C = 7.38E-12 F Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F Stong 25C = 7.57E-12 F Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F Stong 25C = 7.76E-12 F Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F Stong 25C = 7.94E-12 F Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F Stong 25C = 8.13E-12 F Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F Stong 25C = 8.32E-12 F Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F Stong 25C = 8.51E-12 F Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F Stong 25C = 8.70E-12 F Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F Stong 25C = 8.89E-12 F Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F Stong 25C = 9.07E-12 F Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F Stong 25C = 9.26E-12 F Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F Stong 25C = 9.45E-12 F Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F Stong 25C = 9.64E-12 F Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F Stong 25C = 9.82E-12 F Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F Stong 25C = 1.00E-11 F Weak 25C = 1.19E-11 F

Table 6-77. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Q1CAP	R/W	0h	Target HFXT Q1 cap trim 0h = Nominal 25C = 2.57E-12 F Stong 25C = 1.50E-12 F Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F Stong 25C = 1.60E-12 F Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F Stong 25C = 1.69E-12 F Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F Stong 25C = 1.79E-12 F Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F Stong 25C = 1.89E-12 F Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F Stong 25C = 1.99E-12 F Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F Stong 25C = 2.09E-12 F Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F Stong 25C = 2.19E-12 F Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F Stong 25C = 2.29E-12 F Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F Stong 25C = 2.39E-12 F Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F Stong 25C = 2.49E-12 F Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F Stong 25C = 2.59E-12 F Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F Stong 25C = 2.69E-12 F Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F Stong 25C = 2.79E-12 F Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F Stong 25C = 2.89E-12 F Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F Stong 25C = 3.11E-12 F Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F Stong 25C = 3.23E-12 F Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F Stong 25C = 3.36E-12 F Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F Stong 25C = 3.48E-12 F Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F

Table 6-77. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Stong 25C = 3.60E-12 F Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F Stong 25C = 3.73E-12 F Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F Stong 25C = 3.85E-12 F Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F Stong 25C = 3.97E-12 F Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F Stong 25C = 4.09E-12 F Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F Stong 25C = 4.21E-12 F Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F Stong 25C = 4.32E-12 F Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F Stong 25C = 4.44E-12 F Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F Stong 25C = 4.56E-12 F Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F Stong 25C = 4.67E-12 F Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F Stong 25C = 4.79E-12 F Weak 25C = 6.12E-12 F 20h = Nominal 25C = 5.97E-12 F Stong 25C = 5.05E-12 F Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F Stong 25C = 5.20E-12 F Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F Stong 25C = 5.35E-12 F Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F Stong 25C = 5.49E-12 F Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F Stong 25C = 5.63E-12 F Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F Stong 25C = 5.78E-12 F Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F Stong 25C = 5.92E-12 F Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F Stong 25C = 6.06E-12 F Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F Stong 25C = 6.21E-12 F Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F Stong 25C = 6.35E-12 F Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F Stong 25C = 6.49E-12 F Weak 25C = 7.98E-12 F

Table 6-77. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Bh = Nominal 25C = 7.55E-12 F Stong 25C = 6.63E-12 F Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F Stong 25C = 6.77E-12 F Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F Stong 25C = 6.91E-12 F Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F Stong 25C = 7.05E-12 F Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F Stong 25C = 7.38E-12 F Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F Stong 25C = 7.57E-12 F Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F Stong 25C = 7.76E-12 F Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F Stong 25C = 7.94E-12 F Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F Stong 25C = 8.13E-12 F Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F Stong 25C = 8.32E-12 F Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F Stong 25C = 8.51E-12 F Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F Stong 25C = 8.70E-12 F Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F Stong 25C = 8.89E-12 F Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F Stong 25C = 9.07E-12 F Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F Stong 25C = 9.26E-12 F Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F Stong 25C = 9.45E-12 F Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F Stong 25C = 9.64E-12 F Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F Stong 25C = 9.82E-12 F Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F Stong 25C = 1.00E-11 F Weak 25C = 1.19E-11 F

6.6.7.39 HFXTDYN Register (Offset = 120h) [Reset = 00000000h]

HFXTDYN is shown in Table 6-78.

Return to the Summary Table.

Alternative target values for HFXT configuration
Software can change these values to dynamically transition the HFXT configuration while HFXT is running.
Set [SEL] to select the alternative set of target values.

Table 6-78. HFXTDYN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEL	R/W	0x0	Select the dynamic configuration. Amplitude ramping will always happen using the values in [HFXTINIT.*], and [HFXTTARG.*]. Afterwards, this bit can be used to select between [HFXTTARG.*] and [HFXTDYN.*]. Hardware will ensure a smooth transition of analog control signals. 0h = Select configuration in [CKM.HFXTTARG0] and [CKM.HFXTTARG1]. 1h = Select configuration in [CKM.HFXTDYN0] and [CKM.HFXTDYN1].
30	RESERVED	R	0h	
29-23	AMPTHR	R/W	0h	Minimum HFXT amplitude
22-16	IDAC	R/W	0h	Minimum IDAC current
15-12	IREF	R/W	0h	Target HFXT IREF current

Table 6-78. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	Q2CAP	R/W	0h	Target HFXT Q2 cap trim 0h = Nominal 25C = 2.57E-12 F Stong 25C = 1.50E-12 F Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F Stong 25C = 1.60E-12 F Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F Stong 25C = 1.69E-12 F Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F Stong 25C = 1.79E-12 F Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F Stong 25C = 1.89E-12 F Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F Stong 25C = 1.99E-12 F Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F Stong 25C = 2.09E-12 F Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F Stong 25C = 2.19E-12 F Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F Stong 25C = 2.29E-12 F Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F Stong 25C = 2.39E-12 F Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F Stong 25C = 2.49E-12 F Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F Stong 25C = 2.59E-12 F Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F Stong 25C = 2.69E-12 F Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F Stong 25C = 2.79E-12 F Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F Stong 25C = 2.89E-12 F Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F Stong 25C = 3.11E-12 F Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F Stong 25C = 3.23E-12 F Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F Stong 25C = 3.36E-12 F Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F Stong 25C = 3.48E-12 F Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F

Table 6-78. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Stong 25C = 3.60E-12 F Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F Stong 25C = 3.73E-12 F Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F Stong 25C = 3.85E-12 F Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F Stong 25C = 3.97E-12 F Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F Stong 25C = 4.09E-12 F Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F Stong 25C = 4.21E-12 F Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F Stong 25C = 4.32E-12 F Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F Stong 25C = 4.44E-12 F Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F Stong 25C = 4.56E-12 F Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F Stong 25C = 4.67E-12 F Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F Stong 25C = 4.79E-12 F Weak 25C = 6.12E-12 F 20h = Nominal 25C = 5.97E-12 F Stong 25C = 5.05E-12 F Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F Stong 25C = 5.20E-12 F Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F Stong 25C = 5.35E-12 F Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F Stong 25C = 5.49E-12 F Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F Stong 25C = 5.63E-12 F Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F Stong 25C = 5.78E-12 F Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F Stong 25C = 5.92E-12 F Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F Stong 25C = 6.06E-12 F Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F Stong 25C = 6.21E-12 F Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F Stong 25C = 6.35E-12 F Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F Stong 25C = 6.49E-12 F Weak 25C = 7.98E-12 F

Table 6-78. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Bh = Nominal 25C = 7.55E-12 F Stong 25C = 6.63E-12 F Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F Stong 25C = 6.77E-12 F Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F Stong 25C = 6.91E-12 F Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F Stong 25C = 7.05E-12 F Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F Stong 25C = 7.38E-12 F Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F Stong 25C = 7.57E-12 F Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F Stong 25C = 7.76E-12 F Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F Stong 25C = 7.94E-12 F Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F Stong 25C = 8.13E-12 F Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F Stong 25C = 8.32E-12 F Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F Stong 25C = 8.51E-12 F Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F Stong 25C = 8.70E-12 F Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F Stong 25C = 8.89E-12 F Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F Stong 25C = 9.07E-12 F Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F Stong 25C = 9.26E-12 F Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F Stong 25C = 9.45E-12 F Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F Stong 25C = 9.64E-12 F Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F Stong 25C = 9.82E-12 F Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F Stong 25C = 1.00E-11 F Weak 25C = 1.19E-11 F

Table 6-78. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Q1CAP	R/W	0h	Target HFXT Q1 cap trim 0h = Nominal 25C = 2.57E-12 F Stong 25C = 1.50E-12 F Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F Stong 25C = 1.60E-12 F Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F Stong 25C = 1.69E-12 F Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F Stong 25C = 1.79E-12 F Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F Stong 25C = 1.89E-12 F Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F Stong 25C = 1.99E-12 F Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F Stong 25C = 2.09E-12 F Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F Stong 25C = 2.19E-12 F Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F Stong 25C = 2.29E-12 F Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F Stong 25C = 2.39E-12 F Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F Stong 25C = 2.49E-12 F Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F Stong 25C = 2.59E-12 F Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F Stong 25C = 2.69E-12 F Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F Stong 25C = 2.79E-12 F Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F Stong 25C = 2.89E-12 F Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F Stong 25C = 2.98E-12 F Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F Stong 25C = 3.11E-12 F Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F Stong 25C = 3.23E-12 F Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F Stong 25C = 3.36E-12 F Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F Stong 25C = 3.48E-12 F Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F

Table 6-78. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Stong 25C = 3.60E-12 F Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F Stong 25C = 3.73E-12 F Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F Stong 25C = 3.85E-12 F Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F Stong 25C = 3.97E-12 F Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F Stong 25C = 4.09E-12 F Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F Stong 25C = 4.21E-12 F Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F Stong 25C = 4.32E-12 F Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F Stong 25C = 4.44E-12 F Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F Stong 25C = 4.56E-12 F Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F Stong 25C = 4.67E-12 F Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F Stong 25C = 4.79E-12 F Weak 25C = 6.12E-12 F 20h = Nominal 25C = 5.97E-12 F Stong 25C = 5.05E-12 F Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F Stong 25C = 5.20E-12 F Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F Stong 25C = 5.35E-12 F Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F Stong 25C = 5.49E-12 F Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F Stong 25C = 5.63E-12 F Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F Stong 25C = 5.78E-12 F Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F Stong 25C = 5.92E-12 F Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F Stong 25C = 6.06E-12 F Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F Stong 25C = 6.21E-12 F Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F Stong 25C = 6.35E-12 F Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F Stong 25C = 6.49E-12 F Weak 25C = 7.98E-12 F

Table 6-78. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				2Bh = Nominal 25C = 7.55E-12 F Stong 25C = 6.63E-12 F Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F Stong 25C = 6.77E-12 F Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F Stong 25C = 6.91E-12 F Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F Stong 25C = 7.05E-12 F Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F Stong 25C = 7.18E-12 F Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F Stong 25C = 7.38E-12 F Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F Stong 25C = 7.57E-12 F Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F Stong 25C = 7.76E-12 F Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F Stong 25C = 7.94E-12 F Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F Stong 25C = 8.13E-12 F Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F Stong 25C = 8.32E-12 F Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F Stong 25C = 8.51E-12 F Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F Stong 25C = 8.70E-12 F Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F Stong 25C = 8.89E-12 F Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F Stong 25C = 9.07E-12 F Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F Stong 25C = 9.26E-12 F Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F Stong 25C = 9.45E-12 F Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F Stong 25C = 9.64E-12 F Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F Stong 25C = 9.82E-12 F Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F Stong 25C = 1.00E-11 F Weak 25C = 1.19E-11 F

6.6.7.40 AMPCFG0 Register (Offset = 124h) [Reset = 00000000h]

AMPCFG0 is shown in Table 6-79.

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Amplitude Compensation Configuration 0

Table 6-79. AMPCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Q2DLY	R/W	0x0	Q2CAP change delay. Number of clock cycles to wait before changing Q2CAP by one step. Clock frequency defined in FSMRATE.
27-24	Q1DLY	R/W	0x0	Q1CAP change delay. Number of clock cycles to wait before changing Q1CAP by one step. Clock frequency defined in FSMRATE.
23-20	ADCDLY	R/W	0h	ADC and PEAKDET startup time. Number of clock cycles to wait after enabling the PEAKDET and ADC before the first measurement. Clock frequency defined in FSMRATE.
19-15	LDOSTART	R/W	0h	LDO startup time. Number of clock cycles to bypass the LDO resistors for faster startup. Clock frequency defined in FSMRATE.
14-10	INJWAIT	R/W	0h	Inject HFOSC for faster HFXT startup. This value specifies the number of clock cycles to wait after injection is done. The clock speed is defined in FSMRATE.
9-5	INJTIME	R/W	0h	Inject HFOSC for faster HFXT startup. This value specifies the number of clock cycles the injection is enabled. The clock speed is defined in FSMRATE. Set to 0 to disable injection.
4-0	FSMRATE	R/W	0h	Update rate for the AMPCOMP update rate. Also affects the clock rate for the Amplitude ADC. The update rate is 6MHz / (FSMRATE+1). 0h = 6 MHz 1h = 3 MHz 2h = 2 MHz 5h = 1 MHz Bh = 500 kHz 17h = 250 kHz

6.6.7.41 AMPCFG1 Register (Offset = 128h) [Reset = 00000000h]

AMPCFG1 is shown in Table 6-80.

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Amplitude Compensation Configuration 1

Table 6-80. AMPCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	IDACDLY	R/W	0h	IDAC change delay. Time to wait before changing IDAC by one step. This time needs to be long enough for the crystal to settle. The number of clock cycles to wait is IDACDLY<<4 + 15. Clock frequency defined in FSMRATE.
27-24	IREFDLY	R/W	0h	IREF change delay. Number of clock cycles to wait before changing IREF by one step. Clock frequency defined in FSMRATE.
23-12	BIASLT	R/W	0h	Lifetime of the amplitude ADC bias value. This value specifies the number of adjustment intervals, until the ADC bias value has to be measured again. Set to 0 to disable automatic bias measurements.
11-0	INTERVAL	R/W	0h	Interval for amplitude adjustments. Set to 0 to disable periodic adjustments. This value specifies the number of clock cycles between adjustments. The clock speed is defined in FSMRATE.

6.6.7.42 LOOPCFG Register (Offset = 12Ch) [Reset = 00000000h]

LOOPCFG is shown in Table 6-81.

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Configuration Register for the Tracking Loop

Table 6-81. LOOPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	FINETRIM_INIT	R/W	0h	Initial value for the resistor fine trim
25-21	BOOST_TARGET	R/W	0h	Error-updates for 4x[BOOST_TARGET] times using [KI_BOOST]/[KP_BOOST], before using [KI]/[KP]. Note: If boost is used for long duration using large values of [KI_BOOST] & [KP_BOOST], the oscillator frequency can reach well above the max frequence limit of the design, causing unexpected behaviour.
20-18	KP_BOOST	R/W	0h	Proportional loop coefficient during BOOST
17-15	KI_BOOST	R/W	0h	Integral loop coefficient during BOOST
14-10	SETTLED_TARGET	R/W	0h	Number of updates before HFOSC is considered 'settled'
9-6	OOR_LIMIT	R/W	0h	Out-of-range threshold. OOR_LIMIT is compared with absolute value of 5 MSB bits of loop filter error.
5-3	KP	R/W	0h	Proportional loop coefficient
2-0	KI	R/W	0h	Integral loop coefficient

6.6.7.43 LOOPCFG1 Register (Offset = 130h) [Reset = 00000000h]

LOOPCFG1 is shown in Table 6-82.

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Configuration Register for underclocking HFOSC

Table 6-82. LOOPCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24-6	UNDERCLKCNT	R/W	0x0	Timer to trigger HFOSC underclocking. The timer will run at approximately 32.768 KHz.
5-0	KIOFF	R/W	0h	Based on [HFTRACKCTRL.UNDERCLK] configuration, after an event is triggerred, KI of the HFOSC tracking loop will be reduced by this amount.

6.6.7.44 AFOSCCTL Register (Offset = 140h) [Reset = 00000000h]

AFOSCCTL is shown in Table 6-83.

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Audio frequency oscillator control

Table 6-83. AFOSCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PW	W	0h	Password protection for [QUALBYP]. Write this field to 0xA5 to accept writes to [QUALBYP].
23-3	RESERVED	R	0h	
2	AUTODIS	R/W	0x0	If set, AFOSC can be disabled by PMCTL upon standby entry. [EN] bit will be overriden with a value 0 and user has to manually re-enable AFOSC.
1	QUALBYP	R/W	0x0	Clock qualification bypass. AFOSC qualification will skip a fixed number of clock cycles to prevent glitches or frequency overshoots from reaching the system. Setting this bit will bypass the qualification. This bit can be locked in SYS0. If unlocked, it is password protected with [PW].
0	EN	R/W	0x0	Enable AFOSC.

6.6.7.45 AFTRACKCTL Register (Offset = 144h) [Reset = 00000000h]

AFTRACKCTL is shown in Table 6-84.

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Audio frequency tracking loop control

Table 6-84. AFTRACKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0x0	Enable tracking loop.
30	DSMBYP	R/W	0x0	Bypass Delta-Sigma-Modulation of fine trim.
29-0	RATIO	R/W	0h	Ratio. Ratio format is 0b.30b 07D6343Fh = 0x07d6343f 088190ACh = 0x88190ac 08EE23B9h = 0x08ee23b9 0999999Ah = 0x0999999a 09B8B578h = 0x09b8b578

6.6.7.46 BANDGAPCTL Register (Offset = 148h) [Reset = 00000000h]

BANDGAPCTL is shown in Table 6-85.

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Configuration Register for the Tracking Loop

Table 6-85. BANDGAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BGOVR	R/W	0x0	Software override for bandgap control signals. This field is locked using the global-lock within SYS0.
30-4	RESERVED	R	0h	
3	VBGAPBYP	R/W	0x0	Bandgap reference enable.
2	VBGAPREFEN	R/W	0x0	Bandgap bypass counter. The counter runs at 24 MHz.
1	VDDRREFEN	R/W	0x0	This MMR is used only when BANDCFG.BGOVR is set.
0	REFEN	R/W	0x0	Enable reference voltage to AFOSC and HFOSC. This MMR is used only when BANDCFG.BGOVR is set.

6.6.7.47 AFCLKSEL Register (Offset = 150h) [Reset = 00000000h]

AFCLKSEL is shown in Table 6-86.

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Audio clock selection

Table 6-86. AFCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2-0	SRC	R/W	0x0	Select audio frequency clock source Software should make sure that proper clock is selected before enabling the audio IP. 0h = Clock disabled 1h = AFOSC clock 2h = 96MHz CLKHF 3h = 48MHz reference clock (HFXT) 4h = External clock

6.6.7.48 CANCLKSEL Register (Offset = 154h) [Reset = 00000000h]

CANCLKSEL is shown in Table 6-87.

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CAN clock selection

Table 6-87. CANCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	SRC	R/W	0x0	Select audio frequency clock source Software should make sure that proper clock is selected before enabling the audio IP. 0h = Clock disabled 1h = AFOSC clock 2h = 96MHz CLKHF

6.6.7.49 TRACKSTATAF Register (Offset = 160h) [Reset = 00000000h]

TRACKSTATAF is shown in Table 6-88.

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AF tracking loop status information

Table 6-88. TRACKSTATAF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOOPERRVLD	R	0x0	Current AFOSC tracking error valid This bit is one if the tracking loop is running and the error value is valid.
30	RESERVED	R	0h	
29-16	LOOPERR	R	0x0	Current AFOSC tracking error This field uses the internal fractional representation (sign, 9 integer bits, 4 fractional bits). The actual fine trim value of format (sign, 9 integer bits, 30 fractional bits) is saturated to (sign, 9 integer bits, 4 fractional bits).
15-13	RESERVED	R	0h	
12-0	FINETRIM	R	0h	Current AFOSC Fine-trim value This field uses the internal fractional representation (sign, 5 integer bits, 7 fractional bits). The actual fine trim value of format (sign, 5 integer bits, 19 fractional bits) is saturated to (sign, 5 integer bits, 7 fractional bits). The actual trim value applied to the oscillator is delta-sigma modulated 6 bits non-signed (inverted sign bit + integer bits).

6.6.7.50 TRACKSTATAF1 Register (Offset = 164h) [Reset = 00000000h]

TRACKSTATAF1 is shown in Table 6-89.

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AF tracking loop status information

Table 6-89. TRACKSTATAF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	
29-0	LOOPERR	R	0x0	Current AFOSC tracking error This field uses the fractional representation of the actual error(30 fractional bits). The actual error is of format (sign, 9 integer bits, 30 fractional bits).

6.6.7.51 TRACKSTATAF2 Register (Offset = 168h) [Reset = 00000000h]

TRACKSTATAF2 is shown in Table 6-90.

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AF tracking loop status information

Table 6-90. TRACKSTATAF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24-0	FINETRIM	R	0h	Current AFOSC Fine-trim value This field uses the internal fractional representation (sign, 5 integer bits, 19 fractional bits). The actual trim value applied to the oscillator is delta-sigma modulated 6 bits non-signed (inverted sign bit + integer bits). INTERNAL_NOTE: This field can be written by also writing a magic value (0x65) into bits [31:25]

6.6.7.52 LOOPCFGAF Register (Offset = 170h) [Reset = 00000000h]

LOOPCFGAF is shown in Table 6-91.

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Configuration Register for the Audio frequency Tracking Loop

Table 6-91. LOOPCFGAF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	FINETRIM_INIT	R/W	0h	Initial value for the resistor fine trim
25-21	BOOST_TARGET	R/W	0h	Number of error-updates using BOOST values, before using [KI]/[KP]
20-18	KP_BOOST	R/W	0h	Proportional loop coefficient during BOOST
17-15	KI_BOOST	R/W	0h	Integral loop coefficient during BOOST
14-10	SETTLED_TARGET	R/W	0h	Number of updates before AFOSC is considered 'settled'
9-6	OOR_LIMIT	R/W	0h	Out-of-range threshold. Out-of-range threshold. OOR_LIMIT is compared with absolute value of 5 MSB bits of loop filter error.
5-3	KP	R/W	0h	Proportional loop coefficient
2-0	KI	R/W	0h	Integral loop coefficient

6.6.7.53 CTL Register (Offset = 200h) [Reset = 00000000h]

CTL is shown in Table 6-92.

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Control

Table 6-92. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	CMD	HW	0h	**TDC** commands. 0h (W) = Clear SAT, DONE, and VALUE. This is not needed as prerequisite for a measurement. Reliable clear is only guaranteed from IDLE state. 1h (W) = Synchronous counter start. The counter looks for the opposite edge of the selected start event before it starts to count when the selected edge occurs. This guarantees an edge-triggered start and is recommended for frequency measurements. 2h (W) = Asynchronous counter start. The counter starts to count when the start event is high. To achieve precise edge-to-edge measurements you must ensure that the start event is low for at least 420 ns after you write this command. 3h (W) = Force **TDC** state machine back to IDLE state. Never write this command while STATE equals CLR_CNT or WAIT_CLR_CNT_DONE.

6.6.7.54 STAT Register (Offset = 204h) [Reset = 00000000h]

STAT is shown in Table 6-93.

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Status

Table 6-93. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	
9	STOP_BF	R	0h	Internal signal for debug purpose. 0: Stop signal arrived after falling edge of fast clock. 1: Stop signal arrived before falling edge of fast clock. Note that metastability can occur when the stop signal arrives close to an edge of the fast clock. STOP_BF can hence be 0 even though the stop signal arrived before the falling edge.
8	START_BF	R	0h	Internal signal for debug purpose. 0: Start signal arrived after falling edge of fast clock. 1: Start signal arrived before falling edge of fast clock. Note that metastability can occur when the stop signal arrives close to an edge of the fast clock. START_BF can hence be 0 even though the stop signal arrived before the falling edge.
7	SAT	R	0h	**TDC** measurement saturation flag. 0: Conversion has not saturated. 1: Conversion stopped due to saturation. This field is cleared when a new measurement is started or when CLR_RESULT is written to CMD.
6	DONE	R	0h	**TDC** measurement complete flag. 0: TDC measurement has not yet completed. 1: TDC measurement has completed. This field clears when a new TDC measurement starts or when you write CLR_RESULT to CMD.
5-0	STATE	R	0h	**TDC** state machine status. 0h (R) = Current state is TDC_STATE_WAIT_START. The fast-counter circuit looks for the start condition. The state machine waits for the fast-counter to increment. 4h (R) = Current state is TDC_STATE_WAIT_STARTSTOPCNTEN. The fast-counter circuit looks for the start condition. The state machine waits for the fast-counter to increment. 6h (R) = Current state is TDC_STATE_IDLE. This is the default state after reset and abortion. State will change when you write CMD to either RUN_SYNC_START or RUN. 7h (R) = Current state is TDC_STATE_CLRCNT. The fast-counter circuit is reset. 8h (R) = Current state is TDC_STATE_WAIT_STOP. The state machine waits for the fast-counter circuit to stop. Ch (R) = Current state is TDC_STATE_WAIT_STOPCNTDOWN. The fast-counter circuit looks for the stop condition. It will ignore a number of stop events configured in CNT. Eh (R) = Current state is TDC_STATE_GETRESULTS. The state machine copies the counter value from the fast-counter circuit. Fh (R) = Current state is TDC_STATE_POR. This is the reset state. 16h (R) = Current state is TDC_STATE_WAIT_CLRCNT_DONE. The state machine waits for fast-counter circuit to finish reset. 1Eh (R) = Current state is TDC_WAIT_STARTFALL. The fast-counter circuit waits for a falling edge on the start event. 2Eh (R) = Current state is TDC_FORCESTOP. You wrote ABORT to CMD to abort the **TDC** measurement.

6.6.7.55 RESULT Register (Offset = 208h) [Reset = 00000000h]

RESULT is shown in Table 6-94.

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Result Result of last **TDC** conversion.

Table 6-94. RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	0h	TDC conversion result. The result of the TDC conversion is given in number of clock edges of the clock source selected in REFCLK. Both rising and falling edges are counted. Note that LIMIT is given in periods, while VALUE is given in edges (periods*2). If TDC counter saturates, VALUE is slightly higher than LIMIT*2, as it takes a non-zero time to stop the measurement. Hence, the maximum value of this field becomes slightly higher than 2^{31} (2^{30} periods*2) if you configure LIMIT to R30.

6.6.7.56 SATCFG Register (Offset = 20Ch) [Reset = 00000000h]

SATCFG is shown in Table 6-95.

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Saturation Configuration

Table 6-95. SATCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	LIMIT	R/W	0h	Saturation limit. The flag SAT is set when the **TDC** counter saturates. Note that this value is given in periods, while VALUE is given in edges (periods*2). Values not enumerated are not supported 0h (R/W) = No saturation. An additional timer should be used to know if VALUE rolled over. 3h (R/W) = TDC conversion saturates and stops after 2^{12} periods. 4h (R/W) = TDC conversion saturates and stops after 2^{13} periods. 5h (R/W) = TDC conversion saturates and stops after 2^{14} periods. 6h (R/W) = TDC conversion saturates and stops after 2^{15} periods. 7h (R/W) = TDC conversion saturates and stops after 2^{16} periods. 8h (R/W) = TDC conversion saturates and stops after 2^{17} periods. 9h (R/W) = TDC conversion saturates and stops after 2^{18} periods. Ah (R/W) = TDC conversion saturates and stops after 2^{19} periods. Bh (R/W) = TDC conversion saturates and stops after 2^{20} periods. Ch (R/W) = TDC conversion saturates and stops after 2^{21} periods. Dh (R/W) = TDC conversion saturates and stops after 2^{22} periods. Eh (R/W) = TDC conversion saturates and stops after 2^{23} periods. Fh (R/W) = TDC conversion saturates and stops after 2^{24} periods. 10h (R/W) = TDC conversion saturates and stops after 2^{25} periods. 11h (R/W) = TDC conversion saturates and stops after 2^{26} periods. 12h (R/W) = TDC conversion saturates and stops after 2^{27} periods. 13h (R/W) = TDC conversion saturates and stops after 2^{28} periods. 14h (R/W) = TDC conversion saturates and stops after 2^{29} periods. 15h (R/W) = TDC conversion saturates and stops after 2^{30} periods.

6.6.7.57 TRIGSRC Register (Offset = 210h) [Reset = 00000000h]

TRIGSRC is shown in Table 6-96.

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Trigger Source Select source and polarity for **TDC** start and stop events. See the Technical Reference Manual for event timing requirements.

Table 6-96. TRIGSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15	STOP_POL	R/W	0h	Polarity of stop source. Change only while STATE is IDLE. 0h (R/W) = TDC conversion stops when high level is detected. 1h (R/W) = TDC conversion stops when low level is detected.
14-13	RESERVED	R	0h	
12-8	STOP_SRC	R/W	0h	Select stop source from the asynchronous **AUX** event bus. Change only while STATE is IDLE. 0h = LFTICK signal going to the RTC 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = Delayed version of selected LFCLK 4h = General purpose input signal 5h = Digital testbus bit 0 6h = Digital testbus bit 1 7h = Digital testbus bit 2 8h = Digital testbus bit 3 9h = Digital testbus bit 4 Ah = Digital testbus bit 5 Bh = Digital testbus bit 6 Ch = Digital testbus bit 7 Dh = Digital testbus bit 8 Eh = Digital testbus bit 9 Fh = Digital testbus bit 10 10h = Digital testbus bit 11 11h = Digital testbus bit 12 12h = Digital testbus bit 13 13h = Digital testbus bit 14 14h = Digital testbus bit 15 1Fh = Select TDC Prescaler event which is generated by configuration of PRECTL.
7	START_POL	R/W	0h	Polarity of start source. Change only while STATE is IDLE. 0h (R/W) = TDC conversion starts when high level is detected. 1h (R/W) = TDC conversion starts when low level is detected.
6-5	RESERVED	R	0h	

Table 6-96. TRIGSRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	START_SRC	R/W	0h	Select start source from the asynchronous **AUX** event bus. Change only while STATE is IDLE. 0h = LFTICK signal going to the RTC 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = Delayed version of selected LFCLK 4h = General purpose input signal 5h = Digital testbus bit 0 6h = Digital testbus bit 1 7h = Digital testbus bit 2 8h = Digital testbus bit 3 9h = Digital testbus bit 4 Ah = Digital testbus bit 5 Bh = Digital testbus bit 6 Ch = Digital testbus bit 7 Dh = Digital testbus bit 8 Eh = Digital testbus bit 9 Fh = Digital testbus bit 10 10h = Digital testbus bit 11 11h = Digital testbus bit 12 12h = Digital testbus bit 13 13h = Digital testbus bit 14 14h = Digital testbus bit 15 1Fh = Select TDC Prescaler event which is generated by configuration of PRECTL.

6.6.7.58 TRIGCNT Register (Offset = 214h) [Reset = 00000000h]

TRIGCNT is shown in Table 6-97.

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Trigger Counter Stop-counter control and status.

Table 6-97. TRIGCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	CNT	RH/W	0h	Number of stop events to ignore when EN is 1. Read CNT to get the remaining number of stop events to ignore during a **TDC** measurement. Write CNT to update the remaining number of stop events to ignore during a **TDC** measurement. The **TDC** measurement ignores updates of CNT if there are no more stop events left to ignore. When EN is 1, CNT is loaded into CNT at the start of the measurement.

6.6.7.59 TRIGCNTLOAD Register (Offset = 218h) [Reset = 00000000h]

TRIGCNTLOAD is shown in Table 6-98.

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Trigger Counter Load Stop-counter load.

Table 6-98. TRIGCNTLOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	CNT	R/W	0h	Number of stop events to ignore when EN is 1. To measure frequency of an event source: - Set start event equal to stop event. - Set CNT to number of periods to measure. Both 0 and 1 values measures a single event source period. To measure pulse width of an event source: - Set start event source equal to stop event source. - Select different polarity for start and stop event. - Set CNT to 0. To measure time from the start event to the Nth stop event when N > 1: - Select different start and stop event source. - Set CNT to (N-1). See the Technical Reference Manual for event timing requirements. When EN is 1, CNT is loaded into CNT at the start of the measurement.

6.6.7.60 TRIGCNTCFG Register (Offset = 21Ch) [Reset = 00000000h]

TRIGCNTCFG is shown in Table 6-99.

Return to the Summary Table.

Trigger Counter Configuration Stop-counter configuration.

Table 6-99. TRIGCNTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	EN	R/W	0h	Enable stop-counter. 0: Disable stop-counter. 1: Enable stop-counter. Change only while STATE is IDLE.

6.6.7.61 PRECTL Register (Offset = 220h) [Reset = 00000000h]

PRECTL is shown in Table 6-100.

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Prescaler Control
The prescaler can be used to count events that are faster than the bus rate.
It can be used to:
- count pulses on a specified event from the asynchronous event bus.
- prescale a specified event from the asynchronous event bus.
To use the prescaler output as an event source in **TDC** measurements you must set both START_SRC and STOP_SRC to TDC_PRE.
It is recommended to use the prescaler when the signal frequency to measure exceeds 1/10th of the bus rate.

Table 6-100. PRECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	RESET_N	R/W	0h	Prescaler reset. 0: Reset prescaler. 1: Release reset of prescaler. AUX_TDC_PRE event becomes 0 when you reset the prescaler.
6	RATIO	R/W	0h	Prescaler ratio. This controls how often the TDC_PRE event is generated by the prescaler. 0h (R/W) = Prescaler divides input by 16. AUX_TDC_PRE event has a rising edge for every 16 rising edges of the input. AUX_TDC_PRE event toggles on every 8th rising edge of the input. 1h (R/W) = Prescaler divides input by 64. AUX_TDC_PRE event has a rising edge for every 64 rising edges of the input. AUX_TDC_PRE event toggles on every 32nd rising edge of the input.
5	RESERVED	R	0h	
4-0	SRC	R/W	0h	Prescaler event source. Select an event from the asynchronous AUX event bus to connect to the prescaler input. Configure only while RESET_N is 0. 0h = LFTICK signal going to the RTC 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = Delayed version of selected LFCLK 4h = General purpose input signal 5h = Digital testbus bit 0 6h = Digital testbus bit 1 7h = Digital testbus bit 2 8h = Digital testbus bit 3 9h = Digital testbus bit 4 Ah = Digital testbus bit 5 Bh = Digital testbus bit 6 Ch = Digital testbus bit 7 Dh = Digital testbus bit 8 Eh = Digital testbus bit 9 Fh = Digital testbus bit 10 10h = Digital testbus bit 11 11h = Digital testbus bit 12 12h = Digital testbus bit 13 13h = Digital testbus bit 14 14h = Digital testbus bit 15 15h = High frequency on-chip oscillator 16h = High frequency crystal oscillator 17h = Audio frequency on-chip oscillator

6.6.7.62 PRECNTR Register (Offset = 224h) [Reset = 00000000h]

PRECNTR is shown in Table 6-101.

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Prescaler Counter

Table 6-101. PRECNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	CAPT	WC	0x0	Prescaler counter capture strobe. Write a 1 to CAPT to capture the value of the 16-bit prescaler counter into CNT. Read CNT to get the captured value.
15-0	CNT	R	0h	Prescaler counter value. Write a 1 to CAPT to capture the value of the 16-bit prescaler counter into CNT. Read CNT to get the captured value. The read value gets 1 LSB uncertainty if the event source level rises when you release the reset. The read value gets 1 LSB uncertainty if the event source level rises when you capture the prescaler counter. Please note the following: - The prescaler counter is reset to 3 by RESET_N. - The captured value is 3 when the number of rising edges on prescaler input is less than 3. Otherwise, captured value equals number of event pulses. INTERNAL_NOTE: The prescaler counter is implemented as a gray counter, the value is decoded to decimal upon capture.

6.6.7.63 CNT Register (Offset = 300h) [Reset = 00000000h]

CNT is shown in Table 6-102.

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WDT counter value register

Table 6-102. CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0x0	Counter value. A write to this field immediately starts (or restarts) the counter. It will count down from the written value. If the counter reaches 0, a reset will be generated. A write value of 0 immediately generates a reset. This field is only writable if not locked. See LOCK register. Writing this field will automatically activate the lock. A read returns the current value of the counter.

6.6.7.64 TEST Register (Offset = 304h) [Reset = 00000000h]

TEST is shown in Table 6-103.

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WDT test mode register

Table 6-103. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	STALLEN	R/W	0x0	WDT stall enable This field is only writable if not locked. See LOCK register. 0h = DISABLE WDT continues counting while the CPU is stopped by a debugger. 1h = ENABLE WDT stops counting while the CPU is stopped by a debugger.

6.6.7.65 LOCK Register (Offset = 308h) [Reset = 00000000h]

LOCK is shown in Table 6-104.

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WDT lock register

Table 6-104. LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STAT	R/W	0h	A write with value 0x1ACCE551 unlocks the watchdog registers for write access. A write with any other value locks the watchdog registers for write access. Writing the [CNT] register will also lock the watchdog registers. A read of this field returns the state of the lock (0=unlocked, 1=locked).

6.6.8 CKMD Registers

Table 6-105 lists the memory-mapped registers for the CKMD registers. All register offset addresses not listed in Table 6-105 should be considered as reserved locations and the register contents should not be modified.

Table 6-105. CKMD Registers

Offset	Acronym	Register Name	Section
0h	DESC	IP Description	Section 6.6.8.1
44h	IMASK	Interrupt mask.	Section 6.6.8.2
48h	RIS	Raw interrupt flag register	Section 6.6.8.3
4Ch	MIS	Masked interrupt flag register	Section 6.6.8.4
50h	ISET	Interrupt flag set register	Section 6.6.8.5
54h	ICLR	Interrupt flag clear register	Section 6.6.8.6
58h	IMSET	Interrupt mask set register	Section 6.6.8.7
5Ch	IMCLR	Interrupt mask clear register.	Section 6.6.8.8
80h	HFOSCCTL	Internal. Only to be used through TI provided API.	Section 6.6.8.9
84h	HFXTCTL	High frequency crystal control	Section 6.6.8.10
8Ch	LFOSCCTL	Low frequency oscillator control	Section 6.6.8.11
90h	LFXTCTL	Low frequency crystal control	Section 6.6.8.12
94h	LFQUALCTL	Low frequency clock qualification control	Section 6.6.8.13
98h	LFINCCTL	Low frequency time increment control	Section 6.6.8.14
9Ch	LFINCOVR	Low frequency time increment override control	Section 6.6.8.15
A0h	AMPADCCTL	Internal. Only to be used through TI provided API.	Section 6.6.8.16
A4h	HFTRACKCTL	High frequency tracking loop control	Section 6.6.8.17
A8h	LDOCTL	Internal. Only to be used through TI provided API.	Section 6.6.8.18
ACh	NABIASCTL	Nanoamp-bias control	Section 6.6.8.19
B0h	LFMONCTL	Low-frequency clock-monitor control	Section 6.6.8.20
B4h	LFINCCTL2	Low frequency time increment control-2	Section 6.6.8.21
C0h	LFCLKSEL	Low frequency clock selection	Section 6.6.8.22
C4h	TDCCLKSEL	Internal. Only to be used through TI provided API.	Section 6.6.8.23
C8h	ADCCLKSEL	ADC clock selection	Section 6.6.8.24
E0h	LFCLKSTAT	Low-frequency clock status	Section 6.6.8.25
E4h	HFXTSTAT	HFXT status information	Section 6.6.8.26
E8h	AMPADCSTAT	Internal. Only to be used through TI provided API.	Section 6.6.8.27
ECh	TRACKSTAT	HF tracking loop status information	Section 6.6.8.28
F0h	AMPSTAT	HFXT Amplitude Compensation Status	Section 6.6.8.29
F4h	LFCLKSTAT2	Low-frequency clock status-2	Section 6.6.8.30
100h	ATBCTL0	Internal. Only to be used through TI provided API.	Section 6.6.8.31
104h	ATBCTL1	Internal. Only to be used through TI provided API.	Section 6.6.8.32
108h	DTBCTL	Digital test bus mux control	Section 6.6.8.33
10Ch	DTBCTL2	Digital test bus mux control	Section 6.6.8.34
110h	TRIM0	Internal. Only to be used through TI provided API.	Section 6.6.8.35
114h	TRIM1	Internal. Only to be used through TI provided API.	Section 6.6.8.36
118h	HFXTINIT	Initial values for HFXT ramping	Section 6.6.8.37
11Ch	HFXTTARG	Target values for HFXT ramping	Section 6.6.8.38
120h	HFXTDYN	Alternative target values for HFXT configuration	Section 6.6.8.39
124h	AMPCFG0	Amplitude Compensation Configuration 0	Section 6.6.8.40
128h	AMPCFG1	Amplitude Compensation Configuration 1	Section 6.6.8.41

Table 6-105. CKMD Registers (continued)

Offset	Acronym	Register Name	Section
12Ch	LOOPCFG	Configuration Register for the Tracking Loop	Section 6.6.8.42
130h	LOOPCFG1	Configuration Register for underclocking HFOSC	Section 6.6.8.43
140h	AFOSCCTL	Audio frequency oscillator control	Section 6.6.8.44
144h	AFTRACKCTL	Audio frequency tracking loop control	Section 6.6.8.45
148h	BANDGAPCTL	Internal. Only to be used through TI provided API.	Section 6.6.8.46
150h	AFCLKSEL	Audio clock selection	Section 6.6.8.47
154h	CANCLKSEL	CAN clock selection	Section 6.6.8.48
160h	TRACKSTATAF	AF tracking loop status information	Section 6.6.8.49
164h	TRACKSTATAF1	AF tracking loop status information	Section 6.6.8.50
168h	TRACKSTATAF2	AF tracking loop status information	Section 6.6.8.51
170h	LOOPCFGAF	Configuration Register for the Audio frequency Tracking Loop	Section 6.6.8.52
200h	CTL	Control	Section 6.6.8.53
204h	STAT	Status	Section 6.6.8.54
208h	RESULT	Result	Section 6.6.8.55
20Ch	SATCFG	Saturation Configuration	Section 6.6.8.56
210h	TRIGSRC	Trigger Source	Section 6.6.8.57
214h	TRIGCNT	Trigger Counter	Section 6.6.8.58
218h	TRIGCNTLOAD	Trigger Counter Load	Section 6.6.8.59
21Ch	TRIGCNTCFG	Trigger Counter Configuration	Section 6.6.8.60
220h	PRECTL	Prescaler Control	Section 6.6.8.61
224h	PRECNTR	Prescaler Counter	Section 6.6.8.62
300h	CNT	WDT counter value register	Section 6.6.8.63
304h	TEST	WDT test mode register	Section 6.6.8.64
308h	LOCK	WDT lock register	Section 6.6.8.65

Complex bit access types are encoded to fit into small table cells. Table 6-106 shows the codes that are used for access types in this section.

Table 6-106. CKMD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.8.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 6-107.

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IP Description

Table 6-107. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	9B4Bh	Module identifier
15-12	STDIPOFF	R	1h	Standard IP MMR block offset
11-8	RESERVED	R	0h	Reserved
7-4	MAJREV	R	0h	Major revision
3-0	MINREV	R	0h	Minor revision

6.6.8.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 6-108.

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Interrupt mask.;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 6-108. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	R/W	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	R/W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	R/W	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	R/W	0h	AFOSC good indication.
18	TRACKREFAFOOR	R/W	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	R/W	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	R/W	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	R/W	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	R/W	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	R/W	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	R/W	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	R/W	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	R/W	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	R/W	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	R/W	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	R/W	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	R/W	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	R/W	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.

Table 6-108. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRACKREFOOR	R/W	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.
3	TRACKREFLOSS	R/W	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	R/W	0h	HFXT amplitude good indication.
1	HFXTFAULT	R/W	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	R/W	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 6-109.

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Raw interrupt flag register

Table 6-109. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	R	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	R	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	R	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	R	0h	AFOSC good indication.
18	TRACKREFAFOOR	R	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	R	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	R	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	R	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	R	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	R	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	R	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	R	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	R	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	R	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	R	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	R	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	R	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	R	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	R	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.

Table 6-109. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRACKREFLOSS	R	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	R	0h	HFXT amplitude good indication.
1	HFXTFAULT	R	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	R	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 6-110.

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Masked interrupt flag register

Table 6-110. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	R	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	R	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	R	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	R	0h	AFOSC good indication.
18	TRACKREFAFOOR	R	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	R	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	R	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	R	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	R	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	R	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	R	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	R	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	R	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	R	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	R	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	R	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	R	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	R	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	R	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.

Table 6-110. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRACKREFLOSS	R	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	R	0h	HFXT amplitude good indication.
1	HFXTFAULT	R	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	R	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 6-111.

Return to the Summary Table.

Interrupt flag set register

Table 6-111. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	W	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	W	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	W	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.

Table 6-111. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 6-112.

Return to the Summary Table.

Interrupt flag clear register

Table 6-112. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	W	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	W	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	W	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.

Table 6-112. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 6-113.

Return to the Summary Table.

Interrupt mask set register

Table 6-113. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	W	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	W	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	W	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.

Table 6-113. IMSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 6-114.

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Interrupt mask clear register.;Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 6-114. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	HFOSCSETTLED	W	0h	Indicates that HFOSC has settled, based on LOOPCFG.SETTLED_TARGET and LOOPCFG1.SETTLEIRQ
22	LFGEARRSTRTLIM	W	0h	Indicates that the LFINC filter gearing mechanism has restarted more than LFINCCTL2.GEARRSTRTLIM
21	RESERVED	R	0h	Reserved
20	SYSUNDERCLOCKED	W	0h	Indicates system frequency has been lowered. It will be set only if HFTRACKCTL.UNDERCLK is appropriately configured and HFOSC tracking loop is not running.
19	AFOSCGOOD	W	0h	AFOSC good indication.
18	TRACKREFAFOOR	W	0h	Out-of-range indication from the AFOSC tracking loop.;Indicates that the reference clock frequency of AFOSC tracking loop is out-of-range.
17	LFTICK	W	0h	32kHz TICK to RTC and WDT.;Either derived from selected LFCLK or generated from CLKULL in absence of LFCLK.
16	LFGEARRSTRT	W	0h	LFINC filter gearing restart.;Indicates that the LFINC filter restarted gearing. Subsequent LFINC estimates may have higher variation.
15	AMPSETTLED	W	0h	HFXT Amplitude compensation - settled;Indicates that the amplitude compensation FSM has reached the SETTLED or TCXOMODE state,;and the controls configured in HFXTTARG or HFXTDYN are reached.
14	AMPCTRLATTARG	W	0h	HFXT Amplitude compensation - controls at target;Indicates that the control values configured in HFXTTARG or HFXTDYN are reached.;Applies to Q1CAP, Q2CAP and IREF.
13	PRELFEDGE	W	0h	Pre-LF clock edge detect.;Indicates that a positive edge occured on the selected pre-LF clock CLKSEL.PRELFCLK';Can be used by software to confirm that a LF clock source is running and within the expected frequency,;before selecting it as the main LF clock source.
12	LFCLKLOSS	W	0h	LF clock is lost.;Indicates that no LF clock edge occured for ~49us (~1.6 times nominal period).;The system will automatically fall-back to generating LFTICK based on CLKULL,;to avoid timing corruption.;Note that this signal is NOT related to the analog LF clock-loss detector which can reset the device during STANDBY.
11	LFCLKOOR	W	0h	LF clock period out-of-range.;Indicates that a LF clock period was measured to be out-of-range,;according to LFQUALCTL.MAXERR.
10	LFCLKGOOD	W	0h	LF clock good.;Indicates that the LF clock is good, according to the configuration in LFQUALCTL.
9	LFINCUPD	W	0h	LFINC updated.;Indicates that a new LFINC measurement value is available in LFCLKSTAT.LFINC.
8	TDCDONE	W	0h	TDC done event.;Indicates that the TDC measurement is done.
7	ADCPEAKUPD	W	0h	HFXT-ADC PEAK measurement update event.;Indicates that the HFXT-ADC PEAK measurement is done.
6	ADCBIASUPD	W	0h	HFXT-ADC BIAS measurement update event.;Indicates that the HFXT-ADC BIAS measurement is done.
5	ADCCOMPUPD	W	0h	HFXT-ADC comparison update event.;Indicates that the HFXT-ADC comparison is done.
4	TRACKREFOOR	W	0h	Out-of-range indication from the tracking loop.;Indicates that the selected reference clock frequency of the tracking loop is out-of-range.

Table 6-114. IMCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TRACKREFLOSS	W	0h	Clock loss indication from the tracking loop.;Indicates that the selected reference clock of the tracking loop is lost.
2	HFXTAMPGOOD	W	0h	HFXT amplitude good indication.
1	HFXTFAULT	W	0h	HFXT fault indication.;Indicates that HFXT did not start correctly, or its frequency is too low.;HFXT will not recover from this fault and has to be restarted.;This is only a one-time check at HFXT startup.
0	HFXTGOOD	W	0h	HFXT good indication.;Indicates that HFXT started correctly. The frequency is not necessarily good enough for radio operation.;This is only a one-time check at HFXT startup.

6.6.8.9 HFOSCCTL Register (Offset = 80h) [Reset = 00000000h]

HFOSCCTL is shown in Table 6-115.

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Internal. Only to be used through TI provided API.

Table 6-115. HFOSCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PW	W	0h	Internal. Only to be used through TI provided API.
23-2	RESERVED	R	0h	Reserved
1	FORCEOFF	R/W	0h	Internal. Only to be used through TI provided API.
0	QUALBYP	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.10 HFXTCTL Register (Offset = 84h) [Reset = 00000000h]

HFXTCTL is shown in Table 6-116.

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High frequency crystal control

Table 6-116. HFXTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AMPOVR	R/W	0h	Internal. Only to be used through TI provided API.
30-27	RESERVED	R	0h	Reserved
26	BIASEN	R/W	0h	Internal. Only to be used through TI provided API.
25	LPBUFEN	R/W	0h	Internal. Only to be used through TI provided API.
24	INJECT	R/W	0h	Internal. Only to be used through TI provided API.
23	QUALBYP	R/W	0h	Internal. Only to be used through TI provided API.
22-20	RESERVED	R	0h	Reserved
19-8	QUALDLY	R/W	0h	Skip potentially unstable clock cycles after enabling HFXT.;Number of cycles skipped is 8*QUALDLY.
7	TCXOMODE	R/W	0h	Temperature compensated crystal oscillator mode.;Set this bit if a TXCO is connected.
6	TCXOTYPE	R/W	0h	Type of temperature compensated crystal used.;Only has effect if TCXOMODE is set. 0h = Use with clipped-sine TCXO 1h = Use with CMOS TCXO
5-3	RESERVED	R	0h	Reserved
2	AUTOEN	R/W	0h	Internal. Only to be used through TI provided API.
1	HPBUFEN	R/W	0h	High performance clock buffer enable.;This bit controls the clock output for the RF PLL.;It is required for radio operation.
0	EN	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.11 LFOSCCTL Register (Offset = 8Ch) [Reset = 00000000h]

LFOSCCTL is shown in Table 6-117.

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Low frequency oscillator control

Table 6-117. LFOSCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	LFOSC enable

6.6.8.12 LFXTCTL Register (Offset = 90h) [Reset = 00000000h]

LFXTCTL is shown in Table 6-118.

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Low frequency crystal control

Table 6-118. LFXTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-13	LEAKCOMP	R/W	0h	Leakage compensation control 0h = Full leakage compensation 1h = Half leakage compensation 3h = No leakage compensation
12	BUFBIAS	R/W	0h	Control the BIAS current of the input amp in LP buffer 0h = Minimum bias current: 25nA 1h = Maximum bias current: 50nA
11-8	AMPBIAS	R/W	0h	Adjust current mirror ratio into oscillator core. This value is depending on crystal and is set by FW. This field uses a 2's complement encoding.
7-6	BIASBOOST	R/W	0h	Boost oscillator amplitude;This value depends on the crystal and needs to be configured by Firmware.
5-4	REGBIAS	R/W	0h	Regulation loop bias resistor value;This value depends on the crystal and needs to be configured by Firmware.
3	RESERVED	R	0h	Reserved
2	HPBUFEN	R/W	0h	Control the buffer used. In normal operation, low-power buffer is used in all device modes. The high-performance buffer is only used for test purposes.
1	AMPREGMODE	R/W	0h	Amplitude regulation mode 0h = Amplitude control loop enabled 1h = Amplitude control loop disabled
0	EN	R/W	0h	LFXT enable

6.6.8.13 LFQUALCTL Register (Offset = 94h) [Reset = 00000000h]

LFQUALCTL is shown in Table 6-119.

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Low frequency clock qualification control

Table 6-119. LFQUALCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	MAXERR	R/W	20h	Maximum LFCLK period error.;Value given in microseconds, 3 integer bits + 3 fractional bits.
7-0	CONSEC	R/W	64h	Number of consecutive times the LFCLK period error has to be ;smaller than MAXERR to be considered "good".;Setting this value to 0 will bypass clock qualification,;and the "good" indicator will always be 1.

6.6.8.14 LFINCCTL Register (Offset = 98h) [Reset = 00000000h]

LFINCCTL is shown in Table 6-120.

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Low frequency time increment control

Table 6-120. LFINCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PREVENTSTBY	R/W	1h	Controls if the LFINC filter prevents STANBY entry until settled. 0h = Disable. Do not prevent STANDBY entry. 1h = Enable. Prevent STANDBY entry.
30	KEEPHFXTEN	R/W	0h	Keeps the HFXT enabled till the LFINC filter settles 0h = Disable. Do not keep HFXT enabled. 1h = Enable. Keep HFXT enabled.
29-8	INT	R/W	001E8480h	Integral part of the LFINC filter.;This value is updated by Hardware to reflect the current state of the filter.;It can also be written to change the current state.
7	STOPGEAR	R/W	0h	Controls the final gear of the LFINC filter. 0h = The LF filter is considered settled when LFCLKSTAT2.MAINGEAR reads 9 and LFCLKSTAT2.SUBGEAR reads 7. That means the LF filter will take 79 LF periods to settle provided the gear does not restarts. 1h = The LF filter is considered settled when LFCLKSTAT2.MAINGEAR reads 8 and LFCLKSTAT2.SUBGEAR reads 7. That means the LF filter will take 71 LF periods to settle provided the gear does not restarts.
6-5	ERRTHR	R/W	0h	Controls the threshold for gearing restart of the LFINC filter.;Only effective if GEARRSTRT is not ONETHR or TWOTHR. 0h = Restart gearing on large error. Fewer false restarts, slower response on small frequency shifts. 1h = Middle value towards LARGE. 2h = Middle value towards SMALL. 3h = Restart gearing on small error. Potentially more false restarts, faster response on small frequency shifts.
4-3	GEARRSTRT	R/W	2h	Controls gearing restart of the LFINC filter. 0h = Never restart gearing. Very stable filter value, but very slow response on frequency changes. 1h = Restart gearing when the error accumulator crosses the threshold once. 2h = Restart gearing when the error accumulator crosses the threshold twice in a row.
2	SOFTRSTRT	R/W	1h	Use a higher gear after re-enabling / wakeup.;The filter will require 16-24 LFCLK periods to settle (depending on STOPGEAR), but may respond faster to frequency changes during STANDBY. 0h = Don't use soft gearing restarts 1h = Use soft gearing restarts
1-0	EN	R/W	1h	Enable LFINC filter. Programming with a value of 0x3 will disable the LFINC filter 0h = DISABLED 1h = ENABLED 2h = Enable based on HFOS getting settled. HFOSC gets settled after the tracking loop has updated equal to or more than LOOPCFG.SETTLED_TARGET times.

6.6.8.15 LFINCOVR Register (Offset = 9Ch) [Reset = 00000000h]

LFINCOVR is shown in Table 6-121.

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Low frequency time increment override control

Table 6-121. LFINCOVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVERRIDE	R/W	0h	Override LF increment;Use the value provided in LFINC instead of the value calculated by Hardware.
30-22	RESERVED	R	0h	Reserved
21-0	LFINC	R/W	Xh	LF increment value;This value is used when OVERRIDE is set to 1.;Otherwise the value is calculated automatically.;The current LFINC value can be read from [CKM.LFCLKSTAT.LFINC].

6.6.8.16 AMPADCCTL Register (Offset = A0h) [Reset = 00000000h]

AMPADCCTL is shown in Table 6-122.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-122. AMPADCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SWOVR	R/W	0h	Internal. Only to be used through TI provided API.
30-18	RESERVED	R	0h	Reserved
17	PEAKDETEN	R/W	0h	Internal. Only to be used through TI provided API.
16	ADCEN	R/W	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14-8	COMPVAL	R/W	0h	Internal. Only to be used through TI provided API.
7-5	RESERVED	R	0h	Reserved
4	SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
3-2	RESERVED	R	0h	Reserved
1	COMPSTRT	R/W	0h	Internal. Only to be used through TI provided API.
0	SARSTRT	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.17 HFTRACKCTL Register (Offset = A4h) [Reset = 00000000h]

HFTRACKCTL is shown in Table 6-123.

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High frequency tracking loop control

Table 6-123. HFTRACKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable tracking loop.
30	DSMBYP	R/W	0h	Bypass Delta-Sigma-Modulation of fine trim.
29-28	UNDERCLK	R/W	0h	When the HFOSC tracking loop is not running, this bitfield can be used to set the condition to automatically lower the HFOSC frequency. This will prevent frequency drift that may lead to SOC instability. 0h = Disable 1h = Timer event 2h = Temperature event from Batmon 3h = Temperature event from Batmon or Timer event
27-26	REFCLK	R/W	0h	Select the reference clock for the tracking loop.;Change only while the tracking loop is disabled. 0h = Select HFXT as reference clock. 1h = Select LRF reference clock. 2h = Select GPI as reference clock.
25-0	RATIO	R/W	00400000h	Reference clock ratio. Ratio format is 2b.24b;RATIO = 24MHz / (2*reference-frequency) * 2^{24};Commonly used reference clock frequencies are provided as enumerations.

6.6.8.18 LDOCTL Register (Offset = A8h) [Reset = 00000000h]

LDOCTL is shown in Table 6-124.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-124. LDOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SWOVR	R/W	0h	Internal. Only to be used through TI provided API.
30-5	RESERVED	R	0h	Reserved
4	HFXTLVLEN	R/W	0h	Internal. Only to be used through TI provided API.
3	STARTCTL	R/W	0h	Internal. Only to be used through TI provided API.
2	START	R/W	0h	Internal. Only to be used through TI provided API.
1	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
0	EN	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.19 NABIASCTL Register (Offset = ACh) [Reset = 00000000h]

NABIASCTL is shown in Table 6-125.

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Nanoamp-bias control

Table 6-125. NABIASCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Enable nanoamp-bias

6.6.8.20 LFMONCTL Register (Offset = B0h) [Reset = 00000000h]

LFMONCTL is shown in Table 6-126.

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Low-frequency clock-monitor control

Table 6-126. LFMONCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Enable LFMONITOR.;Enable only after a LF clock source has been selected, enabled and is stable.;If LFMONITOR detects a clock loss, the system will be reset.

6.6.8.21 LFINCCTL2 Register (Offset = B4h) [Reset = 00000000h]

LFINCCTL2 is shown in Table 6-127.

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Low frequency time increment control-2

Table 6-127. LFINCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ADJUSTLFINC	R/W	0h	Adjusts LFINC while transitioning from fake to real LF clock if necessary. For the adjustment to happen, tracking loop must be running.
30-10	RESERVED	R	0h	Reserved
9-4	GEARRSTRTLIM	R/W	0h	Specifies the number of times gear could be restarted before raising an interrupt. It has no impact on the number of times gear can be reduced.;A value of 0 indicates that the interrupt mechanism is disabled
3-0	GEARREDCNT	R/W	2h	Specifies the number by which gear should be reduced post standby exit

6.6.8.22 LFCLKSEL Register (Offset = C0h) [Reset = 00000000h]

LFCLKSEL is shown in Table 6-128.

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Low frequency clock selection

Table 6-128. LFCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	PRE	R/W	0h	Select low frequency clock source for the PRELFCLK interrupt.;Can be used by Software to confirm that the clock is running and it's frequency is good, before selecting it in MAIN. 0h = No clock. Output will be tied low. 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = External LF clock through GPI.
1-0	MAIN	R/W	0h	Select the main low frequency clock source.;If running, this clock will be used to generate LFTICK and as CLKULL during STANDBY.;If not running, LFTICK will be generated from HFOSC and STANDBY entry will be prevented. 0h = No LF clock selected. LFTICK will be generated from HFOSC, STANDBY entry will be prevented. 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = External LF clock through GPI.

6.6.8.23 TDCCLKSEL Register (Offset = C4h) [Reset = 00000000h]

TDCCLKSEL is shown in Table 6-129.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-129. TDCCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	REFCLK	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.24 ADCCLKSEL Register (Offset = C8h) [Reset = 00000000h]

ADCCLKSEL is shown in Table 6-130.

Return to the Summary Table.

ADC clock selection

Table 6-130. ADCCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SRC	R/W	0h	Select ADC clock source;Change only while ADC is disabled! 0h = 48MHz CLKSVT 1h = 48MHz HFXT

6.6.8.25 LFCLKSTAT Register (Offset = E0h) [Reset = 00000000h]

LFCLKSTAT is shown in Table 6-131.

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Low-frequency clock status

Table 6-131. LFCLKSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GOOD	R	0h	Low frequency clock good;Note: This is only a coarse frequency check based on LFQUALCTL. The clock may not be accurate enough for timing purposes.
30-26	RESERVED	R	0h	Reserved
25	FLTSETTLED	R	0h	LFINC filter is running and settled.
24	LFTICKSRC	R	1h	Source of LFTICK. 0h = LFTICK generated from the selected LFCLK 1h = LFTICK generated from CLKULL (LFCLK not available)
23-22	LFINCSRC	R	3h	Source of LFINC used by the RTC.;This value depends on LFINCOVR.OVERRIDE, LF clock availability, HF tracking loop status and the device state (ACTIVE/STANDBY). 0h = Using measured value.;This value is updated by hardware and can be read from LFINC. 1h = Using filtered / average value.;This value is updated by hardware and can be read and updated in LFINCCTL.INT. 2h = Using override value from LFINCOVR.LFINC 3h = Using FAKE LFTICKs with corresponding LFINC value.
21-0	LFINC	R	001E8480h	Measured value of LFINC.;Given in microseconds with 16 fractional bits.;This value is calculated by Hardware.;It is the LFCLK period according to CLKULL cycles.

6.6.8.26 HFXTSTAT Register (Offset = E4h) [Reset = 00000000h]

HFXTSTAT is shown in Table 6-132.

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HFXT status information

Table 6-132. HFXTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-16	STARTUPTIME	R	0h	HFXT startup time;Can be used by software to plan starting HFXT ahead in time.;Measured whenever HFXT is enabled in CLKULL periods (24MHz), from HFXTCTL.EN until the clock is good for radio operation (amplitude compensation is settled).
15-2	RESERVED	R	0h	Reserved
1	FAULT	R	0h	HFXT clock fault;Indicates a lower than expected HFXT frequency.;HFXT will not recover from this fault, disabling and re-enabling HFXT is required.
0	GOOD	R	0h	HFXT clock available.;The frequency is not necessarily good enough for radio operation.

6.6.8.27 AMPADCSTAT Register (Offset = E8h) [Reset = 00000000h]

AMPADCSTAT is shown in Table 6-133.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-133. AMPADCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	COMPOUT	R	0h	Internal. Only to be used through TI provided API.
23	RESERVED	R	0h	Reserved
22-16	PEAKRAW	R	0h	Internal. Only to be used through TI provided API.
15-8	PEAK	R	0h	Internal. Only to be used through TI provided API.
7	RESERVED	R	0h	Reserved
6-0	BIAS	R	0h	Internal. Only to be used through TI provided API.

6.6.8.28 TRACKSTAT Register (Offset = ECh) [Reset = 00000000h]

TRACKSTAT is shown in Table 6-134.

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HF tracking loop status information

Table 6-134. TRACKSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOOPERRVLD	R	0h	Current HFOSC tracking error valid;This bit is one if the tracking loop is running and the error value is valid.
30	RESERVED	R	0h	Reserved
29-16	LOOPERR	R	0h	Current HFOSC tracking error;This field uses the internal fractional representation (sign, 9 integer bits, 4 fractional bits).
15-13	RESERVED	R	0h	Reserved
12-0	FINETRIM	R	1D80h	Current HFOSC Fine-trim value;This field uses the internal fractional representation (sign, 5 integer bits, 7 fractional bits).;The actual trim value applied to the oscillator is delta-sigma modulated 6 bits non-signed;(inverted sign bit + integer bits).

6.6.8.29 AMPSTAT Register (Offset = F0h) [Reset = 00000000h]

AMPSTAT is shown in Table 6-135.

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HFXT Amplitude Compensation Status

Table 6-135. AMPSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-25	STATE	R	0h	Current AMPCOMP FSM state. 0h = FSM in idle state 1h = Starting LDO 2h = Second shutdown state 3h = Injecting HFOSC for fast startup 4h = Transition to HFXTTARG values 5h = Initial amplitude ramping with HFXTINIT values 6h = Amplitude down correction 7h = Post injection settle wait Ah = First shutdown state Ch = TCXO settled state Eh = Amplitude up correction Fh = Settled state
24-18	IDAC	R	0h	Current IDAC control value.
17-14	IREF	R	0h	Current IREF control value.
13-8	Q2CAP	R	0h	Current Q2CAP control value.
7-2	Q1CAP	R	0h	Current Q1CAP control value.
1	CTRLATTARGET	R	0h	HFXT control values match target values.;This applies to IREF, Q1CAP, Q2CAP values.
0	AMPGOOD	R	0h	HFXT amplitude good

6.6.8.30 LFCLKSTAT2 Register (Offset = F4h) [Reset = 00000000h]

LFCLKSTAT2 is shown in Table 6-136.

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Low-frequency clock status-2

Table 6-136. LFCLKSTAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	SUBGEAR	R	0h	The value of sub gear in LF filter. It counts from 0 to 7.
3-0	MAINGEAR	R	0h	The value of main gear in LF filter. The main gear increments when the sub gear crosses 7.

6.6.8.31 ATBCTL0 Register (Offset = 100h) [Reset = 00000000h]

ATBCTL0 is shown in Table 6-137.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-137. ATBCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	SEL	R/W	Xh	Internal. Only to be used through TI provided API.

6.6.8.32 ATBCTL1 Register (Offset = 104h) [Reset = 00000000h]

ATBCTL1 is shown in Table 6-138.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-138. ATBCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	BGAP	R/W	0h	Internal. Only to be used through TI provided API.
17-15	AFOSC	R/W	0h	Internal. Only to be used through TI provided API.
14-13	LFOSC	R/W	0h	Internal. Only to be used through TI provided API.
12	NABIAS	R/W	0h	Internal. Only to be used through TI provided API.
11	RESERVED	R	0h	Reserved
10	LFXT	R/W	0h	Internal. Only to be used through TI provided API.
9-8	LFMON	R/W	0h	Internal. Only to be used through TI provided API.
7	HFXT	R/W	0h	Internal. Only to be used through TI provided API.
6-3	RESERVED	R	0h	Reserved
2-0	HFOSC	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.33 DTBCTL Register (Offset = 108h) [Reset = 00000000h]

DTBCTL is shown in Table 6-139.

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Digital test bus mux control

Table 6-139. DTBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-18	DSEL2	R/W	0h	Internal. Only to be used through TI provided API.
17-13	DSEL1	R/W	0h	Internal. Only to be used through TI provided API.
12-8	DSEL0	R/W	0h	Internal. Only to be used through TI provided API.
7-3	CLKSEL	R/W	0h	Select clock to output on DTB[0] 0h = Select CLKULL (24 MHz during ACTIVE, 32kHz during STANDBY) 1h = Select CLKSVT (48 MHz) 2h = Select CLKADC (48 MHz) 4h = Select tracking loop reference clock 7h = Select LFCLK (selected by LFCLKSEL.MAIN) Ah = Select HFOSC after qualification Ch = Select HFXT divided by 8 Dh = Select HFXT Eh = Select LFOSC Fh = Select LFXT 11h = Select AFOSC after qualification 12h = HFOSC div by 2 clock
2-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Enable DTB output

6.6.8.34 DTBCTL2 Register (Offset = 10Ch) [Reset = 00000000h]

DTBCTL2 is shown in Table 6-140.

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Digital test bus mux control

Table 6-140. DTBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-10	CLK2DTBSEL	R/W	0h	Select a DTB other than DTB0 to route the clock. Value of 0 indicates that clock 2 won't be sent to DTB.
9-8	RESERVED	R	0h	Reserved
7-5	CLKSEL2	R/W	0h	Select the clock that needs to be routed to a DTB other than DTB0 0h = Select CLKULL (24 MHz during ACTIVE, 32kHz during STANDBY) 1h = Select CLKSVT (48 MHz)
4-3	RESERVED	R	0h	Reserved
2-1	CLK2DIVVAL	R/W	0h	These bits are used to configure the divider value. 0h = Divide by 2 1h = Divide by 4 2h = Divide by 8 3h = Divide by 16
0	CLK2DIVEN	R/W	0h	Enable divider on second clock path 0h = Disable 1h = Enable

6.6.8.35 TRIM0 Register (Offset = 110h) [Reset = 00000000h]

TRIM0 is shown in Table 6-141.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-141. TRIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	AFOSC_MODE	R/W	0h	Internal. Only to be used through TI provided API.
24-21	AFOSC_MID	R/W	0h	Internal. Only to be used through TI provided API.
20-16	AFOSC_COARSE	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9	HFOSC_MODE	R/W	0h	Internal. Only to be used through TI provided API.
8-5	HFOSC_MID	R/W	0h	Internal. Only to be used through TI provided API.
4-0	HFOSC_COARSE	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.36 TRIM1 Register (Offset = 114h) [Reset = 00000000h]

TRIM1 is shown in Table 6-142.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-142. TRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	HFXTSLICER	R/W	0h	Internal. Only to be used through TI provided API.
29-28	PEAKIBIAS	R/W	0h	Internal. Only to be used through TI provided API.
27	NABIAS_UDIGLDO	R/W	1h	Internal. Only to be used through TI provided API.
26-24	LDOBW	R/W	0h	Internal. Only to be used through TI provided API.
23-20	LDOFB	R/W	6h	Internal. Only to be used through TI provided API.
19-16	LFDLY	R/W	Fh	Internal. Only to be used through TI provided API.
15	NABIAS_LFOSC	R/W	1h	Internal. Only to be used through TI provided API.
14-8	NABIAS_RES	R/W	14h	Internal. Only to be used through TI provided API.
7-0	LFOSC_CAP	R/W	39h	Internal. Only to be used through TI provided API.

6.6.8.37 HFXTINIT Register (Offset = 118h) [Reset = 00000000h]

HFXTINIT is shown in Table 6-143.

Return to the Summary Table.

Initial values for HFXT ramping

Table 6-143. HFXTINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-23	AMPTHR	R/W	28h	Amplitude threshold during HFXT ramping
22-16	IDAC	R/W	7Fh	Initial HFXT IDAC current
15-12	IREF	R/W	8h	Initial HFXT IREF current

Table 6-143. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	Q2CAP	R/W	0h	Initial HFXT Q2 cap trim 0h = Nominal 25C = 2.57E-12 F;Stong 25C = 1.50E-12 F;Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F;Stong 25C = 1.60E-12 F;Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F;Stong 25C = 1.69E-12 F;Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F;Stong 25C = 1.79E-12 F;Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F;Stong 25C = 1.89E-12 F;Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F;Stong 25C = 1.99E-12 F;Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F;Stong 25C = 2.09E-12 F;Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F;Stong 25C = 2.19E-12 F;Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F;Stong 25C = 2.29E-12 F;Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F;Stong 25C = 2.39E-12 F;Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F;Stong 25C = 2.49E-12 F;Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F;Stong 25C = 2.59E-12 F;Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F;Stong 25C = 2.69E-12 F;Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F;Stong 25C = 2.79E-12 F;Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F;Stong 25C = 2.89E-12 F;Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F;Stong 25C = 3.11E-12 F;Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F;Stong 25C = 3.23E-12 F;Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F;Stong 25C = 3.36E-12 F;Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F;Stong 25C = 3.48E-12 F;Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F;Stong 25C = 3.60E-12 F;Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F;Stong 25C = 3.73E-12 F;Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F;Stong 25C = 3.85E-12 F;Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F;Stong 25C = 3.97E-12 F;Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F;Stong 25C = 4.09E-12 F;Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F;Stong 25C = 4.21E-12 F;Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F;Stong 25C = 4.32E-12 F;Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F;Stong 25C = 4.44E-12 F;Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F;Stong 25C = 4.56E-12 F;Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F;Stong 25C = 4.67E-12 F;Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F;Stong 25C = 4.79E-12 F;Weak 25C = 6.12E-12 F

Table 6-143. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h = Nominal 25C = 5.97E-12 F;Stong 25C = 5.05E-12 F;Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F;Stong 25C = 5.20E-12 F;Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F;Stong 25C = 5.35E-12 F;Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F;Stong 25C = 5.49E-12 F;Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F;Stong 25C = 5.63E-12 F;Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F;Stong 25C = 5.78E-12 F;Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F;Stong 25C = 5.92E-12 F;Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F;Stong 25C = 6.06E-12 F;Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F;Stong 25C = 6.21E-12 F;Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F;Stong 25C = 6.35E-12 F;Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F;Stong 25C = 6.49E-12 F;Weak 25C = 7.98E-12 F 2Bh = Nominal 25C = 7.55E-12 F;Stong 25C = 6.63E-12 F;Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F;Stong 25C = 6.77E-12 F;Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F;Stong 25C = 6.91E-12 F;Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F;Stong 25C = 7.05E-12 F;Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F;Stong 25C = 7.38E-12 F;Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F;Stong 25C = 7.57E-12 F;Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F;Stong 25C = 7.76E-12 F;Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F;Stong 25C = 7.94E-12 F;Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F;Stong 25C = 8.13E-12 F;Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F;Stong 25C = 8.32E-12 F;Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F;Stong 25C = 8.51E-12 F;Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F;Stong 25C = 8.70E-12 F;Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F;Stong 25C = 8.89E-12 F;Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F;Stong 25C = 9.07E-12 F;Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F;Stong 25C = 9.26E-12 F;Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F;Stong 25C = 9.45E-12 F;Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F;Stong 25C = 9.64E-12 F;Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F;Stong 25C = 9.82E-12 F;Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F;Stong 25C = 1.00E-11 F;Weak 25C = 1.19E-11 F

Table 6-143. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Q1CAP	R/W	0h	Initial HFXT Q1 cap trim 0h = Nominal 25C = 2.57E-12 F;Stong 25C = 1.50E-12 F;Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F;Stong 25C = 1.60E-12 F;Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F;Stong 25C = 1.69E-12 F;Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F;Stong 25C = 1.79E-12 F;Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F;Stong 25C = 1.89E-12 F;Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F;Stong 25C = 1.99E-12 F;Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F;Stong 25C = 2.09E-12 F;Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F;Stong 25C = 2.19E-12 F;Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F;Stong 25C = 2.29E-12 F;Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F;Stong 25C = 2.39E-12 F;Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F;Stong 25C = 2.49E-12 F;Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F;Stong 25C = 2.59E-12 F;Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F;Stong 25C = 2.69E-12 F;Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F;Stong 25C = 2.79E-12 F;Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F;Stong 25C = 2.89E-12 F;Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F;Stong 25C = 3.11E-12 F;Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F;Stong 25C = 3.23E-12 F;Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F;Stong 25C = 3.36E-12 F;Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F;Stong 25C = 3.48E-12 F;Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F;Stong 25C = 3.60E-12 F;Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F;Stong 25C = 3.73E-12 F;Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F;Stong 25C = 3.85E-12 F;Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F;Stong 25C = 3.97E-12 F;Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F;Stong 25C = 4.09E-12 F;Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F;Stong 25C = 4.21E-12 F;Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F;Stong 25C = 4.32E-12 F;Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F;Stong 25C = 4.44E-12 F;Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F;Stong 25C = 4.56E-12 F;Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F;Stong 25C = 4.67E-12 F;Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F;Stong 25C = 4.79E-12 F;Weak 25C = 6.12E-12 F

Table 6-143. HFXTINIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h = Nominal 25C = 5.97E-12 F;Stong 25C = 5.05E-12 F;Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F;Stong 25C = 5.20E-12 F;Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F;Stong 25C = 5.35E-12 F;Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F;Stong 25C = 5.49E-12 F;Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F;Stong 25C = 5.63E-12 F;Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F;Stong 25C = 5.78E-12 F;Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F;Stong 25C = 5.92E-12 F;Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F;Stong 25C = 6.06E-12 F;Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F;Stong 25C = 6.21E-12 F;Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F;Stong 25C = 6.35E-12 F;Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F;Stong 25C = 6.49E-12 F;Weak 25C = 7.98E-12 F 2Bh = Nominal 25C = 7.55E-12 F;Stong 25C = 6.63E-12 F;Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F;Stong 25C = 6.77E-12 F;Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F;Stong 25C = 6.91E-12 F;Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F;Stong 25C = 7.05E-12 F;Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F;Stong 25C = 7.38E-12 F;Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F;Stong 25C = 7.57E-12 F;Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F;Stong 25C = 7.76E-12 F;Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F;Stong 25C = 7.94E-12 F;Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F;Stong 25C = 8.13E-12 F;Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F;Stong 25C = 8.32E-12 F;Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F;Stong 25C = 8.51E-12 F;Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F;Stong 25C = 8.70E-12 F;Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F;Stong 25C = 8.89E-12 F;Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F;Stong 25C = 9.07E-12 F;Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F;Stong 25C = 9.26E-12 F;Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F;Stong 25C = 9.45E-12 F;Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F;Stong 25C = 9.64E-12 F;Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F;Stong 25C = 9.82E-12 F;Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F;Stong 25C = 1.00E-11 F;Weak 25C = 1.19E-11 F

6.6.8.38 HFXTTARG Register (Offset = 11Ch) [Reset = 00000000h]

HFXTTARG is shown in Table 6-144.

Return to the Summary Table.

Target values for HFXT ramping

Table 6-144. HFXTTARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	AMPHYST	R/W	1h	ADC hysteresis used during IDAC updates.;Every AMPCFG1.INTERVAL, IDAC will be regulated;- up as long as ADC < AMPTHR;- down as long as ADC > AMPTHR+AMPHYST
29-23	AMPTHR	R/W	28h	Minimum HFXT amplitude
22-16	IDAC	R/W	46h	Minimum IDAC current
15-12	IREF	R/W	4h	Target HFXT IREF current

Table 6-144. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	Q2CAP	R/W	2Dh	Target HFXT Q2 cap trim 0h = Nominal 25C = 2.57E-12 F;Stong 25C = 1.50E-12 F;Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F;Stong 25C = 1.60E-12 F;Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F;Stong 25C = 1.69E-12 F;Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F;Stong 25C = 1.79E-12 F;Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F;Stong 25C = 1.89E-12 F;Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F;Stong 25C = 1.99E-12 F;Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F;Stong 25C = 2.09E-12 F;Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F;Stong 25C = 2.19E-12 F;Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F;Stong 25C = 2.29E-12 F;Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F;Stong 25C = 2.39E-12 F;Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F;Stong 25C = 2.49E-12 F;Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F;Stong 25C = 2.59E-12 F;Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F;Stong 25C = 2.69E-12 F;Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F;Stong 25C = 2.79E-12 F;Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F;Stong 25C = 2.89E-12 F;Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F;Stong 25C = 3.11E-12 F;Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F;Stong 25C = 3.23E-12 F;Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F;Stong 25C = 3.36E-12 F;Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F;Stong 25C = 3.48E-12 F;Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F;Stong 25C = 3.60E-12 F;Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F;Stong 25C = 3.73E-12 F;Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F;Stong 25C = 3.85E-12 F;Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F;Stong 25C = 3.97E-12 F;Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F;Stong 25C = 4.09E-12 F;Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F;Stong 25C = 4.21E-12 F;Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F;Stong 25C = 4.32E-12 F;Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F;Stong 25C = 4.44E-12 F;Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F;Stong 25C = 4.56E-12 F;Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F;Stong 25C = 4.67E-12 F;Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F;Stong 25C = 4.79E-12 F;Weak 25C = 6.12E-12 F

Table 6-144. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h = Nominal 25C = 5.97E-12 F;Stong 25C = 5.05E-12 F;Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F;Stong 25C = 5.20E-12 F;Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F;Stong 25C = 5.35E-12 F;Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F;Stong 25C = 5.49E-12 F;Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F;Stong 25C = 5.63E-12 F;Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F;Stong 25C = 5.78E-12 F;Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F;Stong 25C = 5.92E-12 F;Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F;Stong 25C = 6.06E-12 F;Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F;Stong 25C = 6.21E-12 F;Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F;Stong 25C = 6.35E-12 F;Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F;Stong 25C = 6.49E-12 F;Weak 25C = 7.98E-12 F 2Bh = Nominal 25C = 7.55E-12 F;Stong 25C = 6.63E-12 F;Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F;Stong 25C = 6.77E-12 F;Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F;Stong 25C = 6.91E-12 F;Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F;Stong 25C = 7.05E-12 F;Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F;Stong 25C = 7.38E-12 F;Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F;Stong 25C = 7.57E-12 F;Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F;Stong 25C = 7.76E-12 F;Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F;Stong 25C = 7.94E-12 F;Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F;Stong 25C = 8.13E-12 F;Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F;Stong 25C = 8.32E-12 F;Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F;Stong 25C = 8.51E-12 F;Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F;Stong 25C = 8.70E-12 F;Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F;Stong 25C = 8.89E-12 F;Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F;Stong 25C = 9.07E-12 F;Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F;Stong 25C = 9.26E-12 F;Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F;Stong 25C = 9.45E-12 F;Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F;Stong 25C = 9.64E-12 F;Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F;Stong 25C = 9.82E-12 F;Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F;Stong 25C = 1.00E-11 F;Weak 25C = 1.19E-11 F

Table 6-144. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Q1CAP	R/W	2Dh	Target HFXT Q1 cap trim 0h = Nominal 25C = 2.57E-12 F;Stong 25C = 1.50E-12 F;Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F;Stong 25C = 1.60E-12 F;Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F;Stong 25C = 1.69E-12 F;Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F;Stong 25C = 1.79E-12 F;Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F;Stong 25C = 1.89E-12 F;Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F;Stong 25C = 1.99E-12 F;Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F;Stong 25C = 2.09E-12 F;Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F;Stong 25C = 2.19E-12 F;Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F;Stong 25C = 2.29E-12 F;Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F;Stong 25C = 2.39E-12 F;Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F;Stong 25C = 2.49E-12 F;Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F;Stong 25C = 2.59E-12 F;Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F;Stong 25C = 2.69E-12 F;Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F;Stong 25C = 2.79E-12 F;Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F;Stong 25C = 2.89E-12 F;Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F;Stong 25C = 3.11E-12 F;Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F;Stong 25C = 3.23E-12 F;Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F;Stong 25C = 3.36E-12 F;Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F;Stong 25C = 3.48E-12 F;Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F;Stong 25C = 3.60E-12 F;Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F;Stong 25C = 3.73E-12 F;Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F;Stong 25C = 3.85E-12 F;Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F;Stong 25C = 3.97E-12 F;Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F;Stong 25C = 4.09E-12 F;Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F;Stong 25C = 4.21E-12 F;Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F;Stong 25C = 4.32E-12 F;Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F;Stong 25C = 4.44E-12 F;Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F;Stong 25C = 4.56E-12 F;Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F;Stong 25C = 4.67E-12 F;Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F;Stong 25C = 4.79E-12 F;Weak 25C = 6.12E-12 F

Table 6-144. HFXTTARG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h = Nominal 25C = 5.97E-12 F;Stong 25C = 5.05E-12 F;Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F;Stong 25C = 5.20E-12 F;Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F;Stong 25C = 5.35E-12 F;Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F;Stong 25C = 5.49E-12 F;Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F;Stong 25C = 5.63E-12 F;Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F;Stong 25C = 5.78E-12 F;Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F;Stong 25C = 5.92E-12 F;Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F;Stong 25C = 6.06E-12 F;Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F;Stong 25C = 6.21E-12 F;Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F;Stong 25C = 6.35E-12 F;Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F;Stong 25C = 6.49E-12 F;Weak 25C = 7.98E-12 F 2Bh = Nominal 25C = 7.55E-12 F;Stong 25C = 6.63E-12 F;Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F;Stong 25C = 6.77E-12 F;Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F;Stong 25C = 6.91E-12 F;Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F;Stong 25C = 7.05E-12 F;Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F;Stong 25C = 7.38E-12 F;Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F;Stong 25C = 7.57E-12 F;Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F;Stong 25C = 7.76E-12 F;Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F;Stong 25C = 7.94E-12 F;Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F;Stong 25C = 8.13E-12 F;Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F;Stong 25C = 8.32E-12 F;Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F;Stong 25C = 8.51E-12 F;Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F;Stong 25C = 8.70E-12 F;Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F;Stong 25C = 8.89E-12 F;Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F;Stong 25C = 9.07E-12 F;Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F;Stong 25C = 9.26E-12 F;Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F;Stong 25C = 9.45E-12 F;Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F;Stong 25C = 9.64E-12 F;Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F;Stong 25C = 9.82E-12 F;Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F;Stong 25C = 1.00E-11 F;Weak 25C = 1.19E-11 F

6.6.8.39 HFXTDYN Register (Offset = 120h) [Reset = 00000000h]

HFXTDYN is shown in Table 6-145.

Return to the Summary Table.

Alternative target values for HFXT configuration;Software can change these values to dynamically transition the HFXT configuration while HFXT is running.;Set SEL to select the alternative set of target values.

Table 6-145. HFXTDYN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEL	R/W	0h	Select the dynamic configuration.;Amplitude ramping will always happen using the values in HFXTINIT, and HFXTTARG.;Afterwards, this bit can be used to select between HFXTTARG and HFXTDYN.;Hardware will ensure a smooth transition of analog control signals. 0h = Select configuration in CKM.HFXTTARG0 and CKM.HFXTTARG1. 1h = Select configuration in CKM.HFXTDYN0 and CKM.HFXTDYN1.
30	RESERVED	R	0h	Reserved
29-23	AMPTHR	R/W	28h	Minimum HFXT amplitude
22-16	IDAC	R/W	46h	Minimum IDAC current
15-12	IREF	R/W	4h	Target HFXT IREF current

Table 6-145. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	Q2CAP	R/W	2Dh	Target HFXT Q2 cap trim 0h = Nominal 25C = 2.57E-12 F;Stong 25C = 1.50E-12 F;Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F;Stong 25C = 1.60E-12 F;Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F;Stong 25C = 1.69E-12 F;Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F;Stong 25C = 1.79E-12 F;Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F;Stong 25C = 1.89E-12 F;Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F;Stong 25C = 1.99E-12 F;Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F;Stong 25C = 2.09E-12 F;Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F;Stong 25C = 2.19E-12 F;Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F;Stong 25C = 2.29E-12 F;Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F;Stong 25C = 2.39E-12 F;Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F;Stong 25C = 2.49E-12 F;Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F;Stong 25C = 2.59E-12 F;Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F;Stong 25C = 2.69E-12 F;Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F;Stong 25C = 2.79E-12 F;Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F;Stong 25C = 2.89E-12 F;Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F;Stong 25C = 3.11E-12 F;Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F;Stong 25C = 3.23E-12 F;Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F;Stong 25C = 3.36E-12 F;Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F;Stong 25C = 3.48E-12 F;Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F;Stong 25C = 3.60E-12 F;Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F;Stong 25C = 3.73E-12 F;Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F;Stong 25C = 3.85E-12 F;Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F;Stong 25C = 3.97E-12 F;Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F;Stong 25C = 4.09E-12 F;Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F;Stong 25C = 4.21E-12 F;Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F;Stong 25C = 4.32E-12 F;Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F;Stong 25C = 4.44E-12 F;Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F;Stong 25C = 4.56E-12 F;Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F;Stong 25C = 4.67E-12 F;Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F;Stong 25C = 4.79E-12 F;Weak 25C = 6.12E-12 F

Table 6-145. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h = Nominal 25C = 5.97E-12 F;Stong 25C = 5.05E-12 F;Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F;Stong 25C = 5.20E-12 F;Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F;Stong 25C = 5.35E-12 F;Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F;Stong 25C = 5.49E-12 F;Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F;Stong 25C = 5.63E-12 F;Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F;Stong 25C = 5.78E-12 F;Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F;Stong 25C = 5.92E-12 F;Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F;Stong 25C = 6.06E-12 F;Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F;Stong 25C = 6.21E-12 F;Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F;Stong 25C = 6.35E-12 F;Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F;Stong 25C = 6.49E-12 F;Weak 25C = 7.98E-12 F 2Bh = Nominal 25C = 7.55E-12 F;Stong 25C = 6.63E-12 F;Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F;Stong 25C = 6.77E-12 F;Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F;Stong 25C = 6.91E-12 F;Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F;Stong 25C = 7.05E-12 F;Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F;Stong 25C = 7.38E-12 F;Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F;Stong 25C = 7.57E-12 F;Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F;Stong 25C = 7.76E-12 F;Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F;Stong 25C = 7.94E-12 F;Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F;Stong 25C = 8.13E-12 F;Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F;Stong 25C = 8.32E-12 F;Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F;Stong 25C = 8.51E-12 F;Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F;Stong 25C = 8.70E-12 F;Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F;Stong 25C = 8.89E-12 F;Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F;Stong 25C = 9.07E-12 F;Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F;Stong 25C = 9.26E-12 F;Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F;Stong 25C = 9.45E-12 F;Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F;Stong 25C = 9.64E-12 F;Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F;Stong 25C = 9.82E-12 F;Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F;Stong 25C = 1.00E-11 F;Weak 25C = 1.19E-11 F

Table 6-145. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Q1CAP	R/W	2Dh	Target HFXT Q1 cap trim 0h = Nominal 25C = 2.57E-12 F;Stong 25C = 1.50E-12 F;Weak 25C = 2.69E-12 F 1h = Nominal 25C = 2.66E-12 F;Stong 25C = 1.60E-12 F;Weak 25C = 2.79E-12 F 2h = Nominal 25C = 2.76E-12 F;Stong 25C = 1.69E-12 F;Weak 25C = 2.89E-12 F 3h = Nominal 25C = 2.85E-12 F;Stong 25C = 1.79E-12 F;Weak 25C = 2.99E-12 F 4h = Nominal 25C = 2.95E-12 F;Stong 25C = 1.89E-12 F;Weak 25C = 3.09E-12 F 5h = Nominal 25C = 3.04E-12 F;Stong 25C = 1.99E-12 F;Weak 25C = 3.19E-12 F 6h = Nominal 25C = 3.14E-12 F;Stong 25C = 2.09E-12 F;Weak 25C = 3.30E-12 F 7h = Nominal 25C = 3.23E-12 F;Stong 25C = 2.19E-12 F;Weak 25C = 3.40E-12 F 8h = Nominal 25C = 3.33E-12 F;Stong 25C = 2.29E-12 F;Weak 25C = 3.50E-12 F 9h = Nominal 25C = 3.42E-12 F;Stong 25C = 2.39E-12 F;Weak 25C = 3.60E-12 F Ah = Nominal 25C = 3.51E-12 F;Stong 25C = 2.49E-12 F;Weak 25C = 3.70E-12 F Bh = Nominal 25C = 3.61E-12 F;Stong 25C = 2.59E-12 F;Weak 25C = 3.80E-12 F Ch = Nominal 25C = 3.70E-12 F;Stong 25C = 2.69E-12 F;Weak 25C = 3.90E-12 F Dh = Nominal 25C = 3.79E-12 F;Stong 25C = 2.79E-12 F;Weak 25C = 4.00E-12 F Eh = Nominal 25C = 3.88E-12 F;Stong 25C = 2.89E-12 F;Weak 25C = 4.10E-12 F Fh = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 10h = Nominal 25C = 3.97E-12 F;Stong 25C = 2.98E-12 F;Weak 25C = 4.20E-12 F 11h = Nominal 25C = 4.09E-12 F;Stong 25C = 3.11E-12 F;Weak 25C = 4.33E-12 F 12h = Nominal 25C = 4.21E-12 F;Stong 25C = 3.23E-12 F;Weak 25C = 4.46E-12 F 13h = Nominal 25C = 4.33E-12 F;Stong 25C = 3.36E-12 F;Weak 25C = 4.59E-12 F 14h = Nominal 25C = 4.45E-12 F;Stong 25C = 3.48E-12 F;Weak 25C = 4.72E-12 F 15h = Nominal 25C = 4.57E-12 F;Stong 25C = 3.60E-12 F;Weak 25C = 4.85E-12 F 16h = Nominal 25C = 4.68E-12 F;Stong 25C = 3.73E-12 F;Weak 25C = 4.98E-12 F 17h = Nominal 25C = 4.80E-12 F;Stong 25C = 3.85E-12 F;Weak 25C = 5.10E-12 F 18h = Nominal 25C = 4.91E-12 F;Stong 25C = 3.97E-12 F;Weak 25C = 5.23E-12 F 19h = Nominal 25C = 5.03E-12 F;Stong 25C = 4.09E-12 F;Weak 25C = 5.36E-12 F 1Ah = Nominal 25C = 5.15E-12 F;Stong 25C = 4.21E-12 F;Weak 25C = 5.49E-12 F 1Bh = Nominal 25C = 5.26E-12 F;Stong 25C = 4.32E-12 F;Weak 25C = 5.61E-12 F 1Ch = Nominal 25C = 5.37E-12 F;Stong 25C = 4.44E-12 F;Weak 25C = 5.74E-12 F 1Dh = Nominal 25C = 5.49E-12 F;Stong 25C = 4.56E-12 F;Weak 25C = 5.87E-12 F 1Eh = Nominal 25C = 5.60E-12 F;Stong 25C = 4.67E-12 F;Weak 25C = 5.99E-12 F 1Fh = Nominal 25C = 5.72E-12 F;Stong 25C = 4.79E-12 F;Weak 25C = 6.12E-12 F

Table 6-145. HFXTDYN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h = Nominal 25C = 5.97E-12 F;Stong 25C = 5.05E-12 F;Weak 25C = 6.40E-12 F 21h = Nominal 25C = 6.12E-12 F;Stong 25C = 5.20E-12 F;Weak 25C = 6.56E-12 F 22h = Nominal 25C = 6.26E-12 F;Stong 25C = 5.35E-12 F;Weak 25C = 6.72E-12 F 23h = Nominal 25C = 6.41E-12 F;Stong 25C = 5.49E-12 F;Weak 25C = 6.88E-12 F 24h = Nominal 25C = 6.55E-12 F;Stong 25C = 5.63E-12 F;Weak 25C = 7.04E-12 F 25h = Nominal 25C = 6.69E-12 F;Stong 25C = 5.78E-12 F;Weak 25C = 7.20E-12 F 26h = Nominal 25C = 6.84E-12 F;Stong 25C = 5.92E-12 F;Weak 25C = 7.35E-12 F 27h = Nominal 25C = 6.98E-12 F;Stong 25C = 6.06E-12 F;Weak 25C = 7.51E-12 F 28h = Nominal 25C = 7.12E-12 F;Stong 25C = 6.21E-12 F;Weak 25C = 7.67E-12 F 29h = Nominal 25C = 7.26E-12 F;Stong 25C = 6.35E-12 F;Weak 25C = 7.82E-12 F 2Ah = Nominal 25C = 7.40E-12 F;Stong 25C = 6.49E-12 F;Weak 25C = 7.98E-12 F 2Bh = Nominal 25C = 7.55E-12 F;Stong 25C = 6.63E-12 F;Weak 25C = 8.13E-12 F 2Ch = Nominal 25C = 7.69E-12 F;Stong 25C = 6.77E-12 F;Weak 25C = 8.29E-12 F 2Dh = Nominal 25C = 7.83E-12 F;Stong 25C = 6.91E-12 F;Weak 25C = 8.44E-12 F 2Eh = Nominal 25C = 7.97E-12 F;Stong 25C = 7.05E-12 F;Weak 25C = 8.60E-12 F 2Fh = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 30h = Nominal 25C = 8.10E-12 F;Stong 25C = 7.18E-12 F;Weak 25C = 8.75E-12 F 31h = Nominal 25C = 8.30E-12 F;Stong 25C = 7.38E-12 F;Weak 25C = 8.96E-12 F 32h = Nominal 25C = 8.49E-12 F;Stong 25C = 7.57E-12 F;Weak 25C = 9.18E-12 F 33h = Nominal 25C = 8.69E-12 F;Stong 25C = 7.76E-12 F;Weak 25C = 9.39E-12 F 34h = Nominal 25C = 8.88E-12 F;Stong 25C = 7.94E-12 F;Weak 25C = 9.60E-12 F 35h = Nominal 25C = 9.07E-12 F;Stong 25C = 8.13E-12 F;Weak 25C = 9.81E-12 F 36h = Nominal 25C = 9.26E-12 F;Stong 25C = 8.32E-12 F;Weak 25C = 1.00E-11 F 37h = Nominal 25C = 9.46E-12 F;Stong 25C = 8.51E-12 F;Weak 25C = 1.02E-11 F 38h = Nominal 25C = 9.65E-12 F;Stong 25C = 8.70E-12 F;Weak 25C = 1.04E-11 F 39h = Nominal 25C = 9.84E-12 F;Stong 25C = 8.89E-12 F;Weak 25C = 1.07E-11 F 3Ah = Nominal 25C = 1.00E-11 F;Stong 25C = 9.07E-12 F;Weak 25C = 1.09E-11 F 3Bh = Nominal 25C = 1.02E-11 F;Stong 25C = 9.26E-12 F;Weak 25C = 1.11E-11 F 3Ch = Nominal 25C = 1.04E-11 F;Stong 25C = 9.45E-12 F;Weak 25C = 1.13E-11 F 3Dh = Nominal 25C = 1.06E-11 F;Stong 25C = 9.64E-12 F;Weak 25C = 1.15E-11 F 3Eh = Nominal 25C = 1.08E-11 F;Stong 25C = 9.82E-12 F;Weak 25C = 1.17E-11 F 3Fh = Nominal 25C = 1.10E-11 F;Stong 25C = 1.00E-11 F;Weak 25C = 1.19E-11 F

6.6.8.40 AMPCFG0 Register (Offset = 124h) [Reset = 00000000h]

AMPCFG0 is shown in Table 6-146.

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Amplitude Compensation Configuration 0

Table 6-146. AMPCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Q2DLY	R/W	0h	Q2CAP change delay.;Number of clock cycles to wait before changing Q2CAP by one step.;Clock frequency defined in FSMRATE.
27-24	Q1DLY	R/W	0h	Q1CAP change delay.;Number of clock cycles to wait before changing Q1CAP by one step.;Clock frequency defined in FSMRATE.
23-20	ADCDLY	R/W	3h	ADC and PEAKDET startup time.;Number of clock cycles to wait after enabling the PEAKDET and ADC before the first measurement.;Clock frequency defined in FSMRATE.
19-15	LDOSTART	R/W	1Fh	LDO startup time.;Number of clock cycles to bypass the LDO resistors for faster startup.;Clock frequency defined in FSMRATE.
14-10	INJWAIT	R/W	2h	Inject HFOSC for faster HFXT startup.;This value specifies the number of clock cycles to wait after injection is done.;The clock speed is defined in FSMRATE.
9-5	INJTIME	R/W	4h	Inject HFOSC for faster HFXT startup.;This value specifies the number of clock cycles the injection is enabled.;The clock speed is defined in FSMRATE.;Set to 0 to disable injection.
4-0	FSMRATE	R/W	2h	Update rate for the AMPCOMP update rate.;Also affects the clock rate for the Amplitude ADC.;The update rate is 6MHz / (FSMRATE+1). 0h = 6 MHz 1h = 3 MHz 2h = 2 MHz 5h = 1 MHz Bh = 500 kHz 17h = 250 kHz

6.6.8.41 AMPCFG1 Register (Offset = 128h) [Reset = 00000000h]

AMPCFG1 is shown in Table 6-147.

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Amplitude Compensation Configuration 1

Table 6-147. AMPCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	IDACDLY	R/W	2h	IDAC change delay.;Time to wait before changing IDAC by one step.;This time needs to be long enough for the crystal to settle.;The number of clock cycles to wait is IDACDLY<<4 + 15.;Clock frequency defined in AMPCFG0.FSMRATE.
27-24	IREFDLY	R/W	6h	IREF change delay.;Number of clock cycles to wait before changing IREF by one step.;Clock frequency defined in AMPCFG0.FSMRATE.
23-12	BIASLT	R/W	FFh	Lifetime of the amplitude ADC bias value.;This value specifies the number of adjustment intervals,;until the ADC bias value has to be measured again.;Set to 0 to disable automatic bias measurements.
11-0	INTERVAL	R/W	FFh	Interval for amplitude adjustments.;Set to 0 to disable periodic adjustments.;This value specifies the number of clock cycles between adjustments.;The clock speed is defined in AMPCFG0.FSMRATE.

6.6.8.42 LOOPCFG Register (Offset = 12Ch) [Reset = 00000000h]

LOOPCFG is shown in Table 6-148.

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Configuration Register for the Tracking Loop

Table 6-148. LOOPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	FINETRIM_INIT	R/W	18h	Initial value for the resistor fine trim
25-21	BOOST_TARGET	R/W	2h	Error-updates for 4xBOOST_TARGET times using KI_BOOST/ KP_BOOST, before using KI/KP.;Note: If boost is used for long duration using large values of KI_BOOST and KP_BOOST, the oscillator frequency can reach well above the max frequence limit of the design, causing unexpected behaviour.
20-18	KP_BOOST	R/W	7h	Proportional loop coefficient during BOOST
17-15	KI_BOOST	R/W	4h	Integral loop coefficient during BOOST
14-10	SETTLED_TARGET	R/W	13h	Number of HFOSC tracking loop updates before HFOSC is considered "settled". The tracking loop updates at a rough frequency of (2*Reference frequency/256).;If the reference frequency is 48MHz, the loop update frequency comes out to be 375Khz.;Internally the MMR is multiplied by 4
9-6	OOR_LIMIT	R/W	Eh	Out-of-range threshold. OOR_LIMIT is compared with absolute value of 5 MSB bits of loop filter error.
5-3	KP	R/W	6h	Proportional loop coefficient
2-0	KI	R/W	2h	Integral loop coefficient

6.6.8.43 LOOPCFG1 Register (Offset = 130h) [Reset = 00000000h]

LOOPCFG1 is shown in Table 6-149.

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Configuration Register for underclocking HFOSC

Table 6-149. LOOPCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	SETTLEIRQ	R/W	0h	Configuration to enable the interrupt when the HFOSC tracking loop has settled. The interrupt will be based on LOOPCFG.SETTLED_TARGET. 0h = Disable the interrupt to indicate that HFOSC tracking loop has settled. 1h = Enable the interrupt to indicate that HFOSC tracking loop has settled.
24-6	UNDERCLKCNT	R/W	Xh	Timer to trigger HFOSC underclocking. The timer will run at approximately 32.768 KHz.
5-0	KIOFF	R/W	3Fh	Based on HFTRACKCTRL.UNDERCLK configuration, after an event is triggerred, KI of the HFOSC tracking loop will be reduced by this amount.

6.6.8.44 AFOSCCTL Register (Offset = 140h) [Reset = 00000000h]

AFOSCCTL is shown in Table 6-150.

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Audio frequency oscillator control

Table 6-150. AFOSCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PW	W	0h	Password protection for QUALBYP.;Write this field to 0xA5 to accept writes to QUALBYP.
23-3	RESERVED	R	0h	Reserved
2	AUTODIS	R/W	0h	If set, AFOSC can be disabled by PMCTL upon standby entry. EN bit will be overriden with a value 0 and user has to manually re-enable AFOSC.
1	QUALBYP	R/W	0h	Clock qualification bypass.;AFOSC qualification will skip a fixed number of clock cycles to prevent glitches ;or frequency overshoots from reaching the system. Setting this bit will bypass the qualification.;This bit can be locked in SYS0. If unlocked, it is password protected with PW.
0	EN	R/W	0h	Enable AFOSC.

6.6.8.45 AFTRACKCTL Register (Offset = 144h) [Reset = 00000000h]

AFTRACKCTL is shown in Table 6-151.

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Audio frequency tracking loop control

Table 6-151. AFTRACKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable tracking loop.
30	DSMBYP	R/W	0h	Bypass Delta-Sigma-Modulation of fine trim.
29-0	RATIO	R/W	0999999Ah	Ratio. Ratio format is 0b.30b 07D6343Fh = 131478591 088190ACh = 142708908 08EE23B9h = 149824441 0999999Ah = 161061274 09B8B578h = 163100024

6.6.8.46 BANDGAPCTL Register (Offset = 148h) [Reset = 00000000h]

BANDGAPCTL is shown in Table 6-152.

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Internal. Only to be used through TI provided API.

Table 6-152. BANDGAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BGOVR	R/W	0h	Internal. Only to be used through TI provided API.
30-4	RESERVED	R	0h	Reserved
3	VBGAPBYP	R/W	0h	Internal. Only to be used through TI provided API.
2	VBGAPREFEN	R/W	0h	Internal. Only to be used through TI provided API.
1	VDDRREFEN	R/W	0h	Internal. Only to be used through TI provided API.
0	REFEN	R/W	0h	Internal. Only to be used through TI provided API.

6.6.8.47 AFCLKSEL Register (Offset = 150h) [Reset = 00000000h]

AFCLKSEL is shown in Table 6-153.

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Audio clock selection

Table 6-153. AFCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	SRC	R/W	0h	Select audio frequency clock source;Software should make sure that proper clock is selected before enabling the audio IP. 0h = Clock disabled 1h = AFOSC clock 2h = 96MHz CLKHF 3h = 48MHz reference clock (HFXT) 4h = External clock

6.6.8.48 CANCLKSEL Register (Offset = 154h) [Reset = 00000000h]

CANCLKSEL is shown in Table 6-154.

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CAN clock selection

Table 6-154. CANCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SRC	R/W	0h	Select audio frequency clock source;Software should make sure that proper clock is selected before enabling the audio IP. 0h = Clock disabled 1h = AFOSC clock 2h = 96MHz CLKHF

6.6.8.49 TRACKSTATAF Register (Offset = 160h) [Reset = 00000000h]

TRACKSTATAF is shown in Table 6-155.

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AF tracking loop status information

Table 6-155. TRACKSTATAF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOOPERRVLD	R	0h	Current AFOSC tracking error valid;This bit is one if the tracking loop is running and the error value is valid.
30	RESERVED	R	0h	Reserved
29-16	LOOPERR	R	0h	Current AFOSC tracking error;This field uses the internal fractional representation (sign, 9 integer bits, 4 fractional bits).;The actual fine trim value of format (sign, 9 integer bits, 30 fractional bits) is saturated to (sign, 9 integer bits, 4 fractional bits).
15-13	RESERVED	R	0h	Reserved
12-0	FINETRIM	R	1D80h	Current AFOSC Fine-trim value;This field uses the internal fractional representation (sign, 5 integer bits, 7 fractional bits).;The actual fine trim value of format (sign, 5 integer bits, 19 fractional bits) is saturated to (sign, 5 integer bits, 7 fractional bits).;The actual trim value applied to the oscillator is delta-sigma modulated 6 bits non-signed;(inverted sign bit + integer bits).

6.6.8.50 TRACKSTATAF1 Register (Offset = 164h) [Reset = 00000000h]

TRACKSTATAF1 is shown in Table 6-156.

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AF tracking loop status information

Table 6-156. TRACKSTATAF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-0	LOOPERR	R	0h	Current AFOSC tracking error;This field uses the fractional representation of the actual error(30 fractional bits). The actual error is of format (sign, 9 integer bits, 30 fractional bits).

6.6.8.51 TRACKSTATAF2 Register (Offset = 168h) [Reset = 00000000h]

TRACKSTATAF2 is shown in Table 6-157.

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AF tracking loop status information

Table 6-157. TRACKSTATAF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24-0	FINETRIM	R	01D80000h	Current AFOSC Fine-trim value;This field uses the internal fractional representation (sign, 5 integer bits, 19 fractional bits).;The actual trim value applied to the oscillator is delta-sigma modulated 6 bits non-signed;(inverted sign bit + integer bits).

6.6.8.52 LOOPCFGAF Register (Offset = 170h) [Reset = 00000000h]

LOOPCFGAF is shown in Table 6-158.

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Configuration Register for the Audio frequency Tracking Loop

Table 6-158. LOOPCFGAF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	FINETRIM_INIT	R/W	Ch	Initial value for the resistor fine trim
25-21	BOOST_TARGET	R/W	2h	Number of error-updates using BOOST values, before using KI/KP
20-18	KP_BOOST	R/W	7h	Proportional loop coefficient during BOOST
17-15	KI_BOOST	R/W	4h	Integral loop coefficient during BOOST
14-10	SETTLED_TARGET	R/W	Ch	Number of updates before AFOSC is considered "settled"
9-6	OOR_LIMIT	R/W	Eh	Out-of-range threshold. Out-of-range threshold. OOR_LIMIT is compared with absolute value of 5 MSB bits of loop filter error.
5-3	KP	R/W	6h	Proportional loop coefficient
2-0	KI	R/W	3h	Integral loop coefficient

6.6.8.53 CTL Register (Offset = 200h) [Reset = 00000000h]

CTL is shown in Table 6-159.

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Control

Table 6-159. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CMD	W	0h	TDC commands. 0h = Clear [TDC.STAT.SAT], [TDC.STAT.DONE], and [TDC.RESULT.VALUE]. ;This is not needed as prerequisite for a measurement. Reliable clear is only guaranteed from IDLE state. 1h = Synchronous counter start.;The counter looks for the opposite edge of the selected start event before it starts to count when the selected edge occurs. This guarantees an edge-triggered start and is recommended for frequency measurements. 2h = Asynchronous counter start.;The counter starts to count when the start event is high. To achieve precise edge-to-edge measurements you must ensure that the start event is low for at least 420 ns after you write this command. 3h = Force TDC state machine back to IDLE state.;Never write this command while [TDC.STAT.STATE] equals CLR_CNT or WAIT_CLR_CNT_DONE.

6.6.8.54 STAT Register (Offset = 204h) [Reset = 00000000h]

STAT is shown in Table 6-160.

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Status

Table 6-160. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	SAT	R	0h	TDC measurement saturation flag.;0: Conversion has not saturated.;1: Conversion stopped due to saturation.;This field is cleared when a new measurement is started or when CLR_RESULT is written to [TDC.CTL.CMD].
6	DONE	R	0h	TDC measurement complete flag.;0: TDC measurement has not yet completed.;1: TDC measurement has completed.;This field clears when a new TDC measurement starts or when you write CLR_RESULT to [TDC.CTL.CMD].
5-0	STATE	R	6h	TDC state machine status. 0h = Current state is TDC_STATE_WAIT_START. ;The fast-counter circuit looks for the start condition. The state machine waits for the fast-counter to increment. 4h = Current state is TDC_STATE_WAIT_STARTSTOPCNTEN.;The fast-counter circuit looks for the start condition. The state machine waits for the fast-counter to increment. 6h = Current state is TDC_STATE_IDLE. ;This is the default state after reset and abortion. State will change when you write [TDC.CTL.CMD] to either RUN_SYNC_START or RUN. 7h = Current state is TDC_STATE_CLRCNT. The fast-counter circuit is reset. 8h = Current state is TDC_STATE_WAIT_STOP.;The state machine waits for the fast-counter circuit to stop. Ch = Current state is TDC_STATE_WAIT_STOPCNTDOWN.;The fast-counter circuit looks for the stop condition. It will ignore a number of stop events configured in [TDC.TRIGCNTLOAD.CNT]. Eh = Current state is TDC_STATE_GETRESULTS.;The state machine copies the counter value from the fast-counter circuit. Fh = Current state is TDC_STATE_POR. ;This is the reset state. 16h = Current state is TDC_STATE_WAIT_CLRCNT_DONE. ;The state machine waits for fast-counter circuit to finish reset. 1Eh = Current state is TDC_WAIT_STARTFALL. ;The fast-counter circuit waits for a falling edge on the start event. 2Eh = Current state is TDC_FORCESTOP.;You wrote ABORT to [TDC.CTL.CMD] to abort the TDC measurement.

6.6.8.55 RESULT Register (Offset = 208h) [Reset = 00000000h]

RESULT is shown in Table 6-161.

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Result;Result of last TDC conversion.

Table 6-161. RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R	2h	TDC conversion result.;The result of the TDC conversion is given in number of clock edges of the clock source selected in [IPSPECIFIC.CKM.TDCCLKSEL.REFCLK]. Both rising and falling edges are counted.;Note that [TDC.SATCFG.LIMIT] is given in periods, while VALUE is given in edges (periods*2).;If TDC counter saturates, VALUE is slightly higher than [TDC.SATCFG.LIMIT]*2, as it takes a non-zero time to stop the measurement. Hence, the maximum value of this field becomes slightly higher than 2^{31} (2^{30} periods*2) if you configure [TDC.SATCFG.LIMIT] to R30.

6.6.8.56 SATCFG Register (Offset = 20Ch) [Reset = 00000000h]

SATCFG is shown in Table 6-162.

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Saturation Configuration

Table 6-162. SATCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	LIMIT	R/W	0h	Saturation limit.;The flag [TDC.STAT.SAT] is set when the TDC counter saturates.;Note that this value is given in periods, while [TDC.RESULT.VALUE] is given in edges (periods*2).;Values not enumerated are not supported 0h = No saturation. An additional timer should be used to know if [TDC.RESULT.VALUE] rolled over. 3h = TDC conversion saturates and stops after 2^{12} periods. 4h = TDC conversion saturates and stops after 2^{13} periods. 5h = TDC conversion saturates and stops after 2^{14} periods. 6h = TDC conversion saturates and stops after 2^{15} periods. 7h = TDC conversion saturates and stops after 2^{16} periods. 8h = TDC conversion saturates and stops after 2^{17} periods. 9h = TDC conversion saturates and stops after 2^{18} periods. Ah = TDC conversion saturates and stops after 2^{19} periods. Bh = TDC conversion saturates and stops after 2^{20} periods. Ch = TDC conversion saturates and stops after 2^{21} periods. Dh = TDC conversion saturates and stops after 2^{22} periods. Eh = TDC conversion saturates and stops after 2^{23} periods. Fh = TDC conversion saturates and stops after 2^{24} periods. 10h = TDC conversion saturates and stops after 2^{25} periods. 11h = TDC conversion saturates and stops after 2^{26} periods. 12h = TDC conversion saturates and stops after 2^{27} periods. 13h = TDC conversion saturates and stops after 2^{28} periods. 14h = TDC conversion saturates and stops after 2^{29} periods. 15h = TDC conversion saturates and stops after 2^{30} periods.

6.6.8.57 TRIGSRC Register (Offset = 210h) [Reset = 00000000h]

TRIGSRC is shown in Table 6-163.

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Trigger Source;Select source and polarity for TDC start and stop events. See the Technical Reference Manual for event timing requirements.

Table 6-163. TRIGSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	STOP_POL	R/W	0h	Polarity of stop source.;Change only while [TDC.STAT.STATE] is IDLE. 0h = TDC conversion stops when high level is detected. 1h = TDC conversion stops when low level is detected.
14-13	RESERVED	R	0h	Reserved
12-8	STOP_SRC	R/W	0h	Select stop source from the asynchronous AUX event bus.;Change only while [TDC.STAT.STATE] is IDLE. 0h = LFTICK signal going to the RTC 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = Delayed version of selected LFCLK 4h = General purpose input signal 5h = Digital testbus bit 0 6h = Digital testbus bit 1 7h = Digital testbus bit 2 8h = Digital testbus bit 3 9h = Digital testbus bit 4 Ah = Digital testbus bit 5 Bh = Digital testbus bit 6 Ch = Digital testbus bit 7 Dh = Digital testbus bit 8 Eh = Digital testbus bit 9 Fh = Digital testbus bit 10 10h = Digital testbus bit 11 11h = Digital testbus bit 12 12h = Digital testbus bit 13 13h = Digital testbus bit 14 14h = Digital testbus bit 15 1Fh = Select TDC Prescaler event which is generated by configuration of TDC.PRECTL.
7	START_POL	R/W	0h	Polarity of start source.;Change only while [TDC.STAT.STATE] is IDLE. 0h = TDC conversion starts when high level is detected. 1h = TDC conversion starts when low level is detected.
6-5	RESERVED	R	0h	Reserved

Table 6-163. TRIGSRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	START_SRC	R/W	0h	Select start source from the asynchronous AUX event bus.;Change only while [TDC.STAT.STATE] is IDLE. 0h = LFTICK signal going to the RTC 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = Delayed version of selected LFCLK 4h = General purpose input signal 5h = Digital testbus bit 0 6h = Digital testbus bit 1 7h = Digital testbus bit 2 8h = Digital testbus bit 3 9h = Digital testbus bit 4 Ah = Digital testbus bit 5 Bh = Digital testbus bit 6 Ch = Digital testbus bit 7 Dh = Digital testbus bit 8 Eh = Digital testbus bit 9 Fh = Digital testbus bit 10 10h = Digital testbus bit 11 11h = Digital testbus bit 12 12h = Digital testbus bit 13 13h = Digital testbus bit 14 14h = Digital testbus bit 15 1Fh = Select TDC Prescaler event which is generated by configuration of TDC.PRECTL.

6.6.8.58 TRIGCNT Register (Offset = 214h) [Reset = 00000000h]

TRIGCNT is shown in Table 6-164.

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Trigger Counter;Stop-counter control and status.

Table 6-164. TRIGCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CNT	R/W	0h	Number of stop events to ignore when [TDC.TRIGCNTCFG.EN] is 1.;Read CNT to get the remaining number of stop events to ignore during a TDC measurement. ;Write CNT to update the remaining number of stop events to ignore during a TDC measurement. The TDC measurement ignores updates of CNT if there are no more stop events left to ignore.;When [TDC.TRIGCNTCFG.EN] is 1, [TDC.TRIGCNTLOAD.CNT] is loaded into CNT at the start of the measurement.

6.6.8.59 TRIGCNTLOAD Register (Offset = 218h) [Reset = 00000000h]

TRIGCNTLOAD is shown in Table 6-165.

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Trigger Counter Load;Stop-counter load.

Table 6-165. TRIGCNTLOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CNT	R/W	0h	Number of stop events to ignore when [TDC.TRIGCNTCFG.EN] is 1.;To measure frequency of an event source: ;- Set start event equal to stop event.;- Set CNT to number of periods to measure. Both 0 and 1 values measures a single event source period.;To measure pulse width of an event source:;- Set start event source equal to stop event source.;- Select different polarity for start and stop event.;- Set CNT to 0.;To measure time from the start event to the Nth stop event when N > 1:;- Select different start and stop event source.;- Set CNT to (N-1). ;See the Technical Reference Manual for event timing requirements. ;When [TDC.TRIGCNTCFG.EN] is 1, CNT is loaded into [TDC.TRIGCNT.CNT] at the start of the measurement.

6.6.8.60 TRIGCNTCFG Register (Offset = 21Ch) [Reset = 00000000h]

TRIGCNTCFG is shown in Table 6-166.

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Trigger Counter Configuration;Stop-counter configuration.

Table 6-166. TRIGCNTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EN	R/W	0h	Enable stop-counter.;0: Disable stop-counter.;1: Enable stop-counter.;Change only while [TDC.STAT.STATE] is IDLE.

6.6.8.61 PRECTL Register (Offset = 220h) [Reset = 00000000h]

PRECTL is shown in Table 6-167.

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Prescaler Control;The prescaler can be used to count events that are faster than the bus rate. ;It can be used to:;- count pulses on a specified event from the asynchronous event bus.;- prescale a specified event from the asynchronous event bus. ;To use the prescaler output as an event source in TDC measurements you must set both TRIGSRC.START_SRC and TRIGSRC.STOP_SRC to TDC_PRE.;It is recommended to use the prescaler when the signal frequency to measure exceeds 1/10th of the bus rate.

Table 6-167. PRECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESET_N	R/W	0h	Prescaler reset.;0: Reset prescaler.;1: Release reset of prescaler.;AUX_TDC_PRE event becomes 0 when you reset the prescaler.
6	RATIO	R/W	0h	Prescaler ratio. ;This controls how often the TDC_PRE event is generated by the prescaler. 0h = Prescaler divides input by 16. ;AUX_TDC_PRE event has a rising edge for every 16 rising edges of the input. AUX_TDC_PRE event toggles on every 8th rising edge of the input. 1h = Prescaler divides input by 64. ;AUX_TDC_PRE event has a rising edge for every 64 rising edges of the input. AUX_TDC_PRE event toggles on every 32nd rising edge of the input.
5	RESERVED	R	0h	Reserved
4-0	SRC	R/W	0h	Prescaler event source. ;Select an event from the asynchronous AUX event bus to connect to the prescaler input. ;Configure only while RESET_N is 0. 0h = LFTICK signal going to the RTC 1h = Low frequency on-chip oscillator 2h = Low frequency crystal oscillator 3h = Delayed version of selected LFCLK 4h = General purpose input signal 5h = Digital testbus bit 0 6h = Digital testbus bit 1 7h = Digital testbus bit 2 8h = Digital testbus bit 3 9h = Digital testbus bit 4 Ah = Digital testbus bit 5 Bh = Digital testbus bit 6 Ch = Digital testbus bit 7 Dh = Digital testbus bit 8 Eh = Digital testbus bit 9 Fh = Digital testbus bit 10 10h = Digital testbus bit 11 11h = Digital testbus bit 12 12h = Digital testbus bit 13 13h = Digital testbus bit 14 14h = Digital testbus bit 15 15h = High frequency on-chip oscillator 16h = High frequency crystal oscillator 17h = Audio frequency on-chip oscillator

6.6.8.62 PRECNTR Register (Offset = 224h) [Reset = 00000000h]

PRECNTR is shown in Table 6-168.

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Prescaler Counter

Table 6-168. PRECNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CAPT	W	0h	Prescaler counter capture strobe.;Write a 1 to CAPT to capture the value of the 16-bit prescaler counter into CNT. Read CNT to get the captured value.
15-0	CNT	R	0h	Prescaler counter value.;Write a 1 to CAPT to capture the value of the 16-bit prescaler counter into CNT. Read CNT to get the captured value. ;The read value gets 1 LSB uncertainty if the event source level rises when you release the reset.;The read value gets 1 LSB uncertainty if the event source level rises when you capture the prescaler counter.;Please note the following:;- The prescaler counter is reset to 3 by [TDC.PRECTL.RESET_N].;- The captured value is 3 when the number of rising edges on prescaler input is less than 3. Otherwise, captured value equals number of event pulses.

6.6.8.63 CNT Register (Offset = 300h) [Reset = 00000000h]

CNT is shown in Table 6-169.

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WDT counter value register

Table 6-169. CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Counter value.;A write to this field immediately starts (or restarts) the counter. It will count down from the written value.;If the counter reaches 0, a reset will be generated.;A write value of 0 immediately generates a reset.;This field is only writable if not locked. See LOCK register.;Writing this field will automatically activate the lock.;A read returns the current value of the counter.

6.6.8.64 TEST Register (Offset = 304h) [Reset = 00000000h]

TEST is shown in Table 6-170.

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WDT test mode register

Table 6-170. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STALLEN	R/W	0h	WDT stall enable;This field is only writable if not locked. See LOCK register. 0h = DISABLE;WDT continues counting while the CPU is stopped by a debugger. 1h = ENABLE;WDT stops counting while the CPU is stopped by a debugger.

6.6.8.65 LOCK Register (Offset = 308h) [Reset = 00000000h]

LOCK is shown in Table 6-171.

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WDT lock register

Table 6-171. LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STAT	R/W	1h	A write with value 0x1ACCE551 unlocks the watchdog registers for write access.;A write with any other value locks the watchdog registers for write access.;Writing the CNT register will also lock the watchdog registers.;A read of this field returns the state of the lock (0=unlocked, 1=locked).

6.6.9 CLKCTL Registers

Table 6-172 lists the memory-mapped registers for the CLKCTL registers. All register offset addresses not listed in Table 6-172 should be considered as reserved locations and the register contents should not be modified.

Table 6-172. CLKCTL Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 6.6.9.1
4h	DESCEX0	Extended Description Register 0.	Section 6.6.9.2
8h	DESCEX1	Extended Description Register 1.	Section 6.6.9.3
Ch	CLKCFG0	Clock Configuration Register 0.	Section 6.6.9.4
10h	CLKCFG1	Clock Configuration Register 1.	Section 6.6.9.5
14h	CLKENSET0	Clock Enable Set Register 0.	Section 6.6.9.6
18h	CLKENSET1	Clock Enable Set Register 1.	Section 6.6.9.7
20h	CLKENCLR0	Clock Enable Clear Register 0.	Section 6.6.9.8
24h	CLKENCLR1	Clock Enable Clear Register 1.	Section 6.6.9.9
3Ch	STBYPTR	Internal. Only to be used through TI provided API.	Section 6.6.9.10
48h	IDLECFG	IDLE Configuration Register.	Section 6.6.9.11

Complex bit access types are encoded to fit into small table cells. Table 6-173 shows the codes that are used for access types in this section.

Table 6-173. CLKCTL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.6.9.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 6-174.

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Description Register. ;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 6-174. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	254Fh	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	0h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	0h	Major revision of IP 0-15
3-0	MINREV	R	0h	Minor revision of IP 0-15.

6.6.9.2 DESCEX0 Register (Offset = 4h) [Reset = 00000000h]

DESCEX0 is shown in Table 6-175.

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Extended Description Register 0. ;This register shows SVT IP availability, HW features and memory size configuration.

Table 6-175. DESCEX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	LGPT3	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
29	LGPT2	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
28	LGPT1	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
27	LGPT0	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
26-21	RESERVED	R	0h	Reserved
20	I2S	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
19-18	RESERVED	R	0h	Reserved
17	DMA	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
16	LAES	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
15	RESERVED	R	0h	Reserved
14	ADC0	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
13-12	RESERVED	R	0h	Reserved
11	SPI1	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
10	SPI0	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
9-7	RESERVED	R	0h	Reserved
6	I2C0	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
5-4	RESERVED	R	0h	Reserved
3	UART1	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
2	UART0	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available

Table 6-175. DESCEX0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LRFD	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
0	GPIO	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available

6.6.9.3 DESCEX1 Register (Offset = 8h) [Reset = 00000000h]

DESCEX1 is shown in Table 6-176.

Return to the Summary Table.

Extended Description Register 1. ;This register shows SVT IP availability, HW features and memory size configuration.

Table 6-176. DESCEX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	FLASHSZ	R	3h	System flash availability 0h = Flash size set to level 0 (Min size) 1h = Flash size set to level 1 2h = Flash size set to level 2 3h = Flash size set to level 3 (Max size)
29-28	SRAMSZ	R	3h	System SRAM availability 0h = SRAM size set to level 0 (Min size) 1h = SRAM size set to level 1 2h = SRAM size set to level 2 3h = SRAM size set to level 3 (Max size)
27-21	RESERVED	R	0h	Reserved
20-19	HSMOPT	R	3h	HSM IP feature availability. 3h = All features available
18-17	CANOPT	R	3h	CAN IP feature availability 3h = All features available
16	RESERVED	R	0h	Reserved
15-8	ROPT	R	FFh	System radio feature availability FFh = All features available
7	RESERVED	R	0h	Reserved
6	MCAN	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
5	APU	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
4	HSM	R	1h	IP status on device 0h = IP is unavailable 1h = IP is available
3-0	RESERVED	R	0h	Reserved

6.6.9.4 CLKCFG0 Register (Offset = Ch) [Reset = 00000000h]

CLKCFG0 is shown in Table 6-177.

Return to the Summary Table.

Clock Configuration Register 0.;This register shows the IP clock configuration for the system.;The configuration is updated through CLKENSET0 and CLKENCLR0.

Table 6-177. CLKCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	LGPT3	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
29	LGPT2	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
28	LGPT1	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
27	LGPT0	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
26-21	RESERVED	R	0h	Reserved
20	I2S	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
19-18	RESERVED	R	0h	Reserved
17	DMA	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
16	LAES	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
15	RESERVED	R	0h	Reserved
14	ADC0	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
13-12	RESERVED	R	0h	Reserved
11	SPI1	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
10	SPI0	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
9-7	RESERVED	R	0h	Reserved
6	I2C0	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
5-4	RESERVED	R	0h	Reserved
3	UART1	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
2	UART0	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled

Table 6-177. CLKCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LRFD	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
0	GPIO	R	1h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled

6.6.9.5 CLKCFG1 Register (Offset = 10h) [Reset = 00000000h]

CLKCFG1 is shown in Table 6-178.

Return to the Summary Table.

Clock Configuration Register 1.;This register shows the IP clock configuration for the system.;The configuration is updated through CLKENSET1 and CLKENCLR1.

Table 6-178. CLKCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	MCAN	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
5	APU	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
4	HSM	R	0h	IP clock configuration 0h = Clock is disabled 1h = Clock is enabled
3-0	RESERVED	R	0h	Reserved

6.6.9.6 CLKENSET0 Register (Offset = 14h) [Reset = 00000000h]

CLKENSET0 is shown in Table 6-179.

Return to the Summary Table.

Clock Enable Set Register 0.;This register enables IP clocks in the system. ;Used to set the corresponding fields in CLKCFG0 to 1.

Table 6-179. CLKENSET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	LGPT3	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
29	LGPT2	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
28	LGPT1	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
27	LGPT0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
26-21	RESERVED	R	0h	Reserved
20	I2S	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
19-18	RESERVED	R	0h	Reserved
17	DMA	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
16	LAES	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
15	RESERVED	R	0h	Reserved
14	ADC0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
13-12	RESERVED	R	0h	Reserved
11	SPI1	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
10	SPI0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
9-7	RESERVED	R	0h	Reserved
6	I2C0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
5-4	RESERVED	R	0h	Reserved
3	UART1	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
2	UART0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable

Table 6-179. CLKENSET0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LRFD	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
0	GPIO	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable

6.6.9.7 CLKENSET1 Register (Offset = 18h) [Reset = 00000000h]

CLKENSET1 is shown in Table 6-180.

Return to the Summary Table.

Clock Enable Set Register 1.;This register enables IP clocks in the system. ;Used to set the corresponding fields in CLKCFG1 to 1.

Table 6-180. CLKENSET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	MCAN	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
5	APU	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
4	HSM	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Set IP clock enable
3-0	RESERVED	R	0h	Reserved

6.6.9.8 CLKENCLR0 Register (Offset = 20h) [Reset = 00000000h]

CLKENCLR0 is shown in Table 6-181.

Return to the Summary Table.

Clock Enable Clear Register 0.;This register disables IP clocks in the system. ;Used to clear the corresponding fields in CLKCFG0 to 0.

Table 6-181. CLKENCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	LGPT3	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
29	LGPT2	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
28	LGPT1	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
27	LGPT0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
26-21	RESERVED	R	0h	Reserved
20	I2S	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
19-18	RESERVED	R	0h	Reserved
17	DMA	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
16	LAES	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
15	RESERVED	R	0h	Reserved
14	ADC0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
13-12	RESERVED	R	0h	Reserved
11	SPI1	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
10	SPI0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
9-7	RESERVED	R	0h	Reserved
6	I2C0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
5-4	RESERVED	R	0h	Reserved
3	UART1	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
2	UART0	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable

Table 6-181. CLKENCLR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LRFD	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
0	GPIO	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable

6.6.9.9 CLKENCLR1 Register (Offset = 24h) [Reset = 00000000h]

CLKENCLR1 is shown in Table 6-182.

Return to the Summary Table.

Clock Enable Clear Register 1.;This register disables IP clocks in the system. ;Used to clear the corresponding fields in CLKCFG1 to 0.

Table 6-182. CLKENCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	MCAN	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
5	APU	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
4	HSM	W	0h	Configure IP clock enable 0h = IP clock enable is unchanged 1h = Clear IP clock enable
3-0	RESERVED	R	0h	Reserved

6.6.9.10 STBYPTR Register (Offset = 3Ch) [Reset = 00000000h]

STBYPTR is shown in Table 6-183.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 6-183. STBYPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

6.6.9.11 IDLECFG Register (Offset = 48h) [Reset = 00000000h]

IDLECFG is shown in Table 6-184.

Return to the Summary Table.

IDLE Configuration Register.;This register contains flash LDO configuration for IDLE mode.

Table 6-184. IDLECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MODE	R/W	0h	Flash LDO configuration in SLEEP/IDLE mode. 0h = Flash LDO is on in SLEEP/IDLE mode.;Gives fast wake up time from SLEEP/IDLE mode, but increased power consumption. 1h = Flash LDO is off in SLEEP/IDLE mode. ;Decreases power consumption in SLEEP/IDLE mode, but gives longer wake up time.;Note: NVM clock is turned off independent of DMA status. Therefore SW must ensure that DMA never access NVM in this mode.

6.7 Resets

Only a global asynchronous reset is available; no partial or subsystem reset is supported. Reset can be triggered by:

- RSTN pin
- Power-on reset
- VDDS Brown-out detector reset
- VDDR Brown-out detector reset
- Watchdog reset
- CPU hardfault
- Software reset request
- Debug reset request
- LF Clock Loss
- EMFI reset
- TAMPER reset
- SRAM parity reset

The PMCTL.RSTSTA[2:0] RESETSRC and PMCTL.SYSSRC[7:4] SYSSRC bit fields are populated after reset and report which of the above reset sources triggered the reset. The PMCTL.RSTSTA register is read by the ROM boot sequence and used to determine which wake-up action to take. The PMCTL.RSTSTA register can also be read by the user application to take appropriate action. The user application can also determine whether the system was woken from shutdown by reading the PMCTL.RSTSTA[17] SDDET bit. If the bit is set, the system has woken from shutdown.

The hierarchy of reset signals is as follows:

- RSTN_POR: Everything is reset, everything is disabled
- RSTN Asserted until all reset sources are released, and all regulated and unregulated voltage supplies are above the minimum required levels. The following resets are at the same level as RSTN:-
  - RSTN pin
  - VDDS Brown-out detector reset
  - VDDR Brown-out detector reset
  - Watchdog reset
  - CPU hardfault
  - Software reset request
  - Debug reset request
  - LF Clock Loss
  - EMFI reset
  - TAMPER reset

– SRAM parity reset

RSTN_POR is the only reset source that clears the IceMelter and AON/ULL 3P3V REGBANK.

Any reset higher in the hierarchy propagates to everything below. Resets are released at least one clock cycle before any clock starts running or synchronously to the clock edge if that is not possible.

The reset pin on the device serves a dual purpose as an "enable device" signal for a transceiver or Network Processor (NWP).

6.7.1 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is used to regain control when the system has failed due to a software error or due to the failure of an external device to respond in the expected way during standby. This WDT generates a reset when a time-out value is reached. Writing to CKMD.WDTCNT starts the counter which starts counting down from the set value on every LFCLK. The WDT relies on a working LFCLK. The WDT will stop working if LFCLK is lost. In the case of a LFCLK loss the device can be reset by the LF loss detection feature. See Section 6.7.3 for additional details.

If the CKMD.WDTCNT register is written with a new value while the WDT counter is counting, then the counter is loaded with the new value and continues counting. If CKMD.WDTTEST[0] STALLEN is set, the counter can stall when the microcontroller asserts the CPU Halt Flag during debug.

To prevent the WDT configuration from being inadvertently altered by software, the write access to the watchdog registers is automatically locked by writing the CKMD.WDTLOCK register to any value. To unlock the WDT, write the CKMD.WDTLOCK register to the value 0x1ACCE551.

The WDT can be configured using the following sequence:

- Unlock the WDT module by writing 0x1ACCE551 to the CKMD.WDTLOCK register.
- Load the CKMD.WDTCNT register with the desired timer load value. The register will be locked upon write.

Note

When this counter is running, there is no way to stop this counter other than device reset. This is to prevent accidentally disabling the WDT and leaving the device in an unresponsive state.

6.7.2 RTC Reset

RTC TIME Reset is split between sync and non-sync reset system reset, in order to allow the RTC TIME value to survive internally generated synchronous resets so that an application's time base is not lost when such a reset occurs. RTC is reset only with LF Clock Loss reset, EMFI reset, and TAMPER reset.

6.7.3 LF Loss Detection

When the LF clock loss feature is enabled by setting the PMCTL.RSTCTL[2] LFLOSS bit and CKMD.LFMONCTL[0] EN bit, a detected loss of the selected LF source (low frequency crystal (LFXT) or low frequency oscillator (LFOSC)) results in a system reset. After recovery, the PMCTL.RSTSTA[2:0] RESETSRC and PMCTL.RSTSTA[7:4] SYSSRC bit fields show clock loss as the source of reset.

6.8 AON (REG3V3) Register Bank

The device has an AON Register Bank that is directly supplied by VDDS and only resets on RSTN_POR. The content of this register bank is retained in SHUTDOWN and across all resets, except RSTN_POR. The register bank is accessed through the PMCTL.AONRSET1, PMCTL.AONRCLR1, and PMCTL.AONRSTA1 registers.

Chapter 7

Internal Memory

This chapter presents the versatile instruction memory system (VIMS) and related memories including FLASH, SRAM, and bootloader ROM.

7.1 SRAM

7.1.1 Overview

The SRAM controller provides 144 KB of system RAM consisting of single-cycle on-chip SRAM. It is extendable up to 162 KB when parity is disabled. The SRAM also supports full data retention in standby power mode.

7.1.1.1 Purpose of the Peripheral

The purpose of this peripheral is to provide a wrapper for the system SRAM and related control MMRs.

7.1.1.2 Features

High-level features include:

- Single cycle 96 MHz operation.
- Parity error detection
- SRAM Extension
- Hardware Initialization function
- TrustZone Watermarking

7.1.1.3 Functional Block Diagram

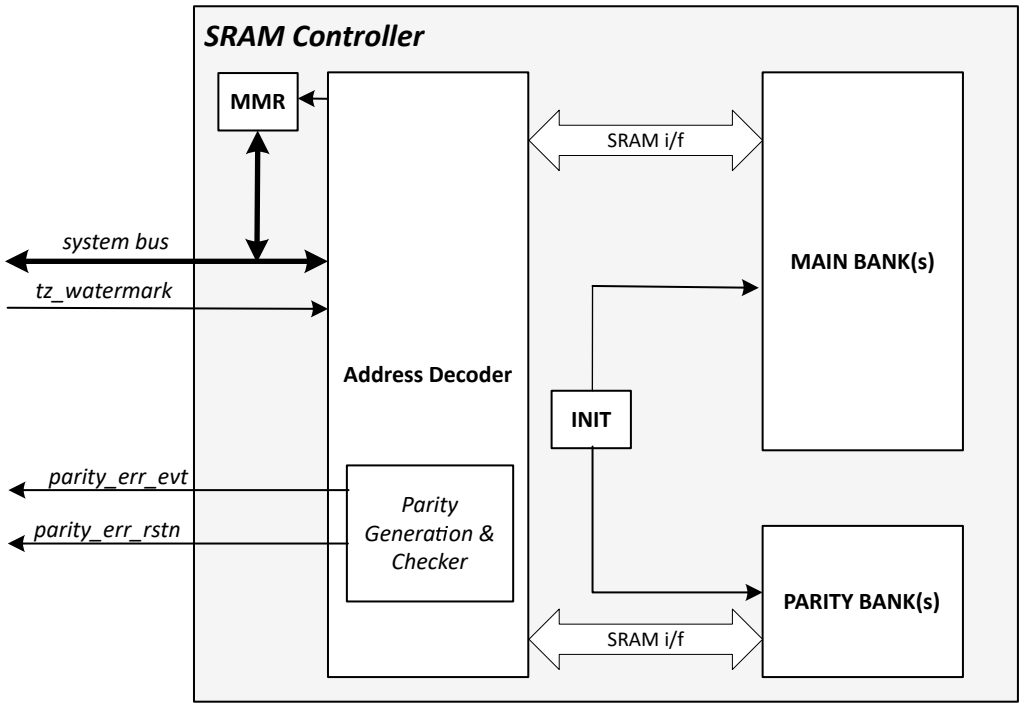

Figure 7-1. SRAM Block Diagram

7.1.2 Peripheral Functional Description

Internally, the 162KB space is organized into

- 4 x 32KB Banks
- 2 x 16KB Banks
- 1 x 2KB bank

At high-level, the SRAM size is split as 144KB Main and 18KB Parity block. When parity is enabled, main block holds the user data and parity block holds the corresponding parity information.

When parity is disabled, the parity block is appended to main block to provide a larger user data space.

7.1.2.1 Parity error detection

During an SRAM write, a parity bit is calculated and stored for each byte that is written. Parity error detection is done on a byte-wide basis during an SRAM read operation.

When a parity error is detected, the error address is captured in the parity error address register **PARERR.ADDR** and an event is generated. This event is acknowledged by reading this register. If another parity error is detected before acknowledging the previous event, the SRAM controller generates a reset request.

7.1.2.1.1 Parity Error Debug Register

The parity error debug feature allows debugging and testing of the handling of parity error detection by injecting a parity error at the specified address. The **PARDBG.ADDR** register holds the word address for the error injection, which is triggered when any byte in this specified word is written.

This feature can be enabled by setting **CFG.PARDBGEN** = 1.

Note

Post disabling this feature, the debug location has to be re-written to clean up the injected parity error.

7.1.2.2 Extension Mode

When parity is disabled, the usable SRAM space for the application is extended to 162KB.

7.1.2.3 Initialization

The SRAM can be initialized by dedicated initialization hardware. The memory initialization ensures that parity errors are not generated due to reads from locations that have not been initialized by software. Banks can be selected for initialization by writing a '1' to specific bits of the INITSEL register - each bit on this register corresponds to one bank. Actual initialization is triggered when a '1' is written to the bit INITTRIG.TRG. This bit auto clears once the initialization is complete.

Note

Only one bank should be selected at a time for initialization.

7.1.2.4 TrustZone Watermarking

Trust-Zone watermark controls the partition of the SRAM space into Secure & Non-Secure regions with granularity of 1KB. The secure region is accessible via secure SRAM address and non-secure is accessible at non-secure SRAM address.

7.1.3 SRAM Registers

Table 7-1 lists the memory-mapped registers for the SRAM registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. SRAM Registers

Offset	Acronym	Register Name	Section
0h	DESC	This register identifies the peripheral	Section 7.1.3.1
64h	DTB	This bit field is used to select DTB mux digital inputs	Section 7.1.3.2
100h	CFG	Configuration Register	Section 7.1.3.3
104h	INITSEL	Initilizataion Select Register.	Section 7.1.3.4
108h	INITTRIG	Initilizataion Select Register. This register is writable only if CFG.LOCKDIS = 1	Section 7.1.3.5
10Ch	INITSTAT	Initilizataion Status	Section 7.1.3.6
110h	PARDBG	Parity error check debug address setting	Section 7.1.3.7
114h	PARERR	Parity error	Section 7.1.3.8

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. SRAM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.3.1 DESC Register (Offset = 0h) [Reset = 1A480010h]

DESC is shown in Table 7-3.

Return to the Summary Table.

This register identifies the peripheral

Table 7-3. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	1A48h	Module identifier
15-12	STDIPOFF	R	0h	64 B Standard IP MMR block#lt gt#0: STDIP MMRs do not exist#lt gt#1:15: These MMRs begin at offset 64*STDIPOFF from IP base address
11-8	INSTIDX	R	0h	IP Instance number
7-4	MAJREV	R	1h	Major revision
3-0	MINREV	R	0h	Minor revision

7.1.3.2 DTB Register (Offset = 64h) [Reset = 00000000h]

DTB is shown in Table 7-4.

Return to the Summary Table.

This bit field is used to select DTB mux digital inputs

Table 7-4. DTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	SEL	R/W	0h	DTB Selection

7.1.3.3 CFG Register (Offset = 100h) [Reset = 000000XXh]

CFG is shown in Table 7-5.

Return to the Summary Table.

Configuration Register

Table 7-5. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	PARDBGEN	R/W	0h	SRAM Parity Debug Enable. 0h = Disable Parity Debug. Normal operation 1h = Enable Parity Debug. An address offset can be written to ADDR and parity errors will be generated on reads from within this offset
7-1	RESERVED	R	0h	
0	PAREN	R/W	0h	SRAM Parity Enable. 0h = Disable Parity 1h = Enable Parity

7.1.3.4 INITSEL Register (Offset = 104h) [Reset = 00000000h]

INITSEL is shown in Table 7-6.

Return to the Summary Table.

Initilizataion Select Register.

Table 7-6. INITSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	
6-0	SEL	R/W	0h	Bank Select. Bit[0]:Bank-0 Bit[1]:Bank-1 ... Bit[n]:Bank-n

7.1.3.5 INITTRIG Register (Offset = 108h) [Reset = 00000000h]

INITTRIG is shown in Table 7-7.

Return to the Summary Table.

Initilizataion Select Register. This register is writable only if CFG.LOCKDIS = 1

Table 7-7. INITTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	TRG	R/W	0h	Trigger Initilization. All banks with its INIT.SEL[x] bit set to 1 will be initilizaed. This bit will auto clear once initlization is complete

7.1.3.6 INITSTAT Register (Offset = 10Ch) [Reset = 00000000h]

INITSTAT is shown in Table 7-8.

Return to the Summary Table.

Initilizataion Status

Table 7-8. INITSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	
6-0	BUSY	R	0h	Each bit indicate that corresponding bank is getting initialzed

7.1.3.7 PARDBG Register (Offset = 110h) [Reset = 0000000Xh]

PARDBG is shown in Table 7-9.

Return to the Summary Table.

Parity error check debug address setting

Table 7-9. PARDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	
19-2	ADDR	R/W	0h	Debug Parity Error Address Offset.# #When PARDBGEN is 1, this field is used to set a parity debug address offset. Writes within this address offset will force incorrect parity bits to be stored together with the data written. The following reads within this same address offset will thus result in parity errors to be generated.
1-0	RESERVED	R	0h	

7.1.3.8 PARERR Register (Offset = 114h) [Reset = 00000000h]

PARERR is shown in Table 7-10.

Return to the Summary Table.

Parity error

Table 7-10. PARERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R	0h	Parity Error Address Offset.# #This holds the address offset that first generated the parity error and an interrupt is generated. # #This register is 'Clear-On-Read'

7.1.4 SRAMCTRL Registers

Table 7-11 lists the memory-mapped registers for the SRAMCTRL registers. All register offset addresses not listed in Table 7-11 should be considered as reserved locations and the register contents should not be modified.

Table 7-11. SRAMCTRL Registers

Offset	Acronym	Register Name	Section
0h	DESC	;This register identifies the peripheral	Section 7.1.4.1
100h	CFG	;Configuration Register	Section 7.1.4.2
110h	PARDBG	;Parity error check debug address setting	Section 7.1.4.3
114h	PARERR	;Parity error	Section 7.1.4.4

Complex bit access types are encoded to fit into small table cells. Table 7-12 shows the codes that are used for access types in this section.

Table 7-12. SRAMCTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.4.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 7-13.

Return to the Summary Table.

;This register identifies the peripheral

Table 7-13. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	1A48h	Module identifier
15-12	STDIPOFF	R	0h	64 B Standard IP MMR block#lt gt#0: STDIP MMRs do not exist#lt gt#1:15: These MMRs begin at offset 64*STDIPOFF from IP base address
11-8	INSTIDX	R	0h	IP Instance number
7-4	MAJREV	R	1h	Major revision
3-0	MINREV	R	0h	Minor revision

7.1.4.2 CFG Register (Offset = 100h) [Reset = 00000000h]

CFG is shown in Table 7-14.

Return to the Summary Table.

;Configuration Register

Table 7-14. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	PARDBGEN	R/W	0h	SRAM Parity Debug Enable. 0h = Disable Parity Debug. Normal operation 1h = Enable Parity Debug. An address offset can be written to PARDBG.ADDR and parity errors will be generated on reads from within this offset
7-1	RESERVED	R	0h	Reserved
0	PAREN	R/W	0h	SRAM Parity Enable. 0h = Disable Parity 1h = Enable Parity

7.1.4.3 PARDBG Register (Offset = 110h) [Reset = 00000000h]

PARDBG is shown in Table 7-15.

Return to the Summary Table.

;Parity error check debug address setting

Table 7-15. PARDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-2	ADDR	R/W	Xh	Debug Parity Error Address Offset.# #When CFG.PARDBGEN is 1, this field is used to set a parity debug address offset. Writes within this address offset will force incorrect parity bits to be stored together with the data written. The following reads within this same address offset will thus result in parity errors to be generated.
1-0	RESERVED	R	0h	Reserved

7.1.4.4 PARERR Register (Offset = 114h) [Reset = 00000000h]

PARERR is shown in Table 7-16.

Return to the Summary Table.

;Parity error

Table 7-16. PARERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R	0h	Parity Error Address Offset.# #This holds the address offset that first generated the parity error and an interrupt is generated. # #This register is 'Clear-On-Read'

7.2 VIMS

7.2.1 Overview

The Versatile Instruction Memory System (VIMS) module provides the access path to the following instruction memories:

- Up to 1MB with 96KB reserved for HSM
- Up to 32KB of Boot ROM

7.2.1.1 Purpose of the Peripheral

The VIMS module forwards CPU accesses (code/data) and system bus accesses to the addressed memories. It also arbitrates access between the CPU, System Bus and HSM.

7.2.1.2 Features

The main features of the VIMS include :

- 96MHz operating frequency
- Up to 1MB with 96KB reserved for HSM
- 32KB ROM
- Dedicated 8KB CPU Cache for instruction fetch and data access
- Dedicated 2KB Hardware Security Module (HSM) Cache for instruction fetch and data access
- Dedicated 128-bit Line buffer for System Bus access
- Configurable Read Protection for first 16KB Flash region
- Read and Write protect-able auxiliary regions.
- Execute while program
- Configurable Secure/Non-Secure Flash partition
- TrustZone Watermark

7.2.1.3 Functional Block Diagram

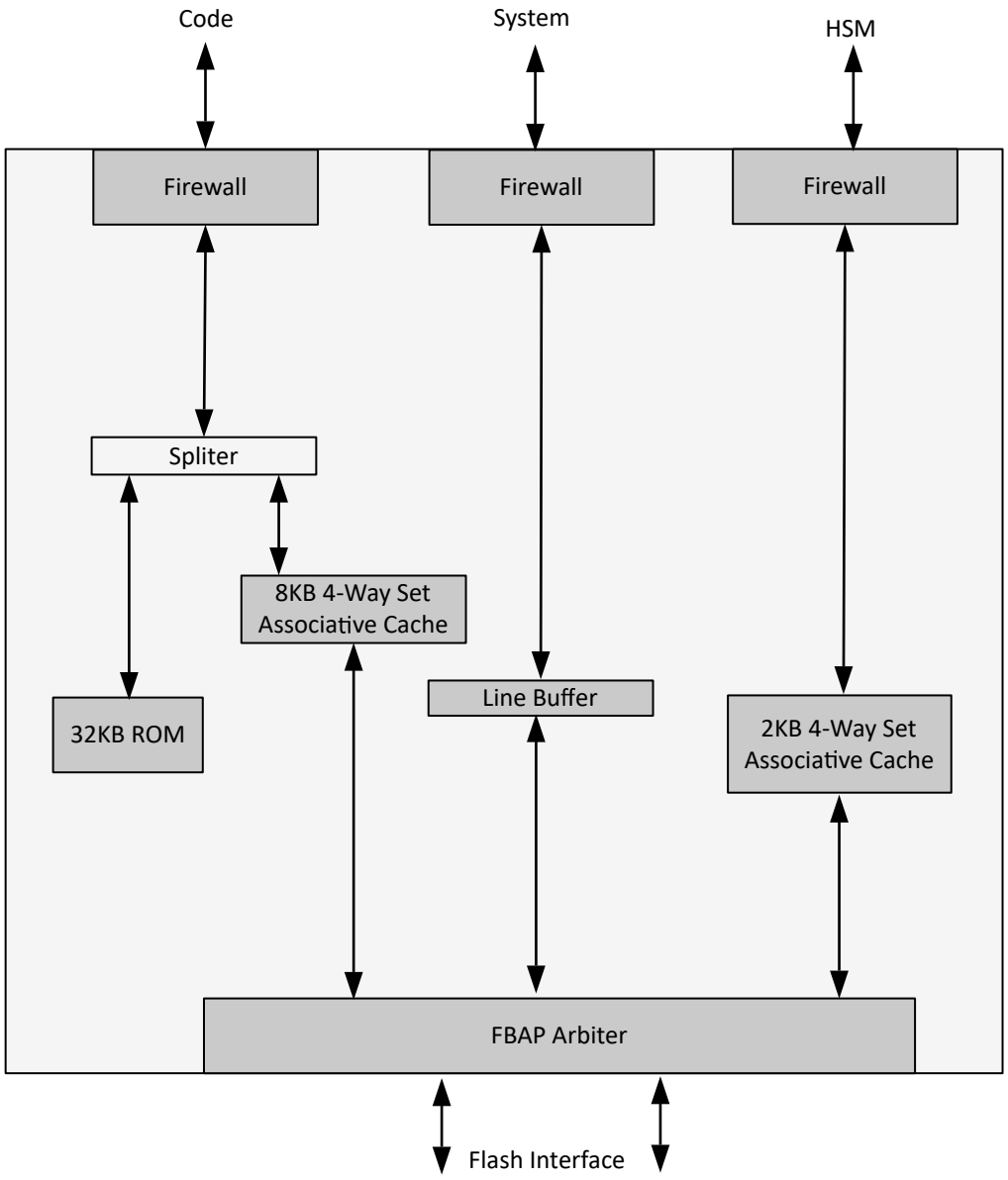

Figure 7-2. VIMS Block Diagram

7.2.2 Peripheral Functional Description

7.2.2.1 Dedicated 8KB CPU Cache

VIMS includes an 8KB 4-Way Set associative Cache for instruction fetches and data accesses from the CPU and any cache hit would result in zero wait state access, except for the case where a hit is immediately following a miss.

7.2.2.2 Dedicated 2KB HSM Cache

VIMS includes an 2KB 4-Way Set associative Cache for instruction fetches and data accesses from the HSM and any cache hit would result in zero wait state access, except for the case where a hit is immediately following a miss.

7.2.2.3 Dedicated 128-bit Line buffer

VIMS includes an 128-bit line buffer for data accesses from the System Bus and any hit would result in zero wait state access.

7.2.2.4 ROM

VIMS encapsulates 32KB of ROM and contains the device boot code.

7.2.2.5 Flash

The Flash is organized in banks of 512kB each, up to the maximum Flash size of the device (consult the device datasheet for the Flash size of each variant). The banks are further divided into sectors of 2KB that can be individually erased. An erase operation on a sector causes the entire content of the sector to be reset to all 1s. A programming operation can change bits from 1 to 0 with byte granularity.

There is a restriction on how many write operations are allowed to a FLASH row between erases. A row is comprised of 2048 bits (or 256 bytes). The FLASH memory is divided evenly into physical rows. One may perform a maximum of 83 write operations within a row between erases. If more than 83 write operations are performed before re-erasure, one may see unwritten bits in the row that are erased (in a logic 1 state) become programmed (change to a logic 0 state). User software must take care of this restriction, there is no hardware that checks and informs if this restriction is violated.

VIMS allows programming or erasing data on one bank without blocking read access to other bank. A read access to same bank that is getting programmed or erased would result in blocking of the access or an invalid data is returned.

Note

The flash is shared between CPU and HSM so the actual available space for user application depends on the CFG.HSMSZ configuration done at the boot.

7.2.2.6 Auxiliary Regions

In addition to the Main Flash region, each bank supports 3 Auxiliary regions.

- Non-Main
- TRIM
- ENGR

Bank	Region	Usage	Description	Read Protection	Write Protection
0	Non-Main0	CCFG	User readable with read protected sub-section. User Programmable	RDPRNMN.CCFG protects last 512 Bytes	*WEPRAUX.CCFG* (single bit) protects this whole region.
	Non-Main1	HSMOTP0	Dedicated for HSM	Protected by *CFG.LOCK*	Protected by CFG.LOCK
	Trim	FCFG	Readable with read protected sub-section. Write Locked	*RDPRTRM.FCFG* protects last 512 Bytes	*WEPRAUX.FCFG* (single bit) protects this whole region.
	ENGR	-	Read and Write Locked	*RDPREGR.ENGR (single bit) protects the whole region*	*WEPRAUX.ENGR* (single bit) protects this whole region.

Bank	Region	Usage	Description	Read Protection	Write Protection
1	Non-Main0	VLOG	Used by Boot code	*RDPRNMN.VLOG (single bit) protects the whole region*	*WEPRAUX.VLOG* (single bit) protects this whole region.
	Non-Main1	HSMOTP1	Dedicated for HSM	Protected by *CFG.LOCK*	Protected by CFG.LOCK
	Trim	SCFG	Used by Boot code	*RDPRTRM.SCFG (single bit) protects the whole region*	*WEPRAUX.SCFG* (single bit) protects this whole region.
	ENGR		Locked	*RDPREGR.ENGR (single bit) protects the whole region*	*WEPRAUX.ENGR* (single bit) protects this whole region.

7.2.2.7 Flash Partition & Protection

7.2.2.7.1 Main Region

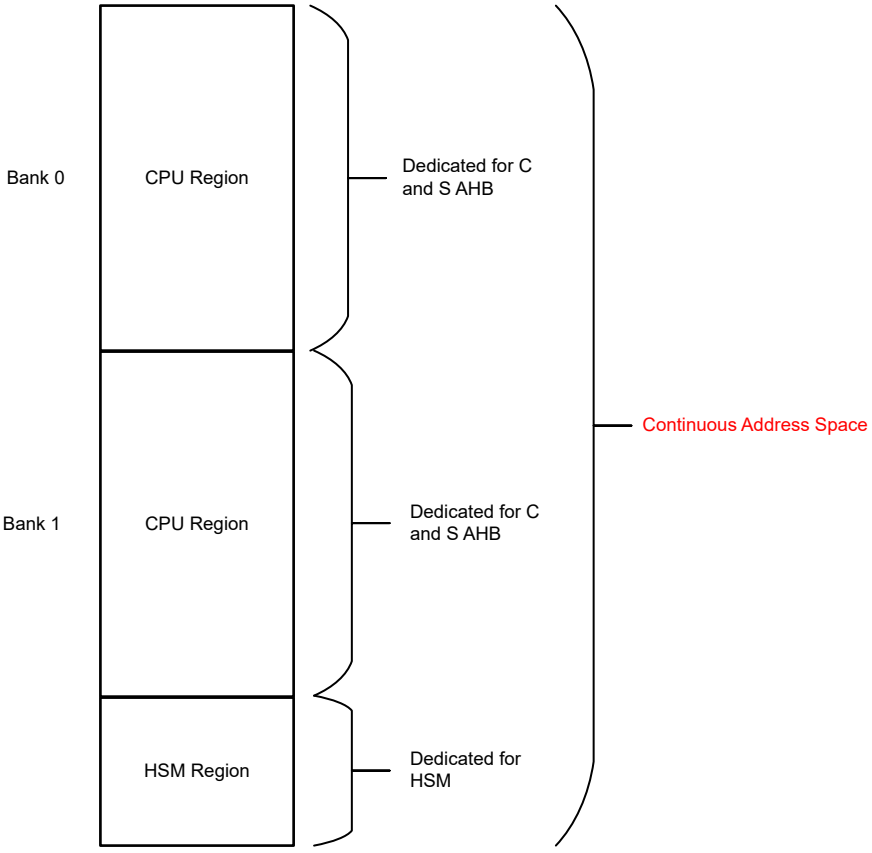

Figure 7-3. Flash Main Region Partition

Using Figure 7-3 above for a 1MB device as an example:

The 1MB logical region is considered as a single region and further partitioned into a "CPU" and "HSM" sub-regions.

The CPU sub-region is dedicated to CPU and can only be accessed by CPU or System Bus , while the HSM sub-region is dedicated to HSM.

7.2.2.7.2 Read Protection

7.2.2.7.3 Sticky Write/Erase Protection

Write/Erase protection bits are sticky 0 and are controlled by following registers :

Register	Description
WEPRA	Protects First 32 Main sectors of Logical Bank 0
WEPRAB0	Protects physical Bank 0 with granularity of 8 Main sectors
WEPRB1	Protects physical Bank 1 with granularity of 8 Main sectors
WEPRAUX	Protects TRIM, ENGR and NonMain

7.2.2.8 TrustZone™ Watermark

TrustZone™ watermark controls the partition of the CPU sub-region space into Non-Secure Callable (NSC) & Non-Secure regions with granularity of 8KB. SAU must be used to mark the NSC region as Secure to avoid the risk of being attacked by a non-secure code. The non-secure region is accessible at non-secure flash address.

Note

P

- There will be at least be one 8KB secure block.
- TrustZone™ watermark configuration only applies to access from CPU.

7.2.2.9 Debug Access

A debug access would be served by Cache/Line buffer if the requested data is available, otherwise will be served directly from the flash memory. This ensures that the cache state is not impacted by debug access.

7.2.3 VIMS Registers

Table 7-17 lists the memory-mapped registers for the VIMS registers. All register offset addresses not listed in Table 7-17 should be considered as reserved locations and the register contents should not be modified.

Table 7-17. VIMS Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 7.2.3.1
4h	DESCEX	Extended Module Description	Section 7.2.3.2
8h	FLWS1T	Waitstate for 1T mode.	Section 7.2.3.3
Ch	FLWS2T	Waitstate for 2T mode.	Section 7.2.3.4
18h	PTRMC0	Flash charge pump trim value.	Section 7.2.3.5
1Ch	B0TRMC1	Flash bank 0 trim value 1.	Section 7.2.3.6
20h	B0TRMC0	Flash bank 0 trim value 0.	Section 7.2.3.7
24h	B1TRMC1	Flash bank 0 trim value 1.	Section 7.2.3.8
28h	B1TRMC0	Flash bank 0 trim value 0.	Section 7.2.3.9
100h	FLBLCK	Flash block	Section 7.2.3.10
3FCh	CFG	Configuration	Section 7.2.3.11
400h	RDPRMN	Flash main region read protection confg.	Section 7.2.3.12
404h	RDPRNMN	Flash non main region read protection confg.	Section 7.2.3.13
408h	RDPRTRM	Flash trim region read protection config.	Section 7.2.3.14
40Ch	RDPREGR	Flash engr region read protection config.	Section 7.2.3.15
410h	WEPRA	Flash main region write/erase protection config.A	Section 7.2.3.16
414h	WEPRB0	Flash main region write/erase protection config.B0	Section 7.2.3.17
418h	WEPRB1	Flash main region write/erase protection config.B1	Section 7.2.3.18
41Ch	WEPRAUX	Flash Aux region write/erase protection config.	Section 7.2.3.19
420h	FLBSTA	Flash status	Section 7.2.3.20
424h	CCHCTL	Cache control	Section 7.2.3.21
428h	CCHSTA	Cache Status	Section 7.2.3.22
430h	CNTHIT	Cache Hit Counter	Section 7.2.3.23
434h	CNTMISS	Cache Miss Counter	Section 7.2.3.24
4FCh	CTL	Control register	Section 7.2.3.25

Complex bit access types are encoded to fit into small table cells. Table 7-18 shows the codes that are used for access types in this section.

Table 7-18. VIMS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.2.3.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 7-19.

Return to the Summary Table.

;Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 7-19. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	D140h	Module identification contains a unique peripheral identification number.
15-12	STDIPOFF	R	0h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP
3-0	MINREV	R	0h	Minor revision of IP

7.2.3.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 7-20.

Return to the Summary Table.

;Extended Description Register.This register describes the configuration of VIMS.

Table 7-20. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-27	NBANK	R	2h	Number of Flash banks
26-15	FLSZ	R	3FFh	FLASH size in Kilo Bytes. The total FLASH size is (FLSZ + 1) KB
14-0	ROMSZ	R	1Fh	ROM size in Kilo Bytes. The total ROM size is (ROMSZ + 1) KB

7.2.3.3 FLWS1T Register (Offset = 8h) [Reset = 00000000h]

FLWS1T is shown in Table 7-21.

Return to the Summary Table.

;Flash Wait State 1T. This register is used to specify the number of waitstates necessary for accessing the flash in 1T mode.

Table 7-21. FLWS1T Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	Fh	Flash read wait states for 1T accesses 0h = Wait state value 0 1h = Wait state value 1 2h = Wait state value 2 3h = Wait state value 3 4h = Wait state value 4 5h = Wait state value 5 6h = Wait state value 6 7h = Wait state value 7 8h = Wait state value 8 9h = Wait state value 9 Ah = Wait state value 10 Bh = Wait state value 11 Ch = Wait state value 12 Dh = Wait state value 13 Eh = Wait state value 14 Fh = Wait state value 15

7.2.3.4 FLWS2T Register (Offset = Ch) [Reset = 00000000h]

FLWS2T is shown in Table 7-22.

Return to the Summary Table.

;Flash Wait State 1T. This register is used to specify the number of waitstates necessary for accessing the flash in 2T mode. This register is writable only when CFG.LOCK is 1

Table 7-22. FLWS2T Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	Fh	Flash read wait states for 2T accesses 0h = Wait state value 0 1h = Wait state value 1 2h = Wait state value 2 3h = Wait state value 3 4h = Wait state value 4 5h = Wait state value 5 6h = Wait state value 6 7h = Wait state value 7 8h = Wait state value 8 9h = Wait state value 9 Ah = Wait state value 10 Bh = Wait state value 11 Ch = Wait state value 12 Dh = Wait state value 13 Eh = Wait state value 14 Fh = Wait state value 15

7.2.3.5 PTRMC0 Register (Offset = 18h) [Reset = 00000000h]

PTRMC0 is shown in Table 7-23.

Return to the Summary Table.

;FLASH Pump trim Bank 0. This register stores different PUMP trims. This register is writable only when CFG.LOCK is 1

Table 7-23. PTRMC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	131A0000h	Flash charge pump trim value.

7.2.3.6 B0TRMC1 Register (Offset = 1Ch) [Reset = 00000000h]

B0TRMC1 is shown in Table 7-24.

Return to the Summary Table.

;FLASH Bank 0 Trim [59:32]. This register stores different bank trims. This register is writable only when CFG.LOCK is 1

Table 7-24. B0TRMC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-0	VAL	R/W	Xh	Flash bank trim value.

7.2.3.7 B0TRMC0 Register (Offset = 20h) [Reset = 00000000h]

B0TRMC0 is shown in Table 7-25.

Return to the Summary Table.

;FLASH Bank 0 Trim [31:0]. This register stores different bank trims. This register is writable only when CFG.LOCK is 1

Table 7-25. B0TRMC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Flash bank trim value.

7.2.3.8 B1TRMC1 Register (Offset = 24h) [Reset = 00000000h]

B1TRMC1 is shown in Table 7-26.

Return to the Summary Table.

;FLASH Bank 1 Trim [59:32]. This register stores different bank trims. This register is writable only when CFG.LOCK is 1

Table 7-26. B1TRMC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-0	VAL	R/W	Xh	Flash bank trim value.

7.2.3.9 B1TRMC0 Register (Offset = 28h) [Reset = 00000000h]

B1TRMC0 is shown in Table 7-27.

Return to the Summary Table.

;FLASH Bank 1 Trim [31:0]. This register stores different bank trims. This register is writable only when CFG.LOCK is 1

Table 7-27. B1TRMC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Flash bank trim value.

7.2.3.10 FLBLCK Register (Offset = 100h) [Reset = 00000000h]

FLBLCK is shown in Table 7-28.

Return to the Summary Table.

;Flash Block. This register is used to block user read, write and erase operation to flash. This register is sticky 1 and writable only when CFG.LOCK is 1

Table 7-28. FLBLCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ACCESS	R/W	0h	Flash Access 0h = Allow 1h = Block

7.2.3.11 CFG Register (Offset = 3FCh) [Reset = 00000000h]

CFG is shown in Table 7-29.

Return to the Summary Table.

;Configuration Register. This register is used for VIMS configuration. This register is writable only when CFG.LOCK is 1

Table 7-29. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	HSMSZ	R/W	3h	HSM Size. Number of 32KB blocks allocated to HSM 0h = No space allocated to HSM 1h = 32KB 2h = 64KB 3h = 96KB 4h = 128KB 5h = 160KB 6h = 192KB 7h = 224KB
7-5	RESERVED	R	0h	Reserved
4	SPLMODE	R/W	0h	Split Mode. The logical address space is split into two equal regions 0h = Disable 1h = Enable
3	RDPRROM	R/W	1h	ROM Read Protection Disable 0h = Enable 1h = Disable
2	ATTEST	R/W	0h	This bit is used to enable flash test mode. 0h = Disable 1h = Enable
1	TRMVLID	R/W	0h	TRIM Valid. This bit indicates if flash charge pump and bank trim values are as applicable. 0h = Invalid 1h = Valid
0	LOCK	R/W	1h	Lock. Lock VIMS configuration. This bit is sticky '0' and when 0 write protects following registers ;FLWS1T;FLWS2T;PTRMC0;B0TRMC1;B0TRMC0;B1TRMC1;B1TRMC0;FLBLCK;CFG 0h = Configuration registers are locked for writing 1h = Configuration registers are open for writing

7.2.3.12 RDPRMN Register (Offset = 400h) [Reset = 00000000h]

RDPRMN is shown in Table 7-30.

Return to the Summary Table.

;Read Protect Main. First 16KB of flash main region can be protected with granularity of 2KB. This register is sticky 0

Table 7-30. RDPRMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	Fh	Protection configuration value. ; Undefined values will read protect whole protectable region 7h = Protect First 16KB 8h = Protect First 14KB 9h = Protect First 12KB Ah = Protect First 10KB Bh = Protect First 8KB Ch = Protect First 6KB Dh = Protect First 4KB Eh = Protect First 2KB Fh = Protection is Disabled

7.2.3.13 RDPRNMN Register (Offset = 404h) [Reset = 00000000h]

RDPRNMN is shown in Table 7-31.

Return to the Summary Table.

;Read Protect Non-Main regions.

Table 7-31. RDPRNMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	VLOG	R/W	1h	VLOG read protection configuration. This field is sticky 0
6	RESERVED	R	0h	Reserved
5-0	CCFG	R/W	3Fh	CCFG read protection configuration. Last 512 bytes of CCFG can be protected with granularity of 16Bytes. This field is sticky 0

7.2.3.14 RDPRTRM Register (Offset = 408h) [Reset = 00000000h]

RDPRTRM is shown in Table 7-32.

Return to the Summary Table.

;Read Protect Trim

Table 7-32. RDPRTRM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	SCFG	R/W	1h	SCFG read protection configuration. This field is sticky 0
6	RESERVED	R	0h	Reserved
5-0	FCFG	R/W	3Fh	FCFG read protection configuration. Last 512 bytes of CCFG can be protected with granularity of 16Bytes. This register is sticky 0

7.2.3.15 RDPREGR Register (Offset = 40Ch) [Reset = 00000000h]

RDPREGR is shown in Table 7-33.

Return to the Summary Table.

;Read Protect ENGR. This register is sticky 0

Table 7-33. RDPREGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ENGR	R/W	1h	ENGR read protection configuration.

7.2.3.16 WEPRA Register (Offset = 410h) [Reset = 00000000h]

WEPRA is shown in Table 7-34.

Return to the Summary Table.

;Write Erase Protect Main A. This register allows the first 32 sectors of the logical bank 0 main region to be protected from program or erase, with 1 bit protecting each sector (sector 0 to sector 31). This register is sticky 0

Table 7-34. WEPRA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Flash write/erase protection configuration value.

7.2.3.17 WEPRB0 Register (Offset = 414h) [Reset = 00000000h]

WEPRB0 is shown in Table 7-35.

Return to the Summary Table.

;Write Erase Protect Main Bank 0. This register allows physical bank 0 main region sectors to be protected from program and erase. Each bit corresponds to a group of 8 sectors. First 4-bit are reserved if physical Bank 0 is logical bank 0 CTL.SWAP = 0. This register is sticky 0

Table 7-35. WEPRB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Flash write/erase protection configuration value.

7.2.3.18 WEPRB1 Register (Offset = 418h) [Reset = 00000000h]

WEPRB1 is shown in Table 7-36.

Return to the Summary Table.

;Write Erase Protect Main Bank 1. This register allows physical bank 1 main region sectors to be protected from program and erase. Each bit corresponds to a group of 8 sectors. First 4-bit are reserved if physical Bank 1 is logical bank 0 CTL.SWAP = 1. This register is sticky 0

Table 7-36. WEPRB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Flash write/erase protection configuration value.

7.2.3.19 WEPRAUX Register (Offset = 41Ch) [Reset = 00000000h]

WEPRAUX is shown in Table 7-37.

Return to the Summary Table.

;Write Erase Protect Auxillary. Flash Write/Erase protection for Non-Main, TRIM and ENGR Regions. This register is sticky 0

Table 7-37. WEPRAUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	VLOG	R/W	1h	Write/Erase Protection for VLOG
3	SCFG	R/W	1h	Write/Erase Protection for SCFG
2	ENGR	R/W	1h	Write/Erase Protection for ENGR
1	FCFG	R/W	1h	Write/Erase Protection for FCFG
0	CCFG	R/W	1h	Write/Erase Protection for CCFG

7.2.3.20 FLBSTA Register (Offset = 420h) [Reset = 00000000h]

FLBSTA is shown in Table 7-38.

Return to the Summary Table.

;Flash Status. This register is used to indicate status of flash.

Table 7-38. FLBSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	B1BSY	R	0h	Bank 1 Busy. This bit indicates if flash Bank 1 is busy. 0h = Idle 1h = Busy
4	B0BSY	R	0h	Bank 0 Busy. This bit indicates if flash Bank 0 is busy. 0h = Idle 1h = Busy
3	PARERR	R	0h	Parity Error. This bit indicates parity error on write/erase and read protection MMRs. This bit is sticky when set to 1 by hardware. 0h = No Error 1h = Error
2	BUSY	R	0h	This bit indicates if flash is busy. 0h = Idle 1h = Busy
1	FL2TRDY	R	0h	Flash 2T Ready. This bit indicates if flash is ready in 2T mode. 0h = Not Ready 1h = Ready
0	FL1TRDY	R	0h	Flash 1T Ready. This bit indicates if flash is ready in 1T mode. 0h = Not Ready 1h = Ready

7.2.3.21 CCHCTL Register (Offset = 424h) [Reset = 00000000h]

CCHCTL is shown in Table 7-39.

Return to the Summary Table.

;Cache Control Register. This register is used for cache control on code bus Interface. This register can only be written when CCHSTA.BUSY is 0

Table 7-39. CCHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	HCHFLUSH	W	0h	Cache Flush for HSM Cache. This bit is used to flush the cache on HSM bus Interface. This bit is self clearing 1h = Trigger Flush
15-9	RESERVED	R	0h	Reserved
8	CNTCLR	W	0h	Cache Hit/Miss Count Clear. Writing 0 to this bit has no affect 1h = Clear Hit/Miss Counter
7	CNTEN	R/W	1h	Cache Hit/Miss Count Enable. 0h = Disable 1h = Enable
6	RPOLICY	R/W	0h	Replacement policy for Cache. 0h = Random Replacement Policy 1h = Sequencial Replacement Policy
5	LINFLUSH	W	0h	Line Buffer Flush. This bit is used to flush the Line buffer on system bus Interface. This bit is self clearing. Writing 0 to this bit has no affect 1h = Trigger Flush
4	LINEN	R/W	1h	Line Buffer Enable. This bit is used to enable the Line buffer on system bus Interface. Disabling the Line buffer will flush it 0h = Disable 1h = Enable
3	CCHFLUSH	W	0h	Cache Flush. This bit is used to flush the cache on code bus Interface. This bit is self clearing. Writing 0 to this bit has no affect 1h = Trigger Flush
2-1	RESERVED	R	0h	Reserved
0	CCHEN	R/W	1h	Cache Enable. This bit is used to enable the cache. Disabling the cache will flush it 0h = Disable 1h = Enable

7.2.3.22 CCHSTA Register (Offset = 428h) [Reset = 00000000h]

CCHSTA is shown in Table 7-40.

Return to the Summary Table.

;Cache Status. This register gives cache status

Table 7-40. CCHSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	BUSY	R	1h	Busy. This bit indicate Cache is changing state 0h = Not Busy 1h = Busy
0	EN	R	1h	Enabled. This bit indicate whether cache is enabled or disabled 0h = Disabled 1h = Enabled

7.2.3.23 CNTHIT Register (Offset = 430h) [Reset = 00000000h]

CNTHIT is shown in Table 7-41.

Return to the Summary Table.

;Cache Hit Counter

Table 7-41. CNTHIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Hit Counter Value. This counter is cleared by writing CCHCTL.CNTCLR

7.2.3.24 CNTMISS Register (Offset = 434h) [Reset = 00000000h]

CNTMISS is shown in Table 7-42.

Return to the Summary Table.

;Cache Miss Counter

Table 7-42. CNTMISS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Miss Counter Value. This counter is cleared by writing CCHCTL.CNTCLR

7.2.3.25 CTL Register (Offset = 4FCh) [Reset = 00000000h]

CTL is shown in Table 7-43.

Return to the Summary Table.

;Control Register.

Table 7-43. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SWAPLOCK	R/W	0h	Swap Lock. If set, CTL.SWAP bit is blocked for writing. This bit is sticky 1 0h = Unlocked 1h = Locked
30-1	RESERVED	R	0h	Reserved
0	SWAP	R/W	0h	Swaps the logical to physical bank mapping. This bit has no effect if CTL.SPLMODE is 0 and is writable ony when CTL.SWAPLOCK is 0 0h = Bank is not swapped 1h = Bank is swapped

7.3 FLASH

7.3.1 FLASH Registers

Table 7-44 lists the memory-mapped registers for the FLASH registers. All register offset addresses not listed in Table 7-44 should be considered as reserved locations and the register contents should not be modified.

Table 7-44. FLASH Registers

Offset	Acronym	Register Name	Section
28h	IMASK	Interrupt Mask Register	Section 7.3.1.1
30h	RIS	Raw Interrupt Status Register	Section 7.3.1.2
38h	MIS	Masked Interrupt Status Register	Section 7.3.1.3
40h	ISET	Interrupt Set Register	Section 7.3.1.4
48h	ICLR	Interrupt Clear Register	Section 7.3.1.5
FCh	DESC	Hardware Version Description Register	Section 7.3.1.6
100h	CMDEXEC	Command Execute Register	Section 7.3.1.7
104h	CMDTYPE	Command Type Register	Section 7.3.1.8
108h	CMDCTL	Command Control Register	Section 7.3.1.9
120h	CMDADDR	Command Address Register	Section 7.3.1.10
124h	CMDBYTEN	Command Program Byte Enable Register	Section 7.3.1.11
130h	CMDDATA0	Command Data Register 0	Section 7.3.1.12
134h	CMDDATA1	Command Data Register 1	Section 7.3.1.13
138h	CMDDATA2	Command Data Register 2	Section 7.3.1.14
13Ch	CMDDATA3	Command Data Register Bits 127:96	Section 7.3.1.15
1D0h	CMDWEPROTA	Command Write Erase Protect A Register	Section 7.3.1.16
1D4h	CMDWEPROTB	Command Write Erase Protect B Register	Section 7.3.1.17
210h	CMDWEPROTNM	Command Write Erase Protect Non-Main Register	Section 7.3.1.18
214h	CMDWEPROTTR	Command Write Erase Protect Trim Register	Section 7.3.1.19
218h	CMDWEPROTEN	Command Write Erase Protect Engr Register	Section 7.3.1.20
3B0h	CFGCMD	Command Configuration Register	Section 7.3.1.21
3B4h	CFGPCNT	Pulse Counter Configuration Register	Section 7.3.1.22
3D0h	STATCMD	Command Status Register	Section 7.3.1.23
3D4h	STATADDR	Address Status Register	Section 7.3.1.24
3D8h	STATPCNT	Pulse Count Status Register	Section 7.3.1.25
3DCh	STATMODE	Mode Status Register	Section 7.3.1.26
3F0h	GBLINFO0	Global Information Register 0	Section 7.3.1.27
3F4h	GBLINFO1	Global Information Register 1	Section 7.3.1.28
3F8h	GBLINFO2	Global Information Register 2	Section 7.3.1.29
400h	BANK0INFO0	Bank Information Register 0 for Bank 0	Section 7.3.1.30
404h	BANK0INFO1	Bank Information Register 1 for Bank 0	Section 7.3.1.31
410h	BANK1INFO0	Bank Information Register 0 for Bank 1	Section 7.3.1.32
414h	BANK1INFO1	Bank Information Register 1 for Bank 1	Section 7.3.1.33

Complex bit access types are encoded to fit into small table cells. Table 7-45 shows the codes that are used for access types in this section.

Table 7-45. FLASH Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

Table 7-45. FLASH Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1.1 IMASK Register (Offset = 28h) [Reset = 00000000h]

IMASK is shown in Table 7-46.

Return to the Summary Table.

Interrupt Mask Register:;The IMASK register holds the current interrupt mask settings. Masked interrupts;are read in the MIS register. PSD compliant register.

Table 7-46. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DONE	R/W	0h	Interrupt mask for DONE:;0: Interrupt is disabled in MIS register;1: Interrupt is enabled in MIS register 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in IPSTANDARD.MIS will be set

7.3.1.2 RIS Register (Offset = 30h) [Reset = 00000000h]

RIS is shown in Table 7-47.

Return to the Summary Table.

Raw Interrupt Status Register:;The RIS register reflects all pending interrupts, regardless of masking. ;The RIS register allows the user to implement a poll scheme. A flag set in this;register can be cleared by writing a 1 to the ICLR register bit even if the ;corresponding IMASK bit is not enabled. A flag can be set by software by writing;a 1 to the ISET register. Reading the IIDX register will also clear the;corresponding bit in RIS. PSD compliant register.

Table 7-47. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DONE	R	0h	Flash wrapper operation completed.;This interrupt bit is set by firmware or the corresponding bit in the ISET register.;It is cleared by the corresponding bit in in the ICLR register or reading the IIDX register when this interrupt is the highest priority. 0h = Interrupt did not occur 1h = Interrupt occurred

7.3.1.3 MIS Register (Offset = 38h) [Reset = 00000000h]

MIS is shown in Table 7-48.

Return to the Summary Table.

Masked Interrupt Status Register:;The MIS register is a bit-wise AND of the contents of the IMASK and RIS ;registers. This is kept mainly for ARM compatibility, and has limited use since; the highest priority interrupt index is returned through the IIDX register.; PSD ;compliant register.

Table 7-48. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DONE	R	0h	Flash wrapper operation completed.;This masked interrupt bit reflects the bitwise AND of the corresponding RIS and IMASK bits. 0h = Masked interrupt did not occur 1h = Masked interrupt occurred

7.3.1.4 ISET Register (Offset = 40h) [Reset = 00000000h]

ISET is shown in Table 7-49.

Return to the Summary Table.

Interrupt Set Register:;The ISET register allows software to write a 1 to set corresponding interrupt. ;Safety:;This meets a safety requirement to allow software diagnostics to trigger ;interrupts.;PSD compliant register.

Table 7-49. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DONE	W	0h	0: No effect;1: Set the DONE interrupt in the RIS register 0h = Writing a 0 has no effect 1h = Set IPSTANDARD.RIS bit

7.3.1.5 ICLR Register (Offset = 48h) [Reset = 00000000h]

ICLR is shown in Table 7-50.

Return to the Summary Table.

Interrupt Clear Register. ;The ICLR register allows allows software to write a 1 to clear corresponding ;interrupt.;PSD compliant register.

Table 7-50. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DONE	W	0h	0: No effect;1: Clear the DONE interrupt in the RIS register 0h = Writing a 0 has no effect 1h = Clear IPSTANDARD.RIS bit

7.3.1.6 DESC Register (Offset = FCh) [Reset = 00000000h]

DESC is shown in Table 7-51.

Return to the Summary Table.

Hardware Version Description Register:;This register identifies the flash wrapper hardware version and feature set used.

Table 7-51. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	B40h	Module ID 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	4h	Feature set 0h = Minimum Value Fh = Maximum Value
11-8	INSTNUM	R	0h	Instance number 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	1h	Major Revision 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor Revision 0h = Smallest value Fh = Highest possible value

7.3.1.7 CMDEXEC Register (Offset = 100h) [Reset = 00000000h]

CMDEXEC is shown in Table 7-52.

Return to the Summary Table.

Command Execute Register:;Initiates execution of the command specified in the CMDTYPE register.;This register is blocked for writes after being written to 1 and prior to ;STATCMD.DONE being set by the flash wrapper hardware.;flash wrapper hardware clears this register after the processing of the command ;has completed.

Table 7-52. CMDEXEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Command Execute value;Initiates execution of the command specified in the CMDTYPE register. 0h = Command will not execute or is not executing in flash wrapper 1h = Command will execute or is executing in flash wrapper

7.3.1.8 CMDTYPE Register (Offset = 104h) [Reset = 00000000h]

CMDTYPE is shown in Table 7-53.

Return to the Summary Table.

Command Type Register;This register specifies the type of command to be executed by the flash wrapper;hardware.;This register is blocked for writes after CMDEXEC is written to a 1 and ;prior to STATCMD.DONE being set by the hardware to indicate that ;command execution has completed.

Table 7-53. CMDTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	SIZE	R/W	0h	Command size 0h = Operate on 1 flash word 1h = Operate on 2 flash words 2h = Operate on 4 flash words 3h = Operate on 8 flash words 4h = Operate on a flash sector 5h = Operate on an entire flash bank
3	RESERVED	R	0h	Reserved
2-0	COMMAND	R/W	0h	Command type 0h = No Operation 1h = Program 2h = Erase 4h = Mode Change - Perform a mode change only, no other operation. 5h = Clear Status - Clear status bits in FW_SMSTAT only. 6h = Blank Verify - Check whether a flash word is in the erased state.;This command may only be used with CMDTYPE.SIZE = ONEWORD

7.3.1.9 CMDCTL Register (Offset = 108h) [Reset = 00000000h]

CMDCTL is shown in Table 7-54.

Return to the Summary Table.

Command Control Register;This register configures specific capabilities of the state machine for related to;the execution of a command.;This register is blocked for writes after CMDEXEC is written to a 1 and ;prior to STATCMD.DONE being set by the hardware to indicate that ;command execution has completed.

Table 7-54. CMDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	DATAVEREN	R/W	0h	Enable invalid data verify. ;This checks for 0->1 transitions in the memory when;a program operation is initiated. If such a transition is found, the program will;fail with an error without executing the program. 0h = Disable 1h = Enable
20	SSERASEDIS	R/W	0h	Disable Stair-Step Erase. If set, the default VHV trim voltage setting will be used;for all erase pulses.;By default, this bit is reset, meaning that the VHV voltage will be stepped during;successive erase pulses. The step count, step voltage, begin and end voltages;are all hard-wired. 0h = Enable 1h = Disable
19-17	RESERVED	R	0h	Reserved
16	ADDRXLATEOVR	R/W	0h	Override hardware address translation of address in CMDADDR from a ;system address to a bank address and bank ID. Use data written to ;CMDADDR directly as the bank address. Use the value written to ;CMDCTL.BANKSEL directly as the bank ID. Use the value written to;CMDCTL.REGIONSEL directly as the region ID. 0h = Do not override 1h = Override
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12-9	REGIONSEL	R/W	0h	Bank Region;A specific region ID can be written to this field to indicate to which region an ;operation is to be applied if CMDCTL.ADDRXLATEOVR is set. 1h = Main Region 2h = Non-Main Region 4h = Trim Region 8h = Engr Region
8-6	RESERVED	R	0h	Reserved
5-4	BANKSEL	R/W	0h	Bank Select;A specific Bank ID can be written to this field to indicate to which bank an ;operation is to be applied if CMDCTL.ADDRXLATEOVR is set. 1h = Bank 0 2h = Bank 1 4h = Bank 2 8h = Bank 3 10h = Bank 4

Table 7-54. CMDCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MODESEL	R/W	0h	Mode;This field is only used for the Mode Change command type. Otherwise, bank;and pump modes are set automaticlly through the NW hardware. 0h = Read Mode 2h = Read Margin 0 Mode 4h = Read Margin 1 Mode 6h = Read Margin 0B Mode 7h = Read Margin 1B Mode 9h = Program Verify Mode Ah = Program Single Word Bh = Erase Verify Mode Ch = Erase Sector Eh = Program Multiple Word Fh = Erase Bank

7.3.1.10 CMDADDR Register (Offset = 120h) [Reset = 00000000h]

CMDADDR is shown in Table 7-55.

Return to the Summary Table.

Command Address Register:;This register forms the target address of a command. The use cases are as;follows:;1) For single-word program, this address indicates the flash bank word to be; programmed.;2) For multi-word program, this address indicates the first flash bank address; for the program. The address will be incremented for further words.;3) For sector erase, this address indicates the sector to be erased.;4) For bank erase, the address indicates the bank to be erased.;Note the address written to this register will be submitted for translation to the;flash wrapper address translation interface, and the translated address;will be used to access the bank. However, if the;CMDCTL.ADDRXLATEOVR bit is set, then the address written to this register will;be used directly as the bank address.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.

Table 7-55. CMDADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Address value 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.11 CMDBYTEN Register (Offset = 124h) [Reset = 00000000h]

CMDBYTEN is shown in Table 7-56.

Return to the Summary Table.

Command Program Byte Enable Register:;This register forms a per-byte enable for programming data. For data bytes to;be programmed, a 1 must be written to the corresponding bit in this register.;Normally, all bits are written to 1, allowing program of full flash words.;However, leaving some bits 0 allows programming of 8-bit, 16-bit, 32-bit;or 64-bit portions of a flash word.;During verify, data bytes read from the flash will not be checked if the;corresponding CMDBYTEN bit is 0.;ECC data bytes are protected by the 1-2 MSB bits in this register, depending on;the presence of ECC and the flash word data width.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;This register is written to all 0 after the completion of all flash wrapper commands.

Table 7-56. CMDBYTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Command Byte Enable value.;A 1-bit per flash word byte value is placed in this register. 0h = Minimum value of VAL 0003FFFFh = Maximum value of VAL

7.3.1.12 CMDDATA0 Register (Offset = 130h) [Reset = 00000000h]

CMDDATA0 is shown in Table 7-57.

Return to the Summary Table.

Command Data Register 0;This register forms the data for a command. ;For DATAWIDTH == 128: This register represents bits 31:0 of flash word data register 0.;For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 0.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;This register is used to aggregate masking for bits that do not;require additional program pulses during program operations, and will be;written to all 1 after the completion of all flash wrapper commands.;Use cases for the CMDDATA* registers are as follows:;1) Program - These registers contain the data to be programmed.;2) Erase - These registers are not used.

Table 7-57. CMDDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.13 CMDDATA1 Register (Offset = 134h) [Reset = 00000000h]

CMDDATA1 is shown in Table 7-58.

Return to the Summary Table.

Command Data Register 1;This register forms the data for a command. ;For DATAWIDTH == 128: This register represents bits 63:32 of flash word data register 0.;For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 0.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to CMDSTAT.DONE being set by the flash wrapper;hardware.;This register is used to aggregate masking for bits that do not;require additional program pulses during program operations, and will be;written to all 1 after the completion of all flash wrapper commands.;Use cases for the CMDDATA* registers are as follows:;1) Program - These registers contain the data to be programmed.;2) Erase - These registers are not used.

Table 7-58. CMDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.14 CMDDATA2 Register (Offset = 138h) [Reset = 00000000h]

CMDDATA2 is shown in Table 7-59.

Return to the Summary Table.

Command Data Register 2;This register forms the data for a command. ;For DATAWIDTH == 128: This register represents bits 95:64 of flash word data register 0.;For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 1.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;This register is used to aggregate masking for bits that do not;require additional program pulses during program operations, and will be;written to all 1 after the completion of all flash wrapper commands.;Use cases for the CMDDATA* registers are as follows:;1) Program - These registers contain the data to be programmed.;2) Erase - These registers are not used.

Table 7-59. CMDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.15 CMDDATA3 Register (Offset = 13Ch) [Reset = 00000000h]

CMDDATA3 is shown in Table 7-60.

Return to the Summary Table.

Command Data Register 3;This register forms the data for a command. ;For DATAWIDTH == 128: This register represents bits 127:96 of flash word data register 0.;For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 1.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;This register is used to aggregate masking for bits that do not;require additional program pulses during program operations, and will be;written to all 1 after the completion of all flash wrapper commands.;Use cases for the CMDDATA* registers are as follows:;1) Program - These registers contain the data to be programmed.;2) Erase - These registers are not used.

Table 7-60. CMDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.16 CMDWEPROTA Register (Offset = 1D0h) [Reset = 00000000h]

CMDWEPROTA is shown in Table 7-61.

Return to the Summary Table.

Command WriteErase Protect A Register;This register allows the first 32 sectors of the main region to be protected from;program or erase, with 1 bit protecting each sector. If the main region size is smaller than 32;sectors, then this register provides protection for the whole region.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;In addition, this register is used to aggregate masking for sectors that do not;require additional erase pulses during bank erase operations, and will be;written to all 1 after the completion of all flash wrapper commands.

Table 7-61. CMDWEPROTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Each bit protects 1 sector.;bit [0]: When 1, sector 0 of the flash memory will be protected from program; and erase.;bit [1]: When 1, sector 1 of the flash memory will be protected from program; and erase.; :; :;bit [31]: When 1, sector 31 of the flash memory will be protected from program; and erase. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.17 CMDWEPROTB Register (Offset = 1D4h) [Reset = 00000000h]

CMDWEPROTB is shown in Table 7-62.

Return to the Summary Table.

Command WriteErase Protect B Register;This register allows main region sectors to be protected from program and;erase. Each bit corresponds to a group of 8 sectors. ;There are multiple cases for how these protect bits are applied:;1. Single-bank system, CMDWEPROTA register present:; The first 32 sectors are protected via the CMDWEPROTA register. Thus, the; protection given by the bits in CMDWEPROTB begin with sector 32.;2. Single-bank system, CMDWEPROTA register not present:; The protection given by the bits in CMDWEPROTB begin with sector 0.;3. Multi-bank system, CMDWEPROTA register present - Bank 0: ; The first 32 sectors of bank 0 are protected via the CMDWEPROTA register.; Thus, only bits 4 and above of CMDWEPROTB would be applicable to bank 0.; The protection of bit 4 and above would begin at sector 32. Bits 3:0; of WEPROTB are ignored for bank 0.;4. Multi-bank system, CMDWEPROTA register present, Banks 1-N:; For banks other than bank 0 in a multi-bank system, CMDWEPROTA has; no effect, so the bits in CMDWEPROTB will protect these banks starting; from sector 0.;5. Multi-bank system, CMDWEPROTA register not present:; The bits in CMDWEPROTB will protect any of the banks starting from sector 0.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;In addition, this register is used to aggregate masking for sectors that do not;require additional erase pulses during bank erase operations, and will be;written to all 1 after the completion of all flash wrapper commands.

Table 7-62. CMDWEPROTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Each bit protects a group of 8 sectors. When a bit is 1, the associated 8 sectors;in the flash will be protected from program and erase. A maximum of 256;sectors can be protected with this register. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.18 CMDWEPROTNM Register (Offset = 210h) [Reset = 00000000h]

CMDWEPROTNM is shown in Table 7-63.

Return to the Summary Table.

Command WriteErase Protect Non-Main; Register;This register allows non-main region region sectors to be protected;from program and erase. Each bit corresponds to 1 sector. ;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;In addition, this register is used to aggregate masking for sectors that do not;require additional erase pulses during bank erase operations, and will be;written to all 1 after the completion of all flash wrapper commands.

Table 7-63. CMDWEPROTNM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	3h	Each bit protects 1 sector.;bit [0]: When 1, sector 0 of the non-main region will be protected from program; and erase.;bit [1]: When 1, sector 1 of the non-main region will be protected from program; and erase.; :; ::bit [31]: When 1, sector 31 of the non-main will be protected from program; and erase. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.19 CMDWEPROTTR Register (Offset = 214h) [Reset = 00000000h]

CMDWEPROTTR is shown in Table 7-64.

Return to the Summary Table.

Command WriteErase Protect Trim; Register;This register allows trim region sectors to be protected;from program and erase. Each bit corresponds to 1 sector. ;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;In addition, this register is used to aggregate masking for sectors that do not;require additional erase pulses during bank erase operations, and will be;written to all 1 after the completion of all flash wrapper commands.

Table 7-64. CMDWEPROTTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	Each bit protects 1 sector.;bit [0]: When 1, sector 0 of the engr region will be protected from program; and erase.;bit [1]: When 1, sector 1 of the engr region will be protected from program; and erase.; :; :;bit [31]: When 1, sector 31 of the engr region will be protected from program; and erase. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.20 CMDWEPROTEN Register (Offset = 218h) [Reset = 00000000h]

CMDWEPROTEN is shown in Table 7-65.

Return to the Summary Table.

Command WriteErase Protect Engr; Register;This register allows engr region sectors to be protected;from program and erase. Each bit corresponds to 1 sector. ;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.;In addition, this register is used to aggregate masking for sectors that do not;require additional erase pulses during bank erase operations, and will be;written to all 1 after the completion of all flash wrapper commands.

Table 7-65. CMDWEPROTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	1h	Each bit protects 1 sector.;bit [0]: When 1, sector 0 of the engr region will be protected from program; and erase.;bit [1]: When 1, sector 1 of the engr region will be protected from program; and erase.; :; :;bit [31]: When 1, sector 31 of the engr region will be protected from program; and erase. 0h = Minimum value of VAL FFFFFFFFh = Maximum value of VAL

7.3.1.21 CFGCMD Register (Offset = 3B0h) [Reset = 00000000h]

CFGCMD is shown in Table 7-66.

Return to the Summary Table.

Command Configuration Register;This register configures specific capabilities of the state machine for related to;the execution of a command.;This register is blocked for writes after CMDEXEC is written to a 1 and ;prior to STATCMD.DONE being set by the hardware to indicate that ;command execution has completed.

Table 7-66. CFGCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3-0	WAITSTATE	R/W	2h	Wait State setting for verify reads 0h = Minimum value Fh = Maximum value

7.3.1.22 CFGPCNT Register (Offset = 3B4h) [Reset = 00000000h]

CFGPCNT is shown in Table 7-67.

Return to the Summary Table.

Pulse Counter Configuration Register;This register allows further configuration of maximum pulse counts for ;program and erase operations.;This register is blocked for writes after a 1 is written to the CMDEXEC;register and prior to STATCMD.DONE being set by the flash wrapper;hardware.

Table 7-67. CFGPCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-17	RESERVED	R	0h	Reserved
16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-4	MAXPCNTVAL	R/W	0h	Override maximum pulse counter with this value. ;If MAXPCNTOVR = 0, then this field is ignored.;If MAXPCNTOVR = 1 and MAXERSPCNTOVR = 0, then this value will be used ;to override the max pulse count for both program and erase. Full max value;will be {4'h0, MAXPCNTVAL} .;If MAXPCNTOVR = 1 and MAXERSPCNTOVR = 1, then this value will be used;to override the max pulse count for program only. Full max value will be;{4'h0, MAXPCNTVAL}. 0h = Minimum value FFh = Maximum value
3-1	RESERVED	R	0h	Reserved
0	MAXPCNTOVR	R/W	0h	Override hard-wired maximum pulse count. If MAXERSPCNTOVR;is not set, then setting this value alone will override the max pulse count for;both program and erase. If MAXERSPCNTOVR is set, then this bit will only;control the max pulse count setting for program.;By default, this bit is 0, and a hard-wired max pulse count is used. 0h = Use hard-wired (default) value for maximum pulse count 1h = Use value from MAXPCNTVAL field as maximum puse count

7.3.1.23 STATCMD Register (Offset = 3D0h) [Reset = 00000000h]

STATCMD is shown in Table 7-68.

Return to the Summary Table.

Command Status Register;This register contains status regarding completion and errors of command;execution.

Table 7-68. STATCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	FAILMISC	R	0h	Command failed due to error other than write/erase protect violation or verify;error. This is an extra bit in case a new failure mechanism is added which;requires a status bit. 0h = No Fail 1h = Fail
11-9	RESERVED	R	0h	Reserved
8	FAILINVDATA	R	0h	Program command failed because an attempt was made to program a stored;0 value to a 1. 0h = No Fail 1h = Fail
7	FAILMODE	R	0h	Command failed because a bank has been set to a mode other than READ.;Program and Erase commands cannot be initiated unless all banks are in READ;mode. 0h = No Fail 1h = Fail
6	FAILILLADDR	R	0h	Command failed due to the use of an illegal address 0h = No Fail 1h = Fail
5	FAILVERIFY	R	0h	Command failed due to verify error 0h = No Fail 1h = Fail
4	FAILWEPROT	R	0h	Command failed due to Write/Erase Protect Sector Violation 0h = No Fail 1h = Fail
3	RESERVED	R	0h	Reserved
2	CMDINPROGRESS	R	0h	Command In Progress 0h = Complete 1h = In Progress
1	CMDPASS	R	0h	Command Pass - valid when CMD_DONE field is 1 0h = Fail 1h = Pass
0	CMDDONE	R	0h	Command Done 0h = Not Done 1h = Done

7.3.1.24 STATADDR Register (Offset = 3D4h) [Reset = 00000000h]

STATADDR is shown in Table 7-69.

Return to the Summary Table.

Current Address Counter Value;Read only register giving read access to the state machine current address.;A bank id, region id and address are stored in this register and are incremented as;necessary during execution of a command.

Table 7-69. STATADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-21	BANKID	R	1h	Current Bank ID;A bank indicator is stored in this register which represents the current bank on;which the state machine is operating. There is 1 bit per bank. 1h = Bank 0 2h = Bank 1 4h = Bank 2 8h = Bank 3 10h = Bank 4
20-16	REGIONID	R	1h	Current Region ID;A region indicator is stored in this register which represents the current flash ;region on which the state machine is operating. 1h = Main Region 2h = Non-Main Region 4h = Trim Region 8h = Engr Region
15-0	BANKADDR	R	0h	Current Bank Address;A bank offset address is stored in this register. 0h = Minimum value FFFFh = Maximum value

7.3.1.25 STATPCNT Register (Offset = 3D8h) [Reset = 00000000h]

STATPCNT is shown in Table 7-70.

Return to the Summary Table.

Current Pulse Count Register:;Read only register giving read access to the state machine current pulse count;value for program/erase operations.

Table 7-70. STATPCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	PULSECNT	R	0h	Current Pulse Counter Value 0h = Minimum value FFFh = Maximum value

7.3.1.26 STATMODE Register (Offset = 3DCh) [Reset = 00000000h]

STATMODE is shown in Table 7-71.

Return to the Summary Table.

Mode Status Register;Indicates one or more banks which not in READ mode, and it indicates the mode;which the bank(s) are in.

Table 7-71. STATMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	BANK1TRDY	R	0h	Bank 1T Ready.;Bank(s) are ready for 1T access. This is accomplished when the bank and pump;have been trimmed. 0h = Not ready 1h = Ready
16	BANK2TRDY	R	0h	Bank 2T Ready.;Bank(s) are ready for 2T access. This is accomplished when the pump has;fully driven power rails to the bank(s). 0h = Not ready 1h = Ready
15-12	RESERVED	R	0h	Reserved
11-8	BANKMODE	R	0h	Indicates mode of bank(s) that are not in READ mode 0h = Read Mode 2h = Read Margin 0 Mode 4h = Read Margin 1 Mode 6h = Read Margin 0B Mode 7h = Read Margin 1B Mode 9h = Program Verify Mode Ah = Program Single Word Bh = Erase Verify Mode Ch = Erase Sector Eh = Program Multiple Word Fh = Erase Bank
7-5	RESERVED	R	0h	Reserved
4-2	RESERVED	R	0h	Reserved
1-0	BANKNOTINRD	R	0h	Bank not in read mode.;Indicates which banks are not in READ mode. There is 1 bit per bank. 1h = Bank 0 2h = Bank 1 4h = Bank 2 8h = Bank 3 10h = Bank 4

7.3.1.27 GBLINFO0 Register (Offset = 3F0h) [Reset = 00000000h]

GBLINFO0 is shown in Table 7-72.

Return to the Summary Table.

Global Info 0 Register;Read only register detailing information about sector size and number of banks;present.

Table 7-72. GBLINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	NUMBANKS	R	2h	Number of banks instantiated;Minimum: 1;Maximum: 5 1h = Minimum value 5h = Maximum value
15-0	SECTORSIZE	R	800h	Sector size in bytes 400h = Sector size is ONEKB 800h = Sector size is TWOKB

7.3.1.28 GBLINFO1 Register (Offset = 3F4h) [Reset = 00000000h]

GBLINFO1 is shown in Table 7-73.

Return to the Summary Table.

Global Info 1 Register;Read only register detailing information about data, ecc and redundant data;widths in bits.

Table 7-73. GBLINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	REDWIDTH	R	4h	Redundant data width in bits 0h = Redundant data width is 0. Redundancy/Repair not present. 2h = Redundant data width is 2 bits 4h = Redundant data width is 4 bits
15-13	RESERVED	R	0h	Reserved
12-8	ECCWIDTH	R	0h	ECC data width in bits 0h = ECC data width is 0. ECC not used. 8h = ECC data width is 8 bits 10h = ECC data width is 16 bits
7-0	DATAWIDTH	R	80h	Data width in bits 40h = Data width is 64 bits 80h = Data width is 128 bits

7.3.1.29 GBLINFO2 Register (Offset = 3F8h) [Reset = 00000000h]

GBLINFO2 is shown in Table 7-74.

Return to the Summary Table.

Global Info 2 Register;Read only register detailing information about the number of data registers;present.

Table 7-74. GBLINFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	DATAREGISTERS	R	1h	Number of data registers present. 1h = Minimum value of DATAREGISTERS 8h = Maximum value of DATAREGISTERS

7.3.1.30 BANK0INFO0 Register (Offset = 400h) [Reset = 00000000h]

BANK0INFO0 is shown in Table 7-75.

Return to the Summary Table.

Bank Info 0 Register for bank 0.;Read only register detailing information about Main region size in the bank.

Table 7-75. BANK0INFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	MAINSIZE	R	100h	Main region size in sectors;Minimum: 0x8 (8);Maximum: 0x200 (512) 8h = Minimum value of MAINSIZE 200h = Maximum value of MAINSIZE

7.3.1.31 BANK0INFO1 Register (Offset = 404h) [Reset = 00000000h]

BANK0INFO1 is shown in Table 7-76.

Return to the Summary Table.

Bank Info1 Register for bank 0.;Read only register detailing information about Non-Main, Trim, and Engr;region sizes in the bank.

Table 7-76. BANK0INFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	ENGRSIZE	R	1h	Engr region size in sectors;Minimum: 0x0 (0);Maximum: 0x10 (16) 0h = Minimum value of ENGRSIZE 20h = Maximum value of ENGRSIZE
15-8	TRIMSIZE	R	1h	Trim region size in sectors;Minimum: 0x0 (0);Maximum: 0x10 (16) 0h = Minimum value of TRIMSIZE 20h = Maximum value of TRIMSIZE
7-0	NONMAINSIZE	R	2h	Non-main region size in sectors;Minimum: 0x0 (0);Maximum: 0x10 (16) 0h = Minimum value of NONMAINSIZE 20h = Maximum value of NONMAINSIZE

7.3.1.32 BANK1INFO0 Register (Offset = 410h) [Reset = 00000000h]

BANK1INFO0 is shown in Table 7-77.

Return to the Summary Table.

Bank Info 0 Register for bank 1.;Read only register detailing information about Main region size in the bank.

Table 7-77. BANK1INFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	MAINSIZE	R	100h	Main region size in sectors;Minimum: 0x8 (8);Maximum: 0x200 (512) 8h = Minimum value of MAINSIZE 200h = Maximum value of MAINSIZE

7.3.1.33 BANK1INFO1 Register (Offset = 414h) [Reset = 00000000h]

BANK1INFO1 is shown in Table 7-78.

Return to the Summary Table.

Bank Info1 Register for bank 1.;Read only register detailing information about Non-Main, Trim, and Engr;region sizes in the bank.

Table 7-78. BANK1INFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	ENGRSIZE	R	1h	Engr region size in sectors;Minimum: 0x0 (0);Maximum: 0x10 (16) 0h = Minimum value of ENGRSIZE 20h = Maximum value of ENGRSIZE
15-8	TRIMSIZE	R	1h	Trim region size in sectors 0h = Minimum value of TRIMSIZE 20h = Maximum value of TRIMSIZE
7-0	NONMAINSIZE	R	2h	Non-main region size in sectors 0h = Minimum value of NONMAINSIZE 20h = Maximum value of NONMAINSIZE

Chapter 8

Hardware Security Module (HSM)

This section describes the Hardware Security Module (HSM).

8.1 Introduction

The CC27xx devices have an integrated hardware security module (HSM) supporting an isolated environment for cryptographic, key management, secure counters, and random number generation operations. Selected algorithms are protected from differential power analysis (DPA) side-channel attacks. Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), the system supports secure and future-proof IoT applications to be easily built on the platform.

8.2 Overview

The following cryptographic functions using energy efficient accelerators and RNG functions are accelerated by the HSM:

- Key Agreement Schemes
  - Elliptic Curve Diffie-Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic Curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE) (See Note below)
  - Diffie Hellman with static or ephemeral keys (DH, and DHE)
- Key Derivation Methods:
  - Random (from DRBG)
  - SHA2 HMAC PRF (Pseudorandom Function)
  - AES CMAC PRF
- Signature Processing
  - Elliptic Curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
  - Edwards-curve Digital Signature Algorithm (EdDSA)
  - RSA PKCS #1 v1.5
  - RSA PSS
- Message Authentication Codes
  - AES CBC-MAC
  - AES CMAC
  - HMAC with SHA2-224, SHA2-256, SHA2-384, and SHA2-512
- Block Cipher Modes of Operation
  - AES CCM and AES CCM* (CCM-Star)
  - AES GCM
  - AES ECB
  - AES CBC
  - AES CTR
- Hash Algorithms
  - SHA2-224
  - SHA2-256
  - SHA2-384
  - SHA2-512
- Random Number Generation:
  - NIST SP800-90B compliant TRNG (True Random Number Generator)
  - AES-CTR DRBG (Deterministic Random Bit Generator)

Cryptographic key sizes and types include:

- Advanced Encryption Standard (AES) key sizes of 128, 192, and 256bits
- RSA key sizes up to 3072-bits (Sign and Verify supported), and up to 4096-bits (Verify only)
- Diffie-Hellman key sizes of 2048-bits and 3072-bits
- Elliptic Curve Support
  - Short Weierstrass
    - NIST-P224 (secp224r1), NIST-P256 (secp256r1), NIST-P384 (secp384r1), NIST-P521 (secp521r1)

    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
  - Montgomery
    - Curve25519
  - Twisted Edwards form, such as:
    - Ed25519

DPA countermeasures are implemented for:

- AES operations
- ECDH operations involving private key material
- ECDSA

The HSM executes the HSM firmware from a secured flash region. The HSM firmware is verified by the HSM ROM before the HSM processor starts executing it. Secure firmware update of the HSM firmware image on-chip is supported by the system ROM bootcode and the HSM ROM.

The HSM also has its own data RAM region that is not accessible to the rest of the system (system CPU, DMA, debug access, and so on). The data RAM region is retained in low power modes, supporting quick power up of the HSM and retention of key material. In addition to the storage of key material in data RAM, the HSM supports importing and exporting wrapped key material (NIST SP800-38F) with a key unique to the device, known as a HW Unique Key (HUK). This allows the wrapped keys to be securely stored anywhere in the system's nonvolatile (Flash) memory.

The HSM is accessible to the application running on the system CPU in a controlled manner via the HSM mailbox interface. The HSM is a bus controller in the device and can access the system memory directly enabling better efficiency for moving data in and out during cryptographic operations.

The SimpleLink™ CC27xx software development kit (SDK) includes the encrypted and signed HSM firmware needed to be programmed on-chip for the HSM operation and drivers for all HSM functions. The SDK includes both SimpleLink™ APIs and Platform Security Architecture (PSA) APIs to enable easy use of the HSM features.

Note

Algorithm is implemented on the applications core using low-level HSM public key accelerator commands for acceleration.

8.3 One-Time-Programmable (OTP) Controller

The internal OTP controller allows HSM to store the secure assets on the OTP emulated region of the flash. The controller ensures confidentiality of the asset by delivering the data directly to the flash.

For each OTP transaction, the controller generates an interrupt to the CPU requesting exclusive access to the shared flash controller. This ensures that the OTP operation doesn't interfere with the normal software operation of the user application.

8.3.1 High-level Sequence to handle OTP requests

- OTP controller will trigger an interrupt to CPU when it needs exclusive access to the Flash Controller.
- CPU needs to safely park all its operations that might access the Flash Controller.
- Acknowledge the OTP controller interrupt.
- Wait until OTP controller completes the operation. OTP controller will generate an interrupt on transaction completion.
- Acknowledge operation completion interrupt.
- Resume any parked tasks.

8.4 Mailbox and Register Access Firewall

The HSM MMR address space is divided into 3 sub-section.

- Mailbox 1

- Mailbox 2
- Control Registers

Each of these sub-sections have individual security access controls configured via TCM.

8.5 DMA Firewall

The DMA firewall is a concatenation of two back-to-back firewalls. The first stage is explained below and the second stage is same as master TrustZone™ in the system and controlled by TCM.

- DMA performing secure transaction for secure mailbox task:
  - All addresses are accessible
- DMA performing non-secure transaction for non-secure mailbox task:
  - Non-secure accesses are allowed i.e. access to address space with bit-28 set to '1'
  - Secure accesses are blocked i.e. access to address space with bit-28 set to '0'

Blocked transactions will internally cause DMA transaction error. This firewall can be enabled/disabled via CTL.DMAFWDIS.

8.6 CoProcessor

HSM allows direct delivery of KEY to the LAES via the co-processor command token.

8.7 HSM FW

Much of the cryptographic functionality that the HSM provides is facilitated by way of the Hardware Security Modules Firmware (HSM FW). The HSM IP will always perform verification of the HSM FW via a RSA 3K public key to ensure that the HSM FW has been properly signed by the TI (part Manufacturer) RSA 3K private key. This ensures that only TI sanctioned HSM FW can be used. Note that the HSM FW will not be programmed to the device from TI. Just as the customer is expected to program their own application and xCFG sectors, the customer is also expected to program the HSM FW as necessary.

Note that the HSM FW consumes at most 96KB of main flash. The System ROM will always write, erase and read protect the upper/last 96KB of main flash for this purpose. Because of this, the last 96KB of main flash will not be usable for application purposes and should be considered to be a reserved region. The HSM FW has both a version and a rollback ID associated with it, both of which can be requested from a device by sending the Get System Information SACI command. The version is used for quickly comparing one HSM FW to another. The rollback ID is used to facilitate anti-rollback protection. This means that if there ever comes a time in which a critical security vulnerability is to be found in a version of the HSM FW that has already been released to the public, TI will work to resolve the vulnerability with priority and release a patched HSM FW version. This version will include an incremented rollback ID. Once this theoretical patched HSM FW has been programmed to the devices in the field, those devices will be unable to accept the older and still vulnerable HSM FW versions which protects the devices from being rolled back to a previously insecure HSM FW version.

Note

Note: If a Chip Erase is performed on the device then anti-rollback protections are reset. Thus, a device which has undergone a SACI Chip Erase will once again accept an older potentially vulnerable HSM FW image. It is the expectation of the customer that the Guidelines for Securely configuring the device are followed so that this cannot happen.

8.7.1 Acquiring the latest HSM FW

The latest HSM firmware can be found in the SimpleLink™ Low Power F3 SDK, please reference the Software Users Guide for more information. This HSM FW binary file will not only be signed by TI's RSA 3K private key but also be encrypted by TI's AES symmetric key.

8.7.2 Programming HSM FW

There are two methods of programming the HSM FW to a device. Please see the SDK's Users Guide and or Release Notes for simple instructions for getting started

- Provisioning via SACI command
  - This method is intended to be used in sequence with the application programming on all devices in a manufacturing line.
  - Trigger the provisioning of the HSM FW and transfer the entire HSM FW to the device
  - The device will go through a series of verification steps and shortly respond with a status code based on the result
- Over the Air (OTA) Update
  - This method is nearly identical to how a secure boot update takes place.
  - Assuming a new HSM FW version update is received via some future SDK release. The customer may choose to transfer this binary file OTA to the devices in the field.
  - Note that since the maximum size of HSM FW is 96KB, your devices memory map must allow a 96KB region of main flash to be used for staging of the HSM FW update
  - Once the new HSM FW has been staged in main flash the application must utilize the Section 11.3 by:
    1. Calling HapiSbSetUpdateImageAddress(sector_addr) to specify the sector address in which the new HSM FW has been staged in (must be sector aligned)
    2. Calling HapiSbSetId(id) to specify the request ID for ROM. Using a value of 0x01 to specify ROM to perform an HSM FW Update on the HSM FW that's been staged at the already specified Update Image Address
    3. Reset the device via the HapiResetDevice() function so that the device can reset into ROM such that ROM can process the update
  - The result of the HSM FW update will be stored in the ROM API Status field. This can be retrieved by your application via the HapiSbGetStatus() function and if the HSM FW update has completed successfully you can expect to see a value of 0x01 (UPDATE_SUCCESS).

8.7.3 Optional Customer Signing of HSM FW

Just as the device will only accept TI sanctioned HSM FW images, so can the customer require the HSM FW images be sanctioned by them. To do this, the customer must have their own RSA 3K private/public key pair. The public key hash must be configured via the SCFG.hsmPublicKeyHash field that can be found in Section 10.4. Once the device has been programmed with this configuration, the device will only accept HSM FW updates which have been signed by both TI's and the customer's RSA 3K private key. A script for signing the HSM FW with the customers RSA 3K private key can be found in the SDK.

Note

Note: Refer to the SDK Users guide and or Release Notes for simple instructions for getting started

8.8 HSM Registers

Table 8-1 lists the memory-mapped registers for the HSM registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. HSM Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 8.8.1
4h	CTL	Control Register	Section 8.8.2
8h	CHARCTL	Control Register	Section 8.8.3
Ch	BIST	BIST for CRNG	Section 8.8.4

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. HSM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.8.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 8-3.

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;Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 8-3. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	654Fh	Module identification contains a unique peripheral identification number.
15-12	STDIPOFF	R	0h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP
3-0	MINREV	R	0h	Minor revision of IP

8.8.2 CTL Register (Offset = 4h) [Reset = 00000000h]

CTL is shown in Table 8-4.

Return to the Summary Table.

;Control Register

Table 8-4. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPUIDUNLK	R/W	1h	CPUID Lock. Sets sticky '0' lock for CTL.CPUIDSEL 0h = Lock 1h = Unlock
30	CPUIDSEL	R/W	0h	CPUID Select. Selects between ROMFW CPUID and Application CPUID 0h = Dassert 1h = Assert
29-8	RESERVED	R	0h	Reserved
7	REFMARK	R/W	0h	Refresher Marker. Trigger writting refresh marker. This bit is auto cleared when programming is done 0h = Done 1h = Trigger/Busy
6	DMAFWDIS	R/W	0h	DMA Firewall Disable 0h = DMA Firewall Enabled 1h = DMA Firewall Disabled
5	OTPBUSY	R	0h	OTP Busy. OTP contoller is busy
4	OTPEVTST	R	0h	OTP Event Status. 0h = OTP Done 1h = OTP Start
3	OTPEVTCLR	W	0h	OTP Event Clear 1h = Request PKA Abort
2	OTPEVTEN	R/W	0h	OTP Event Enable 0h = OTP Event Disable 1h = OTP Event Enable
1	PKABORT	W	0h	PKA Abort. Writing 1 to this bit requests PKA Abort, writing 0 has no effect 1h = Request PKA Abort
1-0	RESERVED	R	0h	Reserved

8.8.3 CHARCTL Register (Offset = 8h) [Reset = 00000000h]

CHARCTL is shown in Table 8-5.

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;Characterization Controls for FRO

Table 8-5. CHARCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-8	FROSEL	R/W	0h	Selects FRO to characterize
7-3	RESERVED	R	0h	Reserved
2	DLYSEL	R/W	0h	Selects delay in target FRO.This input must only be changed when CHARCTL.FROEN = 0 0h = Selects the full chain length 1h = Selects a tap on the approx. 95% of full length
1	FROEN	R/W	0h	Enables selected FRO 0h = Disabled 1h = Enabled
0	EN	R/W	0h	Enables` characterization 0h = Disabled 1h = Enabled

8.8.4 BIST Register (Offset = Ch) [Reset = 00000000h]

BIST is shown in Table 8-6.

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;BIST Controls and Status for CRNG

Table 8-6. BIST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	RDY	R	0h	CRNG BIST ready. When 1, BIST and health checks are complete
17	CMPLT	R	0h	CRNG BIST Complete. When 1, BIST checks are done
16	ERR	R	0h	CRNG BIST Error. When 1, BIST failed
15-1	RESERVED	R	0h	Reserved
0	RSTRT	R/W	0h	CRNG BIST Restart. When 1, starts BIST sequence. Ignored when BIST.RDY = 0

8.9 HSMCRYPTO Registers

Table 8-7 lists the memory-mapped registers for the HSMCRYPTO registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified.

Table 8-7. HSMCRYPTO Registers

Offset	Acronym	Register Name	Section
0h	MB1IN	Input Mailbox 1	Section 8.9.1
0h	MB1OUT	Output Mailbox 1	Section 8.9.2
400h	MB2IN	Input Mailbox 2	Section 8.9.3
400h	MB2OUT	Output Mailbox 2	Section 8.9.4
3E00h	AICPOL	AIC Polarity Control Register	Section 8.9.5
3E04h	AICTYPE	AIC Type Control Register	Section 8.9.6
3E08h	AICEN	AIC Enable Control Register	Section 8.9.7
3E0Ch	AICRSTA	AIC Raw Source Status Register	Section 8.9.8
3E0Ch	AICENSET	AIC Enable Set Registers	Section 8.9.9
3E10h	AICENSTA	AIC Enabled Status Register	Section 8.9.10
3E10h	AICACK	AIC Acknowledge Register	Section 8.9.11
3E14h	AICENCLR	AIC Enable Clear Register	Section 8.9.12
3E18h	AICOPT	AIC Options Register	Section 8.9.13
3E1Ch	AICVER	AIC Version Register	Section 8.9.14
3F00h	MBSTA	Mailbox Status Register	Section 8.9.15
3F00h	MBCTL	Mailbox Control Register	Section 8.9.16
3F04h	MBRSTA	Raw Mailbox Status Register	Section 8.9.17
3F04h	MBRST	Mailbox Reset Register. Only Master Host can write into this register	Section 8.9.18
3F08h	MBLNKID	Mailbox Status - linked Host IDs Register	Section 8.9.19
3F0Ch	MBOUTID	Mailbox Status - output Host IDs Register	Section 8.9.20
3F10h	MBLCKOUT	Host or Mailbox lockout control Register	Section 8.9.21
3FE0h	MODSTA	Module Status Register	Section 8.9.22
3FF4h	OPTIONS2	Configured options(2)	Section 8.9.23
3FF8h	OPTIONS	Configured options(1)	Section 8.9.24
3FFCh	VERSION	Version register	Section 8.9.25

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. HSMCRYPTO Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.9.1 MB1IN Register (Offset = 0h) [Reset = 00000000h]

MB1IN is shown in Table 8-9.

Return to the Summary Table.

Input Mailbox 1

Table 8-9. MB1IN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MEM	R	0h	Input Mailbox Memory

8.9.2 MB1OUT Register (Offset = 0h) [Reset = 00000000h]

MB1OUT is shown in Table 8-10.

Return to the Summary Table.

Output Mailbox 1

Table 8-10. MB1OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MEM	W	0h	Output Mailbox Memory

8.9.3 MB2IN Register (Offset = 400h) [Reset = 00000000h]

MB2IN is shown in Table 8-11.

Return to the Summary Table.

Input Mailbox 2

Table 8-11. MB2IN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MEM	R	0h	Input Mailbox Memory

8.9.4 MB2OUT Register (Offset = 400h) [Reset = 00000000h]

MB2OUT is shown in Table 8-12.

Return to the Summary Table.

Output Mailbox 2

Table 8-12. MB2OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MEM	W	0h	Output Mailbox Memory

8.9.5 AICPOL Register (Offset = 3E00h) [Reset = 00000000h]

AICPOL is shown in Table 8-13.

Return to the Summary Table.

AIC Polarity Control Register

Table 8-13. AICPOL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Polarity 0h = Low level/falling edge 1h = High level/rising edge
3	MB2DONE	R/W	0h	Mailbox 2 Token Done Interrupt Polarity 0h = Low level/falling edge 1h = High level/rising edge
2	MB2FREE	R/W	0h	Mailbox 2 Free Interrupt Polarity 0h = Low level/falling edge 1h = High level/rising edge
1	MB1DONE	R/W	0h	Mailbox 1 Token done Interrupt Polarity 0h = Low level/falling edge 1h = High level/rising edge
0	MB1FREE	R/W	0h	Mailbox 1 Free Interrupt Polarity 0h = Low level/falling edge 1h = High level/rising edge

8.9.6 AICTYPE Register (Offset = 3E04h) [Reset = 00000000h]

AICTYPE is shown in Table 8-14.

Return to the Summary Table.

AIC Type Control Register

Table 8-14. AICTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Type 0h = Level 1h = Edge
3	MB2DONE	R/W	0h	Mailbox 2 Token Done Interrupt Type 0h = Level 1h = Edge
2	MB2FREE	R/W	0h	Mailbox 2 Free Interrupt Type 0h = Level 1h = Edge
1	MB1DONE	R/W	0h	Mailbox 1 Token Done Interrupt Type 0h = Level 1h = Edge
0	MB1FREE	R/W	0h	Mailbox 1 Free Interrupt Type 0h = Level 1h = Edge

8.9.7 AICEN Register (Offset = 3E08h) [Reset = 00000000h]

AICEN is shown in Table 8-15.

Return to the Summary Table.

AIC Enable Control Register

Table 8-15. AICEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Enable. Indicates one or more mailbox can be linked 0h = Disable 1h = Enable
3	MB2DONE	R/W	0h	Mailbox 2 Token Done Interrupt Enable 0h = Disable 1h = Enable
2	MB2FREE	R/W	0h	Mailbox 2 Free Interrupt Enable 0h = Disable 1h = Enable
1	MB1DONE	R/W	0h	Mailbox 1 Token done Interrupt Enable 0h = Disable 1h = Enable
0	MB1FREE	R/W	0h	Mailbox 1 Free Interrupt Enable 0h = Disable 1h = Enable

8.9.8 AICRSTA Register (Offset = 3E0Ch) [Reset = 00000000h]

AICRSTA is shown in Table 8-16.

Return to the Summary Table.

AIC Raw Source Status Register

Table 8-16. AICRSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R	1h	Mailbox Linkable Interrupt Status. Indicates one or more mailbox can be linked
3	MB2DONE	R	1h	Mailbox 2 Token Done Interrupt Status
2	MB2FREE	R	1h	Mailbox 2 Free Interrupt Status
1	MB1DONE	R	1h	Mailbox 1 Token done Interrupt Status
0	MB1FREE	R	1h	Mailbox 1 Free Interrupt Status

8.9.9 AICENSET Register (Offset = 3E0Ch) [Reset = 00000000h]

AICENSET is shown in Table 8-17.

Return to the Summary Table.

AIC Enable Set Registers

Table 8-17. AICENSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Enable Set 1h = Set Enable
3	MB2DONE	R/W	0h	MailBox 2 Token Done Interrupt Enable Set 1h = Set Enable
2	MB2FREE	R/W	0h	MailBox 2 Free Interrupt Enable Set 1h = Set Enable
1	MB1DONE	R/W	0h	MailBox 1 Token Done Interrupt Enable Set 1h = Set Enable
0	MB1FREE	R/W	0h	MailBox 1 Free Interrupt Enable Set 1h = Set Enable

8.9.10 AICENSTA Register (Offset = 3E10h) [Reset = 00000000h]

AICENSTA is shown in Table 8-18.

Return to the Summary Table.

AIC Enabled Status Register

Table 8-18. AICENSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Enable Status
3	MB2DONE	R/W	0h	Mailbox 2 Done Interrupt Enable Status
2	MB2FREE	R/W	0h	MailBox 2 Free Interrupt Enable Status
1	MB1DONE	R/W	0h	MailBox 1 Token Done Interrupt Enable Status
0	MB1FREE	R/W	0h	Mailbox 1 Free Interrupt Enable Status

8.9.11 AICACK Register (Offset = 3E10h) [Reset = 00000000h]

AICACK is shown in Table 8-19.

Return to the Summary Table.

AIC Acknowledge Register

Table 8-19. AICACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Acknowledge 1h = Interrupt Ack
3	MB2DONE	R/W	0h	Mailbox 2 Done Interrupt Acknowledge 1h = Interrupt Ack
2	MB2FREE	R/W	0h	MailBox 2 Free Interrupt Acknowledge 1h = Interrupt Ack
1	MB1DONE	R/W	0h	MailBox 1 Token Done Interrupt Acknowledge 1h = Interrupt Ack
0	MB1FREE	R/W	0h	Mailbox 1 Free Interrupt Acknowledge 1h = Interrupt Ack

8.9.12 AICENCLR Register (Offset = 3E14h) [Reset = 00000000h]

AICENCLR is shown in Table 8-20.

Return to the Summary Table.

AIC Enable Clear Register

Table 8-20. AICENCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	MBLNKABL	R/W	0h	Mailbox Linkable Interrupt Enable Clear 1h = Clear Enable
3	MB2DONE	R/W	0h	Mailbox 2 Done Interrupt Enable Clear 1h = Clear Enable
2	MB2FREE	R/W	0h	MailBox 2 Free Interrupt Enable Clear 1h = Clear Enable
1	MB1DONE	R/W	0h	MailBox 1 Token Done Interrupt Enable Clear 1h = Clear Enable
0	MB1FREE	R/W	0h	Mailbox 1 Free Interrupt Enable Clear 1h = Clear Enable

8.9.13 AICOPT Register (Offset = 3E18h) [Reset = 00000000h]

AICOPT is shown in Table 8-21.

Return to the Summary Table.

AIC Options Register

Table 8-21. AICOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MINRMAP	R	0h	Mini register map.
7	EXTRMAP	R	0h	Extended register map.
6	RESERVED	R	0h	Reserved
5-0	INPUTS	R	5h	The number of interrupt request inputs.

8.9.14 AICVER Register (Offset = 3E1Ch) [Reset = 00000000h]

AICVER is shown in Table 8-22.

Return to the Summary Table.

AIC Version Register

Table 8-22. AICVER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	MAJORVER	R	1h	These bits encode the major version number for the AIC module.
23-20	MINORVER	R	4h	These bits encode the minor version number for the AIC module.
19-16	PATCHLVL	R	0h	These bits encode the hardware patch level for the AIC module, starting at value 0 on the first release.
15-8	NUMCMPL	R	36h	These bits simply contain the complement of bits [7:0], used by a driver to ascertain that this version register is indeed read.
7-0	NUM	R	C9h	These bits encode the AIC number.

8.9.15 MBSTA Register (Offset = 3F00h) [Reset = 00000000h]

MBSTA is shown in Table 8-23.

Return to the Summary Table.

Mailbox Status Register

Table 8-23. MBSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	MB2AVAIL	R	0h	Input Mailbox 2 available status 0h = Input Mailbox is linked to a Host or is filled 1h = Input Mailbox is available for linking by this Host
6	MB2LNKD	R	0h	Mailbox 2 Link Status 0h = This Host is not linked to Mailbox 1h = This Host is linked to Mailbox
5	MB2OUT	R	0h	Output Mailbox 2 Status 0h = Mailbox is Empty 1h = Mailbox is Full
4	MB2IN	R	0h	Input Mailbox 2 Status 0h = Mailbox is Empty 1h = Mailbox is Full
3	MB1AVAIL	R	0h	Input Mailbox 1 available status 0h = Input Mailbox is linked to a Host or is filled 1h = Input Mailbox is available for linking by this Host
2	MB1LNKD	R	0h	Mailbox 1 Link Status 0h = This Host is not linked to Mailbox 1h = This Host is linked to Mailbox
1	MB1OUT	R	0h	Output Mailbox 1 Status 0h = Mailbox is Empty 1h = Mailbox is Full
0	MB1IN	R	0h	Input Mailbox 1 Status 0h = Mailbox is Empty 1h = Mailbox is Full

8.9.16 MBCTL Register (Offset = 3F00h) [Reset = 00000000h]

MBCTL is shown in Table 8-24.

Return to the Summary Table.

Mailbox Control Register

Table 8-24. MBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	MB2ULNK	W	0h	Unlink the Mailbox from this host 1h = unlink Mailbox 2
6	MB2LNK	W	0h	Link Mailbox to this Host. Host can link to a mailbox only if it is not filled and not linked to another host 1h = Link Mailbox 2
5	MB2OUT	W	0h	The Host for whom the token is in Output Mailbox 1 can clear the status 1h = Set output mailbox empty
4	MB2IN	W	0h	The Host linked to input mailbox 2 can set after placing a token into Input Mailbox 2 1h = Set Input Mailbox full
3	MB1UNLNK	W	0h	Unlink the Mailbox from this host 1h = Unlink Mailbox 1
2	MB1LNK	W	0h	Link Mailbox to this Host. Host can link to a mailbox only if it is not filled and not linked to another host 1h = Link Mailbox 1
1	MB1OUT	W	0h	The Host for whom the token is in Output Mailbox 1 can clear the status 1h = Set output mailbox empty
0	MB1IN	W	0h	The Host linked to input mailbox 1 can set after placing a token into Input Mailbox 1 1h = Set Input Mailbox full

8.9.17 MBRSTA Register (Offset = 3F04h) [Reset = 00000000h]

MBRSTA is shown in Table 8-25.

Return to the Summary Table.

Raw Mailbox Status Register

Table 8-25. MBRSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	MB2LNKD	R	0h	Mailbox 2 Linked Raw Status 0h = This Host is not linked to Mailbox 1h = This Host is linked to Mailbox
5	MB2OUT	R	0h	Output Mailbox 2 Raw Status 0h = Mailbox is Empty 1h = Mailbox is Full
4	MB2IN	R	0h	Input Mailbox 2 Raw Status 0h = Mailbox is Empty 1h = Mailbox is Full
3	RESERVED	R	0h	Reserved
2	MB1LNKD	R	0h	Mailbox 1 Linked Raw Status 0h = This Host is not linked to Mailbox 1h = This Host is linked to Mailbox
1	MB1OUT	R	0h	Output Mailbox 1 Raw Status 0h = Mailbox is Empty 1h = Mailbox is Full
0	MB1IN	R	0h	Input Mailbox 1 Raw Status 0h = Mailbox is Empty 1h = Mailbox is Full

8.9.18 MBRST Register (Offset = 3F04h) [Reset = 00000000h]

MBRST is shown in Table 8-26.

Return to the Summary Table.

Mailbox Reset Register. Only Master Host can write into this register

Table 8-26. MBRST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	MB2ULNK	W	0h	Set only - Master Host can unlink mbx from current Host by writing 1b here. 1h = Unlink Mailbox
6	RESERVED	R	0h	Reserved
5	MB2OUT	W	0h	Set only - Master Host can clear mbx_out_full bit in MBSTA by writing 1b here. 1h = Set Mailbox Empty
4	RESERVED	R	0h	Reserved
3	MB1UNLNK	W	0h	Set only - Master Host can unlink mbx from current Host by writing 1b here. 1h = Unlink Mailbox
2	RESERVED	R	0h	Reserved
1	MB1OUT	W	0h	Set only - Master Host can clear mbx_out_full bit in MBSTA by writing 1b here. 1h = Set Mailbox Empty
0	RESERVED	R	0h	Reserved

8.9.19 MBLNKID Register (Offset = 3F08h) [Reset = 00000000h]

MBLNKID is shown in Table 8-27.

Return to the Summary Table.

Mailbox Status - linked Host IDs Register

Table 8-27. MBLNKID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	MB2PACC	R	0h	0: Mailbox 2 can be accessed by the Host using protected or non-protected access. 1: Mailbox 2 is only accessible if the Host uses protected access.
6-4	MB2LNKID	R	0h	Host cpu_id of the Host linked to the Mailbox 2
3	MB1PACC	R	0h	0: Mailbox 1 can be accessed by the Host using protected or non-protected access. 1: Mailbox 1 is only accessible if the Host uses protected access.
2-0	MB1LNKID	R	0h	Host cpu_id of the Host linked to the Mailbox 1

8.9.20 MBOUTID Register (Offset = 3F0Ch) [Reset = 00000000h]

MBOUTID is shown in Table 8-28.

Return to the Summary Table.

Mailbox Status - output Host IDs Register

Table 8-28. MBOUTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	MB2PACC	R	0h	0: Output mailbox 2 can be accessed by the Host using protected or non-protected access. 1: Output mailbox 2 is only accessible if the Host uses protected access.
6-4	MB2ID	R	0h	Host cpu_id of the Host allowed to read a result from the Mailbox 2
3	MB1PACC	R	0h	0: Output mailbox 1 can be accessed by the Host using protected or non-protected access. 1: Output mailbox 1 is only accessible if the Host uses protected access.
2-0	MB1ID	R	0h	HostID of the Host allowed to read a result from the Mailbox 1

8.9.21 MBLCKOUT Register (Offset = 3F10h) [Reset = 00000000h]

MBLCKOUT is shown in Table 8-29.

Return to the Summary Table.

Host or Mailbox lockout control Register

Table 8-29. MBLCKOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	MB2LKOUT	R/W	2h	Bit map indicates which Hosts are blocked from accessing mailbox 2
7-0	MB1LKOUT	R/W	2h	Bit map indicates which Hosts are blocked from accessing mailbox 1

8.9.22 MODSTA Register (Offset = 3FE0h) [Reset = 00000000h]

MODSTA is shown in Table 8-30.

Return to the Summary Table.

Module Status Register

Table 8-30. MODSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FATAL	R	0h	Set if fatal error occured
30-24	RESERVED	R	0h	Reserved
23	FWACPTD	R	0h	Set if firmware is to be executed
22	FWCKDONE	R	0h	Set if firmware checks complete
21-11	RESERVED	R	0h	Reserved
10	CRC24ERR	R	0h	Set if CRC on ProgramROM is fails
9	CRC24OK	R	0h	Set if CRC on ProgramROM is passes
8	CRC24BSY	R	1h	Set if CRC on ProgramROM is busy
7-0	RESERVED	R	0h	Reserved

8.9.23 OPTIONS2 Register (Offset = 3FF4h) [Reset = 00000000h]

OPTIONS2 is shown in Table 8-31.

Return to the Summary Table.

Configured options(2)

Table 8-31. OPTIONS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	ADDCE10	R	0h	An additional crypto engine is available in hardware as custom engine10
24	ADDCE9	R	0h	An additional crypto engine is available in hardware as custom engine9
23	ADDCE8	R	0h	An additional crypto engine is available in hardware as custom engine8
22	ADDCE7	R	0h	An additional crypto engine is available in hardware as custom engine7
21	ADDCE6	R	1h	An additional crypto engine is available in hardware as custom engine6
20	ADDCE5	R	0h	An additional crypto engine is available in hardware as custom engine5
19	ADDCE4	R	0h	An additional crypto engine is available in hardware as custom engine4
18	ADDCE3	R	0h	An additional crypto engine is available in hardware as custom engine3
17	ADDCE2	R	0h	An additional crypto engine is available in hardware as custom engine2
16	ADDCE1	R	0h	An additional crypto engine is available in hardware as custom engine1
15-13	RESERVED	R	0h	Reserved
12	BUSIFC	R	0h	Bus interface type, 0b = 32-bit AHB, 1b = 32-bit AXI
11-10	RESERVED	R	0h	Reserved
9	PROGRAM	R	0h	Downloadable RAM based firmware program memory.
8	CCPU	R	0h	C capable local cpu available
7	RESERVED	R	0h	Reserved
6	CRNG	R	1h	CRNG engine available
5	PKCP	R	1h	PKCP Engine available
4	CRC	R	1h	CRC calculation available
3	TRNG	R	1h	TRNG engine available
2	SHA	R	1h	SHA1/SHA2 combination core available
1	RESERVED	R	0h	Reserved
0	DESAES	R	0h	DES/AES combination crypto core available

8.9.24 OPTIONS Register (Offset = 3FF8h) [Reset = 00000000h]

OPTIONS is shown in Table 8-32.

Return to the Summary Table.

Configured options(1)

Table 8-32. OPTIONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHOST	R	3h	Bits to indicate which of the 8 possible HOSTID codes on the bus interface are active Hosts with secure access
23	MYIDSEC	R	1h	Indicates the current protection bit values of the Host actually reading the register
22-20	MYID	R	1h	Host ID code for the Host that is reading this register
19	RESERVED	R	0h	Reserved
18-16	MASTERID	R	0h	Value of the HOSTID that designates the Master Host
15-8	HOSTID	R	3h	Bits to indicate which of the 8 possible HOSTID codes on the bus interface are active
7-6	RESERVED	R	0h	Reserved
5-4	MBSIZE	R	1h	Mailbox pair Size 0h = 128 Bytes 1h = 256 Bytes 2h = 512 Bytes 3h = 1024 Bytes
3-0	NMB	R	2h	Number of Input/Output Mailbox pairs

8.9.25 VERSION Register (Offset = 3FFCh) [Reset = 00000000h]

VERSION is shown in Table 8-33.

Return to the Summary Table.

Version register

Table 8-33. VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	MAJOR	R	4h	Major Version release number for this module
23-20	MINOR	R	3h	Minor Version release number for this module
19-16	PATCHLVL	R	1h	Hardware Patch Level for this module
15-8	NUMCMPL	R	7Dh	Bit by Bit compliment of IP Number
7-0	NUM	R	82h	IP number

Chapter 9

Device Boot and Bootloader

This section describes the device boot flow coming out of reset state and device bootloader options supported in system ROM.

9.1 Device Boot and Programming

Device boot is the process that happens after a device reset and before the first instruction of a user application is executed. This process runs out of code in ROM memory and performs the following tasks:

- Required hardware trim values are copied to hardware registers
- SRAM repair information is applied
- Various permissions and restrictions are applied as defined by FCFG (factory configuration), SCFG (security configuration), and CCFG (customer configuration)
- SACI, a device management command interface that uses the Serial wire debug (SWD) secure access point (SECAP) mailbox for communication can be entered. It can be used for:
  - Obtaining device information
  - Device lifecycle management
  - Flash programming / validation
  - Debug authentication
  - Entry into various test modes
- A bootloader can be invoked before application entry via the TI-provided ROM serial bootloader (ROM SBL) intended to allow programming of blank devices through SPI or UART

Note

The ROM serial bootloader can be used for updating on-chip flash via the SPI or UART interface after production. However, the ROM serial bootloader doesn't support security functions and a separate secure boot or secure FW update software should be used for validating the new FW images updated by the ROM serial bootloader.

There are multiple ways to reset the device and the PMCTL.RSTSTA register reports which type of reset has occurred to boot code (and later to bootloader and application) see Table 9-1.

Table 9-1. Reset Causes

RSTSTA[7:4] SYSSRC	RSTSTA[3] TSDEV	RSTSTA[2:0] RESETSRC	Reset Type	Description	Memory/state retention
x	0	0	Power-on reset	Power on reset circuit has released due to supply voltage VDDS above threshold. Seen when power first applied	None
x	0	1	Pin reset	External reset pin (active low) has been released	Retained SRAM unreliable REG3V3 registers retained
x	1	1	Thermal shutdown	Thermal shutdown reset has released due to temperature being below threshold	None
x	0	2	VDDS brownout	VDDS brownout detector has reset device	None
x	0	4	VDDR brownout	VDDR brownout detector has reset device	Retained SRAM unreliable REG3V3 register retained
0	0	6	LF clock loss	LF clock stopped running while in standby power state.	REG3V3 register retained
1	0	6	CPU-requested reset	System reset requested through ARM core's AIRCR.SYSRESETREQ flag	REG3V3 register retained
2	0	6	CPU Lockup	ARM core went into lockup state which triggered system reset	REG3V3 register retained
3	0	6	Watchdog timeout	Watchdog timer timeout occurred and triggered system reset	REG3V3 register retained
4	0	6	System reset request	System reset requested through PMCTL.RSTCTL.SYSRST flag	REG3V3 register retained

Table 9-1. Reset Causes (continued)

RSTSTA[7:4] SYSSRC	RSTSTA[3] TSDEV	RSTSTA[2:0] RESETSRC	Reset Type	Description	Memory/state retention
5	0	6	Serial Wire Debug reset request	System reset requested by external debug probe by writing value 0x5C to SWD:SECAP.RSTCTL.RST	REG3V3 register retained
14	0	6	Analog error	TI internal use: should not occur on production devices	None
15	0	6	Digital error	TI internal use: should not occur on production devices	None

9.1.1 Boot Flow

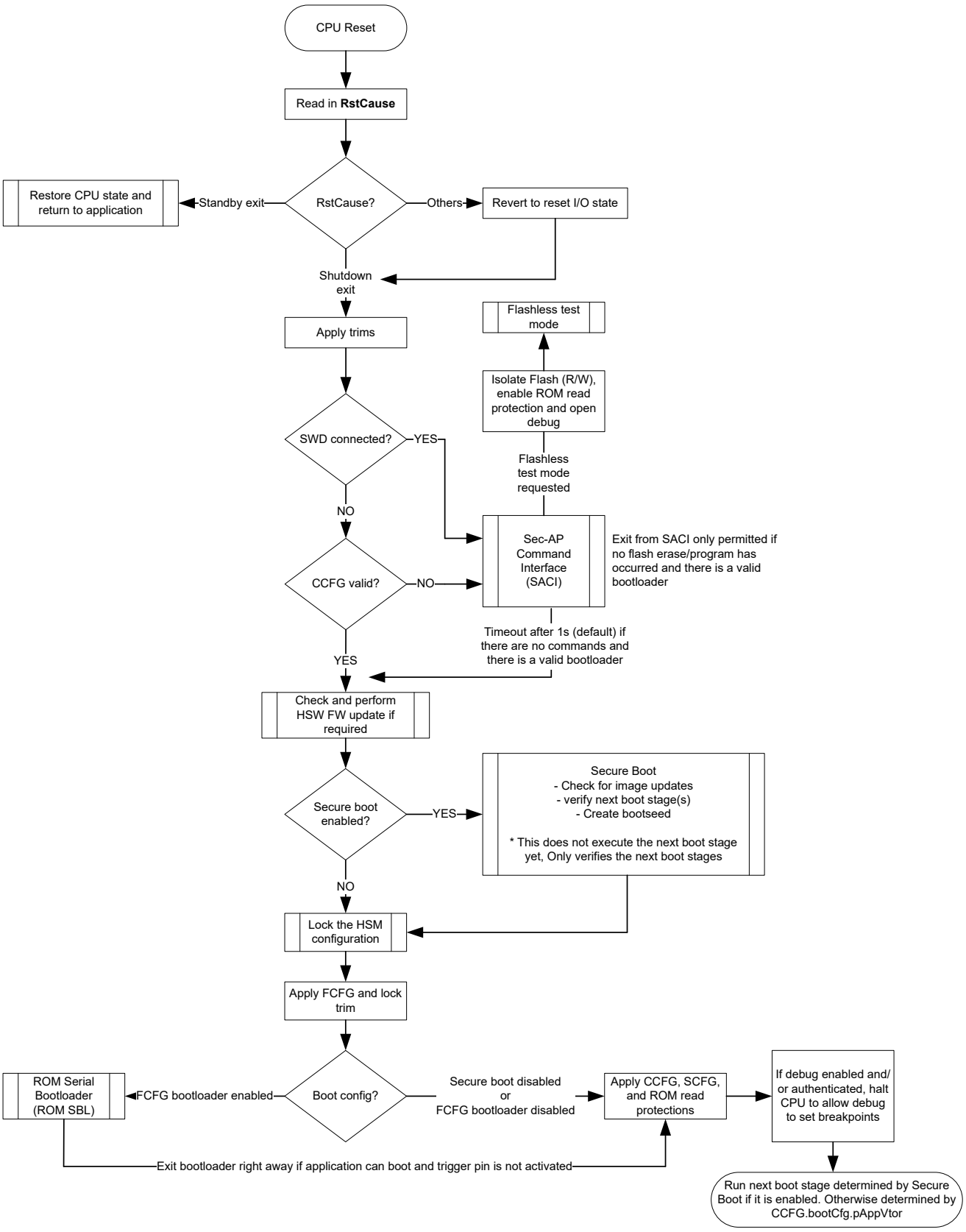

Figure 9-1. Boot Flow

9.1.2 Boot Status

An 8-bit value BOOTSTA is updated in the PMCTL.BOOTSTA register during boot to inform about which stage of boot is ongoing or to report errors. A bootloader can use the same mechanism, and this is even available for user application. BOOTSTA can be read from PMCTL.BOOTSTA using CPU or an external debug probe can read BOOTSTA through SWD:CFGAP.DEVICESTATUS.BOOTSTA.

The BOOTSTA[7:6] bits are sticky, meaning the bits cannot be cleared once set:

BOOTSTA[7:6]	Description
0b00	In boot flow, prior to bootloader invocation. BOOTSTA[5:0] indicates phase of boot or failures (highest numerical values)
0b01	In bootloader. BOOTSTA[5:0] indicates phase of bootloader or failures (highest numerical values)
0b11	Post bootloader boot flow or in application. Some of the lower values of BOOTSTA[5:0] and highest values of BOOTSTA[5:0] are reserved for reporting boot flow phase or failures. The remaining values can be used by an application to report its state in a similar way, and are accessible from SWD:CFGAP even if debugging is not allowed.

The BOOTSTA values used by boot flow and the ROM serial bootloader are given in Table 9-2.

Table 9-2. BOOTSTA Values

BOOTSTA	Set by	Name (waiting for external action) (failure reported; reset device)	Description
0x00	Hardware	BOOT_RESET	Initial value after system reset
0x01	Boot flow	BOOT_COLD_BOOT	Determined that this is not a standby exit scenario and normal boot process starts
0x02	Boot flow	BOOT_SRAM_REP_DONE	SRAM repair has completed; continuing with remaining critical trimming
0x03	Boot flow	BOOT_GENERAL_TRIMS	Critical trimming (flash, oscillators, references, power management) completed, starting general trimming
0x04-0x01F	-	*Reserved*	
0x20	Boot flow	BOOT_ENTERED_SACI	SACI entered (SWD secure access point command interface). If SACI timeout is configured the timer has started running
0x21-0x35	-	*Reserved*	
0x36	Boot flow	BOOT_WAIT_SWD_DISCONNECT	SACI reset command issued with option waitForSwdDisconnect set has been issued. In busy loop until SWD disconnect sequence received by Icemelter
0x37	Boot flow	BOOT_EXITED_SACI	Exit from SACI (due to timeout or SACI exit command)
0x38	Boot flow	BOOT_WAITLOOP_DBGPROBE	TI Internal Test Mode
0x3E	Boot flow	BOOT_FAIL_SRAM_REPAIR	SRAM repair failed: device cannot boot. Remain in infinite loop until reset
0x3F	Boot flow	BOOT_FAULT_HANDLER	Uncaught/unspecified error during boot: device cannot boot. Remain in infinite loop until reset
0x40-0x7F	-	*Cannot be used*	
0x80	Boot flow	BLDR_MODE_ENTRY	Entering bootloader mode; checking which bootloader, if any, to invoke next
0x81	Boot flow	BLDR_WAITLOOP_DBGPROBE	Debug of bootloader allowed; busy loop to allow external probe to set breakpoints before single-stepping or running CPU
0x82-0xB9	-	*Reserved*	
0xBA	ROM serial bootloader	BLDR_STARTED	ROM serial bootloader entered

Table 9-2. BOOTSTA Values (continued)

BOOTSTA	Set by	Name (waiting for external action) (failure reported; reset device)	Description
0xBB	ROM serial bootloader	BLDR_CMD_IDLE	Serial boot ROM has triggered and then either UART or SPI interface was selected (through interface activity); currently bootloader is waiting for a command over selected interface.
0xBC	ROM serial bootloader	BLDR_CMD_PROCESSING	Serial boot ROM has triggered and then either UART or SPI interface was selected (through interface activity); currently bootloader is in the process of receiving or processing a command
0xBD	ROM serial bootloader	BLDR_FAIL_EXECUTION_CONTEXT	Failure: ROM serial bootloader entry function was invoked from the application rather than from the boot flow. Remain in infinite loop until reset
0xBE	ROM serial bootloader	BLDR_FAIL_APPTRANSFER	Failure (should never happen): no valid application for bootloader to transfer to. Remain in infinite loop until reset
0xBF	ROM serial bootloader	BLDR_FAULT_HANDLER	Uncaught/unspecified error during bootlloader execution. Remain in infinite loop until reset
0xC0	Boot flow	APP_MODE_ENTRY	Entering application mode. Exited bootloader if one was invoked. AHB-AP accessible from external debug probe if debug is open or has been authenticated
0xC1	Boot flow	APP_WAITLOOP_DBGPROBE	Debug of application allowed; busy loop to allow external probe to set breakpoints before single-stepping or running CPU
0xC2	Boot flow	BLDR_START_INIT	Boot complete: set immediately before jumping to application entry point
0xC3-0xFC	-	*Available for application usage*	*Suggest 0xC3 set at the very beginning of application startup code*
0xFD	Boot flow	APP_FAIL_NOAPP	Failure: (should never happen) bootloader exited and there is no valid application to boot into. Remain in infinite loop until reset
0xFE	Boot flow	APP_FAIL_APPTRANSFER	Failure: application returned. Should never happen as link register is set to 0xFFFF_FFFF before application entry function is called. A return from application will thus result in a fault (which may or may not be handled by the application)
0xFF	Boot flow	APP_FAULT_HANDLER	Uncaught/unspecified error during transition to application (typically incorrect vector table address provided in CCFG.bootCfg.pAppVtor or incorrect vector table contents).

9.1.3 Boot Protection/Locking Mechanisms

At various phases during boot, protection mechanisms are enabled and certain registers in the design are locked to improve FW security. The majority of ROM (including the implementation of security features) is also read-protected.

- Changes to hardware trims for oscillators, voltage/current references, flash trimming and power management output voltages
  - Wrong hardware trim values can result in the device operating out of spec and thus having unpredictable behavior.
- Flash sector write/erase protection
  - To avoid program errors, malicious attacks or a debug connection from changing contents of certain flash sectors
- SWD port and debug access
  - The SWD port gives access to the CFG-AP and SEC-AP access points from boot to allow device IDs and information to be read out through CFG-AP and communication with SACI through SEC-AP

- The AHB-AP access point that us used by debug probe can be enabled before the bootloader is invoked or the application is invoked using CCFG configurations
- Debug access is enabled by default and if specified by CCFG.debugCfg or with CCFG authentication (password) configurations

9.1.4 Debug and Active SWD Connections at Boot

The SWD debug port is activated whenever a long sequence of bits is clocked into the SWDIO pin by edges on the SWDCK pin. The sequence is detected in all device power states except for reset but including shutdown by a module called IceMelter and the SWD connection status remains until:

- An SWD disconnect sequence is detected
- Power is cycled

In boot, if SWD is connected, the device management interface SACI is always entered even if there is a valid bootloader or application to run. SACI has a configurable timeout for when to continue boot if there is no SWD activity, otherwise SACI waits until instructed by a SACI command over SWD before continuing boot. Communication with SACI is done through SWD using the SEC-AP mailbox.

To allow debugging across resets or shutdown scenarios, SACI commands exist for continuing boot and halting CPU right before application is entered. At this point hardware debug breakpoints must be resubmitted as these do not survive the reset. Debug (re)authentication SACI commands can also be required if dictated by CCFG.debugCfg.

See Chapter 5 or Section 9.3 for more details.

9.1.4.1 Secure Debug & Persistent Debug

Public key based authentication is being used here. When **ccfg.debugCfg.authorization == REQ_AUTH**, the user must continue configuring secure debug in the **scfg.debugAuthCfg** field. The authentication process uses a challenge response sequence where the device will provide a challenge for the debugging host to sign with the relevant private key. The private key can be looked up in a user's database with the **scfg.debugAuthCfg.*.keyId** field. The debugging host sends the signed challenge back to the device which will verify the signature based on the public key information it has in **scfg.debugAuthCfg.*.publicKeyHash**

- Secure debug is authenticated through SACI just as was previously done on some other TI devices. However the SACI commands are different.
- Levels of authentication:
  - Secure
    - Requires the configuration of the **scfg.debugAuthCfg.secureKey** field and for the relevant key to be used during authentication
  - Non-Secure
    - Requires the configuration of the **scfg.debugAuthCfg.nonSecureKey** field and for the relevant key to be used during authentication
  - Non-Invasive Only
    - Requires the configuration of the **scfg.debugAuthCfg.nonSecureKey** field and for the relevant key to be used during authentication
- Using the **scfg.debugAuthCfg.challengeVector** field the user can configure the challenge vector lifetime and deviceConst fields:
  - lifetime
    - Ephemeral - Each debug auth request to a given device will result in a securely random challenge vector. More secure and stops replay attacks
    - Endless - Each debug auth request to a given device will result in an identical challenge vector. This is a simplified process but it could potentially provide less security.
  - deviceConst

- Mac Const - Each debug auth request between a fleet of devices will have a unique challenge vector. More secure and stops replay attacks.
- Zeroed Const - Each debug auth request between a fleet of devices will result in an identical challenge vector. Less Secure. Potentially useful as a stepping stone or temp simplification as users ramp up with the feature.

Persistent Debug, as its name suggests, allows the device to remember a secure debug connection had previously been made and to automatically re-authorize that debug connection again for a simplified user experience. A secure debug connection if fully authenticated initially will persist until either a PoR or the DEBUG_CLOSE_SESSION SACI command is received.

- The user can be confident that, by either removing power from the device or explicitly sending the debug close session command, the secure debug connection has been closed and for a new secure debug connection to be opened the full challenge response sequence must be followed as described above.

9.1.5 Flashless Test Mode and Tools Client Mode

There are two special modes that can be entered where the flash is completely isolated from the rest of the design and no reads, writes or erasures can be performed. These modes are designed to not allow the contents of flash to be read out or modified in any way. These modes are forbidden if either of the SCFG or CCFG forbid the allowToolsClientMode permission. Both SCFG and CCFG must be configured to allow these modes.

9.1.5.1 Flashless Test Mode

Used by Texas Instruments for failure analysis on any parts returned by customers. This mode allows TI to run most production tests anew on the device and to analyze any reported symptoms/failures without gaining access to or modifying the contents of flash. After a reset the device boots into the programmed application again. A 256-bit password is required to gain access to this mode.

9.1.5.2 Tools Client Mode

Used by Texas Instruments tools such as SmartRF Studio and Packet Sniffer to allow in-situ RF testing on customer boards without disturbing the application stored in flash. This mode is similar to flashless test mode except that DFT mechanisms (scan test, RAM BIST, etc) remain unavailable and that FCFG.appTrims (radio trim values) are copied to the beginning of SRAM before the flash is isolated and then the SWD debugging is enabled allowing test programs to be loaded into and run from SRAM. Tools client mode can also be used by customers to do end-of-line testing without having to perform multiple flash program cycles. Tools client mode is not password protected.

9.1.6 Retest Mode and Return-to-Factory Procedure

To do full failure analysis (including flash), a return to factory procedure is supported. This procedure is only allowed if CCFG is blank or CCFG.permissions.allowReturnToFactory == ALLOWED. If a specific permission field is forbidden in either SCFG or CCFG, that particular permission will be forbidden. Both SCFG and CCFG must be configured to allow the feature. Before changing to the RETEST life cycle, all of these steps have to take place:

- All of SRAM is cleared.
- All MAIN flash sectors are unconditionally erased.
- CCFG is erased.
- FCFG.lifeCycle is updated to RETEST.
- A reset is required.

9.1.7 Disabling SWD Debug Port

If CCFG.permissions.allowDebugPort == FORBID then the SWD port is disabled altogether at a certain point in boot before invoking either bootloader or application. From this point onwards not even SWD:CFG-AP or SWD:SEC-AP access points are accessible. Even then, if the SWD connection sequence has been detected by IceMelter, the device enters SACI during boot and device management commands are available. Debugging is not possible when CCFG.permissions.allowDebugPort == FORBID.

9.2 Flash Programming

A flash image can be programmed into the device using one of two methods:

- SWD Device Management Command Interface (Section 9.3)
  - Interface is always accessible unless an image is already programmed where CCFG.permissions.allowDebugPort==FORBID
  - Communication is done over the 2-pin serial wire debug (SWD) port also used for debug
  - Pipelined flash sector transfer and programming implemented to allow highest possible programming speed
  - Used by IDEs to download image and TI's UniFlash tool. Available on TI's evaluation modules.
  - Used by supported 3rd party gang programmers
- ROM Serial Bootloader
  - A simple serial (UART or SPI) bootloader for flash programming that resides in ROM
  - ROM serial bootloader invoked by default on blank devices and customers can choose to invoke the serial bootloader with their applications too
  - Implements flash erase/programming commands similar to what SACI implements
  - Easily integrates into automated or semi-automated end-of-line testing

9.2.1 CCFG

The CCFG flash sector (described in Section 10.3) contains meta-information about/for the application:

- Boot configuration
  - Where the initial vector table of the application is so that the application entry function can be invoked and the application stack pointer set. Application can change vector table location later if needed.
  - Whether to invoke a bootloader and if so which bootloader and parameters to pass to the bootloader. Location of user bootloader.
  - If Secure Boot is enabled (described in Chapter 11) then the initial vector table of the application instead comes from the SCFG (described in Section 10.4)
- Permissions and hardware options
  - Whether various boot operations or non-debug SWD-related features are allowed
  - Ability to lock application out of certain hardware features or IPs (e.g. to minimize harm that programming errors can do)
- Flash write/erase protections that apply to application
- Hardware initialization to perform before first application instruction is run
- Debug permissions
- User record

The user record is a 128-byte record in CCFG that can be written at the same time as CCFG is written or with a separate **SACI** command later. This allows the user record to be written as part of a commissioning step separate from the application image that has been programmed. In this case the user record typically contains some kind of device unique ID, address or key.

9.2.2 CCFG Permissions/Restrictions that Affect Flash Programming

The CCFG.permissions record contains fields that controls which types of flash programming operations are allowed:

CCFG.permissions	Description
.allowChipErase	Determines whether the Chip Erase command is allowed. *Normally allowed, as otherwise the device cannot be reprogrammed through SACI or ROM serial bootloader*

CCFG.permissions	Description
.allowMainAppErase	Determines whether the Main App Erase command is allowed. This command will **not** erase the entire chip. Instead, it will only erase main flash sectors where the customer application resides. **Note** The HSM FW region of main flash will never be erased by this command.
.allowFlashProgram	Determines whether flash programming commands are allowed. Reset to allowed after a chip erase. *Normally not allowed to avoid changes to flash through flash programming interface after initial programming.*
.allowFlashVerify	Determines whether flash verify commands are allowed. These commands only check integrity against a provided CRC32 value, never return any flash contents. Flash verify commands are always allowed after a chip erase and until the first reset after the CCFG sector has been programmed *Normally allowed for checking integrity or identifying the flash image.*

On a blank device or a device otherwise without a valid CCFG, including after a chip erase command, these all default to *allowed*.

The CCFG.flashprot.writeEraseProt sub-record controls with finer granularity (down to sector or groups of 8 sector level) whether flash programming is allowed through SACI. The same mechanism controls whether the application is allowed to program these sectors. If flash programming operations are done on a blank device or a device otherwise without a valid CCFG, including after a chip erase command, these all default to *unrestricted*.

The CCFG.flashprot.chipEraseRetain sub-record controls with finer granularity (down to sector or groups of 8 sector level) whether a chip erase affects a sector or not. The mechanism is intended to allow flash sectors devoted to logging or runtime state/configuration to survive the chip erase during a FW update. This retention mechanism is not intended to be bullet-proof: a sequence of (chip erase → reset → chip erase) erases both CCFG and non-retained MAIN sectors the first time around and CCFG and all MAIN sectors the second time around.

9.2.3 SACI Flash Programming Commands

- User record commands
  - SACI_CMD_MISC_GET_CCFG_USER_REC
    - Allows the user record to be read out (only if CCFG is valid)
    - *Typically invoked prior to a chip erase command when the contents of user record need to be programmed back in after image update*
  - SACI_CMD_FLASH_PROG_CCFG_USER_REC
    - Program the user record with provided data (only if the user record is fully blank)
    - *Typically invoked either as part of some commissioning procedure long after the flash image was originally programmed, or as part of a flash image update to restore the previous user record content*
- Flash erasure commands
  - SACI_CMD_FLASH_ERASE_CHIP
    - First invalidates CCFG, then erases all (non-retained) MAIN sectors, then finally erases CCFG fully
    - CCFG considered as invalid from here on out
    - Boot may not continue after flash programming commands complete: device must be reset and rebooted
    - *Typically invoked at the beginning of a flash programming session*
  - SACI_CMD_FLASH_ERASE_MAIN_APP
    - Erases all (non-retained) MAIN sectors
    - HSM FW is always protected
    - Boot may not continue after flash programming commands complete: device must be reset and rebooted
    - *Typically invoked at the beginning of a flash programming session if erasing the entire chip is not desired*

- Flash programming commands
  - SACI_CMD_FLASH_PROG_SCFG_SECTOR
    - Programs the entire sector (optionally skipping un-provisioned key slots)
    - Only allowed if SCFG is already erased
    - Boot may not continue after flash programming commands complete: device must be reset and rebooted
    - *Typically invoked near the end of a flash image update just before programming the CCFG*
  - SACI_CMD_FLASH_PROG_CCFG_SECTOR
    - Programs the entire CCFG sector (optionally skipping past the user record)
    - Only allowed if CCFG is already entirely blank
    - Boot may not continue after flash programming commands complete: device must be reset and rebooted
    - *Typically invoked at end of flash image update so that device does not boot into incomplete image if there is a power failure*
  - SACI_CMD_FLASH_PROG_MAIN_SECTOR
    - Program an arbitrary amount of data at an arbitrary address within a MAIN sector, up to and including the whole sector
    - Considers CCFG.flashProt.writeEraseProt for this sector and allowFlashProgram
  - SACI_CMD_FLASH_PROG_MAIN_PIPELINED
    - Program any number of whole MAIN sectors starting at the beginning of a MAIN sector
    - Program data can be streamed continuously and sector programming happens in the background while data is being streamed
- Flash verification commands
  - **Note**

    All flash programming commands perform a full integrity check during programming as well, so verification is not strictly required.
  - SACI_CMD_FLASH_VERIFY_SCFG_SECTOR
    - Used for verifying the integrity of the SCFG sector
    - Integrity checks the SCFG against the embedded CRC32 checksum and reports whether it is valid or not
    - Only allowed if allowFlashVerify == ALLOW
    - Designed to prevent an outside attacker from gaining any information about the contents of the SCFG
  - SACI_CMD_FLASH_VERIFY_CCFG_SECTOR
    - Used for verification of CCFG sector, as one of:
      - Blank check: returns whether CCFG is fully unprogrammed or not
      - Integrity check: checks each part of CCFG against the embedded CRC32 checksums and reports whether all parts are valid or not. User record can be skipped
      - Identity check: computes checksum of each part of CCFG and compares against user provided CRC32 values to report whether all match or not. User record can be skipped
    - Only allowed if allowFlashVerify == ALLOW
    - Designed to prevent an outside attacker from gaining any information about the contents of CCFG
  - SACI_CMD_FLASH_VERIFY_MAIN_SECTORS
    - Used for verification of one or more whole MAIN sectors (optionally -4B to allow a CRC32 to be appended at end), as one of:
      - Blank check: return whether range is fully unprogrammed or not
      - Integrity/identity check: computes CRC32 over range and compares against user provided CRC32 value to report whether the value matches or not
    - Only allowed if allowFlashVerify == ALLOW
    - Designed to prevent an outside attacker from gaining any information about flash content

For full details see Section Section 9.3.

9.2.4 Flash Programming Flows

Some typical flash programming flows are given below:

9.2.4.1 Initial Programming of a New Device

Note

TI ships the devices with a blank CCFG sector but possibly with bit patterns from flash production test still in the main sectors.

- Perform SWD connect and reset device (through SWD reset or pin reset) to enter SACI
- Perform SACI_CMD_FLASH_ERASE_CHIP command
- Program in image using a sequence of SACI_CMD_FLASH_PROG_MAIN_SECTOR commands and/or one or more SACI_CMD_FLASH_PROG_MAIN_PIPELINED commands
- *Optionally* verify that image is correctly programmed using one or more SACI_CMD_FLASH_VERIFY_MAIN_SECTORS(crc32_calculated_or_extracted_from_image)
- Program in CCFG sector using SACI_CMD_FLASH_PROG_CCFG_SECTOR. If user record is in use either:
  - Program the user record now as part of SACI_CMD_FLASH_PROG_CCFG_SECTOR command
  - Program the user record in separate step using SACI_CMD_FLASH_PROG_CCFG_USER_REC command
  - Leave the user record unprogrammed for later commissioning step
- Program in SCFG sector using SACI_CMD_FLASH_PROG_SCFG_SECTOR
- Optionally verify CCFG sector using SACI_CMD_FLASH_VERIFY_CCFG_SECTOR and/or the SCFG sector using SACI_CMD_FLASH_VERIFY_SCFG_SECTOR
- Device can now be reset with SACI_CMD_BLDR_APP_RESET_DEVICE after which the device boots into application and/or any configured bootloader

9.2.4.2 Reprogramming of Previously Programmed Device

Note

Requires that CCFG.permissions.allowChipErase == ALLOWED

- Perform SWD connect and reset device (through SWD reset or pin reset) to enter SACI
- *If user record needs to be kept*, read out contents using SACI_CMD_MISC_GET_CCFG_USER_REC.
- Perform SACI_CMD_FLASH_ERASE_CHIP command
  - If there are main sectors (logging, runtime configuration, etc) that shouldn't be erased these should have been identified in CCFG.flashProt.chipEraseRetain and the option retainSelMainSectors passed to the SACI_CMD_FLASH_ERASE_CHIP command
- *If applicable*, write back user record using SACI_CMD_FLASH_PROG_CCFG_USER_REC
- Program in image using a sequence of SACI_CMD_FLASH_PROG_MAIN_SECTOR commands and/or one or more SACI_CMD_FLASH_PROG_MAIN_PIPELINED commands
- *Optionally* verify that image is correctly programmed using one or more SACI_CMD_FLASH_VERIFY_MAIN_SECTORS(crc32_calculated_or_extracted_from_image)
- Program in CCFG sector using SACI_CMD_FLASH_PROG_CCFG_SECTOR(skipUserRec).
- *Optionally* verify CCFG sector using SACI_CMD_FLASH_VERIFY_CCFG_SECTOR(identity check). If user record has CRC32 at end the user record integrity can be checked too
- Device can now be reset/rebooted with SACI_CMD_BLDR_APP_RESET_DEVICE after which the device boots into application and/or any configured bootloader

9.2.4.3 Add User Record on Already Programmed Device as Part of Commissioning Step

- Perform SWD connect and reset device (through SWD reset or pin reset) to enter SACI
- Write user record using SACI_CMD_FLASH_PROG_CCFG_USER_REC. Command fails if user record was not already blank
- *Optionally and if user record has a CRC32 at the end* the user record integrity can now be checked with SACI_CMD_FLASH_VERIFY_CCFG_SECTOR and SACI_CMD_FLASH_VERIFY_SCFG_SECTOR.

- Device can now be reset/rebooted with SACI_CMD_BLDR_APP_RESET_DEVICE after which the device boots into application and/or any configured bootloader

9.2.4.4 Incrementally Program Ancillary Data to MAIN Flash Sectors of a Previously Programmed Device

Note

Requires that CCFG.permissions.allowFlashProgram == ALLOWED and that sectors in question are not write/erase protected by CCFG.flashProt.writeEraseProt

- Perform SWD connect and reset device (through SWD reset or pin reset) to enter SACI
- Program in ancillary data using one or more SACI_CMD_FLASH_PROG_MAIN_SECTOR or SACI_CMD_FLASH_PROG_MAIN_PIPELINED commands
- *Optionally* verify ancillary data that covers whole sectors through SACI_CMD_FLASH_VERIFY_MAIN_SECTORS(crc32_calculated_over_ancillary_data)
- Device can now be reset/rebooted with SACI_CMD_BLDR_APP_RESET_DEVICE after which the device boots into application and/or any configured bootloader

9.2.4.5 Reprogramming of Only the Main Flash Application of a Previously Programmed Device

Note

This requires that CCFG.permissions.allowFlashProgram == ALLOWED, CCFG.permissions.allowMainAppErase == ALLOWED and that sectors in question are not write/erase protected by CCFG.flashProt.writeEraseProt

- Perform SWD connect and reset device (through SWD reset or pin reset) to enter SACI
- Perform SACI_CMD_FLASH_ERASE_MAIN_APP command
  - If there are main sectors (logging, runtime configuration, etc) that shouldn't be erased these should have been identified in CCFG.flashProt.chipEraseRetain and the option retainSelMainSectors passed to the SACI_CMD_FLASH_ERASE_MAIN_APP command
- Program in image using a sequence of SACI_CMD_FLASH_PROG_MAIN_SECTOR commands and/or one or more SACI_CMD_FLASH_PROG_MAIN_PIPELINED commands
- Optionally verify that image is correctly programmed using one or more SACI_CMD_FLASH_VERIFY_MAIN_SECTORS(crc32_calculated_or_extracted_from_image)
- Device can now be reset/rebooted with SACI_CMD_BLDR_APP_RESET_DEVICE after which the device boots into application and/or any configured bootloader

9.3 Device Management Command Interface

SEC-AP Command Interface (SACI) is a controlled is a controlled privilege state the device enters during boot when:

- The device is in certain (manufacturing and failure analysis) lifecycle states
- There is no valid firmware image to boot into (unprogrammed device)
- An active SWD connection exists
- Invalid CCFG detected during boot

SACI implements a set of commands through a hardware mailbox mechanism in SEC-AP that allow an external debug probe or production programmer to:

- Get information about the device and/or firmware image currently on the device
- Manage device lifecycle state
- Erase device, program a new firmware image and verify image integrity
- Control in-circuit debugging
- Enter test modes

During boot in general and while in SACI, the AHB-AP is not open and thus a debug probe can not access any part of memory or control the CPU. SACI implements a controlled privilege environment and which commands

are available depends on CCFG validity/configuration and device lifecycle. When entering/exiting SACI all SRAM memory is cleared to eliminate the risk of any application state to leak out.

If the device has a valid firmware image or bootloader image to boot into, SACI times out if a first command is not received within a configurable timeout (see CCFG.misc.saciTimeoutOverride and CCFG.misc.saciTimeoutExp) and boots normally.

9.3.1 SACI Communication Protocol

A SWD connection must first have been established and the device either halted in SACI during boot or reset (pin reset or SEC_AP reset see Chapter 5). Communication from external host to device uses these SWD registers in SEC-AP:

- DEBUGSS:TXD (data)
- DEBUGSS:TXCTL (flags)
  - Bit 0 / TXD_FULL: Indicates that TXD can be read. Set by hardware when TXD is written, cleared by hardware when TXD is read
  - Bit 1 / CMD_START: Indicates that TXD contains the first word of a command

Communication from device to host uses these registers:

- DEBUGSS:RXD (data)
- DEBUGSS:RXCTL (flags)
  - Bit 0 / RXD_FULL: Set by hardware when RXD is written, cleared by hardware when RXD is read
  - Bit 1 / CMD_ABORTED: Indicates that the previous command was aborted, meaning a new command was started before:
    - All parameter words for the previous command were received, or
    - The last response word of the previous command could be written to RXD
  - Bit 2 / CMD_WORKING: Indicates that SACI is working on a command after receiving all parameters
  - Bit 3 / CMD_ERROR: Indicates any type of error (invalid SACI command ID, prohibited operation, invalid parameters)

9.3.1.1 Host Side Protocol

The external host must follow these steps to execute any SACI command:

- Wait until TXD_FULL = 0
- Set CMD_START
- Write first parameter word to TXD
- If there are more parameter words:
  - Wait until TXD_FULL = 0
  - Clear CMD_START
  - Write second parameter word to TXD
  - Wait until TXD_FULL = 0
  - For each additional word:
    - Write the parameter word to TXD
    - There is no need to check TXD_FULL
- Wait until TXD_FULL = 0
- For commands with returned response, if relevant:
  - Wait until RXD_FULL = 1
  - Read RXD
  - For each response data word:
    - Wait until RXD_FULL = 1
    - Read RXD

The host must implement a timeout while waiting for TXD_FULL = 0:

- If the timeout occurs, the host should assume that the target is in an unknown state and abort or restart the session.

- This timeout can be set relatively high (e.g. 1 second), since the timeout should not occur frequently and only one time per session.

9.3.1.2 Command Format

Bits 15:0 of the first SACI command parameter word have fixed formatting. Bits 31:16 of the first parameter word, and later parameter words, if any, are command specific.

Words	Bits	Field	Value	Description
0	7:0	cmdId	-	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	< command specific >	-	Command specific parameters, if any

9.3.1.3 Response Format

The first SACI command response word has fixed formatting.

Note the extended usage of the "first response word" for SACI_CMD_FLASH_PROG_MAIN_PIPELINED.

Words	Bits	Field	Value	Description
0	7:0	cmdId	-	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result
	31:24	dataWordCount	-	Size of additional response data, in number of 32-bit words

9.3.1.4 Response Result Field

The result field of the first response word can have the values in the table below:

- Value 0x80 or higher indicates some type an error that is also reflected by CMD_ERROR

Result	Value	Description
SUCCESS	0x00	Command executed successfully
INVALID_CMD_ID	0x80	Invalid command ID
INVALID_ADDRESS_PARAM	0x81	Invalid address parameter
INVALID_SIZE_PARAM	0x82	Invalid size parameter
INVALID_KEY_PARAM	0x83	Invalid key parameter
FLASH_FSM_ERROR	0x84	Flash hardware FSM error
PARAM_BUFFER_OVERFLOW	0x85	Parameter data buffer overflow (host must slow down or implement flow control)
NOT_ALLOWED	0x86	Command is not allowed due to restrictions (the command had no effect)
CRC32_MISMATCH	0x87	Calculated CRC32 does not match embedded/expected CRC32
INVALID_PWD_PARAM	0x88	Invalid password parameter
BLANK_CHECK_FAILED	0x89	Blank check detected one or more flash bits that were zero
INVALID_DBG_AUTH_LVL_PARAM	0x8A	Invalid auth level parameter
INVALID_DBG_AUTH_CONFIG	0x8B	Invalid auth configuration
CHALLENGE_RESP_VERIFY_FAIL	0x8C	Challenge Response verification failed
KEY_HASH_MISMATCH	0x8D	Calculated key hash does not match the provided expected key hash
HSM_BOOT_FAILED	0x8E	HSM failed to boot
HSM_FW_HDR_INVALID	0x8F	HSM FW update failed due to invalid header contents
HSM_FW_VER_INVALID	0x90	HSM FW update failed due to invalid version number (anti-rollback)
HSM_FW_CRYPTO_FAIL	0x91	HSM FW update failed during either signature verification or decryption
CMD_FAILED	0xFF	Command failed, non-specific error (should not be used)

9.3.1.5 Command Sequence Tag

The host can optionally increment the response sequence number in the first parameter word of each command sent to SACI. This can be used to identify the corresponding response.

The host should read and check the response for each command.

9.3.1.6 Host Side Timeout

The host must implement a response timeout in case:

- Parameter words are lost due to electrical noise
- Parameter words (e.g. a length related field) are incorrectly received due to electrical noise
- The device fails to complete the operation for some other reason (e.g. due to electrical noise on the reset pin)

Note

Some commands take more time to complete than others.

Note

Flash related commands take more and more time as flash wear increases.

9.3.2 SACI Commands

SACI Command	cmdId	Category	Parameters	Restrictions	Description
SACI_CMD_MISC_ NO_OPERATION	0x01	-	-	-	Performs no operation.
TI Internal Command	0x02	-	-	-	-
SACI_CMD_MISC_ GET_DIE_ID	0x03	Information	-	Tested device only	Get the 128-bit die ID which identifies uniquely the die on the wafer
SACI_CMD_MISC_ GET_CCFG_USER_REC	0x04	Information	-	CCFG valid	Get the user record in CCFG, up to 128 bytes (in increments of 16 bytes)
SACI_CMD_GET_SECBOOT_ HSMFWUPDATE_STATUS	0x23	Information	-	-	It may be useful when a host needs to determine why a device may not be booting into the application. The command is used to read the STATUS field from the PMCTL_O_AONSTA0[14:12].
SACI_CMD_HSM_GET_SYS_ INFO	0x22	Information	-		This command returns the HSM system information.
SACI_CMD_DEBUG_ REQ_PWD_ID	0x05	Debug/control	-	Tested device only	Request password ID for debug authentication
SACI_CMD_DEBUG_ SUBMIT_AUTH	0x06	Debug/control	wordCount, pwd	CCFG valid and debug allowed	The host uses this command to submit the debug authentication password. If correct, debugging is enabled after exiting SACI
SACI_CMD_DEBUG_ EXIT_SACI_HALT	0x07	Debug/control	-	Debugging allowed, valid user bootloader or application	Exit SACI for debug mode, and wait for the host to setup breakpoints or run/single-step CPU through AHB-AP at the first instruction of the bootloader/application
SACI_CMD_DEBUG_ EXIT_SACI_SHUTDOWN	0x08	Debug/control	-	Wakeup from shutdown power state due to SWD activity	Exit SACI, and re-enter shutdown power state

SACI Command	cmdId	Category	Parameters	Restrictions	Description
SACI_CMD_DEBUG_REQ_KEY_ID	0x08	Debug/control	-	CCFG must be valid. Ccfg.debugCfg.authorization = 0xA5, 0x5A or 0xC3.	Request key ID for debug authentication
SACI_CMD_DEBUG_REQ_CHALLENGE	0x1E	Debug/control	authLevel	CCFG must be valid. SCFG must be valid. Ccfg.debugCfg.authorization = 0xA5 or 0x5A.	This command will trigger the start of the "debug auth process".
SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP	0x1F	Debug/control	pubKeyByteCount, signatureByteCount, publicKey, signature	CCFG must be valid. SCFG must be valid. There must be an ongoing debug auth process by first submitting the SACI_CMD_DEBUG_REQ_CHALLENGE command. Ccfg.debugCfg.authorization = 0xA5 or 0x5A.	This command will trigger the end of the "debug auth process".
SACI_CMD_DEBUG_CLOSE_SESSION	0x20	Debug/control	-	-	Close the debug session.
SACI_CMD_FLASH_ERASE_CHIP	0x09	Flash programming	retainSelMainSectors, key	Chip erase allowed	Perform chip erase: erase CCFG and main sectors. Optionally a set of main sectors indicated by CCFG can be retained

SACI Command	cmdId	Category	Parameters	Restrictions	Description
SACI_CMD_FLASH_ERASE_MAIN_APP	0x1C	Flash programming	retainSelMainSectors, key	• Fcfg.misc.allowMainAppErase = 0xA (FCFG_PERMISSION_ALLOW) • If CCFG is valid: – Ccfg.misc.allowMainAppErase = 0xA (CCFG_PERMISSION_ALLOW) • If the "retain selected MAIN sectors" option is used: – CCFG must be valid – The value of these invalid sectors within Ccfg.flashProt.chipEraseRetain.mainSectors0_31, Ccfg.flashProt.chipEraseRetain.mainSectors32_255 and Ccfg.chipEraseRetain.mainSectors256_511, must be set to the register reset value of the corresponding sectors within the VIMS:WEPRA, VIMS:WEP	Erase only the MAIN flash application.

SACI Command	cmdId	Category	Parameters	Restrictions	Description
				RB0 and VIMS:WEP RB1 protection registers • – SACI_CMD_FLASH_ERASE_MAIN_APP or SACI_CMD_FLASH_ERASE_CHIP must not have executed previously in the current SACI session with the "retain selected MAIN sectors" option	
SACI_CMD_FLASH_PROG_CCFG_SECTOR	0x0C	Flash Programming	skipUserRec, key, data	CCFG erased	Program the entire CCFG sector, with option to leave the user record part unprogrammed
SACI_CMD_FLASH_PROG_CCFG_USER_REC	0x0D	Flash programming	key, data	CCFG.userRecord unprogrammed	Program the user record part of the CCFG sector
SACI_CMD_FLASH_PROG_OTP_SECTOR	0x19	Flash programming	byteCount, key, data	All bytes in the OTP sector must be 0xFF before the OTP sector programming begins (a chip erase must have been performed since the previous OTP programming).	Program OTP Sector

SACI Command	cmdId	Category	Parameters	Restrictions	Description
SACI_CMD_FLASH_PROG_SCFG_SECTOR	0x1A	Flash programming	byteCount, key, data	Since SCFG is a 2T sector all bytes in the SCFG will be random after erasure. For this reason, the SCFG can only be programmed if the SCFG is invalid. SCFG is invalid if the boot code detects an issue in the CRC field or if the SCFG was specifically erased during the SACI Idle loop. The only way to do this is the SACI_CMD_FLASH_ERASE_CHIP cmd which will invalidate the SCFG.	Program the SCFG sector.
SACI_CMD_FLASH_PROG_MAIN_SECTOR	0x0E	Flash programming	key, firstByteAddr, data	Flash erased or CCFG allows flash programming	Program all or a part of one MAIN sector
SACI_CMD_FLASH_PROG_MAIN_PIPELINED	0x0F	Flash programming	key, firstSectorAddr	Flash erased or CCFG allows flash programming	Program multiple whole, back-to-back MAIN sectors of the flash (full programming speed)
SACI_CMD_FLASH_VERIFY_MAIN_SECTORS	0x10	Flash programming	doBlankCheck, firstSectorAddr, byteCount,expCrc32	Flash erased (blank check only) or CCFG allows flash verify	Verify the contents of one or more whole (with option to exclude the last 4 bytes) flash MAIN sectors against supplied CRC32 or check that the sectors are blank (all bytes are 0xFF)
SACI_CMD_FLASH_VERIFY_CCFG_SECTOR	0x11	Flash programming	checkExpCrcs, skipUserRec, doBlankCheck, expBootCfgCrc32, expCentralCrc32, expUserRecCrc32, expDebugCfgCrc32	Flash erased (blank check only) or CCFG allows flash verify	Verify the contents of records in CCFG sectors against supplied CRC32 values or check that CCFG sector is blank (all bytes are 0xFF)

SACI Command	cmdId	Category	Parameters	Restrictions	Description
SACI_CMD_FLASH_VERIFY_SCFG_SECTOR	0x1B	Flash programming	checkExpCrcs, expCrc32	• Fcfg.permissions.allowFlashVerify = 0xA (FCFG_PERMISSION_ALLOW) • If CCFG is valid: – Ccfg.permissions.allowFlashVerify = 0xA (CCFG_PERMISSION_ALLOW) • If SCFG is valid: – Scfg.permissions.allowFlashVerify = 0xA (SCFG_PERMISSION_ALLOW)	Verify Flash SCFG Sector
TI Internal Command	0x12				
TI Internal Command	0x13				
SACI_CMD_BLDR_APP_RESET_DEVICE	0x14	Debug/control	waitForSwdDisconnect	-	Reset the device and reboot (possibly into SACI again)
SACI_CMD_BLDR_APP_EXIT_SACI_RUN	ox15	Debug/control	-	Valid bootloader or application present, no flash programming commands in current SACI session	Exit SACI, and run bootloader or application
TI Internal Command	0x16				
SACI_CMD_MODE_REQ_TOOLS_CLIENT	0x17	Test Mode	-	Flash erased or CCFG allows tool client mode	Locks all accesses to flash, erase SRAM and then open up device for debug access. Used by TI development tools
TI Internal Command	0x18	-	-	-	-
SACI_CMD_HSM_FW_PROVISION	0x21	Test Mode	huiSize	-	This allows the HSM provision process to be triggered and completed with only one SACI command.

9.3.2.1 Miscellaneous Commands

9.3.2.1.1 SACI_CMD_MISC_NO_OPERATION

Performs no operation.

This command can be used to:

- Disable the inactivity timeout after reset
- Check SACI connection

Restrictions

None.

Table 9-3. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x01	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-4. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x01	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	See desc.	Command result (no special result codes for this command)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

9.3.2.1.2 SACI_CMD_MISC_GET_TEST_ID

Get the 128-bit test ID from FCFG, which identifies uniquely the device during production testing.

The test ID is fetched from Fcfg.faUnlock.testId.

Restrictions

None.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x02	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x02	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result (no special result codes for this command)
	31:24	dataWordCount	1	Size of additional response data, in number of 32-bit words
1	31:0	testId	Fcfg.faUnlock.testId	The test ID, as 32-bit word: • The first byte of the test ID is in bits 7:0 of word 1

9.3.2.1.3 SACI_CMD_MISC_GET_DIE_ID

Get the 128-bit die ID from FCFG, which identifies uniquely the die on the wafer.

The die ID is fetched from Fcfg.deviceInfo.dieId.

Restrictions

None.

Table 9-5. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x03	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-6. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x03	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result (no special result codes for this command)
	31:24	dataWordCount	4	Size of additional response data, in number of 32-bit words
4:1	31:0	dieId	Fcfg.deviceInfo.dieId	The die ID, as 4 x 32-bit words: • The first byte of the die ID is in bits 7:0 of word 1 • The last byte of the die ID is in bits 31:24 of word 4

9.3.2.1.4 SACI_CMD_MISC_GET_CCFG_USER_REC

Get the readable part of the user record in CCFG, up to 128 bytes (in increments of 16 bytes).

The "non-readable part" of Ccfg.userRecord is specified by Ccfg.flashProt.readProt.ccfgSector. The read protection starts at the end of the CCFG sector, and is specified in increments of 16 bytes.

The "non-readable part" can be read by a bootloader, before CCFG restrictions are applied, but not by the application.

Restrictions

CCFG must be valid (Ccfg.bootCfg.crc32 is valid).

Table 9-7. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x04	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-8. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x04	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result (no special result codes for this command)
	31:24	dataWordCount	0-32	Size of additional response data, in number of 32-bit words: • 32 words = 128 bytes • 0 = 0 bytes if restrictions are not met
1+	31:0	data	-	User record data.

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.1.5 SACI_CMD_GET_SECBOOT_HSMFWUPDATE_STATUS

It may be useful when a host needs to determine why a device may not be booting into the application. The command is used to read the STATUS field from the PMCTL_O_AONSTA0[14:12].

Availability

This command is not available in the P1STBDAY lifecycle state (result is INVALID_CMD_ID).

Restrictions

None.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x23	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x23	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	SCR_SUCCESS
	31:24	dataWordCount	1	Size of additional response data, in number of 32-bit words
1+	31:0	status	-	SB_STA_NA (value 0): Regular boot w/o a new image, No error. SB_STA_UPDATE_SUCCESS(value:1): Requested update was successful (any types) SB_STA_FIH_ERROR(value: 2): ROM panic mode due to a fault Injection SB_STA_IMG_REJECTED (value:3) : Invalid image detected (any types). SB_STA_IMG_VERIF_FAILED (value:4): The target image failed to verify (any types) SB_STA_UPDATE_FAILED(value:5): Requested image update process failed. SB_STA_INVALID_CONFIG(value6): SCFG configuration is invalid SB_STA_HSM_BOOT_FAILURE(value:7) : HSM FW failed to boot

9.3.2.1.6 SACI_CMD_HSM_GET_SYS_INFO

This command returns the HSM system information.

Restrictions

None.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x22	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x22	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	SCR_HSM_BOOT_FAILED: HSM failed to boot SCR_SUCCESS: HSM system info has been retrieved successfully
	31:24	dataWordCount	9	Size of additional response data, in number of 32-bit words
1	7:0		-	HSM FW Version Patch
	15:8			HSM FW Version Minor
	23:16			HSM FW Version Major
	31:24			HSM FW Rollback ID
2	7:0			HSM HW Version Patch
	15:8			HSM HW Version Minor
	23:16			HSM HW Version Major
	31:24			Reserved

3	15:0			Available Memory Size
	18:16			HOST ID of the Token Writer
	19			1: Host is in non Secure side 0: Host is in Secure side
	26:20			Reserved
	27			1: COID is set 0: COID is not set
	31:28			Mode 0000: ‘Functional Mode’ state, the Power-On Self-Tests have been executed successfully 1111: ‘Functional-Mode’ state, with successful Login done 0011: ‘Error’ state, Login failed 0100: ‘Error’ state, at least one of the self-tests has failed 0101: ‘Error’ state, DMA error detected 0110: ‘Error’ state, NRBG or DRBG stuck error detected 0111: ‘Error’ state, key generation failed
4	31:0			Identify of the caller
5	11:0			Reserved
	15:12			OTP Anomaly 0000: No anomaly 0001 : OTP area is empty 0010 : Unsupported size 0100 : FAT Error 1000: OTP are is zeroized
	31:16			SelftestActive The value of this field is only applicable when the system is in ‘Error’ state A non-zero value refers to the self-test that caused the transition to the 'Error' state.

6	7:0			HSM BOOT FW Version Patch
	15:8			HSM BOOT FW Version Minor
	23:16			HSM BOOT FW Version Major
	31:24			Reserved
7	7:0			Custom BOOT FW Version Patch
	15:8			Custom BOOT FW Version Minor
	23:16			Custom BOOT FW Version Major
	31:24			Reserved
8	7:0			Custom FW Version Patch
	15:8			Custom FW Version Minor
	23:16			Custom FW Version Major
	31:24			Reserved
9	7:0			Custom HW Version Patch
	15:8			Custom HW Version Minor
	23:16			Custom HW Version Major
	31:24			Reserved

9.3.2.2 Debug Commands

Debug authentication and SACI exit to debug mode functionality.

9.3.2.2.1 SACI_CMD_DEBUG_REQ_PWD_ID

Request password ID for debug authentication.

This command must be used to check whether debugging is allowed, and obtain the password ID for SACI_CMD_DEBUG_SUBMIT_AUTH, if required. As indicated, there are three possible states:

Ccfg.debugCfg.authorization	Description	Indicated by
0xA5	Debug authentication is required	Response contains a 64-bit debug password ID
0x5A	Debug authentication is not required	Response contains no password ID. Debugging is enabled after exiting SACI.
Any other value	Debugging is not allowed	Response result is NOT_ALLOWED

The password ID is fetched from Ccfg.debugCfg.pwdId.

Restrictions

CCFG must be valid (Ccfg.bootCfg.crc32 is valid)..

Ccfg.debugCfg.authorization = 0xA5 or 0x5A.

Table 9-9. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x05	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-10. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x05	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0 or 2	Size of additional response data, in number of 32-bit words: • 2 if debug authentication is required • 0 if debug authentication is not required, or debugging is not allowed
2:1	31:0	pwdId	Ccfg.debugCfg.pwdId	The 64-bit debug password ID: • The first byte of the password ID is in bits 7:0 of word 1 • The last byte of the password ID is in bits 31:24 of word 2

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.2.2 SACI_CMD_DEBUG_SUBMIT_AUTH

If the SACI_CMD_DEBUG_REQ_PWD_ID command returns a 64-bit password ID, the host must use this command to submit the password that corresponds to this ID. The host must know the password length.

If the submitted password is correct, debugging is enabled after exiting SACI.

The password check calculates SHA-256 of the submitted password, and compares the resulting 256b hash with Ccfg.debugCfg.pwdHash. The password check takes constant time.

The password is only checked if debug authentication is required (see SACI_CMD_DEBUG_REQ_PWD_ID). If not required, the result is always SUCCESS.

Restrictions

CCFG must be valid (Ccfg.bootCfg.crc32 is valid)..

Ccfg.debugCfg.authorization = 0xA5 or 0x5A.

Table 9-11. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x06	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	wordCount	3 - 16	Size of the password, in number of 32-bit words (min = 3, max = 16)
N:1	31:0	pwd	Device specific	The password, N = wordCount

Table 9-12. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x06	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • NOT_ALLOWED if restrictions are not met • INVALID_SIZE_PARAM if the wordCount parameter is invalid – For wordCount > 16, the response will come after reception of the 16th word • INVALID_PWD_PARAM if the pwd parameter is required and invalid
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.2.3 SACI_CMD_DEBUG_EXIT_SACI_HALT

Exit SACI for debug mode, and wait for the host to setup a breakpoint at the first instruction of the bootloader/application.

Before this command, the host must use SACI_CMD_DEBUG_REQ_PWD_ID, and if needed SACI_CMD_DEBUG_SUBMIT_AUTH, to enable access to AHB-AP. Otherwise the debug session fails.

Host Follow-Up Actions

After executing this command, the host must:

- Wait until CFGAP.DEVICESTATUS.BOOTSTA equals one of these values:
  - 0x81 (BLDR_WAITLOOP_DBGPROBE) = The boot code is waiting before bootloader entry (CCFG restrictions not yet applied)
  - 0xC1 (APP_WAITLOOP_DBGPROBE) = The boot code is waiting before application entry
- Halt the CPU
- Optional: Configure breakpoint at start of main() or at the start of the application reset vector
- If debugging an application that runs in flash:
  - Write CPU register R3 = 0x00000000
  - Run the CPU
- Otherwise, if debugging an application that runs in SRAM:
  - Write the application image to SRAM
  - Load CPU register SP
  - Load CPU register PC
  - Run the CPU
- Wait until the CPU has reached the breakpoint, if any

Restrictions

SACI_CMD_FLASH_ERASE_CHIP and/or SACI_CMD_FLASH_PROG_CCFG_SECTOR must not have been used during the current SACI session.

Bootloader must be specified in CCFG or FCFG, or there must be a valid application.

Debugging must be allowed (see SACI_CMD_DEBUG_REQ_PWD_ID for details).

Table 9-13. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x07	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-14. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x07	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.2.4 SACI_CMD_DEBUG_EXIT_SACI_SHUTDOWN

Exit SACI, and enter shutdown mode.

Restrictions

The device must have woken up from shutdown due to SWCLK activity.

Table 9-15. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x08	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-16. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x07	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. (1) • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

(1) Normally none: the device immediately returns to shutdown when the command is processed if restrictions are met. A response is only generated if the command fails to meet the restrictions.

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.2.5 SACI_CMD_DEBUG_REQ_KEY_ID

Request key ID for debug authentication

This command must be used to check whether debugging is allowed, and obtain the key ID for SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP, if required. As indicated, there are three possible states:

Ccfg.debugCfg.authorization	Description	Indicated by
0xA5	Debug authentication is required	Response contains a 64-bit debug key ID based on the requested auth level.
0x5A	Debug authentication is not required	Response contains no key ID. Debugging will be enabled after exiting SACI.
0xC3	Only non-invasive debugging is allowed	Response contains no key ID. Debugging will be enabled after exiting SACI.
Any other value	Debugging is not allowed	Response result is NOT_ALLOWED

The key ID is fetched from Scfg.debugAuthCfg.secureKey or Scfg.debugAuthCfg.nonSecureKey based on the requested auth level.

As described in the SACI_CMD_DEBUG_REQ_CHALLENGE and SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP sections. Once the debug auth process has started it must be completed without interruption by non debug auth related commands. For this purpose, the SACI_CMD_DEBUG_REQ_KEY_ID is considered a debug auth related command meaning an ongoing debug auth process will not be halted by submitting this command. On the other hand, the debug auth process will

also not begin by submitting this command meaning it can be submitted at any time without consequence on the state of a future or ongoing debug auth process.

Restrictions

CCFG must be valid.

Ccfg.debugCfg.authorization = 0xA5, 0x5A or 0xC3.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1D	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved
1	31:0	authLevel	User defined	The requested authentication level for specifying which key ID to return • 0x401AA5A5 for requesting the key ID capable for secure debug access • 0x989B5A5A for requesting the key ID capable for non-secure debug access • 0xFB86C3C3 for requesting the key ID capable for non-invasive only debug access

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x1D	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_DEBUG_AUTH_LVL_PARAM if the authLevel is invalid • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0 or 2	Size of additional response data, in number of 32-bit words: • 2 if debug authentication is required • 0 if debug authentication is not required, or debugging is not allowed
2:1	31:0	keyId	Scfg.debugAuthCfg.secureKey.keyID or Scfg.debugAuthCfg.nonSecureKey.keyID	The 64-bit debug key ID: • The first byte of the key ID is in bits 7:0 of word 1 • The last byte of the key ID is in bits 31:24 of word 2

Check Sequence

These checks are performed before command execution, in the indicated order:

- If Ccfg is valid and Scfg is valid and Ccfg.debugCfg.authorization = 0xA5 but requested authLevel is invalid: Fail with result INVALID_DEBUG_AUTH_LVL_PARAM
- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.2.6 SACI_CMD_DEBUG_REQ_CHALLENGE

If the SACI_CMD_DEBUG_REQ_KEY_ID command returns a 64-bit key ID, the host must use this command to request the 40 byte debug challenge vector.

The content of the challenge is configured via the Scfg.debugAuthCfg.challengeVector.

- If Scfg.debugAuthCfg.challengeVector.lifetime = 0xF1A1A5A5 (SCFG_DBGAUTH_EPHEMERAL_LIFETIME)
  - The challenge vector will contain a cryptographically random number causing no two requested vectors to be identical
- If Scfg.debugAuthCfg.challengeVector.lifetime = 0x51445A5A (SCFG_DBGAUTH_ENDLESS_LIFETIME)
  - The challenge vector will **not** contain a cryptographically random number causing every requested vector for a specific device to be identical

- If Scfg.debugAuthCfg.challengeVector.deviceConst= 0x3262A5A5 (SCFG_DBGAUTH_DEVICE_MAC_CONST)
  - The challenge vector will contain the device specific MAC address causing no two devices to produce the same challenge vector
- If Scfg.debugAuthCfg.challengeVector.deviceConst = 0x62BB5A5A (SCFG_DBGAUTH_DEVICE_ZERO_CONST)
  - The challenge vector will **not** contain the device specific MAC address causing every requested vector from device to device to produce the same vector (depending on the value of Scfg.debugAuthCfg.challengeVector.lifetime)

The requested 40 byte debug challenge vector must then be signed by the host using the private key which corresponds to the public key on the device. The exact public/private key pair to use is determined by the 64-bit key ID returned by the SAC_CMD_DEBUG_REQ_KEY_ID command. The type of cryptographic signing depends on the type of the key pair being used. The type of key pair depends on the configuration of Scfg.secBootCfg.policyCfg.authAlgorithm

After signing, the host must continue the debug auth process by sending the SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP command.

This command will trigger the start of the "debug auth process". This process shall not be interrupted by non debug auth related commands. If it is, then the process will be halted and this command must be submitted again to complete the debug auth process. The list of debug auth related commands that can be sent without halting the ongoing debug auth process are:

- SACI_CMD_DEBUG_REQ_KEY_ID
- SACI_CMD_DEBUG_REQ_CHALLENGE
  - Note that if this command is submitted again, it will technically begin a new debug auth process which could result in a different challenge vector based on the configuration of Scfg.debugAuthCfg.challengeVector
- SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP

Restrictions

CCFG must be valid.

SCFG must be valid.

Ccfg.debugCfg.authorization = 0xA5 or 0x5A.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1E	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

1	31:0	authLevel	User defined	The requested authentication level for the debug authentication process being started • 0x401AA5A5 for requesting a challenge vector capable for secure debug access • 0x989B5A5A for requesting a challenge vector capable for non-secure debug access • 0xFB86C3C3 for requesting a challenge vector capable for non-invasive only debug access

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x1E	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • NOT_ALLOWED if restrictions are not met • HSM_BOOT_FAILED if the HSM FW was unable to boot while generating a cryptographically random number • CMD_FAILED if the HSM FW was unable to generate a cryptographically random number • INVALID_DBG_AUTH_CONFIG if an invalid Scfg.debugAuthCfg was detected • INVALID_DBUG_AUTH_LVL_PARAM if authLevel was invalid
	31:24	dataWordCount	0 or 10	Size of additional response data, in number of 32-bit words
41:1	31:0	challengeVector	-	The requested 40 byte debug challenge vector

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.2.7 SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP

If the SACI_CMD_DEBUG_REQ_KEY_ID command returns a 64-bit key ID, the host must first request a challenge via the SACI_CMD_DEBUG_REQ_CHALLENGE command, sign the challenge and then use this command to submit the challenge response.

This command will trigger the end of the "debug auth process". This process shall not be interrupted by non debug auth related commands. If it is, then the process will be halted and the debug auth process must be started again. The list of debug auth related commands that can be sent without halting the ongoing debug auth process are:

- SACI_CMD_DEBUG_REQ_KEY_ID
- SACI_CMD_DEBUG_REQ_CHALLENGE

  - Note that if this command is submitted again, it will technically begin a new debug auth process which could result in a different challenge vector based on the configuration of Scfg.debugAuthCfg.challengeVector
- SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP
  - Note that this command will end the ongoing debug auth process

Take special care to understand the BLE High PG2.0's persistent debug feature

After the SAC_CMD_DEBUG_SUBMIT_CHALLENGE_RESP command is completed successfully, the BLE High PG2.0 device will persist the debug authentication. This debug authentication will persist either until the device goes through a power cycle or until the SACI_CMD_DEBUG_CLOSE_SESSION command is sent.

Restrictions

CCFG must be valid.

SCFG must be valid.

There must be an ongoing debug auth process by first submitting the SACI_CMD_DEBUG_REQ_CHALLENGE command.

Ccfg.debugCfg.authorization = 0xA5 or 0x5A.

Parameter Words

Words	Bits	Fields	Value	Description
0	7:0	cmdId	0x1F	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	wordCount	-	Length of the remainder of the command in 32-bit words
1	31:0	pubKeyByteCount	-	Length of the public key in 8-bit bytes (max = 512)
2	31:0	signatureByteCount	-	Length of the signature in 8-bit bytes (max = 384)
131:3	31:0	publicKey	-	The public key for debug authentication in the DER format. Length of the key depends on the type of key and signing process. • The first byte of the public key is in bits 7:0 of word 3 • If the length of the key is less than the max then padding bytes of 0x00 should be added to fill up the entire field

516:132	31:0	signature	-	The resulting signature from signing the challenge vector Length of the signature depends on the type of key and signing process. • The first byte of the signature is in bits 7:0 of word 132 • If the length of the signature is less than the max then padding bytes of 0x00 should be added to fill up the entire field

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x1F	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. • NOT_ALLOWED if restrictions are not met • INVALID_SIZE_PARAM if either pubKeyByteCount or signatureByteCount are invalid • KEY_HASH_MISMATCH if the public key does not match the appropriate publicKeyHash in Scfg.debugAuthCfg • INVALID_DBG_AUTH_LVL_PARAM if the internal state of the auth level of the ongoing debug auth process is incorrect • CMD_FAILED if SHA256 hash calculation failed • INVALID_KEY_PARAM if the public key provided cannot be parsed correctly • CHALLENGE_RESP_VERIFY_FAIL if the signature cannot be verified correctly • INVALID_DBG_AUTH_CONFIG if the Scfg.secBootCfg.policyCfg.authAlgorithm is not a valid algorithm • SUCCESS if the debug authorization process was successful
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If the pubKeyByteCount or signatureByteCount are invalid: Fail with result INVALID_SIZE_PARAM
- if the signature does not pass verification: Fail with the result of CMD_FAILED

9.3.2.2.8 SACI_CMD_DEBUG_CLOSE_SESSION

The BLE High PG2.0 device has a feature known has debug persistence. Once the SACI_CMD_DEBUG_SUBMIT_CHALLENGE_RESP command has returned with success the device will persist the successful debug authentication. This means that a simple reset of the device will not clear the debug authentication status. There are three ways to clear the debug persistence.

1. Sending the SACI_CMD_DEBUG_CLOSE_SESSION command
2. Power cycling the device
3. Using either the debugger and or a flash application to clear the debug persistence bits in the relevant SYS0 register and then performing a SW reset.

Restrictions

None.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x20	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x20	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	SUCCESS	Command result
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

No checks.

9.3.2.2.9 SACI_CMD_BLDR_APP_RESET_DEVICE

Reset the device, with or without reentering SACI.

The command has an option to wait for an SWD disconnection sequence (DBGSS:DBGBCTRL.SWDSEL = 0) before the reset is triggered.

- If used, the boot code will not enter SACI after the reset
  - CFGAP.DEVICESTATUS.BOOTSTA is changed to 0x36 (WAIT_SWD_DISCONNECT) when starting to wait for the disconnect sequence
- If not used, the boot code will reenter SACI after the reset (or move on to the bootloader/application after the SACI inactivity timeout)

There is a 1 ms delay immediately before the reset is triggered.

The command uses PMCTL.RSTCTL.SYSRSTREQ to trigger a system reset. This is indicated by PMCTL.RSTSTA.SYSRSTEV = 1 after the reset.

Restrictions

None.

Table 9-17. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x14	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	16	waitForSwdDisconnect	-	Specify whether to wait for SWD disconnection before the device reset occurs: • 0 to reset and re-enter SACI • 1 to wait for SWD disconnection sequence, and then reset without re-entering SACI
	31:17	reserved0	0x0000	Reserved

Table 9-18. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x14	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result (no special result codes for this command) [1]
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

(1) The command only generates a response if waitForSwdDisconnect = 1. The response is generated before the SWD disconnect sequence detection.

9.3.2.2.10 SACI_CMD_BLDR_APP_EXIT_SACI_RUN

Exit SACI, and run bootloader or application.

If a bootloader is specified in CCFG or FCFG, the device enters the bootloader. Otherwise the device enterts the application.

The device enables access to AHB-AP if Ccfg.debugCfg.authorization = 0x5A, or if SACI_CMD_DEBUG_SUBMIT_AUTH has been performed successfully. This allows a debugger to "attach to running target".

Restrictions

SACI_CMD_FLASH_ERASE_CHIP and/or SACI_CMD_FLASH_PROG_CCFG_SECTOR must not have been used during the current SACI session.

Bootloader must be specified in CCFG or FCFG, or there must be a valid application.

Table 9-19. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x15	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved

Table 9-20. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x15	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.3 Flash Programming Commands

9.3.2.3.1 SACI_CMD_FLASH_ERASE_CHIP

Perform chip erase.

This erases the CCFG sector and MAIN sectors of the flash, by:

- Invalidating CCFG (all fields in Ccfg.bootCfg changed to 0)
- Erasing all MAIN sectors, except retained sectors (if any)
- Erasing the CCFG sector

The command has an option to retain selected MAIN sectors:

- Specified by the existing CCFG (before the chip erase) in:
  - Ccfg.chipEraseRetain.mainSectors0_31 (1 sector per bit) and Ccfg.chipEraseRetain.mainSectors32_255 (8 sectors per bit)
- The option relies on sticky write/erase protection in the VIMS module. Therefore, after use:
  - SACI_CMD_FLASH_ERASE_CHIP cannot be used again during the current SACI session
  - The retained MAIN sectors are write protected during the current SACI session

If successful, CCFG becomes invalid:

- CCFG restrictions do no longer apply
- Commands that require valid CCFG are prohibited

Restrictions

These conditions must be true:

- Fcfg.permissions.allowChipErase = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.permissions.allowChipErase = 0xA (CCFG_PERMISSION_ALLOW)
- If the "retain selected MAIN sectors" option is used:
  - CCFG must be valid (Ccfg.bootCfg.crc32 is valid).
  - For flash sector not valid for the device type, the value of these invalid sectors within Ccfg.flashProt.chipEraseRetain.mainSectors0_31 and Ccfg.flashProt.chipEraseRetain.mainSectors32_255, must be set to the register reset value of the corresponding sectors within the VIMS:WEPRA and VIMS:WEPRB protection registers
- SACI_CMD_FLASH_ERASE_CHIP must not have executed previously in the current SACI session with the "retain selected MAIN sectors" option

Considerations

This command modifies CCFG. Certain commands are not allowed after chip erase:

- SACI_CMD_DEBUG_EXIT_SACI_HALT
- SACI_CMD_BLDR_EXIT_SACI_RUN
- In some cases SACI_CMD_FLASH_ERASE_CHIP (see restrictions)

Reseting the device and reentering SACI is required to reenable those commands.

Table 9-21. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x09	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	16	retainSelMainSectors	-	Retain MAIN sectors, as specified by • Ccfg.chipEraseRetain.mainSectors0_31 (1 sector per bit) • Ccfg.chipEraseRetain.mainSectors32_255 (8 sectors per bit)
	31:17	reserved0	0x0000	Reserved
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)

Table 9-22. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x09	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • FLASH_FSM_ERROR if the flash hardware FSM reported an error • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0 or 2	Size of additional response data, in number of 32-bit words: • 0 if retainSelMainSectors = 0 • 2 if retainSelMainSectors = 1
1	31:0	retainedMain0_31	-	The initial value of Ccfg.chipEraseRetain.mainSectors0_31 (1 sector per bit)
2	31:0	retainedMain32_255	-	The initial value of Ccfg.chipEraseRetain.mainSectors32_255 (8 sectors per bit)

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.2 SACI_CMD_FLASH_ERASE_MAIN_APP

Erase only the MAIN flash application.

The command has an option to retain selected MAIN sectors:

- Specified by the existing CCFG (before the main app erase) in:
  - Ccfg.chipEraseRetain.mainSectors0_31 (1 sector per bit), Ccfg.chipEraseRetain.mainSectors32_255 (8 sectors per bit) and Ccfg.chipEraseRetain.mainSectors256_511 (8 sectors per bit)
- The option relies on sticky write/erase protection in the VIMS module. Therefore, after use:
  - SACI_CMD_FLASH_ERASE_MAIN_APP and SACI_CMD_FLASH_ERASE_CHIP cannot be used again during the current SACI session
  - The retained MAIN sectors will be write protected during the current SACI session

The command will always protect the HSM FW which also resides in MAIN sectors. Before erasure, this command will enable sticky write/erase protection in the VIMS module to ensure the HSM FW is protected. It is not necessary to use Ccfg.chipEraseRetain fields in order to protect the HSM FW when using this command.

Restrictions

These conditions must be true:

- Fcfg.misc.allowMainAppErase = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.misc.allowMainAppErase = 0xA (CCFG_PERMISSION_ALLOW)
- If the "retain selected MAIN sectors" option is used:
  - CCFG must be valid
  - For flash sector not valid for the device type, **for BLE High PG2.0** the value of these invalid sectors within Ccfg.flashProt.chipEraseRetain.mainSectors0_31, Ccfg.flashProt.chipEraseRetain.mainSectors32_255 and Ccfg.chipEraseRetain.mainSectors256_511, must be set to the register reset value of the corresponding sectors within the VIMS:WEPRA, VIMS:WEPRB0 and VIMS:WEPRB1 protection registers
- SACI_CMD_FLASH_ERASE_MAIN_APP or SACI_CMD_FLASH_ERASE_CHIP must not have executed previously in the current SACI session with the "retain selected MAIN sectors" option

Side Effects

Certain commands are not allowed after SACI_CMD_FLASH_ERASE_MAIN_APP:

- SACI_CMD_DEBUG_EXIT_SACI_HALT
- SACI_CMD_BLAPP_EXIT_SACI_RUN
- In some cases SACI_CMD_FLASH_ERASE_MAIN_APP or SACI_CMD_FLASH_ERASE_CHIP (see restrictions)

Reset the device and reenter SACI to reenable those commands.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1C	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	16	retainSelMainSectors	-	Retain MAIN sectors, as specified by • Ccfg.chipEraseRetain.mainSectors0_31 (1 sector per bit) • Ccfg.chipEraseRetain.mainSectors32_255 (8 sectors per bit) • Ccfg.chipEraseRetain.mainSectors256_511 (8 sectors per bit)
	31:17	reserved0	0x0000	Reserved
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)

Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1C	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • FLASH_FSM_ERROR if the flash hardware FSM reported an error • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0 or 3	Size of additional response data, in number of 32-bit words: • 0 if retainSelMainSectors = 0 • 3 if retainSelMainSectors = 1
1	31:0	retainedMain0_31	-	The initial value of Ccfg.chipEraseRetain.mainSectors0_31 (1 sector per bit)
2	31:0	retainedMain32_255	-	The initial value of Ccfg.chipEraseRetain.mainSectors32_255 (8 sectors per bit)
3	31:0	retainedMain256_511	-	The initial value of Ccfg.chipEraseRetain.mainSectors256_511 (8 sectors per bit)

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.3 SACI_CMD_FLASH_PROG_CCFG_SECTOR

Program the entire CCFG sector, with option to skip the user record part.

If skipped, the user record (Ccfg.userRecord) can be programmed later, using SACI_CMD_FLASH_PROG_CCFG_USER_REC.

The CCFG is still considered invalid after executing this command. The new CCFG sector contents take effect after reset.

Restrictions

All bytes in the CCFG sector must be 0xFF before the CCFG sector programming begins (a chip erase must have been performed since the previous CCFG programming).

Considerations

This command modifies CCFG. Certain commands are not allowed after CCFG sector programming:

- SACI_CMD_MISC_GET_CCFG_USER_REC
- SACI_CMD_DEBUG_EXIT_SACI_HALT
- SACI_CMD_BLDR_EXIT_SACI_RUN

Reseting the device and reentering SACI is required to reenable those commands.

Table 9-23. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0C	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	16	skipUserRec	-	Skip user record part
	31:17	reserved0	0x0000	Reserved
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)
513:2	31:0	data	-	Bytes to be programmed: • The first byte is in bits 7:0 of word 2 • The last byte is in bits 31:24 of word 513 If skipUserRec = 1, the user record part of data is don't care.

Table 9-24. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0C	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • FLASH_FSM_ERROR if the flash hardware FSM reported an error • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.4 SACI_CMD_FLASH_PROG_CCFG_USER_REC

Program the user record part of the CCFG sector, Ccfg.userRecord.

This command can be used **after** SACI_CMD_FLASH_PROG_CCFG_SECTOR has executed with the option to skip the user record.

Restrictions

All bytes in the CCFG user record must be 0xFF before the CCFG user record programming begins.

Table 9-25. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0D	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	reserved0	0x0000	Reserved
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)
33:2	31:0	data	-	Bytes to be programmed: • The first byte is in bits 7:0 of word 2 • The last byte is in bits 31:24 of word 33

Table 9-26. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0D	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • FLASH_FSM_ERROR if the flash hardware FSM reported an error • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.5 SACI_CMD_FLASH_PROG_OTP_SECTOR

Program the One Time Programmable(OTP) sector. The OTP sector may not function exactly as you would expect given the OTP name. In reality, the OTP sector is simply another 1T nonmain sector just as the CCFG is. It has the same physical properties as the CCFG which means that the OTP sector can in fact be physically written multiple times. OTP is used to hold HSM assets, so from the application's perspective it is designed to be immutable. This command can only be used if it is preceded by a SACI_CMD_FLASH_ERASE_CHIP resulting in the OTP sector being completely erased.

Restrictions

All bytes in the OTP sector must be 0xFF before the OTP sector programming begins (a chip erase must have been performed since the previous OTP programming).

Side-Effects

This command modifies OTP. Certain commands are not allowed after OTP sector programming:

- SACI_CMD_DEBUG_EXIT_SACI_HALT
- SACI_CMD_BLAPP_EXIT_SACI_RUN

Reset the device and reenter SACI to reenable those commands.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x19	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	byteCount	-	Number of bytes to program. If 0, the command has no effect.
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)
513:2	31:0	data	User defined	Bytes to be programmed: • The first byte is in bits 7:0 of word 2 • Although only the first **byteCount** bytes will be written, zero-padding must be added to send the full size of the OTP sector

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x19	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • FLASH_FSM_ERROR if the flash hardware FSM reported an error • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.6 SACI_CMD_FLASH_PROG_SCFG_SECTOR

Program the SCFG sector.

- By nature of the Scfg.keyRingCfg, it's typical to only program one or two of the keyEntries and leave the remaining keyEntries empty. This is intentional and for the purpose of performing key updates in the field at a future time via the secure boot key update process.
- If you wish to leave the last *N* keyEntries[] slots open for future use then the byteCount parameter of the command should be **CCFG_SIZE - (N * sizeof(keyRingEntry_t))**
  - Only the last (SCFG_KEY_HASH_RING_NUM-1) keyEntry slots can be left unprogrammed
  - The remaining/unprogrammed bytes of the SCFG must be sizeof(keyRingEntry_t) aligned

Restrictions

Since SCFG is a 2T sector all bytes in the SCFG will be random after erasure. For this reason, the SCFG can only be programmed if the SCFG is invalid. SCFG is invalid if the boot code detects an issue in the CRC field or if the SCFG was specifically erased during the SACI Idle loop. The only way to do this is the SACI_CMD_FLASH_ERASE_CHIP cmd which will invalidate the SCFG.

Side Effects

This command modifies SCFG. Certain commands are not allowed after SCFG sector programming:

- SACI_CMD_DEBUG_EXIT_SACI_HALT
- SACI_CMD_BLAPP_EXIT_SACI_RUN

Reset the device and reenter SACI to reenable those commands.

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1A	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	byteCount	-	Number of bytes to program. If 0, the command has no effect. • min = 276 bytes = (SCFG_SIZE - (sizeof(keyEntry) * 17)) • max = 1024 bytes = SCFG_SIZE
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)
257:2	31:0	data	User defined	Bytes to be programmed: • The first byte is in bits 7:0 of word 2

Response Words

Words	Bits	Field	Value	Description

0	7:0	cmdId	0x1A	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • FLASH_FSM_ERROR if the flash hardware FSM reported an error • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If byteCount is invalid: Fail with result
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.7 SACI_CMD_FLASH_PROG_MAIN_SECTOR

Program all or a part of one MAIN sector (see Chapter 7).

The programming starts when the specified number of bytes (padded to a whole number of words) has been received by SACI.

Restrictions

These conditions must be true:

- Fcfg.permissions.allowFlashProgram = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.permissions.allowFlashProgram= 0xA (CCFG_PERMISSION_ALLOW)

The sector can be protected by:

- Fcfg.flashProt.writeEraseProt.mainSectors0_31 and Ccfg.flashProt.writeEraseProt.mainSectors0_31 (1 sector per bit)
- Fcfg.flashProt.writeEraseProt.mainSectors32_255 and Ccfg.flashProt.writeEraseProt.mainSectors32_255 (8 sectors per bit)

Table 9-27. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0E	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	31:16	byteCount	-	Number of bytes to program. If 0, the command has no effect.
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)
2	31:0	firstByteAddr	-	Address of the first byte to be programmed
3+	31:0	data	User defined	Bytes to be programmed: • The first byte is in bits 7:0 of word 3 • Zero-padding must be added to the most significant part of the last word if byteCount is not a multiple of 4.

Table 9-28. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0E	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • INVALID_ADDRESS_PARAM if the firstByteAddr parameter is invalid • INVALID_SIZE_PARAM if the byteCount parameter is invalid (address range spans over multiple MAIN sectors) • FLASH_FSM_ERROR if the flash hardware FSM reported an error – May indicate that the sector was retained by chip erase during the current SACI session • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If firstByteAddr is invalid: Fail with result INVALID_ADDRESS_PARAM
- If byteCount = 0: Succeed with result SUCCESS
- If byteCount is invalid: Fail with result INVALID_SIZE_PARAM
- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

9.3.2.3.8 SACI_CMD_FLASH_PROG_MAIN_PIPELINED

Program multiple whole, back-to-back MAIN sectors of the flash.

This allows the entire MAIN bank to be programmed with only one SACI command, with high performance.

For this command, SACI has data buffers for two MAIN sectors. This enables pipelined programming:

- SACI starts programming a flash sector when all data for that sector has been received.
- During this programming, the host can send the data for the next sector.

Flow Control Mechanism and Response Handling

When SACI receives the last word of a sector, this triggers or pends programming of that sector. When SACI finishes programming of a sector, a response is generated for that sector. This can overwrite the response for the previous sector if the host has not yet read that.

If SACI fails to program a sector (e.g. due to protection), the command ends, and the response for that sector indicates the error. If the host skips/misses reading the response for a sector, the host can assume that the sector was successfully programmed if the host sees the response for a later sector.

The host must not write data for another sector while one sector is being programmed, and another sector is pending. This means:

- The host does not need to check the response until the host has written the first two sectors.
- After the two first sectors, the host can only write data for sector N after the host has read the response for either sector N-2 (one free buffer) or sector N-1 (two free buffers).

The host should always wait for and check the response for the last sector.

Restrictions

These conditions must be true:

- Fcfg.permissions.allowFlashProgram = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.permissions.allowFlashProgram= 0xA (CCFG_PERMISSION_ALLOW)

Each sector can be protected by:

- Fcfg.flashProt.writeEraseProt.mainSectors0_31 and Ccfg.flashProt.writeEraseProt.mainSectors0_31 (1 sector per bit)
- Fcfg.flashProt.writeEraseProt.mainSectors32_255 and Ccfg.flashProt.writeEraseProt.mainSectors32_255 (8 sectors per bit)

Table 9-29. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0F	Command ID
	15:8	respSeqNumber	User defined	Base response sequence number
	31:16	reserved0	0x0000	Reserved
1	31:0	key	0xB7E3A08F	Flash operation key (magic number)
2	31:0	firstSectorAddr	-	Address of the first byte of the first sector to be programmed

Then, for each flash sector:

Words	Bits	Field	Value	Description
511:0	31:0	data	User defined	Sector data: • The first byte of the sector is in bits 7:0 of word 0 • The last byte of the sector is in bits 31:24 of word 511

This response is generated after each sector has been programmed:

Table 9-30. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x0F	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Response sequence number. For the first sector, the number is equal to the respSeqNumber in the first parameter. For later sectors, the number increments by 1 for each sector.
	23:16	result	-	Command result. One of the common results, or: • INVALID_KEY_PARAM if the key parameter is incorrect • INVALID_ADDRESS_PARAM if the firstSectorAddr parameter is invalid • PARAM_BUFFER_OVERFLOW if the host sends sector data too quickly, without implementing the described response-based flow control mechanism • FLASH_FSM_ERROR if the operation failed (not due to restrictions) – Can indicate that the sector was retained by chip erase during the current SACI session • NOT_ALLOWED if restrictions are not met (the command has no effect)
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Checks

These checks are performed before command execution, in the indicated order:

- If firstSectorAddr is invalid: Fail with result INVALID_ADDRESS_PARAM

These checks are performed before programming of each sector, in indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED
- If key is invalid: Fail with result INVALID_KEY_PARAM

The command finishes prematurely when a buffer overflow condition occurs, with result PARAM_BUFFER_OVERFLOW.

9.3.2.3.9 SACI_CMD_FLASH_VERIFY_MAIN_SECTORS

Verify the contents of one or more whole flash MAIN sectors, using CRC32, with option to exclude the last 4 bytes, or check that the sectors are blank (all bytes are 0xFF).

The command perform one of these checks:

- Check that the specified address range is blank (all bytes are 0xFF).
- Compute and check CRC32 over a whole number of back-to-back flash MAIN sectors
  - This can be used when the flash programming tool is able to calculate CRC32
- Compute and check CRC32 over a whole number of back-to-back flash MAIN sectors, minus 4 bytes
  - This can be used when the flash programming tools is unable to calculate CRC32, but the expected CRC32 is stored in the last 4 bytes of the last sector

The command result is SUCCESS if the performed check is successful. The command result is also SUCCESS if the number of bytes to check is 0.

Restrictions

These conditions must be true:

- Fcfg.permissions.allowFlashVerify = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.permissions.allowFlashVerify= 0xA (CCFG_PERMISSION_ALLOW)

Table 9-31. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x10	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	30:16	reserved0	0	Reserved
	31	doBlankCheck	-	Check if the entire address range is blank (all bytes are 0xFF), instead of CRC check
1	31:0	firstSectorAddr	-	Address of the first byte of the first sector
2	31:0	byteCount	-	Number of bytes to calculate CRC32 over, one of the following: • Whole number of sectors • Whole number of sectors minus 4 bytes
3	31:0	expCrc32	-	Expected CRC32

Table 9-32. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x10	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • INVALID_ADDRESS_PARAM if the firstSectorAddr parameter is invalid • INVALID_SIZE_PARAM if the byteCount parameter is invalid • For doBlankCheck = 0: CRC32_MISMATCH if the calculated CRC32 does not match expCrc32 • For doBlankCheck = 1: BLANK_CHECK_FAILED if one or more bits in the address range are 0 • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If firstSectorAddr is invalid: Fail with result INVALID_ADDRESS_PARAM
- If byteCount = 0: Succeed with result SUCCESS
- If byteCount is invalid: Fail with result INVALID_SIZE_PARAM
- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.3.10 SACI_CMD_FLASH_VERIFY_CCFG_SECTOR

Verify the specified parts of the flash CCFG sector, using CRC32, or check that the entire sector is blank (all bytes are 0xFF).

CCFG is divided into four parts, each with an embedded CRC32 that covers the data:

- Boot configuration part
  - Data:
    - Ccfg.bootCfg, excluding Ccfg.bootCfg.crc32
  - Embedded CRC32:
    - Ccfg.bootCfg.crc32
- Central part
  - Data:
    - Ccfg.hwOpts
    - Ccfg.misc
    - Ccfg.flashProt
    - Ccfg.permissions
    - Ccfg.hwInitCopyList
  - Embedded CRC32:
    - Ccfg.crc32
- User record part
  - Data:
    - Ccfg.userRecord, excluding Ccfg.userRecord.crc32
  - Embedded CRC32:
    - Ccfg.userRecord.crc32
- Debug configuration part
  - Data:
    - Ccfg.debugCfg, excluding Ccfg.debugCfg.crc32
  - Embedded CRC32:
    - Ccfg.debugCfg.crc32

The command performs one of these checks:

- Check that CCFG is blank (all bytes are 0xFF).
- Compute and check CRC32 of data, using only embedded CRCs:
  - For all parts of CCFG, or
  - For all parts of CCFG except the user record part
- Compute and check CRC32 of data, using both embedded CRCs and expected CRCs (provided in the command):
  - For all parts of CCFG, or
  - For all parts of CCFG except the user record part

The command result is SUCCESS if all performed checks are successful.

Restrictions

These conditions must be true:

- Fcfg.permissions.allowFlashVerify = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.permissions.allowFlashVerify= 0xA (CCFG_PERMISSION_ALLOW)

Table 9-33. Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x11	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	16	checkExpCrcs	-	Check CCFG data also against the expected CRC32 fields the command: • 0: Use only embedded CRCs • 1: Use both embedded CRCs and the expected CRCs
	17	skipUserRec	-	Skip CRC check of the user record part of CCFG
	30:18	reserved0	0b000000	Reserved
	31	doBlankCheck	-	Check if the entire CCFG sector is blank (all bytes are 0xFF), instead of CRC checks
1	31:0	expBootCfgCrc32	-	Expected CRC32 of the boot configuration part: • If checkExpCrcs = 1: Same value as in Ccfg.bootCfg.crc32 • Otherwise: Don't care
2	31:0	expCentralCrc32	-	Expected CRC32 of the central part: • If checkExpCrcs = 1: Same value as in Ccfg.crc32 • Otherwise: Don't care
3	31:0	expUserRecCrc32	-	Expected CRC32 of the user record part: • If skipUserRec = 0 and checkExpCrcs = 1: Same value as in Ccfg.userRecord.crc32 • Otherwise: Don't care
4	31:0	expDebugCfgCrc32	-	Expected CRC32 of the debug configuration part: • If checkExpCrcs = 1: Same value as in Ccfg.debugCfg.crc32 • Otherwise: Don't care

Table 9-34. Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x11	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • For doBlankCheck = 0: CRC32_MISMATCH if any of the performed CRC checks failed • For doBlankCheck = 1: BLANK_CHECK_FAILED if one or more bits in the CCFG sector are 0 • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.3.2.3.11 SACI_CMD_FLASH_VERIFY_SCFG_SECTOR

Verify the specified parts of the flash SCFG sector, using CRC32. There is no check for blank SCFG because it is in 2T memory which will read as random when unprogrammed.

The SCFG is covered by a single CRC which spans from the first field to the Scfg.res0 field

- SCFG
  - Data:
    - Scfg.hsmCfg.publicKeyHash through entire Scfg.res0
  - Embedded CRC32:
    - Scfg.crc32

The command perform one of these checks:

- Compute and check CRC32 of data, using only embedded CRCs
- Compute and check CRC32 of data, using both embedded CRCs and expected CRCs (provided in the command)

The command result is SUCCESS if all performed checks are successful.

Restrictions

These conditions must be true:

- Fcfg.permissions.allowFlashVerify = 0xA (FCFG_PERMISSION_ALLOW)
- If CCFG is valid:
  - Ccfg.permissions.allowFlashVerify= 0xA (CCFG_PERMISSION_ALLOW)
- If SCFG is valid:
  - Scfg.permissions.allowFlashVerify = 0xA (SCFG_PERMISSION_ALLOW)

Parameter Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1B	Command ID
	15:8	respSeqNumber	User defined	Optional response sequence number, included in the response header
	16	checkExpCrcs	-	Check SCFG data also against the expected CRC32 fields the command: • 0: Use only embedded CRCs • 1: Use both embedded CRCs and the expected CRCs
	31:17	reserved0	0x00	Reserved
1	31:0	expCrc32	-	Expected CRC32 of the SCFG: • If checkExpCrcs = 1: Same value as in Scfg.crc32 • Otherwise: Don't care

Response Words

Words	Bits	Field	Value	Description
0	7:0	cmdId	0x1B	Command ID, copied from the first command parameter word
	15:8	respSeqNumber	User defined	Optional sequence number, copied from the first command parameter word
	23:16	result	-	Command result. One of the common results, or: • CRC32_MISMATCH if any of the performed CRC checks failed • NOT_ALLOWED if restrictions are not met
	31:24	dataWordCount	0	Size of additional response data, in number of 32-bit words

Check Sequence

These checks are performed before command execution, in the indicated order:

- If any restriction is violated: Fail with result NOT_ALLOWED

9.4 Bootloader Support

Whether a bootloader is run or not and where bootloader parameters are picked from depends on CCFG.

Table 9-35. Bootloader CCFG Configurations

CCFG valid	CCFG.bootCfg.pBldrVtor	Bootloader Invoked	Bootloader parameters selected
No	-	ROM Serial bootloader	FCFG.bootCfg.bldrParam
Yes	USE_FCFG (0xFFFFFFF0)	ROM Serial bootloader	FCFG.bootCfg.bldrParam
Yes	FORBID (0xFFFFFFFC)	None	-
Yes	UNDEF (0xFFFFFFFF)	ROM Serial bootloader	CCFG.bootCfg.bldrParam

If a bootloader is selected then that bootloader is always invoked as part of the boot process. The bootloader must thus quickly determine whether to activate or not. The ROM serial bootloader determines whether the serial bootloader has been triggered or not within a few microseconds.

9.4.1 Bootloader v.s Secure Boot

The ROM SBL and Secure Boot features are mutually exclusive. When Secure Boot is enabled in the SCFG, the ROM SBL will not execute. When Secure Boot is enabled, the concept of the bootloader is transformed and alternatively defined by the SCFG settings. See Chapter 11 for more details on how to configure the device to execute a Secondary Secure Bootloader (SSB).

9.5 ROM Serial Bootloader

The ROM contains a simple serial bootloader that by default is run on a blank device. Users can elect to run the serial bootloader before their application once one is programmed. The ROM serial bootloader:

- Implements a set of commands for programming/erasing flash (similar to SACI but slightly simplified)

- These commands can be accessed over UART or SPI. Whichever interface sees activity first is selected from there on out. UART has an autobaud feature and can detect the baud rate within the range from 9600 to 1.6 Mbaud.
- Supports selecting any DIO pin as a trigger pin and selecting which logic level triggers the bootloader. Otherwise the bootloader continues on to application (if one exists) immediately

9.5.1 ROM Serial Bootloader Interfaces

The bootloader communicates with an external device over a 2-pin UART or a 4-pin SPI interface. The communication protocol and transport layers are described in the following subsections.

9.5.1.1 Packet Handling

The bootloader uses well-defined packets to ensure reliable communications with the external communicating program. All communications (with the exception of the UART automatic baud [see UART Transport Section 9.5.1.2.1]) use these well-defined packets. The packets are always acknowledged or not acknowledged by the communicating devices with defined ACK or NACK bytes.

The packets use the same format for receiving and sending packets. This format includes the method to acknowledge successful or unsuccessful reception of a packet.

While the actual signaling on the serial ports is different, the packet format remains the same for supported UART and SPI interfaces.

Packet send and packet receive must adhere to the simple protocol shown in Figure 9-2.

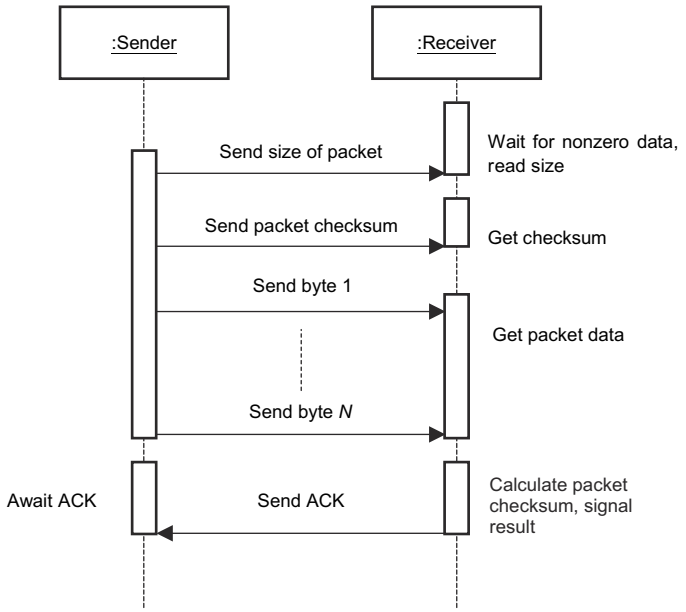

Figure 9-2. Sequence Diagram for Send and Receive Protocol

Perform the following steps to successfully send a packet:

1. Send the size of the packet to be transmitted to the device. The size is always the size of the data + 2 with truncation to 8 bits.
2. Send the checksum of the data buffer to ensure proper transmission of the command. The checksum algorithm is a sum of the data bytes.
3. Send the actual data bytes.
4. Wait for a single-byte acknowledgment from the device that the data was properly received or that a transmission error was detected.

Perform the following steps to successfully receive a packet:

1. Wait for nonzero data to be returned from the device. This is important as the device may send zero bytes between a sent and a received data packet. The first nonzero byte received is the size of the packet that is being received.
2. Read the next byte, which is the checksum for the packet.
3. Read the data bytes from the device. During the data phase, packet size minus 2 bytes is sent. For example, if the packet size was 3, then there is only 1 byte of data to be received.
4. Calculate the checksum of the data bytes and verify it matches the checksum received in the packet.
5. Send an acknowledge byte or a not-acknowledge byte to the device to indicate the successful or unsuccessful reception of the packet.

Acknowledge (ACK) bytes are sent out whenever a packet is successfully received and verified by the receiver. A not-acknowledge (NACK) byte is sent out whenever a sent packet is detected to have an error, usually as a result of a checksum error or just malformed data in the packet, which allows the sender to retransmit the previous packet.

To illustrate packet handling, the basic packet format is shown in Figure 9-3.

In Figure 9-3, the top line shows the device that is transmitting data; the bottom line is the response from the other device.

In this case, a 6-byte packet is sent with the data shown in Figure 9-3. This data results in a checksum of 0x48+0x6f+0x6c+0x61 which, when truncated to 8 bits, is 0x84. The first byte transmitted holds the size of the packet in number of bytes. Then the checksum byte is transmitted. The next bytes to go out are the 4 data bytes in this packet. The transmitter is allowed to send zeros until a nonzero response is received, that is necessary for SPI and is allowed by the UART. The receiver is allowed to return zeros until it is ready to ACK or NACK the packet that is being sent. Neither device transfers a nonzero byte until it has received a response after transmitting a packet.

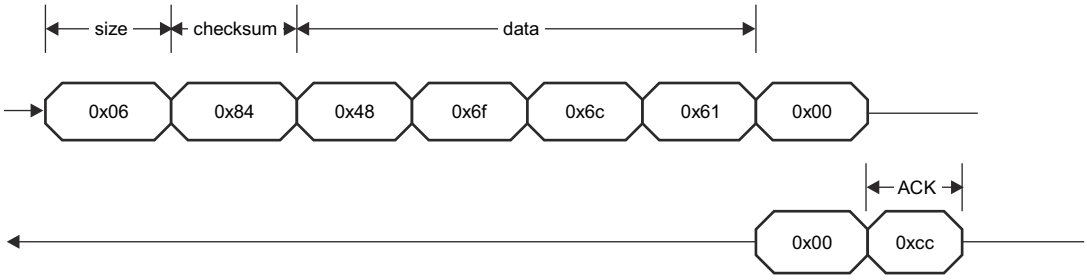

Figure 9-3. Serial Bus Packet Format

9.5.1.1.1 Packet Acknowledge and Not-Acknowledge Bytes

Table 9-36 shows the defined values for packet acknowledge (ACK) and not-acknowledge (NACK) bytes.

Table 9-36. Protocol Acknowledge and Not-Acknowledge Bytes

Protocol Byte	Value
ACK	0xCC
NACK	0x33

9.5.1.2 Transport Layer

The bootloader supports updating through the UART and SPI ports. The SPI port has the advantage of supporting higher and more flexible data rates, but it also requires more connections. The UART has the disadvantage of having slightly lower and possibly less flexible rates. However, the UART requires fewer pins and can be easily implemented with any standard UART connection.

Table 9-37 specifies which serial interface signals are configured to specific DIOs. There is only one possible configurations for the serial interfaces. Configuration of the ROM Bootloader is done between the FCFG and the CCFG. There are defaults that are set in the FCFG that will take effect if a valid CCFG is not present on start-up. If the user wants to alter the defaults set by the FCFG they can update their CCFG to provide the behavior they desire. See Chapter 10.

Table 9-37. Configuration of Serial Interfaces

Signal	serialIoCfgIndex == 0
UART_RX	DIO2
UART_TX	DIO1
SPI_CLK	DIO3
SPI_CS	DIO7
SPI_POCI	DIO5
SPI_PICO	DIO4

The bootloader initially configures only the input pins on the two serial interfaces. By default, all I/O pins have their input buffers disabled, so the bootloader configures the required pins to be input pins so that the bootloader interface is not accessible from a host before this point in time. For this initial configuration of input pins, the firmware configures the IOC to route the input signals listed in Table 9-37 to their corresponding peripheral signals.

The bootloader selects the interface that is the first to be accessed by the external device. Once selected, the TX output pin for the selected interface is configured; the module on the inactive interface (UART or SPI) is disabled. To switch to the other interface, the device must be reset. The delayed configuration of the TX pin imposes special consideration on a SPI controller device regarding the transfer of the first byte of the first packet (see Section 9.5.1.2.2).

9.5.1.2.1 UART Transport

The connections required to use the UART port are the following two pins: UART0 TX and UART0 RX. The device communicating with the bootloader drives the UART0 RX pin on the CC27XX, while the CC27XX drives the UART0 TX pin.

While the baud rate is flexible, the UART serial format is fixed at 8 data bits, no parity, and 1 stop bit. The bootloader automatically detects the baud rate for communication.

9.5.1.2.1.1 UART Baud Rate Automatic Detection

The bootloader provides a method to automatically detect the UART baud rate being used to communicate with it.

To synchronize with the host, the bootloader must receive 2 bytes with the value of 0x55. If synchronization succeeds, the bootloader returns an acknowledge consisting of 2 bytes with the values of 0x00 and 0xCC.

If synchronization fails, the bootloader waits for synchronization attempts.

In the automatic-detection function, the UART0 RX pin is monitored for edges using GPIO interrupts. When enough edges are detected, the bootloader determines the ratio of baud rate and frequency needed to program the UART.

The UART module system clock must be at least 16 times the baud rate; thus, the maximum baud rate can be no higher than 3 Mbaud (48 MHz divided by 16). The maximum baud rate is restricted to 1.6 Mbaud because of the firmware function that detects the transfer rate of the host.

9.5.1.2.2 SPI Transport

The connections required to use the SPI port are the following four pins:

- SPI_POCI

- SPI_PICO
- SPI_CLK
- SPI_CS

The device communicating with the bootloader drives the SPI_PICO, SPI_SCLK, and SPI_CS, while the CC27XX drives the SPI_POCI pin.

The format used for SPI communications is the Motorola format with SPH set to 1 and SPO set to 1 (see Figure 24-5 for more information on this format). Refer to the device specific data-sheet for the maximum rate supported on the SPI clock in the peripheral mode.

The controller must take special consideration (regarding the use of the SPI interface) due to the functionality of not configuring any output pins before the external controller device has selected a serial interface.

Note

On the first packet transferred by the controller, no data is received from the bootloader while the bootloader clocks out the bits in the first byte of the packet.

When the bootloader detects that 1 byte has been received on SPI_PICO, the bootloader configures the SPI_POCI output pin.

Before transmitting the next byte in the first packet, the controller must include a small delay to ensure that the bootloader has completed the configuration of the SPI_POCI output pin.

9.5.2 ROM Serial Bootloader Parameters

The ROM serial bootloader parameters are as follows:

<table>
<tr><th>CCFG.bootCfg.bldrParam</th><th>Name</th><th>Description</th><th>Blank device / FCFG default value</th></tr>
<tr><td>[0]</td><td>bldrEnabled</td><td>If 0, bootloader ignores all commands except BLDR_CMD_GET_STATUS, else normal operation</td><td>1</td></tr>
<tr><td>[1]</td><td>pinTriggerEnabled</td><td>If 0, bootloader unconditionally triggers, else normal pin trigger check is performed</td><td>1</td></tr>
<tr><td>[2]</td><td>pinTriggerLevel</td><td>If 0, a low level on trigger pin triggers bootloader, else a high level</td><td>0</td></tr>
<tr><td>[15:3]</td><td>Reserved</td><td></td><td></td></tr>
<tr><td>[21:16]</td><td>pinTriggerDio</td><td>Index of DIO pin to use for pin trigger check</td><td>21</td></tr>
<tr><td>[23:22]</td><td>Reserved</td><td></td><td></td></tr>
<tr><td>[26:24]</td><td>serialIoCfgIndex</td><td>Index of which I/O mapping to use for UART/SPI:
<table>
<tr><th>UART</th><th>SPI</th><th>Index 0</th><th>Index 1...7</th></tr>
<tr><td>RXD</td><td></td><td>DIO2</td><td>Reserved</td></tr>
<tr><td>TXD</td><td></td><td>DIO1</td><td>Reserved</td></tr>
<tr><td></td><td>POCI</td><td>DIO5</td><td>Reserved</td></tr>
<tr><td></td><td>PICO</td><td>DIO4</td><td>Reserved</td></tr>
<tr><td></td><td>SCLK</td><td>DIO5</td><td>Reserved</td></tr>
<tr><td></td><td>CS</td><td>DIO7</td><td>Reserved</td></tr>
</table></td><td>0</td></tr>
<tr><td>[31:27]</td><td>Reserved</td><td></td><td></td></tr>
</table>

9.5.3 ROM Serial Bootloader Commands

Table 9-38. Command IDs

CMD ID	Value
BLDR_CMD_PING	0x20
BLDR_CMD_GET_STATUS	0x21
BLDR_CMD_GET_PART_ID	0x22
BLDR_CMD_RESET	0x23
BLDR_CMD_CHIP_ERASE	0x24
BLDR_CMD_CRC32	0x25
BLDR_CMD_DOWNLOAD	0x26
BLDR_CMD_DOWNLOAD_CRC	0x27
BLDR_CMD_SEND_DATA	0x28

9.5.3.1 BLDR_CMD_PING

This command is used to receive an acknowledge from the bootloader proving that communication has been established. This command is a single byte.

Byte	Field	Value	Description
0	cmdId	BLDR_CMD_PING	Ping Command ID

9.5.3.2 BLDR_CMD_GET_STATUS

This command returns the status of the last command that was issued. Typically this command should be received after every command is sent to ensure that the previous command was successful or, if unsuccessful, to properly respond to a failure. The command requires one don't care byte in the data of the packet and the bootloader will respond by sending a packet with one byte of data that contains the current status code.

Byte	Field	Value	Description
0	cmdId	BLDR_CMD_GET_STATUS	Get StatusCommand ID

Table 9-39. Return Status Codes

Return Name	Value	Description
BLDR_CMD_RET_SUCCESS	0x40	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that the previous command completed successfully.
BLDR_CMD_RET_UNKNOWN_CMD	0x41	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that the command sent was an unknown command.
BLDR_CMD_RET_INVALID_CMD	0x42	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that the previous command was formatted incorrectly.
BLDR_CMD_RET_INVALID_ADR	0x43	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that the previous download command contained an invalid address value.
BLDR_CMD_RET_FLASH_FAIL	0x44	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that an attempt to program or erase the flash has failed.
BLDR_CMD_RET_CRC_FAIL	0x45	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that the previous CRC32 command match failed.
BLDR_CMD_RET_NEEDS_CHIP_ERASE	0x46	This is returned in response to a **BLDR_CMD_GET_STATUS** command and indicates that the previous Download command failed because a **BLDR_CMD_CHIP_ERASE** command must be run first.

9.5.3.3 BLDR_CMD_GET_PART_ID

This command is sent to the bootloader to get the Part ID of the device.

Byte	Field	Description
0	cmdId	BLDR_CMD_GET_PART_ID command ID

9.5.3.4 BLDR_CMD_RESET

This command is used to tell the bootloader to reset. This is used after downloading a new image to the device to cause the new application to start from a reset. The normal boot sequence occurs and the image runs as if from a hardware reset. This command can also be used to reset the bootloader if a critical error occurs and the host device wants to restart communication with the bootloader.

The bootloader responds with an ACK signal to the host device before actually executing the system reset of the device running the bootloader. This informs the updater host device that the command was received successfully and the part will be reset.

Byte	Field	Description
0	cmdId	BLDR_CMD_RESET command ID

9.5.3.5 BLDR_CMD_CHIP_ERASE

This command is used to perform a chip erase of the device. All main flash bank sectors not protected by FCFG and CCFG protect bits are erased. The CCFG is erased once the bank erase has completed.

This command first invalidates the CCFG and then begin erasing all unprotected sectors in the main flash bank. Once the flash sectors have been erased, the command finally erases the contents of the CCFG.

If the CCFG permissions disallow a chip erase, the command responds with CMD_INVALID_CMD.

Byte	Field	Description
0	cmdId	BLDR_CMD_CHIP_ERASE command ID

9.5.3.6 BLDR_CMD_CRC32

This command is sent to the bootloader to calculate a CRC32 for a specified memory area. The command consists of three 32-bit values that are each transferred MSB first.

The Memory address must be sector aligned. Only memory addresses within the main flash region or the CCFG_BASE address itself are valid.

The Size must be sector aligned or (sector - 4 bytes) aligned.

The combination of memory address and size cannot go outside of either the main flash region or the CCFG region. If the parameters are valid, the command only reports if the expected CRC matches the calculated CRC. Follow up this command with the **BLDR_CMD_GET_STATUS** to read the result of the CRC comparison.

Byte	Field	Description
0	cmdId	BLDR_CMD_CRC32 command ID
1	Memory Address [31:24]	Memory Address to start the CRC calculation
2	Memory Address [23:16]	
3	Memory Address [15:8]	
4	Memory Address [7:0]	
5	Memory Area Size [31:24]	Number of bytes to run the CRC calculation over
6	Memory Area Size [23:16]	
7	Memory Area Size [15:8]	
8	Memory Area Size [7:0]	

Byte	Field	Description
9	Expected CRC [31:24]	The CRC value the host is expecting the CRC calculation results in
10	Expected CRC [23:16]	
11	Expected CRC [15:8]	
12	Expected CRC [7:0]	

9.5.3.7 BLDR_CMD_DOWNLOAD

This command is sent to the bootloader to indicate where to store data and how many bytes are sent by the **BLDR_CMD_SEND_DATA** commands that follow. The command consists of two 32-bit values that are both transferred MSB first.

The first 32-bit value is the address to start programming data into, while the second is the 32-bit size of the data that is to be sent.

This command should be followed by **BLDR_CMD_GET_STATUS** to ensure that the program address and program size were valid for the device running the bootloader.

Byte	Field	Description
0	cmdId	BLDR_CMD_DOWNLOAD command ID
1	Program Address [31:24]	Start address of the download
2	Program Address [23:16]	
3	Program Address [15:8]	
4	Program Address [7:0]	
5	Program Size [31:24]	Number of bytes (length of the download)
6	Program Size [23:16]	
7	Program Size [15:8]	
8	Program Size [7:0]	

9.5.3.8 BLDR_CMD_DOWNLOAD_CRC

This command is sent to the bootloader to indicate where to store data, how many bytes are to be sent by the **BLDR_CMD_SEND_DATA** commands that follow and the CRC32 value covering all the bytes.

The command consists of three 32-bit values that are all transferred MSB first. The first 32-bit value is the address to start programming data into, the second is the 32-bit size of the data that is to be sent and the third is the 32-bit CRC expected value.

This command should be followed by a **BLDR_CMD_GET_STATUS** to ensure that the program address and program size were valid for the device running the bootloader.

Byte	Field	Description
0	cmdId	BLDR_CMD_DOWNLOAD_CRC command ID
1	Program Address [31:24]	Start address of the download
2	Program Address [23:16]	
3	Program Address [15:8]	
4	Program Address [7:0]	
5	Program Size [31:24]	Number of bytes (length of the download)
6	Program Size [23:16]	
7	Program Size [15:8]	
8	Program Size [7:0]	

Byte	Field	Description
9	Expected CRC [31:24]	The expected CRC calculation over the completed download image. If the CRC calculation fails, the download is considered a failure and the content that was downloaded is immediately erased.
10	Expected CRC [23:16]	
11	Expected CRC [15:8]	
12	Expected CRC [7:0]	

9.5.3.9 BLDR_CMD_SEND_DATA

This command should only follow a **BLDR_CMD_DOWNLOAD** command or another **BLDR_CMD_SEND_DATA** command, if more data is needed.

Consecutive send data commands automatically increment the address and continue programming from the previous location. The caller should allow the device to finish the flash programming before issuing another command in order to avoid overflowing the input buffers of the serial interface. The command terminates programming once the number of bytes indicated by the **BLDR_CMD_DOWNLOAD** command has been received. Each time this function is called, it should be followed by a **BLDR_CMD_GET_STATUS** command to ensure that the data was successfully programmed into the flash.

If the bootloader responds with a NACK to this command, the bootloader does not increment the current address to allow re-transmission of the previous data.

A maximum of 253 bytes of data can be sent per **BLDR_CMD_SEND_DATA** command.

Byte	Field	Description
0	cmdId	BLDR_CMD_SEND_DATA command ID
1	download_image[0]	Consecutive bytes of the image to be downloaded
....	....	
X <= 252	download_image[X <= 252]	

9.5.4 Bootloader Firmware Update Example

The following steps can be followed to perform a FW image update to a device enabled to run the ROM Bootloader.

For this example, let's assume we have an updated application which begins at address 0x00000000, has a length of 0x28000 and a CRC over all of the bytes has a value of 0xFACEFACE.

1. The device needs to bootup into the ROM Bootloader. This can be done either by setting the pAppVtor to an invalid value OR by setting the pinTriggerDio to the specified pinTriggerLevel.
2. The bootloader needs to know which serial interface is being used.
   a. UART - send the AutoBaud sequence as described in Section 9.5.1.2.1.1
   b. SPI - send any ROM Bootloader cmd (ping command is a good suggestion)
3. Now that the bootloader is triggered and communicating correctly, prepare the device for the FW image update
   a. Send the BLDR_CMD_CHIP_ERASE command
   b. Wait for the ACK/NACK and then send the BLDR_CMD_GET_STATUS
   c. Wait for the ACK/NACK and ensure the previous command was completed successfully with the BLDR_CMD_RET_SUCCESS value
4. Start the Application Download
   a. Send the BLDR_CMD_DOWNLOAD_CRC command, passing as input the startAddress=(0x00000000), length=(0x28000), CRC=(0xFACEFACE)
   b. wait for the ACK/NACK and then send the BLDR_CMD_GET_STATUS
   c. wait for the ACK/NACK and ensure the previous command was completed successfully with the BLDR_CMD_RET_SUCCESS value
5. Loop over the bytes of the image and send the data to the ROM Bootloader

   a. Send the BLDR_CMD_SEND_DATA command, passing as input the next 252 bytes of the application image.
   b. wait for the ACK/NACK and then send the BLDR_CMD_GET_STATUS
   c. wait for the ACK/NACK and ensure the previous command was completed successfully with the BLDR_CMD_RET_SUCCESS value
   d. Repeat steps 5a-5c until all 0x28000 bytes have been transferred
6. Start the CCFG Download
   a. Send the BLDR_CMD_DOWNLOAD_CRC command passing as input the startAddress=(0x4E020000), length=(2048), CRC=(calc_crc(ccfg_contents))
   b. wait for the ACK/NACK and then send the BLDR_CMD_GET_STATUS
   c. wait for the ACK/NACK and ensure the previous command was completed successfully with the BLDR_CMD_RET_SUCCESS value
7. Loop over the bytes of the CCFG contents and send the data to the ROM Bootloader
   a. Send the BLDR_CMD_SEND_DATA command, passing as input the next 252 bytes of the CCFG content.
   b. wait for the ACK/NACK and then send the BLDR_CMD_GET_STATUS
   c. wait for the ACK/NACK and ensure the previous command was completed successfully with the BLDR_CMD_RET_SUCCESS value
   d. Repeat steps 5a-5c until all 2048 bytes have been transferred
8. Reset the device either by pulling the RST pin externally or by sending the BLDR_CMD_RESET command.
   a. Keeping in mind that the triggerPin should now be inverted so that the bootcode/bootlaoder can freely pass execution onto the application this time around
9. DONE! The device will now bootup into the new flash content that has been programmed to it.

Chapter 10

Device Configuration

This chapter describes the device configuration areas. The factory configuration (FCFG), security configuration (SCFG), and customer configuration (CCFG) areas are located in flash. The FCFG is set by Texas Instruments during device production and contains device-specific trim values and configuration. The CCFG and SCFG must be set by the application and contains configuration parameters for the ROM boot code, device hardware, and device firmware.

10.1 Guidelines for securely configuring your device

The CC27xx device family has additional security features, many of which are only secure if configured correctly. The following guidelines should be followed in order to securely configure the device before deployment into the field.

10.1.1 Enabling and Configuring Secure Boot

- For more details on enabling Secure boot, refer to Chapter 11.
  - With Secure Boot enabled, the CCFG is no longer responsible for defining the app or bootloader vector definitions.
  - Even though a user-defined bootloader cannot be defined in the CCFG, it is recommended to explicitly disable the use of the ROM SBL via the ccfg.bootCfg.bldrEnabled field.
- With Secure Boot enabled, ROM will only transfer control to an application/SSB that has been authenticated.
- Decide on how many, if any at all, key updates are desired. Reducing this number will limit the number of future key updates your device can accept.
  - By default, 18 are allowed. See Chapter 11for more details.

10.1.2 Configure Debug Access

- Decide between forbidding debug access altogether and enabling public key authenticated debug access.
- If access should be forbidden, disable it via the ccfg.debugCfg.authorization field as well as the permissions (see permissions guidelines below) and then move on.
- If authenticated debug access is desired,
  1. Configure the ccfg.debugCfg.authorization accordingly.
  2. Configure the scfg.debugAuthCfg fields accordingly.
- The highest security quality is achieved by configuring the scfg.debugAuthCfg.challengeVector as follows:
  - lifetime = EPHERMERAL
  - deviceConst = MAC_CONST
- Decide which levels of authorization are desired.
  - Secure, Non-Secure and/or Non-Invasive only
  - If access to secure memory partitions is not required, then leave the scfg.debugAuthCfg.secureKey fields all 0x00s.

10.1.3 Configure Flash Protections

- Any sectors which should not be modified during runtime by either the SSB or the application should be write/erase-protected via the ccfg.flashProt.writeEraseProt fields.
- Any sectors which should not be readable during runtime by either the SSB or the application should be read-protected via the ccfg.flashProt.readProt fields.
- At a minimum, the CCFG and SCFG sectors should be write/erase-protected.
- If there is a desire to protect from chip erase and if chip erase is allowed (see Section 10.1.4), then configure ccfg.flashProt.chipEraseRetain accordingly.

10.1.4 Configure Device Permissions

Note

" ***x*** CFG" refers to the combination of both CCFG and SCFG.

- If the device should **not** have the capability to be returned to TI for failure analysis, then disable xcfg.permissions.allowReturnToFactory.
- Disable xcfg.permissions.allowToolsClientMode.
- Disable xcfg.permissions.allowChipErase and xcfg.misc.allowMainAppErase as is acceptable for the device.
- Disable xcfg.permissions.allowFlashProgram.

- If no debug access is required, disable xcfg.permissions.allowDebugPort.

10.1.5 Configure HSM FW Update Keys

Most crypto acceleration on the CC27XX device requires the HSM FW to function. See Chapter 8 for more details. By default, the SimpleLink™ Low Power F3 Software Development Kit (SDK) will provide HSM FW which has been encrypted and signed by Texas Instruments.

If it is desired to additionally require HSM FW to be signed by a customer private key, do the following below. See the SDK Quick Start Guide as well as the `hsmFwUpdate` example in the SDK for more details. Using those guides, scripts and examples, you will be walked through how to:

1. Create a RSA 3K private/public key pair.
2. Obtain the correct public key digest/hash and configure the SCFG accordingly.
3. Sign the default HSM FW image from the SDK with your private key.

When this is done, only HSM FW, which has been signed by your company's private key, will be accepted by the device.

10.1.6 Configure emSensor

Configure scfg.emSensorCfg = ENABLED.

10.2 Factory Configuration (FCFG)

The FCFG flash sector is written during TI manufacturing and is write and erase protected out of device boot.

FCFG contains the following:

- Unique device identifiers and MAC addresses
- Device configurations
- Device trims
- Default bootloader definition

This section lists only a subset of the defined fields within the FCFG flash sector.

Fields listed are either referenced by other chapters in the TRM or can be accessed by a non-TI part of an application executing in flash.

For a detailed list of fields please refer to the hw_fcfg.h file found in the driverlib part of the SimpleLink™ Low Power F3 Software Development Kit (SDK).

This C-header file holds a struct defining the complete layout of the FCFG flash sector.

Please note that minor updates of the FCFG field description (hw_fcfg.h) can occur as part of a Product SDK release.

The FCFG flash sector is split in sections as listed in the table below.

Table 10-1. FCFG Structure

FCFG hierarchy/field		Description
.deviceInfo		**Device information**
	.uuid[8]	64-bit device-unique UUID (non-sequential across parts)
	.bleAddr[6]	48-bit device-unique BLE address
	.macAddr[8]	64-bit device-unique IEEE MAC address
	.dieId[16]	128-bit die identifier (lot #, wafer #, die X/Y, date, etc).This ID is reported by the SACI_MISC_GET_DIE_ID SACI command.
	.partId	**Identification information specific to this orderable part number as reported in CFG-AP:PARTID**
		Random bit pattern to uniquely identify numeric TI part number
		Random bit pattern to uniquely identify package/memory variant suffix to TI part number
		Major revision for orderable part starting at 1
		Minor revision for orderable part starting at 0
.bootCfg		**Bootloader configuration**
	.pBldrVtor	Pointer to ISR vector table of bootloader (default: vector table for ROM serial bootloader)
	.bldrParam	Parameters passed to bootloader controlling bootloader behavior. For the ROM serial bootloader this controls the I/O pin used to trigger bootloader and which I/O pins are used for SPI/UART interfaces. (default: see Chapter 9)

10.3 Customer Configuration (CCFG)

The CCFG flash sector contains metainformation about or for the application:

- Boot configuration:
  - Where the initial vector table of the application is so that the application's entry function can be invoked and the stack pointer set. Application can change the vector table location later if needed.
  - Whether to invoke a bootloader and if so which bootloader and parameters to pass to the bootloader. See Chapter 9 for more information.
  - The location of user bootloader.
  - If Secure Boot is enabled, the CCFG based Boot Configuration (ccfg.bootCfg) will not be responsible for determining the next boot stage. See Chapter 9 and Chapter 11 for more details. Instead, the Section 10.4 section will be used.
- Permissions and hardware options:
  - Whether various boot operations or non-debug Serial Wire Debug (SWD) related features are allowed.
  - The ability to lock application out of certain hardware features or peripherals (e.g. to minimize harm that programming errors can do)
- Flash write and erase protections that apply to the application
- Hardware initialization to perform before first application instruction is run
- Debug permissions and optional authorization options
- User record

For regular software application development, the TI supported SysConfig tool is used to create the contents of the CCFG.

This section covers only the main parts of the CCFG. For a detailed view of the CCFG structure please refer to the hw_ccfg.h file provided by the driverlib part of the SimpleLink™ Low Power F3 Software Development Kit (SDK) or the SysConfig tool.

The C header file, hw_ccfg.h, provides a struct defining the complete CCFG layout.

Please note that minor updates of the CCFG field description (hw_ccfg.h) can occur as part of a Product SDK release.

The CCFG structure is split into sections, each having multiple fields. The table below presents a high level view of CCFG sections.

Most sections contain multiple fields. Only a subset of the fields are listed.

Table 10-2. CCFG Structure

CCFG hierarchy/field				Description
.bootCfg				**Contains function pointer that defines how to enter bootloader/application and also bootloader parameters.**
	.pBldrVtor			Pointer to user bootloader vector table
	.bldrParam			Parameter passed to bootloader
	.pAppVtor			Pointer to application VTOR table
	.crc32			CRC32 integrity checksum for CCFG
.hwOpts[2]				**Bitmask defining which peripherals/features and how much memory is accessible**
.permissions				**Device permission fields. This is maximally-restrictive combined with similar fields in FCFG and SCFG.**
	...			*Misc unused/reserved permissions*
	.allowReturnToFactory			Allow Return-To-Factory procedure by SACI. Refer to Section 9.1.6 for details. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID
	.allowToolsClientMode			Allow tools client mode to be enabled by SACI. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID
	.allowChipErase			Allow chip erase by SACI. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID
	.allowFlashProgram			Allow flash program by SACI. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID
	.allowFlashVerify			Allow flash verify by SACI. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID
	...			*Misc unused/reserved permissions*
	.allowDebugPort			Allow enabling of SWD port. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID

Table 10-2. CCFG Structure (continued)

CCFG hierarchy/field				Description
.misc				**Misc. boot-related fields**
	.saciTimeoutExp			Configures the SACI timeout when there is a bootloader or application to boot into: SACI timeout is infinite when 0, else (2^saciTimeoutExp)*64 ms. (default: 0x4 = 1s)
	.allowMainAppErase			Allow main app erase by SACI. Defined options are: • CCFG_PERMISSION_ALLOW (default) • CCFG_PERMISSION_FORBID
	.saciTimeoutOverride			Determines if SACI timeout defined in FCFG is overridden by SACI timeout defined in CCFG
.flashProt				**Flash write/erase protection fields. Protection is applied before entering bootloader/ application during boot**
	.writeEraseProt			**Write/erase protection fields**
		.mainSectors0_31		Bitmask for write/erase protection of individual sectors in sector range [0, 31]. 0 = protected (default: 1)
		.mainSectors32_255		Bitmask for write/erase protection of groups of 8 sectors. Bit i protects sectors [32+8i, 39+8i]. 0 = protected (default: 1)
		.mainSectors256_511		Bitmask for write/erase protection of groups of 8 sectors. Bit i protects sectors [256+8i, 263+8i]. 0 = protected (default: 1)
				Bitmasks for write/erase protection of auxilliary sectors
		.auxSectors	.ccfgSector	Protect CCFG sector 0 = protected (default: 1)
			.fcfgSector	Protect FCFG sector 0 = protected (default: 1)
			.scfgSector	Protect SCFG sector 0 = protected (default: 0)
			.vlogSector	
			...	*Misc internal flash sector protections*
	.readProt		.mainSectors	
			.ccfgSector	
	.chipErase		.mainSectors	
.hwInitCopyList[]				Remaining hardware trims applied during boot. Stored in a flexible copy list format.
.userRecord				User record (programmable also through separate SACI command).

Table 10-2. CCFG Structure (continued)

CCFG hierarchy/field				Description
.debugCfg				Bootloader configuration
	.authorization			Debug authorization requirements. Defined options are: • CCFG_DBGAUTH_REQAUTH • CCFG_DBGAUTH_DBGOPEN (default) • CCFG_DBGAUTH_ONLY_NON_INVASIVE • CCFG_DBGAUTH_DBGFORBID
	.res0[43]			Reserved
	.crc32			Integrity check of debugCfg section. Any integrity check error of debugCfg section is interpreted as debugCfg.authorization=CCFG_DBGAUTH_DBGFORBID

10.4 Security Configuration (SCFG)

The SCFG flash sector contains security related metainformation about or for the application:

- HSM FW Update Configuration
  - The HSM FW update process can optionally include verification of a customer based key.
  - This allows the device to require any given HSM FW update to be signed by the customer prior to the device accepting the update.
- Secure Debug Authorization Configuration
  - Extended debug configuration when ccfg.debugCfg.authorization is configured to require authorization.
  - Three debug authorization levels are supported (Secure, Non-Secure, Non-Invasive Only)
    - By configuring and authorizing debug access with the **Secure** key, you will have access to all three authorization levels.
    - By configuring and authorizing debug access with the **Non-Secure**, you will only have access to the bottom two authorization levels.
  - Configuration of the Challenge Vector can allow a tradeoff between debug authorization complexity and security.
- Secure Boot Configuration
  - Secure Boot flash layout
    - Define the primary and secondary application slots so that Secure Boot knows how to properly verify and update the images within those slots.
    - Define the SSB slot so that Secure Boot knows how to properly verify and update the image.
  - Secure Boot Policy
    - Enable secure boot and specify the authentication method to be used.
      - If *Signature* authentication is chosen the next boot stages will be verified upon every boot up.
      - If *Hash Lock* authentication is chosen, the full signature verification will only occur on the very first boot of a given image. From that point on there will be a hash of the image to allow for much quicker subsequent bootups.
- Device Permissions
  - A similar set of device permissions as compared to the FCFG and SCFG sector
- Key Ring Configuration

  Secure Boot allows to provision some keys and update those keys in the field at a later time.

For regular software application development, the TI supported SysConfig tool is used to create the contents of the SCFG.

This section covers only the main parts of the SCFG. For a detailed view of the SCFG structure, please refer to the hw_scfg.h file provided by the driverlib part of the SimpleLink™ Low Power F3 Software Development Kit (SDK) or the SysConfig tool.

The C header file, hw_scfg.h, provides a struct defining the complete SCFG layout.

Note

Minor updates of the SCFG field descriptions (hw_scfg.h) can occur as part of a Product SDK release.

The SCFG is split into sections, each having multiple fields. The table below presents a high level view of SCFG sections. Most sections contain multiple fields. Only a subset of the fields are listed.

Table 10-3. SCFG Structure

SCFG hierarchy/field			Description
.hsmCfg			**Configures the optional signature verification of the HSM FW**
	.publicKeyHash		Specially formatted SHA-256 hash of the RSA 3K public key. Leave all 0xFF's to disable the additional public key verification. *It is recommended to use the example script and documentation in the Product SDK to ensure correct generation and population of this field.*

Table 10-3. SCFG Structure (continued)

SCFG hierarchy/field			Description
.debugAuthCfg			**Secure debug authorization configuration** *These fields are only relevant if the CCFG is configured with CCFG_DBGAUTH_REQAUTH.*
	.secureKey		**Configuration of the secure key**
		.keyId	8B customer defined Key ID used for lookup of the key in the customer database
		.publicKeyHash	SHA-256 hash of the debug key *Key type depends on the configuration of scfg.secBootCfg.policyCfg.authAlgorithm.*
	.nonSecureKey		**Configuration of the non secure key**
		.keyId	8B customer defined Key ID used for lookup of the key in the customer database
		.publicKeyHash	SHA-256 hash of the debug key *Key type depends on the configuration of scfg.secBootCfg.policyCfg.authAlgorithm.*
	.challengeVector		**Configuration of the secure debug challenge vector**
		.lifetime	Allows for more/less security at the cost of complexity Defined options are: • SCFG_DBGAUTH_EPHEMERAL_LIFETIME (most secure) • SCFG_DBGAUTH_ENDLESS_LIFETIME (least secure)
		.deviceConst	Allows for more/less security at the cost of complexity Defined options are: • SCFG_DBGAUTH_DEVICE_MAC_CONST (most secure) • SCFG_DBGAUTH_ZERO_CONST (least secure)

Table 10-3. SCFG Structure (continued)

SCFG hierarchy/field			Description
.flashCfg	.flashLayout		**Secure Boot Flash configuration** *These fields are only relevant if Secure Boot is enabled. See hw_scfg.h for more details on the slot.*
		.primaryAppSlots[2]	Two *primary* application slots
		.secondaryAppSlots[2]	Two *secondary* application slots
		.bldrSlot	A single slot to define the SSB
	...		*Misc unused/reserved*

Table 10-3. SCFG Structure (continued)

SCFG hierarchy/field			Description
.secBootCfg			**Secure Boot configuration**
	.policyCfg		**Secure Boot policy configuration**
		.authMethod	Enable Secure Boot and decide which authentication method will be used. Defined options are: • SCFG_POLICY_NO_AUTH (disable secure boot entirely) • SCFG_POLICY_SIGNATURE • SCFG_POLICY_HASH_LOCK
		.authAlgorithm	Decide which authentication algorithm will be used if secure boot is enabled. Defined options are: • SCFG_POLICY_ALG_RSA_3K_SHA256 • SCFG_POLICY_ALG_ECDSA_P256_SHA256 • SCFG_POLICY_ALG_ECDSA_P521_SHA512
		.mode	Decide which secure boot update mode will be used if secure boot is enabled. Defined options are: • SCFG_POLICY_OVRWRT • SCFG_POLICY_XIP_REVERT_ENABLED • SCFG_POLICY_XIP_REVERT_DISABLED
			Secure Boot *key* update key configuration
	.keyUpdateKeyHash		SHA-256 hash of the key update key *Key type depends on the configuration of scfg.secBootCfg.policyCfg.authAlgorithm.*

Table 10-3. SCFG Structure (continued)

SCFG hierarchy/field			Description
.permissions			**Device permission fields. This is maximally restrictive combined with similar fields in FCFG and CCFG.**
	...		*Misc unused/reserved permissions*
	.allowReturnToFactory		Allow Return-To-Factory procedure by SACI. Refer to Section 9.1.6for details. Defined options are: • SCFG_PERMISSION_ALLOW (default) • SCFG_PERMISSION_FORBID
	.allowToolsClientMode		Allow tools client mode to be enabled by SACI. Defined options are: • SCFG_PERMISSION_ALLOW (default) • SCFG_PERMISSION_FORBID
	.allowChipErase		Allow chip erase by SACI Defined options are: • SCFG_PERMISSION_ALLOW (default) • SCFG_PERMISSION_FORBID
	.allowFlashProgram		Allow flash program by SACI Defined options are: • SCFG_PERMISSION_ALLOW (default) • SCFG_PERMISSION_FORBID
	.allowFlashVerify		Allow flash verify by SACI Defined options are: • SCFG_PERMISSION_ALLOW (default) • SCFG_PERMISSION_FORBID
	...		*Misc unused/reserved permissions*
	.allowDebugPort		Allow enabling of SWD port. Defined options are: • SCFG_PERMISSION_ALLOW (default) • SCFG_PERMISSION_FORBID
	.allowMainAppErase		Allow main app erase by SACI. Defined options are: • SCFG_PERMISSION_ALLOW (default)

Table 10-3. SCFG Structure (continued)

SCFG hierarchy/field			Description
.emSensorCfg			HW EM sensor configuration Defined options are: • SCFG_EMSENSOR_ENABLE (default) • SCFG_EMSENSOR_DISABLE
...			*Misc fields*
.keyRingCfg			**Secure boot key ring configuration**
	.keyEntries[18]		A max of 18 keys can be stored in this key ring.*See Section 11.4.4 for more details.*

Chapter 11

Secure Boot

This chapter describes the functionality of the ROM Secure Boot module.

11.1 Secure Boot

Secure boot is a verification mechanism that ensures that the firmware to be booted is trusted, in that the code to be executed originates from a known source. Therefore, it prevents unauthorized firmware from booting.

The System ROM is the root of trust. The ROM Secure Boot verifies that the next boot stage, either an Application (App 0 or App 1) or a Secondary Secure Bootloader (SSB), is trusted. In this context, the next boot stage is trusted if it complies with the properties of integrity (hash) and authenticity (signature).

In general, the following are the steps required to enable Secure Boot in the system and generate compatible images.

- Generate private keys of the same type as configured in the Authentication Algorithm for:
  - Key updates
  - App updates (only necessary if Secure Boot will boot Application images)
  - SSB updates (only required if Secure Boot will boot a Secondary Secure Bootloader)
- Configure SCFG fields as desired:
  - Application and/or secondary secure bootloader slots
  - Authentication method, algorithm and update mode
  - Key Update Key Hash
  - Initial key ring entries for application and/or secondary secure bootloader
  - Boot Seed

Note that SCFG needs to be programmed only once. After that additional images can be programmed separately without the need to program SCFG again. SCFG only needs to be reprogrammed if a change in the security configuration needs to be made.

Refer to the Secure Boot example project in the SDK to learn how to perform the steps described above using the tools provided in the Code Composer IDE.

11.2 Execution Flow

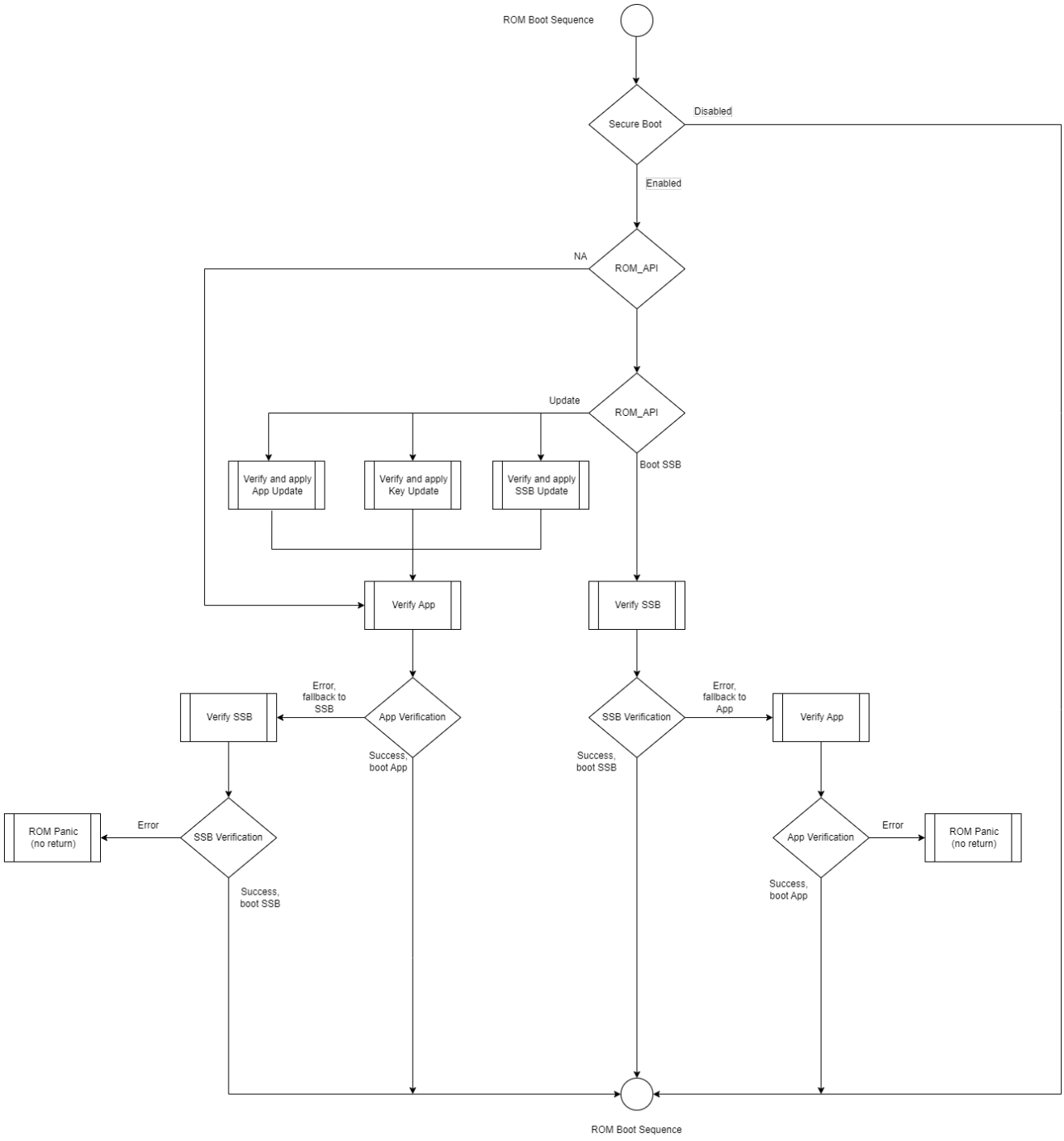

Figure 11-1. Secure Boot Flow

In the Execution Flow depicted above, the ROM Boot Sequence will invoke Secure Boot only if enabled. In general, Secure Boot is configured in SCFG (Secure Configuration). For Secure Boot to be considered enabled, field **scfg.secBootCfg.authMethod** must be set to either SCFG_POLICY_SIGNATURE or SCFG_POLICY_HASH_LOCK. If **scfg.secBootCfg.authMethod** is set to SCFG_POLICY_NO_AUTH, Secure Boot is considered disabled.

Secure Boot will return the target address to transfer control to the ROM Boot Sequence, unless it is determined that there is no target to boot, in which case the system will enter ROM Panic.

For Secure Boot to boot or update a given target, it is required that the verification and antirollback checks are successful. Otherwise, the target image will be rejected.

11.3 ROM API

The ROM API is the mechanism in which an Application (or an SSB) communicates with System ROM to request commands to Secure Boot. Similarly, Secure Boot will use the ROM API to communicate to the Application (or SSB) the status of the operation that was requested.

In general, the target being executed needs to set the ID and Sector (using the HAPI described below), and then issue a device reset. ROM Secure Boot will then take control and perform the requested actions.

11.3.1 HAPI (Hardware API)

<table>
<tr><th>HAPI</th><th>Usage</th></tr>
<tr><td>HapiSbSetUpdateImageAddress(address)</td><td>Used to specify the sector address in which update images for SSB or Key are located. The provided address value must be sector aligned and within device on-chip flash range.</td></tr>
<tr><td>HapiSbSetId(id)</td><td>Used to specify the request ID for ROM Secure Boot. The following is a description of the meaning of each request ID:
<table>
<tr><th>ID [1]</th><th>ID [0]</th><th>Meaning</th></tr>
<tr><td>0</td><td>0</td><td>NA (No Action). Target to boot is Application.</td></tr>
<tr><td>0</td><td>1</td><td>Section 8.7Update</td></tr>
<tr><td>1</td><td>0</td><td>Target to boot is SSB.</td></tr>
<tr><td>1</td><td>1</td><td>Update, either Application, SSB, or Key.</td></tr>
</table>
</td></tr>
<tr><td>HapiSbGetUpdateImageAddress()</td><td>Returns the current address that was requested using HapiSbSetUpdateImageAddress(address).</td></tr>
</table>

<table>
<tr><td>HapiSbGetStatus()</td><td>Return the current status for the requested operation. The following is a description of the meaning of each status code:
<table>
<tr><th>Status [2]</th><th>Status [1]</th><th>Status [0]</th><th>Meaning</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Selected target booted successfully.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Update success.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Fault Injection Attack Detected.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Image Rejected.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Image Verification Failure.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Update Failure (generically).</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Invalid Device Configuration. Requires device Chip Erase and re-programming to recover.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>HSM Boot Failure. Requires device Chip Erase and re-programming to recover.</td></tr>
</table></td></tr>
<tr><td>HapiSbGetId()</td><td>Returns the ID that was requested using HapiSbSetId(id).</td></tr>
</table>

11.3.2 Registers

The following is a description of the registers used for communication between System ROM and Application (or SSB). The HAPI described above act upon these registers.

Note:

- The state of these registers is persistent across device reset.
- The state of these resisters is not persistent across a power cycle.
- Secure Boot will clear Sector and ID fields after reading them to perform the requested operation.

- Secure Boot will set the Status field, but the Application (or SSB) is responsible to clear it.

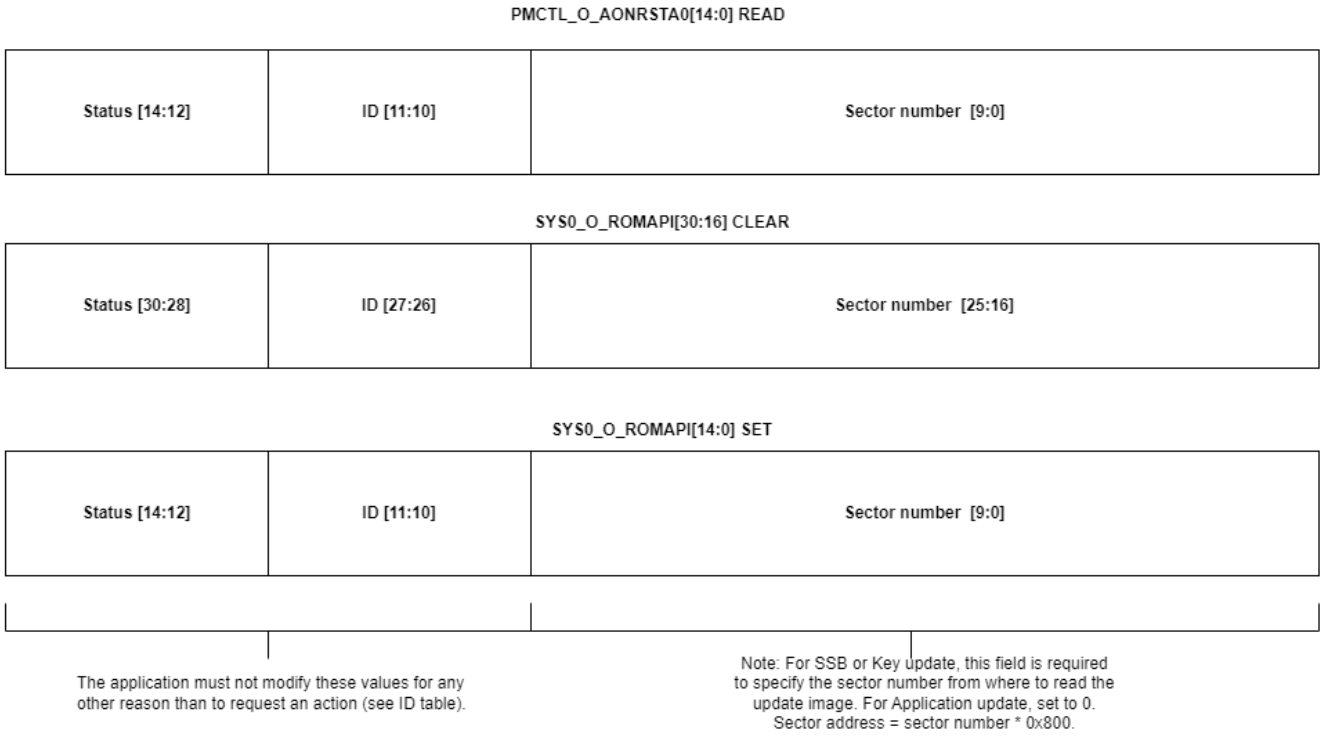

Figure 11-2. Secure Boot Related Registers

11.4 Configuration

Secure Boot is configured by setting specific fields in the SCFG (Secure Configuration) memory region. The sections below describe these fields in detail. Refer to the SCFG configuration chapter for additional information.

11.4.1 Slot Configuration

Secure Boot allows the configuration of Application and Secondary Secure Bootloader slots. Each slot is defined by its start address and length. The start address must be aligned to a sector boundary (0x800), its length must be a multiple of sector size (0x800), and the region defined by the start address and length must be within physical flash memory space. If these conditions are not met, the slot will be considered undefined.

- For Secondary Secure Bootloader, define scfg.flashCfg.flashLayout.bldrSlot.addr and scfg.flashCfg.flashLayout.bldrSlot.len
- For Application, define the following as necessary:
  - scfg.flashCfg.flashLayout.primaryAppSlots[0].start and scfg.flashCfg.flashLayout.primaryAppSlots[0].len
  - scfg.flashCfg.flashLayout.primaryAppSlots[1].start and scfg.flashCfg.flashLayout.primaryAppSlots[1].len
  - scfg.flashCfg.flashLayout.secondaryAppSlots[0].start and scfg.flashCfg.flashLayout.secondaryAppSlots[0].len
  - scfg.flashCfg.flashLayout.secondaryAppSlots[1].start and scfg.flashCfg.flashLayout.secondaryAppSlots[1].len

In addition, if it is desired not to configure a given slot, set the corresponding slot address = SCFG_SLOT_ADDR_UNDEF and length as SCFG_SLOT_LEN_UNDEF.

The following sections explain how these different application slots are used depending on the chosen Update Mode.

11.4.2 Policy

The Secure Boot Policy configuration consists of the following:

- Authentication Method
- Authentication Algorithm
- Mode

11.4.2.1 Authentication Method

Secure Boot supports the following 3 authentication methods:

- No Authentication
  - To configure this option, set scfg.secBootCfg.policyCfg.authMethod = SCFG_POLICY_NO_AUTH
  - Note that under this option, Secure Boot is disabled, so no image verification will occur. Refer to the Execution Flow diagram above, in which System ROM will transfer control to the specified address in CCFG instead. Refer to the CCFG configuration chapter for additional details.
- Signature
  - To configure this option, set scfg.secBootCfg.policyCfg.authMethod = SCFG_POLICY_SIGNATURE
  - In this mode, Secure Boot will perform signature verification of the target image (Application or Secondary Secure Bootloader, depending on the request specified when invoking HapiSbSetId()) each time the device boots.
- Hash Lock
  - To configure this option, set scfg.secBootCfg.policyCfg.authMethod = SCFG_POLICY_HASH_LOCK
  - In this mode, Secure Boot will perform signature verification only once when the target image is to be executed for the first time, and store a sha256 hash of the entire target image in the VLOG region. Refer to Antirollback section for more details.
  - In subsequent device boots, Secure Boot will compute a sha256 hash of the target image and compare it with the stored sha256 hash in the VLOG region. If there is a match between the hashes, Secure Boot will allow the target image to be booted.
  - The advantage of this option is that System ROM will transfer control to the target image in less time than in Signature mode, as performing a sha256 hash is significantly faster than performing a signature verification operation.

11.4.2.2 Authentication Algorithm

Secure Boot supports 3 types of signature algorithms:

- RSA 3K PKCS
  - To configure this option, set scfg.secBootCfg.policyCfg.authAlgorithm = SCFG_POLICY_ALG_RSA_3K_SHA256
- ECDSA P256
  - To configure this option, set scfg.secBootCfg.policyCfg.authAlgorithm = SCFG_POLICY_ALG_ECDSA_P256_SHA256
- ECDSA P521
  - To configure this option, set scfg.secBootCfg.policyCfgauthAlgorithm = SCFG_POLICY_ALG_ECDSA_P521_SHA512

The signature for the image is located at the signature TLV (see image format in following sections).

Refer to the Secure Boot example in the SDK for instructions on private key generation.

11.4.2.3 Update Mode

Secure Boot supports the following update modes for images of type App 0 or App 1:

- Overwrite
  - To configure this option, set scfg.secBootCfg.policyCfg.mode = SCFG_POLICY_OVRWRT
  - It requires that at least scfg.flashCfg.flashLayout.primaryAppSlots[0] is defined. Otherwise Secure Boot will fallback to SSB (if valid).
  - If scfg.flashCfg.flashLayout.secondaryAppSlots[1] is defined, it requires that scfg.flashCfg.flashLayout.primaryAppSlots[1] is defined.
  - If scfg.flashCfg.flashLayout.primaryAppSlots[1] is defined, Secure Boot will verify both scfg.flashCfg.flashLayout.primaryAppSlots[0] and scfg.flashCfg.flashLayout.primaryAppSlots[1] before booting the image stored in scfg.flashCfg.flashLayout.primaryAppSlots[0].
- XIP Revert Enabled
  - To configure this option, set scfg.secBootCfg.policyCfg.mode = SCFG_POLICY_XIP_REVERT_ENABLED
  - It requires that both scfg.flashCfg.flashLayout.primaryAppSlots[0] and scfg.flashCfg.flashLayout.secondaryAppSlots[0] are defined. Otherwise Secure Boot will fallback to SSB (if valid).
- XIP Revert Disabled
  - To configure this option, set scfg.secBootCfg.policyCfg.mode = SCFG_POLICY_XIP_REVERT_DISABLED
  - It requires that both scfg.flashCfg.flashLayout.primaryAppSlots[0] and scfg.flashCfg.flashLayout.secondaryAppSlots[0] are defined. Otherwise Secure Boot will fallback to SSB (if valid).

11.4.2.3.1 Overwrite

In overwrite update mode, Secure Boot will overwrite the contents of scfg.flashCfg.flashLayout.primaryAppSlots[n] with the contents of scfg.flashCfg.flashLayout.secondaryAppSlots[n]. When TrustZone is enabled, that is, if scfg.flashCfg.flashLayout.primaryAppSlots[0] and scfg.flashCfg.flashLayout.primaryAppSlots[1] are defined, Secure Boot allows the update of either the Secure Image, the Non-Secure Image, or both.

The following illustrates the update pattern for Overwrite mode when TrustZone is disabled.

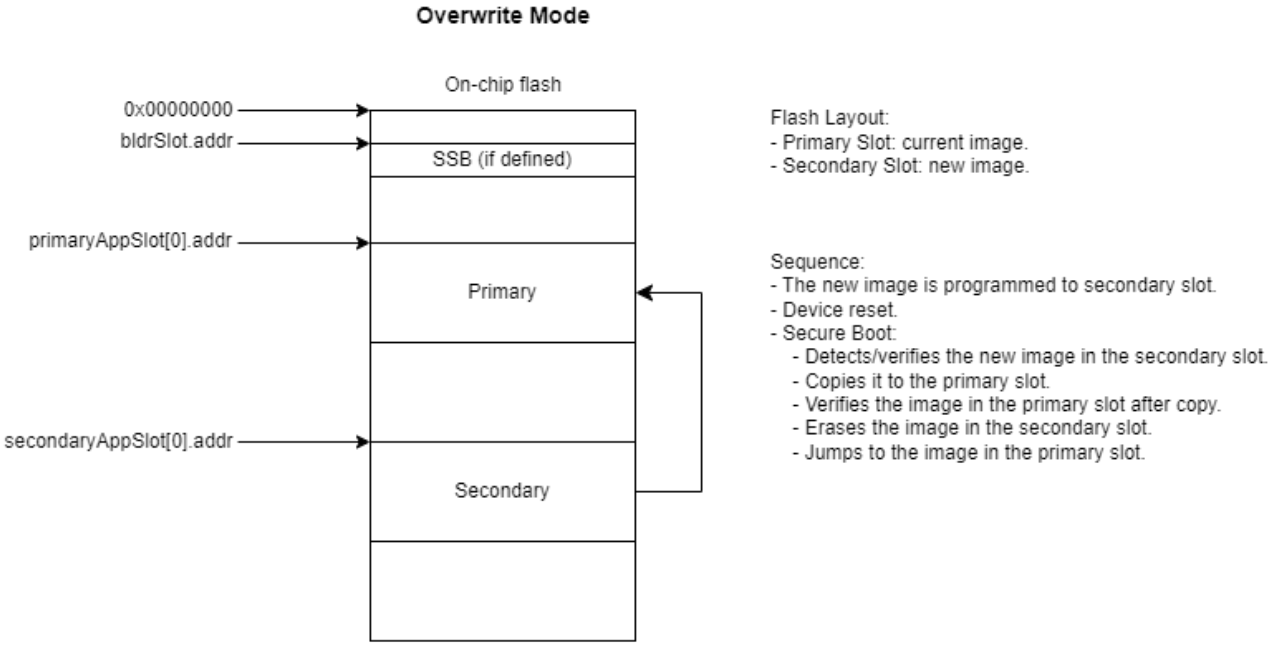

Figure 11-3. Overwrite update mode with TrustZone disabled

The following illustrates the update pattern for Overwrite mode when TrustZone is enabled.

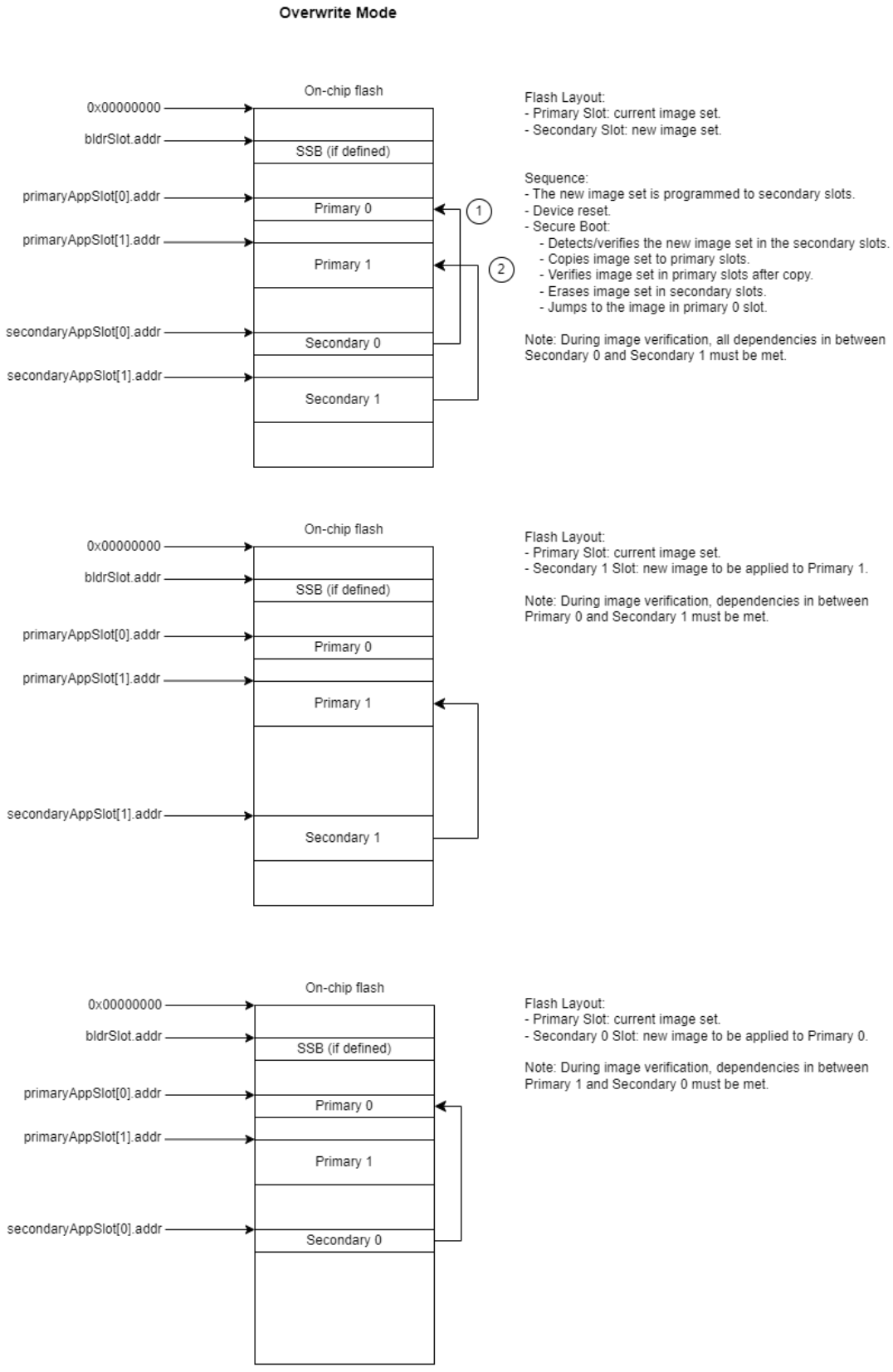

Figure 11-4. Overwrite update mode with TrustZone enabled

11.4.2.3.2 XIP Revert Enabled/Disabled

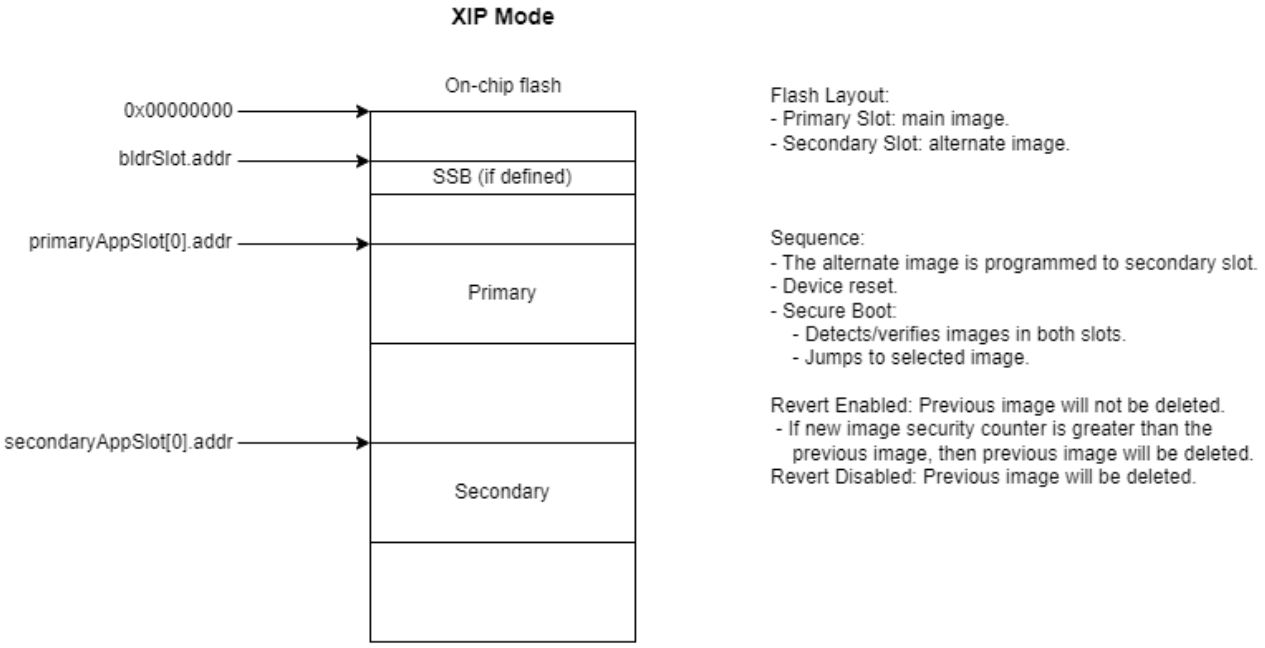

Figure 11-5. XIP Update Mode

Note:

- XIP Revert Enabled is not allowed if TrustZone is enabled.
- XIP Revert Disabled is not allowed if TrustZone is enabled.
- Hash Lock is not supported in XIP Revert Enabled mode.

11.4.3 Key Update Key Hash

Field scfg.secBootCfg.keyUpdateKeyHash must be set with a sha256 of the public key used to verify Key Update images.

11.4.4 Key Ring

This region is located at the last 792 bytes of the SCFG memory region. It is used to store up to 18 key hashes of either App or SSB type. In this context, a Key Ring of type App is applicable for App 0 and App 1 image types. It is used to validate that the Public Key used to verify the signature of a given target, either App or SSB, is in fact the authorized key. If an image public key does not match the active key of the corresponding image type, the image will be rejected.

If a given private key, either to sign App or SSB, gets compromised, a new key of that given type can be added to the system. The Key Update section describes how new keys can be added to the ring.

The following describes the binary structure of each entry.

```
// Key ring config, length 792B
struct {
   // Key Entries
   #define SCFG_KEY_HASH_RING_NUM 18U

   struct keyRingEntry {
       // SHA-256 hash a public key (key type depends on secBootCfg.policyCfg.authAlgorithm)
       uint8_t keyHash[32];

       // ID corresponding to type of keyEntry
       uint32_t type;
            #define SCFG_KEY_ENTRY_TYPE_APP 0x3F68A5A5U
```

```
            #define SCFG_KEY_ENTRY_TYPE_BLDR 0x6C715A5AU

       // CRC across keyHash through type
       uint32_t crc32;

       // Status is intentionally left out of crc32 coverage
       // A value other than SCFG_KEY_ENTRY_STATUS_ACTIVE is considered inactive
       uint32_t status;
            #define SCFG_KEY_ENTRY_STATUS_ACTIVE 0x59183d3bU
   } keyEntries[SCFG_KEY_HASH_RING_NUM];
} keyRingCfg;
```

Once the Key Ring is full, no more Key Updates will be allowed. A chip erase will always reset the state of the key ring.

11.4.5 Boot Seed

Boot Seed represents a unique value that gets generated at boot time. This is typically used by attestation services implemented in the Secondary Secure Bootloader.

This feature gets enabled by writing a value to scfg.bootSeedOffset in the range from [0, 13], which represents the offset from RAM base, in multiples of 16-byte blocks, up to an offset of 208 bytes (13 16-byte blocks).

To disable this feature, set scfg.bootSeedOffset = 0xff.

If Boot Seed is enabled, a Concise Binary Object Representation (CBOR) header 0xA1 0x3A 0x00 0x01 0x24 0xFB 0x58 0x20 (8 bytes) will be written to the RAM location encoded by scfg.bootSeedOffset, followed by 32 random bytes.

If Boot Seed is enabled, care must be taken so that the target linker file generates code that does not use the RAM region used by Boot Seed. Otherwise, when the target runs, the contents of the Boot Seed RAM region will be overwritten.

11.5 Generic Image Format

In general, Secure Boot compatible images must adhere to the following format:

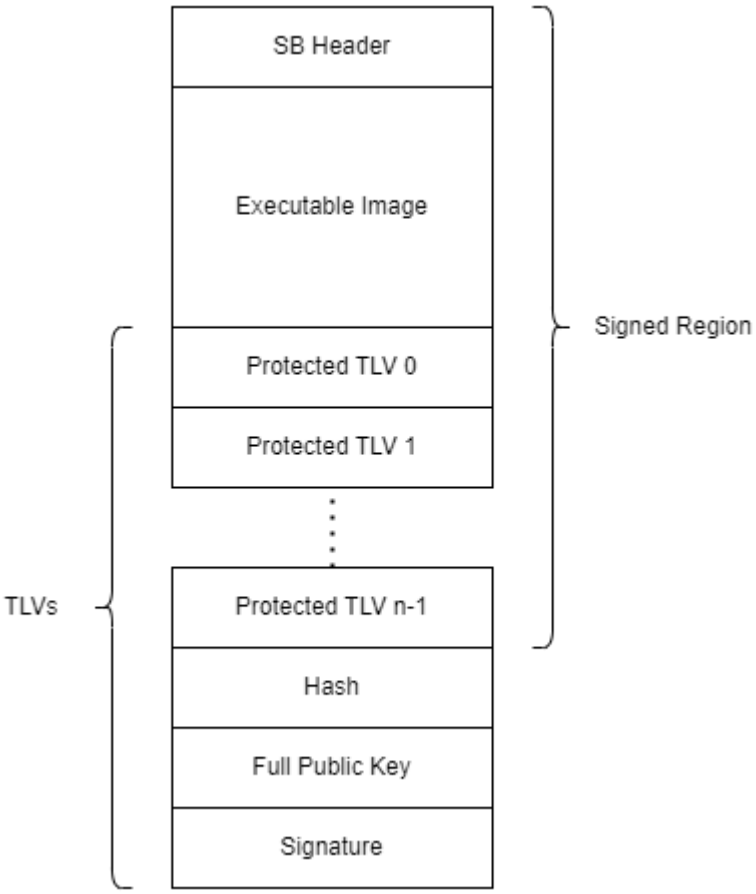

Figure 11-6. Secure Boot Image Format

Note:

- SB: Secure Boot Header.
- TLV: Type Length Value.

Tools in the SDK are provided to create Secure Boot compatible images. Refer to the Secure Boot example in the SDK for detailed instructions.

To get more details about the image header and TLV fields, refer to MCUBoot Image Format.

11.6 Application Update

To trigger an application, follow these steps:

- Program the update image in the corresponding slot:
  - For Overwrite mode:
    - App 0 update images must be flashed to scfg.flashCfg.flashLayout.secondaryAppSlots[0].
    - App 1 update images must be flashed to scfg.flashCfg.flashLayout.secondaryAppSlots[1].
  - For XIP mode:
    - App 0 update images must be flashed to the slot these have been linked for.
- Call HapiSbSetUpdateImageAddress(0)

- Call HapiSbSetId(3)
- Reset the device

When the system is being provisioned for the first time, the target image can be programmed directly to the slot in which it will be executed.

Application images must be signed with the key that corresponds to the App active key in the Key Ring.

Refer to the Secure Boot SDK example on instructions on how to create Application update images.

11.6.1 Image Format

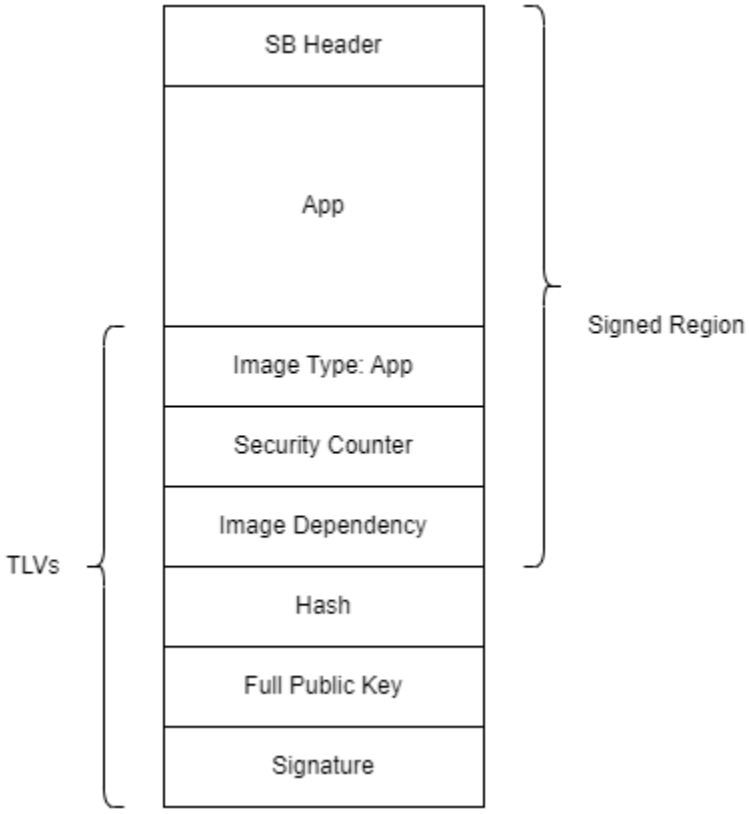

Figure 11-7.

Image type is a protected TLV with type 0xa0 and a value of 0xabb0c380 for App 0.

Image type is a protected TLV with type 0xa0 and a value of 0xabb11193 for App 1.

An incorrectly formatted image will result in an Image Rejected status.

App 0

- In Overwrite Mode:
  - Will be executed from scfg.flashCfg.flashLayout.primaryAppSlots[0], so it must be linked for this address space.
  - Updates will be taken from scfg.flashCfg.flashLayout.secondaryAppSlots[0], so it must be linked for the scfg.flashCfg.flashLayout.primaryAppSlots[0] address space.
- In any XIP mode:
  - Will be executed from either scfg.flashCfg.flashLayout.primaryAppSlots[0] or scfg.flashCfg.flashLayout.secondaryAppSlots[0], so the image must be linked for the proper slot.

App 1

- Only Overwrite mode is allowed.
- Will be executed from scfg.flashCfg.flashLayout.primaryAppSlots[1], so it must be linked for this address space.
- Updates will be taken from scfg.flashCfg.flashLayout.secondaryAppSlots[1], so it must be linked for the scfg.flashCfg.flashLayout.primaryAppSlots[1] address space.

11.7 Secondary Secure Bootloader Update

To trigger a Secondary Secure Bootloader Update, follow these steps:

- Set the address in which the update image is located by calling HapiSbSetUpdateImageAddress(address)
- Call HapiSbSetId(3)
- Reset the device

When the system is being provisioned for the first time, the target image can be programmed directly to the slot in which it will be executed.

Secondary Secure Bootloader images must be signed with the key that corresponds to the SSB active key in the Key Ring.

Refer to the Secure Boot SDK example on instructions on how to create Secondary Secure Bootloader update images.

11.7.1 Image Format

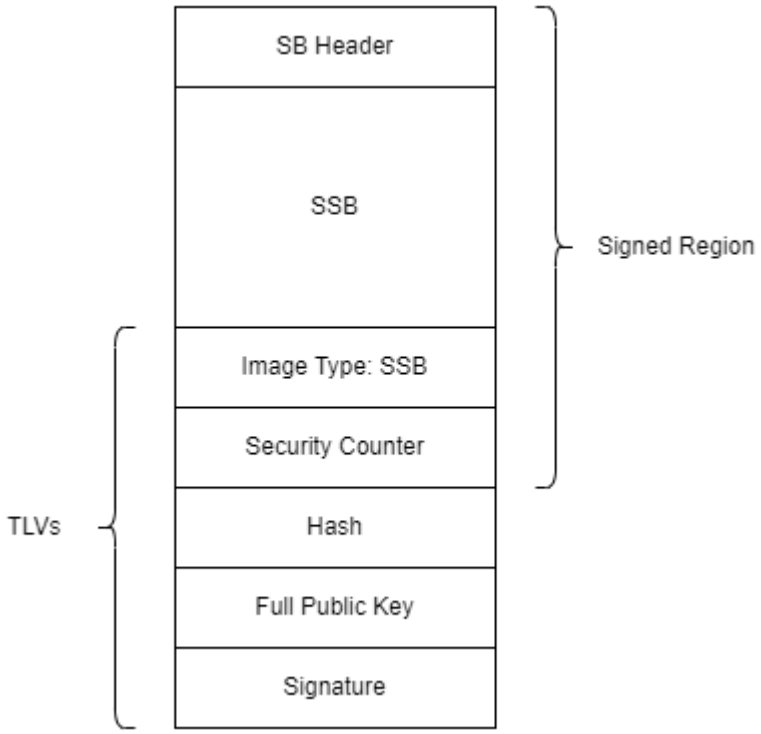

Figure 11-8.

Image type is a protected TLV with type 0xa0 and a value of 0x53c0b001.

An incorrectly formatted image will result in an Image Rejected status.

- Will be executed from scfg.flashCfg.flashLayout.bldrSlot, so it must be linked for this address space.
- Updates will be taken from the address that results from 0x800 * PMCTL_O_AONRSTA0[9:0]. See ROM API Registers for reference.

11.7.2 Update Pattern

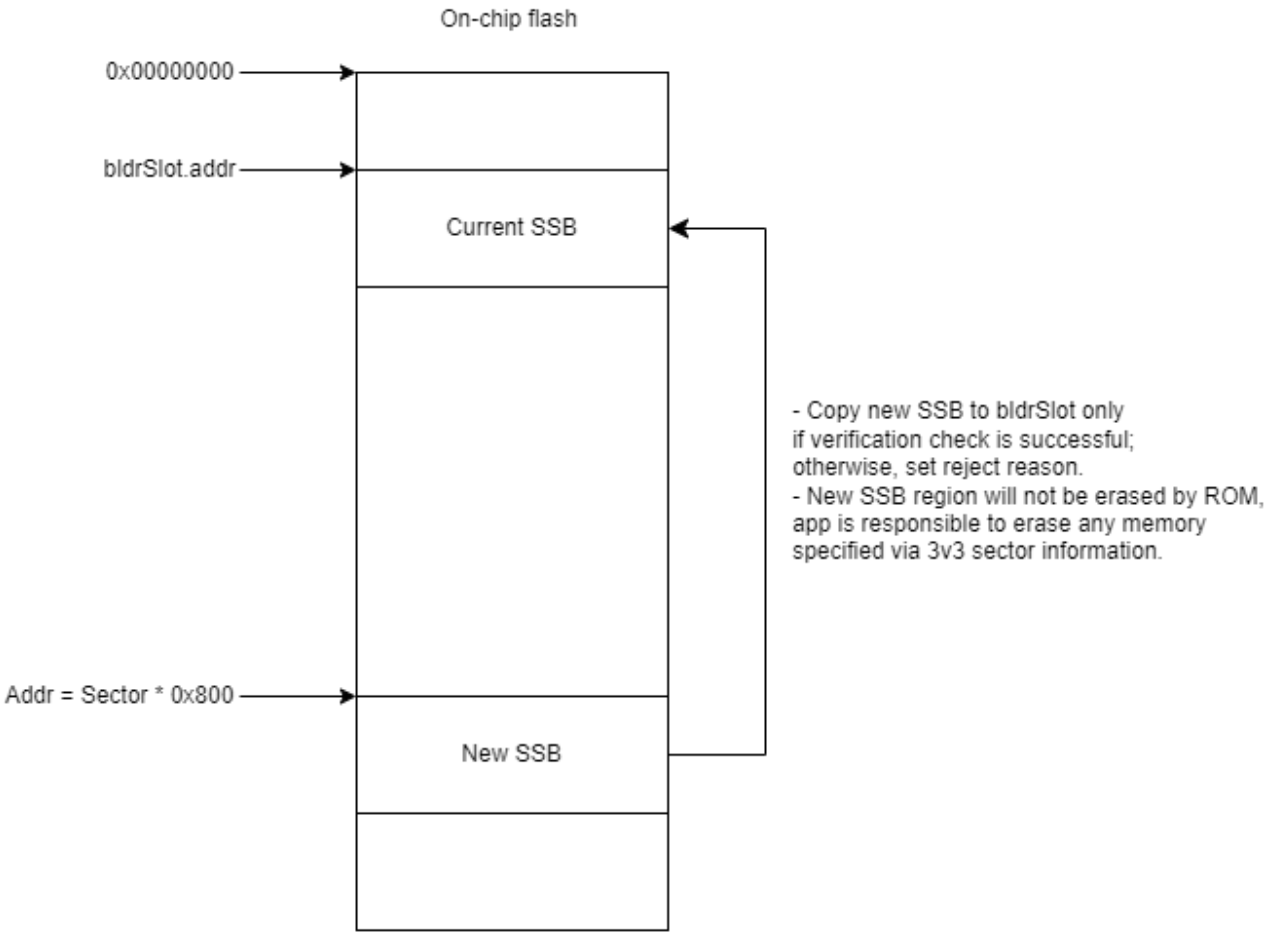

Figure 11-9.

11.8 Key Update

This is the process in which new keys for either SSB or Application can be added to the Key Ring in SCFG. When a new key is added, there will be 2 active keys of a given type in the Key Ring until a target is verified with the new key.

At that point, the old key will be made invalid and no more updates for a given target with the old key will be accepted.

To trigger a Key Update, follow these steps:

- Set the address in which the Key Update image is located by calling HapiSbSetUpdateImageAddress(address)
- Call HapiSbSetId(3)
- Reset the device

Old keys cannot be added again, as Secure Boot keeps a record of old keys in the Key Ring.

Key Update images must be signed with the key that corresponds to the key specified by scfg.secBootCfg.keyUpdateKeyHash.

Refer to the Secure Boot SDK example on instructions on how to create Key Update images.

11.8.1 Image Format

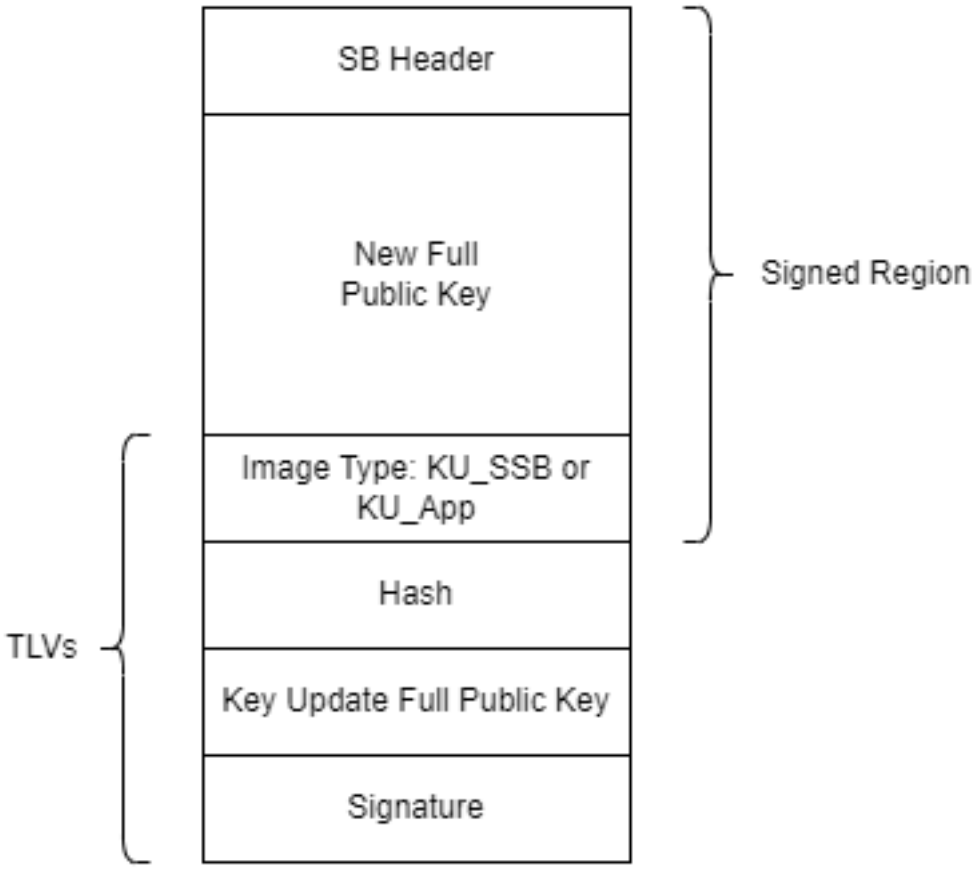

Figure 11-10.

Image type is a protected TLV with type 0xa0 and a value of 0xc3100bda for Application Key Update images, and 0xc310055b for Secondary Secure Bootloader Key Update images.

An incorrectly formatted image will result in an Image Rejected status.

- Updates will be taken from the address that results from 0x800 * PMCTL_O_AONRSTA0[9:0]. See ROM API Registers for reference.

11.9 Antirollback

This feature allows Secure Boot to avoid accepting updates that do not meet minimum version and security counter values for SSB, App 0 or App 1.

For updates, the following conditions must be met:

- The major/minor version of the update image must be greater than the version of the current image.
- The security counter of the update image must be greater than or equal than the security counter of the current image.

Secure Boot will always perform the antirollback check to determine if a target can be booted.

11.10 Version Log (VLOG)

The Version Log is a dedicated area of non-main flash memory of 0x800 (2048) bytes in size, used to store records for security counter, version and hash lock, for either SSB, App 0 or App1 image types, independently.

The first 8 bytes of VLOG are reserved to store the Crypto Officer ID for the HSM. Therefore, only 0x7f8 (2040) bytes are available to store VLOG records.

The Version Log area of memory is **only** accessible to System ROM. This allows Secure Boot to reject update images that do not meet the antirollback conditions for an update. In addition, a hash lock record is used to detect if the target to boot matches the expected hash lock, and to only proceed to boot it if the hash retrieved from VLOG for a given target matches the hash computed by Secure Boot.

A new security counter record will only be created if the security counter of the new image is greater than the current security counter for an image of a given type. As each security counter record consumes 11 bytes, if each update increments the security counter, a total of 2040 / 11 = 185 security counter updates would be allowed.

If scfg.secBootCfg.policyCfg.authMethod = SCFG_POLICY_HASH_LOCK, then a new hash lock record will be created only if an update for SSB, App 0 or App 1 has been accepted. As each hash lock record consumes 41 bytes, assuming no security counter increments occur, a total of 2040 / 41 = 49 hash lock updates would be allowed. Alternatively, if each update incremented the security counter, a total of 2040 / (41 + 11) = 39 updates would be allowed.

Once VLOG is full, no more updates that require the creation of a VLOG record will be allowed, unless the device is subject to a Chip Erase.

11.10.1 Record structure

```
#define TYPEDEF_STRUCT_PACKED     typedef struct __attribute__((packed))

TYPEDEF_STRUCT_PACKED {
   uint8_t ivMajor;
   uint8_t ivMinor;
} vlogImgVer_t; /* 2 Bytes = 0x2 */

TYPEDEF_STRUCT_PACKED {
   uint16_t sof; /* 0x564c */
   struct Control {
      uint8_t status: 4;
      uint8_t recordType: 2;
      uint8_t imgType: 2;
   } control;
} vlogHdr_t; /* 3 Bytes = 0x3 */

TYPEDEF_STRUCT_PACKED {
   vlogHdr_t vlogHdr;
   vlogImgVer_t version;
   uint8_t hash[32];
   uint32_t crc32;
} vlogHashLock_t; /* 41 Bytes = 0x29 */

TYPEDEF_STRUCT_PACKED {
   vlogHdr_t vlogHdr;
   vlogImgVer_t version;
   uint16_t secCnt;
   uint32_t crc32;
} vlogSecCnt_t; /* 11 Bytes = 0xB */
```

11.11 Fallback

The fallback mechanism allows Secure Boot to boot the Secondary Secure Bootloader (if valid) if it is determined that the Application cannot be booted.

Alternatively, if Secure Boot is requested to boot a Secondary Secure Bootloader but it is determined that it cannot be booted, then Secure Boot will fallback to attempt to boot the Application (if valid).

By design, if application slots are undefined, Secure Boot will fallback to boot Secondary Secure Bootloader (if valid) and will set the status as Invalid Configuration.

11.12 ROM Panic

Secure Boot will enter ROM Panic mode if it is determined that there are no targets that can be booted. The following is a list of steps for System ROM to perform when it determines that the boot sequence cannot proceed:

- Isolate (decouple) main flash, so that it cannot be written / read.
- Enable ROM Read protections.
- Disable master IRQs.
- Set Boot Status to FAIL_NO_APP.
- Processor enters Shutdown mode.

Chapter 12

General Purpose Timers (LGPT)

This section describes the General Purpose Timer (LGPT) module and provides example use case scenarios.

12.1 Overview

The General Purpose Timer (LGPT) is used to count or time external or internal events, generate Pulse-Width Modulation (PWM) signals, and generate IR modulated codes.

There are up to four general purpose timers available. See the device specific data sheet for available timers and features.

Features

- General timing features, capture and compare
  - 3 Capture/Compare channels per timer
  - 16-bit counter width or
  - 32-bit counter width
- 8-bit prescaler
  - Configurable counter rate
  - Count from external event
- Different counter modes
  - Count up once
  - Count up repeatedly
  - Count up and down repeatedly
  - Start counting on configurable event
  - Quadrature decoding (QDEC)
- 15 different channel Capture/Compare actions
  - Period and pulse width measurement
  - 3 capture actions
  - 12 compare actions
- Filtering on capture inputs
- Generate PWM
  - Complementary PWM outputs
  - Programmable dead-band insertion
  - Park Mode on fault, sets the DIO to a predetermined state upon fault
- IR signal generation
- Generate interrupts, DMA requests and ADC triggers
- Possible to chain the timers together and synchronize them.

12.2 Block Diagram

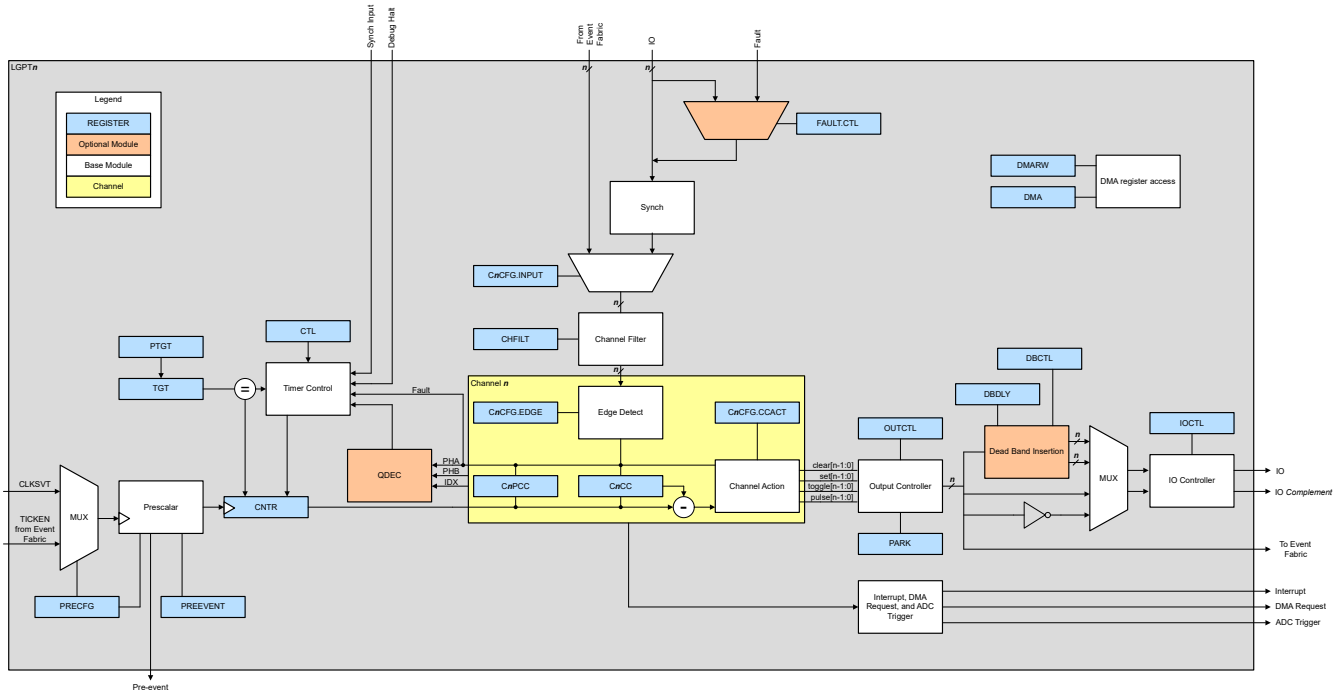

Figure 12-1. Single Timer Block Diagram

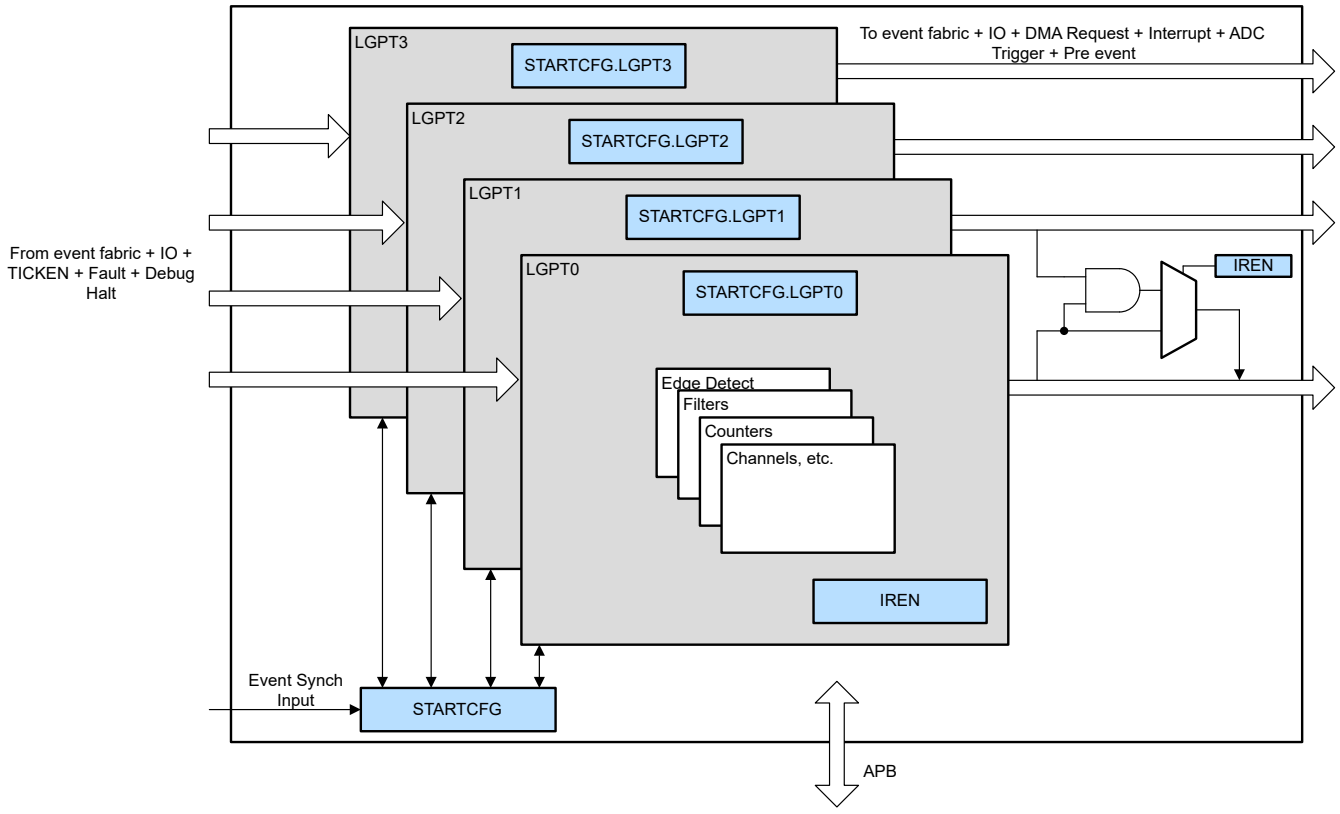

Figure 12-2. Multiple Timer Block Diagram

12.3 Functional Description

12.3.1 Prescaler

The prescaler is an 8-bit counter which counts down from the value PRECFG.TICKDIV to zero repeatedly. The rate of the down count is referred to as the prescaler clock. When the prescaler counter reaches zero, CNTR is updated. The rate of the CNTR update is referred to as the timer clock.

The prescaler can optionally run on the system clock (96MHz) or the TICKEN signal from the event fabric. This can be configured in the PRECFG.TICKSRC register field.

If the prescaler clock is configured to be the TICKEN event signal from the Event fabric, the source of the event must be subscribed by the EVTSVT.LGPT*x*TENSEL register.

The timer clock and prescaler clock determine the following:

- **Prescaler clock**
  - Timer clock
  - Prescaler event output update
  - Sampling of channel filter (optionally)
- **Timer clock**
  - CNTR rate
  - Channels update event outputs on this clock
  - Sampling of channel filter (optionally)
  - QDEC sampling

12.3.2 Counter

The value written to CTL.MODE[0:2] determines the counter mode as follows:

- UP_ONCE: The timer counts from 0 to the selected target. The timer then becomes disabled.
- UP_PER: The timer counts from 0 to the selected target, repeatedly.
- UPDWN_PER: The timer counts from 0 to the selected target and decrements back to 0, repeatedly.
- QDEC: The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectively as PHA, PHB and IDX inputs. IDX can be turned off by setting CH2CCFG.EDGE = NONE.
- SYNC_UP_ONCE: Same as UP_ONCE but the timer synchronizes to another timer. Choose which timer in STARTCFG.
- SYNC_UP_PER: Same as UP_PER but the timer synchronizes to another timer. Choose which timer in STARTCFG.
- SYNC_UPDWN_PER: Same as SYNC_UPDWN_PER but the timer synchronizes to another timer. Choose which timer in STARTCFG.

Note

While the counter can be written, the intent is only to support the setting of an initial position in QDEC mode. The ability to write the counter in other modes while the timer is running is possible, but the resulting behavior is unpredictable.

12.3.3 Target

The Target TGT register sets the target value for the counter.

The Pipline Target PTGT register, if written to, is loaded into TGT on counter zero crossing.

The QDEC mode and the SYNC modes are further described in Section 12.4.1 and Section 12.3.9.

12.3.4 Channel Input Logic

Every channel has an input which is used when the channel is configured in a capture action. The channel input can come from different sources, can be filtered and goes through an edge detection logic before triggering the channel capture. See Figure 12-3 detailing the input logic.

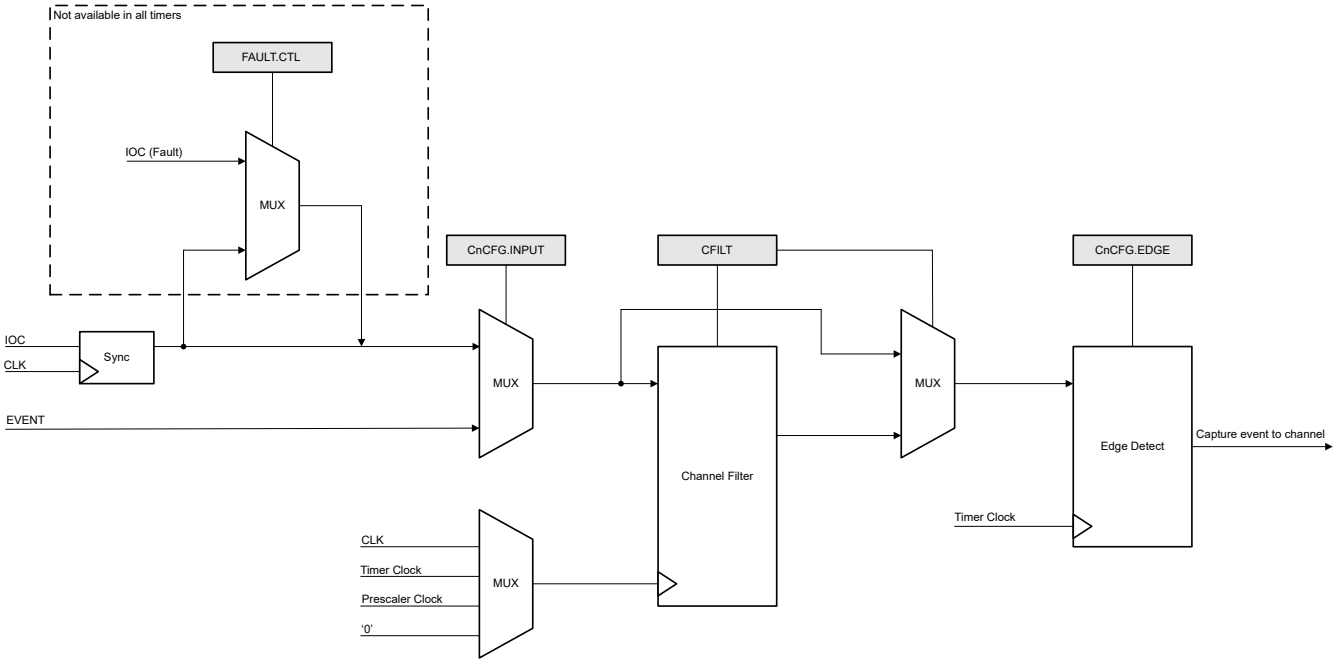

Figure 12-3. Channel Input Logic

If the FAULT register is present then enabling the FAULT logic uses channel 0 as fault input. The CnCFG.INPUT field configures if the input comes from the IOC or Event logic. The channel filter can be configured to require up to CHFILT.LOAD +1 consecutive input samples before the input is propagated to the edge detection logic. This can typically be used to avoid capturing on glitches. After the channel filter the input goes into the edge detection logic. This is configured in the CnCFG.EDGE field.

The different components of the capture data path are clocked as follow:

- The asynchronous IOC inputs are synchronized at the system clock (48MHz).
- The *channel filter*, if used, is either clocked at the system clock, timer clock or the prescaler clock.
- The *edge detect* logic is always clocked at the timer clock.

12.3.5 Channel Output Logic

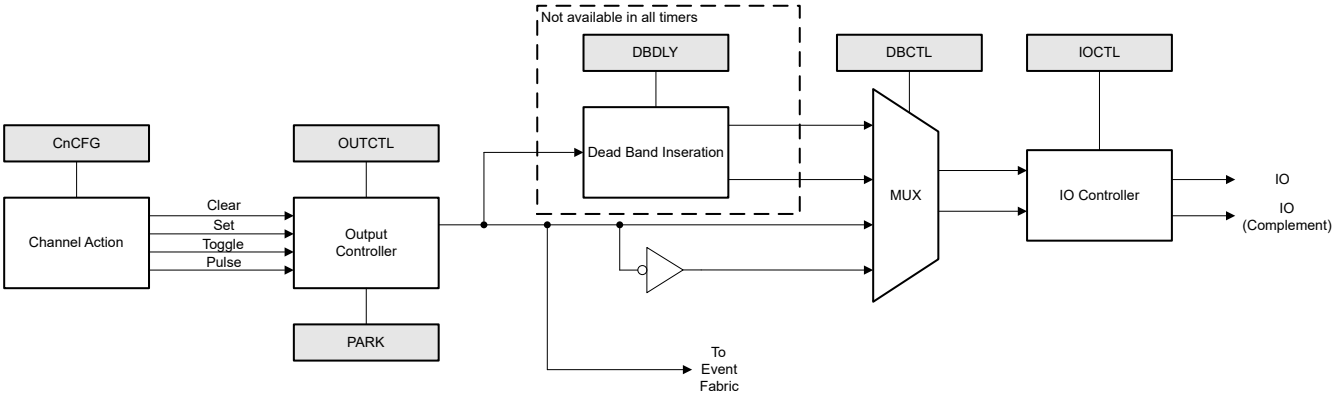

Figure 12-4. Channel Output Logic

Each timer has the same number of outputs as channels, but each channel does not control a dedicated output. Instead every channel can control every output. Which output each channel controls is configured in the CnCFG.OUTn fields.

The user can set and clear timer outputs manually by writing OUTCTL. Manual update of an output takes priority over automatic channel updates of the same output. Listed in decreasing order of priority, each output can:

1.Clear

2.Set

3.Toggle

4.Pulse (The output remains high for two counter clock periods, then goes low.)

An output can receive update requests from several channels at the same time. In this case, the output is updated according to the priority list. The output updated from an channel is decided by the channel action, CnCFG.CCACT.

12.3.6 Channel Actions

Each channel implements 15 different channel actions. Configured in CnCFG.CCACT, actions are categorized as one-shot and continuous:

- A one-shot channel action performs a function only once before the timer disables the channel.
- A continuous channel action performs a function until the user disables the channel.

Table 12-1 lists the 15 channel actions.

Table 12-1. Channel Actions

LGPT.CnCFG[3:0] CCACT bit field	**Action**	**One-shot or Continuous**
0	Disable channel	One-shot
1	Set on capture, and then disable channel	One-shot
2	Clear on zero, toggle on compare, and then disable channel	One-shot
3	Set on zero, toggle on compare, and then disable channel	One-shot
4	Clear on compare, and then disable channel	One-shot
5	Set on compare, and then disable channel	One-shot
6	Toggle on compare, and then disable channel	One-shot
7	Pulse on compare, and then disable channel	One-shot
8	Period and pulse width measurement	Continuous
9	Set on capture repeatedly	Continuous
10	Clear on zero, toggle on compare repeatedly	Continuous
11	Set on zero, toggle on compare repeatedly	Continuous
12	Clear on compare repeatedly	Continuous
13	Set on compare repeatedly	Continuous
14	Toggle on compare repeatedly	Continuous
15	Pulse on compare repeatedly	Continuous

After configuration, the channel requests updates of enabled event outputs (set by CnCFG.OUT fields) according to the channel action description in the table above. There are three channel actions that require further description.

12.3.6.1 Period and Pulse Width Measurement

This channel action continuously captures period and pulse width of the channel's input signal relative to the signal edge given by CnCFG.EDGE. The channel requests to set enabled events when CnCC.VALUE contains signal period and PCnCC.VALUE contains signal pulse width. The channel function synchronizes the timer counter to the selected signal edge of the incoming signal. Hence:

- The counter restarts regularly, so other channel actions must be chosen with this in mind.

- The channels configured for this channel action cannot perform measurements simultaneously. The measurements are done in a time-interleaved manner.

Example: Two channels in Timer Period and Pulse Width Capture

The timer measures signal period and pulse width of two different signals A (From IO Controller or Event Fabric) and B (From IO Controller or Event Fabric). See Chapter 22 and Section 4.4 for more information on configuring the I/O Controller and Event Fabric.

In this example, both signals have periods less than the counter range. Hence, time-out detection as described in the register documentation is not required. Configure as follows:

- Channel 0:
  - C0CFG. CCACT = PER_PULSE_WIDTH_MEAS
  - C0CFG. OUT0 = 1
  - C0CFG.INPUT = EVT/IO (Signal A)
  - C0CFG.EDGE = RISING
- Channel 1:
  - C1CFG. CCACT = PER_PULSE_WIDTH_MEAS
  - C1CFG. OUT1 = 1
  - C1CFG.INPUT = EVT/IO (Signal B)
  - C1CFG.EDGE = FALLING
- Timer:
  - CTL.MODE = UP_PER

Figure 12-5 shows how the timer counter first synchronizes to signal A. Channel 0 then captures the high phase of signal A into PC0CC at time t_0.The period of signal A is captured in C0CC at time t_1. At the same time, Channel 0 sets the event output 0 high, and the timer counter starts to synchronize to signal B. Channel 1 then captures the low phase of signal B into PC1CC at time t_2. Finally, the period of signal B is captured in C1CC at time t_3. At the same time, channel 1 sets the event output 1 high, and the timer counter starts to synchronize to signal A. The sequence then repeats itself until stopped by the user.

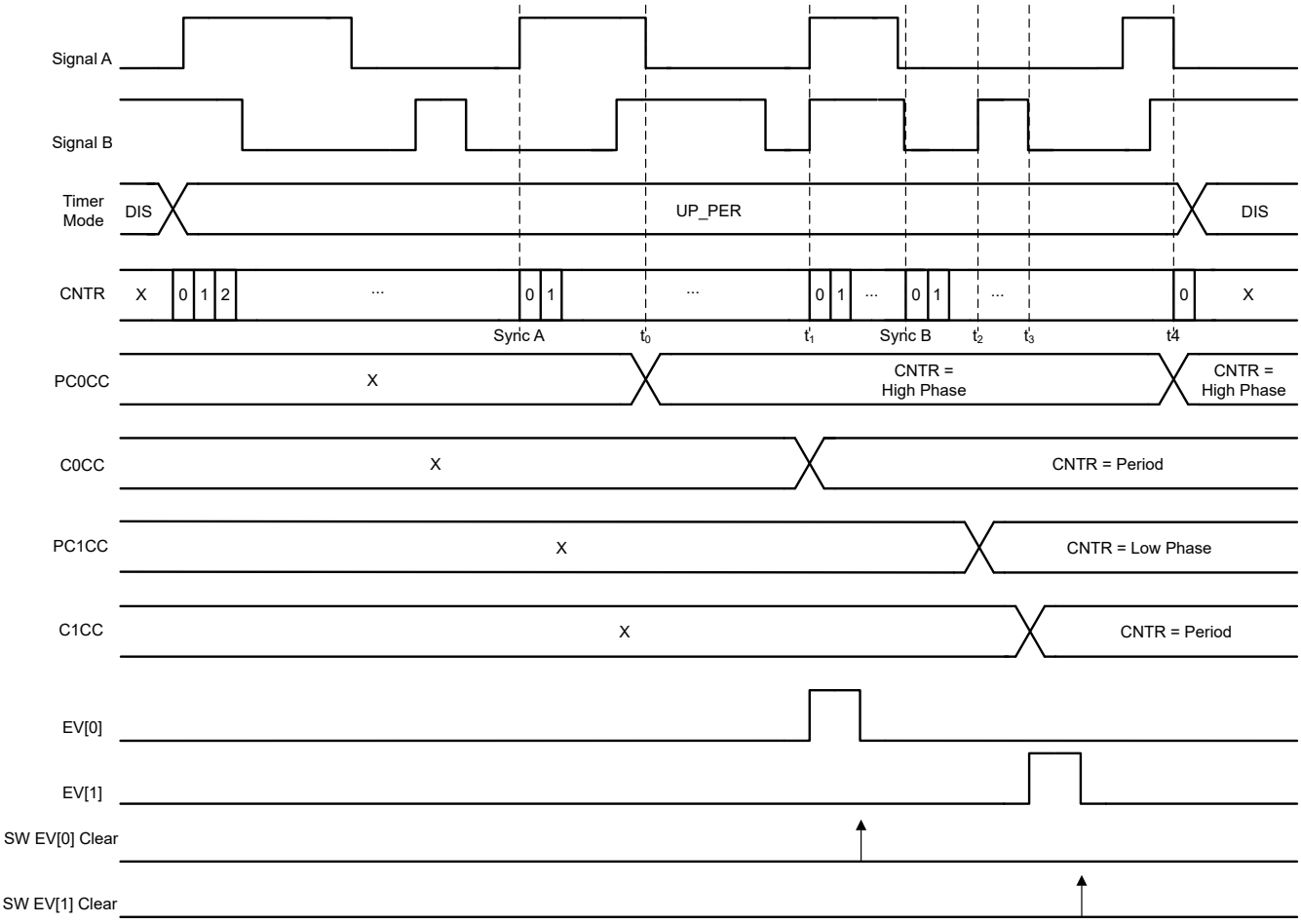

Figure 12-5. Period Pulse Width Measurement

12.3.6.2 Clear on Zero, Toggle on Compare Repeatedly

This channel action continuously:

- Clears the enabled output events when CNTR = 0
- Toggles the enabled output events when CNTR = CnCC

The channel generates center-aligned PWM waveform when CTL.MODE = UPDWN_PER. The channel copies a new value written in PCnCC to CnCC when CNTR becomes 0. This action prevents jitter on the edges of the generated PWM signal. Similarly, the timer copies a new value written in PTGT to TGT when CNTR becomes 0. This action avoids period-jitter in PWM applications with time-varying periods.

Example: Center-Aligned PWM Generation by Channel 0

This example illustrates center-aligned PWM generation by channel 0. The waveform is synthesized on output 0. The timer period is kept static, and the target value is set to half the period. Configure as follows:

- Channel 0:
  - C0CFG.CCACT = CLR_ON_0_TGL_ON_CMP
  - C0CFG.OUT0 = 1
  - C0CC = C0
- Timer:
  - TARGET = PERIOD / 2
  - CTL.MODE = UPDWN_PER

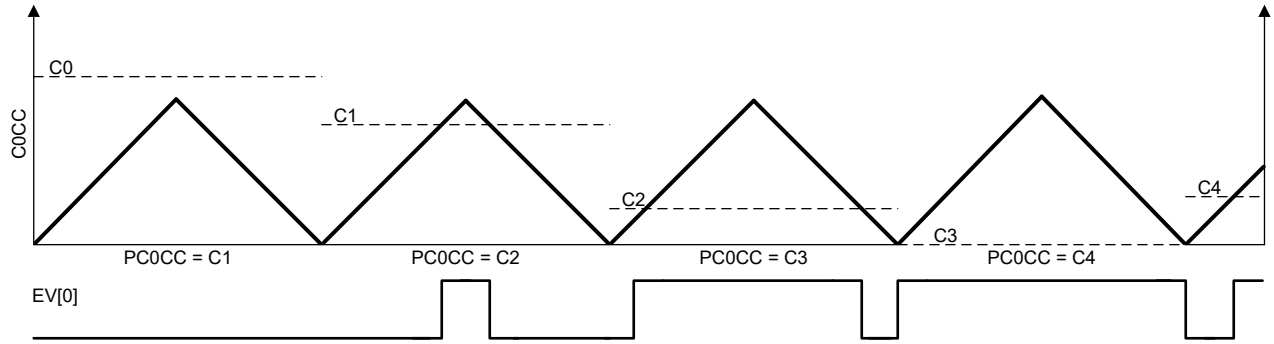

Figure 12-6. Center-Aligned PWM

The duty-cycle of the generated PWM waveform is controlled by PC0CC updates. Waveform generation on event output 0 continues until aborted by the user.

If the user wants to stop/pause the PWM generation in a controlled manner, the following procedure is recommended:

- Set FAULT.CTL = ZEROCOND
- Then set ISET.FAULT. The counter then halts at CNTR = 0.
- Counter can then either be started again by clearing RIS.FAULT, or turned completely off by setting CTL.MODE = DIS.

12.3.6.3 Set on Zero, Toggle on Compare Repeatedly

This channel action continuously does the following:

- Sets the enabled output events when CNTR = 0.
- Toggles the enabled output events when CNTR = CnCC

The channel generates an edge-aligned PWM waveform when CTL.MODE = UP_PER. The channel copies a new value written in PCnCC to CnCC when CNTR becomes 0. This prevents jitter on the edges of the generated PWM signal. Similarly, the timer copies a new value written in PTGT to TGT when CNTR becomes 0. This avoids period-jitter in PWM applications with time-varying period.

Example: Edge-Aligned PWM Generation by Channel 0

This example illustrates edge-aligned PWM generation by channel 0 (see below). The waveform is synthesized on event output 0. The timer period is kept static, and the target value is set to period minus 1. Configure as follows:

- Channel 0:
  - C0CFG.CCACT = SET_ON_0_TGL_ON_CMP
  - C0CFG. OUT0 = 1
  - C0CC = C0
- Timer:
  - TGT = PERIOD - 1
  - CTL.MODE = UP_PER

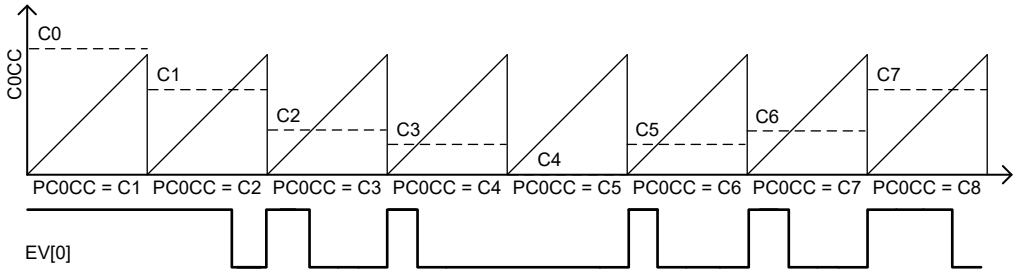

Figure 12-7. Edge-Aligned PWM

The duty-cycle of the generated PWM waveform is controlled by PC0CC updates. Waveform generation on event output 0 continues until aborted by the user.

12.3.7 Channel Capture Configuration

The channel's capture source can be set by the LGPT.CnCFG[6] INPUT bit field. Here the bit field INPUT sets either the synchronous event from event fabric, or the asynchronous IOC inputs as capture source. See Chapter 22 and Section 4.4 for more information on configuring the I/O Controller and Event Fabric.

12.3.8 Channel Filters

The channel filter sets a window within which the input must remain stable, otherwise the transition is not passed to the edge detection logic.

The channel filter counts down from CHFILT.LOAD[15:8] while two consecutive input samples are equal. If two consecutive input samples are unequal the filter counter is re-loaded with LOAD. If the channel filter reaches zero the input is passed to the edge detection logic. The filter delays the input signal by at least LOAD + 1 filter clock cycles.

When writing CTL.MODE to any other value than disabled (0x0) the internal channel filter counter is loaded with the LOAD value. Do not change the CHFILT register while the timer is running and CTL.MODE[2:0] is not disabled (0x0).

12.3.8.1 Setting up the Channel Filters

To setup the channel filters in LGPT follow these steps:

- Set the channel filter sample period by setting CHFILT.MODE:
  - CHFILT.MODE = BYPASS: No filter is used
  - CHFILT.MODE = CLK: 48 MHz sample rate (CLKSVT)
  - CHFILT.MODE = TICKCLK: Sample same as PRECFG.TICKSRC
  - CHFILT.MODE = TIMERCLK: Samples rate is same as counter rate
- Set CHFILT.LOAD value
- Start LGPT

When configuring the channel filter make sure the channel filter period is not shorter than the timer clock period. That is,

(Channel filter clock period) x (CHFILT.LOAD) > timer clock period.

If this is not satisfied capture events can be missed.

12.3.9 Synchronize Multiple LGPT Timers

The STARTCFG register can be used to synchronize multiple timers. The LGPT timers are configured in the following manner to synch to LGPT0:

- Configure LGPT1.STARTCFG = 1 and LGPT1.CTL.MODE in one of the SYNC modes.
- Configure LGPT2.STARTCFG = 1 and LGPT2.CTL.MODE in one of the SYNC modes.
- Configure LGPT3.STARTCFG = 1 and LGPT3.CTL.MODE in one of the SYNC modes.
- Start LGTP0 in the wanted mode.

Table 12-2. Sync Modes

LGPTn.CTL[2:0] MODE bit field	SYNC MODE
0	Disable
1	Not Synchronous
2	Not Synchronous
3	Not Synchronous
4	Not Synchronous
5	Count Up Once - Synchronous to another LGPT
6	Count Up Periodically - Synchronous to another LGPT
7	Count Up and Down Periodically - Synchronous to another LGPT

The timers are started when LGPT0 starts by changing the CTL.MODE field from SYNC mode to the respective active mode.

12.3.10 Interrupts, ADC Trigger, and DMA Request

Each timer can generate an Interrupt request, ADC trigger and DMA request output event. These output events can be triggered on different internal timer events. The different internal events can be viewed in the RIS register.

If one or more of the fields in the IMASK register are set high, the timer sends out an interrupt event when the internal timer event corresponding to the fields set in IMASK occur.

These internal timer events can also set the ADC trigger or DMA request depending on the configuration of the ADCTRG.SRC and DMA.REQ field. That is, the ADC trigger and DMA request output events are generated when the corresponding interrupt is set in the RIS register.

Below are some important side effects regarding the Interrupts, ADC trigger and DMA request.

- Reading/writing to the CnCC or PCnCC register shall clear the corresponding channel interrupt.
- Reading/writing to NC (No Clear) registers does not have any side effects on interrupts.
- Reading/writing to PTGT or TGT clears both RIS.ZERO and RIS.TGT.
- The CMP interrupts are updated on the timer clock. These interrupts trigger at the same time as an CMP event.
- The ZERO and TGT interrupts trigger after one system clock cycle when CNTR = ZERO/TARGET.
- The field CTL.INTP gets set when the ZERO and TGT interrupts are set. This field decides if the interrupts are set on the beginning of the timer period or on the end of the timer period.
- The RIS.ZERO interrupt is not set when starting the timer.
- Note that if you have a short timer period, and you have configured the LGPT to set the interrupt output on both ZERO and TGT, you can accidentally clear both ZERO and TGT when reading/writing to PTGT/TGT. This depends on the CPU's response time. If you want to make sure both the ZERO and TGT interrupts are received, use PTGTNC/TGTNC and clear the corresponding interrupt by writing to RIS.ICLR.
- If the µDMA request is used in addition to the interrupt make sure that a write/read does not clear unhandled interrupt requests. As an example, if the µDMA updates PTGT on ZERO interrupt and the CPU does some external handling on TGT interrupt, then if the timer period is short, the µDMA write to PTGT can clear the unhandled TGT interrupt. This can be avoided by letting the µDMA write to PTGTNC and letting the CPU clear both TGT and ZERO

12.4 Timer Modes

12.4.1 Quadrature Decoder

The Phase A (PHA), Phase B (PHB) and IDX signals are input events of channel 0, channel 1 and channel 2 respectively. PHA and PHB are required and IDX is optional. The signals are typically provided from an incremental encoder. An incremental encoder can provide two outputs which indicate a linear or a rotary motion. The output of the incremental encoder is typically a 90º shifted square wave and is provided as an input to the LGPT. When enabled in QDEC mode, the LGPT is used to decode the quadrature encoded data to provide

information on the relative positioning and movement of a linear or rotary motion. The accumulation of the counter value in LGPT with respect to PHA/PHB follows the following table:

Table 12-3. Counter Accumulation Based on QDEC Inputs

Previous Pin Event	Current Pin Event	Counter (+ or -)	Direction
PHA Falling	PHB Rising	-	Down
PHA Falling	PHB Falling	+	Up
PHA Falling	PHA Rising	+ if new dir is up, - if new dir is down	Toggle
PHA Rising	PHB Rising	+	Up
PHA Rising	PHB Falling	-	Down
PHA Rising	PHA Falling	+ if new dir is up, - if new dir is down	Toggle
PHB Falling	PHA Rising	+	Up
PHB Falling	PHA Falling	-	Down
PHB Falling	PHB Rising	+ if new dir is up, - if new dir is down	Toggle
PHB Rising	PHA Rising	-	Down
PHB Rising	PHA Falling	+	Up
PHB Rising	PHB Falling	+ if new dir is up, - if new dir is down	Toggle

To setup LGPT in QDEC mode follow these steps:

- Configure where the input is from, IOC or event fabric. Normally this is IOC:
  - PHA: C0CFG.INPUT = 1 (IOC)
  - PHB: C1CFG.INPUT = 1 (IOC)
- (Optional) IDX: C2CFG.INPUT = 1 (IOC)
- (Optional) If IDX is used set C2CFG.EDGE != 0.
- Set the sample rate. Use PRECFG.TICKDIV/TICKSRC to set the sample rate. The sample rate is:
  - TICKSRC = 0: 48 MHz / (PRECFG.TICKDIV + 1)
  - TICKSRC !=0: (ticken freq) / (PREVFG.TICKDIV + 1)
- Configure TGT and PTGT.
- (Optional) Enable channel filters. See Section 12.3.8
- (Optional) Enable QDEC interrupts:
  - (Optional) Set IMASK.DBLTRANS to get interrupt when a double transition occurs. This indicates that the sampling rate is too low.
  - (Optional) Set IMASK.CNTRCHNG to get interrupt when the counter changes. This indicates a movement of the measuring device.
  - (Optional) Set IMASK.DIRCHNG to get interrupt when the direction of the counter changes.
- (Optional) Configure PREEVENT if you want a high output signal just before the sampling, e.g. turn on a LED.
- Start timer in QDEC by writing CTL.MODE= QDEC_MODE.

Figure 12-8 shows the QDEC related signals with PREEVENT.

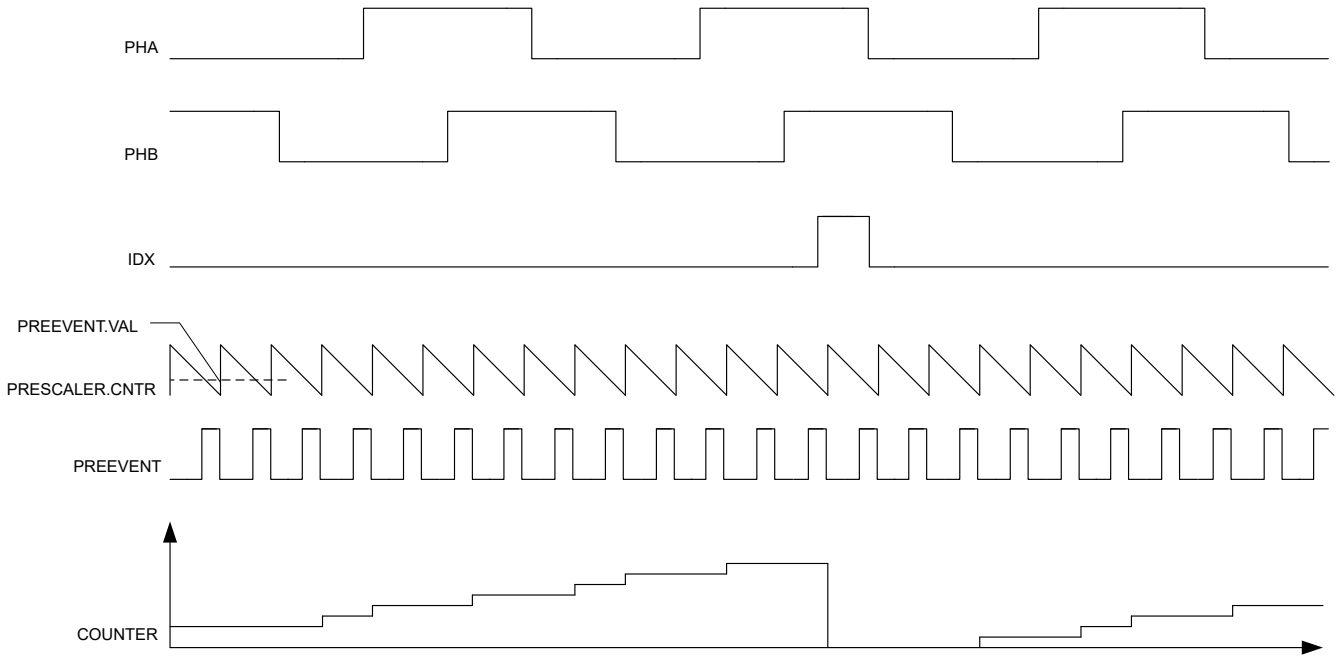

Figure 12-8. QDEC Example with PREEVENT

12.4.2 DMA

The register DMA is used to enable DMA requests. The DMA.REQ field sets which interrupt event generates a DMA request. The request is a pulse (one system clock period) which is generated when the corresponding interrupt is set in the RIS register. Upon a DMA request defined by REQ an internal address pointer is set to RWADDR*4. Every access to DMARW increments the internal pointer by 4 such that the next DMA access is to the next register.

The internal pointer stops after RWCNTR increments. Further access is ignored.

Below is an example of how to setup DMA and DMARW for updating PTGT, PC0CC, PC1CC when the counter hits zero.

- Set DMA.REQ = 2
- Set DMA.RWADDR = 63 (The PTGT address is 63*4=0xFC)
- Set DMA.RWCNTR = 2 (The PC1CC address is 63*4 + 2*4 = 0x104)
- Start timer in required mode.
- Upon receiving the DMA request the DMA should make at least 3 writes to DMARW which will be as if writing to PTGT, PC0CC then PC1CC. Any other read/writes to DMARW will be ignored.

12.4.3 IR Generation

By using LGPT0 and LGPT1 the timers can generate IR codes with minimal software interaction. By enabling IRGEN.CTL in LGPT0 an AND gate is set between T0C0 and T1C0, the output of this AND gate replaces T0C0. In IR generation mode LGPT0 generates the carrier wave, while LGP1 works as the modulator.

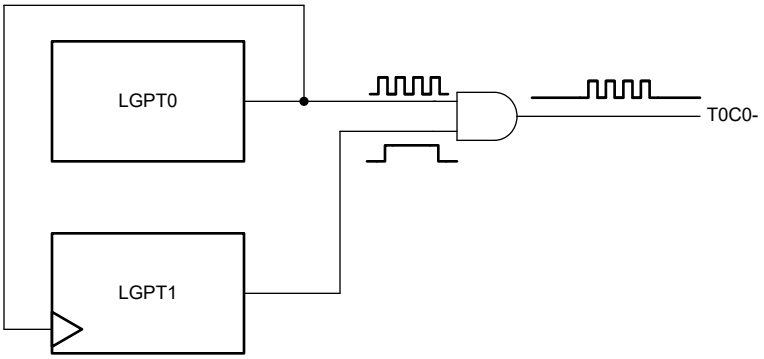

Figure 12-9. LGPT IR Generation

Below is an example on how to setup the timers for IR with a 38 kHz carrier wave.

LGPT0 (Carrier wave generation):

- Set the PRECFG.TICKDIV and TGT to fulfill the following equation:

(PRECFG.TICKDIV+1)*TGT*2 = 48 MHz / 38 kHz

E.g. PRECFG.TICKDIV = 3 and TGT 421. This gives a carrier wave of approximately 38 kHz (Theoretically 38.00475 kHz).

- Set C0CC = 210 to give roughly 50% duty cycle.
- Set C0CFG.CCACT = TGL_ON_CMP, and C0CFG.OUT0 = 1.
- Set IRGEN.CTL = 1.
- Start timer in up-periodic. CTL.MODE = 2

Configure EVTSVT

- Set EVTSVT.LGPT1TENSEL = LGPT0C0.

LGPT1 (Modulator, example for the NEC protocol)

- Set PRECFG.TICKSRC = FALL_TICK
- Set C0CFG.CCACT = SET_ON_0_TGL_ON_CMP, C0CFG.OUT0 = 1
- Set TGT to the length of the symbol.
- Set C0CC to number of 38 kHz pulses in the symbol.
- Update PTGT on RIS.ZERO interrupt to send a new symbol.

12.4.4 Fault and Park

If LGPTn.DESCEX[18] HBDF (Has Dead-Band, Fault, and Park logic) bit is set to one, the LGPT implements the FAULT and PARK registers. The FAULT register is used to stop the timer upon an active fault input signal from the IOC. The PARK register can be used to set the IOC outputs of the LGPT to a given state when the timer has stopped as a result of fault.

The fault input overrides channel 0 IOC input when FAULT.CTL != DIS. See Figure 12-3.

This means that channel 0 receives fault as input signal when C0CFG.INPUT = IO and FAULT.CTL != DIS. CHFILT can be used to avoid glitching on the fault input. Fault is level triggered, the polarity is set by the C0CFG.EDGE field. Here C0CFG.EDGE = RISE gives active high and C0CFG.EDGE = FALL gives active low polarity.

Set the Fault mode by setting FAULT.CTL. There are four different modes:

- **DIS**: The counter ignores the fault input.
- **IMMEDIATE**: In this mode the counter stops immediately on an active fault input (2 system clock cycles of synch delay is expected). This is done by hardware by setting CTL.MODE = DIS. To start the counter software must set CTL.MODE != DIS. The RIS.FAULT interrupt is also set immediately on active fault input. If

the RIS.FAULT input is cleared, it will not be set again while CTL.MODE == DIS even though the fault input is active. This is because the 2 stage synchronizers and the channel filter is not active while CTL.MODE == DIS. If the counter is started by setting CTL.MODE != DIS when the fault input is active it will immediately stop the counter and set RIS.FAULT.

- **ZEROCOND**: In this mode the counter stops when CNTR = 0 after an active fault input. If the RIS.FAULT flag has been cleared by software before CNTR= 0, and the fault input is inactive, the counter will continue as normal. When the counter stops on zero, it can be started again by clearing the RIS.FAULT flag. If you want to change the counter mode you should set CTL.MODE = DIS, clear the RIS.FAULT interrupt, then start timer in required mode. The channel filter will keep running while the CNTR is halted at zero. This ensures an up-to-date fault input.
- **IRQ**: In this mode only the RIS.FAULT interrupt is set on active fault.

General notes on Fault:

- When the channel filter is used together with Fault, and and the timer is restarted, the fault input will not be evaluated before CHFILT.LOAD number of consecutive equal samples. This means that an active fault could have been present when the timer started (by setting CTL.MODE != DIS), but the timer will not stop before CHFILT.LOAD samples.
- In IMMEDIATE mode clear RIS.FAULT to start the timer again. Not doing so will immediately stop the timer upon start.

Example setup of Fault and Park.

- Set FAULT.CTL to wanted mode.
- Set C0CFG.EDGE = RISE/FALL. Here RISE = active high, and FALL = active low.
- Set C0CFG.INPUT = IO.
- (Optional) Config CHFILT
- (Optional) Config IMASK to set CPU interrupt on fault. Typically required.
- (Optional) Config PARK.
- Start timer in wanted mode.

Figure 12-10 and Figure 12-11 illustrate the consequences of some of the possible Fault and Park configurations.

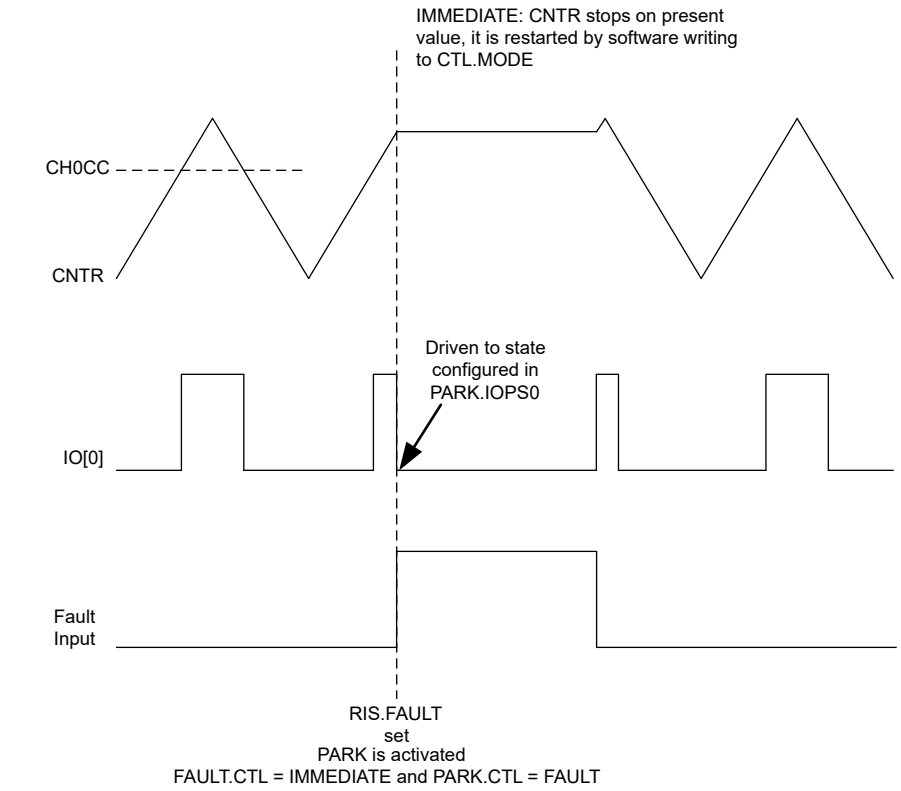

Figure 12-10. Fault and Park - Immediate Mode

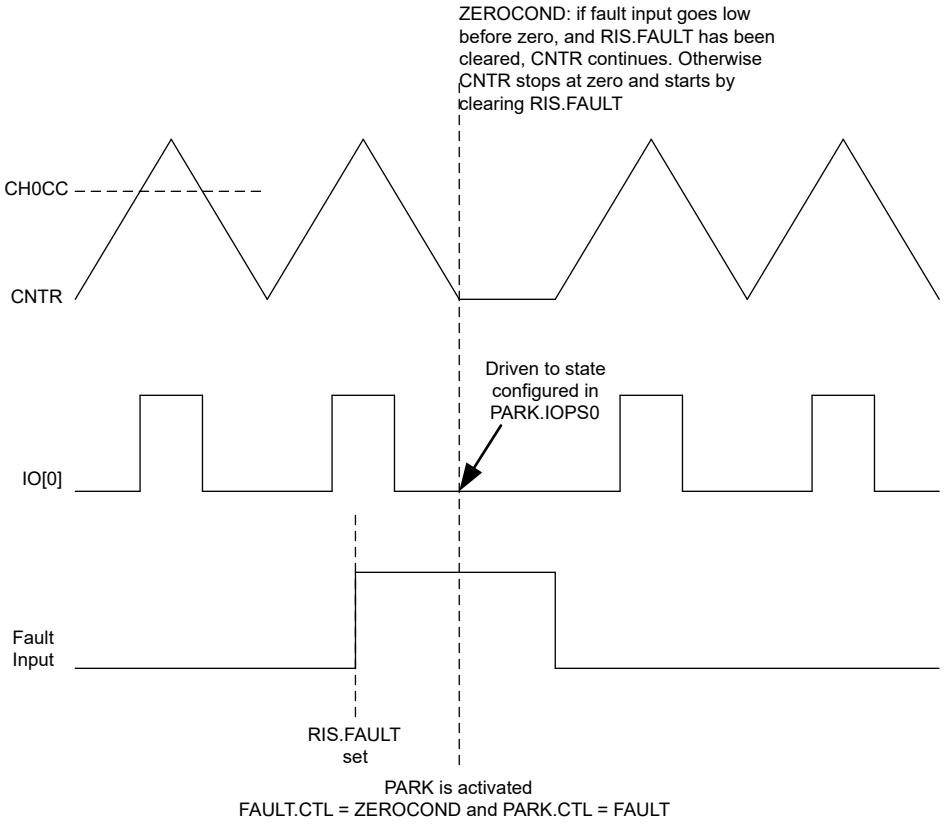

Figure 12-11. Fault and Park - Zero Condition

12.4.5 Dead-Band

If the SYS_HDBF=1 the LGPT can optionally insert a dead-band transition in a reference PWM signal. Dead band insertion is accomplished by taking a reference pulse width modulated signal and generating two pulse width modulated signals (IO*n* and IO_C*n*) of the same frequency but with a dead band period inserted between the signals. This is shown in Figure 12-12.

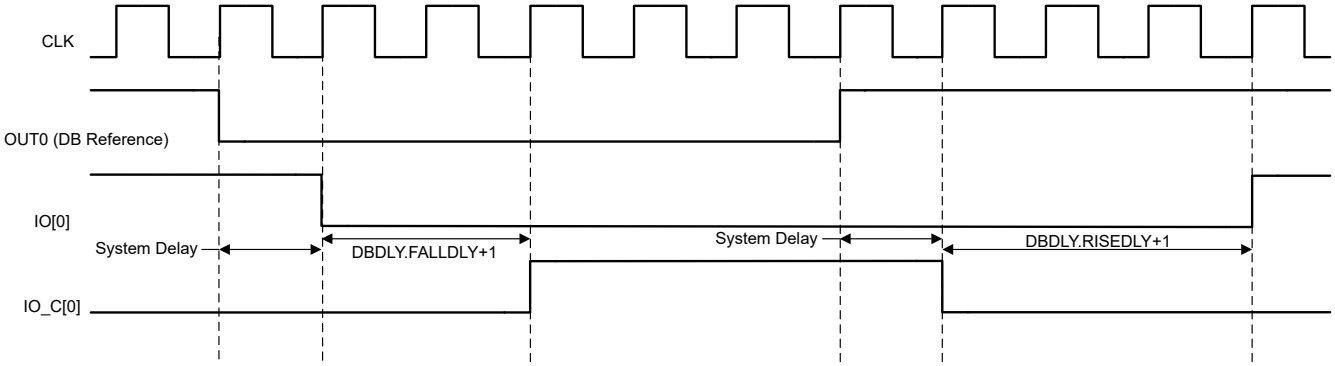

Figure 12-12. Dead-band Insertion

As shown in Figure 12-12 RISEDLY and FALLDLY fields from the DBDLY register are added with a value of 1 during Dead-Band insertion. Both IO and IO_C signals are also one system clock cycled delayed due to the Dead-band insertion logic.

Note

- Configuring RISEDLY longer than or equal to the pulse width of the reference signal results in a constant low IO output.
- Configuring FALLDLY longer than or equal to the low pulse width of the reference signal results in a constant low IO_C output.

Example setup of Dead-Band on IO0 and IO_C0

- Configure PWM output as required on channel 0. See Section 12.3.6.2
- Set PWM output to be generated on output 0 by setting C0CFG.OUT0 = 1
- Set wanted fall/rise delay by setting DBDLY.RISEDLY and DBDLY.FALLDLY.
- Set DBCTL to generate dead band on IO0 and IO_C0 by setting DBCTL.IO0 = 1.
- Start timer by writing to CTL.

12.4.6 Dead-Band, Fault and Park

An important feature to maintain when dead-band is used together with Fault and Park is to never make a switch on the IO outputs without dead band insertion. When the park values for IO and IO_C are opposite this switch is trivial, as this corresponds to a switch done under normal PWM dead band operation. See Figure 12-13.

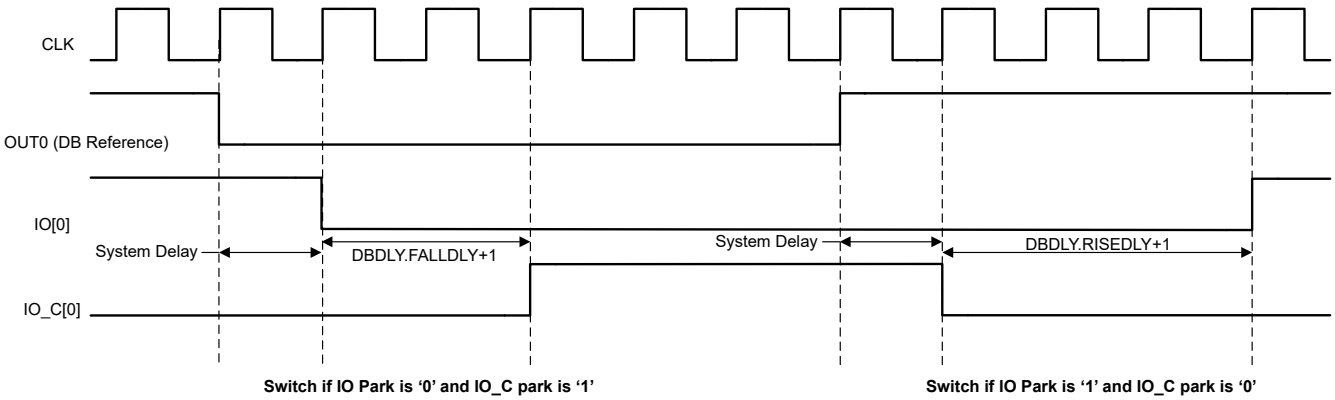

Figure 12-13. Dead-band Switch to Opposite Park States

If the IO and IO_C park values are equal the switch is not trivial. To maintain a dead-band insertion between switches, the implementation principle is as follows:

- When park is activated (either from fault or debug) the dead band reference input is set to IO park state immediately.
- This will ensure that the IO output gets set to park state after a fall/rise delay.
- When the delay is finished, meaning that IO output is in park state, this output is "locked" to the park state. The dead-band logic does not control this output anymore.
- At the same time as the IO output is locked, the dead-band reference signal is switched to the inverse of IO_C park state. This then sets IO_C to the IO_C park state after a fall/rise delay.
- As the IO output is locked, the output does not change as the dead-band reference signal changes.

When using this method, the IO and IO_C outputs can use (FALLDLY+RISEDLY+2) cycles before settling in the park state when the IO and IO_C outputs are equal. The IO and IO_C outputs use FALLDLY+1 or RISEDLY+1 to settle when the IO and IO_C outputs are opposite.

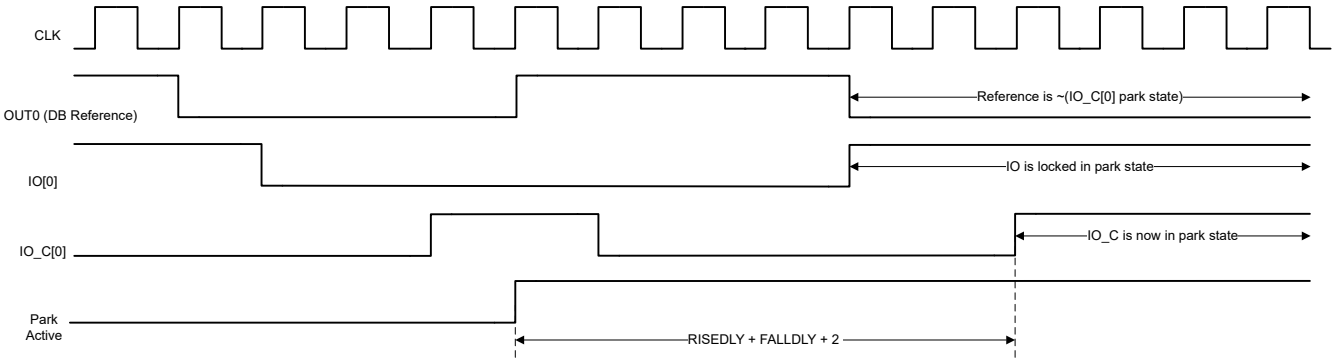

Figure 12-14. Dead-band Switch to Equal Park States

In Figure 12-14 Park active is an internal signal set by either Fault or Debug depending on the configuration. Park active is set one clock cycle after Fault or Debug is registered.

12.4.7 Example Application: Brushless DC (BLDC) Motor

The LGPT can be used to drive a BLDC motor. Consider a BLDC motor with 3 half bridges, this requires three or more channels. In this scenario the 3 IOC and the 3 IOC complementary outputs of one LGPT are connected to a motor driver or directly to the half bridges. See Figure 12-15.

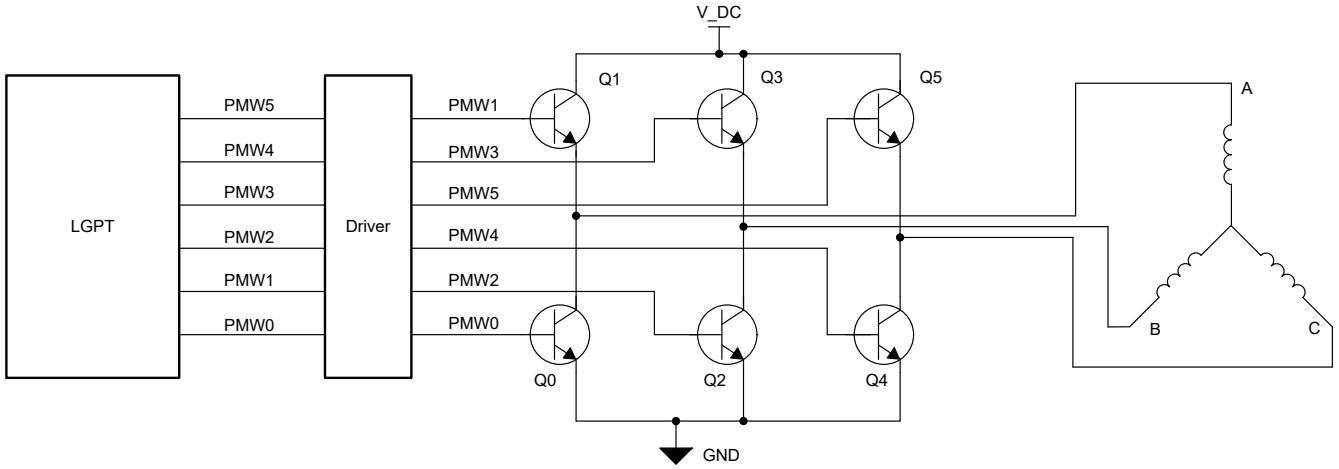

Figure 12-15. BLDC Application Example

Here each half bridge is controlled by an IOC and IOC complementary pair, that is, PWM0 and PWM1 corresponds to IOC[0] and IOC_C[0], PWM2 and PWM3 to IOC[1] and IOC_C[1] and so on. To operate the motor in a basic fashion current is driven through two of the inductors at a time in a sequential pattern. This is done by switching the transistors in a distinct pattern, see Figure 12-16.

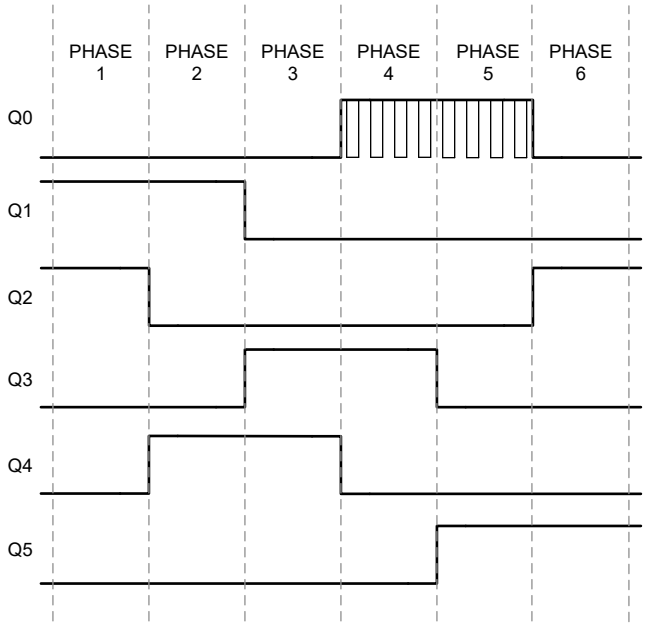

Figure 12-16. Example of Transition Phases to Drive a BLDC Motor

Notice that the high time of each transistor consists of a PWM signal (as illustrated in Q0). The duty cycle of the PWM signal corresponds to the current that is driven through the inductors and consequently the motor speed/load. The PWM can be generated as mentioned in Section 12.3.6.2. The software interactions needed to operate the motor (We assume Q0 is connected to IOC[0] and Q1 connected to IOC_C[0] etc.) are as follows:

SW operations:

- Phase 1: Configure IOCTL to invert IOC_C[0] (Q1) and let IOC[1] (Q2) out. All other outputs are configured low.
- Phase 2: Configure IOCTL to invert IOC_C[0] (Q1) and let IOC[2] (Q4) out. All other outputs are configured low.

- Phase 3: Configure IOCTL to invert IOC_C[1] (Q3) and let IOC[2] (Q4) out. All other outputs are configured low.
- Phase 4: Configure IOCTL to invert IOC_C[1] (Q3) and let IOC[0] (Q0) out. All other outputs are configured low.
- Phase 5: Configure IOCTL to invert IOC_C[2] (Q5) and let IOC[0] (Q0) out. All other outputs are configured low.
- Phase 6: Configure IOCTL to invert IOC_C[2] (Q5) and let IOC[1] (Q2) out. All other outputs are configured low.

Software needs a signal to determine when to change between the different phases, this can for example be done by an ADC measuring the back (EMF) Electromotive Force at the inactive inductor. Software can also change phases only on a ZERO interrupt from LGPT to ensure complete PWM pulses during phase changes.

12.5 LGPT0 Registers

Table 12-4 lists the memory-mapped registers for the LGPT0 registers. All register offset addresses not listed in Table 12-4 should be considered as reserved locations and the register contents should not be modified.

Table 12-4. LGPT0 Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 12.5.1
4h	DESCEX	Description Extended	Section 12.5.2
8h	STARTCFG	Start Configuration	Section 12.5.3
Ch	CTL	Timer Control	Section 12.5.4
10h	OUTCTL	Output Control	Section 12.5.5
14h	CNTR	Counter	Section 12.5.6
18h	PRECFG	Clock Prescaler Configuration	Section 12.5.7
1Ch	PREEVENT	Prescaler Event	Section 12.5.8
20h	CHFILT	Channel Input Filter	Section 12.5.9
34h	QDECSTAT	Quadrature Decoder Status	Section 12.5.10
38h	IRGEN	IR Generation	Section 12.5.11
3Ch	DMA	Direct Memory Accsess	Section 12.5.12
40h	DMARW	Direct Memory Access	Section 12.5.13
44h	ADCTRG	ADC Trigger	Section 12.5.14
48h	IOCTL	IO Controller	Section 12.5.15
68h	IMASK	Interrupt mask.	Section 12.5.16
6Ch	RIS	Raw interrupt status.	Section 12.5.17
70h	MIS	Masked interrupt status.	Section 12.5.18
74h	ISET	Interrupt set register.	Section 12.5.19
78h	ICLR	Interrupt clear register.	Section 12.5.20
7Ch	IMSET	Interrupt mask set register.	Section 12.5.21
80h	IMCLR	Interrupt mask clear register.	Section 12.5.22
84h	EMU	Debug control	Section 12.5.23
C0h	C0CFG	Channel 0 Configuration	Section 12.5.24
C4h	C1CFG	Channel 1 Configuration	Section 12.5.25
C8h	C2CFG	Channel 2 Configuration	Section 12.5.26
FCh	PTGT	Pipeline Target	Section 12.5.27
100h	PC0CC	Pipeline Channel 0 Capture Compare	Section 12.5.28
104h	PC1CC	Pipeline Channel 1 Capture Compare	Section 12.5.29
108h	PC2CC	Pipeline Channel 2 Capture Compare	Section 12.5.30
13Ch	TGT	Target	Section 12.5.31
140h	C0CC	Channel 0 Capture Compare	Section 12.5.32
144h	C1CC	Channel 1 Capture Compare	Section 12.5.33
148h	C2CC	Channel 2 Capture Compare	Section 12.5.34
17Ch	PTGTNC	Pipeline Target No Clear	Section 12.5.35
180h	PC0CCNC	Pipeline Channel 0 Capture Compare No Clear	Section 12.5.36
184h	PC1CCNC	Pipeline Channel 1 Capture Compare No Clear	Section 12.5.37
188h	PC2CCNC	Pipeline Channel 2 Capture Compare No Clear	Section 12.5.38
1BCh	TGTNC	Target No Clear	Section 12.5.39
1C0h	C0CCNC	Channel 0 Capture Compare No Clear	Section 12.5.40
1C4h	C1CCNC	Channel 1 Capture Compare No Clear	Section 12.5.41

Table 12-4. LGPT0 Registers (continued)

Offset	Acronym	Register Name	Section
1C8h	C2CCNC	Channel 2 Capture Compare No Clear	Section 12.5.42

Complex bit access types are encoded to fit into small table cells. Table 12-5 shows the codes that are used for access types in this section.

Table 12-5. LGPT0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

12.5.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 12-6.

Return to the Summary Table.

Description Register.;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 12-6. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	DE49h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number.
7-4	MAJREV	R	1h	Major revision of IP.
3-0	MINREV	R	1h	Minor revision of IP.

12.5.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 12-7.

Return to the Summary Table.

Description Extended;This register describes the parameters of the LGPT.

Table 12-7. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	HIR	R	1h	Has IR logic.
18	HDBF	R	0h	Has Dead-Band, Fault, and Park logic.
17-14	PREW	R	8h	Prescale width. The prescaler can maximum be configured to 2^{PREW}-1.
13	HQDEC	R	1h	Has Quadrature Decoder.
12	HCIF	R	1h	Has channel input filter.
11-8	CIFS	R	8h	Channel input filter size. The prevailing state filter can maximum be configured to 2^{CIFS}-1.
7	HDMA	R	1h	Has uDMA output and logic.
6	HINT	R	1h	Has interrupt output and logic.
5-4	CNTRW	R	0h	Counter bit-width.;The maximum counter value is equal to 2^{CNTRW}-1. 0h = 16-bit counter. 1h = 24-bit counter. 2h = 32-bit counter. 3h = RESERVED
3-0	NCH	R	3h	Number of channels.

12.5.3 STARTCFG Register (Offset = 8h) [Reset = 00000000h]

STARTCFG is shown in Table 12-8.

Return to the Summary Table.

Start Configuration;This register is only for when CTL.MODE is configured to one of the SYNC modes.;This register defines when this LGPT starts.

Table 12-8. STARTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LGPT0	R/W	0h	LGPT start

12.5.4 CTL Register (Offset = Ch) [Reset = 00000000h]

CTL is shown in Table 12-9.

Return to the Summary Table.

Timer Control

Table 12-9. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2RST	W	0h	Channel 2 reset. 0h = No effect. 1h = Reset C2CC, PC2CC, and C2CFG.
9	C1RST	W	0h	Channel 1 reset. 0h = No effect. 1h = Reset C1CC, PC1CC, and C1CFG.
8	C0RST	W	0h	Channel 0 reset. 0h = No effect. 1h = Reset C0CC, PC0CC, and C0CFG.
7-6	RESERVED	R	0h	Reserved
5	INTP	R/W	0h	Interrupt Phase.;This bit field controls when the RIS.TGT and RIS.ZERO interrupts are set. 0h = RIS.TGT and RIS.ZERO are set one system clock cycle after CNTR = TARGET/ZERO. 1h = RIS.TGT and RIS.ZERO are set one timer clock cycle after CNTR = TARGET/ZERO.
4-3	CMPDIR	R/W	0h	Compare direction.;This bit field controls the direction the counter must have in order to set the RIS.CnCC channel interrupts. This bitfield is only relevant if [CnCFG.CCACT] is configured to a compare action. 0h = Compare RIS fields are set on up count and down count. 1h = Compare RIS fields are only set on up count. 2h = Compare RIS fields are only set on down count. 3h = RESERVED

Table 12-9. CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MODE	R/W	0h	Timer mode control;The CNTR restarts from 0 when MODE is written to UP_ONCE, UP_PER, UPDWN_PER, QDEC, SYNC_UP_ONCE, SYNC_UP_PER or SYNC_UPDWN_PER.;When writing MODE all internally queued updates to the channels and TGT is cleared.;When configuring the timer, MODE should be the last thing to configure. If changing timer configuration after MODE has been set is necessary, instructions, if any, given in the configuration registers should be followed. See for example C0CFG. 0h = Disable timer. Updates to counter, channels, and events stop. 1h = Count up once. The timer increments from 0 to target value, then stops and sets MODE to DIS. 2h = Count up periodically. The timer increments from 0 to target value, repeatedly.;Period = (target value + 1) * timer clock period 3h = Count up and down periodically. The timer counts from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period 4h = The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectivly as PHA, PHB and IDX inputs. IDX can be turned off by setting C2CFG.EDGE = NONE.;The timer clock frequency sets the sample rate of the QDEC logic. This frequency can be configured in PRECFG. 5h = Start counting up once synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_ONCE automatically. ;It then functions as a normal timer in CTL.MODE = UP_ONCE, incrementing from 0 to target value, then stops and sets MODE to DIS. 6h = Start counting up periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_PER automatically. ;It then operates as a normal timer in CTL.MODE = UP_PER, incrementing from 0 to target value, repeatedly.;Period = (target value * 2) * timer clock period 7h = Start counting up and down periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UPDWN_PER automatically. ;It then operates as a normal timer in CTL.MODE = UPDWN_PER, counting from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period

12.5.5 OUTCTL Register (Offset = 10h) [Reset = 00000000h]

OUTCTL is shown in Table 12-10.

Return to the Summary Table.

Output Control;Set and clear individual outputs manually. Manual update of an output takes priority over automatic channel updates to the same output. It is not possible to set and clear an output at the same time, such requests will be neglected.;An output can be automatically cleared, set, toggled, or pulsed by each channel, listed in decreasing order of priority. The action with highest priority happens when multiple channels want to update an output at the same time.;All outputs are connected to the event fabric and the IO controller. The outputs going to the IO controller have an aditional complementary output, this output is the inverted IO output. Both the IO and the IO complementary outputs are passed through an IO Controller, see IOCTL.

Table 12-10. OUTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	SETOUT2	W	0h	Set output 2.;Write 1 to set output 2.
4	CLROUT2	W	0h	Clear output 2.;Write 1 to clear output 2.
3	SETOUT1	W	0h	Set output 1.;Write 1 to set output 1.
2	CLROUT1	W	0h	Clear output 1.;Write 1 to clear output 1.
1	SETOUT0	W	0h	Set output 0.;Write 1 to set output 0.
0	CLROUT0	W	0h	Clear output 0.;Write 1 to clear output 0.

12.5.6 CNTR Register (Offset = 14h) [Reset = 00000000h]

CNTR is shown in Table 12-11.

Return to the Summary Table.

Counter;The counter of this timer. After CTL.MODE is set the counter updates at the rate specified in PRECFG.

Table 12-11. CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Current counter value.;If CTL.MODE = QDEC this can be used to set the initial counter value during QDEC. Writing to CNTR in other modes than QDEC is possible, but may result in unpredictable behavior.

12.5.7 PRECFG Register (Offset = 18h) [Reset = 00000000h]

PRECFG is shown in Table 12-12.

Return to the Summary Table.

Clock Prescaler Configuration;This register is used to set the timer clock period. The prescaler is a counter which counts down from the value TICKDIV. When the prescaler counter reaches zero, CNTR is updated. The field TICKDIV effectively divides the prescaler tick source. The timer clock frequency can be calculated as TICKSRC/(TICKDIV+1).

Table 12-12. PRECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	TICKDIV	R/W	0h	Tick division.;TICKDIV determines the timer clock frequency for the counter, and timer output updates. The timer clock frequency is the clock selected by TICKSRC divided by (TICKDIV + 1). This inverse is the timer clock period.;0x00: Divide by 1.;0x01: Divide by 2.;... ;0xFF: Divide by 256.
7-2	RESERVED	R	0h	Reserved
1-0	TICKSRC	R/W	0h	Prescaler tick source.;TICKSRC determines the source which decrements the prescaler. 0h = Prescaler is updated at the system clock. 1h = Prescaler is updated at the rising edge of TICKEN. 2h = Prescaler is updated at the falling edge of TICKEN. 3h = Prescaler is updated at both edges of TICKEN.

12.5.8 PREEVENT Register (Offset = 1Ch) [Reset = 00000000h]

PREEVENT is shown in Table 12-13.

Return to the Summary Table.

Prescaler Event;This register is used to output a logic high signal before the zero crossing of the prescaler counter. The output is routed to the IOC.

Table 12-13. PREEVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Sets the HIGH time of the prescaler event output. ;Event goes high when the prescaler counter equals VAL. Event goes low when prescaler counter is 0.;Note:;- Can be used to precharge or turn an external component on for a short time before sampling, like in QDEC.;- If there is a requirement to create such events that have very short periods compared to timer clock period, use two timers. One timer acts as prescaler and event generator for another timer.

12.5.9 CHFILT Register (Offset = 20h) [Reset = 00000000h]

CHFILT is shown in Table 12-14.

Return to the Summary Table.

Channel Input Filter;This register is used to configure the filter on the channel inputs. The configuration is for all inputs.;The filter is enabled when a channel is in capture mode.;The input to the filter is passed to the edge detection logic if LOAD + 1 consecutive input samples are equal. The filter functions as a down counter, counting down every input sample.;If two consecutive samples are unequal, the filter counter restarts from LOAD.;If the filter counter reaches zero, the input signal is valid and passed to the edge detection logic.;The channel filter should only be configured while the CTL.MODE = DIS. Configuring the filter while the timer is running can result in unexpected behavior.

Table 12-14. CHFILT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	LOAD	R/W	0h	The input of the channel filter is passed to the edge detection logic after LOAD + 1 consecutive equal samples.
7-2	RESERVED	R	0h	Reserved
1-0	MODE	R/W	0h	Channel filter mode 0h = Filter is bypassed. No Filter is used. 1h = Filter is clocked by system clock. 2h = Filter is clocked by PRECFG.TICKSRC. 3h = Filter is clocked by timer clock.

12.5.10 QDECSTAT Register (Offset = 34h) [Reset = 00000000h]

QDECSTAT is shown in Table 12-15.

Return to the Summary Table.

Quadrature Decoder Status;This register can be used during QDEC mode to check the status of the quadrature decoder.

Table 12-15. QDECSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	DBLTRANS	R	0h	Double transition 0h = Single or no transition on phase inputs. 1h = Double transition on phase inputs.
0	QDIR	R	0h	Direction of count during QDEC mode. 0h = Up (PHA leads PHB) 1h = Down (PHB leads PHA)

12.5.11 IRGEN Register (Offset = 38h) [Reset = 00000000h]

IRGEN is shown in Table 12-16.

Return to the Summary Table.

IR Generation;Use this register to generate IR codes. When CTL = 1, an AND gate is enabled between IO output 0 in LGPT0 and IC output 0 in LGPT1. The output of the gate overrides IO output 0 in LGPT0. See OUTCTL for explanation of outputs. ;To generate IR codes let LGPT0 generate the carrier wave on output 0. Set this output as tick input of LGPT1, with PRECFG.TICKSRC = FALL_TICK. ;Generate wanted IR codes by adjusting LGPT1 PTGT and PC0CC.

Table 12-16. IRGEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CTL	R/W	0h	Control 0h = Disable. 1h = Enable.

12.5.12 DMA Register (Offset = 3Ch) [Reset = 00000000h]

DMA is shown in Table 12-17.

Return to the Summary Table.

Direct Memory Accsess;This register is used to enable DMA requests from the timer and set the register addresses which the DMA will access (read/write).;Choose DMA request source by setting the REQ field. The setting of the corresponding interrupt in the RIS registers also sets the DMA request. ;Upon a DMA request defined by REQ an internal address pointer is set to RWADDR*4. Every access to DMARW will increment the internal pointer by 4 such that the next DMA access will be to the next register.;The internal pointer will stop after RWCNTR increments. Further access will be ignored.

Table 12-17. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RWCNTR	R/W	0h	The read/write counter. RWCNTR+1 is the number of times the DMA can access (read/write) the DMARW register. For each DMA access to DMARW an internal counter is incremented, writing to the next address field. RWADDR + 4*RWCNTR is the final register address which can be accessed by the DMA.
15	RESERVED	R	0h	Reserved
14-8	RWADDR	R/W	0h	The base address which the DMA access when reading/writing DMARW. The base address is set by taking the 9 LSB of the physical address and divide by 4.;For example, if you wanted the RWADDR to point to the PTGT register you should set RWADDR = 0x0FC/4.
7-4	RESERVED	R	0h	Reserved
3-0	REQ	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates a DMA request. 2h = Setting of RIS.ZERO generates a DMA request. 3h = Setting of RIS.FAULT generates a DMA request. 4h = Setting of RIS.C0CC generates a DMA request. 5h = Setting of RIS.C1CC generates a DMA request. 6h = Setting of RIS.C2CC generates a DMA request. 7h = Setting of RIS.C3CC generates a DMA request. 8h = Setting of RIS.C4CC generates a DMA request. 9h = Setting of RIS.C5CC generates a DMA request. Ah = Setting of RIS.C6CC generates a DMA request. Bh = Setting of RIS.C7CC generates a DMA request. Ch = Setting of RIS.C8CC generates a DMA request. Dh = Setting of RIS.C9CC generates a DMA request. Eh = Setting of RIS.C10CC generates a DMA request. Fh = Setting of RIS.C11CC generates a DMA request.

12.5.13 DMARW Register (Offset = 40h) [Reset = 00000000h]

DMARW is shown in Table 12-18.

Return to the Summary Table.

Direct Memory Access;This register is used by the DMA to access (read/write) register inside this LGPT module.;Each access to this register will increment the internal DMA address counter. See DMA for description.

Table 12-18. DMARW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	DMA read write value.;The value that is read/written from/to the registers.

12.5.14 ADCTRG Register (Offset = 44h) [Reset = 00000000h]

ADCTRG is shown in Table 12-19.

Return to the Summary Table.

ADC Trigger;This register is used to enable ADC trigger from the timer. ;Choose ADC trigger source by setting the SRC field. The setting of the corresponding interrupt in the RIS registers also sets the ADC trigger.

Table 12-19. ADCTRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	SRC	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates an ADC trigger. 2h = Setting of RIS.ZERO generates an ADC trigger. 3h = Setting of RIS.FAULT generates an ADC trigger. 4h = Setting of RIS.C0CC generates an ADC trigger. 5h = Setting of RIS.C1CC generates an ADC trigger. 6h = Setting of RIS.C2CC generates an ADC trigger. 7h = Setting of RIS.C3CC generates an ADC trigger. 8h = Setting of RIS.C4CC generates an ADC trigger. 9h = Setting of RIS.C5CC generates an ADC trigger. Ah = Setting of RIS.C6CC generates an ADC trigger. Bh = Setting of RIS.C7CC generates an ADC trigger. Ch = Setting of RIS.C8CC generates an ADC trigger. Dh = Setting of RIS.C9CC generates an ADC trigger. Eh = Setting of RIS.C10CC generates an ADC trigger. Fh = Setting of RIS.C11CC generates an ADC trigger.

12.5.15 IOCTL Register (Offset = 48h) [Reset = 00000000h]

IOCTL is shown in Table 12-20.

Return to the Summary Table.

IO Controller;This register overrides the IO outputs.

Table 12-20. IOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-10	COUT2	R/W	0h	IO complementary output 2 control;This bit field controls IO complementary output 2. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
9-8	OUT2	R/W	0h	IO output 2 control;This bit field controls IO output 2. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
7-6	COUT1	R/W	0h	IO complementary output 1 control;This bit field controls IO complementary output 1. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
5-4	OUT1	R/W	0h	IO output 1 control;This bit field controls IO output 1. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
3-2	COUT0	R/W	0h	IO complementary output 0 control;This bit field controls IO complementary output 0. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
1-0	OUT0	R/W	0h	IO output 0 control;This bit field controls IO output 0. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.

12.5.16 IMASK Register (Offset = 68h) [Reset = 00000000h]

IMASK is shown in Table 12-21.

Return to the Summary Table.

Interrupt mask. ;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 12-21. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R/W	0h	Enable RIS.C2CC interrupt. 0h = Disable 1h = Enable
9	C1CC	R/W	0h	Enable RIS.C1CC interrupt. 0h = Disable 1h = Enable
8	C0CC	R/W	0h	Enable RIS.C0CC interrupt. 0h = Disable 1h = Enable
7	RESERVED	R	0h	Reserved
6	FAULT	R/W	0h	Enable RIS.FAULT interrupt. 0h = Disable 1h = Enable
5	IDX	R/W	0h	Enable RIS.IDX interrupt. 0h = Disable 1h = Enable
4	DIRCHNG	R/W	0h	Enable RIS.DIRCHNG interrupt. 0h = Disable 1h = Enable
3	CNTRCHNG	R/W	0h	Enable RIS.CNTRCHNG interrupt. 0h = Disable 1h = Enable
2	DBLTRANS	R/W	0h	Enable RIS.DBLTRANS interrupt. 0h = Disable 1h = Enable
1	ZERO	R/W	0h	Enable RIS.ZERO interrupt. 0h = Disable 1h = Enable
0	TGT	R/W	0h	Enable RIS.TGT interrupt. 0h = Disable 1h = Enable

12.5.17 RIS Register (Offset = 6Ch) [Reset = 00000000h]

RIS is shown in Table 12-22.

Return to the Summary Table.

Raw interrupt status. ;This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-22. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Status of the C2CC interrupt. The interrupt is set when C2CC has capture or compare event. 0h = Cleared 1h = Set
9	C1CC	R	0h	Status of the C1CC interrupt. The interrupt is set when C1CC has capture or compare event. 0h = Cleared 1h = Set
8	C0CC	R	0h	Status of the C0CC interrupt. The interrupt is set when C0CC has capture or compare event. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Status of the FAULT interrupt. The interrupt is set immediately on active fault input. 0h = Cleared 1h = Set
5	IDX	R	0h	Status of the IDX interrupt. The interrupt is set when IDX is active. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Status of the DIRCHNG interrupt. The interrupt is set when the direction of the counter changes. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Status of the CNTRCHNG interrupt. The interrupt is set when the counter increments or decrements. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Status of the DBLTRANS interrupt. The interrupt is set when a double transition has happened during QDEC mode. 0h = Cleared 1h = Set
1	ZERO	R	0h	Status of the ZERO interrupt. The interrupt is set when CNTR = 0. 0h = Cleared 1h = Set
0	TGT	R	0h	Status of the TGT interrupt. The interrupt is set when CNTR = TGT. 0h = Cleared 1h = Set

12.5.18 MIS Register (Offset = 70h) [Reset = 00000000h]

MIS is shown in Table 12-23.

Return to the Summary Table.

Masked interrupt status. ;This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-23. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Masked status of the RIS.C2CC interrupt. 0h = Cleared 1h = Set
9	C1CC	R	0h	Masked status of the RIS.C1CC interrupt. 0h = Cleared 1h = Set
8	C0CC	R	0h	Masked status of the RIS.C0CC interrupt. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Masked status of the RIS.FAULT interrupt. 0h = Cleared 1h = Set
5	IDX	R	0h	Masked status of the RIS.IDX interrupt. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Masked status of the RIS.DIRCHNG interrupt. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Masked status of the RIS.CNTRCHNG interrupt. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Masked status of the RIS.DBLTRANS interrupt. 0h = Cleared 1h = Set
1	ZERO	R	0h	Masked status of the RIS.ZERO interrupt. 0h = Cleared 1h = Set
0	TGT	R	0h	Masked status of the RIS.TGT interrupt. 0h = Cleared 1h = Set

12.5.19 ISET Register (Offset = 74h) [Reset = 00000000h]

ISET is shown in Table 12-24.

Return to the Summary Table.

Interrupt set register. ;This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 12-24. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the RIS.C2CC interrupt. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the RIS.C1CC interrupt. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the RIS.C0CC interrupt. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the RIS.FAULT interrupt. 0h = No effect 1h = Set
5	IDX	W	0h	Set the RIS.IDX interrupt. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the RIS.DIRCHNG interrupt. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the RIS.DBLTRANS interrupt. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the RIS.ZERO interrupt. 0h = No effect 1h = Set
0	TGT	W	0h	Set the RIS.TGT interrupt. 0h = No effect 1h = Set

12.5.20 ICLR Register (Offset = 78h) [Reset = 00000000h]

ICLR is shown in Table 12-25.

Return to the Summary Table.

Interrupt clear register. ;This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 12-25. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the RIS.C2CC interrupt. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the RIS.C1CC interrupt. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the RIS.C0CC interrupt. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the RIS.FAULT interrupt. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the RIS.IDX interrupt. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the RIS.DIRCHNG interrupt. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the RIS.DBLTRANS interrupt. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the RIS.ZERO interrupt. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the RIS.TGT interrupt. 0h = No effect 1h = Clear

12.5.21 IMSET Register (Offset = 7Ch) [Reset = 00000000h]

IMSET is shown in Table 12-26.

Return to the Summary Table.

Interrupt mask set register. ;Writing a 1 to a bit in this register will set the corresponding IMASK bit.

Table 12-26. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the MIS.C2CC mask. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the MIS.C1CC mask. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the MIS.C0CC mask. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the MIS.FAULT mask. 0h = No effect 1h = Set
5	IDX	W	0h	Set the MIS.IDX mask. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the MIS.DIRCHNG mask. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the MIS.CNTRCHNG mask. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the MIS.DBLTRANS mask. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the MIS.ZERO mask. 0h = No effect 1h = Set
0	TGT	W	0h	Set the MIS.TGT mask. 0h = No effect 1h = Set

12.5.22 IMCLR Register (Offset = 80h) [Reset = 00000000h]

IMCLR is shown in Table 12-27.

Return to the Summary Table.

Interrupt mask clear register. ;Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 12-27. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the MIS.C2CC mask. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the MIS.C1CC mask. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the MIS.C0CC mask. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the MIS.FAULT mask. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the MIS.IDX mask. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the MIS.DIRCHNG mask. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the MIS.CNTRCHNG mask. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the MIS.DBLTRANS mask. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the MIS.ZERO mask. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the MIS.TGT mask. 0h = No effect 1h = Clear

12.5.23 EMU Register (Offset = 84h) [Reset = 00000000h]

EMU is shown in Table 12-28.

Return to the Summary Table.

Debug control;This register can be used to freeze the timer when CPU halts when HALT is set to 1. When HALT is set to 0, or when the CPU releases debug halt, the filters and edge detection logic is flushed and the timer starts. For setting a predefined output value during a CPU debug halt, PARK, if the timer has this register, should be configured additionally. If this timer does not have the PARK register a predefined output value during CPU halt is not possible.

Table 12-28. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CTL	R/W	0h	Halt control.;Configure when the counter shall stop upon CPU halt. This bitfield only applies if HALT = 1. 0h = Immediate reaction. The counter stops immediately on debug halt. 1h = Zero condition. The counter stops when CNTR = 0.
0	HALT	R/W	0h	Halt LGPT when CPU is halted in debug. 0h = Disable. 1h = Enable.

12.5.24 C0CFG Register (Offset = C0h) [Reset = 00000000h]

C0CFG is shown in Table 12-29.

Return to the Summary Table.

Channel 0 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-29. C0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 2. 1h = Channel 0 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 1. 1h = Channel 0 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 0. 1h = Channel 0 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-29. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C0CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C0CC when C0CC.VAL contains signal period and PC0CC.VAL contains signal pulse width.;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C0CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-29. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C0CC.VAL / TGT.VAL).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle = C0CC.VAL / (TGT.VAL + 1).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.5.25 C1CFG Register (Offset = C4h) [Reset = 00000000h]

C1CFG is shown in Table 12-30.

Return to the Summary Table.

Channel 1 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-30. C1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 2. 1h = Channel 1 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 1. 1h = Channel 1 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 0. 1h = Channel 1 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-30. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C1CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C1CC when C1CC.VAL contains signal period and PC1CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C1CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-30. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C1CC.VAL / TGT.VAL).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle = C1CC.VAL / (TGT.VAL + 1).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.5.26 C2CFG Register (Offset = C8h) [Reset = 00000000h]

C2CFG is shown in Table 12-31.

Return to the Summary Table.

Channel 2 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-31. C2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 2. 1h = Channel 2 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 1. 1h = Channel 2 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 0. 1h = Channel 2 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-31. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C2CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C2CC when C2CC.VAL contains signal period and PC2CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C2CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-31. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C2CC.VAL / TGT.VAL).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle = C2CC.VAL / (TGT.VAL + 1).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.5.27 PTGT Register (Offset = FCh) [Reset = 00000000h]

PTGT is shown in Table 12-32.

Return to the Summary Table.

Pipeline Target;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer will copy PTGT.VAL to TGT.VAL on the upcoming CNTR zero crossing only if PTGT.VAL has been written. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC;The CNTR value is updated with VALUE on IDX if the counter is counting down. If the counter is counting up, CNTR is loaded with zero on IDX.;In this mode the VALUE is not loaded into TGT on zero crossing.

Table 12-32. PTGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	The pipleline target value.

12.5.28 PC0CC Register (Offset = 100h) [Reset = 00000000h]

PC0CC is shown in Table 12-33.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare

Table 12-33. PC0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.5.29 PC1CC Register (Offset = 104h) [Reset = 00000000h]

PC1CC is shown in Table 12-34.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare

Table 12-34. PC1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.5.30 PC2CC Register (Offset = 108h) [Reset = 00000000h]

PC2CC is shown in Table 12-35.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare

Table 12-35. PC2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.5.31 TGT Register (Offset = 13Ch) [Reset = 00000000h]

TGT is shown in Table 12-36.

Return to the Summary Table.

Target;User defined counter target. ;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.

Table 12-36. TGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	FFFFh	User defined counter target value.

12.5.32 C0CC Register (Offset = 140h) [Reset = 00000000h]

C0CC is shown in Table 12-37.

Return to the Summary Table.

Channel 0 Capture Compare

Table 12-37. C0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.5.33 C1CC Register (Offset = 144h) [Reset = 00000000h]

C1CC is shown in Table 12-38.

Return to the Summary Table.

Channel 1 Capture Compare

Table 12-38. C1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.5.34 C2CC Register (Offset = 148h) [Reset = 00000000h]

C2CC is shown in Table 12-39.

Return to the Summary Table.

Channel 2 Capture Compare

Table 12-39. C2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.5.35 PTGTNC Register (Offset = 17Ch) [Reset = 00000000h]

PTGTNC is shown in Table 12-40.

Return to the Summary Table.

Pipeline Target No Clear;Use this register to read or write to PTGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-40. PTGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	A read or write to this register will not clear the RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer copies VAL to TGT.VAL when CNTR.VAL becomes 0. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC.;The CNTR.VAL is updated with VAL on IDX. VAL is not loaded into TGT.VAL when CNTR.VAL becomes 0.

12.5.36 PC0CCNC Register (Offset = 180h) [Reset = 00000000h]

PC0CCNC is shown in Table 12-41.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare No Clear

Table 12-41. PC0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.5.37 PC1CCNC Register (Offset = 184h) [Reset = 00000000h]

PC1CCNC is shown in Table 12-42.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare No Clear

Table 12-42. PC1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.5.38 PC2CCNC Register (Offset = 188h) [Reset = 00000000h]

PC2CCNC is shown in Table 12-43.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare No Clear

Table 12-43. PC2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.5.39 TGTNC Register (Offset = 1BCh) [Reset = 00000000h]

TGTNC is shown in Table 12-44.

Return to the Summary Table.

Target No Clear;Use this register to read or write to TGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-44. TGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	FFFFh	User defined counter target value.

12.5.40 C0CCNC Register (Offset = 1C0h) [Reset = 00000000h]

C0CCNC is shown in Table 12-45.

Return to the Summary Table.

Channel 0 Capture Compare No Clear

Table 12-45. C0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.5.41 C1CCNC Register (Offset = 1C4h) [Reset = 00000000h]

C1CCNC is shown in Table 12-46.

Return to the Summary Table.

Channel 1 Capture Compare No Clear

Table 12-46. C1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.5.42 C2CCNC Register (Offset = 1C8h) [Reset = 00000000h]

C2CCNC is shown in Table 12-47.

Return to the Summary Table.

Channel 2 Capture Compare No Clear

Table 12-47. C2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.6 LGPT1 Registers

Table 12-48 lists the memory-mapped registers for the LGPT1 registers. All register offset addresses not listed in Table 12-48 should be considered as reserved locations and the register contents should not be modified.

Table 12-48. LGPT1 Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 12.6.1
4h	DESCEX	Description Extended	Section 12.6.2
8h	STARTCFG	Start Configuration	Section 12.6.3
Ch	CTL	Timer Control	Section 12.6.4
10h	OUTCTL	Output Control	Section 12.6.5
14h	CNTR	Counter	Section 12.6.6
18h	PRECFG	Clock Prescaler Configuration	Section 12.6.7
1Ch	PREEVENT	Prescaler Event	Section 12.6.8
20h	CHFILT	Channel Input Filter	Section 12.6.9
24h	FAULT	Fault	Section 12.6.10
28h	PARK	Park	Section 12.6.11
2Ch	DBDLY	Dead Band Delay	Section 12.6.12
30h	DBCTL	Dead Band Control	Section 12.6.13
3Ch	DMA	Direct Memory Accsess	Section 12.6.14
40h	DMARW	Direct Memory Access	Section 12.6.15
44h	ADCTRG	ADC Trigger	Section 12.6.16
48h	IOCTL	IO Controller	Section 12.6.17
68h	IMASK	Interrupt mask.	Section 12.6.18
6Ch	RIS	Raw interrupt status.	Section 12.6.19
70h	MIS	Masked interrupt status.	Section 12.6.20
74h	ISET	Interrupt set register.	Section 12.6.21
78h	ICLR	Interrupt clear register.	Section 12.6.22
7Ch	IMSET	Interrupt mask set register.	Section 12.6.23
80h	IMCLR	Interrupt mask clear register.	Section 12.6.24
84h	EMU	Debug control	Section 12.6.25
C0h	C0CFG	Channel 0 Configuration	Section 12.6.26
C4h	C1CFG	Channel 1 Configuration	Section 12.6.27
C8h	C2CFG	Channel 2 Configuration	Section 12.6.28
FCh	PTGT	Pipeline Target	Section 12.6.29
100h	PC0CC	Pipeline Channel 0 Capture Compare	Section 12.6.30
104h	PC1CC	Pipeline Channel 1 Capture Compare	Section 12.6.31
108h	PC2CC	Pipeline Channel 2 Capture Compare	Section 12.6.32
13Ch	TGT	Target	Section 12.6.33
140h	C0CC	Channel 0 Capture Compare	Section 12.6.34
144h	C1CC	Channel 1 Capture Compare	Section 12.6.35
148h	C2CC	Channel 2 Capture Compare	Section 12.6.36
17Ch	PTGTNC	Pipeline Target No Clear	Section 12.6.37
180h	PC0CCNC	Pipeline Channel 0 Capture Compare No Clear	Section 12.6.38
184h	PC1CCNC	Pipeline Channel 1 Capture Compare No Clear	Section 12.6.39
188h	PC2CCNC	Pipeline Channel 2 Capture Compare No Clear	Section 12.6.40
1BCh	TGTNC	Target No Clear	Section 12.6.41

Table 12-48. LGPT1 Registers (continued)

Offset	Acronym	Register Name	Section
1C0h	C0CCNC	Channel 0 Capture Compare No Clear	Section 12.6.42
1C4h	C1CCNC	Channel 1 Capture Compare No Clear	Section 12.6.43
1C8h	C2CCNC	Channel 2 Capture Compare No Clear	Section 12.6.44

Complex bit access types are encoded to fit into small table cells. Table 12-49 shows the codes that are used for access types in this section.

Table 12-49. LGPT1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

12.6.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 12-50.

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Description Register.;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 12-50. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	DE49h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number.
7-4	MAJREV	R	1h	Major revision of IP.
3-0	MINREV	R	1h	Minor revision of IP.

12.6.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 12-51.

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Description Extended;This register describes the parameters of the LGPT.

Table 12-51. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	HIR	R	0h	Has IR logic.
18	HDBF	R	1h	Has Dead-Band, Fault, and Park logic.
17-14	PREW	R	8h	Prescale width. The prescaler can maximum be configured to 2^{PREW}-1.
13	HQDEC	R	0h	Has Quadrature Decoder.
12	HCIF	R	1h	Has channel input filter.
11-8	CIFS	R	8h	Channel input filter size. The prevailing state filter can maximum be configured to 2^{CIFS}-1.
7	HDMA	R	1h	Has uDMA output and logic.
6	HINT	R	1h	Has interrupt output and logic.
5-4	CNTRW	R	0h	Counter bit-width.;The maximum counter value is equal to 2^{CNTRW}-1. 0h = 16-bit counter. 1h = 24-bit counter. 2h = 32-bit counter. 3h = RESERVED
3-0	NCH	R	3h	Number of channels.

12.6.3 STARTCFG Register (Offset = 8h) [Reset = 00000000h]

STARTCFG is shown in Table 12-52.

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Start Configuration;This register is only for when CTL.MODE is configured to one of the SYNC modes.;This register defines when this LGPT starts.

Table 12-52. STARTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LGPT0	R/W	0h	LGPT start

12.6.4 CTL Register (Offset = Ch) [Reset = 00000000h]

CTL is shown in Table 12-53.

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Timer Control

Table 12-53. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2RST	W	0h	Channel 2 reset. 0h = No effect. 1h = Reset C2CC, PC2CC, and C2CFG.
9	C1RST	W	0h	Channel 1 reset. 0h = No effect. 1h = Reset C1CC, PC1CC, and C1CFG.
8	C0RST	W	0h	Channel 0 reset. 0h = No effect. 1h = Reset C0CC, PC0CC, and C0CFG.
7-6	RESERVED	R	0h	Reserved
5	INTP	R/W	0h	Interrupt Phase.;This bit field controls when the RIS.TGT and RIS.ZERO interrupts are set. 0h = RIS.TGT and RIS.ZERO are set one system clock cycle after CNTR = TARGET/ZERO. 1h = RIS.TGT and RIS.ZERO are set one timer clock cycle after CNTR = TARGET/ZERO.
4-3	CMPDIR	R/W	0h	Compare direction.;This bit field controls the direction the counter must have in order to set the RIS.CnCC channel interrupts. This bitfield is only relevant if [CnCFG.CCACT] is configured to a compare action. 0h = Compare RIS fields are set on up count and down count. 1h = Compare RIS fields are only set on up count. 2h = Compare RIS fields are only set on down count. 3h = RESERVED

Table 12-53. CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MODE	R/W	0h	Timer mode control;The CNTR restarts from 0 when MODE is written to UP_ONCE, UP_PER, UPDWN_PER, QDEC, SYNC_UP_ONCE, SYNC_UP_PER or SYNC_UPDWN_PER.;When writing MODE all internally queued updates to the channels and TGT is cleared.;When configuring the timer, MODE should be the last thing to configure. If changing timer configuration after MODE has been set is necessary, instructions, if any, given in the configuration registers should be followed. See for example C0CFG. 0h = Disable timer. Updates to counter, channels, and events stop. 1h = Count up once. The timer increments from 0 to target value, then stops and sets MODE to DIS. 2h = Count up periodically. The timer increments from 0 to target value, repeatedly.;Period = (target value + 1) * timer clock period 3h = Count up and down periodically. The timer counts from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period 4h = The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectivly as PHA, PHB and IDX inputs. IDX can be turned off by setting C2CFG.EDGE = NONE.;The timer clock frequency sets the sample rate of the QDEC logic. This frequency can be configured in PRECFG. 5h = Start counting up once synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_ONCE automatically. ;It then functions as a normal timer in CTL.MODE = UP_ONCE, incrementing from 0 to target value, then stops and sets MODE to DIS. 6h = Start counting up periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_PER automatically. ;It then operates as a normal timer in CTL.MODE = UP_PER, incrementing from 0 to target value, repeatedly.;Period = (target value * 2) * timer clock period 7h = Start counting up and down periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UPDWN_PER automatically. ;It then operates as a normal timer in CTL.MODE = UPDWN_PER, counting from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period

12.6.5 OUTCTL Register (Offset = 10h) [Reset = 00000000h]

OUTCTL is shown in Table 12-54.

Return to the Summary Table.

Output Control;Set and clear individual outputs manually. Manual update of an output takes priority over automatic channel updates to the same output. It is not possible to set and clear an output at the same time, such requests will be neglected.;An output can be automatically cleared, set, toggled, or pulsed by each channel, listed in decreasing order of priority. The action with highest priority happens when multiple channels want to update an output at the same time.;All outputs are connected to the event fabric and the IO controller. The outputs going to the IO controller have an aditional complementary output, this output is the inverted IO output. Both the IO and the IO complementary outputs are passed through an IO Controller, see IOCTL.

Table 12-54. OUTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	SETOUT2	W	0h	Set output 2.;Write 1 to set output 2.
4	CLROUT2	W	0h	Clear output 2.;Write 1 to clear output 2.
3	SETOUT1	W	0h	Set output 1.;Write 1 to set output 1.
2	CLROUT1	W	0h	Clear output 1.;Write 1 to clear output 1.
1	SETOUT0	W	0h	Set output 0.;Write 1 to set output 0.
0	CLROUT0	W	0h	Clear output 0.;Write 1 to clear output 0.

12.6.6 CNTR Register (Offset = 14h) [Reset = 00000000h]

CNTR is shown in Table 12-55.

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Counter;The counter of this timer. After CTL.MODE is set the counter updates at the rate specified in PRECFG.

Table 12-55. CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Current counter value.;If CTL.MODE = QDEC this can be used to set the initial counter value during QDEC. Writing to CNTR in other modes than QDEC is possible, but may result in unpredictable behavior.

12.6.7 PRECFG Register (Offset = 18h) [Reset = 00000000h]

PRECFG is shown in Table 12-56.

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Clock Prescaler Configuration;This register is used to set the timer clock period. The prescaler is a counter which counts down from the value TICKDIV. When the prescaler counter reaches zero, CNTR is updated. The field TICKDIV effectively divides the prescaler tick source. The timer clock frequency can be calculated as TICKSRC/(TICKDIV+1).

Table 12-56. PRECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	TICKDIV	R/W	0h	Tick division.;TICKDIV determines the timer clock frequency for the counter, and timer output updates. The timer clock frequency is the clock selected by TICKSRC divided by (TICKDIV + 1). This inverse is the timer clock period.;0x00: Divide by 1.;0x01: Divide by 2.;... ;0xFF: Divide by 256.
7-2	RESERVED	R	0h	Reserved
1-0	TICKSRC	R/W	0h	Prescaler tick source.;TICKSRC determines the source which decrements the prescaler. 0h = Prescaler is updated at the system clock. 1h = Prescaler is updated at the rising edge of TICKEN. 2h = Prescaler is updated at the falling edge of TICKEN. 3h = Prescaler is updated at both edges of TICKEN.

12.6.8 PREEVENT Register (Offset = 1Ch) [Reset = 00000000h]

PREEVENT is shown in Table 12-57.

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Prescaler Event;This register is used to output a logic high signal before the zero crossing of the prescaler counter. The output is routed to the IOC.

Table 12-57. PREEVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Sets the HIGH time of the prescaler event output. ;Event goes high when the prescaler counter equals VAL. Event goes low when prescaler counter is 0.;Note:;- Can be used to precharge or turn an external component on for a short time before sampling, like in QDEC.;- If there is a requirement to create such events that have very short periods compared to timer clock period, use two timers. One timer acts as prescaler and event generator for another timer.

12.6.9 CHFILT Register (Offset = 20h) [Reset = 00000000h]

CHFILT is shown in Table 12-58.

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Channel Input Filter;This register is used to configure the filter on the channel inputs. The configuration is for all inputs.;The filter is enabled when a channel is in capture mode.;The input to the filter is passed to the edge detection logic if LOAD + 1 consecutive input samples are equal. The filter functions as a down counter, counting down every input sample.;If two consecutive samples are unequal, the filter counter restarts from LOAD.;If the filter counter reaches zero, the input signal is valid and passed to the edge detection logic.;The channel filter should only be configured while the CTL.MODE = DIS. Configuring the filter while the timer is running can result in unexpected behavior.

Table 12-58. CHFILT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	LOAD	R/W	0h	The input of the channel filter is passed to the edge detection logic after LOAD + 1 consecutive equal samples.
7-2	RESERVED	R	0h	Reserved
1-0	MODE	R/W	0h	Channel filter mode 0h = Filter is bypassed. No Filter is used. 1h = Filter is clocked by system clock. 2h = Filter is clocked by PRECFG.TICKSRC. 3h = Filter is clocked by timer clock.

12.6.10 FAULT Register (Offset = 24h) [Reset = 00000000h]

FAULT is shown in Table 12-59.

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Fault;This register is used to configure the fault input logic. ;Primary use scenario is to select CTL before starting the timer. Follow these steps to configure CTL while CTL.MODE is different from DIS:;- Set C0CFG.EDGE to NONE. ;- Configure CTL.;- Wait for three system clock periods before setting C0CFG.EDGE different from NONE.;These steps prevent fault detection caused by expired signal values in synchronizers and edge-detection circuit.

Table 12-59. FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CTL	R/W	0h	Fault control;On active fault input the counter can optionally stop. If the counter stops this is done by hardware, software must then restart the timer if wanted. The fault input overrides channel 0 IOC input when CTL != DIS. ;This means that channel 0 receives fault as input signal when C0CFG.INPUT = IO and CTL != DIS. ;CHFILT can be used to avoid glitching on the fault input. Fault is level triggered, the polarity is set by the C0CFG.EDGE field. Here C0CFG.EDGE = RISE gives active high and C0CFG.EDGE = FALL gives active low polarity.;Fault is typically used together with PARK to stop the PWM signal to an external motor control circuit safely. Configure PARK to ensure predefined values of the PWM outputs.;If CTL != DIS the RIS.FAULT interrupt is set immediately when the fault input is active while CTL.MODE != DIS.;The three modes of fault is described below:;CTL = IMMEDIATE;In this mode the counter stops immediately on an active fault input. This is done by hardware by setting CTL.MODE = DIS. To start the counter software must set CTL.MODE != DIS.;When the counter has stopped, the input synchronizers and the channel filter is not running. This means that if RIS.FAULT is cleared it will not be set again while CTL.MODE = DIS. ;CTL = ZEROCOND;In this mode the counter stops when CNTR = 0 after an active fault input. If the RIS.FAULT interrupt has been cleared by software before CNTR = 0, and the fault input is inactive, the counter will continue as normal.;When the counter stops on zero, it can be started again by clearing the RIS.FAULT interrupt if the fault input is inactive. To change the counter mode set CTL.MODE = DIS, clear the RIS.FAULT interrupt, then start timer in wanted mode.;CTL = IRQ;In this mode only the RIS.FAULT flag is set on an active fault input. 0h = Disable. The timer ignores fault. 1h = Immediate reaction. The counter stops immediately on fault. 2h = Zero condition. The counter stops when CNTR = 0. 3h = Interrupt request. Only set RIS.FAULT on active fault.

12.6.11 PARK Register (Offset = 28h) [Reset = 00000000h]

PARK is shown in Table 12-60.

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Park;This register configures how the outputs should be set in Park mode. Park mode is either entered by debug halt or fault. Park mode is activated when the counter stops. Park mode is inactive when the counter starts. When park mode is active all outputs are set to their predefined states. ;For IO output signals which have enabled dead band, a dead band insertion will be done before switching to the predefined state.

Table 12-60. PARK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	IOCPS2	R/W	0h	IO Complementary Park State 2;Park state for IO Complementary output 2. 0h = Output is set low in park mode. 1h = Output is set high in park mode.
6	IOPS2	R/W	0h	IO Park State 2;Park state for IO output 2. 0h = Output is set low in park mode. 1h = Output is set high in park mode.
5	IOCPS1	R/W	0h	IO Complementary Park State 1;Park state for IO Complementary output 1. 0h = Output is set low in park mode. 1h = Output is set high in park mode.
4	IOPS1	R/W	0h	IO Park State 1;Park state for IO output 1. 0h = Output is set low in park mode. 1h = Output is set high in park mode.
3	IOCPS0	R/W	0h	IO Complementary Park State 0;Park state for IO Complementary output 0. 0h = Output is set low in park mode. 1h = Output is set high in park mode.
2	IOPS0	R/W	0h	IO Park State 0;Park state for IO output 0. 0h = Output is set low in park mode. 1h = Output is set high in park mode.
1-0	CTL	R/W	0h	Park Control. 0h = Disable park mode. 1h = Enter park mode on fault. 2h = Enter park mode on debug. 3h = Enter parkmode on fault or debug.

12.6.12 DBDLY Register (Offset = 2Ch) [Reset = 00000000h]

DBDLY is shown in Table 12-61.

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Dead Band Delay;This register is used to insert a dead band delay when generating complementary PWM signals. To enable dead band, on for example IO output 0, create a reference PWM signal on Output 0, then set DBCTL.IOC0 = EN.;TBD: 12-bit width fall delay and rise delay may be excessive, if 8-bits are enough we can join DBDLY and DBCTL.

Table 12-61. DBDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	FALLDLY	R/W	0h	Fall delay.;The number of system clock periods inserted between the fall of the dead band reference signal and the rise of the inverted output signal.
15-12	RESERVED	R	0h	Reserved
11-0	RISEDLY	R/W	0h	Rise delay.;The number of system clock periods inserted between the rise of the dead band reference signal and the rise of the output signal.

12.6.13 DBCTL Register (Offset = 30h) [Reset = 00000000h]

DBCTL is shown in Table 12-62.

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Dead Band Control;This register is used to enable dead band for IOC outputs.

Table 12-62. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	IO2	R/W	0h	Enable dead band on IO and IO complementary output 2. 0h = Disable 1h = Enable
1	IO1	R/W	0h	Enable dead band on IO and IO complementary output 1. 0h = Disable 1h = Enable
0	IO0	R/W	0h	Enable dead band on IO and IO complementary output 0. 0h = Disable 1h = Enable

12.6.14 DMA Register (Offset = 3Ch) [Reset = 00000000h]

DMA is shown in Table 12-63.

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Direct Memory Accsess;This register is used to enable DMA requests from the timer and set the register addresses which the DMA will access (read/write).;Choose DMA request source by setting the REQ field. The setting of the corresponding interrupt in the RIS registers also sets the DMA request. ;Upon a DMA request defined by REQ an internal address pointer is set to RWADDR*4. Every access to DMARW will increment the internal pointer by 4 such that the next DMA access will be to the next register.;The internal pointer will stop after RWCNTR increments. Further access will be ignored.

Table 12-63. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RWCNTR	R/W	0h	The read/write counter. RWCNTR+1 is the number of times the DMA can access (read/write) the DMARW register. For each DMA access to DMARW an internal counter is incremented, writing to the next address field. RWADDR + 4*RWCNTR is the final register address which can be accessed by the DMA.
15	RESERVED	R	0h	Reserved
14-8	RWADDR	R/W	0h	The base address which the DMA access when reading/writing DMARW. The base address is set by taking the 9 LSB of the physical address and divide by 4.;For example, if you wanted the RWADDR to point to the PTGT register you should set RWADDR = 0x0FC/4.
7-4	RESERVED	R	0h	Reserved
3-0	REQ	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates a DMA request. 2h = Setting of RIS.ZERO generates a DMA request. 3h = Setting of RIS.FAULT generates a DMA request. 4h = Setting of RIS.C0CC generates a DMA request. 5h = Setting of RIS.C1CC generates a DMA request. 6h = Setting of RIS.C2CC generates a DMA request. 7h = Setting of RIS.C3CC generates a DMA request. 8h = Setting of RIS.C4CC generates a DMA request. 9h = Setting of RIS.C5CC generates a DMA request. Ah = Setting of RIS.C6CC generates a DMA request. Bh = Setting of RIS.C7CC generates a DMA request. Ch = Setting of RIS.C8CC generates a DMA request. Dh = Setting of RIS.C9CC generates a DMA request. Eh = Setting of RIS.C10CC generates a DMA request. Fh = Setting of RIS.C11CC generates a DMA request.

12.6.15 DMARW Register (Offset = 40h) [Reset = 00000000h]

DMARW is shown in Table 12-64.

Return to the Summary Table.

Direct Memory Access;This register is used by the DMA to access (read/write) register inside this LGPT module.;Each access to this register will increment the internal DMA address counter. See DMA for description.

Table 12-64. DMARW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	DMA read write value.;The value that is read/written from/to the registers.

12.6.16 ADCTRG Register (Offset = 44h) [Reset = 00000000h]

ADCTRG is shown in Table 12-65.

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ADC Trigger;This register is used to enable ADC trigger from the timer. ;Choose ADC trigger source by setting the SRC field. The setting of the corresponding interrupt in the RIS registers also sets the ADC trigger.

Table 12-65. ADCTRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	SRC	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates an ADC trigger. 2h = Setting of RIS.ZERO generates an ADC trigger. 3h = Setting of RIS.FAULT generates an ADC trigger. 4h = Setting of RIS.C0CC generates an ADC trigger. 5h = Setting of RIS.C1CC generates an ADC trigger. 6h = Setting of RIS.C2CC generates an ADC trigger. 7h = Setting of RIS.C3CC generates an ADC trigger. 8h = Setting of RIS.C4CC generates an ADC trigger. 9h = Setting of RIS.C5CC generates an ADC trigger. Ah = Setting of RIS.C6CC generates an ADC trigger. Bh = Setting of RIS.C7CC generates an ADC trigger. Ch = Setting of RIS.C8CC generates an ADC trigger. Dh = Setting of RIS.C9CC generates an ADC trigger. Eh = Setting of RIS.C10CC generates an ADC trigger. Fh = Setting of RIS.C11CC generates an ADC trigger.

12.6.17 IOCTL Register (Offset = 48h) [Reset = 00000000h]

IOCTL is shown in Table 12-66.

Return to the Summary Table.

IO Controller;This register overrides the IO outputs.

Table 12-66. IOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-10	COUT2	R/W	0h	IO complementary output 2 control;This bit field controls IO complementary output 2. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
9-8	OUT2	R/W	0h	IO output 2 control;This bit field controls IO output 2. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
7-6	COUT1	R/W	0h	IO complementary output 1 control;This bit field controls IO complementary output 1. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
5-4	OUT1	R/W	0h	IO output 1 control;This bit field controls IO output 1. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
3-2	COUT0	R/W	0h	IO complementary output 0 control;This bit field controls IO complementary output 0. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
1-0	OUT0	R/W	0h	IO output 0 control;This bit field controls IO output 0. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.

12.6.18 IMASK Register (Offset = 68h) [Reset = 00000000h]

IMASK is shown in Table 12-67.

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Interrupt mask. ;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 12-67. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R/W	0h	Enable RIS.C2CC interrupt. 0h = Disable 1h = Enable
9	C1CC	R/W	0h	Enable RIS.C1CC interrupt. 0h = Disable 1h = Enable
8	C0CC	R/W	0h	Enable RIS.C0CC interrupt. 0h = Disable 1h = Enable
7	RESERVED	R	0h	Reserved
6	FAULT	R/W	0h	Enable RIS.FAULT interrupt. 0h = Disable 1h = Enable
5	IDX	R/W	0h	Enable RIS.IDX interrupt. 0h = Disable 1h = Enable
4	DIRCHNG	R/W	0h	Enable RIS.DIRCHNG interrupt. 0h = Disable 1h = Enable
3	CNTRCHNG	R/W	0h	Enable RIS.CNTRCHNG interrupt. 0h = Disable 1h = Enable
2	DBLTRANS	R/W	0h	Enable RIS.DBLTRANS interrupt. 0h = Disable 1h = Enable
1	ZERO	R/W	0h	Enable RIS.ZERO interrupt. 0h = Disable 1h = Enable
0	TGT	R/W	0h	Enable RIS.TGT interrupt. 0h = Disable 1h = Enable

12.6.19 RIS Register (Offset = 6Ch) [Reset = 00000000h]

RIS is shown in Table 12-68.

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Raw interrupt status. ;This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-68. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Status of the C2CC interrupt. The interrupt is set when C2CC has capture or compare event. 0h = Cleared 1h = Set
9	C1CC	R	0h	Status of the C1CC interrupt. The interrupt is set when C1CC has capture or compare event. 0h = Cleared 1h = Set
8	C0CC	R	0h	Status of the C0CC interrupt. The interrupt is set when C0CC has capture or compare event. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Status of the FAULT interrupt. The interrupt is set immediately on active fault input. 0h = Cleared 1h = Set
5	IDX	R	0h	Status of the IDX interrupt. The interrupt is set when IDX is active. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Status of the DIRCHNG interrupt. The interrupt is set when the direction of the counter changes. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Status of the CNTRCHNG interrupt. The interrupt is set when the counter increments or decrements. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Status of the DBLTRANS interrupt. The interrupt is set when a double transition has happened during QDEC mode. 0h = Cleared 1h = Set
1	ZERO	R	0h	Status of the ZERO interrupt. The interrupt is set when CNTR = 0. 0h = Cleared 1h = Set
0	TGT	R	0h	Status of the TGT interrupt. The interrupt is set when CNTR = TGT. 0h = Cleared 1h = Set

12.6.20 MIS Register (Offset = 70h) [Reset = 00000000h]

MIS is shown in Table 12-69.

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Masked interrupt status. ;This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-69. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Masked status of the RIS.C2CC interrupt. 0h = Cleared 1h = Set
9	C1CC	R	0h	Masked status of the RIS.C1CC interrupt. 0h = Cleared 1h = Set
8	C0CC	R	0h	Masked status of the RIS.C0CC interrupt. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Masked status of the RIS.FAULT interrupt. 0h = Cleared 1h = Set
5	IDX	R	0h	Masked status of the RIS.IDX interrupt. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Masked status of the RIS.DIRCHNG interrupt. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Masked status of the RIS.CNTRCHNG interrupt. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Masked status of the RIS.DBLTRANS interrupt. 0h = Cleared 1h = Set
1	ZERO	R	0h	Masked status of the RIS.ZERO interrupt. 0h = Cleared 1h = Set
0	TGT	R	0h	Masked status of the RIS.TGT interrupt. 0h = Cleared 1h = Set

12.6.21 ISET Register (Offset = 74h) [Reset = 00000000h]

ISET is shown in Table 12-70.

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Interrupt set register. ;This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 12-70. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the RIS.C2CC interrupt. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the RIS.C1CC interrupt. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the RIS.C0CC interrupt. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the RIS.FAULT interrupt. 0h = No effect 1h = Set
5	IDX	W	0h	Set the RIS.IDX interrupt. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the RIS.DIRCHNG interrupt. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the RIS.DBLTRANS interrupt. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the RIS.ZERO interrupt. 0h = No effect 1h = Set
0	TGT	W	0h	Set the RIS.TGT interrupt. 0h = No effect 1h = Set

12.6.22 ICLR Register (Offset = 78h) [Reset = 00000000h]

ICLR is shown in Table 12-71.

Return to the Summary Table.

Interrupt clear register. ;This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 12-71. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the RIS.C2CC interrupt. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the RIS.C1CC interrupt. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the RIS.C0CC interrupt. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the RIS.FAULT interrupt. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the RIS.IDX interrupt. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the RIS.DIRCHNG interrupt. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the RIS.DBLTRANS interrupt. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the RIS.ZERO interrupt. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the RIS.TGT interrupt. 0h = No effect 1h = Clear

12.6.23 IMSET Register (Offset = 7Ch) [Reset = 00000000h]

IMSET is shown in Table 12-72.

Return to the Summary Table.

Interrupt mask set register. ;Writing a 1 to a bit in this register will set the corresponding IMASK bit.

Table 12-72. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the MIS.C2CC mask. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the MIS.C1CC mask. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the MIS.C0CC mask. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the MIS.FAULT mask. 0h = No effect 1h = Set
5	IDX	W	0h	Set the MIS.IDX mask. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the MIS.DIRCHNG mask. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the MIS.CNTRCHNG mask. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the MIS.DBLTRANS mask. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the MIS.ZERO mask. 0h = No effect 1h = Set
0	TGT	W	0h	Set the MIS.TGT mask. 0h = No effect 1h = Set

12.6.24 IMCLR Register (Offset = 80h) [Reset = 00000000h]

IMCLR is shown in Table 12-73.

Return to the Summary Table.

Interrupt mask clear register. ;Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 12-73. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the MIS.C2CC mask. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the MIS.C1CC mask. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the MIS.C0CC mask. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the MIS.FAULT mask. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the MIS.IDX mask. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the MIS.DIRCHNG mask. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the MIS.CNTRCHNG mask. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the MIS.DBLTRANS mask. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the MIS.ZERO mask. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the MIS.TGT mask. 0h = No effect 1h = Clear

12.6.25 EMU Register (Offset = 84h) [Reset = 00000000h]

EMU is shown in Table 12-74.

Return to the Summary Table.

Debug control;This register can be used to freeze the timer when CPU halts when HALT is set to 1. When HALT is set to 0, or when the CPU releases debug halt, the filters and edge detection logic is flushed and the timer starts. For setting a predefined output value during a CPU debug halt, PARK, if the timer has this register, should be configured additionally. If this timer does not have the PARK register a predefined output value during CPU halt is not possible.

Table 12-74. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CTL	R/W	0h	Halt control.;Configure when the counter shall stop upon CPU halt. This bitfield only applies if HALT = 1. 0h = Immediate reaction. The counter stops immediately on debug halt. 1h = Zero condition. The counter stops when CNTR = 0.
0	HALT	R/W	0h	Halt LGPT when CPU is halted in debug. 0h = Disable. 1h = Enable.

12.6.26 C0CFG Register (Offset = C0h) [Reset = 00000000h]

C0CFG is shown in Table 12-75.

Return to the Summary Table.

Channel 0 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-75. C0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 2. 1h = Channel 0 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 1. 1h = Channel 0 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 0. 1h = Channel 0 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-75. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C0CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C0CC when C0CC.VAL contains signal period and PC0CC.VAL contains signal pulse width.;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C0CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-75. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C0CC.VAL / TGT.VAL).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle = C0CC.VAL / (TGT.VAL + 1).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.6.27 C1CFG Register (Offset = C4h) [Reset = 00000000h]

C1CFG is shown in Table 12-76.

Return to the Summary Table.

Channel 1 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-76. C1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 2. 1h = Channel 1 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 1. 1h = Channel 1 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 0. 1h = Channel 1 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-76. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C1CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C1CC when C1CC.VAL contains signal period and PC1CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C1CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-76. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C1CC.VAL / TGT.VAL).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle = C1CC.VAL / (TGT.VAL + 1).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.6.28 C2CFG Register (Offset = C8h) [Reset = 00000000h]

C2CFG is shown in Table 12-77.

Return to the Summary Table.

Channel 2 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-77. C2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 2. 1h = Channel 2 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 1. 1h = Channel 2 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 0. 1h = Channel 2 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-77. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C2CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C2CC when C2CC.VAL contains signal period and PC2CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C2CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-77. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C2CC.VAL / TGT.VAL).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle = C2CC.VAL / (TGT.VAL + 1).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.6.29 PTGT Register (Offset = FCh) [Reset = 00000000h]

PTGT is shown in Table 12-78.

Return to the Summary Table.

Pipeline Target;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer will copy PTGT.VAL to TGT.VAL on the upcoming CNTR zero crossing only if PTGT.VAL has been written. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC;The CNTR value is updated with VALUE on IDX if the counter is counting down. If the counter is counting up, CNTR is loaded with zero on IDX.;In this mode the VALUE is not loaded into TGT on zero crossing.

Table 12-78. PTGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	The pipleline target value.

12.6.30 PC0CC Register (Offset = 100h) [Reset = 00000000h]

PC0CC is shown in Table 12-79.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare

Table 12-79. PC0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.6.31 PC1CC Register (Offset = 104h) [Reset = 00000000h]

PC1CC is shown in Table 12-80.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare

Table 12-80. PC1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.6.32 PC2CC Register (Offset = 108h) [Reset = 00000000h]

PC2CC is shown in Table 12-81.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare

Table 12-81. PC2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.6.33 TGT Register (Offset = 13Ch) [Reset = 00000000h]

TGT is shown in Table 12-82.

Return to the Summary Table.

Target;User defined counter target. ;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.

Table 12-82. TGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	FFFFh	User defined counter target value.

12.6.34 C0CC Register (Offset = 140h) [Reset = 00000000h]

C0CC is shown in Table 12-83.

Return to the Summary Table.

Channel 0 Capture Compare

Table 12-83. C0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.6.35 C1CC Register (Offset = 144h) [Reset = 00000000h]

C1CC is shown in Table 12-84.

Return to the Summary Table.

Channel 1 Capture Compare

Table 12-84. C1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.6.36 C2CC Register (Offset = 148h) [Reset = 00000000h]

C2CC is shown in Table 12-85.

Return to the Summary Table.

Channel 2 Capture Compare

Table 12-85. C2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.6.37 PTGTNC Register (Offset = 17Ch) [Reset = 00000000h]

PTGTNC is shown in Table 12-86.

Return to the Summary Table.

Pipeline Target No Clear;Use this register to read or write to PTGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-86. PTGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	A read or write to this register will not clear the RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer copies VAL to TGT.VAL when CNTR.VAL becomes 0. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC.;The CNTR.VAL is updated with VAL on IDX. VAL is not loaded into TGT.VAL when CNTR.VAL becomes 0.

12.6.38 PC0CCNC Register (Offset = 180h) [Reset = 00000000h]

PC0CCNC is shown in Table 12-87.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare No Clear

Table 12-87. PC0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.6.39 PC1CCNC Register (Offset = 184h) [Reset = 00000000h]

PC1CCNC is shown in Table 12-88.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare No Clear

Table 12-88. PC1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.6.40 PC2CCNC Register (Offset = 188h) [Reset = 00000000h]

PC2CCNC is shown in Table 12-89.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare No Clear

Table 12-89. PC2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.6.41 TGTNC Register (Offset = 1BCh) [Reset = 00000000h]

TGTNC is shown in Table 12-90.

Return to the Summary Table.

Target No Clear;Use this register to read or write to TGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-90. TGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	FFFFh	User defined counter target value.

12.6.42 C0CCNC Register (Offset = 1C0h) [Reset = 00000000h]

C0CCNC is shown in Table 12-91.

Return to the Summary Table.

Channel 0 Capture Compare No Clear

Table 12-91. C0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.6.43 C1CCNC Register (Offset = 1C4h) [Reset = 00000000h]

C1CCNC is shown in Table 12-92.

Return to the Summary Table.

Channel 1 Capture Compare No Clear

Table 12-92. C1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.6.44 C2CCNC Register (Offset = 1C8h) [Reset = 00000000h]

C2CCNC is shown in Table 12-93.

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Channel 2 Capture Compare No Clear

Table 12-93. C2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.7 LGPT2 Registers

Table 12-94 lists the memory-mapped registers for the LGPT2 registers. All register offset addresses not listed in Table 12-94 should be considered as reserved locations and the register contents should not be modified.

Table 12-94. LGPT2 Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 12.7.1
4h	DESCEX	Description Extended	Section 12.7.2
8h	STARTCFG	Start Configuration	Section 12.7.3
Ch	CTL	Timer Control	Section 12.7.4
10h	OUTCTL	Output Control	Section 12.7.5
14h	CNTR	Counter	Section 12.7.6
18h	PRECFG	Clock Prescaler Configuration	Section 12.7.7
1Ch	PREEVENT	Prescaler Event	Section 12.7.8
20h	CHFILT	Channel Input Filter	Section 12.7.9
34h	QDECSTAT	Quadrature Decoder Status	Section 12.7.10
3Ch	DMA	Direct Memory Accsess	Section 12.7.11
40h	DMARW	Direct Memory Access	Section 12.7.12
44h	ADCTRG	ADC Trigger	Section 12.7.13
48h	IOCTL	IO Controller	Section 12.7.14
68h	IMASK	Interrupt mask.	Section 12.7.15
6Ch	RIS	Raw interrupt status.	Section 12.7.16
70h	MIS	Masked interrupt status.	Section 12.7.17
74h	ISET	Interrupt set register.	Section 12.7.18
78h	ICLR	Interrupt clear register.	Section 12.7.19
7Ch	IMSET	Interrupt mask set register.	Section 12.7.20
80h	IMCLR	Interrupt mask clear register.	Section 12.7.21
84h	EMU	Debug control	Section 12.7.22
C0h	C0CFG	Channel 0 Configuration	Section 12.7.23
C4h	C1CFG	Channel 1 Configuration	Section 12.7.24
C8h	C2CFG	Channel 2 Configuration	Section 12.7.25
FCh	PTGT	Pipeline Target	Section 12.7.26
100h	PC0CC	Pipeline Channel 0 Capture Compare	Section 12.7.27
104h	PC1CC	Pipeline Channel 1 Capture Compare	Section 12.7.28
108h	PC2CC	Pipeline Channel 2 Capture Compare	Section 12.7.29
13Ch	TGT	Target	Section 12.7.30
140h	C0CC	Channel 0 Capture Compare	Section 12.7.31
144h	C1CC	Channel 1 Capture Compare	Section 12.7.32
148h	C2CC	Channel 2 Capture Compare	Section 12.7.33
17Ch	PTGTNC	Pipeline Target No Clear	Section 12.7.34
180h	PC0CCNC	Pipeline Channel 0 Capture Compare No Clear	Section 12.7.35
184h	PC1CCNC	Pipeline Channel 1 Capture Compare No Clear	Section 12.7.36
188h	PC2CCNC	Pipeline Channel 2 Capture Compare No Clear	Section 12.7.37
1BCh	TGTNC	Target No Clear	Section 12.7.38
1C0h	C0CCNC	Channel 0 Capture Compare No Clear	Section 12.7.39
1C4h	C1CCNC	Channel 1 Capture Compare No Clear	Section 12.7.40
1C8h	C2CCNC	Channel 2 Capture Compare No Clear	Section 12.7.41

Complex bit access types are encoded to fit into small table cells. Table 12-95 shows the codes that are used for access types in this section.

Table 12-95. LGPT2 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

12.7.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 12-96.

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Description Register.;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 12-96. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	DE49h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number.
7-4	MAJREV	R	1h	Major revision of IP.
3-0	MINREV	R	1h	Minor revision of IP.

12.7.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 12-97.

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Description Extended;This register describes the parameters of the LGPT.

Table 12-97. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	HIR	R	0h	Has IR logic.
18	HDBF	R	0h	Has Dead-Band, Fault, and Park logic.
17-14	PREW	R	8h	Prescale width. The prescaler can maximum be configured to 2^{PREW}-1.
13	HQDEC	R	1h	Has Quadrature Decoder.
12	HCIF	R	1h	Has channel input filter.
11-8	CIFS	R	8h	Channel input filter size. The prevailing state filter can maximum be configured to 2^{CIFS}-1.
7	HDMA	R	1h	Has uDMA output and logic.
6	HINT	R	1h	Has interrupt output and logic.
5-4	CNTRW	R	0h	Counter bit-width.;The maximum counter value is equal to 2^{CNTRW}-1. 0h = 16-bit counter. 1h = 24-bit counter. 2h = 32-bit counter. 3h = RESERVED
3-0	NCH	R	3h	Number of channels.

12.7.3 STARTCFG Register (Offset = 8h) [Reset = 00000000h]

STARTCFG is shown in Table 12-98.

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Start Configuration;This register is only for when CTL.MODE is configured to one of the SYNC modes.;This register defines when this LGPT starts.

Table 12-98. STARTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LGPT0	R/W	0h	LGPT start

12.7.4 CTL Register (Offset = Ch) [Reset = 00000000h]

CTL is shown in Table 12-99.

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Timer Control

Table 12-99. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2RST	W	0h	Channel 2 reset. 0h = No effect. 1h = Reset C2CC, PC2CC, and C2CFG.
9	C1RST	W	0h	Channel 1 reset. 0h = No effect. 1h = Reset C1CC, PC1CC, and C1CFG.
8	C0RST	W	0h	Channel 0 reset. 0h = No effect. 1h = Reset C0CC, PC0CC, and C0CFG.
7-6	RESERVED	R	0h	Reserved
5	INTP	R/W	0h	Interrupt Phase.;This bit field controls when the RIS.TGT and RIS.ZERO interrupts are set. 0h = RIS.TGT and RIS.ZERO are set one system clock cycle after CNTR = TARGET/ZERO. 1h = RIS.TGT and RIS.ZERO are set one timer clock cycle after CNTR = TARGET/ZERO.
4-3	CMPDIR	R/W	0h	Compare direction.;This bit field controls the direction the counter must have in order to set the RIS.CnCC channel interrupts. This bitfield is only relevant if [CnCFG.CCACT] is configured to a compare action. 0h = Compare RIS fields are set on up count and down count. 1h = Compare RIS fields are only set on up count. 2h = Compare RIS fields are only set on down count. 3h = RESERVED

Table 12-99. CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MODE	R/W	0h	Timer mode control;The CNTR restarts from 0 when MODE is written to UP_ONCE, UP_PER, UPDWN_PER, QDEC, SYNC_UP_ONCE, SYNC_UP_PER or SYNC_UPDWN_PER.;When writing MODE all internally queued updates to the channels and TGT is cleared.;When configuring the timer, MODE should be the last thing to configure. If changing timer configuration after MODE has been set is necessary, instructions, if any, given in the configuration registers should be followed. See for example C0CFG. 0h = Disable timer. Updates to counter, channels, and events stop. 1h = Count up once. The timer increments from 0 to target value, then stops and sets MODE to DIS. 2h = Count up periodically. The timer increments from 0 to target value, repeatedly.;Period = (target value + 1) * timer clock period 3h = Count up and down periodically. The timer counts from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period 4h = The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectivly as PHA, PHB and IDX inputs. IDX can be turned off by setting C2CFG.EDGE = NONE.;The timer clock frequency sets the sample rate of the QDEC logic. This frequency can be configured in PRECFG. 5h = Start counting up once synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_ONCE automatically. ;It then functions as a normal timer in CTL.MODE = UP_ONCE, incrementing from 0 to target value, then stops and sets MODE to DIS. 6h = Start counting up periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_PER automatically. ;It then operates as a normal timer in CTL.MODE = UP_PER, incrementing from 0 to target value, repeatedly.;Period = (target value * 2) * timer clock period 7h = Start counting up and down periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UPDWN_PER automatically. ;It then operates as a normal timer in CTL.MODE = UPDWN_PER, counting from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period

12.7.5 OUTCTL Register (Offset = 10h) [Reset = 00000000h]

OUTCTL is shown in Table 12-100.

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Output Control;Set and clear individual outputs manually. Manual update of an output takes priority over automatic channel updates to the same output. It is not possible to set and clear an output at the same time, such requests will be neglected.;An output can be automatically cleared, set, toggled, or pulsed by each channel, listed in decreasing order of priority. The action with highest priority happens when multiple channels want to update an output at the same time.;All outputs are connected to the event fabric and the IO controller. The outputs going to the IO controller have an aditional complementary output, this output is the inverted IO output. Both the IO and the IO complementary outputs are passed through an IO Controller, see IOCTL.

Table 12-100. OUTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	SETOUT2	W	0h	Set output 2.;Write 1 to set output 2.
4	CLROUT2	W	0h	Clear output 2.;Write 1 to clear output 2.
3	SETOUT1	W	0h	Set output 1.;Write 1 to set output 1.
2	CLROUT1	W	0h	Clear output 1.;Write 1 to clear output 1.
1	SETOUT0	W	0h	Set output 0.;Write 1 to set output 0.
0	CLROUT0	W	0h	Clear output 0.;Write 1 to clear output 0.

12.7.6 CNTR Register (Offset = 14h) [Reset = 00000000h]

CNTR is shown in Table 12-101.

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Counter;The counter of this timer. After CTL.MODE is set the counter updates at the rate specified in PRECFG.

Table 12-101. CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Current counter value.;If CTL.MODE = QDEC this can be used to set the initial counter value during QDEC. Writing to CNTR in other modes than QDEC is possible, but may result in unpredictable behavior.

12.7.7 PRECFG Register (Offset = 18h) [Reset = 00000000h]

PRECFG is shown in Table 12-102.

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Clock Prescaler Configuration;This register is used to set the timer clock period. The prescaler is a counter which counts down from the value TICKDIV. When the prescaler counter reaches zero, CNTR is updated. The field TICKDIV effectively divides the prescaler tick source. The timer clock frequency can be calculated as TICKSRC/(TICKDIV+1).

Table 12-102. PRECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	TICKDIV	R/W	0h	Tick division.;TICKDIV determines the timer clock frequency for the counter, and timer output updates. The timer clock frequency is the clock selected by TICKSRC divided by (TICKDIV + 1). This inverse is the timer clock period.;0x00: Divide by 1.;0x01: Divide by 2.;... ;0xFF: Divide by 256.
7-2	RESERVED	R	0h	Reserved
1-0	TICKSRC	R/W	0h	Prescaler tick source.;TICKSRC determines the source which decrements the prescaler. 0h = Prescaler is updated at the system clock. 1h = Prescaler is updated at the rising edge of TICKEN. 2h = Prescaler is updated at the falling edge of TICKEN. 3h = Prescaler is updated at both edges of TICKEN.

12.7.8 PREEVENT Register (Offset = 1Ch) [Reset = 00000000h]

PREEVENT is shown in Table 12-103.

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Prescaler Event;This register is used to output a logic high signal before the zero crossing of the prescaler counter. The output is routed to the IOC.

Table 12-103. PREEVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Sets the HIGH time of the prescaler event output. ;Event goes high when the prescaler counter equals VAL. Event goes low when prescaler counter is 0.;Note:;- Can be used to precharge or turn an external component on for a short time before sampling, like in QDEC.;- If there is a requirement to create such events that have very short periods compared to timer clock period, use two timers. One timer acts as prescaler and event generator for another timer.

12.7.9 CHFILT Register (Offset = 20h) [Reset = 00000000h]

CHFILT is shown in Table 12-104.

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Channel Input Filter;This register is used to configure the filter on the channel inputs. The configuration is for all inputs.;The filter is enabled when a channel is in capture mode.;The input to the filter is passed to the edge detection logic if LOAD + 1 consecutive input samples are equal. The filter functions as a down counter, counting down every input sample.;If two consecutive samples are unequal, the filter counter restarts from LOAD.;If the filter counter reaches zero, the input signal is valid and passed to the edge detection logic.;The channel filter should only be configured while the CTL.MODE = DIS. Configuring the filter while the timer is running can result in unexpected behavior.

Table 12-104. CHFILT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	LOAD	R/W	0h	The input of the channel filter is passed to the edge detection logic after LOAD + 1 consecutive equal samples.
7-2	RESERVED	R	0h	Reserved
1-0	MODE	R/W	0h	Channel filter mode 0h = Filter is bypassed. No Filter is used. 1h = Filter is clocked by system clock. 2h = Filter is clocked by PRECFG.TICKSRC. 3h = Filter is clocked by timer clock.

12.7.10 QDECSTAT Register (Offset = 34h) [Reset = 00000000h]

QDECSTAT is shown in Table 12-105.

Return to the Summary Table.

Quadrature Decoder Status;This register can be used during QDEC mode to check the status of the quadrature decoder.

Table 12-105. QDECSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	DBLTRANS	R	0h	Double transition 0h = Single or no transition on phase inputs. 1h = Double transition on phase inputs.
0	QDIR	R	0h	Direction of count during QDEC mode. 0h = Up (PHA leads PHB) 1h = Down (PHB leads PHA)

12.7.11 DMA Register (Offset = 3Ch) [Reset = 00000000h]

DMA is shown in Table 12-106.

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Direct Memory Accsess;This register is used to enable DMA requests from the timer and set the register addresses which the DMA will access (read/write).;Choose DMA request source by setting the REQ field. The setting of the corresponding interrupt in the RIS registers also sets the DMA request. ;Upon a DMA request defined by REQ an internal address pointer is set to RWADDR*4. Every access to DMARW will increment the internal pointer by 4 such that the next DMA access will be to the next register.;The internal pointer will stop after RWCNTR increments. Further access will be ignored.

Table 12-106. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RWCNTR	R/W	0h	The read/write counter. RWCNTR+1 is the number of times the DMA can access (read/write) the DMARW register. For each DMA access to DMARW an internal counter is incremented, writing to the next address field. RWADDR + 4*RWCNTR is the final register address which can be accessed by the DMA.
15	RESERVED	R	0h	Reserved
14-8	RWADDR	R/W	0h	The base address which the DMA access when reading/writing DMARW. The base address is set by taking the 9 LSB of the physical address and divide by 4.;For example, if you wanted the RWADDR to point to the PTGT register you should set RWADDR = 0x0FC/4.
7-4	RESERVED	R	0h	Reserved
3-0	REQ	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates a DMA request. 2h = Setting of RIS.ZERO generates a DMA request. 3h = Setting of RIS.FAULT generates a DMA request. 4h = Setting of RIS.C0CC generates a DMA request. 5h = Setting of RIS.C1CC generates a DMA request. 6h = Setting of RIS.C2CC generates a DMA request. 7h = Setting of RIS.C3CC generates a DMA request. 8h = Setting of RIS.C4CC generates a DMA request. 9h = Setting of RIS.C5CC generates a DMA request. Ah = Setting of RIS.C6CC generates a DMA request. Bh = Setting of RIS.C7CC generates a DMA request. Ch = Setting of RIS.C8CC generates a DMA request. Dh = Setting of RIS.C9CC generates a DMA request. Eh = Setting of RIS.C10CC generates a DMA request. Fh = Setting of RIS.C11CC generates a DMA request.

12.7.12 DMARW Register (Offset = 40h) [Reset = 00000000h]

DMARW is shown in Table 12-107.

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Direct Memory Access;This register is used by the DMA to access (read/write) register inside this LGPT module.;Each access to this register will increment the internal DMA address counter. See DMA for description.

Table 12-107. DMARW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	DMA read write value.;The value that is read/written from/to the registers.

12.7.13 ADCTRG Register (Offset = 44h) [Reset = 00000000h]

ADCTRG is shown in Table 12-108.

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ADC Trigger;This register is used to enable ADC trigger from the timer. ;Choose ADC trigger source by setting the SRC field. The setting of the corresponding interrupt in the RIS registers also sets the ADC trigger.

Table 12-108. ADCTRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	SRC	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates an ADC trigger. 2h = Setting of RIS.ZERO generates an ADC trigger. 3h = Setting of RIS.FAULT generates an ADC trigger. 4h = Setting of RIS.C0CC generates an ADC trigger. 5h = Setting of RIS.C1CC generates an ADC trigger. 6h = Setting of RIS.C2CC generates an ADC trigger. 7h = Setting of RIS.C3CC generates an ADC trigger. 8h = Setting of RIS.C4CC generates an ADC trigger. 9h = Setting of RIS.C5CC generates an ADC trigger. Ah = Setting of RIS.C6CC generates an ADC trigger. Bh = Setting of RIS.C7CC generates an ADC trigger. Ch = Setting of RIS.C8CC generates an ADC trigger. Dh = Setting of RIS.C9CC generates an ADC trigger. Eh = Setting of RIS.C10CC generates an ADC trigger. Fh = Setting of RIS.C11CC generates an ADC trigger.

12.7.14 IOCTL Register (Offset = 48h) [Reset = 00000000h]

IOCTL is shown in Table 12-109.

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IO Controller;This register overrides the IO outputs.

Table 12-109. IOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-10	COUT2	R/W	0h	IO complementary output 2 control;This bit field controls IO complementary output 2. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
9-8	OUT2	R/W	0h	IO output 2 control;This bit field controls IO output 2. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
7-6	COUT1	R/W	0h	IO complementary output 1 control;This bit field controls IO complementary output 1. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
5-4	OUT1	R/W	0h	IO output 1 control;This bit field controls IO output 1. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
3-2	COUT0	R/W	0h	IO complementary output 0 control;This bit field controls IO complementary output 0. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
1-0	OUT0	R/W	0h	IO output 0 control;This bit field controls IO output 0. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.

12.7.15 IMASK Register (Offset = 68h) [Reset = 00000000h]

IMASK is shown in Table 12-110.

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Interrupt mask. ;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 12-110. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R/W	0h	Enable RIS.C2CC interrupt. 0h = Disable 1h = Enable
9	C1CC	R/W	0h	Enable RIS.C1CC interrupt. 0h = Disable 1h = Enable
8	C0CC	R/W	0h	Enable RIS.C0CC interrupt. 0h = Disable 1h = Enable
7	RESERVED	R	0h	Reserved
6	FAULT	R/W	0h	Enable RIS.FAULT interrupt. 0h = Disable 1h = Enable
5	IDX	R/W	0h	Enable RIS.IDX interrupt. 0h = Disable 1h = Enable
4	DIRCHNG	R/W	0h	Enable RIS.DIRCHNG interrupt. 0h = Disable 1h = Enable
3	CNTRCHNG	R/W	0h	Enable RIS.CNTRCHNG interrupt. 0h = Disable 1h = Enable
2	DBLTRANS	R/W	0h	Enable RIS.DBLTRANS interrupt. 0h = Disable 1h = Enable
1	ZERO	R/W	0h	Enable RIS.ZERO interrupt. 0h = Disable 1h = Enable
0	TGT	R/W	0h	Enable RIS.TGT interrupt. 0h = Disable 1h = Enable

12.7.16 RIS Register (Offset = 6Ch) [Reset = 00000000h]

RIS is shown in Table 12-111.

Return to the Summary Table.

Raw interrupt status. ;This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-111. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Status of the C2CC interrupt. The interrupt is set when C2CC has capture or compare event. 0h = Cleared 1h = Set
9	C1CC	R	0h	Status of the C1CC interrupt. The interrupt is set when C1CC has capture or compare event. 0h = Cleared 1h = Set
8	C0CC	R	0h	Status of the C0CC interrupt. The interrupt is set when C0CC has capture or compare event. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Status of the FAULT interrupt. The interrupt is set immediately on active fault input. 0h = Cleared 1h = Set
5	IDX	R	0h	Status of the IDX interrupt. The interrupt is set when IDX is active. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Status of the DIRCHNG interrupt. The interrupt is set when the direction of the counter changes. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Status of the CNTRCHNG interrupt. The interrupt is set when the counter increments or decrements. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Status of the DBLTRANS interrupt. The interrupt is set when a double transition has happened during QDEC mode. 0h = Cleared 1h = Set
1	ZERO	R	0h	Status of the ZERO interrupt. The interrupt is set when CNTR = 0. 0h = Cleared 1h = Set
0	TGT	R	0h	Status of the TGT interrupt. The interrupt is set when CNTR = TGT. 0h = Cleared 1h = Set

12.7.17 MIS Register (Offset = 70h) [Reset = 00000000h]

MIS is shown in Table 12-112.

Return to the Summary Table.

Masked interrupt status. ;This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-112. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Masked status of the RIS.C2CC interrupt. 0h = Cleared 1h = Set
9	C1CC	R	0h	Masked status of the RIS.C1CC interrupt. 0h = Cleared 1h = Set
8	C0CC	R	0h	Masked status of the RIS.C0CC interrupt. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Masked status of the RIS.FAULT interrupt. 0h = Cleared 1h = Set
5	IDX	R	0h	Masked status of the RIS.IDX interrupt. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Masked status of the RIS.DIRCHNG interrupt. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Masked status of the RIS.CNTRCHNG interrupt. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Masked status of the RIS.DBLTRANS interrupt. 0h = Cleared 1h = Set
1	ZERO	R	0h	Masked status of the RIS.ZERO interrupt. 0h = Cleared 1h = Set
0	TGT	R	0h	Masked status of the RIS.TGT interrupt. 0h = Cleared 1h = Set

12.7.18 ISET Register (Offset = 74h) [Reset = 00000000h]

ISET is shown in Table 12-113.

Return to the Summary Table.

Interrupt set register. ;This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 12-113. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the RIS.C2CC interrupt. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the RIS.C1CC interrupt. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the RIS.C0CC interrupt. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the RIS.FAULT interrupt. 0h = No effect 1h = Set
5	IDX	W	0h	Set the RIS.IDX interrupt. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the RIS.DIRCHNG interrupt. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the RIS.DBLTRANS interrupt. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the RIS.ZERO interrupt. 0h = No effect 1h = Set
0	TGT	W	0h	Set the RIS.TGT interrupt. 0h = No effect 1h = Set

12.7.19 ICLR Register (Offset = 78h) [Reset = 00000000h]

ICLR is shown in Table 12-114.

Return to the Summary Table.

Interrupt clear register. ;This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 12-114. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the RIS.C2CC interrupt. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the RIS.C1CC interrupt. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the RIS.C0CC interrupt. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the RIS.FAULT interrupt. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the RIS.IDX interrupt. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the RIS.DIRCHNG interrupt. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the RIS.DBLTRANS interrupt. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the RIS.ZERO interrupt. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the RIS.TGT interrupt. 0h = No effect 1h = Clear

12.7.20 IMSET Register (Offset = 7Ch) [Reset = 00000000h]

IMSET is shown in Table 12-115.

Return to the Summary Table.

Interrupt mask set register. ;Writing a 1 to a bit in this register will set the corresponding IMASK bit.

Table 12-115. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the MIS.C2CC mask. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the MIS.C1CC mask. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the MIS.C0CC mask. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the MIS.FAULT mask. 0h = No effect 1h = Set
5	IDX	W	0h	Set the MIS.IDX mask. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the MIS.DIRCHNG mask. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the MIS.CNTRCHNG mask. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the MIS.DBLTRANS mask. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the MIS.ZERO mask. 0h = No effect 1h = Set
0	TGT	W	0h	Set the MIS.TGT mask. 0h = No effect 1h = Set

12.7.21 IMCLR Register (Offset = 80h) [Reset = 00000000h]

IMCLR is shown in Table 12-116.

Return to the Summary Table.

Interrupt mask clear register. ;Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 12-116. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the MIS.C2CC mask. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the MIS.C1CC mask. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the MIS.C0CC mask. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the MIS.FAULT mask. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the MIS.IDX mask. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the MIS.DIRCHNG mask. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the MIS.CNTRCHNG mask. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the MIS.DBLTRANS mask. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the MIS.ZERO mask. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the MIS.TGT mask. 0h = No effect 1h = Clear

12.7.22 EMU Register (Offset = 84h) [Reset = 00000000h]

EMU is shown in Table 12-117.

Return to the Summary Table.

Debug control;This register can be used to freeze the timer when CPU halts when HALT is set to 1. When HALT is set to 0, or when the CPU releases debug halt, the filters and edge detection logic is flushed and the timer starts. For setting a predefined output value during a CPU debug halt, PARK, if the timer has this register, should be configured additionally. If this timer does not have the PARK register a predefined output value during CPU halt is not possible.

Table 12-117. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CTL	R/W	0h	Halt control.;Configure when the counter shall stop upon CPU halt. This bitfield only applies if HALT = 1. 0h = Immediate reaction. The counter stops immediately on debug halt. 1h = Zero condition. The counter stops when CNTR = 0.
0	HALT	R/W	0h	Halt LGPT when CPU is halted in debug. 0h = Disable. 1h = Enable.

12.7.23 C0CFG Register (Offset = C0h) [Reset = 00000000h]

C0CFG is shown in Table 12-118.

Return to the Summary Table.

Channel 0 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-118. C0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 2. 1h = Channel 0 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 1. 1h = Channel 0 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 0. 1h = Channel 0 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-118. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C0CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C0CC when C0CC.VAL contains signal period and PC0CC.VAL contains signal pulse width.;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C0CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-118. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C0CC.VAL / TGT.VAL).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle = C0CC.VAL / (TGT.VAL + 1).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.7.24 C1CFG Register (Offset = C4h) [Reset = 00000000h]

C1CFG is shown in Table 12-119.

Return to the Summary Table.

Channel 1 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-119. C1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 2. 1h = Channel 1 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 1. 1h = Channel 1 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 0. 1h = Channel 1 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-119. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C1CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C1CC when C1CC.VAL contains signal period and PC1CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C1CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-119. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C1CC.VAL / TGT.VAL).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle = C1CC.VAL / (TGT.VAL + 1).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.7.25 C2CFG Register (Offset = C8h) [Reset = 00000000h]

C2CFG is shown in Table 12-120.

Return to the Summary Table.

Channel 2 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-120. C2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 2. 1h = Channel 2 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 1. 1h = Channel 2 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 0. 1h = Channel 2 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-120. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C2CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C2CC when C2CC.VAL contains signal period and PC2CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C2CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-120. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C2CC.VAL / TGT.VAL).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle = C2CC.VAL / (TGT.VAL + 1).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.7.26 PTGT Register (Offset = FCh) [Reset = 00000000h]

PTGT is shown in Table 12-121.

Return to the Summary Table.

Pipeline Target;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer will copy PTGT.VAL to TGT.VAL on the upcoming CNTR zero crossing only if PTGT.VAL has been written. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC;The CNTR value is updated with VALUE on IDX if the counter is counting down. If the counter is counting up, CNTR is loaded with zero on IDX.;In this mode the VALUE is not loaded into TGT on zero crossing.

Table 12-121. PTGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	The pipleline target value.

12.7.27 PC0CC Register (Offset = 100h) [Reset = 00000000h]

PC0CC is shown in Table 12-122.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare

Table 12-122. PC0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.7.28 PC1CC Register (Offset = 104h) [Reset = 00000000h]

PC1CC is shown in Table 12-123.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare

Table 12-123. PC1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.7.29 PC2CC Register (Offset = 108h) [Reset = 00000000h]

PC2CC is shown in Table 12-124.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare

Table 12-124. PC2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.7.30 TGT Register (Offset = 13Ch) [Reset = 00000000h]

TGT is shown in Table 12-125.

Return to the Summary Table.

Target;User defined counter target. ;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.

Table 12-125. TGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	FFFFh	User defined counter target value.

12.7.31 C0CC Register (Offset = 140h) [Reset = 00000000h]

C0CC is shown in Table 12-126.

Return to the Summary Table.

Channel 0 Capture Compare

Table 12-126. C0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.7.32 C1CC Register (Offset = 144h) [Reset = 00000000h]

C1CC is shown in Table 12-127.

Return to the Summary Table.

Channel 1 Capture Compare

Table 12-127. C1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.7.33 C2CC Register (Offset = 148h) [Reset = 00000000h]

C2CC is shown in Table 12-128.

Return to the Summary Table.

Channel 2 Capture Compare

Table 12-128. C2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.7.34 PTGTNC Register (Offset = 17Ch) [Reset = 00000000h]

PTGTNC is shown in Table 12-129.

Return to the Summary Table.

Pipeline Target No Clear;Use this register to read or write to PTGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-129. PTGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	A read or write to this register will not clear the RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer copies VAL to TGT.VAL when CNTR.VAL becomes 0. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC.;The CNTR.VAL is updated with VAL on IDX. VAL is not loaded into TGT.VAL when CNTR.VAL becomes 0.

12.7.35 PC0CCNC Register (Offset = 180h) [Reset = 00000000h]

PC0CCNC is shown in Table 12-130.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare No Clear

Table 12-130. PC0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.7.36 PC1CCNC Register (Offset = 184h) [Reset = 00000000h]

PC1CCNC is shown in Table 12-131.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare No Clear

Table 12-131. PC1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.7.37 PC2CCNC Register (Offset = 188h) [Reset = 00000000h]

PC2CCNC is shown in Table 12-132.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare No Clear

Table 12-132. PC2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.7.38 TGTNC Register (Offset = 1BCh) [Reset = 00000000h]

TGTNC is shown in Table 12-133.

Return to the Summary Table.

Target No Clear;Use this register to read or write to TGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-133. TGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	FFFFh	User defined counter target value.

12.7.39 C0CCNC Register (Offset = 1C0h) [Reset = 00000000h]

C0CCNC is shown in Table 12-134.

Return to the Summary Table.

Channel 0 Capture Compare No Clear

Table 12-134. C0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.7.40 C1CCNC Register (Offset = 1C4h) [Reset = 00000000h]

C1CCNC is shown in Table 12-135.

Return to the Summary Table.

Channel 1 Capture Compare No Clear

Table 12-135. C1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.7.41 C2CCNC Register (Offset = 1C8h) [Reset = 00000000h]

C2CCNC is shown in Table 12-136.

Return to the Summary Table.

Channel 2 Capture Compare No Clear

Table 12-136. C2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.8 LGPT3 Registers

Table 12-137 lists the memory-mapped registers for the LGPT3 registers. All register offset addresses not listed in Table 12-137 should be considered as reserved locations and the register contents should not be modified.

Table 12-137. LGPT3 Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 12.8.1
4h	DESCEX	Description Extended	Section 12.8.2
8h	STARTCFG	Start Configuration	Section 12.8.3
Ch	CTL	Timer Control	Section 12.8.4
10h	OUTCTL	Output Control	Section 12.8.5
14h	CNTR	Counter	Section 12.8.6
18h	PRECFG	Clock Prescaler Configuration	Section 12.8.7
1Ch	PREEVENT	Prescaler Event	Section 12.8.8
20h	CHFILT	Channel Input Filter	Section 12.8.9
3Ch	DMA	Direct Memory Accsess	Section 12.8.10
40h	DMARW	Direct Memory Access	Section 12.8.11
44h	ADCTRG	ADC Trigger	Section 12.8.12
48h	IOCTL	IO Controller	Section 12.8.13
68h	IMASK	Interrupt mask.	Section 12.8.14
6Ch	RIS	Raw interrupt status.	Section 12.8.15
70h	MIS	Masked interrupt status.	Section 12.8.16
74h	ISET	Interrupt set register.	Section 12.8.17
78h	ICLR	Interrupt clear register.	Section 12.8.18
7Ch	IMSET	Interrupt mask set register.	Section 12.8.19
80h	IMCLR	Interrupt mask clear register.	Section 12.8.20
84h	EMU	Debug control	Section 12.8.21
C0h	C0CFG	Channel 0 Configuration	Section 12.8.22
C4h	C1CFG	Channel 1 Configuration	Section 12.8.23
C8h	C2CFG	Channel 2 Configuration	Section 12.8.24
FCh	PTGT	Pipeline Target	Section 12.8.25
100h	PC0CC	Pipeline Channel 0 Capture Compare	Section 12.8.26
104h	PC1CC	Pipeline Channel 1 Capture Compare	Section 12.8.27
108h	PC2CC	Pipeline Channel 2 Capture Compare	Section 12.8.28
13Ch	TGT	Target	Section 12.8.29
140h	C0CC	Channel 0 Capture Compare	Section 12.8.30
144h	C1CC	Channel 1 Capture Compare	Section 12.8.31
148h	C2CC	Channel 2 Capture Compare	Section 12.8.32
17Ch	PTGTNC	Pipeline Target No Clear	Section 12.8.33
180h	PC0CCNC	Pipeline Channel 0 Capture Compare No Clear	Section 12.8.34
184h	PC1CCNC	Pipeline Channel 1 Capture Compare No Clear	Section 12.8.35
188h	PC2CCNC	Pipeline Channel 2 Capture Compare No Clear	Section 12.8.36
1BCh	TGTNC	Target No Clear	Section 12.8.37
1C0h	C0CCNC	Channel 0 Capture Compare No Clear	Section 12.8.38
1C4h	C1CCNC	Channel 1 Capture Compare No Clear	Section 12.8.39
1C8h	C2CCNC	Channel 2 Capture Compare No Clear	Section 12.8.40

Complex bit access types are encoded to fit into small table cells. Table 12-138 shows the codes that are used for access types in this section.

Table 12-138. LGPT3 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

12.8.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 12-139.

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Description Register.;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 12-139. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	DE49h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number.
7-4	MAJREV	R	1h	Major revision of IP.
3-0	MINREV	R	1h	Minor revision of IP.

12.8.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 12-140.

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Description Extended;This register describes the parameters of the LGPT.

Table 12-140. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	HIR	R	0h	Has IR logic.
18	HDBF	R	0h	Has Dead-Band, Fault, and Park logic.
17-14	PREW	R	8h	Prescale width. The prescaler can maximum be configured to 2^{PREW}-1.
13	HQDEC	R	0h	Has Quadrature Decoder.
12	HCIF	R	1h	Has channel input filter.
11-8	CIFS	R	8h	Channel input filter size. The prevailing state filter can maximum be configured to 2^{CIFS}-1.
7	HDMA	R	1h	Has uDMA output and logic.
6	HINT	R	1h	Has interrupt output and logic.
5-4	CNTRW	R	1h	Counter bit-width.;The maximum counter value is equal to 2^{CNTRW}-1. 0h = 16-bit counter. 1h = 24-bit counter. 2h = 32-bit counter. 3h = RESERVED
3-0	NCH	R	3h	Number of channels.

12.8.3 STARTCFG Register (Offset = 8h) [Reset = 00000000h]

STARTCFG is shown in Table 12-141.

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Start Configuration;This register is only for when CTL.MODE is configured to one of the SYNC modes.;This register defines when this LGPT starts.

Table 12-141. STARTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LGPT0	R/W	0h	LGPT start

12.8.4 CTL Register (Offset = Ch) [Reset = 00000000h]

CTL is shown in Table 12-142.

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Timer Control

Table 12-142. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2RST	W	0h	Channel 2 reset. 0h = No effect. 1h = Reset C2CC, PC2CC, and C2CFG.
9	C1RST	W	0h	Channel 1 reset. 0h = No effect. 1h = Reset C1CC, PC1CC, and C1CFG.
8	C0RST	W	0h	Channel 0 reset. 0h = No effect. 1h = Reset C0CC, PC0CC, and C0CFG.
7-6	RESERVED	R	0h	Reserved
5	INTP	R/W	0h	Interrupt Phase.;This bit field controls when the RIS.TGT and RIS.ZERO interrupts are set. 0h = RIS.TGT and RIS.ZERO are set one system clock cycle after CNTR = TARGET/ZERO. 1h = RIS.TGT and RIS.ZERO are set one timer clock cycle after CNTR = TARGET/ZERO.
4-3	CMPDIR	R/W	0h	Compare direction.;This bit field controls the direction the counter must have in order to set the RIS.CnCC channel interrupts. This bitfield is only relevant if [CnCFG.CCACT] is configured to a compare action. 0h = Compare RIS fields are set on up count and down count. 1h = Compare RIS fields are only set on up count. 2h = Compare RIS fields are only set on down count. 3h = RESERVED

Table 12-142. CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MODE	R/W	0h	Timer mode control;The CNTR restarts from 0 when MODE is written to UP_ONCE, UP_PER, UPDWN_PER, QDEC, SYNC_UP_ONCE, SYNC_UP_PER or SYNC_UPDWN_PER.;When writing MODE all internally queued updates to the channels and TGT is cleared.;When configuring the timer, MODE should be the last thing to configure. If changing timer configuration after MODE has been set is necessary, instructions, if any, given in the configuration registers should be followed. See for example C0CFG. 0h = Disable timer. Updates to counter, channels, and events stop. 1h = Count up once. The timer increments from 0 to target value, then stops and sets MODE to DIS. 2h = Count up periodically. The timer increments from 0 to target value, repeatedly.;Period = (target value + 1) * timer clock period 3h = Count up and down periodically. The timer counts from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period 4h = The timer functions as a quadrature decoder. IOC input 0, IOC input 1 and IOC input 2 are used respectivly as PHA, PHB and IDX inputs. IDX can be turned off by setting C2CFG.EDGE = NONE.;The timer clock frequency sets the sample rate of the QDEC logic. This frequency can be configured in PRECFG. 5h = Start counting up once synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_ONCE automatically. ;It then functions as a normal timer in CTL.MODE = UP_ONCE, incrementing from 0 to target value, then stops and sets MODE to DIS. 6h = Start counting up periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UP_PER automatically. ;It then operates as a normal timer in CTL.MODE = UP_PER, incrementing from 0 to target value, repeatedly.;Period = (target value * 2) * timer clock period 7h = Start counting up and down periodically synchronous to another LGPT, selected within STARTCFG. The timer is started by setting CTL.MODE = UPDWN_PER automatically. ;It then operates as a normal timer in CTL.MODE = UPDWN_PER, counting from 0 to target value and back to 0, repeatedly.;Period = (target value * 2) * timer clock period

12.8.5 OUTCTL Register (Offset = 10h) [Reset = 00000000h]

OUTCTL is shown in Table 12-143.

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Output Control;Set and clear individual outputs manually. Manual update of an output takes priority over automatic channel updates to the same output. It is not possible to set and clear an output at the same time, such requests will be neglected.;An output can be automatically cleared, set, toggled, or pulsed by each channel, listed in decreasing order of priority. The action with highest priority happens when multiple channels want to update an output at the same time.;All outputs are connected to the event fabric and the IO controller. The outputs going to the IO controller have an aditional complementary output, this output is the inverted IO output. Both the IO and the IO complementary outputs are passed through an IO Controller, see IOCTL.

Table 12-143. OUTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	SETOUT2	W	0h	Set output 2.;Write 1 to set output 2.
4	CLROUT2	W	0h	Clear output 2.;Write 1 to clear output 2.
3	SETOUT1	W	0h	Set output 1.;Write 1 to set output 1.
2	CLROUT1	W	0h	Clear output 1.;Write 1 to clear output 1.
1	SETOUT0	W	0h	Set output 0.;Write 1 to set output 0.
0	CLROUT0	W	0h	Clear output 0.;Write 1 to clear output 0.

12.8.6 CNTR Register (Offset = 14h) [Reset = 00000000h]

CNTR is shown in Table 12-144.

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Counter;The counter of this timer. After CTL.MODE is set the counter updates at the rate specified in PRECFG.

Table 12-144. CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Current counter value.;If CTL.MODE = QDEC this can be used to set the initial counter value during QDEC. Writing to CNTR in other modes than QDEC is possible, but may result in unpredictable behavior.

12.8.7 PRECFG Register (Offset = 18h) [Reset = 00000000h]

PRECFG is shown in Table 12-145.

Return to the Summary Table.

Clock Prescaler Configuration;This register is used to set the timer clock period. The prescaler is a counter which counts down from the value TICKDIV. When the prescaler counter reaches zero, CNTR is updated. The field TICKDIV effectively divides the prescaler tick source. The timer clock frequency can be calculated as TICKSRC/(TICKDIV+1).

Table 12-145. PRECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	TICKDIV	R/W	0h	Tick division.;TICKDIV determines the timer clock frequency for the counter, and timer output updates. The timer clock frequency is the clock selected by TICKSRC divided by (TICKDIV + 1). This inverse is the timer clock period.;0x00: Divide by 1.;0x01: Divide by 2.;... ;0xFF: Divide by 256.
7-2	RESERVED	R	0h	Reserved
1-0	TICKSRC	R/W	0h	Prescaler tick source.;TICKSRC determines the source which decrements the prescaler. 0h = Prescaler is updated at the system clock. 1h = Prescaler is updated at the rising edge of TICKEN. 2h = Prescaler is updated at the falling edge of TICKEN. 3h = Prescaler is updated at both edges of TICKEN.

12.8.8 PREEVENT Register (Offset = 1Ch) [Reset = 00000000h]

PREEVENT is shown in Table 12-146.

Return to the Summary Table.

Prescaler Event;This register is used to output a logic high signal before the zero crossing of the prescaler counter. The output is routed to the IOC.

Table 12-146. PREEVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Sets the HIGH time of the prescaler event output. ;Event goes high when the prescaler counter equals VAL. Event goes low when prescaler counter is 0.;Note:;- Can be used to precharge or turn an external component on for a short time before sampling, like in QDEC.;- If there is a requirement to create such events that have very short periods compared to timer clock period, use two timers. One timer acts as prescaler and event generator for another timer.

12.8.9 CHFILT Register (Offset = 20h) [Reset = 00000000h]

CHFILT is shown in Table 12-147.

Return to the Summary Table.

Channel Input Filter;This register is used to configure the filter on the channel inputs. The configuration is for all inputs.;The filter is enabled when a channel is in capture mode.;The input to the filter is passed to the edge detection logic if LOAD + 1 consecutive input samples are equal. The filter functions as a down counter, counting down every input sample.;If two consecutive samples are unequal, the filter counter restarts from LOAD.;If the filter counter reaches zero, the input signal is valid and passed to the edge detection logic.;The channel filter should only be configured while the CTL.MODE = DIS. Configuring the filter while the timer is running can result in unexpected behavior.

Table 12-147. CHFILT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	LOAD	R/W	0h	The input of the channel filter is passed to the edge detection logic after LOAD + 1 consecutive equal samples.
7-2	RESERVED	R	0h	Reserved
1-0	MODE	R/W	0h	Channel filter mode 0h = Filter is bypassed. No Filter is used. 1h = Filter is clocked by system clock. 2h = Filter is clocked by PRECFG.TICKSRC. 3h = Filter is clocked by timer clock.

12.8.10 DMA Register (Offset = 3Ch) [Reset = 00000000h]

DMA is shown in Table 12-148.

Return to the Summary Table.

Direct Memory Accsess;This register is used to enable DMA requests from the timer and set the register addresses which the DMA will access (read/write).;Choose DMA request source by setting the REQ field. The setting of the corresponding interrupt in the RIS registers also sets the DMA request. ;Upon a DMA request defined by REQ an internal address pointer is set to RWADDR*4. Every access to DMARW will increment the internal pointer by 4 such that the next DMA access will be to the next register.;The internal pointer will stop after RWCNTR increments. Further access will be ignored.

Table 12-148. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RWCNTR	R/W	0h	The read/write counter. RWCNTR+1 is the number of times the DMA can access (read/write) the DMARW register. For each DMA access to DMARW an internal counter is incremented, writing to the next address field. RWADDR + 4*RWCNTR is the final register address which can be accessed by the DMA.
15	RESERVED	R	0h	Reserved
14-8	RWADDR	R/W	0h	The base address which the DMA access when reading/writing DMARW. The base address is set by taking the 9 LSB of the physical address and divide by 4.;For example, if you wanted the RWADDR to point to the PTGT register you should set RWADDR = 0x0FC/4.
7-4	RESERVED	R	0h	Reserved
3-0	REQ	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates a DMA request. 2h = Setting of RIS.ZERO generates a DMA request. 3h = Setting of RIS.FAULT generates a DMA request. 4h = Setting of RIS.C0CC generates a DMA request. 5h = Setting of RIS.C1CC generates a DMA request. 6h = Setting of RIS.C2CC generates a DMA request. 7h = Setting of RIS.C3CC generates a DMA request. 8h = Setting of RIS.C4CC generates a DMA request. 9h = Setting of RIS.C5CC generates a DMA request. Ah = Setting of RIS.C6CC generates a DMA request. Bh = Setting of RIS.C7CC generates a DMA request. Ch = Setting of RIS.C8CC generates a DMA request. Dh = Setting of RIS.C9CC generates a DMA request. Eh = Setting of RIS.C10CC generates a DMA request. Fh = Setting of RIS.C11CC generates a DMA request.

12.8.11 DMARW Register (Offset = 40h) [Reset = 00000000h]

DMARW is shown in Table 12-149.

Return to the Summary Table.

Direct Memory Access;This register is used by the DMA to access (read/write) register inside this LGPT module.;Each access to this register will increment the internal DMA address counter. See DMA for description.

Table 12-149. DMARW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	DMA read write value.;The value that is read/written from/to the registers.

12.8.12 ADCTRG Register (Offset = 44h) [Reset = 00000000h]

ADCTRG is shown in Table 12-150.

Return to the Summary Table.

ADC Trigger;This register is used to enable ADC trigger from the timer. ;Choose ADC trigger source by setting the SRC field. The setting of the corresponding interrupt in the RIS registers also sets the ADC trigger.

Table 12-150. ADCTRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	SRC	R/W	0h	0h = Disabled 1h = Setting of RIS.TGT generates an ADC trigger. 2h = Setting of RIS.ZERO generates an ADC trigger. 3h = Setting of RIS.FAULT generates an ADC trigger. 4h = Setting of RIS.C0CC generates an ADC trigger. 5h = Setting of RIS.C1CC generates an ADC trigger. 6h = Setting of RIS.C2CC generates an ADC trigger. 7h = Setting of RIS.C3CC generates an ADC trigger. 8h = Setting of RIS.C4CC generates an ADC trigger. 9h = Setting of RIS.C5CC generates an ADC trigger. Ah = Setting of RIS.C6CC generates an ADC trigger. Bh = Setting of RIS.C7CC generates an ADC trigger. Ch = Setting of RIS.C8CC generates an ADC trigger. Dh = Setting of RIS.C9CC generates an ADC trigger. Eh = Setting of RIS.C10CC generates an ADC trigger. Fh = Setting of RIS.C11CC generates an ADC trigger.

12.8.13 IOCTL Register (Offset = 48h) [Reset = 00000000h]

IOCTL is shown in Table 12-151.

Return to the Summary Table.

IO Controller;This register overrides the IO outputs.

Table 12-151. IOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-10	COUT2	R/W	0h	IO complementary output 2 control;This bit field controls IO complementary output 2. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
9-8	OUT2	R/W	0h	IO output 2 control;This bit field controls IO output 2. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
7-6	COUT1	R/W	0h	IO complementary output 1 control;This bit field controls IO complementary output 1. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
5-4	OUT1	R/W	0h	IO output 1 control;This bit field controls IO output 1. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.
3-2	COUT0	R/W	0h	IO complementary output 0 control;This bit field controls IO complementary output 0. 0h = Normal output. The IO complementary output is not changed. 1h = Driven low. The IO complementary output is driven low. 2h = Driven high. The IO complementary output is driven high. 3h = Inverted value. The IO complementary output is inverted.
1-0	OUT0	R/W	0h	IO output 0 control;This bit field controls IO output 0. 0h = Normal output. The IO output is not changed. 1h = Driven low. The IO output is driven low. 2h = Driven high. The IO output is driven high. 3h = Inverted value. The IO output is inverted.

12.8.14 IMASK Register (Offset = 68h) [Reset = 00000000h]

IMASK is shown in Table 12-152.

Return to the Summary Table.

Interrupt mask. ;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 12-152. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R/W	0h	Enable RIS.C2CC interrupt. 0h = Disable 1h = Enable
9	C1CC	R/W	0h	Enable RIS.C1CC interrupt. 0h = Disable 1h = Enable
8	C0CC	R/W	0h	Enable RIS.C0CC interrupt. 0h = Disable 1h = Enable
7	RESERVED	R	0h	Reserved
6	FAULT	R/W	0h	Enable RIS.FAULT interrupt. 0h = Disable 1h = Enable
5	IDX	R/W	0h	Enable RIS.IDX interrupt. 0h = Disable 1h = Enable
4	DIRCHNG	R/W	0h	Enable RIS.DIRCHNG interrupt. 0h = Disable 1h = Enable
3	CNTRCHNG	R/W	0h	Enable RIS.CNTRCHNG interrupt. 0h = Disable 1h = Enable
2	DBLTRANS	R/W	0h	Enable RIS.DBLTRANS interrupt. 0h = Disable 1h = Enable
1	ZERO	R/W	0h	Enable RIS.ZERO interrupt. 0h = Disable 1h = Enable
0	TGT	R/W	0h	Enable RIS.TGT interrupt. 0h = Disable 1h = Enable

12.8.15 RIS Register (Offset = 6Ch) [Reset = 00000000h]

RIS is shown in Table 12-153.

Return to the Summary Table.

Raw interrupt status. ;This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-153. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Status of the C2CC interrupt. The interrupt is set when C2CC has capture or compare event. 0h = Cleared 1h = Set
9	C1CC	R	0h	Status of the C1CC interrupt. The interrupt is set when C1CC has capture or compare event. 0h = Cleared 1h = Set
8	C0CC	R	0h	Status of the C0CC interrupt. The interrupt is set when C0CC has capture or compare event. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Status of the FAULT interrupt. The interrupt is set immediately on active fault input. 0h = Cleared 1h = Set
5	IDX	R	0h	Status of the IDX interrupt. The interrupt is set when IDX is active. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Status of the DIRCHNG interrupt. The interrupt is set when the direction of the counter changes. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Status of the CNTRCHNG interrupt. The interrupt is set when the counter increments or decrements. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Status of the DBLTRANS interrupt. The interrupt is set when a double transition has happened during QDEC mode. 0h = Cleared 1h = Set
1	ZERO	R	0h	Status of the ZERO interrupt. The interrupt is set when CNTR = 0. 0h = Cleared 1h = Set
0	TGT	R	0h	Status of the TGT interrupt. The interrupt is set when CNTR = TGT. 0h = Cleared 1h = Set

12.8.16 MIS Register (Offset = 70h) [Reset = 00000000h]

MIS is shown in Table 12-154.

Return to the Summary Table.

Masked interrupt status. ;This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 12-154. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	R	0h	Masked status of the RIS.C2CC interrupt. 0h = Cleared 1h = Set
9	C1CC	R	0h	Masked status of the RIS.C1CC interrupt. 0h = Cleared 1h = Set
8	C0CC	R	0h	Masked status of the RIS.C0CC interrupt. 0h = Cleared 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	R	0h	Masked status of the RIS.FAULT interrupt. 0h = Cleared 1h = Set
5	IDX	R	0h	Masked status of the RIS.IDX interrupt. 0h = Cleared 1h = Set
4	DIRCHNG	R	0h	Masked status of the RIS.DIRCHNG interrupt. 0h = Cleared 1h = Set
3	CNTRCHNG	R	0h	Masked status of the RIS.CNTRCHNG interrupt. 0h = Cleared 1h = Set
2	DBLTRANS	R	0h	Masked status of the RIS.DBLTRANS interrupt. 0h = Cleared 1h = Set
1	ZERO	R	0h	Masked status of the RIS.ZERO interrupt. 0h = Cleared 1h = Set
0	TGT	R	0h	Masked status of the RIS.TGT interrupt. 0h = Cleared 1h = Set

12.8.17 ISET Register (Offset = 74h) [Reset = 00000000h]

ISET is shown in Table 12-155.

Return to the Summary Table.

Interrupt set register. ;This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 12-155. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the RIS.C2CC interrupt. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the RIS.C1CC interrupt. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the RIS.C0CC interrupt. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the RIS.FAULT interrupt. 0h = No effect 1h = Set
5	IDX	W	0h	Set the RIS.IDX interrupt. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the RIS.DIRCHNG interrupt. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the RIS.DBLTRANS interrupt. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the RIS.ZERO interrupt. 0h = No effect 1h = Set
0	TGT	W	0h	Set the RIS.TGT interrupt. 0h = No effect 1h = Set

12.8.18 ICLR Register (Offset = 78h) [Reset = 00000000h]

ICLR is shown in Table 12-156.

Return to the Summary Table.

Interrupt clear register. ;This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 12-156. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the RIS.C2CC interrupt. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the RIS.C1CC interrupt. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the RIS.C0CC interrupt. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the RIS.FAULT interrupt. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the RIS.IDX interrupt. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the RIS.DIRCHNG interrupt. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the RIS.CNTRCHNG interrupt. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the RIS.DBLTRANS interrupt. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the RIS.ZERO interrupt. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the RIS.TGT interrupt. 0h = No effect 1h = Clear

12.8.19 IMSET Register (Offset = 7Ch) [Reset = 00000000h]

IMSET is shown in Table 12-157.

Return to the Summary Table.

Interrupt mask set register. ;Writing a 1 to a bit in this register will set the corresponding IMASK bit.

Table 12-157. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Set the MIS.C2CC mask. 0h = No effect 1h = Set
9	C1CC	W	0h	Set the MIS.C1CC mask. 0h = No effect 1h = Set
8	C0CC	W	0h	Set the MIS.C0CC mask. 0h = No effect 1h = Set
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Set the MIS.FAULT mask. 0h = No effect 1h = Set
5	IDX	W	0h	Set the MIS.IDX mask. 0h = No effect 1h = Set
4	DIRCHNG	W	0h	Set the MIS.DIRCHNG mask. 0h = No effect 1h = Set
3	CNTRCHNG	W	0h	Set the MIS.CNTRCHNG mask. 0h = No effect 1h = Set
2	DBLTRANS	W	0h	Set the MIS.DBLTRANS mask. 0h = No effect 1h = Set
1	ZERO	W	0h	Set the MIS.ZERO mask. 0h = No effect 1h = Set
0	TGT	W	0h	Set the MIS.TGT mask. 0h = No effect 1h = Set

12.8.20 IMCLR Register (Offset = 80h) [Reset = 00000000h]

IMCLR is shown in Table 12-158.

Return to the Summary Table.

Interrupt mask clear register. ;Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 12-158. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	C2CC	W	0h	Clear the MIS.C2CC mask. 0h = No effect 1h = Clear
9	C1CC	W	0h	Clear the MIS.C1CC mask. 0h = No effect 1h = Clear
8	C0CC	W	0h	Clear the MIS.C0CC mask. 0h = No effect 1h = Clear
7	RESERVED	R	0h	Reserved
6	FAULT	W	0h	Clear the MIS.FAULT mask. 0h = No effect 1h = Clear
5	IDX	W	0h	Clear the MIS.IDX mask. 0h = No effect 1h = Clear
4	DIRCHNG	W	0h	Clear the MIS.DIRCHNG mask. 0h = No effect 1h = Clear
3	CNTRCHNG	W	0h	Clear the MIS.CNTRCHNG mask. 0h = No effect 1h = Clear
2	DBLTRANS	W	0h	Clear the MIS.DBLTRANS mask. 0h = No effect 1h = Clear
1	ZERO	W	0h	Clear the MIS.ZERO mask. 0h = No effect 1h = Clear
0	TGT	W	0h	Clear the MIS.TGT mask. 0h = No effect 1h = Clear

12.8.21 EMU Register (Offset = 84h) [Reset = 00000000h]

EMU is shown in Table 12-159.

Return to the Summary Table.

Debug control;This register can be used to freeze the timer when CPU halts when HALT is set to 1. When HALT is set to 0, or when the CPU releases debug halt, the filters and edge detection logic is flushed and the timer starts. For setting a predefined output value during a CPU debug halt, PARK, if the timer has this register, should be configured additionally. If this timer does not have the PARK register a predefined output value during CPU halt is not possible.

Table 12-159. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CTL	R/W	0h	Halt control.;Configure when the counter shall stop upon CPU halt. This bitfield only applies if HALT = 1. 0h = Immediate reaction. The counter stops immediately on debug halt. 1h = Zero condition. The counter stops when CNTR = 0.
0	HALT	R/W	0h	Halt LGPT when CPU is halted in debug. 0h = Disable. 1h = Enable.

12.8.22 C0CFG Register (Offset = C0h) [Reset = 00000000h]

C0CFG is shown in Table 12-160.

Return to the Summary Table.

Channel 0 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-160. C0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 2. 1h = Channel 0 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 1. 1h = Channel 0 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 0 does not control output 0. 1h = Channel 0 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-160. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C0CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C0CC when C0CC.VAL contains signal period and PC0CC.VAL contains signal pulse width.;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C0CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C0CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-160. C0CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C0CC.VAL / TGT.VAL).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C0CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C0CC.VAL <= TGT.VAL: ; Duty cycle = C0CC.VAL / (TGT.VAL + 1).;When C0CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C0CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C0CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C0CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C0CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C0CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.8.23 C1CFG Register (Offset = C4h) [Reset = 00000000h]

C1CFG is shown in Table 12-161.

Return to the Summary Table.

Channel 1 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-161. C1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 2. 1h = Channel 1 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 1. 1h = Channel 1 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 1 does not control output 0. 1h = Channel 1 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-161. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C1CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C1CC when C1CC.VAL contains signal period and PC1CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C1CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C1CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-161. C1CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C1CC.VAL / TGT.VAL).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C1CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C1CC.VAL <= TGT.VAL: ; Duty cycle = C1CC.VAL / (TGT.VAL + 1).;When C1CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C1CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C1CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C1CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C1CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C1CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.8.24 C2CFG Register (Offset = C8h) [Reset = 00000000h]

C2CFG is shown in Table 12-162.

Return to the Summary Table.

Channel 2 Configuration;This register configures channel function and enables outputs.;Each channel has an edge-detection circuit. The the edge-detection circuit is: ; - enabled while CCACT selects a capture function and CTL.MODE is different from DIS.; - flushed while CCACT selects a capture function and CTL.MODE is changed from DIS to another mode.;The flush action uses two system clock periods. It prevents capture events caused by expired signal values stored in the edge-detection circuit.;The channel input signal enters the edge-detection circuit. False capture events can occur when:;- the edge-detection circuit contains expired signal samples and the circuit is enabled without flush as described above.;- the CCACT field is reconfigured while CTL.MODE is different from DIS.;Primary use scenario is to select CCACT before starting the timer. Follow these steps to configure CCACT to a capture action while CTL.MODE is different from DIS:;- Set EDGE to NONE.;- Configure CCACT.;- Wait for three system clock periods before setting EDGE different from NONE.;These steps prevent capture events caused by expired signal values in edge-detection circuit.

Table 12-162. C2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	OUT2	R/W	0h	Output 2 enable.;When 0 < CCACT < 8, OUT2 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 2. 1h = Channel 2 controls output 2.
9	OUT1	R/W	0h	Output 1 enable.;When 0 < CCACT < 8, OUT1 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 1. 1h = Channel 2 controls output 1.
8	OUT0	R/W	0h	Output 0 enable.;When 0 < CCACT < 8, OUT0 becomes zero after a capture or compare event. 0h = Channel 2 does not control output 0. 1h = Channel 2 controls output 0.
7	RESERVED	R	0h	Reserved
6	INPUT	R/W	0h	Select channel input. 0h = Event fabric 1h = IO controller
5-4	EDGE	R/W	0h	Determines the edge that triggers the channel input event. This happens post filter. 0h = Input is turned off. 1h = Input event is triggered at rising edge. 2h = Input event is triggered at falling edge. 3h = Input event is triggered at both edges.

Table 12-162. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CCACT	R/W	0h	Capture-Compare action.;Capture-Compare action defines 15 different channel functions that utilize capture, compare, and zero events. In every compare event the timer looks at the current value of CNTR. The corresponding output event will be set 1 timer period after CNTR = C2CC. 0h = Disable channel. 1h = Set on capture, and then disable channel.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL.;- Disable channel. ;Primary use scenario is to select this function before starting the timer.;Follow these steps to select this function while CTL.MODE is different from DIS: ; - Set CCACT to SET_ON_CAPT with no output enable.; - Configure INPUT (optional).; - Wait for three timer clock periods as defined in PRECFG before setting CCACT to SET_ON_CAPT_DIS. Output enable is optional.;These steps prevent capture events caused by expired signal values in edge-detection circuit. 2h = Clear on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. 3h = Set on zero, toggle on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. 4h = Clear on compare, and then disable channel.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 5h = Set on compare, and then disable channel.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 6h = Toggle on compare, and then disable channel.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel. 7h = Pulse on compare, and then disable channel.;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.;- Disable channel.; The output is high for two timer clock periods. 8h = Period and pulse width measurement.;Continuously capture period and pulse width of the signal selected by INPUT relative to the signal edge given by EDGE. ;Set enabled outputs and RIS.C2CC when C2CC.VAL contains signal period and PC2CC.VAL contains signal pulse width. ;Notes: ;- Make sure to configure INPUT and CCACT when CTL.MODE equals DIS, then set CTL.MODE to UP_ONCE or UP_PER. ;- The counter restarts in the selected timer mode when C2CC.VAL contains the signal period.;- If more than one channel uses this function, the channels will perform this function one at a time. The channel with lowest number has priority and performs the function first. Next measurement starts when current measurement completes successfully or times out. A timeout occurs when counter equals target. ;- To observe a timeout event the RIS.TGT interrupt can be used, or another channel can be configured to SET_ON_CMP with compare value equal TGT.;Signal property requirements:;- Signal Period >= 2 * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal Period <= MAX(CNTR) * (1 + PRECFG.TICKDIV) * timer clock period.;- Signal low and high phase >= (1 + PRECFG.TICKDIV) * timer clock period. 9h = Set on capture repeatedly.;Channel function sequence: ;- Set enabled outputs on capture event and copy CNTR.VAL to C2CC.VAL. Ah = Clear on zero, toggle on compare repeatedly.; ;Channel function sequence: ;- Clear enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UPDWN_PER for center-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle

Table 12-162. C2CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				= 1 - (C2CC.VAL / TGT.VAL).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 0.;Enabled outputs are set when C2CC.VAL = 0 and CNTR.VAL = 0. Bh = Set on zero, toggle on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when CNTR.VAL = 0.;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL.;Set CTL.MODE to UP_PER for edge-aligned PWM generation. Duty cycle is given by: ;When C2CC.VAL <= TGT.VAL: ; Duty cycle = C2CC.VAL / (TGT.VAL + 1).;When C2CC.VAL > TGT.VAL: ; Duty cycle = 1.;Enabled outputs are cleared when C2CC.VAL = 0 and CNTR.VAL = 0. Ch = Clear on compare repeatedly.;Channel function sequence: ;- Clear enabled outputs when C2CC.VAL = CNTR.VAL. Dh = Set on compare repeatedly.;Channel function sequence: ;- Set enabled outputs when C2CC.VAL = CNTR.VAL. Eh = Toggle on compare repeatedly.;Channel function sequence: ;- Toggle enabled outputs when C2CC.VAL = CNTR.VAL. Fh = Pulse on compare repeatedly. ;Channel function sequence: ;- Pulse enabled outputs when C2CC.VAL = CNTR.VAL.; The output is high for two timer clock periods.

12.8.25 PTGT Register (Offset = FCh) [Reset = 00000000h]

PTGT is shown in Table 12-163.

Return to the Summary Table.

Pipeline Target;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer will copy PTGT.VAL to TGT.VAL on the upcoming CNTR zero crossing only if PTGT.VAL has been written. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC;The CNTR value is updated with VALUE on IDX if the counter is counting down. If the counter is counting up, CNTR is loaded with zero on IDX.;In this mode the VALUE is not loaded into TGT on zero crossing.

Table 12-163. PTGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	The pipleline target value.

12.8.26 PC0CC Register (Offset = 100h) [Reset = 00000000h]

PC0CC is shown in Table 12-164.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare

Table 12-164. PC0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.8.27 PC1CC Register (Offset = 104h) [Reset = 00000000h]

PC1CC is shown in Table 12-165.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare

Table 12-165. PC1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.8.28 PC2CC Register (Offset = 108h) [Reset = 00000000h]

PC2CC is shown in Table 12-166.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare

Table 12-166. PC2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.8.29 TGT Register (Offset = 13Ch) [Reset = 00000000h]

TGT is shown in Table 12-167.

Return to the Summary Table.

Target;User defined counter target. ;A read or write to this register will clear the RIS.ZERO and RIS.TGT interrupt.

Table 12-167. TGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	00FFFFFFh	User defined counter target value.

12.8.30 C0CC Register (Offset = 140h) [Reset = 00000000h]

C0CC is shown in Table 12-168.

Return to the Summary Table.

Channel 0 Capture Compare

Table 12-168. C0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.8.31 C1CC Register (Offset = 144h) [Reset = 00000000h]

C1CC is shown in Table 12-169.

Return to the Summary Table.

Channel 1 Capture Compare

Table 12-169. C1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.8.32 C2CC Register (Offset = 148h) [Reset = 00000000h]

C2CC is shown in Table 12-170.

Return to the Summary Table.

Channel 2 Capture Compare

Table 12-170. C2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.8.33 PTGTNC Register (Offset = 17Ch) [Reset = 00000000h]

PTGTNC is shown in Table 12-171.

Return to the Summary Table.

Pipeline Target No Clear;Use this register to read or write to PTGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-171. PTGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	A read or write to this register will not clear the RIS.TGT interrupt.;If CTL.MODE != QDEC.;Target value for next counter period.;The timer copies VAL to TGT.VAL when CNTR.VAL becomes 0. The copy does not happen when restarting the timer.;This is useful to avoid period jitter in PWM applications with time-varying period, sometimes referenced as phase corrected PWM.;If CTL.MODE = QDEC.;The CNTR.VAL is updated with VAL on IDX. VAL is not loaded into TGT.VAL when CNTR.VAL becomes 0.

12.8.34 PC0CCNC Register (Offset = 180h) [Reset = 00000000h]

PC0CCNC is shown in Table 12-172.

Return to the Summary Table.

Pipeline Channel 0 Capture Compare No Clear

Table 12-172. PC0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;An update of VAL will be transferred to C0CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C0CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C0CFG.EDGE.

12.8.35 PC1CCNC Register (Offset = 184h) [Reset = 00000000h]

PC1CCNC is shown in Table 12-173.

Return to the Summary Table.

Pipeline Channel 1 Capture Compare No Clear

Table 12-173. PC1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;An update of VAL will be transferred to C1CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C1CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C1CFG.EDGE.

12.8.36 PC2CCNC Register (Offset = 188h) [Reset = 00000000h]

PC2CCNC is shown in Table 12-174.

Return to the Summary Table.

Pipeline Channel 2 Capture Compare No Clear

Table 12-174. PC2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Pipeline Capture Compare value.;User defined pipeline compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;An update of VAL will be transferred to C2CC.VAL when the next CNTR.VAL is zero and CTL.MODE is different from DIS. This is useful for PWM generation and prevents jitter on the edges of the generated signal.;Capture mode: ;When C2CFG.CCACT equals PER_PULSE_WIDTH_MEAS then VAL contains the width of the low or high phase of the selected signal. This is specified by C2CFG.EDGE.

12.8.37 TGTNC Register (Offset = 1BCh) [Reset = 00000000h]

TGTNC is shown in Table 12-175.

Return to the Summary Table.

Target No Clear;Use this register to read or write to TGT without clearing the RIS.ZERO and RIS.TGT interrupt.

Table 12-175. TGTNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	00FFFFFFh	User defined counter target value.

12.8.38 C0CCNC Register (Offset = 1C0h) [Reset = 00000000h]

C0CCNC is shown in Table 12-176.

Return to the Summary Table.

Channel 0 Capture Compare No Clear

Table 12-176. C0CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C0CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C0CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C0CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.8.39 C1CCNC Register (Offset = 1C4h) [Reset = 00000000h]

C1CCNC is shown in Table 12-177.

Return to the Summary Table.

Channel 1 Capture Compare No Clear

Table 12-177. C1CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C1CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C1CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C1CFG.CCACT determines if VAL is a signal period or a regular capture value.

12.8.40 C2CCNC Register (Offset = 1C8h) [Reset = 00000000h]

C2CCNC is shown in Table 12-178.

Return to the Summary Table.

Channel 2 Capture Compare No Clear

Table 12-178. C2CCNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	VAL	R/W	Xh	Capture Compare value.;User defined compare value or channel-updated capture value.;A read or write to this register will not clear the RIS.C2CC interrupt.;Compare mode: ;VAL is compared against CNTR.VAL and an event is generated as specified by C2CFG.CCACT when these are equal. ;Capture mode: ;The current counter value is stored in VAL when a capture event occurs. C2CFG.CCACT determines if VAL is a signal period or a regular capture value.

Chapter 13

Algorithm Processing Unit (APU)

This section describes the Algorithm Processing Unit (APU).

13.1 Introduction

The device includes a generic mathematical hardware accelerator, the Algorithm Processing Unit (APU) provided to offload numerically intensive operations from the system CPU. The APU operates on floating point numbers using IEEE 754 single precision format and it is optimized to work with complex numbers. APU operation is autonomous from the system CPU. A local memory for data storage is provided for the APU, and this memory is also accessed by the system CPU. The APU is capable of handling vector and matrix operations efficiently and can sustain a complete multiply-and-accumulate operation on complex numbers in each clock cycle. Usage of the APU as an accelerator for the system CPU significantly reduces the runtime for computational-intensive algorithms such as MUSIC (Multiple Signal Classification) needed to support the Channel Sounding feature of the Bluetooth standard, and also signal pre-processing algorithms to support Edge Machine Learning use cases. This allows the system CPU to off-load applications to the APU, to then perform other high priority tasks.

The main features of the APU are the following :

- 8 KB zero-latency local data memory with a data access width allowing:
  - Memory read bandwidth of 12.288 Gbps
- Set of pipelined hardware accelerators:
  - Real-to-complex number converter
  - Fixed point to floating point converter
  - Floating point multipliers
  - Floating point CORDIC function
  - Floating point adder and accumulator
  - Max-min function
  - Floating point divider
  - Sine and cosine operations
- Peak FLOPS performance of 0.672 GFLOPS

13.2 APU Related Collateral

Getting Started Material

- *Kindly see **SIMPLELINK-LOWPOWER-F3-SDK**\docs\drivers\tidriversAPIs.html for more information.*

13.3 Functional Description

All mathematical operations which can be performed on the APU are accessed by the system CPU through SIMPLELINK-LOWPOWER-F3-SDK APU Driver APIs. This allows higher-level algorithms implemented on the system CPU to use the APU as an accelerator for these mathematical operations.

Examples of the mathematical operations provided by the APIs are listed below:

- Generic linear algebra:
  - Vector operations e.g. scalar product, vector summation, vector sorting
  - Matrix operations e.g. scalar multiplication, multiplication of two matrices
- Cartesian and polar coordinate functions:
  - Polar to Cartesian conversion and vice versa
- Advanced algebraic operations:
  - Covariance matrix generation with spatial smoothing
  - Gauss-Jordan elimination method
  - Jacobi eigenvalue decomposition
  - Frobenius norm (L2 norm) of a matrix
- Fourier-related transforms

- Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT)
- Discrete Cosine Transform (DCT)

The APU consists of a number of individual hardware accelerators which are used in conjunction with each other by the various APIs in order to implement a specific mathematical operation.

The internal pipeline organization of the hardware accelerators allows a peak performance of 0.672 GFLOPS where FLOPS performance is measured from a complex number multiply-and-accumulate operation consisting of 7 FLOPs operating at 96 MHz clock frequency.

The APU includes data memory for local storage of input and output data. The data memory consists of 1024 64-bit words i.e. 8 KB of storage. The APU will access two complex numbers i.e. a total of 64 bits, from the data memory during each clock cycle. The data memory access width gives a memory read bandwidth of 12.288 Gbps.

13.4 APU Operation

The following sequence is executed by the system CPU to perform a APU operation:

- Transfer the input data into the APU data memory
- Initiate the required operation by calling the API
- Receive an interrupt request (IRQ) from the APU when the API has completed its operation
- Read the result data from the APU data memory

13.5 Interrupts and Events

The APU generates a completion interrupt on the interrupt vector of the peripheral when a APU API function has completed.

13.6 Data Representation

Data is represented as two consecutive 32-bit floating point numbers using IEEE 754 format. In order to represent a complex number, one 32-bit floating point value is used to represent the imaginary part, and another 32-bit floating point value is used to represent the real part of the complex number. Thus 64 bits are used to represent an entire complex number value. Complex numbers can be stored in either Cartesian or polar representation as shown in the table below.

In Cartesian representation a complex number is stored as two real numbers, with bits 63:32 being the imaginary part and bits 31:0 the real part.

In polar representation, a complex number is stored as two real numbers, where bits 63:32 are the phase (theta) and bits 31:0 the magnitude (r). In both representations, a 64 bit number can be used to indicate a real number simply by making the upper 32-bits (imaginary part) all zero.

Table 13-1. Number Representation

	Bits 63:32	Bits 31:0
Cartesian	imag(x)	real(x)
Polar	theta(x)	r(x)

Note

The APU will not automatically handle number representation conversions. One must make sure that the proper conversions are employed before operating on complex numbers stored using different representations. In other words, adding two numbers where one number is stored in Cartesian format and the other number is in Polar format, produces wrong results.

13.7 Data Memory

The system CPU writes input data to the APU Data memory, of size 8kB. Result data is also read from the same APU Data memory. The system CPU shall access the APU Data memory as regular SRAM with 32-bit words, whereas the APU will internally access this memory using 128-bit wide access.

The APU Data memory can be used by the system CPU as a scratchpad memory if the APU is not in use. This memory does not support retention nor parity checking and therefore should not be used as program memory.

The API functions for mathematical operations will provide pointers to vector or matrix input data, and also a pointer to vector or matrix result data. Matrix data shall be stored using column-major order.

The data memory can be used by the APU in two different configurations, depending on the API function. These configurations are known as Interleaved Mode (RAID 0) or Mirrored Mode (RAID 1). The APU shall be configured to either of those operation modes through a dedicated API function. Note that currently, all supported APIs operate in mirrored mode. The configured mode determines the positioning of input data:

- Interleaved Mode: elements of input vector A (or input matrix A) must be stored in even addresses and elements of input vector B (or input matrix B) must be stored in odd addresses.
- Mirrored Mode: elements of input vectors (or input matrices) can be positioned anywhere in memory.

13.8 Software

APU Examples

Software examples are provided and documented in the SimpleLink™ Low Power F3 software development kit (SDK).

13.9 APU Registers

Table 13-2 lists the memory-mapped registers for the APU registers. All register offset addresses not listed in Table 13-2 should be considered as reserved locations and the register contents should not be modified.

Table 13-2. APU Registers

Offset	Acronym	Register Name	Section
0h	DESC	IP Description	Section 13.9.1
44h	IMASK	Interrupt mask register	Section 13.9.2
48h	RIS	Raw interrupt flag register	Section 13.9.3
4Ch	MIS	Masked interrupt flag register	Section 13.9.4
50h	ISET	Interrupt flag set register	Section 13.9.5
54h	ICLR	Interrupt flag clear register	Section 13.9.6
58h	IMSET	Interrupt mask set register	Section 13.9.7
5Ch	IMCLR	Interrupt mask clear register	Section 13.9.8
800h	ENABLE	Internal. Only to be used through TI provided API.	Section 13.9.9
804h	FWSRC	Internal. Only to be used through TI provided API.	Section 13.9.10
808h	INIT	Internal. Only to be used through TI provided API.	Section 13.9.11
80Ch	PDREQ	Internal. Only to be used through TI provided API.	Section 13.9.12
810h	API	Internal. Only to be used through TI provided API.	Section 13.9.13
814h	MSGBOX	Internal. Only to be used through TI provided API.	Section 13.9.14
818h	CMDPAR0	Internal. Only to be used through TI provided API.	Section 13.9.15
81Ch	CMDPAR1	Internal. Only to be used through TI provided API.	Section 13.9.16
820h	CMDPAR2	Internal. Only to be used through TI provided API.	Section 13.9.17
824h	CMDPAR3	Internal. Only to be used through TI provided API.	Section 13.9.18
828h	CMDPAR4	Internal. Only to be used through TI provided API.	Section 13.9.19
82Ch	CMDPAR5	Internal. Only to be used through TI provided API.	Section 13.9.20
830h	STROBES	Internal. Only to be used through TI provided API.	Section 13.9.21
834h	IRQ	Internal. Only to be used through TI provided API.	Section 13.9.22
838h	EVT	Internal. Only to be used through TI provided API.	Section 13.9.23
83Ch	EVTMSK	Internal. Only to be used through TI provided API.	Section 13.9.24
840h	EVTCLR	Internal. Only to be used through TI provided API.	Section 13.9.25
844h	GPO	Internal. Only to be used through TI provided API.	Section 13.9.26
848h	GPOE	Internal. Only to be used through TI provided API.	Section 13.9.27
84Ch	GPI	Internal. Only to be used through TI provided API.	Section 13.9.28
850h	TRCCTL	Internal. Only to be used through TI provided API.	Section 13.9.29
854h	TRCSTAT	Internal. Only to be used through TI provided API.	Section 13.9.30
858h	TRCCMD	Internal. Only to be used through TI provided API.	Section 13.9.31
85Ch	TRCPAR0	Internal. Only to be used through TI provided API.	Section 13.9.32
860h	TRCPAR1	Internal. Only to be used through TI provided API.	Section 13.9.33
864h	TIMCTL	Internal. Only to be used through TI provided API.	Section 13.9.34
868h	TIMINC	Internal. Only to be used through TI provided API.	Section 13.9.35
86Ch	TIMPER	Internal. Only to be used through TI provided API.	Section 13.9.36
870h	TIMCNT	Internal. Only to be used through TI provided API.	Section 13.9.37
874h	TIMCAPT	Internal. Only to be used through TI provided API.	Section 13.9.38
878h	LSECTL	Internal. Only to be used through TI provided API.	Section 13.9.39
87Ch	LSESTART	Internal. Only to be used through TI provided API.	Section 13.9.40
880h	LSEBASESRCA	Internal. Only to be used through TI provided API.	Section 13.9.41

Table 13-2. APU Registers (continued)

Offset	Acronym	Register Name	Section
884h	LSEMODESRCA	Internal. Only to be used through TI provided API.	Section 13.9.42
888h	LSESUBMODESRCA	Internal. Only to be used through TI provided API.	Section 13.9.43
88Ch	LSENSRCA	Internal. Only to be used through TI provided API.	Section 13.9.44
890h	LSEMSRCA	Internal. Only to be used through TI provided API.	Section 13.9.45
894h	LSEELEMENTSRCA	Internal. Only to be used through TI provided API.	Section 13.9.46
898h	LSESTRIDESRCA	Internal. Only to be used through TI provided API.	Section 13.9.47
89Ch	LSEBASEDSTA	Internal. Only to be used through TI provided API.	Section 13.9.48
8A0h	LSEMODEDSTA	Internal. Only to be used through TI provided API.	Section 13.9.49
8A4h	LSESUBMODEDSTA	Internal. Only to be used through TI provided API.	Section 13.9.50
8A8h	LSENDSTA	Internal. Only to be used through TI provided API.	Section 13.9.51
8ACh	LSEMDSTA	Internal. Only to be used through TI provided API.	Section 13.9.52
8B0h	LSEELEMENTDSTA	Internal. Only to be used through TI provided API.	Section 13.9.53
8B4h	LSESTRIDEDSTA	Internal. Only to be used through TI provided API.	Section 13.9.54
8B8h	LSEBASESRCB	Internal. Only to be used through TI provided API.	Section 13.9.55
8BCh	LSEMODESRCB	Internal. Only to be used through TI provided API.	Section 13.9.56
8C0h	LSESUBMODESRCB	Internal. Only to be used through TI provided API.	Section 13.9.57
8C4h	LSENSRCB	Internal. Only to be used through TI provided API.	Section 13.9.58
8C8h	LSEMSRCB	Internal. Only to be used through TI provided API.	Section 13.9.59
8CCh	LSEELEMENTSRCB	Internal. Only to be used through TI provided API.	Section 13.9.60
8D0h	LSESTRIDESRCB	Internal. Only to be used through TI provided API.	Section 13.9.61
8D4h	LSEBASEDSTB	Internal. Only to be used through TI provided API.	Section 13.9.62
8D8h	LSEMODEDSTB	Internal. Only to be used through TI provided API.	Section 13.9.63
8DCh	LSESUBMODEDSTB	Internal. Only to be used through TI provided API.	Section 13.9.64
8E0h	LSENDSTB	Internal. Only to be used through TI provided API.	Section 13.9.65
8E4h	LSEMDSTB	Internal. Only to be used through TI provided API.	Section 13.9.66
8E8h	LSEELEMENTDSTB	Internal. Only to be used through TI provided API.	Section 13.9.67
8ECh	LSESTRIDEDSTB	Internal. Only to be used through TI provided API.	Section 13.9.68
8F0h	XBAR0	Internal. Only to be used through TI provided API.	Section 13.9.69
8F4h	XBAR1	Internal. Only to be used through TI provided API.	Section 13.9.70
8F8h	XBAR2	Internal. Only to be used through TI provided API.	Section 13.9.71
8FCh	R2C	Internal. Only to be used through TI provided API.	Section 13.9.72
900h	FMUL0	Internal. Only to be used through TI provided API.	Section 13.9.73
904h	FMUL1	Internal. Only to be used through TI provided API.	Section 13.9.74
908h	UCRD	Internal. Only to be used through TI provided API.	Section 13.9.75
90Ch	ADDSUB	Internal. Only to be used through TI provided API.	Section 13.9.76
910h	ADDSUBDECACC	Internal. Only to be used through TI provided API.	Section 13.9.77
914h	ADDSUBSTAT	Internal. Only to be used through TI provided API.	Section 13.9.78
918h	MAXMIN	Internal. Only to be used through TI provided API.	Section 13.9.79
91Ch	MAXMINDECACC	Internal. Only to be used through TI provided API.	Section 13.9.80
920h	MAXMININDEX	Internal. Only to be used through TI provided API.	Section 13.9.81
924h	FX2FP	Internal. Only to be used through TI provided API.	Section 13.9.82
928h	FX2FPR	Internal. Only to be used through TI provided API.	Section 13.9.83
92Ch	FX2FPCONVR	Internal. Only to be used through TI provided API.	Section 13.9.84
930h	FDIV	Internal. Only to be used through TI provided API.	Section 13.9.85
934h	FDIVSTAT	Internal. Only to be used through TI provided API.	Section 13.9.86

Table 13-2. APU Registers (continued)

Offset	Acronym	Register Name	Section
C00h	CFG	Internal. Only to be used through TI provided API.	Section 13.9.87
C04h	CH1CMD	Internal. Only to be used through TI provided API.	Section 13.9.88
C08h	CH2CMD	Internal. Only to be used through TI provided API.	Section 13.9.89
C0Ch	CH3CMD	Internal. Only to be used through TI provided API.	Section 13.9.90
C14h	CH1PAR01	Internal. Only to be used through TI provided API.	Section 13.9.91
C18h	CH2PAR01	Internal. Only to be used through TI provided API.	Section 13.9.92
C1Ch	CH3PAR01	Internal. Only to be used through TI provided API.	Section 13.9.93
C24h	CH1PAR23	Internal. Only to be used through TI provided API.	Section 13.9.94
C28h	CH2PAR23	Internal. Only to be used through TI provided API.	Section 13.9.95
C2Ch	CH3PAR23	Internal. Only to be used through TI provided API.	Section 13.9.96

Complex bit access types are encoded to fit into small table cells. Table 13-3 shows the codes that are used for access types in this section.

Table 13-3. APU Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

13.9.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 13-4.

Return to the Summary Table.

IP Description

Table 13-4. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	784Eh	Module identifier
15-12	STDIPOFF	R	1h	Standard IP MMR block offset
11-8	RESERVED	R	0h	Reserved
7-4	MAJREV	R	0h	Major revision
3-0	MINREV	R	0h	Minor revision

13.9.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 13-5.

Return to the Summary Table.

Interrupt mask register

Table 13-5. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	R/W	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	R/W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	R/W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	R/W	0h	APU API finished mask. 0h = The bit is 0 1h = The bit is 1

13.9.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 13-6.

Return to the Summary Table.

Raw interrupt flag register

Table 13-6. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	R	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	R	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	R	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	R	0h	APU API finished. This flag is set when an API call is finished. 0h = The bit is 0 1h = The bit is 1

13.9.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 13-7.

Return to the Summary Table.

Masked interrupt flag register

Table 13-7. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	R	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	R	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	R	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	R	0h	APU API finished masked interrupt status. 0h = The bit is 0 1h = The bit is 1

13.9.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 13-8.

Return to the Summary Table.

Interrupt flag set register

Table 13-8. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	W	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	W	0h	Set the APU API finish interrupt. 0h = The bit is 0 1h = The bit is 1

13.9.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 13-9.

Return to the Summary Table.

Interrupt flag clear register

Table 13-9. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	W	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	W	0h	Clear the APU API finish interrupt. 0h = The bit is 0 1h = The bit is 1

13.9.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 13-10.

Return to the Summary Table.

Interrupt mask set register

Table 13-10. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	W	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	W	0h	Set the APU API finish mask. 0h = The bit is 0 1h = The bit is 1

13.9.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 13-11.

Return to the Summary Table.

Interrupt mask clear register

Table 13-11. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MSGBOX	W	0h	Hardware defined interrupt triggered on msgbox write. 0h = The bit is 0 1h = The bit is 1
2	SOFT2	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
1	SOFT1	W	0h	Software defined interrupt. Not in use. 0h = The bit is 0 1h = The bit is 1
0	API	W	0h	Clear the APU API finish mask. 0h = The bit is 0 1h = The bit is 1

13.9.9 ENABLE Register (Offset = 800h) [Reset = 00000000h]

ENABLE is shown in Table 13-12.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-12. ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	LSE	R/W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	R/W	0h	Internal. Only to be used through TI provided API.

13.9.10 FWSRC Register (Offset = 804h) [Reset = 00000000h]

FWSRC is shown in Table 13-13.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-13. FWSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BANK	R/W	0h	Internal. Only to be used through TI provided API.

13.9.11 INIT Register (Offset = 808h) [Reset = 00000000h]

INIT is shown in Table 13-14.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-14. INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	FDIV	W	0h	Internal. Only to be used through TI provided API.
7	MAXMIN	W	0h	Internal. Only to be used through TI provided API.
6	ADDSUB	W	0h	Internal. Only to be used through TI provided API.
5	UCRD	W	0h	Internal. Only to be used through TI provided API.
4	FMUL1	W	0h	Internal. Only to be used through TI provided API.
3	FMUL0	W	0h	Internal. Only to be used through TI provided API.
2	ARBITER	W	0h	Internal. Only to be used through TI provided API.
1	LSE	W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	W	0h	Internal. Only to be used through TI provided API.

13.9.12 PDREQ Register (Offset = 80Ch) [Reset = 00000000h]

PDREQ is shown in Table 13-15.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-15. PDREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TOPSMPDREQ	R/W	0h	Internal. Only to be used through TI provided API.

13.9.13 API Register (Offset = 810h) [Reset = 00000000h]

API is shown in Table 13-16.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-16. API Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	CMD	R/W	0h	Internal. Only to be used through TI provided API.

13.9.14 MSGBOX Register (Offset = 814h) [Reset = 00000000h]

MSGBOX is shown in Table 13-17.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-17. MSGBOX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.15 CMDPAR0 Register (Offset = 818h) [Reset = 00000000h]

CMDPAR0 is shown in Table 13-18.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-18. CMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.16 CMDPAR1 Register (Offset = 81Ch) [Reset = 00000000h]

CMDPAR1 is shown in Table 13-19.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-19. CMDPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.17 CMDPAR2 Register (Offset = 820h) [Reset = 00000000h]

CMDPAR2 is shown in Table 13-20.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-20. CMDPAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.18 CMDPAR3 Register (Offset = 824h) [Reset = 00000000h]

CMDPAR3 is shown in Table 13-21.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-21. CMDPAR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.19 CMDPAR4 Register (Offset = 828h) [Reset = 00000000h]

CMDPAR4 is shown in Table 13-22.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-22. CMDPAR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.20 CMDPAR5 Register (Offset = 82Ch) [Reset = 00000000h]

CMDPAR5 is shown in Table 13-23.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-23. CMDPAR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.21 STROBES Register (Offset = 830h) [Reset = 00000000h]

STROBES is shown in Table 13-24.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-24. STROBES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	S0	W	0h	Internal. Only to be used through TI provided API.

13.9.22 IRQ Register (Offset = 834h) [Reset = 00000000h]

IRQ is shown in Table 13-25.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-25. IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	SOFT2	W	0h	Internal. Only to be used through TI provided API.
1	SOFT1	W	0h	Internal. Only to be used through TI provided API.
0	SOFT0	W	0h	Internal. Only to be used through TI provided API.

13.9.23 EVT Register (Offset = 838h) [Reset = 00000000h]

EVT is shown in Table 13-26.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-26. EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	LSEPUSHFINISH	R	0h	Internal. Only to be used through TI provided API.
3	LSEPULLFINISH	R	0h	Internal. Only to be used through TI provided API.
2	COUNTER	R	0h	Internal. Only to be used through TI provided API.
1	TIMER	R	0h	Internal. Only to be used through TI provided API.
0	API	R	0h	Internal. Only to be used through TI provided API.

13.9.24 EVTMSK Register (Offset = 83Ch) [Reset = 00000000h]

EVTMSK is shown in Table 13-27.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-27. EVTMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	LSEPUSHFINISH	R/W	0h	Internal. Only to be used through TI provided API.
3	LSEPULLFINISH	R/W	0h	Internal. Only to be used through TI provided API.
2	COUNTER	R/W	0h	Internal. Only to be used through TI provided API.
1	TIMER	R/W	0h	Internal. Only to be used through TI provided API.
0	API	R/W	0h	Internal. Only to be used through TI provided API.

13.9.25 EVTCLR Register (Offset = 840h) [Reset = 00000000h]

EVTCLR is shown in Table 13-28.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-28. EVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	LSEPUSHFINISH	W	0h	Internal. Only to be used through TI provided API.
3	LSEPULLFINISH	W	0h	Internal. Only to be used through TI provided API.
2	COUNTER	W	0h	Internal. Only to be used through TI provided API.
1	TIMER	W	0h	Internal. Only to be used through TI provided API.
0	API	W	0h	Internal. Only to be used through TI provided API.

13.9.26 GPO Register (Offset = 844h) [Reset = 00000000h]

GPO is shown in Table 13-29.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-29. GPO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	GPO7	R/W	0h	Internal. Only to be used through TI provided API.
6	GPO6	R/W	0h	Internal. Only to be used through TI provided API.
5	GPO5	R/W	0h	Internal. Only to be used through TI provided API.
4	GPO4	R/W	0h	Internal. Only to be used through TI provided API.
3	GPO3	R/W	0h	Internal. Only to be used through TI provided API.
2	GPO2	R/W	0h	Internal. Only to be used through TI provided API.
1	GPO1	R/W	0h	Internal. Only to be used through TI provided API.
0	GPO0	R/W	0h	Internal. Only to be used through TI provided API.

13.9.27 GPOE Register (Offset = 848h) [Reset = 00000000h]

GPOE is shown in Table 13-30.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-30. GPOE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	GPOE7	R/W	0h	Internal. Only to be used through TI provided API.
6	GPOE6	R/W	0h	Internal. Only to be used through TI provided API.
5	GPOE5	R/W	0h	Internal. Only to be used through TI provided API.
4	GPOE4	R/W	0h	Internal. Only to be used through TI provided API.
3	GPOE3	R/W	0h	Internal. Only to be used through TI provided API.
2	GPOE2	R/W	0h	Internal. Only to be used through TI provided API.
1	GPOE1	R/W	0h	Internal. Only to be used through TI provided API.
0	GPOE0	R/W	0h	Internal. Only to be used through TI provided API.

13.9.28 GPI Register (Offset = 84Ch) [Reset = 00000000h]

GPI is shown in Table 13-31.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-31. GPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	GPI7	R	0h	Internal. Only to be used through TI provided API.
6	GPI6	R	0h	Internal. Only to be used through TI provided API.
5	GPI5	R	0h	Internal. Only to be used through TI provided API.
4	GPI4	R	0h	Internal. Only to be used through TI provided API.
3	GPI3	R	0h	Internal. Only to be used through TI provided API.
2	GPI2	R	0h	Internal. Only to be used through TI provided API.
1	GPI1	R	0h	Internal. Only to be used through TI provided API.
0	GPI0	R	0h	Internal. Only to be used through TI provided API.

13.9.29 TRCCTL Register (Offset = 850h) [Reset = 00000000h]

TRCCTL is shown in Table 13-32.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-32. TRCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SEND	W	0h	Internal. Only to be used through TI provided API.

13.9.30 TRCSTAT Register (Offset = 854h) [Reset = 00000000h]

TRCSTAT is shown in Table 13-33.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-33. TRCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BUSY	R	0h	Internal. Only to be used through TI provided API.

13.9.31 TRCCMD Register (Offset = 858h) [Reset = 00000000h]

TRCCMD is shown in Table 13-34.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-34. TRCCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-8	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.

13.9.32 TRCPAR0 Register (Offset = 85Ch) [Reset = 00000000h]

TRCPAR0 is shown in Table 13-35.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-35. TRCPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.33 TRCPAR1 Register (Offset = 860h) [Reset = 00000000h]

TRCPAR1 is shown in Table 13-36.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-36. TRCPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.34 TIMCTL Register (Offset = 864h) [Reset = 00000000h]

TIMCTL is shown in Table 13-37.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-37. TIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	CPTSRC	R/W	0h	Internal. Only to be used through TI provided API.
7	CPTCTL	R/W	0h	Internal. Only to be used through TI provided API.
6-5	CNTRSRC	R/W	0h	Internal. Only to be used through TI provided API.
4	CNTRCLR	R/W	0h	Internal. Only to be used through TI provided API.
3	CNTRCTL	R/W	0h	Internal. Only to be used through TI provided API.
2-1	TIMSRC	R/W	0h	Internal. Only to be used through TI provided API.
0	TIMCTL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.35 TIMINC Register (Offset = 868h) [Reset = 00000000h]

TIMINC is shown in Table 13-38.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-38. TIMINC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.36 TIMPER Register (Offset = 86Ch) [Reset = 00000000h]

TIMPER is shown in Table 13-39.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-39. TIMPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.37 TIMCNT Register (Offset = 870h) [Reset = 00000000h]

TIMCNT is shown in Table 13-40.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-40. TIMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

13.9.38 TIMCAPT Register (Offset = 874h) [Reset = 00000000h]

TIMCAPT is shown in Table 13-41.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-41. TIMCAPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

13.9.39 LSECTL Register (Offset = 878h) [Reset = 00000000h]

LSECTL is shown in Table 13-42.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-42. LSECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	BITREV	R/W	0h	Internal. Only to be used through TI provided API.
1	SCHEDULING	R/W	0h	Internal. Only to be used through TI provided API.
0	MEMORY	R/W	0h	Internal. Only to be used through TI provided API.

13.9.40 LSESTART Register (Offset = 87Ch) [Reset = 00000000h]

LSESTART is shown in Table 13-43.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-43. LSESTART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	INITDST	W	0h	Internal. Only to be used through TI provided API.
0	START	W	0h	Internal. Only to be used through TI provided API.

13.9.41 LSEBASESRCA Register (Offset = 880h) [Reset = 00000000h]

LSEBASESRCA is shown in Table 13-44.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-44. LSEBASESRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.42 LSEMODESRCA Register (Offset = 884h) [Reset = 00000000h]

LSEMODESRCA is shown in Table 13-45.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-45. LSEMODESRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.43 LSESUBMODESRCA Register (Offset = 888h) [Reset = 00000000h]

LSESUBMODESRCA is shown in Table 13-46.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-46. LSESUBMODESRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.44 LSENSRCA Register (Offset = 88Ch) [Reset = 00000000h]

LSENSRCA is shown in Table 13-47.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-47. LSENSRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.45 LSEMSRCA Register (Offset = 890h) [Reset = 00000000h]

LSEMSRCA is shown in Table 13-48.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-48. LSEMSRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.46 LSEELEMENTSRCA Register (Offset = 894h) [Reset = 00000000h]

LSEELEMENTSRCA is shown in Table 13-49.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-49. LSEELEMENTSRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.47 LSESTRIDESRCA Register (Offset = 898h) [Reset = 00000000h]

LSESTRIDESRCA is shown in Table 13-50.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-50. LSESTRIDESRCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.48 LSEBASEDSTA Register (Offset = 89Ch) [Reset = 00000000h]

LSEBASEDSTA is shown in Table 13-51.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-51. LSEBASEDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.49 LSEMODEDSTA Register (Offset = 8A0h) [Reset = 00000000h]

LSEMODEDSTA is shown in Table 13-52.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-52. LSEMODEDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.50 LSESUBMODEDSTA Register (Offset = 8A4h) [Reset = 00000000h]

LSESUBMODEDSTA is shown in Table 13-53.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-53. LSESUBMODEDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.51 LSENDSTA Register (Offset = 8A8h) [Reset = 00000000h]

LSENDSTA is shown in Table 13-54.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-54. LSENDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.52 LSEMDSTA Register (Offset = 8ACh) [Reset = 00000000h]

LSEMDSTA is shown in Table 13-55.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-55. LSEMDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.53 LSEELEMENTDSTA Register (Offset = 8B0h) [Reset = 00000000h]

LSEELEMENTDSTA is shown in Table 13-56.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-56. LSEELEMENTDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.54 LSESTRIDEDSTA Register (Offset = 8B4h) [Reset = 00000000h]

LSESTRIDEDSTA is shown in Table 13-57.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-57. LSESTRIDEDSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.55 LSEBASESRCB Register (Offset = 8B8h) [Reset = 00000000h]

LSEBASESRCB is shown in Table 13-58.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-58. LSEBASESRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.56 LSEMODESRCB Register (Offset = 8BCh) [Reset = 00000000h]

LSEMODESRCB is shown in Table 13-59.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-59. LSEMODESRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.57 LSESUBMODESRCB Register (Offset = 8C0h) [Reset = 00000000h]

LSESUBMODESRCB is shown in Table 13-60.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-60. LSESUBMODESRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.58 LSENSRCB Register (Offset = 8C4h) [Reset = 00000000h]

LSENSRCB is shown in Table 13-61.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-61. LSENSRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.59 LSEMSRCB Register (Offset = 8C8h) [Reset = 00000000h]

LSEMSRCB is shown in Table 13-62.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-62. LSEMSRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.60 LSEELEMENTSRCB Register (Offset = 8CCh) [Reset = 00000000h]

LSEELEMENTSRCB is shown in Table 13-63.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-63. LSEELEMENTSRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.61 LSESTRIDESRCB Register (Offset = 8D0h) [Reset = 00000000h]

LSESTRIDESRCB is shown in Table 13-64.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-64. LSESTRIDESRCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.62 LSEBASEDSTB Register (Offset = 8D4h) [Reset = 00000000h]

LSEBASEDSTB is shown in Table 13-65.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-65. LSEBASEDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.63 LSEMODEDSTB Register (Offset = 8D8h) [Reset = 00000000h]

LSEMODEDSTB is shown in Table 13-66.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-66. LSEMODEDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.64 LSESUBMODEDSTB Register (Offset = 8DCh) [Reset = 00000000h]

LSESUBMODEDSTB is shown in Table 13-67.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-67. LSESUBMODEDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.65 LSENDSTB Register (Offset = 8E0h) [Reset = 00000000h]

LSENDSTB is shown in Table 13-68.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-68. LSENDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.66 LSEMDSTB Register (Offset = 8E4h) [Reset = 00000000h]

LSEMDSTB is shown in Table 13-69.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-69. LSEMDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.67 LSEELEMENTDSTB Register (Offset = 8E8h) [Reset = 00000000h]

LSEELEMENTDSTB is shown in Table 13-70.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-70. LSEELEMENTDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.68 LSESTRIDEDSTB Register (Offset = 8ECh) [Reset = 00000000h]

LSESTRIDEDSTB is shown in Table 13-71.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-71. LSESTRIDEDSTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.69 XBAR0 Register (Offset = 8F0h) [Reset = 00000000h]

XBAR0 is shown in Table 13-72.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-72. XBAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	OUTSRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
13-12	OUTSRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
11-10	B3SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
9-8	B3SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
7-6	B2SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
5-4	B2SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
3-2	B1SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
1-0	B1SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.

13.9.70 XBAR1 Register (Offset = 8F4h) [Reset = 00000000h]

XBAR1 is shown in Table 13-73.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-73. XBAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	OUTSRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
13-12	OUTSRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
11-10	B3SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
9-8	B3SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
7-6	B2SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
5-4	B2SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
3-2	B1SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
1-0	B1SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.

13.9.71 XBAR2 Register (Offset = 8F8h) [Reset = 00000000h]

XBAR2 is shown in Table 13-74.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-74. XBAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	OUTSRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
13-12	OUTSRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
11-10	B3SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
9-8	B3SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
7-6	B2SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
5-4	B2SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.
3-2	B1SRCSELB	R/W	0h	Internal. Only to be used through TI provided API.
1-0	B1SRCSELA	R/W	0h	Internal. Only to be used through TI provided API.

13.9.72 R2C Register (Offset = 8FCh) [Reset = 00000000h]

R2C is shown in Table 13-75.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-75. R2C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	OP	R/W	0h	Internal. Only to be used through TI provided API.

13.9.73 FMUL0 Register (Offset = 900h) [Reset = 00000000h]

FMUL0 is shown in Table 13-76.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-76. FMUL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	RNDADDSUB	R/W	0h	Internal. Only to be used through TI provided API.
3-1	RNDMUL	R/W	0h	Internal. Only to be used through TI provided API.
0	OP	R/W	0h	Internal. Only to be used through TI provided API.

13.9.74 FMUL1 Register (Offset = 904h) [Reset = 00000000h]

FMUL1 is shown in Table 13-77.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-77. FMUL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	RNDADDSUB	R/W	0h	Internal. Only to be used through TI provided API.
3-1	RNDMUL	R/W	0h	Internal. Only to be used through TI provided API.
0	OP	R/W	0h	Internal. Only to be used through TI provided API.

13.9.75 UCRD Register (Offset = 908h) [Reset = 00000000h]

UCRD is shown in Table 13-78.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-78. UCRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MODE	R/W	0h	Internal. Only to be used through TI provided API.

13.9.76 ADDSUB Register (Offset = 90Ch) [Reset = 00000000h]

ADDSUB is shown in Table 13-79.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-79. ADDSUB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-2	RNDADD	R/W	0h	Internal. Only to be used through TI provided API.
1-0	OP	R/W	0h	Internal. Only to be used through TI provided API.

13.9.77 ADDSUBDECACC Register (Offset = 910h) [Reset = 00000000h]

ADDSUBDECACC is shown in Table 13-80.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-80. ADDSUBDECACC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.78 ADDSUBSTAT Register (Offset = 914h) [Reset = 00000000h]

ADDSUBSTAT is shown in Table 13-81.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-81. ADDSUBSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	LASTSIGNIM	R	0h	Internal. Only to be used through TI provided API.
0	LASTSIGNRE	R	0h	Internal. Only to be used through TI provided API.

13.9.79 MAXMIN Register (Offset = 918h) [Reset = 00000000h]

MAXMIN is shown in Table 13-82.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-82. MAXMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	OP	R/W	0h	Internal. Only to be used through TI provided API.

13.9.80 MAXMINDECACC Register (Offset = 91Ch) [Reset = 00000000h]

MAXMINDECACC is shown in Table 13-83.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-83. MAXMINDECACC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

13.9.81 MAXMININDEX Register (Offset = 920h) [Reset = 00000000h]

MAXMININDEX is shown in Table 13-84.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-84. MAXMININDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	VAL	R	0h	Internal. Only to be used through TI provided API.

13.9.82 FX2FP Register (Offset = 924h) [Reset = 00000000h]

FX2FP is shown in Table 13-85.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-85. FX2FP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-1	RND	R/W	0h	Internal. Only to be used through TI provided API.
0	OP	R/W	0h	Internal. Only to be used through TI provided API.

13.9.83 FX2FPR Register (Offset = 928h) [Reset = 00000000h]

FX2FPR is shown in Table 13-86.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-86. FX2FPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	R	R/W	0h	Internal. Only to be used through TI provided API.

13.9.84 FX2FPCONVR Register (Offset = 92Ch) [Reset = 00000000h]

FX2FPCONVR is shown in Table 13-87.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-87. FX2FPCONVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	INIT	W	0h	Internal. Only to be used through TI provided API.

13.9.85 FDIV Register (Offset = 930h) [Reset = 00000000h]

FDIV is shown in Table 13-88.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-88. FDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	RND	R/W	0h	Internal. Only to be used through TI provided API.

13.9.86 FDIVSTAT Register (Offset = 934h) [Reset = 00000000h]

FDIVSTAT is shown in Table 13-89.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-89. FDIVSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DIVZERO	R	0h	Internal. Only to be used through TI provided API.

13.9.87 CFG Register (Offset = C00h) [Reset = 00000000h]

CFG is shown in Table 13-90.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-90. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-7	PRESCAL	R/W	0h	Internal. Only to be used through TI provided API.
6	TSCLR	W	0h	Internal. Only to be used through TI provided API.
5	TSEN	R/W	0h	Internal. Only to be used through TI provided API.
4-3	CH3EN	R/W	0h	Internal. Only to be used through TI provided API.
2-1	CH2EN	R/W	0h	Internal. Only to be used through TI provided API.
0	CH1EN	R/W	0h	Internal. Only to be used through TI provided API.

13.9.88 CH1CMD Register (Offset = C04h) [Reset = 00000000h]

CH1CMD is shown in Table 13-91.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-91. CH1CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
7-3	RESERVED	R	0h	Reserved
2-0	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.

13.9.89 CH2CMD Register (Offset = C08h) [Reset = 00000000h]

CH2CMD is shown in Table 13-92.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-92. CH2CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
7-3	RESERVED	R	0h	Reserved
2-0	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.

13.9.90 CH3CMD Register (Offset = C0Ch) [Reset = 00000000h]

CH3CMD is shown in Table 13-93.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-93. CH3CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
7-3	RESERVED	R	0h	Reserved
2-0	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.

13.9.91 CH1PAR01 Register (Offset = C14h) [Reset = 00000000h]

CH1PAR01 is shown in Table 13-94.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-94. CH1PAR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR1	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR0	R/W	0h	Internal. Only to be used through TI provided API.

13.9.92 CH2PAR01 Register (Offset = C18h) [Reset = 00000000h]

CH2PAR01 is shown in Table 13-95.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-95. CH2PAR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR1	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR0	R/W	0h	Internal. Only to be used through TI provided API.

13.9.93 CH3PAR01 Register (Offset = C1Ch) [Reset = 00000000h]

CH3PAR01 is shown in Table 13-96.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-96. CH3PAR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR1	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR0	R/W	0h	Internal. Only to be used through TI provided API.

13.9.94 CH1PAR23 Register (Offset = C24h) [Reset = 00000000h]

CH1PAR23 is shown in Table 13-97.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-97. CH1PAR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR3	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR2	R/W	0h	Internal. Only to be used through TI provided API.

13.9.95 CH2PAR23 Register (Offset = C28h) [Reset = 00000000h]

CH2PAR23 is shown in Table 13-98.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-98. CH2PAR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR3	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR2	R/W	0h	Internal. Only to be used through TI provided API.

13.9.96 CH3PAR23 Register (Offset = C2Ch) [Reset = 00000000h]

CH3PAR23 is shown in Table 13-99.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 13-99. CH3PAR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR3	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR2	R/W	0h	Internal. Only to be used through TI provided API.

Chapter 14

Voltage Glitch Monitor (VGM)

This section describes the Voltage Glitch Monitor (VGM)

14.1 Overview

The CC27xx devices include a Voltage Glitch Monitor (VGM) for security reasons to detect any physical tampering of the VDDD supply rail which is brought out to a device pin for a decoupling capacitor connection. The purpose of the VGM module is to detect any glitch on the VDDD rail during the boot up process to trigger device reset thereby preventing any kind of disturbance or instruction bypass during boot code execution. The VGM is enabled automatically when the device is powered on or reset so that it is always operational during device boot up. It remains enabled post boot and user software may disable the VGM module if it is not required for the application.

14.2 Features and operation

The VGM module monitors the VDDD supply rail for any positive or negative glitches which means detection of overshoot or undershoot conditions and triggers a device reset. It detects transients or glitches on the VDDD supply pin at the rate of 100 MV/s to 2 GV/s and it detects glitches with a minimum width of 1-2ns. When the VGM module is enabled it is ready for operation in a maximum of 70us.

The VGM digital logic and configuration bits are implemented in SYS0 and PMCTL modules. The VGMCFG register in SYS0 contains 2 separate bits to disable the undershoot detector and overshoot detector. The reset value of these 2 disable bits is 0 so that both the detector circuits in VGM are enabled once the VDDD domain is powered and comes out of reset to start device boot up.

The VGM module remains enabled after boot up so the user application can take advantage of this module if useful for the application, else the individual detectors of VGM can be disabled through the VGMCFG register. Both of the VGM detectors can be individually disabled and re-enabled by software at a later point if needed. VGM detectors will be automatically enabled by hardware upon power cycle or shut down exit or any of the other chip reset conditions. The outputs from the undershoot and overshoot detectors are combined (logical OR) inside the VGM analog module to generate a reset request output. When VGM is enabled it always triggers a device reset when it detects a glitch on VDDD and this reset can not be masked.

When VGM undershoot and/or overshoot detectors are kept enabled by the user application, then they are disabled during standby entry and are automatically re-enabled by hardware upon wake up. There is no need for VGM operation in standby as the VDDD supply is turned off. The VGM enable qualifier signal from the PMCTL is used inside the SYS0 module to override the VGM enables during standby entry. VGM module is disabled by hardware and is not operational in shutdown mode.

VGM enable status is signaled by SYS0 to PMCTL based on USHTDETDIS and OSHTDETDIS bits in the VGMCFG register. When VGM is disabled, PMCTL does not delay the SVT reset release. When VGM is enabled, PMCTL checks the value of the user policy bit in its MMR. If the value is 0 (default case) it will wait for the VGM ready signal to get asserted by VGM analog. VGM ready is asserted by VGM analog to PMCTL once it fully settles and it may take up to 70us maximum. VGM reset request output will be gated within VGM analog until it fully settles and VGM ready is generated. Once PMCTL observes VGM ready getting set, it releases SVT reset. When the user policy bit is programmed to a value of 1, PMCTL does not wait for VGM ready from VGM analog and proceeds with SVT reset release.

VGM will be enabled by default so PMCTL will always delay SVT reset release until VGM ready is received and this will be the behavior for cold power up, pin reset, internal chip resets and shutdown exit. The user needs to program the policy bit value to 1 in PMCTL if no impact to standby wake latency (~40us) is desired, else the policy bit default value of 0 will impact the standby latency by up to a maximum of ~70us. Since the user policy bit is implemented in PMCTL MMR it is retained during standby and the setting takes effect during standby exit operation. Refer to the device specific datasheet for standby exit latencies for both values of the PMCTL policy bit when VGM is enabled.

Note

Refer to SYS0 chapter for VGMCFG MMR description of VGM module.

Chapter 15

System Timer (SYSTIM)

This chapter discusses the features and configurations of the System Timer (SYSTIM) module.

15.1 Overview

SYSTIM is a 34-bit timer running at a resolution of 250 ns with a low range (about 1.2 hr) but high precision (of 250 ns) that can be used by both the RF-Core and the system CPU. SYSTIM follows the RTC (Chapter 16) and can only be used in device ACTIVE state. The SYSTIM synchronizes with the RTC. This is done during start-up and continuously during ACTIVE state. When the device goes from STANDBY/RESET/SHUTDOWN to ACTIVE the value of the RTC time is loaded to SYSTIM with a resolution of 250 ns.

SYSTIM has six channels:

- 3 channels with capture and compare dedicated to RF-Core
  - Channels 2, 3, and 4
  - These channels work with 250 ns compare and capture value
  - These channels are reserved for radio functions
- 1 channel with capture and compare for the system software
  - Channel 0
  - Works with 1 µs resolution compare and capture value
  - This channel is reserved for TI Software functions
- 2 channels in backup with capture and compare
  - Channel 1 and channel 5
  - Configurable for 1 µs or 250 ns resolution
  - These channels is available for custom use cases

15.2 Block Diagram

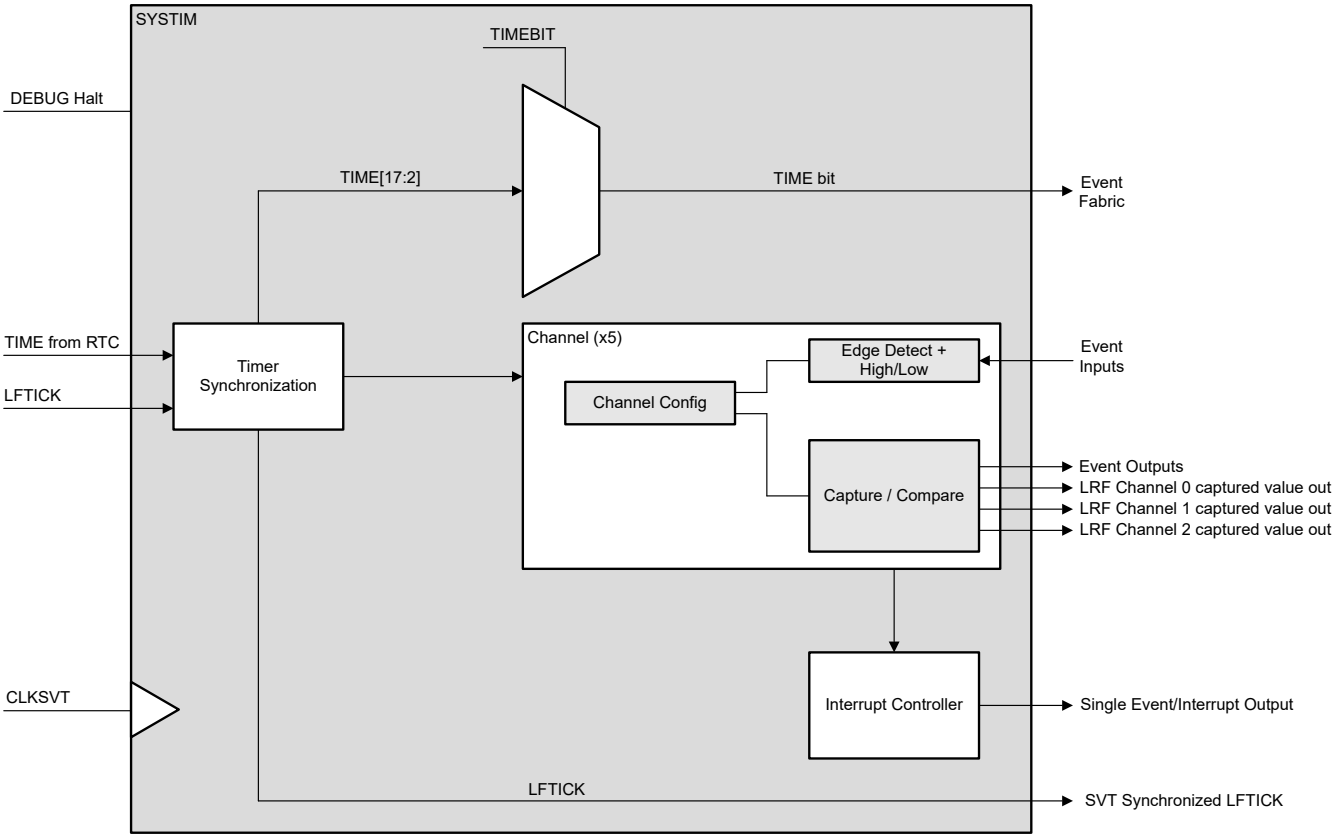


Figure 15-1. SYSTIM Block Diagram

15.3 Functional Description

15.3.1 Common Channel Features

15.3.1.1 Compare Mode

A channel is automatically armed in compare mode by writing any value to SYSTIM.CH*n*VAL[31:0] DATA bit field.

Once programmed in compare mode the channel generates an event when SYSTIM time reaches the programmed value.

The SYSTIM channel generates an event immediately if the value programmed is within a certain limit in the past. This limit is 4 seconds in the past for 1 µs resolution channels. And the limit is 1 second in the past for 250 ns resolution channel.

15.3.1.2 Capture Mode

A channel can be armed in Capture mode by setting the SYSTIM.CH*n*CFG[0] MODE bit to 1.

In capture mode the channel captures the 32 bits of SYSTIM time based on the event which the channel receives. The resolution of these 32 bits is based on the type of channel which is being used. The capture can be configured on different edges of the input event . For more details refer to the SYSTIM.CH*n*CFG register.

By default a channel is disarmed after capture happens. The SYSTIM.CH*n*CFG[0] MODE bit is cleared to 0.

15.3.1.3 Additional Channel Arming Methods

In addition to the previously mentioned methods for arming a channel, a channel can be armed via programming the ARMSET register. When the SYSTIM.CH*n*CFG[0] MODE bit is 0 and SYSTIM.ARMSET[*n*] CH*n* bit is set for that channel, the channel is armed in compare mode and starts comparison based on the current CH*n*VAL register value.

When SYSTIM.CH*n*CFG[3] REARM is set to 1, rearm is enabled. The channel remains in continuous capture mode. Otherwise the channel is in one-shot capture mode. Re-arm is only valid for capture mode.

A channel can be disarmed by setting the SYSTIM.ARMCLR[*n*] CH*n* bit to 1. ARMCLR disarms the channel and resets the SYSTIM.CH*n*CFG[0] MODE bit to 0.

The CHnSR register can be written to load the channel with a value without triggering the channel to enter compare mode. Then ARMSET can be used to arm the channel in Compare mode by setting the ARMSET[n], provided the CHnCFG[0] MODE is zero.

15.3.2 Interrupts and Events

- SYSTIM capture/compare event
  - SYSTIM event output:
    - One event output per channel + one combined event output for all the channels routed to the MCU event fabric.
    - Total of 6+1 event outputs. Only the combined event has a standard complement of MIS/RIS/IMASK/ ISET/ICLR/IMCLR/IMSET registers. RIS is automatically cleared when reading capture value or writing compare value.
      - The combined event also includes a timer overflow event. This event is asserted when time overflows and remain asserted till 4sec.
    - The event set within RIS can be cleared via ICLR, and also when any of the following occurs:
      - Reading from the capture register (this only occurs if the channel is in capture mode or disarmed).
      - Writing to the compare register.
      - Arming the channel in capture mode via writing CH ***n*** CFG.MODE bit to 1.
      - Arming the channel in compare mode via writing ARMSET ***n*** bit to 1, provided CH ***n*** CFG.MODE bit as 0.

    - Trigger past event
        - A compare event triggers immediately if 0 <= TIME-CMP < 2^22, in other words if the compare time is now or up to 1.048576s in the past for LRF channel, and up to 4.294s in the past for system and backup channels (if the backup channel is configured to 1 µs resolution).
- SYSTIM event inputs:
    - One event input per channel.
    - Can be configured to capture on a configurable condition (rising edge, falling edge and both edges). This also generates a capture event output on the same channel, setting the RIS interrupt flag.
    - The SYSTIM.CH*n*CFG[2:1] INP bit field can be used to configure the capture condition.
        - If SYSTIM.CH*n*CFG[2:1] INP bit field = 0 then capture on the rising edge.
        - If SYSTIM.CH*n*CFG[2:1] INP bit field = 1 then capture on the falling edge.
        - If SYSTIM.CH*n*CFG[2:1] INP bit field = 2 then capture on both rising and falling edges.
    - Software must arm a channel for capture, and a capture event automatically disarms the channel.

15.4 SYSTIM Registers

Table 15-1 lists the memory-mapped registers for the SYSTIM registers. All register offset addresses not listed in Table 15-1 should be considered as reserved locations and the register contents should not be modified.

Table 15-1. SYSTIM Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 15.4.1
44h	IMASK	Interrupt mask	Section 15.4.2
48h	RIS	Raw interrupt status	Section 15.4.3
4Ch	MIS	Masked interrupt status	Section 15.4.4
50h	ISET	Interrupt set	Section 15.4.5
54h	ICLR	Interrupt clear	Section 15.4.6
58h	IMSET	Interrupt mask set	Section 15.4.7
5Ch	IMCLR	Interrupt mask clear	Section 15.4.8
60h	EMU	Emulation	Section 15.4.9
100h	TIME250N	Systime Count Value [31:0]	Section 15.4.10
104h	TIME1U	Systime Count Value [33:2]	Section 15.4.11
108h	OUT	channel's Ouput Value	Section 15.4.12
10Ch	CH0CFG	channel0 Configuration.	Section 15.4.13
110h	CH1CFG	channel1 Configuration.	Section 15.4.14
114h	CH2CFG	channel2 Configuration.	Section 15.4.15
118h	CH3CFG	channel3 Configuration.	Section 15.4.16
11Ch	CH4CFG	channel4 Configuration.	Section 15.4.17
120h	CH0CC	Channel 0 Capture/Compare Value	Section 15.4.18
124h	CH1CC	Channel 1 Capture/Compare Value	Section 15.4.19
128h	CH2CC	Channel 2 Capture/Compare Value	Section 15.4.20
12Ch	CH3CC	Channel 3 Capture/Compare Value	Section 15.4.21
130h	CH4CC	Channel 4 Capture/Compare Value	Section 15.4.22
134h	TIMEBIT	Systimer's Time bit	Section 15.4.23
140h	STATUS	Timer Status	Section 15.4.24
144h	ARMSET	Channel arming set	Section 15.4.25
148h	ARMCLR	Channel Arming clear	Section 15.4.26
14Ch	CH0CCSR	Channel 0 Save/Restore Value	Section 15.4.27
150h	CH1CCSR	Channel 1 Save/Restore Value	Section 15.4.28
154h	CH2CCSR	Channel 2 Save/Restore Value	Section 15.4.29
158h	CH3CCSR	Channel 3 Save/Restore Value	Section 15.4.30
15Ch	CH4CCSR	Channel 4 Save/Restore Value	Section 15.4.31
160h	CH5CCSR	Channel 5 Save/Restore Value	Section 15.4.32
164h	CH5CFG	channel5 Configuration.	Section 15.4.33
168h	CH5CC	Channel 5 Capture/Compare Value	Section 15.4.34

Complex bit access types are encoded to fit into small table cells. Table 15-2 shows the codes that are used for access types in this section.

Table 15-2. SYSTIM Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 15-2. SYSTIM Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

15.4.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 15-3.

Return to the Summary Table.

Description. ;This register identifies the peripheral and its exact version.

Table 15-3. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	9443h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exists in SOC, this field can identify the instance number 0-15
7-4	MAJREV	R	1h	Major revision of IP 0-15
3-0	MINREV	R	0h	Minor revision of IP 0-15.

15.4.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 15-4.

Return to the Summary Table.

Interrupt mask. ;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 15-4. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	R/W	0h	Systimer counter overflow event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask
5	EV5	R/W	0h	Systimer channel 5 event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask
4	EV4	R/W	0h	Systimer channel 4 event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask
3	EV3	R/W	0h	Systimer channel 3 event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask
2	EV2	R/W	0h	Systimer channel 2 event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask
1	EV1	R/W	0h	Systimer channel 1 event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask
0	EV0	R/W	0h	Systimer channel 0 event interrupt mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask

15.4.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 15-5.

Return to the Summary Table.

Raw interrupt status. ;This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 15-5. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	R	0h	Raw interrupt status for Systimer counter overflow event.;This bit is set to 1 when an event is received on SysTimer Overflow occurs. 0h = Interrupt did not occur 1h = Interrupt occured
5	EV5	R	0h	Raw interrupt status for channel 5 event.;This bit is set to 1 when a CAPTURE or COMPARE event is received on channel 5. 0h = Interrupt did not occur 1h = Interrupt occured
4	EV4	R	0h	Raw interrupt status for channel 4 event.;This bit is set to 1 when a CAPTURE or COMPARE event is received on channel 4. 0h = Interrupt did not occur 1h = Interrupt occured
3	EV3	R	0h	Raw interrupt status for channel 3 event.;This bit is set to 1 when a CAPTURE or COMPARE event is received on channel 3. 0h = Interrupt did not occur 1h = Interrupt occured
2	EV2	R	0h	Raw interrupt status for channel 2 Event.;This bit is set to 1 when a CAPTURE or COMPARE event is received on channel 2. 0h = Interrupt did not occur 1h = Interrupt occured
1	EV1	R	0h	Raw interrupt status for channel 1 event.;This bit is set to 1 when a CAPTURE or COMPARE event is received on channel 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	EV0	R	0h	Raw interrupt status for channel 0 event.;This bit is set to 1 when a CAPTURE or COMPARE event is received on channel 0. 0h = Interrupt did not occur 1h = Interrupt occured

15.4.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 15-6.

Return to the Summary Table.

Masked interrupt status. ;This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 15-6. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	R	0h	Mask Interrupt status for Systimer counter overflow Event in MIS register. 0h = Interrupt did not occur 1h = Interrupt occured
5	EV5	R	0h	Mask interrupt status for channel 5 event. 0h = Interrupt did not occur 1h = Interrupt occured
4	EV4	R	0h	Mask interrupt status for channel 4 event. 0h = Interrupt did not occur 1h = Interrupt occured
3	EV3	R	0h	Mask interrupt status for channel 3 event. 0h = Interrupt did not occur 1h = Interrupt occured
2	EV2	R	0h	Mask interrupt status for channel 2 event. 0h = Interrupt did not occur 1h = Interrupt occured
1	EV1	R	0h	Mask interrupt status for channel 1 event. 0h = Interrupt did not occur 1h = Interrupt occured
0	EV0	R	0h	Mask interrupt status for channel 0 event. 0h = Interrupt did not occur 1h = Interrupt occured

15.4.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 15-7.

Return to the Summary Table.

Interrupt set.; ;This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 15-7. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Sets Systimer counter overflow interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
5	EV5	W	0h	Sets channel 5 interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
4	EV4	W	0h	Sets channel 4 interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
3	EV3	W	0h	Sets channel 3 interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
2	EV2	W	0h	Sets channel 2 interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
1	EV1	W	0h	Sets channel 1 interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
0	EV0	W	0h	Sets channel 0 interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt

15.4.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 15-8.

Return to the Summary Table.

Interrupt clear.;'This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 15-8. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Clears Systimer counter overflow interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
5	EV5	W	0h	Clears channel 5 interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	EV4	W	0h	Clears channel 4 interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	EV3	W	0h	Clears channel 3 interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
2	EV2	W	0h	Clears channel 2 interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
1	EV1	W	0h	Clears channel 1 interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	EV0	W	0h	Clears channel 0 interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt

15.4.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 15-9.

Return to the Summary Table.

Interrupt mask set. ;Writing a 1 to a bit in this register will set the corresponding IMASK bit.

Table 15-9. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Sets Timer Overflow Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Set interrupt mask
5	EV5	W	0h	Sets channel5 Event Interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
4	EV4	W	0h	Sets channel4 Event Interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
3	EV3	W	0h	Sets channel3 Event Interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
2	EV2	W	0h	Sets channel2 Event Interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
1	EV1	W	0h	Sets channel1 Event Interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
0	EV0	W	0h	Sets channel0 Event Interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask

15.4.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 15-10.

Return to the Summary Table.

Interrupt mask clear. ;Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 15-10. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	OVFL	W	0h	Clears Timer Overflow Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask
5	EV5	W	0h	Clears channel5 Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask
4	EV4	W	0h	Clears channel4 Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask
3	EV3	W	0h	Clears channel3 Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask
2	EV2	W	0h	Clears channel2 Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask
1	EV1	W	0h	Clears channel1 Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask
0	EV0	W	0h	Clears channel0 Event Interrupt Mask. 0h = Writing 0 has no effect 1h = Clear interrupt mask

15.4.9 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 15-11.

Return to the Summary Table.

Emulation control. ;This register controls the behavior of the IP related to core halted input.

Table 15-11. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HALT	R/W	0h	Halt control. 0h = Free run option. The IP ignores the state of the core halted input. 1h = Freeze option. The IP freezes functionality when the core halted input is asserted, and resumes when it is deasserted. The freeze can either be immediate or after the IP has reached a boundary from where it can resume without corruption.

15.4.10 TIME250N Register (Offset = 100h) [Reset = 00000000h]

TIME250N is shown in Table 15-12.

Return to the Summary Table.

Systimer Counter Value - 250ns resolution. ;This 32-bit value reads out bits [31:0] of the systimer counter. The counter is 34-bit and runs on CLKSVT/12. It maintains a resolution of 250ns with a range of about 17.9m.

Table 15-12. TIME250N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	32-bit counter value [31:0]. This will provide a 250ns resolution and a range of 17.9m.

15.4.11 TIME1U Register (Offset = 104h) [Reset = 00000000h]

TIME1U is shown in Table 15-13.

Return to the Summary Table.

Systimer Counter Value - 1µs resolution ;This 32-bit value reads out bits[33:2] of the systimer counter. The counter is 34-bit and runs on CLKSVT/12. It maintains a resolution of 1us with a range of about 1 h 11m.

Table 15-13. TIME1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	32-bit counter value [33:2]. This will provide a resolution of 1us and a range of 1hr and 11m.

15.4.12 OUT Register (Offset = 108h) [Reset = 00000000h]

OUT is shown in Table 15-14.

Return to the Summary Table.

Systimer's channel Output Event Values

Table 15-14. OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	OUT5	R	0h	Output Value of channel 5. 0h = Event did not occur. 1h = Event occured
4	OUT4	R	0h	Output Value of channel 4. 0h = Event did not occur. 1h = Event occured
3	OUT3	R	0h	Output Value of channel 3. 0h = Event did not occur. 1h = Event occured
2	OUT2	R	0h	Output Value of channel 2. 0h = Event did not occur. 1h = Event occured
1	OUT1	R	0h	Output Value of channel 1. 0h = Event did not occur. 1h = Event occured
0	OUT0	R	0h	Output Value of channel 0. 0h = Event did not occur. 1h = Event occured

15.4.13 CH0CFG Register (Offset = 10Ch) [Reset = 00000000h]

CH0CFG is shown in Table 15-15.

Return to the Summary Table.

Systimer channel 0 configuration. ;This channel has configurability for 250ns and 1us based capture and compare operations.

Table 15-15. CH0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RES	R/W	0h	This bit decides the RESOLUTION of the channel that will be used. 0h = channel Works in Timer's 1us Resolution. 1h = channel Works in Timer's 250ns resolution
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in one shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function. 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = channel is disabled 1h = channel is in capture mode

15.4.14 CH1CFG Register (Offset = 110h) [Reset = 00000000h]

CH1CFG is shown in Table 15-16.

Return to the Summary Table.

Systimer channel 1 configuration. ;This channel works in 1us based capture and compare operations.

Table 15-16. CH1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in one shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = channel is disabled 1h = channel is in capture mode

15.4.15 CH2CFG Register (Offset = 114h) [Reset = 00000000h]

CH2CFG is shown in Table 15-17.

Return to the Summary Table.

Systimer channel 2 configuration. ;This channel works in 250ns based capture and compare operations.

Table 15-17. CH2CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in one shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = channel is disabled 1h = channel is in capture mode

15.4.16 CH3CFG Register (Offset = 118h) [Reset = 00000000h]

CH3CFG is shown in Table 15-18.

Return to the Summary Table.

Systimer channel 3 configuration. ;This channel works in 250ns based capture and compare operations.

Table 15-18. CH3CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in one shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = channel is disabled 1h = channel is in capture mode

15.4.17 CH4CFG Register (Offset = 11Ch) [Reset = 00000000h]

CH4CFG is shown in Table 15-19.

Return to the Summary Table.

Systimer channel 4 configuration. ;This channel works in 250ns based capture and compare operations.

Table 15-19. CH4CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in one shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = channel is disabled 1h = channel is in capture mode

15.4.18 CH0CC Register (Offset = 120h) [Reset = 00000000h]

CH0CC is shown in Table 15-20.

Return to the Summary Table.

System Timer channel 0 Capture/Compare register. ;This register when written with any compare value will arm the channel to work in compare mode. Reads to this register will clear the Corresponding RIS.EV0 bit.

Table 15-20. CH0CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.19 CH1CC Register (Offset = 124h) [Reset = 00000000h]

CH1CC is shown in Table 15-21.

Return to the Summary Table.

System Timer channel 1 Capture/Compare register. ;This register when written with any compare value will arm the channel to work in compare mode. Reads to this register will clear the Corresponding RIS.EV1 bit.

Table 15-21. CH1CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.20 CH2CC Register (Offset = 128h) [Reset = 00000000h]

CH2CC is shown in Table 15-22.

Return to the Summary Table.

System Timer channel 2 Capture/Compare register. ;This register when written with any compare value will arm the channel to work in compare mode. Reads to this register will clear the Corresponding RIS.EV2 bit.

Table 15-22. CH2CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.21 CH3CC Register (Offset = 12Ch) [Reset = 00000000h]

CH3CC is shown in Table 15-23.

Return to the Summary Table.

System Timer channel 3 Capture/Compare register. ;This register when written with any compare value will arm the channel to work in compare mode. Reads to this register will clear the Corresponding RIS.EV3 bit.

Table 15-23. CH3CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.22 CH4CC Register (Offset = 130h) [Reset = 00000000h]

CH4CC is shown in Table 15-24.

Return to the Summary Table.

System Timer channel 4 Capture/Compare register. ;This register when written with any compare value will arm the channel to work in compare mode. Reads to this register will clear the Corresponding RIS.EV4 bit.

Table 15-24. CH4CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.23 TIMEBIT Register (Offset = 134h) [Reset = 00000000h]

TIMEBIT is shown in Table 15-25.

Return to the Summary Table.

Systimer's Time bit.;This Register will be used to specify which TIME bit is required by LGPT to be forwarded from SYSTIMER.

Table 15-25. TIMEBIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	The corresponding bit will have value '1' rest should be '0'. If more than one bit is asserted, output is "or" of all the bits. 0h = No bit is forwarded to the event fabric. 1h = Bit2 is forwarded to the event fabric. 2h = Bit3 is forwarded to the event fabric. 4h = Bit4 is forwarded to the event fabric. 8h = Bit5 is forwarded to the event fabric. 10h = Bit6 is forwarded to the event fabric. 20h = Bit7 is forwarded to the event fabric. 40h = Bit8 is forwarded to the event fabric. 80h = Bit9 is forwarded to the event fabric. 100h = Bit10 is forwarded to the event fabric. 200h = Bit11 is forwarded to the event fabric. 400h = Bit12 is forwarded to the event fabric. 800h = Bit13 is forwarded to the event fabric. 1000h = Bit14 is forwarded to the event fabric. 2000h = Bit15 is forwarded to the event fabric. 4000h = Bit16 is forwarded to the event fabric. 8000h = Bit17 is forwarded to the event fabric.

15.4.24 STATUS Register (Offset = 140h) [Reset = 00000000h]

STATUS is shown in Table 15-26.

Return to the Summary Table.

Systimer status.;This register can be used to read the running status of the timer and to resync the Systimer with RTC.

Table 15-26. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	SYNCUP	R/W	1h	This bit indicates sync status of Systimer with RTC. The bitfield has a reset value of '1', which gets cleared to '0' after the Systimer synchronizes with RTC on the first LFTICK edge. A write to this bit resynchronizes the Systimer with RTC on the next LFTICK edge. A read value of '1' indicates the synchronization is ongoing and a read of '0' indicates the synchronization is done.
3-1	RESERVED	R	0h	Reserved
0	VAL	R	0h	This bit indicates if the system time is initialized and running. 0h = system timer is not running. 1h = system timer is running

15.4.25 ARMSET Register (Offset = 144h) [Reset = 00000000h]

ARMSET is shown in Table 15-27.

Return to the Summary Table.

ARMSET ;Reading this register gives out the status of the 5 channels.; Channel state UNARMED returns 0.; Channel state CAPTURE or COMPARE returns 1.;A write to ARMSET has for each channel the following effect -; If ARMSTA[x]==0 -> no effect; If ARMSTA[x]==1 and channel x is in CAPTURE state then no effect on the channel; Else, set channel in COMPARE mode using existing CHxVAL value

Table 15-27. ARMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	CH5	R/W	0h	Arming channel 5 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 5 is in CAPTURE state then no effect on the channel else it can set channel in COMPARE mode using existing CH4CC.VAL value.
4	CH4	R/W	0h	Arming channel 4 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 4 is in CAPTURE state then no effect on the channel else it can set channel in COMPARE mode using existing CH4CC.VAL value.
3	CH3	R/W	0h	Arming channel 3 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 3 is in CAPTURE state then no effect on the channel else it can set channel in COMPARE mode using existing CH3CC.VAL value
2	CH2	R/W	0h	Arming channel 2 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 2 is in CAPTURE state then no effect on the channel else it can set channel in COMPARE mode using existing CH2CC.VAL value
1	CH1	R/W	0h	Arming channel 1 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 1 is in CAPTURE state then no effect on the channel else it can Set channel in COMPARE mode using existing CH1CC.VAL value
0	CH0	R/W	0h	Arming channel 0 for either compare or capture operation. 0h = No effect on the channel 1h = if channel 0 is in CAPTURE state then no effect on the channel else it can set channel in COMPARE mode using existing CH0CC.VAL value

15.4.26 ARMCLR Register (Offset = 148h) [Reset = 00000000h]

ARMCLR is shown in Table 15-28.

Return to the Summary Table.

ARMCLR ;Read of this register gives out the status of the 5 channels .; Channel state UNARMED returns 0.; Channel state CAPTURE or COMPARE returns 1.;A write to ARMCLR has for each channel the following effect -; If ARMCLR[x]==0 -> no effect.; Else, set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle

Table 15-28. ARMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	CH5	R/W	0h	Disarming channel 5 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle
4	CH4	R/W	0h	Disarming channel 4 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle
3	CH3	R/W	0h	Disarming channel 3 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle
2	CH2	R/W	0h	Disarming channel 2 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle
1	CH1	R/W	0h	Disarming channel 1 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle
0	CH0	R/W	0h	Disarming channel 0 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare/capture event happens in the same cycle

15.4.27 CH0CCSR Register (Offset = 14Ch) [Reset = 00000000h]

CH0CCSR is shown in Table 15-29.

Return to the Summary Table.

Save/restore alias register for channel 0.; ;A read to this register, will give out the value of register CH0CC. Moreover, reads to this register will not have any effects on RIS.EV0 or configuration of the channel.;Write to CH0CCSR sets CH0CC.VAL value of register without affecting channel state or configuration

Table 15-29. CH0CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.28 CH1CCSR Register (Offset = 150h) [Reset = 00000000h]

CH1CCSR is shown in Table 15-30.

Return to the Summary Table.

Save/restore alias register for channel 1.; ;A read to this register, will give out the value of register CH1CC. Moreover, reads to this register will not have any effects on RIS.EV1 or configuration of the channel.;Write to CH1CCSR sets CH1CC.VAL value of register without affecting channel state or configuration.

Table 15-30. CH1CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.29 CH2CCSR Register (Offset = 154h) [Reset = 00000000h]

CH2CCSR is shown in Table 15-31.

Return to the Summary Table.

Save/restore alias register for channel 2.; ;A read to this register, will give out the value of register CH2CC. Moreover, reads to this register will not have any effects on RIS.EV2 or configuration of the channel.;Write to CH2CCSR sets CH2CC.VAL value of register without affecting channel state or configuration.

Table 15-31. CH2CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.30 CH3CCSR Register (Offset = 158h) [Reset = 00000000h]

CH3CCSR is shown in Table 15-32.

Return to the Summary Table.

Save/restore alias register for channel 3.; ;A read to this register, will give out the value of register CH3CC. Moreover, reads to this register will not have any effects on RIS.EV3 or configuration of the channel.;Write to CH3CCSR sets CH3CC.VAL value of register without affecting channel state or configuration.

Table 15-32. CH3CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.31 CH4CCSR Register (Offset = 15Ch) [Reset = 00000000h]

CH4CCSR is shown in Table 15-33.

Return to the Summary Table.

Save/restore alias register for channel 4.; ;A read to this register, will give out the value of register CH4CC. Moreover, reads to this register will not have any effects on RIS.EV4 or configuration of the channel.;Write to CH4CCSR sets CH4CC.VAL value of register without affecting channel state or configuration.

Table 15-33. CH4CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.32 CH5CCSR Register (Offset = 160h) [Reset = 00000000h]

CH5CCSR is shown in Table 15-34.

Return to the Summary Table.

Save/restore alias register for channel 5.; ;A read to this register, will give out the value of register CH5CC. Moreover, reads to this register will not have any effects on RIS.EV5 or configuration of the channel.;Write to CH5CCSR sets CH5CC.VAL value of register without affecting channel state or configuration.

Table 15-34. CH5CCSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

15.4.33 CH5CFG Register (Offset = 164h) [Reset = 00000000h]

CH5CFG is shown in Table 15-35.

Return to the Summary Table.

Systimer channel 5 configuration. ;This channel has configurability for 250ns and 1us based capture and compare operations.

Table 15-35. CH5CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RES	R/W	0h	This bit decides the RESOLUTION of the channel that will be used. 0h = channel Works in Timer's 1us Resolution. 1h = channel Works in Timer's 250ns resolution
3	REARM	R/W	0h	When Rearm is enabled the channel remains in continous capture mode. Otherwise it'll be in one shot capture mode. Rearm is only valid for capture mode. 0h = Re Arm is disabled 1h = Re arm is enabled
2-1	INP	R/W	0h	Decides the channel input signal's mode. Setting the Value as 2'b11 selects the Rise Function. 0h = Capture on rising edge 1h = Capture on Falling Edge 2h = Capture on both Edge
0	MODE	R/W	0h	Decides the channel mode. 0h = channel is disabled 1h = channel is in capture mode

15.4.34 CH5CC Register (Offset = 168h) [Reset = 00000000h]

CH5CC is shown in Table 15-36.

Return to the Summary Table.

System Timer channel 5 Capture/Compare register. ;This register when written with any compare value will arm the channel to work in compare mode. Reads to this register will clear the Corresponding RIS.EV5 bit.

Table 15-36. CH5CC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Capture/compare value

Chapter 16

Real Time Clock (RTC)

This chapter describes the functionality of the Real Time Clock (RTC) module.

16.1 Introduction

The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock. The RTC is active in STANDBY and ACTIVE power states. When the device enters the RESET or SHUTDOWN state the RTC is reset.

Upon asynchronous device resets (e.g. reset pin, exit from shutdown, LF clock loss,etc.), the RTC is reset. However, upon internally generated synchronous device resets (e.g. WDT, debug reset,system reset request, etc.), the RTC is not reset.

The RTC accumulates time elapsed since reset on each LFCLK. The RTC counter is incremented by LFINC at a rate of 32.768 kHz. LFINC indicates the period of LFCLK in µs, with an additional granularity of 16 fractional bits.

The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multi-channel and higher resolution SYSTIM remain in synchronization with the RTC's time base.

The RTC has two channels: one compare channel and one capture channel and is capable of waking the device out of the standby power state. The RTC compare channel is typically used only by system software and only during the standby power state.

16.2 Block Diagram

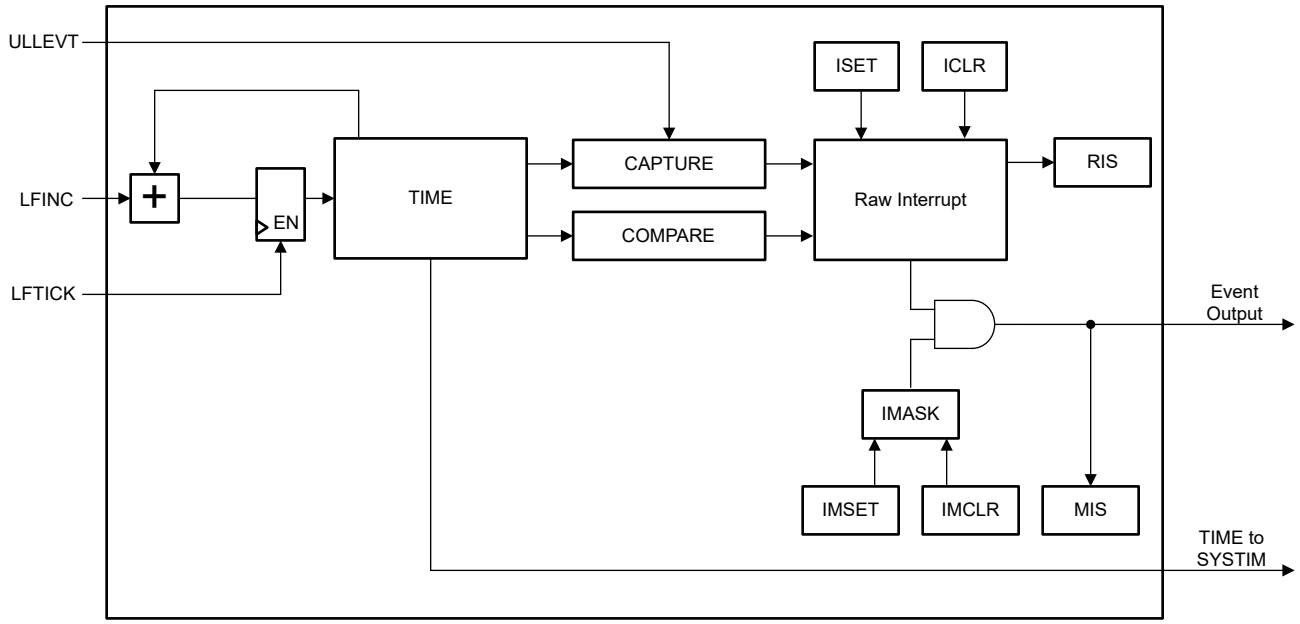


Figure 16-1. RTC Block Diagram

16.3 Interrupts and Events

16.3.1 Input Event

RTC has one capture input event from the AON/ULL event fabric. The capture event is selected by writing EVTULL.RTCCPTSEL[5:0] PUBID bit field. The capture can be on a rising or falling edge. This is configured by writing or clearing the RTC.CH1CFG[0] EDGE bit.

- RTC.CH1CFG[0] EDGE = 0 is rising edge configuration. This is the reset value for this bit.
- RTC.CH1CFG[0] EDGE = 1 is falling edge configuration.

16.3.2 Output Event

The RTC has one combined interrupt request event output. See Section 4.4 for more information on interrupt and event handling.

Interrupt flags for the combined interrupt can be read from the RTC.MIS register. Interrupts can be cleared by writing to the RTC.ICLR register. Interrupt status for the capture channel is cleared by reading the RTC.CH1CC8U[20:0] VAL bit field. Interrupt status for the compare channel is cleared by writing to the RTC.CH0CC8U[31:0] VAL bit field.

16.3.3 Arming and Disarming Channels

RTC.ARMSET and RTC.ARMCLR are provided as additional methods of arming and disarming channels. A read of either the RTC.ARMCLR or RTC.ARMSET register returns the armed status of each channel. If the capture or compare channel is armed, setting the corresponding bit in the RTC.ARMCLR register to 1 sets the channel in the unarmed state without triggering an event (unless a compare or capture event happens in the same cycle).

If the channel is not armed, writing the RTC.ARMSET[1] CH1 bit arms the capture channel. Writing to RTC.ARMSET[0] CH0 has no effect on the compare channel. The compare channel is automatically armed when a value is written to the RTC.CH0COMP register.

16.4 CAPTURE and COMPARE Configurations

RTC has two channels.

16.4.1 CHANNEL 0 - COMPARE CHANNEL

The compare channel has the option to get armed through three different resolutions of time - 250ns, 1µs, and 8µs.

The compare channel

- Is armed in 250ns resolution when a compare value is written to the RTC.CH0CC250N register.
- Is armed in 1us resolution when a compare value is written to the RTC.CH0CC1U register.
- Is armed in 8µs resolution when a compare value is written to the RTC.CH0CC8U register.

The compare channel is disarmed when a compare event occurs.

Note

Although the CH0CC250N/CH0CC1U registers are arming the channel in compare mode, the comparison still occurs w.r.t the TIME8U register, Hence the events are generated every 32KHz based on the TIME8U register.

- RTC generates an immediate event if the compare value is between now and 1 second in the past.
- Otherwise, RTC generates a compare event when the difference between the compare value and RTC value is within 32µs.

16.4.2 CHANNEL 1 - CAPTURE CHANNEL

The capture event is selected by writing EVTULL.RTCCPTSEL[5:0] PUBID bit field. Event capture can occur on either the rising or falling edge of the event by setting or clearing the RTC.CH1CFG[0] EDGE bit. Capture is armed by setting the RTC.ARMSET[1] CH1 bit. Once capture is armed the RTC.CH1CC8U[20:0] bit field is updated with the value from the RTC.TIME8U[31:0] VAL bit field at the time the capture event occurs.

16.5 RTC Registers

Table 16-1 lists the memory-mapped registers for the RTC registers. All register offset addresses not listed in Table 16-1 should be considered as reserved locations and the register contents should not be modified.

Table 16-1. RTC Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 16.5.1
4h	CTL	RTC control Register	Section 16.5.2
8h	ARMSET	Channel Arming Set	Section 16.5.3
Ch	ARMCLR	Channel Arming Clear	Section 16.5.4
10h	TIME250N	RTC Lower Time Slice	Section 16.5.5
14h	TIME1U	RTC Lower Time Slice	Section 16.5.6
18h	TIME8U	RTC Lower Time Slice	Section 16.5.7
1Ch	TIME524M	RTC Upper Time Slice	Section 16.5.8
20h	CH0CC250N	Channel0 compare value	Section 16.5.9
24h	CH0CC1U	Channel0 compare value	Section 16.5.10
28h	CH0CC8U	Channel0 compare value	Section 16.5.11
38h	CH1CC8U	Channel1 capture Value	Section 16.5.12
3Ch	CH1CFG	Channel 1 Input Configuration	Section 16.5.13
44h	IMASK	Interrupt mask	Section 16.5.14
48h	RIS	Raw interrupt status	Section 16.5.15
4Ch	MIS	Masked interrupt status	Section 16.5.16
50h	ISET	Interrupt set	Section 16.5.17
54h	ICLR	Interrupt clear	Section 16.5.18
58h	IMSET	Interrupt mask set	Section 16.5.19
5Ch	IMCLR	Interrupt clear	Section 16.5.20
60h	EMU	Emulation	Section 16.5.21
68h	DTIME	Delta Time	Section 16.5.22

Complex bit access types are encoded to fit into small table cells. Table 16-2 shows the codes that are used for access types in this section.

Table 16-2. RTC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

16.5.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 16-3.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 16-3. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6442h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

16.5.2 CTL Register (Offset = 4h) [Reset = 00000000h]

CTL is shown in Table 16-4.

Return to the Summary Table.

RTC Control register. This register controls resetting the of RTC counter

Table 16-4. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RST	W	0h	RTC counter reset. Writing 1 to this bit will reset the RTC counter, and cause it to resume counting from 0x0 0h = No effect 1h = Reset the timer.

16.5.3 ARMSET Register (Offset = 8h) [Reset = 00000000h]

ARMSET is shown in Table 16-5.

Return to the Summary Table.

RTC channel mode set register. Read to each bit field of this register provides the current channel mode. ;- Read of 1'b0 indicates the channel is unarmed.;- Read of 1'b1 indicates the channel is either in capture or compare mode.;A write to each bitfield of this register the following effect:;- Write of 1'b0 has no effect on channel mode.;- Write of 1'b1 has no effect on the compare channel. While write of 1'b1 for capture channel will arm it in capture mode if it is disabled.

Table 16-5. ARMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CH1	R/W	0h	Arming Channel 1 for capture operation. 0h = No effect on the channel 1h = Enable the Channel 1 for capture operation
0	CH0	R/W	0h	No effect on arming the channel. Read will give the status of the Channel 0. 0h = No effect on the channel 1h = No effect on the compare channel

16.5.4 ARMCLR Register (Offset = Ch) [Reset = 00000000h]

ARMCLR is shown in Table 16-6.

Return to the Summary Table.

RTC channel mode clear register. Read to each bit field of this register provides the current channel mode. ;- Read of 1'b0 indicates the channel is unarmed.;- Read of 1'b1 indicates the channel is either in capture or compare mode.;A write to each bitfield of this register the following effect:;- Write of 1'b0 has no effect on channel mode.;- Write of 1'b1 for capture/compare channel will disarm it without triggering event unless a compare/capture event happens in the same cycle.

Table 16-6. ARMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CH1	R/W	0h	Disarming Channel 1 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a capture event happens in the same cycle
0	CH0	R/W	0h	Disarming Channel 0 0h = No effect on the channel 1h = Set channel in UNARMED state without triggering event unless a compare event happens in the same cycle

16.5.5 TIME250N Register (Offset = 10h) [Reset = 00000000h]

TIME250N is shown in Table 16-7.

Return to the Summary Table.

RTC Time value register. 32-bit unsigned integer representing [29:-2] time slice of the real time clock counter. The counter runs on LFCLK. This field has a resolution of 250ns, and range of about 17.8 minutes.

Table 16-7. TIME250N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	[29:-2] slice of RTC TIME[50:-2]. Slice has an LSB weight of 250 ns and modular range 17m 53.74182002 s. RTC.TIME is updated every LF clock modulo by a fixed or measured LFINC value and will thus on average update only every ~30.5 us.; ;SYSTIM.TIME is synchronized to RTC TIME[31:-2] and is updated every 250 ns if better resolution is needed (in addition to having a much shorter access time of 1-2 cycles instead of 22-26 cycles for RTC.TIMEx).

16.5.6 TIME1U Register (Offset = 14h) [Reset = 00000000h]

TIME1U is shown in Table 16-8.

Return to the Summary Table.

RTC Time value register. 32-bit unsigned integer representing [31:0] time slice of the real time clock counter. The counter runs on LFCLK. This field has a resolution of 1us, and range of about 1.19 hours.

Table 16-8. TIME1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	[31:0] slice of RTC TIME[50:-2]. Slice has an LSB weight of 1 us and modular range 1h 11m 34.967296s. RTC.TIME is updated every LF clock modulo by a fixed or measured LFINC value and will thus on average update only every ~30.5 us.; ;SYSTIM.TIME is synchronized to RTC TIME[31:-2] and is updated every 250 ns if better resolution is needed (in addition to having a much shorter access time of 1-2 cycles instead of 22-26 cycles for RTC.TIMEx).

16.5.7 TIME8U Register (Offset = 18h) [Reset = 00000000h]

TIME8U is shown in Table 16-9.

Return to the Summary Table.

RTC Time value register. 32-bit unsigned integer representing [34:3] time slice of the real time clock counter. The counter runs on LFCLK. This field has a resolution of 8us, and range of about 9.5 hours.

Table 16-9. TIME8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	[34:3] slice of RTC TIME[50:-2]. Slice has an LSB weight of 8 us and modular range 9h 32m 39.73836s. RTC.TIME is updated every LF clock modulo by a fixed or measured LFINC value and will thus on average update only every ~30.5 us.; ;SYSTIM.TIME is synchronized to RTC TIME[31:-2] and is updated every 250 ns if better resolution is needed (in addition to having a much shorter access time of 1-2 cycles instead of 22-26 cycles for RTC.TIMEx).

16.5.8 TIME524M Register (Offset = 1Ch) [Reset = 00000000h]

TIME524M is shown in Table 16-10.

Return to the Summary Table.

RTC time value register. 32-bit unsigned integer representing [50:19] time slice of the real time clock counter. This field has a resolution of about 0.5s and a range of about 71.4 years.

Table 16-10. TIME524M Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	[50:19] slice of RTC TIME[50:-2]. Slice has an LSB weight of 0.524288s and modular range of approximately 71 years 147 days 11h 56m 53s. RTC.TIME is updated every LF clock modulo by a fixed or measured LFINC value and will thus on average update only every ~30.5 us.; ;SYSTIM.TIME is synchronized to RTC TIME[31:-2] and is updated every 250 ns if better resolution is needed (in addition to having a much shorter access time of 1-2 cycles instead of 22-26 cycles for RTC.TIMEx).

16.5.9 CH0CC250N Register (Offset = 20h) [Reset = 00000000h]

CH0CC250N is shown in Table 16-11.

Return to the Summary Table.

Channel 0 compare value with 250ns resolution. A read to this register returns the value {CH0CC8U[29:3], 5b'0};A write to this register arms the channel in compare mode. Event would occur at the same time +/ Tlfclk/2 on the RTC as if it was written to SYSTIM.

Table 16-11. CH0CC250N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	RTC Channel 0 compare value. This value is compared against TIME8U.VAL. A Channel 0 event is generated when TIME8U.VAL value reaches or exceeds this compare value.

16.5.10 CH0CC1U Register (Offset = 24h) [Reset = 00000000h]

CH0CC1U is shown in Table 16-12.

Return to the Summary Table.

Channel 0 compare value with 1us resolution. A read to this register returns the value {CH0CC8U[31:3], 3b'0};A write to this register arms the channel in compare mode. Event would occur at the same time +/ Tlfclk/2 on the RTC as if it was written to SYSTIM.

Table 16-12. CH0CC1U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	RTC Channel 0 compare value. This value is compared against TIME8U.VAL. A Channel 0 event is generated when TIME8U.VAL value reaches or exceeds this compare value.

16.5.11 CH0CC8U Register (Offset = 28h) [Reset = 00000000h]

CH0CC8U is shown in Table 16-13.

Return to the Summary Table.

Channel 0 compare value. A write to this register automatically enables the channel to trigger an event when RTC timer reaches the programmed value or if the programmed value is 1 sec in the past.

Table 16-13. CH0CC8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	RTC Channel 0 compare value. This value is compared against TIME8U.VAL. A Channel 0 event is generated when TIME8U.VAL value reaches or exceeds this compare value.

16.5.12 CH1CC8U Register (Offset = 38h) [Reset = 00000000h]

CH1CC8U is shown in Table 16-14.

Return to the Summary Table.

Channel 1 capture value. This register captures the RTC time slice [34:3] on each selected edge of the capture event when the ARMSET.CH1 = 1.

Table 16-14. CH1CC8U Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	VAL	R	Xh	TIME8U.VAL captured value at the last selected edge of capture event.

16.5.13 CH1CFG Register (Offset = 3Ch) [Reset = 00000000h]

CH1CFG is shown in Table 16-15.

Return to the Summary Table.

Channel 1 configuration register. This register can be used to select the capture edge for generating the capture event.

Table 16-15. CH1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EDGE	R/W	0h	Edge detect configuration for capture source 0h = Rising Edge. 1h = Falling Edge.

16.5.14 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 16-16.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 16-16. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	R/W	0h	Channel 1 Event Interrupt Mask. 0h = Clear Interrupt Mask 1h = Enable Interrrupt Mask
0	EV0	R/W	0h	Channel 0 Event Interrupt Mask. 0h = Disable Interrupt Mask 1h = Enable Interrrupt Mask

16.5.15 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 16-17.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 16-17. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	R	0h	Raw interrupt status for Channel 1 event.;This bit is set to 1 when a capture event is received on Channel 1. ;This bit will be cleared when the bit in ICLR.EV1 is set to 1 or when the captured time value is read from the CH1CC8U register. 0h = Interrupt did not occur 1h = Interrupt occured
0	EV0	R	0h	Raw interrupt status for Channel 0 event.;This bit is set to 1 when a compare event occurs on Channel 0. ;This bit will be cleared. When the corresponding bit in ICLR.EV0 is set to 1. Or when a new compare value is written in CH0CC8U register 0h = Interrupt did not occur 1h = Interrupt occured

16.5.16 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 16-18.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 16-18. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	R	0h	Masked interrupt status for channel 1 event. 0h = Interrupt did not occur 1h = Interrupt occured
0	EV0	R	0h	Masked interrupt status for channel 0 event. 0h = Interrupt did not occur 1h = Interrupt occured

16.5.17 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 16-19.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 16-19. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Set Channel 1 event Interrupt. 0h = Writing 0 has no effect 1h = Set interrupt
0	EV0	W	0h	Set Channel 0 event Interrupt. 0h = Writing 0 has no effect 1h = Set interrupt

16.5.18 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 16-20.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 16-20. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Clears channel 1 event interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	EV0	W	0h	Clears channel 0 event interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt.

16.5.19 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 16-21.

Return to the Summary Table.

Interrupt mask set register. Writing a 1 to a bit in this register will set the corresponding IMASK bit.

Table 16-21. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Set channel 1 event interrupt mask. 0h = Writing 0 has no effect 1h = Set interrupt mask
0	EV0	W	0h	Set channel 0 event interrupt mask. 0h = Writing 0 has no effect 1h = Set interrupt mask

16.5.20 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 16-22.

Return to the Summary Table.

Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding IMASK bit.

Table 16-22. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EV1	W	0h	Clears Channel 1 event interrupt mask. 0h = Writing 0 has no effect 1h = Clear Interrupt Mask
0	EV0	W	0h	Clears Channel 0 event interrupt mask. 0h = Writing 0 has no effect 1h = Clear Interrupt Mask

16.5.21 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 16-23.

Return to the Summary Table.

Emulation control register. This register controls the behavior of the IP related to core halted input.

Table 16-23. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HALT	R/W	0h	Halt control. 0h = Free run option. The IP ignores the state of the core halted input. 1h = Freeze option. The IP freezes functionality when the core halted input is asserted, and resumes when it is deasserted. The freeze can either be immediate or after the IP has reached a boundary from where it can resume without corruption.

16.5.22 DTIME Register (Offset = 68h) [Reset = 00000000h]

DTIME is shown in Table 16-24.

Return to the Summary Table.

A delta time mechanism is implemented for RTC that allows the TIME value to be adjusted under software control. This is used by boot code to perform the compensation for reset duration (accomplished by adding MMR write to FCFG.generalTrims copylist to avoid ROM changes);TIME[50:-2] is adjusted by TIME += sxt(MANT[30:0], 53) * 2^{22*EXP}. ;In other words:;(EXP==0): TIME is adjusted by MANT * 250 ns (range +/-134 s);(EXP==1): TIME is adjusted by MANT * 1.049 s (range +/- 35.7 yr);If used by an application to adjust RTC TIME value, the write to DTIME must occur as quickly as possible after an lftick event. It should also be followed by a write of 1 to SYSTIM.STATUS.SYNCUP to ensure that SYSTIM resynchronizes to the new RTC TIME value at the next lftick event.

Table 16-24. DTIME Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXP	W	0h	Exponent
30-0	MANT	W	0h	Mantissa

Chapter 17

Low Power Comparator (SYS0)

This chapter discusses the features and functions of the CC27xx low power comparator configured with the resgisters located in SYS0.

17.1 Introduction

LPCOMP is a ultra low-power clocked comparator that can be used for medium accuracy, low speed operations where power consumption is the main concern. Typical applications are wake-up on analog events like power supply monitoring or external transducers that generate analog output signals. The comparator includes input multiplexers on both signal (positive) side and reference (negative) side, a capacitive divider for low-power division of either the reference signal or the input signal, and programmable hysteresis that can be configured to trigger on both low and high comparator output.

Features

- Can be used for voltage monitoring in standby mode with ultra-low power consumption
- Operational across device supply voltage range
- Programmable Voltage Divider with two modes of operation:
  - Voltage Divider on Reference Side: The voltage divider block is configured on the reference side of the amplifier and the inputs can be divided in the ratio of 1/4, 1/3, 1/2, 3/4, and 1/1 with optional hysteresis applied.
  - Voltage Divider on Signal Side: The voltage divider block is configured on the signal side of the amplifier and the inputs can be divided in the ratio of 1/4, 1/3, 1/2, 3/4, and 1/1 with optional hysteresis applied.
- Input multiplexers - The input multiplexers present on the reference and signal side of amplifier provide greater flexibility on selecting the signal and reference inputs to the amplifier based on system requirements. The multiplexers can pass inputs from external pins or from supply voltages. The multiplexer on the reference side is connected to both VDDS and VDDD which can be used as internal references. The multiplexer on the signal side is directly connected to VDDS which can be used for monitoring the supply voltage.
- Hysteresis Polarity - The polarity of the hysteresis can be changed based on whether the voltage divider is present on signal side or reference side. This is controlled by the SYS0:LPCMPCFG[30] HYSPOL bit.

17.2 Block Diagram

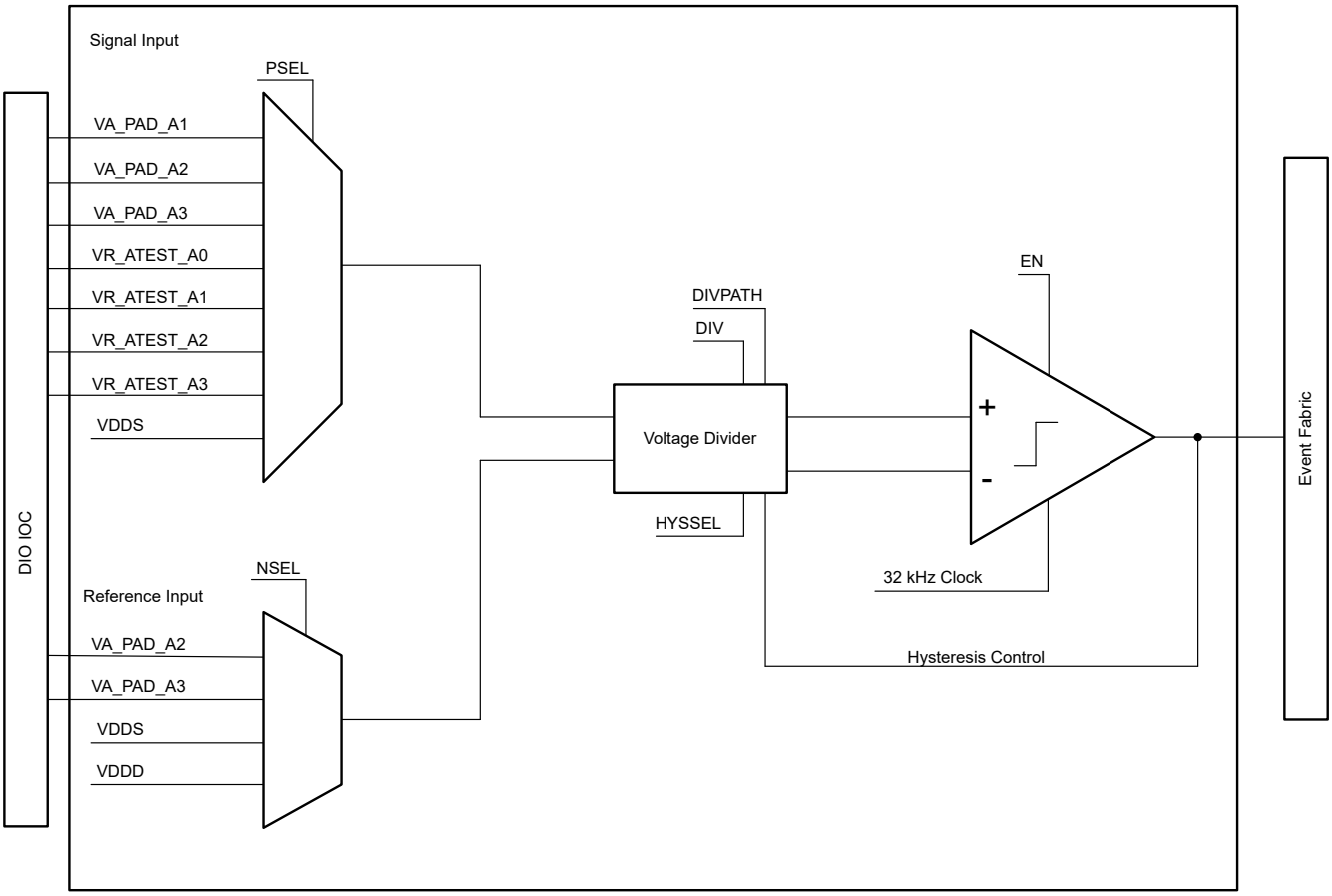


Figure 17-1. LPCOMP Block Diagram

17.3 Functional Description

LPCOMP consists of two input multiplexors which select between various inputs as shown in Figure 17-1. These inputs are routed to a programmable voltage divider. From there the inputs are routed to the comparator. The comparator has a latching output that latches on the 32 kHz clock. The comparator result has a 1-3 clock cycle delay. The entire comparator module can be enabled or disabled by setting or clearing the SYS0.LPCMPCFG[0] EN bit. LFOSC must be enabled before LPCOMP is enabled.

17.3.1 Input Selection

Signal Input

The AUX_LP_COMP signal input can connect to:

- VA_PAD_A1
- VA_PAD_A2
- VA_PAD_A3
- VR_ATEST_A0
- VR_ATEST_A1
- VA_ATEST_A0
- VA_ATEST_A1
- VDDS

The selection is made by configuring SYS0.LPCMPCFG[11:8] PSEL bit field.

Reference Input

The AUX_LP_COMP reference input can connect to:

- VA_PAD_A2
- VA_PAD_A3
- VDDS
- VDDD

The selection is made by configuring SYS0.LPCMPCFG NSEL[14:12] bit field.

The mapping between AUX_LP_COMP input and DIO for CC27xx is shown in Table 17-1.

Table 17-1. AUX_LP_COMP Input to DIO Mapping

Pin name	Analog function	ATB	HH port	Comments
DIO19_A6	ADC6/LPC+		VA_PAD_A0	Selectable As LPCOMP +ve input inside AUX
DIO20_A5	ADC5/LPC+/LPC-		VA_PAD_A1	Selectable As LPCOMP +ve or -ve input inside AUX
DIO21_A4	ADC4/LPC+/LPC-	ATEST0	VA_PAD_A2	Selectable As LPCOMP +ve or -ve input inside AUX, also connects to ATEST0
DIO22_A3	ADC3	ATEST1	VA_PAD_A3	Connects to ATEST1

17.3.2 Voltage Divider

The voltage divider is applied to either the signal input or the reference input of the comparator. The voltage divider is capable of dividing the input voltage in the ratio of 1/4, 1/3 1/2, 3/4, and 1/1 with the addition of voltage to the input signal to control hysteresis on the output. Connect the divider on the reference side. The minimum equivalent input resistance of the divider is 30 M-Ohm.

17.3.3 Hysteresis

The purpose of hysteresis is to prevent rapid changes on the comparator output due to noise on the input. This is done by increasing the voltage difference of the signal input compared to the reference input. Because of this, hysteresis will affect the accuracy of the measurement and should be disabled before the measurement. This means that the hysteresis should be enabled by the comparator output going low, if the input signal is above the threshold before the measurement is done (e.g. supply monitoring where the signal is slowly dropping to the reference level). If the signal is rising towards the reference level, hysteresis should be enabled by the comparator output going high. This is accommodated by a control-bit where the user can select if the hysteresis should be enabled by a high or low comparator output signal.

The table below shows the possible permutations and the resulting necessary configuration of the hysteresis polarity and trigger level.

Table 17-2. Hysteresis Configuration

User Case		Hysteresis polarity	Hysteresis trig-level
Divider on reference input	Signal starting high and going low	Positive (1)	Low (0)
Divider on reference input	Signal starting low and going high	Negative (0)	High (1)
Divider on signal input	Signal starting high and going low	Negative (0)	Low (0)
Divider on signal input	Signal starting low and going high	Positive (1)	High (1)

17.3.4 Wake-up

The LPCOMP can be configured to wake the CC27XX from standby mode. This is enabled by setting the SYS0.LPCMPCFG[18] WUENSB bit.

17.4 SYS0 Registers

Table 17-3 lists the memory-mapped registers for the SYS0 registers. All register offset addresses not listed in Table 17-3 should be considered as reserved locations and the register contents should not be modified.

Table 17-3. SYS0 Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register	Section 17.4.1
Ch	MUNLOCK	Mutable section Unlock	Section 17.4.2
100h	ATESTCFG	ATEST Configuration	Section 17.4.3
108h	TSENSCFG	TSENSE Configuration	Section 17.4.4
10Ch	LPCMPCFG	LPCMP configuration	Section 17.4.5
110h	VGMCFG	This register is used to configure the VGM module.	Section 17.4.6
114h	VGMTRIMDBG	This register is used to trim and debug VGM module.	Section 17.4.7
3FCh	DEVICEID	Device ID	Section 17.4.8
410h	DBGAUTH	Debug Authentication.	Section 17.4.9
7F8h	PARTID	Part ID	Section 17.4.10
800h	TMUTE0	Internal. Only to be used through TI provided API.	Section 17.4.11
804h	TMUTE1	Internal. Only to be used through TI provided API.	Section 17.4.12
808h	TMUTE2	TMUTE2 trim Register	Section 17.4.13
80Ch	TMUTE3	Internal. Only to be used through TI provided API.	Section 17.4.14
810h	TMUTE4	TMUTE4 trim Register	Section 17.4.15
814h	TMUTE5	Internal. Only to be used through TI provided API.	Section 17.4.16

Complex bit access types are encoded to fit into small table cells. Table 17-4 shows the codes that are used for access types in this section.

Table 17-4. SYS0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WCap	W Cap	Write Capture
Reset or Default Value		
-n		Value after reset or the default value

17.4.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 17-5.

Return to the Summary Table.

Description Register ;This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 17-5. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6B4Eh	Module Identifier is used to uniquely identify this IP
15-12	STDIPOFF	R	0h	Standard IP MMR block offset. Standard IP MMRs are the set from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

17.4.2 MUNLOCK Register (Offset = Ch) [Reset = 00000000h]

MUNLOCK is shown in Table 17-6.

Return to the Summary Table.

Mutable section Unlock;This register unlocks registers in mutable section

Table 17-6. MUNLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	WCap	0h	Write the unlock key 0xC5AF6927 to temporarily unlock registers in mutable section. The lock is set automatically if no write accesses, to the mutable section, are detected for consecutive 32 CLKULL (24MHz) clock cycles. Writing any value other than that, the unlock key will immediately lock the mutable register space for write access. 0h = Lock registers in the mutable section C5AF6927h = Unlock registers in the mutable section

17.4.3 ATESTCFG Register (Offset = 100h) [Reset = 00000000h]

ATESTCFG is shown in Table 17-7.

Return to the Summary Table.

ATEST Configuration;This register is used to configure analog switches in ATEST module.

Table 17-7. ATESTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Key must be written with value 0x5A for successful write to ATESTCFG and to unlock register state. ;Write with any value other than 0x5A to KEY will be ignored and register content is not updated.;It is recommended to write this register with incorrect KEY to lock back register state after necessary ATESTCFG updates are done. ;Read value of KEY is 0x0.
23-9	RESERVED	R	0h	Reserved
8	VSEL	R/W	0h	Selects supply for ATEST switches. 0h = Selects VDDBOOST 1h = Selects VDDS
7	VA2VA1	R/W	0h	Enables isolation switch between VA_ATEST_A1 and VA_PAD_A1. 0h = Switch is open 1h = Switch is closed
6	VA2VA0	R/W	0h	Enables isolation switch between VA_ATEST_A0 and VA_PAD_A0. 0h = Switch is open 1h = Switch is closed
5	VR2VA1	R/W	0h	Enables isolation switch between VR_ATEST_A1 and VA_ATEST_A1. 0h = Switch is open 1h = Switch is closed
4	VR2VA0	R/W	0h	Enables isolation switch between VR_ATEST_A0 and VA_ATEST_A0. 0h = Switch is open 1h = Switch is closed
3	SHTVA1	R/W	1h	Shorts VA_ATEST_A1 to ground. 0h = Switch is open 1h = Switch is closed
2	SHTVA0	R/W	1h	Shorts VA_ATEST_A0 to ground. 0h = Switch is open 1h = Switch is closed
1	SHTVR1	R/W	1h	Shorts VR_ATEST_A1 to ground. 0h = Switch is open 1h = Switch is closed
0	SHTVR0	R/W	1h	Shorts VR_ATEST_A0 to ground. 0h = Switch is open 1h = Switch is closed

17.4.4 TSENSCFG Register (Offset = 108h) [Reset = 00000000h]

TSENSCFG is shown in Table 17-8.

Return to the Summary Table.

TSENSE Configuration;This register is used to configure temperature sensor module.

Table 17-8. TSENSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-12	RESERVED	R	0h	Software should not rely on the value of a reserved field. Writing any other value than the reset value may result in undefined behavior
11	TSENS2EN	R/W	0h	This is the enable bit for the second temperature sensor in AUX. 0h = Second temperature sensor is disabled. 1h = Second temperature sensor is enabled.
10-2	RESERVED	R	0h	Reserved
1-0	SEL	R/W	0h	Used to enable and configure temperature sensor module. Setting the value to 0x3 will disable the temperature sensor. 0h = Temperature sensor is disabled 1h = 20uA current is injected on VR_ATEST_A0 and voltage measured on VR_ATEST_A1 2h = 20uA current is injected on VR_ATEST_A0 and ground measured on VR_ATEST_A1

17.4.5 LPCMPCFG Register (Offset = 10Ch) [Reset = 00000000h]

LPCMPCFG is shown in Table 17-9.

Return to the Summary Table.

LPCMP configuration;This register is used to configure and check the status of low-power comparator (LPCOMP) module.

Table 17-9. LPCMPCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Software should not rely on the value of a reserved field. Writing any other value than the reset value may result in undefined behavior
30	HYSPOL	R/W	0h	Hysteresis polarity 0h = Not inverted 1h = Inverted
29-28	ATESTMUX	R/W	0h	Used to configure ATEST mux in comparator module and provides chosen output on VA_ATEST_A0.;Note: This bit field is write-protected using global lock indicator on production device. 0h = ATEST mux is off 1h = Selects comparator output 2h = Selects voltage divider output 3h = Selects bias current output
27-25	RESERVED	R	0h	Reserved
24	EVTIFG	R/W	0h	Event flag;The event flag is set when the comparator output transition is qualified based on the edge polarity configuration in EDGCFG. 0h = Clear 1h = Set
23-22	RESERVED	R	0h	Reserved
21	COUTEN	R/W	0h	Enables LPCOMP output on device pin. 0h = Disabled 1h = Enabled
20	COUT	R	0h	LPCOMP output status. This bit captures the value LPCOMP raw output. 0h = Output is low 1h = Output is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Enables lpcmpcfg output to wake device from standby. 0h = Disable 1h = Enable
17	EVTEN	R/W	0h	Enables event generation. Comparator module will produce event on ULL event fabric when EVTIFG is set. 0h = Disable 1h = Enable
16	EDGCFG	R/W	0h	Selects positive edge or negative edge detection on comparator output to set the event flag 0h = Rise edge detection 1h = Fall edge detection
15	RESERVED	R	0h	Reserved
14-12	NSEL	R/W	0h	Negative input selection. Setting values 0x5-0x7 will open all the switches. 0h = All switches are open 1h = Selects VA_PAD_A2 2h = Selects VA_PAD_A3 3h = Selects VDDS 4h = Selects VDDD

Table 17-9. LPCMPCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	PSEL	R/W	0h	Positive input selection. Setting values 0x9-0xF will open all the switches. 0h = All switches are open 1h = Selects VA_PAD_A1 2h = Selects VA_PAD_A2 3h = Selects VA_PAD_A3 4h = Selects VR_ATEST_A0 5h = Selects VR_ATEST_A1 6h = Selects VA_ATEST_A0 7h = Selects VA_ATEST_A1 8h = Selects VDDS
7-5	HYSSEL	R/W	0h	Used to enable and select hysteresis level;Hysteresis is disabled when HYSSEL = 0 and enabled for other values of HYSSEL from 1 to 7. Refer to device specific datasheet for individual hysteresis values. 0h = Hysteresis is disabled 1h = Hysteresis value 1 2h = Hysteresis value 2 3h = Hysteresis value 3 4h = Hysteresis value 4 5h = Hysteresis value 5 6h = Hysteresis value 6 7h = Hysteresis value 7
4	DIVPATH	R/W	0h	Used to select the path on which voltage divider is applied 0h = Divider is applied on N-side 1h = Divider is applied on P-side
3-1	DIV	R/W	0h	Used to configure reference divider. Setting values 0x5-0x7 will set the divide value to 1. 0h = Divide value is 1 1h = Divide value is 3/4 2h = Divide value is 1/2 3h = Divide value is 1/3 4h = Divide value is 1/4
0	EN	R/W	0h	Used to enable comparator module. 0h = Disable 1h = Enable

17.4.6 VGMCFG Register (Offset = 110h) [Reset = 00000000h]

VGMCFG is shown in Table 17-10.

Return to the Summary Table.

This register is used to configure the VGM module.

Table 17-10. VGMCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Key must be written with value 0x5A for successful write to VGMCFG and to unlock register state. ;Write with any value other than 0x5A to KEY will be ignored and the register content is not updated.;Read value of KEY is 0x0.
23-12	RESERVED	R	0h	Reserved
11-8	ATBMUXSEL	R/W	0h	These bits are used to generate VGM ATB mux selection control.
7-2	RESERVED	R	0h	Reserved
1	OSHDETDIS	R/W	1h	Disables overshoot detector in VGM. 0h = Enable 1h = Disable
0	USHTDETDIS	R/W	1h	Disables undershoot detector in VGM. 0h = Enable 1h = Disable

17.4.7 VGMTRIMDBG Register (Offset = 114h) [Reset = 00000000h]

VGMTRIMDBG is shown in Table 17-11.

Return to the Summary Table.

This register is used to trim and debug VGM module.

Table 17-11. VGMTRIMDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	RESERVED
30	TMODE5	R/W	0h	Test mode bit for glitchy supply mux selection.
29-27	TMODE4	R/W	0h	Test mode bits for VREF mux selection for overshoot detector.
26-24	TMODE3	R/W	0h	Test mode bits for VREF mux selection for undershoot detector.
23-22	RESERVED	R	0h	Reserved
21-20	TMODE2	R/W	0h	Test mode for level shifter isolation.
19-18	TMODE1	R/W	0h	Test mode bits for low voltage SR latch reset.
17-16	TMODE0	R/W	0h	Test mode bits for 3V SR latch reset.
15-12	RESERVED	R	0h	Reserved
11-8	IBPROG	R/W	0h	These bits are used to program VGM bias current generator.
7-4	OSHDETTRIM	R/W	0h	These bits are used to trim VGM overshoot detector.
3-0	USHTDETTRIM	R/W	0h	These bits are used to trim VGM undershoot detector.

17.4.8 DEVICEID Register (Offset = 3FCh) [Reset = 00000000h]

DEVICEID is shown in Table 17-12.

Return to the Summary Table.

Device ID;This register provides Device ID information.;Note: This 32-bit register value is provided as output to DEBUGSS.

Table 17-12. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	VERSION	R	0h	Monotonic increasing value indicating new hardware revision. A newer hardware revision shall never have a lower version than an older revision of hardware.
27-12	DEVICE	R	BB98h	Value generated by RAMP for the SOC. This value uniquely identifies the die from any other TI device.
11-1	MANFACTURER	R	17h	JEP 106 assigned manufacturer ID. This field identifies the device as a Texas Instruments device.
0	ALWAYSONE	R	1h	Value 1 in this bit field means that a 32-bit scan register exists.

17.4.9 DBGAUTH Register (Offset = 410h) [Reset = 00000000h]

DBGAUTH is shown in Table 17-13.

Return to the Summary Table.

Debug Authentication. ;This register is used by ROM to store Debug Authnetication Status

Table 17-13. DBGAUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	CLR	W	0h	Clears Authentication Status
15-2	RESERVED	R	0h	Reserved
1-0	SET	W	0h	Sets Authentication Status 0h = Debug Unauthorized 1h = Only Non-Invasive Debug Authorized 2h = Non-Secure Debug Authorized 3h = Secure Debug Authorized

17.4.10 PARTID Register (Offset = 7F8h) [Reset = 00000000h]

PARTID is shown in Table 17-14.

Return to the Summary Table.

Part ID;This register is programmed by boot code with Part ID information. Note: This 32-bit register value is provided as output to DEBUGSS

Table 17-14. PARTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31	START	R/W	0h	Start bit 0h = Clear 1h = Set
30-28	MAJORREV	R/W	0h	Monotonic increasing value indicating a new revision of the SKU significant enough that users of the device may have to revise PCB or software design
27-24	MINORREV	R/W	0h	Monotonic increasing value indicating a new revision of the SKU that preserves compatibility with lesser MINORREV values
23-16	VARIANT	R/W	0h	Bit pattern uniquely identifying a variant of a part
15-0	PART	R/W	0h	Bit pattern uniquely identifying a part

17.4.11 TMUTE0 Register (Offset = 800h) [Reset = 00000000h]

TMUTE0 is shown in Table 17-15.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 17-15. TMUTE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CDACL	R/W	0h	Internal. Only to be used through TI provided API.

17.4.12 TMUTE1 Register (Offset = 804h) [Reset = 00000000h]

TMUTE1 is shown in Table 17-16.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 17-16. TMUTE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CDACM	R/W	0h	Internal. Only to be used through TI provided API.

17.4.13 TMUTE2 Register (Offset = 808h) [Reset = 00000000h]

TMUTE2 is shown in Table 17-17.

Return to the Summary Table.

TMUTE2 trim Register

Table 17-17. TMUTE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	RESERVED
30-26	IBTRIM	R/W	0h	LPCOMP: Bias current trim, 250nA to be terminated across I2V, 1M Ω setting. Resulting target trim voltage 250mV.
25-23	TRIM	R/W	1h	ADC REFBUF trim bits.
22-16	LATCH	R/W	0h	SOC ADC: Latch trim bits. These bits are used in the analog IP.
15-4	OFFSET	R/W	0h	SOCADC: Offset trim bits. These bits are used in DTC.
3-2	RES	R/W	0h	SOCADC: Resistor trim bits. These bits are used in the analog IP.
1-0	CDACU	R/W	0h	SOCADC: Upper 2 bits of CDAC trim. These bits are used in DTC.

17.4.14 TMUTE3 Register (Offset = 80Ch) [Reset = 00000000h]

TMUTE3 is shown in Table 17-18.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 17-18. TMUTE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	BATC1	R/W	0h	Internal. Only to be used through TI provided API.
25-19	BATC0	R/W	0h	Internal. Only to be used through TI provided API.
18-14	TEMPC2	R/W	0h	Internal. Only to be used through TI provided API.
13-8	TEMPC1	R/W	0h	Internal. Only to be used through TI provided API.
7-0	TEMPC0	R/W	0h	Internal. Only to be used through TI provided API.

17.4.15 TMUTE4 Register (Offset = 810h) [Reset = 00000000h]

TMUTE4 is shown in Table 17-19.

Return to the Summary Table.

TMUTE4 trim Register

Table 17-19. TMUTE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RECHCOMPREFLVL	R/W	Bh	Internal. Only to be used through TI provided API.
27-26	IOSTRCFG2	R/W	0h	Internal. Only to be used through TI provided API.
25-22	IOSTRCFG1	R/W	0h	Internal. Only to be used through TI provided API.
21-19	MAX	R/W	5h	Internal. Only to be used through TI provided API.
18-16	MED	R/W	6h	Internal. Only to be used through TI provided API.
15-13	MIN	R/W	3h	Internal. Only to be used through TI provided API.
12-11	DCDCLOAD	R/W	0h	Internal. Only to be used through TI provided API.
10-8	IPEAK	R/W	0h	DCDC: Set inductor peak current;Min = 0x0;Max = 0x7;DCDC load support increases from 0x0 to 0x7
7-6	DTIME	R/W	0h	Internal. Only to be used through TI provided API.
5-3	LENSEL	R/W	7h	Internal. Only to be used through TI provided API.
2-0	HENSEL	R/W	7h	Internal. Only to be used through TI provided API.

17.4.16 TMUTE5 Register (Offset = 814h) [Reset = 00000000h]

TMUTE5 is shown in Table 17-20.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 17-20. TMUTE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Internal. Only to be used through TI provided API.
12-10	DCDCDRVDS	R/W	0h	Internal. Only to be used through TI provided API.
9-5	GLDOISCLR	W	0h	Internal. Only to be used through TI provided API.
4-0	GLDOISSET	W	0h	Internal. Only to be used through TI provided API.
4-0	RESERVED	R	0h	Reserved

Chapter 18

Battery Monitor, Temperature Sensor and DCDC Controller (PMUD)

This chapter describes the function of the Power Management Unit - Digital (PMUD).

18.1 Introduction

PMUD is composed of two components, BATMON (battery monitoring unit) and DCDC control logic.

BATMON monitors both the VDDS supply voltage and the temperature through an on-chip temperature sensor, outputs the voltage dependent control signals to the I/O pads, gives a coarse temperature measure and provides a software interface for accessing battery state and temperature measurements. When enabled, the battery and temperature monitor module is operational in all operation modes except the lowest power mode, SHUTDOWN. When the device is in STANDBY, the measurements of the battery monitor module are limited to recharge cycles. At least two measurements are performed in each recharge cycle.

The battery monitor provides voltage and temperature information to several modules. This is done to enable correct operation and lowest power consumption. Therefore, the recommendation is to not modify any settings in the battery monitor or turn the battery monitor off.

DCDC outputs the control signals for DCDC switches, measures battery voltage, and also takes care of turning off GLDO when not required.

18.2 Functional Description

18.2.1 BATMON

The battery monitor is a 7-bit SAR-like ADC running at 125 kHz that performs alternate measurements of the supply voltage and the temperature. When the battery monitor has settled on the first measurement, the ADC stops working in SAR mode and starts linear tracking of voltage and temperature. A small digital core transforms these measurements to voltage and temperature in °C, which are read directly from the PMUD:BAT and PMUD:TEMP registers.

When a change in supply voltage or temperature is detected, the battery monitor solely tracks the voltage until the voltage has settled on a new constant level. The resolution of the ADC and the 125 kHz clock speed limits the battery monitor's capability of measuring voltage spikes. Due to the battery monitor not only alternating between temperature and battery voltage, but also between checking if there has been a positive or negative change since last read, there can be a delay of 6 clock cycles between a voltage dip and the time when the ADC can detect that the temperature or voltage has changed. Due to the prioritization of voltage tracking upon detection of voltage changes, temperature changes can be detected with more delays if the voltage is also changing at the same time. This is important to keep in mind because the battery monitor is designed to measure the battery voltage; the battery monitor is not designed to measure voltage spurs due to short periods of higher current consumption.

The module also includes an event register, PMUD.EVENT, that includes six event bits:

- PMUD.EVENT[5] TEMP_UPDATE bit: indicates that the temperature has changed
- PMUD.EVENT[4] BATT_UPDATE bit: indicates that the voltage has changed
- PMUD.EVENT[3] TEMP_BELOW_LL bit: indicates that the temperature is below the lower limit value that is set in the PMUD.TEMPLL register
- PMUD.EVENT[2] TEMP_OVER_UL bit: indicates that the temperature is over the upper limit value that is set in the PMUD.TEMPUL register
- PMUD.EVENT[1] BATT_BELOW_LL bit: indicates that the voltage is below the lower limit value that is set in the PMUD:BATTLL register
- PMUD.EVENT[0] BATT_OVER_UL bit: indicates that the voltage is over the upper limit value that is set in the PMUD.BATTUL register

These events must be cleared by writing to the PMUD:EVENT register. The events are asserted again if the conditions for the events are met (assertion of the new events takes precedence over the clearing of the events). In addition to the individual events listed previously, the battery monitor module has a combined event that is connected to the CPU as an interrupt line. The mask register, PMUD.EVENTMASK, can be used to select which of the events in PMUD.EVENT contribute to the combined event. This combined event is connected to the AON event fabric. For details, see Section 4.4.

18.2.2 DCDC

DCDC buck converter is a switch mode power supply which generates regulated output voltage from higher unregulated supply. Compared to linear regulators, DCDC has a higher power efficiency which reduces total energy consumption of the device.

DCDC is connected in parallel with a linear regulator (GLDO).

DCDC generally supports a lower maximum load current than that of the peak load current of the GLDO. In applications where higher load current needs are to be met, GLDO is enabled automatically preventing VDDR output going low. The best possible power efficiency is achieved across load variations with the parallel operation of DCDC and GLDO.

The input supply of DCDC can range from 2.2V to 3.8V. DCDC regulates the output to 1.5V. But for GLDO, the supply can range from 1.71V to 3.8V to generate a regulated output of 1.5V. DCDC hardware is designed so that when the supply voltage drops below 2.2V, DCDC automatically shuts off and only GLDO generates the regulated VDDR.

GLDO can operate independently, but DCDC needs GLDO to support driving a higher load above the DCDC limit.

DCDC hardware implements these features to provide smooth and parallel operation of DCDC and GLDO:

- Load meter.
- GLDO enable toggle logic.
- Adaptive peak current control.

Load meter:

Load meter is used to measure load on DCDC output as a percentage of maximum load support by DCDC. The load meter can be enabled using PMUD.DCDCCFG.LM_EN[0], and its output is available in the status register PMUD.DCDCSTAT.LOAD[6:0]. The register value ranges from 0 to 100, representing the percentage of the DCDC output load. If the load exceeds the DCDC limit, the register will always display a value of 100. After the load meter feature is enabled, it takes approximately 500µs to generate the first output, and for any subsequent load change it can take approximately 250 us to update the register to the accurate load level.

GLDO enable toggle logic:

GLDO enable toggle logic is used for parallel operation of DCDC and GLDO. As load increases on VDDR above DCDC load support, GLDO is enabled by analog circuit almost instantly. This feature is used to prevent undesirable and repeated enable and disable toggles of GLDO when load on VDDR is close to maximum DCDC load support, which can result in a higher VDDR ripple.

This feature also enables the load meter. Once GLDO is enabled due to higher VDDR load, load meter output is continuously compared with an internally programmed DCDC load threshold. Once the load on DCDC is less than the threshold, GLDO is safely disabled. The hardware also provides a minimum enable window for GLDO to reduce the ripples on VDDR.

Adaptive peak current control:

DCDC has programmable peak current to vary the maximum load support. To support higher load, DCDC can be programmed to higher peak current setting, but then DCDC operates on a reduced power efficiency. With lower peak current DCDC works with higher efficiency but with lower maximum load support. So, for given load on VDDR, there is an optimum peak current setting for DCDC which provides the best power efficiency. If DCDC is not able to meet the load requirement, then GLDO would be turned on to supply additional load current, which reduces the overall efficiency. Therefore, the minimum peak current configuration which would also enable DCDC to meet the load requirement would be the most optimum configuration which will provide the best power efficiency. Adaptive peak current control is an algorithm which updates peak current dynamically until the optimum value is reached.

For the operation of adaptive peak current control, load meter output is continuously monitored against two programmable DCDC load thresholds (high threshold and low threshold). If the load on DCDC is more than the high threshold, the algorithm increments peak current value programmed. If the load on DCDC drops below the low threshold, the programmed peak current value is decremented. For a given load on VDDR, after few increments and decrements the final peak current value reaches the optimum setting for the best power efficiency. Each increment or decrement operation can have a delay up to 250µs, and to reach optimum peak current setting, adaptive peak current control algorithm can take up to 1 ms.

It is recommended to use the provided drivers in the SDK for ease of use. Registers used for adaptive peak current control:

1. DCDCCFG.ADP_IPEAK_EN: Enables adaptive peak current control hardware algorithm.
2. DCDCCFG.LM_HIGHTH: DCDC load meter high threshold value. DCDC load meter output is in a percentage scale so the valid values are ‘d1 to ‘d100. Values from ‘d101 to ‘d127 are invalid and are not to be used. The recommended value is ‘d80.
3. DCDCCFG.LM_LOWTH: DCDC load meter low threshold value. The recommended value is ‘d50.
4. SYS0.TMUTE4.IPEAK: This field can be used to program the maximum current that has to be supported by DCDC from ‘d0 (approximately 14 mA) to ‘d7 (approximately 45 mA). When the adaptive algorithm is enabled, then this value acts as the limit up to which the algorithm can increment the DCDC peak current.
5. DCDCSTAT.IPEAK: DCDC peak current value programmed within SYS0.TMUTE4.IPEAK register when this algorithm is not enabled. When this is enabled, this register outputs the peak current value being driven by the algorithm.

18.3 PMUD Registers

Table 18-1 lists the memory-mapped registers for the PMUD registers. All register offset addresses not listed in Table 18-1 should be considered as reserved locations and the register contents should not be modified.

Table 18-1. PMUD Registers

Offset	Acronym	Register Name	Section
0h	CTL	Control	Section 18.3.1
4h	MEASCFG	Internal. Only to be used through TI provided API.	Section 18.3.2
28h	BAT	Last Measured Battery Voltage	Section 18.3.3
2Ch	BATUPD	Battery Update	Section 18.3.4
30h	TEMP	Last measured Temperature in Degree Celsius	Section 18.3.5
34h	TEMPUPD	Temperature Update	Section 18.3.6
48h	EVENTMASK	Event Mask	Section 18.3.7
4Ch	EVENT	Event	Section 18.3.8
50h	BATTUL	Battery Upper Limit	Section 18.3.9
54h	BATTLL	Battery Lower Limit	Section 18.3.10
58h	TEMPUL	Temperature Upper Limit	Section 18.3.11
5Ch	TEMPLL	Temperature Lower Limit	Section 18.3.12
80h	PREFSYS	Internal. Only to be used through TI provided API.	Section 18.3.13
90h	PREG0	Internal. Only to be used through TI provided API.	Section 18.3.14
94h	PREG1	Internal. Only to be used through TI provided API.	Section 18.3.15
98h	PREG2	Internal. Only to be used through TI provided API.	Section 18.3.16
9Ch	DCDCCFG	DCDC configuration	Section 18.3.17
A0h	DCDCSTAT	DCDC status	Section 18.3.18

Complex bit access types are encoded to fit into small table cells. Table 18-2 shows the codes that are used for access types in this section.

Table 18-2. PMUD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

18.3.1 CTL Register (Offset = 0h) [Reset = 00000000h]

CTL is shown in Table 18-3.

Return to the Summary Table.

Control;General Configuration of BATMON

Table 18-3. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	HYST_EN	R/W	1h	Enables hysteresis on both battery and temperature measurements. 0h = Disable 1h = Enable
1	CALC_EN	R/W	0h	Configuration of the calculation block that converts the digital battery/temperature level to a Volt/Celsius value. 0h = Calculation disabled 1h = Calculation enabled
0	MEAS_EN	R/W	0h	Configuration of the measurement block that interfaces with the analog domain. 0h = Measurements disabled 1h = Measurements enabled (battery voltage and temperature)

18.3.2 MEASCFG Register (Offset = 4h) [Reset = 00000000h]

MEASCFG is shown in Table 18-4.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 18-4. MEASCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	PER	R/W	0h	Internal. Only to be used through TI provided API.

18.3.3 BAT Register (Offset = 28h) [Reset = 00000000h]

BAT is shown in Table 18-5.

Return to the Summary Table.

Last Measured Battery Voltage;This register should be read when BATUPD.STA = 1

Table 18-5. BAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	INT	R	0h	Integer part:;0x0: Battery voltage = 0V + fractional part;...;0x3: Battery voltage = 3V + fractional part;0x4: Battery voltage = 4V + fractional part
7-0	FRAC	R	0h	Fractional part, standard binary fractional encoding.;0x00: .0V;...;0x20: 1/8 = .125V;0x40: 1/4 = .25V;0x80: 1/2 = .5V;...;0xA0: 1/2 + 1/8 = .625V;...;0xFF: 1/2 + 1/4 + 1/8 + ... + 1/256 = 0.99V

18.3.4 BATUPD Register (Offset = 2Ch) [Reset = 00000000h]

BATUPD is shown in Table 18-6.

Return to the Summary Table.

Battery Update;Indicates BAT Updates

Table 18-6. BATUPD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STA	R/W	0h	Battery update status. Write 1 to clear the status. 0h = No update since last clear 1h = New battery voltage present

18.3.5 TEMP Register (Offset = 30h) [Reset = 00000000h]

TEMP is shown in Table 18-7.

Return to the Summary Table.

Last measured Temperature in Degree Celsius;This register should be read when TEMPUPD.STA = 1.

Table 18-7. TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16-8	INT	R	0h	Integer part of temperature value (signed) ;Total value = INT + FRAC;2's complement encoding;0x100: Min value (-256°C);0x1D8: -40°C;0x1FF: -1°C;0x00: 0°C;0x1B: 27°C;0x55: 85°C;0xFF: Max value (255°C)
7-6	FRAC	R	0h	Fractional part of temperature value.;Total value = INT + FRAC;The encoding is an extension of the 2's complement encoding.;00: 0.0°C;01: 0.25°C;10: 0.5°C;11: 0.75°C;For example:;000000001,00 = (1+0,00) = 1,00;000000000,11 = (0+0,75) = 0,75;000000000,10 = (0+0,50) = 0,50;000000000,01 = (0+0,25) = 0,25;000000000,00 = (0+0,00) = 0,00;111111111,11 = (-1+0,75) = -0,25;111111111,10 = (-1+0,50) = -0,50;111111111,01 = (-1+0,25) = -0,75;111111111,00 = (-1+0,00) = -1,00;111111110,11 = (-2+0,75) = -1,25
5-0	RESERVED	R	0h	Reserved

18.3.6 TEMPUPD Register (Offset = 34h) [Reset = 00000000h]

TEMPUPD is shown in Table 18-8.

Return to the Summary Table.

Temperature Update;Indicates TEMP Updates

Table 18-8. TEMPUPD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STA	R/W	0h	Temperature update status. Write 1 to clear the status. 0h = No temperature update since last clear 1h = New temperature value present

18.3.7 EVENTMASK Register (Offset = 48h) [Reset = 00000000h]

EVENTMASK is shown in Table 18-9.

Return to the Summary Table.

Event Mask

Table 18-9. EVENTMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	TEMP_UPDATE_MASK	R/W	0h	1: EVENT.TEMP_UPDATE contributes to combined event from BATMON;0: EVENT.TEMP_UPDATE does not contribute to combined event from BATMON
4	BATT_UPDATE_MASK	R/W	0h	1: EVENT.BATT_UPDATE contributes to combined event from BATMON;0: EVENT.BATT_UPDATE does not contribute to combined event from BATMON
3	TEMP_BELOW_LL_MASK	R/W	0h	1: EVENT.TEMP_BELOW_LL contributes to combined event from BATMON;0: EVENT.TEMP_BELOW_LL does not contribute to combined event from BATMON
2	TEMP_OVER_UL_MASK	R/W	0h	1: EVENT.TEMP_OVER_UL contributes to combined event from BATMON;0: EVENT.TEMP_OVER_UL does not contribute to combined event from BATMON
1	BATT_BELOW_LL_MASK	R/W	0h	1: EVENT.BATT_BELOW_LL contributes to combined event from BATMON;0: EVENT.BATT_BELOW_LL does not contribute to combined event from BATMON
0	BATT_OVER_UL_MASK	R/W	0h	1: EVENT.BATT_OVER_UL contributes to combined event from BATMON;0: EVENT.BATT_OVER_UL does not contribute to combined event from BATMON

18.3.8 EVENT Register (Offset = 4Ch) [Reset = 00000000h]

EVENT is shown in Table 18-10.

Return to the Summary Table.

Event

Table 18-10. EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	TEMP_UPDATE	R/W	0h	Alias to TEMPUPD.STA
4	BATT_UPDATE	R/W	0h	Alias to BATUPD.STA
3	TEMP_BELOW_LL	R/W	0h	Read:;1: Temperature level is below the lower limit set by TEMPLL.;0: Temperature level is not below the lower limit set by TEMPLL.;Write:;1: Clears the flag;0: No change in the flag
2	TEMP_OVER_UL	R/W	0h	Read:;1: Temperature level is above the upper limit set by TEMPUL.;0: Temperature level is not above the upper limit set by TEMPUL.;Write:;1: Clears the flag;0: No change in the flag
1	BATT_BELOW_LL	R/W	0h	Read:;1: Battery level is below the lower limit set by BATTLL.;0: Battery level is not below the lower limit set by BATTLL.;Write:;1: Clears the flag;0: No change in the flag
0	BATT_OVER_UL	R/W	0h	Read:;1: Battery level is above the upper limit set by BATTUL.;0: Battery level is not above the upper limit set by BATTUL.;Write:;1: Clears the flag;0: No change in the flag

18.3.9 BATTUL Register (Offset = 50h) [Reset = 00000000h]

BATTUL is shown in Table 18-11.

Return to the Summary Table.

Battery Upper Limit;Total battery voltage = INT + FRAC;It is a sum of integer and fractional parts

Table 18-11. BATTUL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	INT	R/W	7h	Integer part:;Total battery voltage = INT + FRAC (integer and fractional part);0x0: Battery voltage = 0V + fractional part;...;0x3: Battery voltage = 3V + fractional part;0x4: Battery voltage = 4V + fractional part
7-0	FRAC	R/W	FFh	Fractional part, standard binary fractional encoding.;0x00: .0V;...;0x20: 1/8 = .125V;0x40: 1/4 = .25V;0x80: 1/2 = .5V;...;0xA0: 1/2 + 1/8 = .625V;...;0xFF: 1/2 + 1/4 + 1/8 + ... + 1/256 = 0.99V

18.3.10 BATTLL Register (Offset = 54h) [Reset = 00000000h]

BATTLL is shown in Table 18-12.

Return to the Summary Table.

Battery Lower Limit;Total battery voltage = INT + FRAC;It is a sum of integer and fractional parts

Table 18-12. BATTLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	INT	R/W	0h	Integer part:;Total battery voltage = INT + FRAC (integer and fractional part);0x0: Battery voltage = 0V + fractional part;...;0x3: Battery voltage = 3V + fractional part;0x4: Battery voltage = 4V + fractional part
7-0	FRAC	R/W	0h	Fractional part, standard binary fractional encoding.;0x00: .0V;...;0x20: 1/8 = .125V;0x40: 1/4 = .25V;0x80: 1/2 = .5V;...;0xA0: 1/2 + 1/8 = .625V;...;0xFF: 1/2 + 1/4 + 1/8 + ... + 1/256 = 0.99V

18.3.11 TEMPUL Register (Offset = 58h) [Reset = 00000000h]

TEMPUL is shown in Table 18-13.

Return to the Summary Table.

Temperature Upper Limit

Table 18-13. TEMPUL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16-8	INT	R/W	FFh	Integer part (signed) of temperature upper limit. ;Total value = INT + FRAC;2's complement encoding;0x100: Min value (-256°C);0x1D8: -40°C;0x1FF: -1°C;0x00: 0°C;0x1B: 27°C;0x55: 85°C;0xFF: Max value (255°C)
7-6	FRAC	R/W	3h	Fractional part of temperature upper limit.;Total value = INT + FRAC;The encoding is an extension of the 2's complement encoding.;00: 0.0°C;01: 0.25°C;10: 0.5°C;11: 0.75°C;For example:;000000001,00 = (1+0,00) = 1,00;000000000,11 = (0+0,75) = 0,75;000000000,10 = (0+0,50) = 0,50;000000000,01 = (0+0,25) = 0,25;000000000,00 = (0+0,00) = 0,00;111111111,11 = (-1+0,75) = -0,25;111111111,10 = (-1+0,50) = -0,50;111111111,01 = (-1+0,25) = -0,75;111111111,00 = (-1+0,00) = -1,00;111111110,11 = (-2+0,75) = -1,25
5-0	RESERVED	R	0h	Reserved

18.3.12 TEMPLL Register (Offset = 5Ch) [Reset = 00000000h]

TEMPLL is shown in Table 18-14.

Return to the Summary Table.

Temperature Lower Limit

Table 18-14. TEMPLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16-8	INT	R/W	100h	Integer part (signed) of temperature lower limit. ;Total value = INT + FRAC;2's complement encoding;0x100: Min value (-256°C);0x1D8: -40°C;0x1FF: -1°C;0x00: 0°C;0x1B: 27°C;0x55: 85°C;0xFF: Max value (255°C)
7-6	FRAC	R/W	0h	Fractional part of temperature lower limit.;Total value = INT + FRAC;The encoding is an extension of the 2's complement encoding.;00: 0.0°C;01: 0.25°C;10: 0.5°C;11: 0.75°C;For example:;000000001,00 = (1+0,00) = 1,00;000000000,11 = (0+0,75) = 0,75;000000000,10 = (0+0,50) = 0,50;000000000,01 = (0+0,25) = 0,25;000000000,00 = (0+0,00) = 0,00;111111111,11 = (-1+0,75) = -0,25;111111111,10 = (-1+0,50) = -0,50;111111111,01 = (-1+0,25) = -0,75;111111111,00 = (-1+0,00) = -1,00;111111110,11 = (-2+0,75) = -1,25
5-0	RESERVED	R	0h	Reserved

18.3.13 PREFSYS Register (Offset = 80h) [Reset = 00000000h]

PREFSYS is shown in Table 18-15.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 18-15. PREFSYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-11	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
10	TEST10	R/W	0h	Internal. Only to be used through TI provided API.
9	TEST9	R/W	0h	Internal. Only to be used through TI provided API.
8	TEST8	R/W	0h	Internal. Only to be used through TI provided API.
7	TEST7	R/W	0h	Internal. Only to be used through TI provided API.
6	TEST6	R/W	0h	Internal. Only to be used through TI provided API.
5	TEST5	R/W	0h	Internal. Only to be used through TI provided API.
4	TEST4	R/W	0h	Internal. Only to be used through TI provided API.
3	TEST3	R/W	0h	Internal. Only to be used through TI provided API.
2	TEST2	R/W	0h	Internal. Only to be used through TI provided API.
1	TEST1	R/W	0h	Internal. Only to be used through TI provided API.
0	TEST0	R/W	0h	Internal. Only to be used through TI provided API.

18.3.14 PREG0 Register (Offset = 90h) [Reset = 00000000h]

PREG0 is shown in Table 18-16.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 18-16. PREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	LOW_IPEAK_DIS	R/W	0h	Internal. Only to be used through TI provided API.
10	SOCLDO_ITESTEN	R/W	0h	Internal. Only to be used through TI provided API.
9-7	SOCLDO_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.
6-5	UDIGLDO_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.
4-2	DIGLDO_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.
1	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
0	UDIGLDO_EN	R/W	0h	Internal. Only to be used through TI provided API.

18.3.15 PREG1 Register (Offset = 94h) [Reset = 00000000h]

PREG1 is shown in Table 18-17.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 18-17. PREG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	TEST_DCDC_NMOS	R/W	0h	Internal. Only to be used through TI provided API.
18	TEST_DCDC_PMOS	R/W	0h	Internal. Only to be used through TI provided API.
17	DITHER_EN	R/W	0h	Internal. Only to be used through TI provided API.
16	GLDO_AON	R/W	0h	Internal. Only to be used through TI provided API.
15	RCHG_BLK_VTRIG_EN	R/W	0h	Internal. Only to be used through TI provided API.
14	RCHG_BLK_ATEST_EN	R/W	0h	Internal. Only to be used through TI provided API.
13	RCHG_FORCE_SAMP_VREF	R/W	0h	Internal. Only to be used through TI provided API.
12	RCHG_COMP_CLK_DIS	R/W	0h	Internal. Only to be used through TI provided API.
11-8	RESERVED	R	0h	Reserved
7	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
6	VDDR_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.
5	GLDO_EA_BIAS_DIS	R/W	0h	Internal. Only to be used through TI provided API.
4-1	GLDO_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.
0	RESERVED	R	0h	Reserved

18.3.16 PREG2 Register (Offset = 98h) [Reset = 00000000h]

PREG2 is shown in Table 18-18.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 18-18. PREG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	RSTNMASK	R/W	0h	Internal. Only to be used through TI provided API.
4	DCDC_RCHG_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.
3-0	PMUREG_ATBSEL	R/W	0h	Internal. Only to be used through TI provided API.

18.3.17 DCDCCFG Register (Offset = 9Ch) [Reset = 00000000h]

DCDCCFG is shown in Table 18-19.

Return to the Summary Table.

DCDC configuration register

Table 18-19. DCDCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	LM_HIGHTH	R/W	0h	DCDC load meter high threshold value for adaptive IPEAK adjustment. DCDC load meter output is in percentage scale so the applicable values are 'd1 to 'd100. Values from 'd101 to 'd127 are invalid and not to be used.
15	RESERVED	R	0h	Reserved
14-8	LM_LOWTH	R/W	0h	DCDC load meter low threshold value for adaptive IPEAK adjustment. DCDC load meter output is in percentage scale so the applicable values are 'd1 to 'd100. Values from 'd101 to 'd127 are invalid and not to be used.
7-5	RESERVED	R	0h	Reserved
4	ADP_IPEAK_EN	R/W	0h	This bit is used to enable adaptive IPEAK adjustment scheme in hardware. When this bit is set, DCDC IPEAK value is automatically adjusted to suitable value by sensing the DCDC load meter output for better DCDC operational efficiency. 0h = Disable 1h = Enable
3-1	RESERVED	R	0h	Reserved
0	LMEN	R/W	0h	This bit is used to enable DCDC load meter. Software can obtain DCDC load meter value from DCDCSTAT regiser and adjust IPEAK setting in SYS0.TDCDC register accordingly. 0h = Disable 1h = Enable

18.3.18 DCDCSTAT Register (Offset = A0h) [Reset = 00000000h]

DCDCSTAT is shown in Table 18-20.

Return to the Summary Table.

DCDC status register

Table 18-20. DCDCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	IPEAK	R	0h	DCDC IPEAK value. This value is same as what is programmed in SYS0:TMUTE4.IPEAK when adaptive IPEAK adjustment scheme is not enabled, and it shows current IPEAK value applied by hardware when adaptive IPEAK adjustment scheme is enabled.;Note: Software can only support IPEAK = 1
7	RESERVED	R	0h	Reserved
6-0	LOAD	R	0h	This indicates DCDC load meter output value in percentage scale. ;Applicable range is 'd1 to 'd100.

Chapter 19

Micro Direct Memory Access (µDMA)

This chapter describes the direct memory access (DMA) controller, known as µDMA.

19.1 Introduction

The CC27XX includes a direct memory access (DMA) controller, known as µDMA. The µDMA controller provides a way to offload data transfer tasks from the Arm® Cortex®-M33 Armprocessor, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfers between memory and peripherals. The controller has dedicated channels for each supported on-chip module, and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. The µDMA controller provides the following features:

- Arm®PrimeCell® 12-channel configurable µDMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes:
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of arbitrary transfers initiated from a single request
- Highly flexible and configurable channel operation:
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - Primary and secondary channel assignments
  - Flexible channel assignments
  - One channel each for receive and transmit paths for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable priority scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, halfword, word, or no increment
- Maskable peripheral requests
- Interrupt on transfer completion with a separate interrupt per channel

19.2 Block Diagram

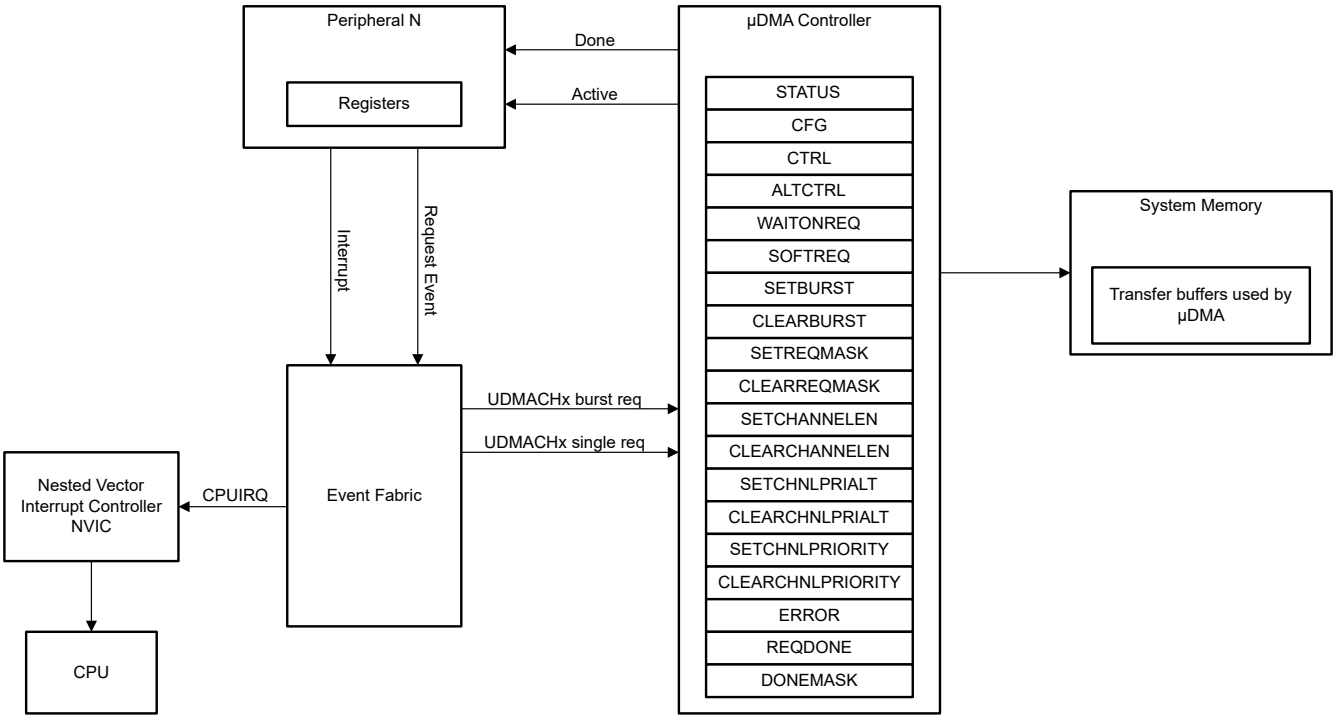


Figure 19-1. µDMA Block Diagram

19.3 Functional Description

The µDMA controller is a flexible and highly configurable DMA controller designed to work efficiently with the Arm® Cortex® -M33 processor core of the microcontroller. The controller supports multiple data sizes and address increment schemes, multiple levels of priority among DMA channels, and several transfer modes to allow for sophisticated programmed data transfers.

Each supported peripheral function has a dedicated channel on the µDMA controller that can be configured independently. The µDMA controller implements a configuration method using channel control structures maintained in system memory by the processor. While simple transfer modes are supported, it is also possible to build up sophisticated task lists in memory that allow the µDMA controller to perform arbitrary-sized transfers to and from arbitrary locations as part of a single transfer request. The µDMA controller also supports the use of ping-pong buffering to accommodate constant streaming of data to or from a peripheral.

Each channel also has a configurable arbitration size. The arbitration size is the number of items that are transferred in a burst before the µDMA controller requests channel priority. Using the arbitration size, it is possible to control exactly how many items are transferred to or from a peripheral every time a µDMA service request is made.

19.3.1 Channel Assignments

Table 19-1 lists µDMA channel assignments to peripherals.

Table 19-1. Channel Assignments

µDMA Channel	Type [1] [2]	DTB [3]	Triggers
0	DCH	YES	SPI0TXTRG, UART1RXTRG
1	DCH	YES	SPI0RXTRG, UART1TXTRG
2	DCH	YES	LRFDTRG, UART0TXTRG
3	DCH	YES	ADC0TRG, UART0RXTRG
4	DCH	YES	LAESTRGA, LRFDTRG
5	DCH	YES	LAESTRGB, ADC0TRG
6	DCH	YES	CANTRGA,SPI1TXTRG
7	DCH	YES	CANTRGB,SPI1RXTRG
8	ECH	YES	ANY
9	ECH	YES	ANY
10	ECH	YES	ANY
11	ECH	YES	ANY

(1) Dedicated µDMA Channel (DCH) type can only be connected to peripherals with dedicated µDMA interface
(2) Event Publisher Channel (ECH) type can only be connected to publishers,

See also Section 4.4.5.1
(3) For DTB output, only SREQ and REQ is considered.

19.3.2 Priority

The µDMA controller assigns priority to each channel based on the channel number and the priority-level bit for the channel. Channel 0 has the highest priority, and as the channel number increases, the priority of a channel decreases. Each channel has a priority-level bit to provide two levels of priority: default priority and high priority. If the priority-level bit is set, then that channel has a higher priority than all other channels at default priority. If multiple channels are set for high priority, then the channel number is used to determine relative priority among all the high-priority channels.

The priority bit for a channel can be set using the DMA.SETCHNLPRIORITY register and cleared with the DMA.CLEARCHNLPRIORITY register.

19.3.3 Arbitration Size

When a µDMA channel requests a transfer, the µDMA controller arbitrates among all the channels making a request, and services the µDMA channel with the highest priority. Once a transfer begins, it continues for a selectable number of transfers before re-arbitrating among the requesting channels. The arbitration size can be configured for each channel, ranging from 1 to 1024 item transfers. After the µDMA controller transfers the number of items specified by the arbitration size, the controller then checks among all the channels making a request, and services the channel with the highest priority.

If a lower-priority µDMA channel uses a large arbitration size, the latency for higher-priority channels is increased because the µDMA controller completes the lower-priority burst before checking for higher-priority requests. Therefore, lower-priority channels must not use a large arbitration size for best response on high-priority channels.

The arbitration size can also be thought of as burst size. Arbitration size is the maximum number of items that are transferred at any one time in a burst. Here, the term *arbitration* refers to the determination of the µDMA channel priority, not arbitration for the bus. When the µDMA controller arbitrates for the bus, the processor always takes priority. Furthermore, the µDMA controller is delayed whenever the processor must perform a bus transaction on the same bus, even in the middle of a burst transfer.

19.3.4 Request Types

The µDMA controller responds to two types of requests from a peripheral: single request or burst request. Each peripheral can support either or both types of requests. A single request means that the peripheral is ready to transfer one item, while a burst request means that the peripheral is ready to transfer multiple items.

The µDMA controller responds differently depending on whether the peripheral is making a single request or a burst request. If both types of requests are asserted and the µDMA channel has been set up for a burst transfer, then the burst request takes precedence. Table 19-2 lists how each peripheral supports the two request types.

Table 19-2. Request Type Support

Peripheral	Single Request Signal	Burst Request Signal
ADC	None (FIFO is not empty)	Sequencer IE bit (FIFO is half full)
General-purpose timer	Raw interrupt pulse	None
GPIO	Raw interrupt pulse	None
SPI TX	TXFIFO not full	TXFIFO level (configurable)
SPI RX	RXFIFO not empty	RXFIFO level (configurable)
UART TX	TXFIFO not full	TXFIFO level (configurable)
UART RX	RXFIFO not empty	RXFIFO level (configurable)

19.3.4.1 Single Request

When a single request is detected (not a burst request), the µDMA controller transfers one item and then stops to wait for another request.

19.3.4.2 Burst Request

When a burst request is detected, the µDMA controller transfers the number of items that is the lesser of the arbitration size or the number of items remaining in the transfer. Therefore, the arbitration size must be the same as the number of data items that the peripheral can accommodate when making a burst request. For example, the UART and SPI, which use a mix of single or burst requests, could generate a burst request based on the FIFO trigger level. In this case, the arbitration size must be set to the amount of data that the FIFO can transfer when the trigger level is reached. A burst transfer runs to completion once it starts and cannot be interrupted, even by a higher-priority channel. Burst transfers complete in a shorter time than the same number of non-burst transfers.

It may be desirable to use only burst transfers and not allow single transfers (for example, when the nature of the data is such that it only makes sense when transferred together as a single unit rather than one piece at a

time). The single request can be disabled in the DMA.SETBURST register. By setting the bit for a channel in this register, the µDMA controller responds only to burst requests for that channel.

19.3.5 Channel Configuration

The µDMA controller uses an area of system memory to store a set of channel control structures in a table. The control table can have one or two entries for each µDMA channel. Each entry in the table structure contains source and destination pointers, transfer size, and transfer mode. The control table can be located anywhere in system memory, but the control table must be contiguous and aligned on a 256-byte boundary.

Table 19-3 describes the memory layout of the channel control table. Each channel can have one or two control structures in the control table—a primary control structure and an optional, alternate control structure. The table is organized with all of the primary entries in the first half of the table, and with all the alternate structures in the second half of the table. The primary entry is used for simple transfer modes where transfers can be reconfigured and restarted after each transfer completes. In this case, the alternate control structures are not used and only the first half of the table must be allocated in memory. The rest of the memory can be used for something else. If a more complex transfer mode is used, such as ping-pong or scatter-gather, then the alternate control structure is also used and memory space must be allocated for the entire table.

Any unused memory in the control table can be used by the application, which includes the control structures for any channels that are unused by the application, as well as the unused control word for each channel.

Table 19-3. Control Structure Memory Map

Offset	Channel
0x0	0, Primary
0x10	1, Primary
...	...
0x70	7, Primary
0x80	0, Alternate
0x90	1, Alternate
...	...
0xF00	7, Alternate

Table 19-4 describes an individual control-structure entry in the control table. Each entry is aligned on a 16-byte boundary. The entry contains four 4-byte long words: the source end pointer, the destination end pointer, the control word, and an unused entry. The inclusive end pointers point to the ending address of the transfer. If the source or destination is non-incrementing (as for a peripheral register), then the pointer must point to the transfer address.

Table 19-4. Channel Control Structure

Offset	Description
0x000	Source end pointer
0x004	Destination end pointer
0x008	Control word
0x00C	Unused entry

The control word contains the following fields:

- Source and destination data sizes
- Source and destination address increment size
- Number of transfers before bus arbitration
- Total number of items to transfer
- Useburst flag
- Transfer mode

The control parameters for a channel can be set using the driver library function:

```
void uDMAChannelControlSet();
```

The µDMA controller updates the transfer size and transfer mode fields as the transfer is performed. At the end of a transfer, the transfer size indicates 0, and the transfer mode indicates stopped. Because the control word is modified by the µDMA controller, the control word must be reconfigured before each new transfer. The source and destination end pointers are not modified, so the source and destination end pointers can be left unchanged if the source or destination addresses remain the same.

Before starting a transfer, a µDMA channel must be enabled by setting the appropriate bit in the DMA.SETCHANNELEN register. A channel can be disabled by setting the channel bit in the DMA.CLEARCHANNELEN register. At the end of a complete µDMA transfer, the controller automatically disables the channel.

19.3.6 Transfer Modes

The µDMA controller supports several transfer modes. Two of the modes support simple, one-time transfers. Several complex modes support a continuous flow of data.

19.3.6.1 Stop Mode

While stop mode is not actually a transfer mode, stop is a valid value for the *mode* field of the control word. When the mode field has the *stop* value, the µDMA controller does not perform any transfers and disables the channel if enabled. The µDMA controller updates the control word to set the mode to stop at the end of a transfer. This mode can be useful in scatter-gather operations.

19.3.6.2 Basic Mode

In basic mode, the µDMA controller performs transfers as long as there are more items to transfer, and a transfer request is present. This mode is used with peripherals that assert a µDMA request signal whenever the peripheral is ready for a data transfer. Basic mode must not be used in any situation where the request is not present during the entire transfer.

The µDMA controller sets the mode for that channel to stop when all of the items have been transferred using basic mode.

19.3.6.3 Auto Mode

Auto mode is similar to basic mode, except that when a transfer request is received, the transfer completes, even if the µDMA request is removed. This mode is suitable for software-triggered transfers. Generally, auto mode is not used with a peripheral.

The µDMA controller sets the mode for that channel to stop when all the items have been transferred using auto mode.

19.3.6.4 Ping-Pong Mode

Ping-pong mode is used to support a continuous data flow to or from a peripheral. Both the primary and alternate data structures must be implemented to use ping-pong mode. Both structures are set up by the processor for data transfer between memory and a peripheral. The transfer is started using the primary control structure.

When the transfer using the primary control structure completes, the µDMA controller reads the alternate control structure for that channel to continue the transfer. Each time this occurs, an interrupt is generated, and the processor can reload the control structure for the just-completed transfer. Data flow can continue indefinitely this way, using the primary and alternate control structures to switch between buffers as the data flows to or from the peripheral.

Figure 19-2 shows an example operation in ping-pong mode.

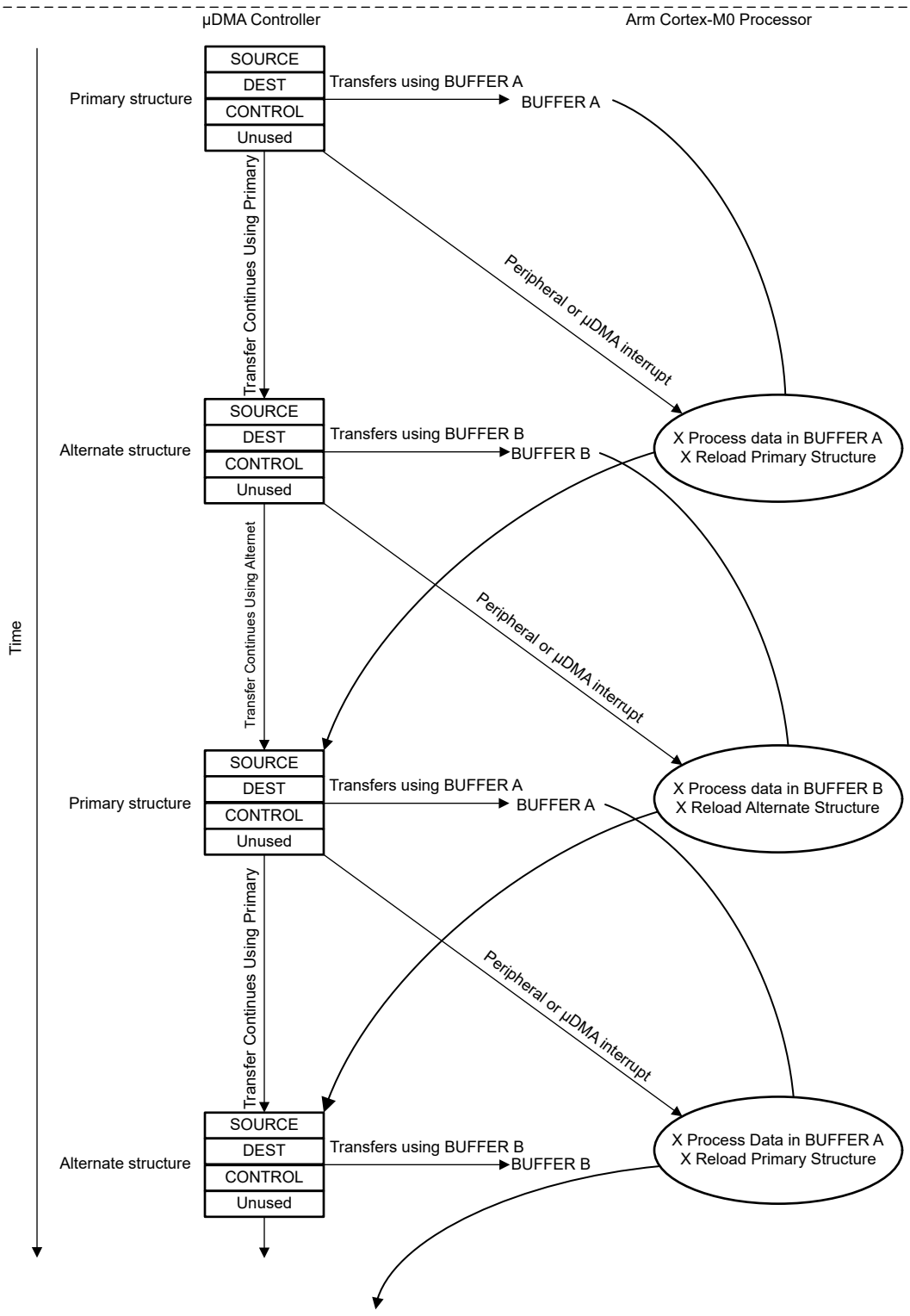


Figure 19-2. Example of Ping-Pong µDMA Transaction

19.3.6.5 Memory Scatter-Gather Mode

Memory scatter-gather mode is a complex mode used when data must be transferred to or from varied locations in memory instead of a set of contiguous locations in a memory buffer. For example, a gather µDMA operation could be used to selectively read the payload of several stored packets of a communication protocol, and store them together in sequence in a memory buffer.

In memory scatter-gather mode, the primary control structure is used to program the alternate control structure from a table in memory. The table is set up by the processor software and contains a list of control structures, each containing the source and destination end pointers, and the control word for a specific transfer. The mode of each control word must be set to memory scatter-gather mode. Each entry in the table is, in turn, copied to the alternate structure where it is then executed. The µDMA controller alternates between using the primary control structure to copy the next transfer instruction from the list, and then executing the new transfer instruction. The end of the list is marked by programming the control word for the last entry to use auto transfer mode. When the last transfer is performed using auto mode, the µDMA controller stops. A completion interrupt is generated only after the last transfer.

It is possible to loop the list by having the last entry copy the primary control structure to point back to the beginning of the list (or to a new list). It is also possible to trigger a set of other channels to perform a transfer, either directly, by programming a write to the software trigger for another channel, or indirectly, by causing a peripheral action that results in a µDMA request.

By programming the µDMA controller using this method, a set of arbitrary transfers can be performed based on a single µDMA request.

Figure 19-3 shows an example of operation in memory scatter-gather mode. This example shows a gather operation, where data in three separate buffers in memory is copied together into one buffer. Figure 19-3 shows how the application sets up a µDMA task list in memory, that is then used by the controller to perform three sets of copy operations from different locations in memory. The primary control structure for the channel used for the operation is configured to copy from the task list to the alternate control structure.

Figure 19-4 shows the sequence as the µDMA controller performs the three sets of copy operations. First, using the primary control structure, the µDMA controller loads the alternate control structure with Task A. The µDMA controller then performs the copy operation specified by Task A, copying the data from the source buffer A to the destination buffer. Next, the µDMA controller again uses the primary control structure to load Task B into the alternate control structure, and then performs the B operation with the alternate control structure. The process is repeated for Task C.

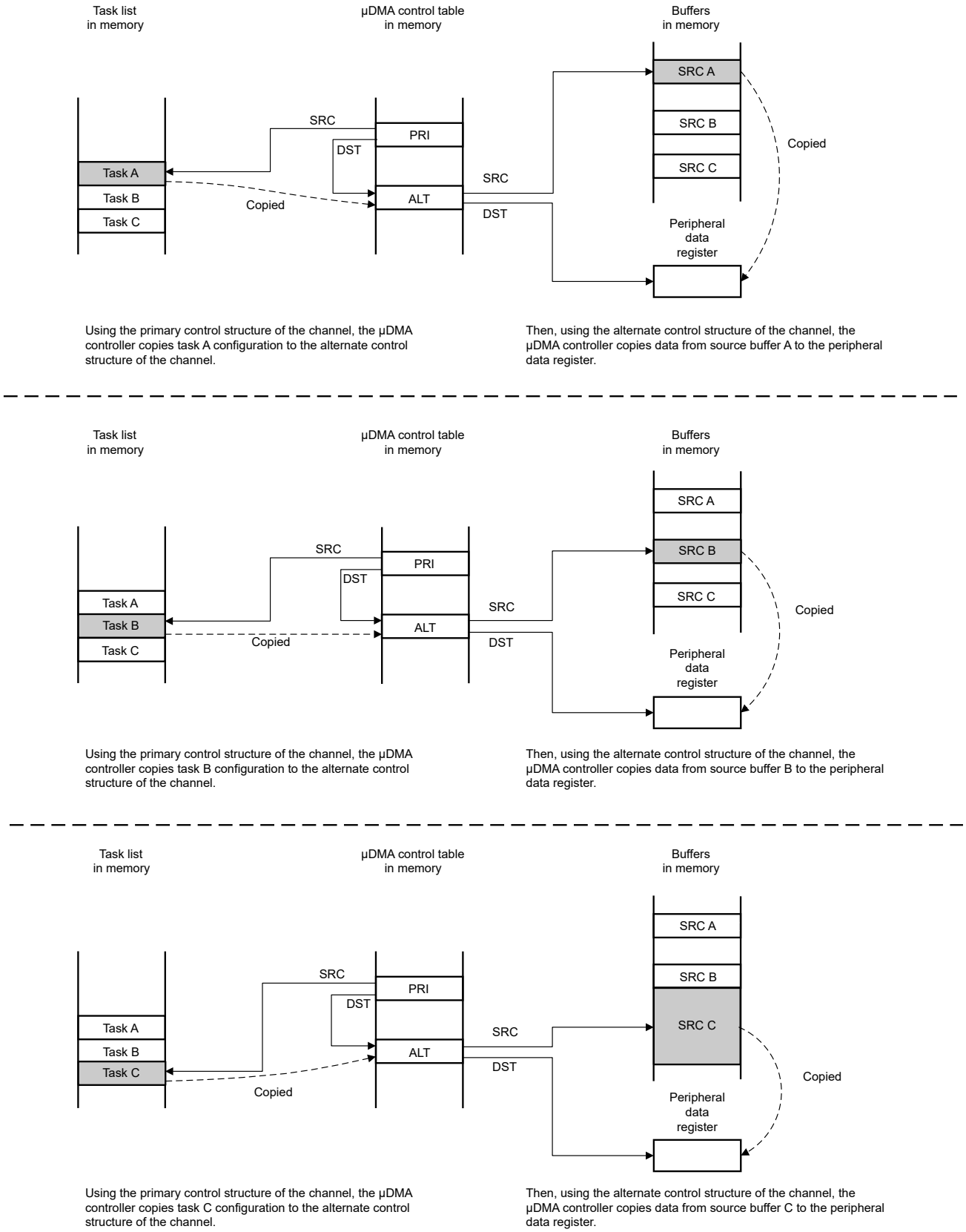
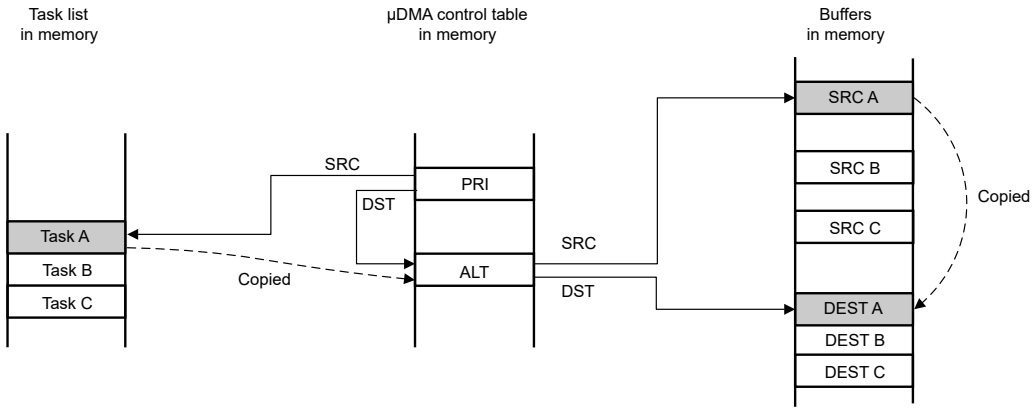


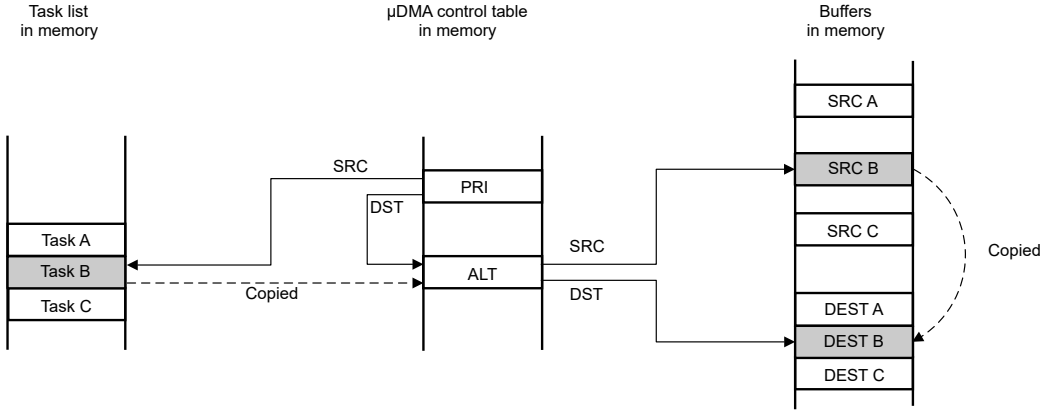
Figure 19-3. Memory Scatter-Gather, Setup, and Configuration

1. The application has a need to copy data items from three separate locations in memory into one combined buffer.
2. The application sets up µDMA "task list" in memory, which contains the pointers and control configuration for three µDMA copy "tasks."
3. The application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the µDMA controller.



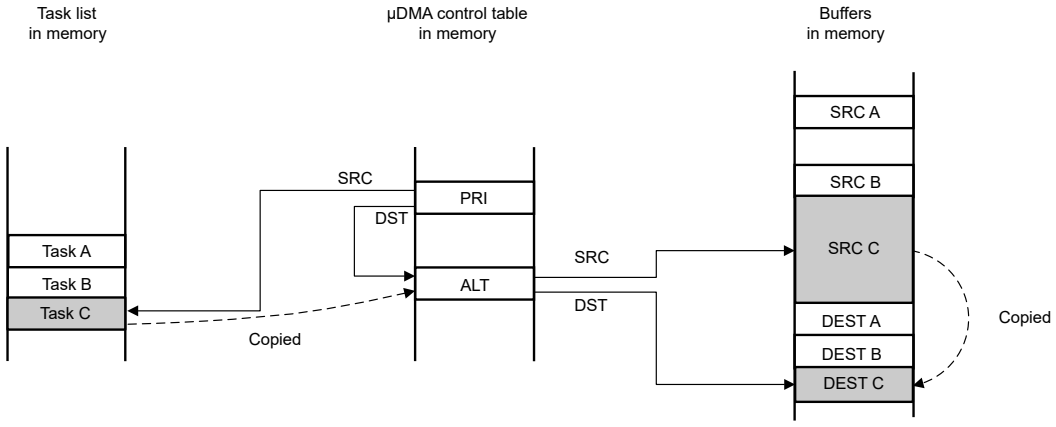
Using the primary control structure of the channel, the µDMA controller copies task A configuration to the alternate control structure of the channel.

Then, using the alternate control structure of the channel, the µDMA controller copies data from source buffer A to the destination buffer.



Using the primary control structure of the channel, the µDMA controller copies task B configuration to the alternate control structure of the channel.

Then, using the alternate control structure of the channel, the µDMA controller copies data from source buffer B to the destination buffer.



Using the primary control structure of the channel, the µDMA controller copies task C configuration to the alternate control structure of the channel.

Then, using the alternate control structure of the channel, the µDMA controller copies data from source buffer C to destination buffer.

Figure 19-4. Memory Scatter-Gather, µDMA Copy Sequence

19.3.6.6 Peripheral Scatter-Gather Mode

Peripheral scatter-gather mode is similar to memory scatter-gather mode, except that the transfers are controlled by a peripheral making a µDMA request. When the µDMA controller detects a request from the peripheral, the µDMA controller uses the primary control structure to copy one entry from the list to the alternate control structure, and then performs the transfer. At the end of this transfer, the next transfer is started only if the peripheral again asserts a µDMA request. The µDMA controller continues to perform transfers from the list only when the peripheral makes a request, until the last transfer completes. A completion interrupt is generated only after the last transfer.

By using this method, the µDMA controller can transfer data to or from a peripheral from a set of arbitrary locations whenever the peripheral is ready to transfer data.

Figure 19-5 shows an example of operation in peripheral scatter-gather mode. This example shows a gather operation where data from three separate buffers in memory is copied to a single peripheral data register. Figure 19-5 shows how the application sets up a µDMA task list in memory, that is then used by the controller to perform three sets of copy operations from different locations in memory. The primary control structure for the channel used for the operation is configured to copy from the task list to the alternate control structure.

Figure 19-6 shows the sequence as the µDMA controller performs the three sets of copy operations. First, using the primary control structure, the µDMA controller loads the alternate control structure with Task A. The µDMA controller then performs the copy operation specified by Task A, copying the data from the source buffer A to the peripheral data register. Next, the µDMA controller again uses the primary control structure to load Task B into the alternate control structure, and then performs the B operation with the alternate control structure. The process is repeated for Task C.

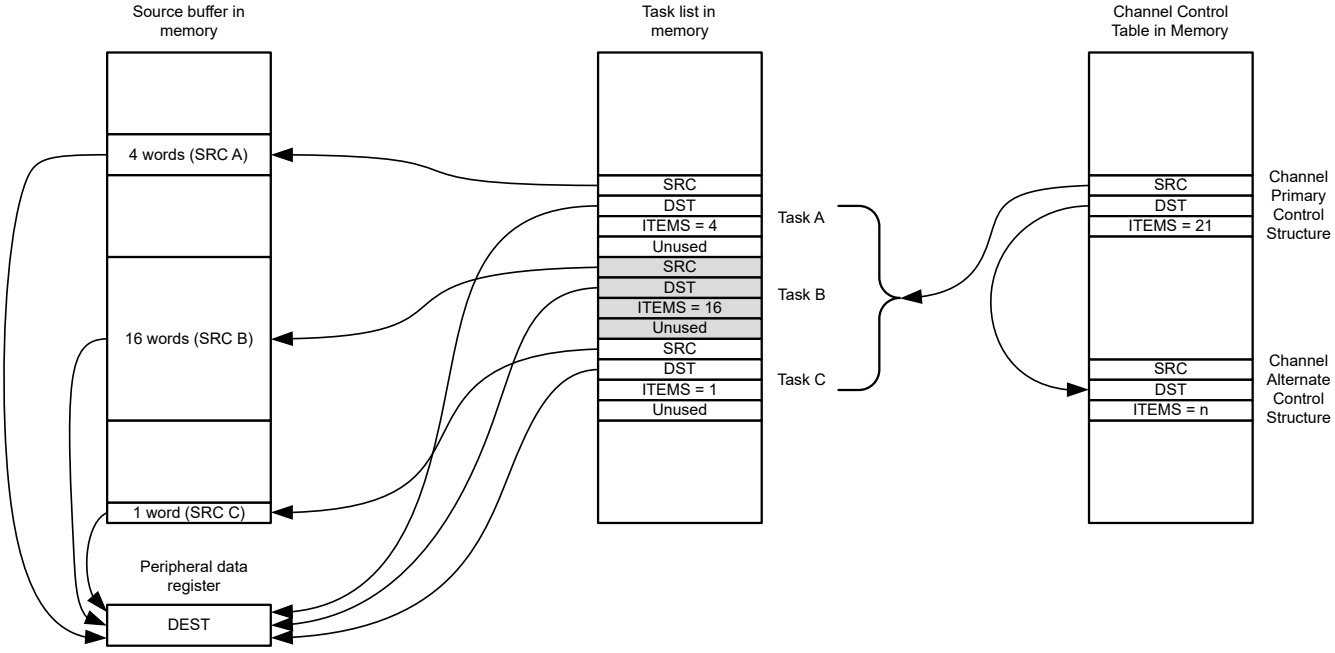
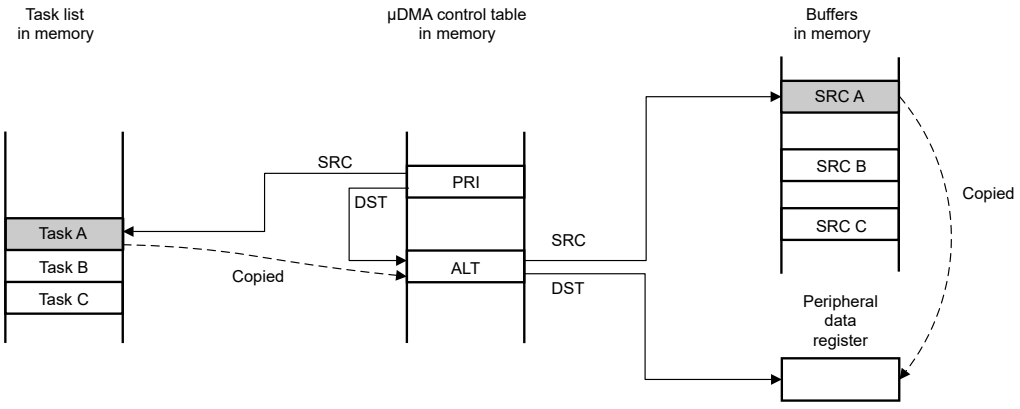


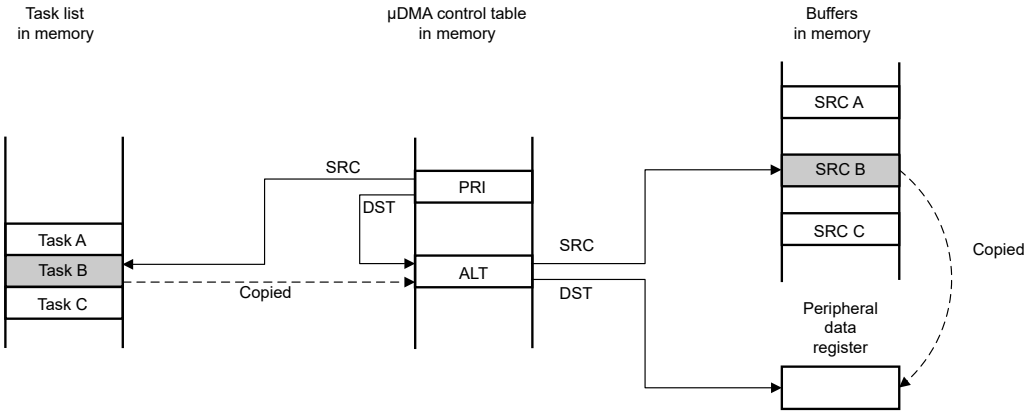
Figure 19-5. Peripheral Scatter-Gather, Setup, and Configuration

1. The application has a need to copy data items from three separate locations in memory into a peripheral data register.
2. The application sets up the µDMA "task list" in memory, which contains the pointers and control configuration for three µDMA copy "tasks."
3. The application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the µDMA controller.



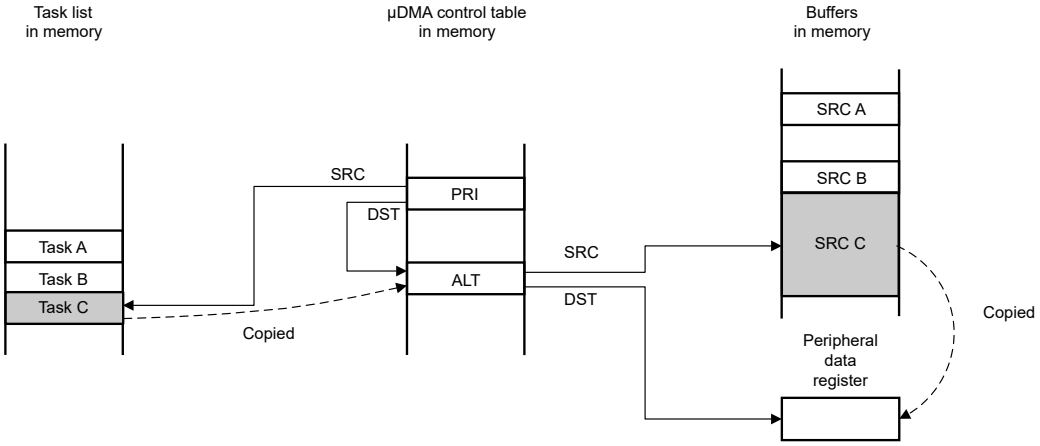
Using the primary control structure of the channel, the µDMA controller copies task A configuration to the alternate control structure of the channel.

Then, using the alternate control structure of the channel, the µDMA controller copies data from source buffer A to the peripheral data register.



Using the primary control structure of the channel, the µDMA controller copies task B configuration to the alternate control structure of the channel.

Then, using the alternate control structure of the channel, the µDMA controller copies data from source buffer B to the peripheral data register.



Using the primary control structure of the channel, the µDMA controller copies task C configuration to the alternate control structure of the channel.

Then, using the alternate control structure of the channel, the µDMA controller copies data from source buffer C to the peripheral data register.

Figure 19-6. Peripheral Scatter-Gather, µDMA Copy Sequence

19.3.7 Transfer Size and Increments

The µDMA controller supports transfer data sizes of 8, 16, or 32 bits. The source and destination data size must be the same for any given transfer. The source and destination address can be automatically incremented by bytes, half-words, words, or set to no increment. The source and destination address increment values can be set independently; it is not necessary for the address increment to match the data size, as long as the increment is the same or larger than the data size. For example, it is possible to perform a transfer using 8-bit data size by using an address increment of full words (4 bytes). The data to be transferred must be aligned in memory according to the data size (8, 16, or 32 bits).

Table 19-5 provides the configuration to read from a peripheral that supplies 8-bit data.

Table 19-5. µDMA Read Example: 8-Bit Peripheral

Field	Configuration
Source data size	8 bits
Destination data size	8 bits
Source address increment	No increment
Destination address increment	Byte
Source end pointer	Peripheral read FIFO register
Destination end pointer	End of the data buffer in memory

19.3.8 Peripheral Interface

Each peripheral that supports µDMA has a single request or burst request signal that is asserted when the peripheral is ready to transfer data (see Table 19-2). The request signal can be disabled or enabled using the DMA.SETREQMASK and DMA.CLEARREQMASK registers, respectively. The µDMA request signal is disabled or masked when the channel request mask bit is set. When the request is not masked and the µDMA channel is configured correctly and enabled, the peripheral asserts the request signal and the µDMA controller begins the transfer.

Note

The peripheral must disable all interrupts to the event fabric when using µDMA to transfer data to and from a peripheral.

When a µDMA transfer is complete, the µDMA controller generates an interrupt; for more information, see Section 19.3.10.

For more information on how a specific peripheral interacts with the µDMA controller, refer to the DMA Operation section in the chapter that discusses that peripheral.

19.3.9 Software Request

Channels can be set up to perform software transfers through the DMA.SOFTREQ register. If the channel used for software is also tied to a specific peripheral, the dma_done/interrupt signal is provided directly to the Arm® Cortex®-M33 CPU instead of sending the signal to the peripheral. The interrupt used is a combined interrupt, software µDMA interrupt, for all software transfers.

If software uses a µDMA channel of the peripheral to initiate a request, then the completion interrupt occurs on the interrupt vector for the peripheral instead of occurring on the software interrupt vector.

Note

DMA software requests are specified on DMA channels 8, 9, 10, and 11.

19.3.10 Interrupts and Errors

The µDMA controller generates a completion interrupt on the interrupt vector of the peripheral when a µDMA transfer completes. Therefore, if µDMA is used to transfer data for a peripheral and interrupts are used, then the

interrupt handler for that peripheral must be designed to handle the µDMA transfer completion interrupt. If the transfer uses the software µDMA channel, then the completion interrupt occurs on the dedicated software µDMA interrupt vector (see Table 19-6).

When µDMA is enabled for a peripheral, the µDMA controller stops the normal transfer interrupts for a peripheral from reaching the interrupt controller (INTC). The interrupts are still reported in the interrupt registers of the peripheral. Thus, when a large amount of data is transferred using µDMA, instead of receiving multiple interrupts from the peripheral as data flows, the INTC receives only one interrupt when the transfer completes. Unmasked peripheral error interrupts continue to be sent to the INTC.

When a µDMA channel generates a completion interrupt, the CHNLS bit corresponding to the peripheral channel is set in the DMA Channel Request Done register, DMA.REQDONE. This register can be used by the interrupt handler code of the peripheral to determine if the interrupt was caused by the µDMA channel or an error event reported by the interrupt registers of the peripheral. The completion interrupt request from the µDMA controller is automatically cleared when the interrupt handler is activated.

If the µDMA controller encounters a bus or memory protection error when trying to perform a data transfer, the controller disables the µDMA channel that caused the error and generates an interrupt on the µDMA error interrupt vector. The processor can read the DMA Clear Bus Error register, DMA.ERROR[0] STATUS bit to determine if an error is pending. The STATUS bit is set if an error occurred. The error can be cleared by setting the STATUS bit to 1.

Note

The µDMA error event is connected as an interrupt to Arm Cortex-M33 processor via event fabric.

Table 19-6 lists the dedicated interrupt assignments for the µDMA controller.

Table 19-6. µDMA Interrupt Assignments

Interrupt	Assignment
28	µDMA software channel transfer done
29	µDMA error

19.3.11 Initialization and Configuration

19.3.11.1 Module Initialization

The µDMA controller resides in the peripheral domain, which must be powered up to enable the µDMA controller. The following steps are necessary:

1. Enable the µDMA controller by setting the CLKCTL.CLKENSET0[17] DMA bit or by using the driver library function:

```
Power_enable_DMA()
```

2. Enable the µDMA controller by setting the DMA Configuration register, DMA.CFG[0] MASTERENABLE bit.
3. Program the location of the channel control table by writing the base address of the table to the DMA Channel Control Base Pointer register, DMA.CTRL. The base address must be aligned on a 256-byte boundary.

19.3.11.2 Configuring a Memory-to-Memory Transfer

The µDMA channels 6 and 7 are dedicated for software-initiated transfers. This specific example uses channel 6. No attributes must be set for a software-based transfer. The attributes are cleared by default, but are explicitly cleared as shown in the following sections.

19.3.11.3 Configure the Channel Attributes

Configure the channel attributes as follows, or use the following driver library function:

```
uDMAChannelAttributeDisable(uint32_t ui32Base, uint32_t ui32ChannelNum, uint32_t ui32Attr)
```

1. Program bit 0 of the DMA Set Channel Priority register, DMA.SETCHNLPRIORITY, or the DMA Clear Channel Priority register, DMA.CLEARCHNLPRIORITY, to set the channel to high priority or default priority.
2. Set bit 6 of the DMA Clear Channel Primary Alternate register, DMA.CLEARCHNLPRIALT, to select the primary channel control structure for this transfer.
3. Set bit 6 of the DMA Channel Clear Useburst register, DMA.CLEARBURST, to allow the µDMA controller to respond to single requests and burst requests.
4. Set bit 6 of the DMA Clear Channel Request Mask register, DMA.CLEARREQMASK, to allow the µDMA controller to recognize requests for this channel.

19.3.11.4 Configure the Channel Control Structure

This example transfers 256 words from one memory buffer to another. Channel 6 is used for a software transfer, and the control structure for channel 6 must be configured to transfer 8-bit data with source and destination increments in bytes and byte-wise buffer copy. A bus arbitration size of eight can be used here.

The transfer buffer and transfer size are now configured. The transfer uses auto mode, which means that the transfer automatically runs to completion after the first request.

19.3.11.5 Start the Transfer

Finally, the channel must be enabled. A request must also be made because this is a software-initiated transfer. The request starts the transfer.

1. Enable global interrupts:

```
IntMasterEnable()
```

   and enable interrupt for µDMA:

```
IntEnable(uint32_t ui32Interrupt)
```

2. Enable the channel by setting bit 0 of the µDMA Set Channel Enable register, DMA.SETCHANNELEN.
3. Issue a transfer request by setting bit 0 of the µDMA Channel Software Request register, DMA.SOFTREQ.
4. The µDMA transfer begins. If the interrupt is enabled, then the processor is notified by interrupt when the transfer completes.

If needed, the status can be checked by reading the DMA.SETCHANNELEN register bit 0. This bit is automatically cleared when the transfer completes.

19.3.11.6 Software Considerations

The µDMA driver should not disable µDMA when it has active transactions.The behavior when µDMA starts up again is not defined and by the time µDMA is re-enabled, peripheral state and memory contents might have changed.

Software should also take care that no new request should be created when setting IDLE REQ high for µDMA. Software must also ensure that all µDMA channels from peripherals are disabled before entering standby, so no new requests are generated when µDMA is being disabled.

If the software doesn't take care of turning off µDMA only after all ongoing µDMA transactions are completed, and instead turns the clocks off in the middle of a transfer sequence – µDMA just ensures that the current transaction is cleanly terminated and the bus does not hang – but it does not wait until all transactions within the ongoing sequence are completed (which might take an arbitrarily large amount of time).

19.4 DMA Registers

Table 19-7 lists the memory-mapped registers for the DMA registers. All register offset addresses not listed in Table 19-7 should be considered as reserved locations and the register contents should not be modified.

Table 19-7. DMA Registers

Offset	Acronym	Register Name	Section
0h	STATUS	Status Register.	Section 19.4.1
4h	CFG	Configuration Register.	Section 19.4.2
8h	CTRL	Channel Control Data Base Pointer Register.	Section 19.4.3
Ch	ALTCTRL	Channel Alternate Control Data Base Pointer Register.	Section 19.4.4
10h	WAITONREQ	Channel Wait On Request Status Register.	Section 19.4.5
14h	SOFTREQ	Channel Software Request Register.	Section 19.4.6
18h	SETBURST	Channel Set UseBurst Register.	Section 19.4.7
1Ch	CLEARBURST	Channel Clear UseBurst Register.	Section 19.4.8
20h	SETREQMASK	Channel Set Request Mask Register.	Section 19.4.9
24h	CLEARREQMASK	Clear Channel Request Mask Register.	Section 19.4.10
28h	SETCHANNELEN	Set Channel Enable Register.	Section 19.4.11
2Ch	CLEARCHANNELEN	Clear Channel Enable Register.	Section 19.4.12
30h	SETCHNLPRIALT	Channel Set Primary-Alternate Register.	Section 19.4.13
34h	CLEARCHNLPRIALT	Channel Clear Primary-Alternate Register.	Section 19.4.14
38h	SETCHNLPRIORITY	Set Channel Priority Register.	Section 19.4.15
3Ch	CLEARCHNLPRIORITY	Clear Channel Priority Register.	Section 19.4.16
4Ch	ERROR	Error Status and Clear Register.	Section 19.4.17
504h	REQDONE	Channel Request Done Register.	Section 19.4.18
520h	DONEMASK	Channel Request Done Mask Register.	Section 19.4.19

Complex bit access types are encoded to fit into small table cells. Table 19-8 shows the codes that are used for access types in this section.

Table 19-8. DMA Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

19.4.1 STATUS Register (Offset = 0h) [Reset = 00000000h]

STATUS is shown in Table 19-9.

Return to the Summary Table.

Status Register.

Table 19-9. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TEST	R	0h	;0x0: Controller does not include the integration test logic;0x1: Controller includes the integration test logic;0x2: Undefined;...;0xF: Undefined
27-21	RESERVED	R	0h	Reserved
20-16	TOTALCHANNELS	R	Bh	Register value returns number of available uDMA channels minus one. For example a read out value of:;0x00: Show that the controller is configured to use 1 uDMA channel;0x01: Shows that the controller is configured to use 2 uDMA channels;...;0x1F: Shows that the controller is configured to use 32 uDMA channels (32-1=31=0x1F)
15-8	RESERVED	R	0h	Reserved
7-4	STATE	R	0h	Current state of the control state machine. State can be one of the following:;0x0: Idle;0x1: Reading channel controller data;0x2: Reading source data end pointer;0x3: Reading destination data end pointer;0x4: Reading source data;0x5: Writing destination data;0x6: Waiting for uDMA request to clear;0x7: Writing channel controller data;0x8: Stalled;0x9: Done;0xA: Peripheral scatter-gather transition;0xB: Undefined;...;0xF: Undefined.
3-1	RESERVED	R	0h	Reserved
0	MASTERENABLE	R	0h	Shows the enable status of the controller as configured by CFG.MASTERENABLE: 0h = Controller is disabled 1h = Controller is enabled

19.4.2 CFG Register (Offset = 4h) [Reset = 00000000h]

CFG is shown in Table 19-10.

Return to the Summary Table.

Configuration Register.

Table 19-10. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-5	PRTOCTRL	W	0h	Sets the AHB-Lite bus protocol protection state by controlling the AHB signal HProt[3:1] as follows:;Bit [7] Controls HProt[3] to indicate if a cacheable access is occurring.;Bit [6] Controls HProt[2] to indicate if a bufferable access is occurring.;Bit [5] Controls HProt[1] to indicate if a privileged access is occurring.;When bit [n] = 1 then the corresponding HProt bit is high.;When bit [n] = 0 then the corresponding HProt bit is low.;This field controls HProt[3:1] signal for all transactions initiated by uDMA except two transactions below:;- the read from the address indicated by source address pointer;- the write to the address indicated by destination address pointer;HProt[3:1] for these two exceptions can be controlled by dedicated fields in the channel configutation descriptor.
4-1	RESERVED	R	0h	Reserved
0	MASTERENABLE	W	0h	Enables the controller. 0h = Disables the controller 1h = Enables the controller

19.4.3 CTRL Register (Offset = 8h) [Reset = 00000000h]

CTRL is shown in Table 19-11.

Return to the Summary Table.

Channel Control Data Base Pointer Register.

Table 19-11. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	BASEPTR	R/W	Xh	This register point to the base address for the primary data structures of each DMA channel. This is not stored in module, but in system memory, thus space must be allocated for this usage when DMA is in usage
8-0	RESERVED	R	0h	Reserved

19.4.4 ALTCTRL Register (Offset = Ch) [Reset = 00000000h]

ALTCTRL is shown in Table 19-12.

Return to the Summary Table.

Channel Alternate Control Data Base Pointer Register.

Table 19-12. ALTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASEPTR	R	100h	This register shows the base address for the alternate data structures and is calculated by module, thus read only

19.4.5 WAITONREQ Register (Offset = 10h) [Reset = 00000000h]

WAITONREQ is shown in Table 19-13.

Return to the Summary Table.

Channel Wait On Request Status Register.

Table 19-13. WAITONREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLSTATUS	R	FFFh	Channel wait on request status:;Bit [Ch] = 0: Once uDMA receives a single or burst request on channel Ch, this channel may come out of active state even if request is still present.;Bit [Ch] = 1: Once uDMA receives a single or burst request on channel Ch, it keeps channel Ch in active state until the requests are deasserted. This handshake is necessary for channels where the requester is in an asynchronous domain or can run at slower clock speed than uDMA

19.4.6 SOFTREQ Register (Offset = 14h) [Reset = 00000000h]

SOFTREQ is shown in Table 19-14.

Return to the Summary Table.

Channel Software Request Register.

Table 19-14. SOFTREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	W	0h	Set the appropriate bit to generate a software uDMA request on the corresponding uDMA channel;Bit [Ch] = 0: Does not create a uDMA request for channel Ch;Bit [Ch] = 1: Creates a uDMA request for channel Ch;Writing to a bit where a uDMA channel is not implemented does not create a uDMA request for that channel

19.4.7 SETBURST Register (Offset = 18h) [Reset = 00000000h]

SETBURST is shown in Table 19-15.

Return to the Summary Table.

Channel Set UseBurst Register.

Table 19-15. SETBURST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Returns the useburst status, or disables individual channels from generating single uDMA requests. The value R is the arbitration rate and stored in the controller data structure. ;Read as:;Bit [Ch] = 0: uDMA channel Ch responds to both burst and single requests on channel Ch. The controller performs 2^R, or single, bus transfers.;Bit [Ch] = 1: uDMA channel Ch does not respond to single transfer requests. The controller only responds to burst transfer requests and performs 2^R transfers.;Write as:;Bit [Ch] = 0: No effect. Use the CLEARBURST.CHNLS to set bit [Ch] to 0.;Bit [Ch] = 1: Disables single transfer requests on channel Ch. The controller performs 2^R transfers for burst requests.;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.8 CLEARBURST Register (Offset = 1Ch) [Reset = 00000000h]

CLEARBURST is shown in Table 19-16.

Return to the Summary Table.

Channel Clear UseBurst Register.

Table 19-16. CLEARBURST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	W	0h	Set the appropriate bit to enable single transfer requests. ;Write as:;Bit [Ch] = 0: No effect. Use the SETBURST.CHNLS to disable single transfer requests.;Bit [Ch] = 1: Enables single transfer requests on channel Ch.;Writing to a bit where a uDMA channel is not implemented has no effect.

19.4.9 SETREQMASK Register (Offset = 20h) [Reset = 00000000h]

SETREQMASK is shown in Table 19-17.

Return to the Summary Table.

Channel Set Request Mask Register.

Table 19-17. SETREQMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Returns the burst and single request mask status, or disables the corresponding channel from generating uDMA requests. ;Read as:;Bit [Ch] = 0: External requests are enabled for channel Ch.;Bit [Ch] = 1: External requests are disabled for channel Ch.;Write as:;Bit [Ch] = 0: No effect. Use the CLEARREQMASK.CHNLS to enable uDMA requests.;Bit [Ch] = 1: Disables uDMA burst request channel [Ch] and uDMA single request channel [Ch] input from generating uDMA requests.;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.10 CLEARREQMASK Register (Offset = 24h) [Reset = 00000000h]

CLEARREQMASK is shown in Table 19-18.

Return to the Summary Table.

Clear Channel Request Mask Register.

Table 19-18. CLEARREQMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	W	0h	Set the appropriate bit to enable uDMA request for the channel. ;Write as:;Bit [Ch] = 0: No effect. Use the SETREQMASK.CHNLS to disable channel Ch from generating requests.;Bit [Ch] = 1: Enables channel [Ch] to generate uDMA requests.;Writing to a bit where a uDMA channel is not implemented has no effect.

19.4.11 SETCHANNELEN Register (Offset = 28h) [Reset = 00000000h]

SETCHANNELEN is shown in Table 19-19.

Return to the Summary Table.

Set Channel Enable Register.

Table 19-19. SETCHANNELEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Returns the enable status of the channels, or enable the corresponding channels. ;Read as:;Bit [Ch] = 0: Channel Ch is disabled.;Bit [Ch] = 1: Channel Ch is enabled.;Write as:;Bit [Ch] = 0: No effect. Use the CLEARCHANNELEN.CHNLS to disable a channel;Bit [Ch] = 1: Enables channel Ch;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.12 CLEARCHANNELEN Register (Offset = 2Ch) [Reset = 00000000h]

CLEARCHANNELEN is shown in Table 19-20.

Return to the Summary Table.

Clear Channel Enable Register.

Table 19-20. CLEARCHANNELEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	W	0h	Set the appropriate bit to disable the corresponding uDMA channel. ;Write as:;Bit [Ch] = 0: No effect. Use the SETCHANNELEN.CHNLS to enable uDMA channels.;Bit [Ch] = 1: Disables channel Ch;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.13 SETCHNLPRIALT Register (Offset = 30h) [Reset = 00000000h]

SETCHNLPRIALT is shown in Table 19-21.

Return to the Summary Table.

Channel Set Primary-Alternate Register.

Table 19-21. SETCHNLPRIALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Returns the channel control data structure status, or selects the alternate data structure for the corresponding uDMA channel. ;Read as:;Bit [Ch] = 0: uDMA channel Ch is using the primary data structure.;Bit [Ch] = 1: uDMA channel Ch is using the alternate data structure.;Write as:;Bit [Ch] = 0: No effect. Use the CLEARCHNLPRIALT.CHNLS to disable a channel;Bit [Ch] = 1: Selects the alternate data structure for channel Ch;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.14 CLEARCHNLPRIALT Register (Offset = 34h) [Reset = 00000000h]

CLEARCHNLPRIALT is shown in Table 19-22.

Return to the Summary Table.

Channel Clear Primary-Alternate Register.

Table 19-22. CLEARCHNLPRIALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	W	0h	Clears the appropriate bit to select the primary data structure for the corresponding uDMA channel.;Write as:;Bit [Ch] = 0: No effect. Use the SETCHNLPRIALT.CHNLS to select the alternate data structure.;Bit [Ch] = 1: Selects the primary data structure for channel Ch.;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.15 SETCHNLPRIORITY Register (Offset = 38h) [Reset = 00000000h]

SETCHNLPRIORITY is shown in Table 19-23.

Return to the Summary Table.

Set Channel Priority Register.

Table 19-23. SETCHNLPRIORITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Returns the channel priority mask status, or sets the channel priority to high. ;Read as:;Bit [Ch] = 0: uDMA channel Ch is using the default priority level.;Bit [Ch] = 1: uDMA channel Ch is using a high priority level.;Write as:;Bit [Ch] = 0: No effect. Use the CLEARCHNLPRIORITY.CHNLS to set channel Ch to the default priority level.;Bit [Ch] = 1: Channel Ch uses the high priority level.;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.16 CLEARCHNLPRIORITY Register (Offset = 3Ch) [Reset = 00000000h]

CLEARCHNLPRIORITY is shown in Table 19-24.

Return to the Summary Table.

Clear Channel Priority Register.

Table 19-24. CLEARCHNLPRIORITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	W	0h	Clear the appropriate bit to select the default priority level for the specified uDMA channel.;Write as:;Bit [Ch] = 0: No effect. Use the SETCHNLPRIORITY.CHNLS to set channel Ch to the high priority level.;Bit [Ch] = 1: Channel Ch uses the default priority level.;Writing to a bit where a uDMA channel is not implemented has no effect

19.4.17 ERROR Register (Offset = 4Ch) [Reset = 00000000h]

ERROR is shown in Table 19-25.

Return to the Summary Table.

Error Status and Clear Register.

Table 19-25. ERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STATUS	R/W	0h	Returns the status of bus error flag in uDMA, or clears this bit ;Read as:;0: No bus error detected;1: Bus error detected;Write as:;0: No effect, status of bus error flag is unchanged.;1: Clears the bus error flag.

19.4.18 REQDONE Register (Offset = 504h) [Reset = 00000000h]

REQDONE is shown in Table 19-26.

Return to the Summary Table.

Channel Request Done Register.

Table 19-26. REQDONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Reflects the uDMA done status for the given channel, channel [Ch]. It's a sticky done bit. Unless cleared by writing a 1, it holds the value of 1.;Read as:;Bit [Ch] = 0: Request has not completed for channel Ch;Bit [Ch] = 1: Request has completed for the channel Ch;Writing a 1 to individual bits would clear the corresponding bit. ;Write as:;Bit [Ch] = 0: No effect.;Bit [Ch] = 1: The corresponding [Ch] bit is cleared and is set to 0

19.4.19 DONEMASK Register (Offset = 520h) [Reset = 00000000h]

DONEMASK is shown in Table 19-27.

Return to the Summary Table.

Channel Request Done Mask Register.

Table 19-27. DONEMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	CHNLS	R/W	0h	Controls the propagation of the uDMA done and active state to the assigned peripheral. Specifically used for software channels.;Read as:;Bit [Ch] = 0: uDMA done and active state for channel Ch is not blocked from reaching to the peripherals. ;Note that the uDMA done state for channel [Ch] is blocked from contributing to generation of combined uDMA done signal;Bit [Ch] = 1: uDMA done and active state for channel Ch is blocked from reaching to the peripherals. ;Note that the uDMA done state for channel [Ch] is not blocked from contributing to generation of combined uDMA done signal ;Write as:;Bit [Ch] = 0: Allows uDMA done and active state to propagate to the peripherals. ;Note that this disables uDMA done state for channel [Ch] from contributing to generation of combined uDMA done signal;Bit [Ch] = 1: Blocks uDMA done and active state to propagate to the peripherals. ;Note that this enables uDMA done for channel [Ch] to contribute to generation of combined uDMA done signal.

Chapter 20

Advanced Encryption Standard (AES)

This chapter describes the functionality of the Advanced Encryption Standard (AES) system.

20.1 Introduction

The AES accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit key in hardware according to the Advanced Encryption Standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197. Encryption converts data to an unintelligible form called ciphertext. Decryption converts the ciphertext back into the original form called plaintext.

Features

- AES supports AES-128 block cipher encryption
- AES supports the following cipher modes for encryption: ECB, CBC-MAC, CBC, CTR, CFB, OFB, PCBC
- CCM can also be accelerated by software configuring CBC-MAC and CTR modes accordingly
- Decryption of cipher modes are supported, except for ECB, CBC and PCBC
- The module supports AES CTR-DRBG acceleration
- Data can be routed to and from the module through CPU and µDMA
- µDMA interface includes 2 channels to enable parallel execution of writing and reading data
- µDMA is capable of feeding the module in all listed cipher modes
- Capable of completing 256 B CCM using the AES module within 60 µs
- AES implements hardware features to minimize bus traffic and disturbances to running code
- AES key is stored within AES module, avoiding need to re-load the key for every encryption operation
- Implements hardware acceleration and configurable increment option for AES-CTR modes
- Supports writing next block of plaintext during ongoing encryption, which enables parallel processing

20.1.1 AES Performance

The Finite State Machine (FSM) processes the data in a column-fashioned way, processing 2 columns/cycle, completing 10 rounds in 20 cycles. With three cycles of pre-processing, the execution/encryption time is 23 cycles or 5.56bits/cycle.

20.2 Functional Description

The AES accelerator consists of the register interface and the finite state machine (FSM).

The register bank provides various options to the user to configure the plaintext source, encryption triggers, µDMA channel triggers, counter size, endianness, alignment, and actions that clear status events and IRQs. In addition to key storage register, there are registers for plaintext and buffer. Users can also configure side effects such as XORing, clearing of events or IRQs, and generation of µDMA and AES triggers. Due to these options, external intervention by the CPU or µDMA is kept to a minimum, thereby significantly increasing throughput.

The FSM operates on the input block, performing the required substitution, shift, and mix operations. A new subkey is generated and XORed with the data each round. Round keys are generated on-the-fly and parallel to data processing. To accommodate CTR cipher mode, the IP offers a 128-bit register acting either as a counter in CTR cipher mode or acting as a pipeline buffer to enable update of next plaintext/ciphertext while AES-128 encryption is ongoing.

Data blocks can be transferred to and from AES either through µDMA or CPU.

AES supports key programming from the HSM. This allows key to be fetched from a secure key store in HSM and configured into AES. However, configuring AES operation and transferring plaintext and ciphertext, shall be still done by the CPU/µDMA.

The KEY0 to KEY3 registers are protected from partial writes to ensure it is not infringed by any malicious software. When a different AHB initiator, say H1, writes to any of the KEY registers, STA.KEYSTATE is cleared indicating that the KEY is not completely written and hence not valid. Only after all the other KEY bits are written by H1, STA.KEYSTATE is set back to 1. In short, STA.KEYSTATE is asserted only when all the bits in KEY0 to KEY3 are written by the same initiator. AES operations are allowed only after the STA.KEYSTATE is set.

20.2.1 Reset Considerations

A hardware reset will reset all the registers. After reset, KEY, µDMA, AUTOCFG registers should be re-initialized.

20.2.2 Interrupt and Event Support

20.2.2.1 Interrupt Events and Requests

The following are the interrupt sources

- Channel A µDMA done
- Channel B µDMA done
- Start of AES operation
- End of AES operation

20.2.2.2 Connection to Event Fabric

The combined OR of the AES.MIS register bits generates an event, which is connected to the SVT/MCU Event Fabric module. See Chapter 4 for more information.

20.2.3 µDMA

µDMA channel numbers four and five are assigned to AES Channels A and B. Each channel has an interface consisting of µDMA request and µDMA done signals. Configure µDMA channels to specify the total transfers. For multi-block encryption, specify the total transfers required for all the blocks. The µDMA request signal is generated by AES to alert µDMA for data transfer. The µDMA done signal from the µDMA indicates the completion of all data transfers.

Note

Channel A has higher priority over Channel B.

20.2.3.1 µDMA Example

Consider AES encryption has to be performed on 4 blocks of 128-bit plaintext which is stored in SRAM. The primary control structure of µDMA Channel 4 which is assigned to AES channel A, can be configured as below, to transfer the plaintext from SRAM to AES.

Transfer size	16 words
Source end pointer	Plaintext memory location in SRAM
Destination end pointer	[DMA.DMACHA]
Source Increment	32 bits
Destination Increment	None
Arbitration size	4 words
Transfer Mode	Basic

µDMA channel 5 which is assigned to AES channel B, can be configured as below, to transfer ciphertext from AES to SRAM

Transfer size	16 words
Source end pointer	[DMA.DMACHB]
Destination end pointer	SRAM memory location to store ciphertext
Source Increment	None
Destination Increment	32 bits
Arbitration size	4 words
Transfer Mode	Basic

Note

The address pointed by [DMA.DMACHA] and [DMA.DMACHB] is automatically incremented within the design after every transfer. Thus, the Destination Increment and Source Increment for AES channel A and channel B, respectively, is configured as None.

Refer to Chapter 19 for more details on configuring µDMA channels.

20.3 Encryption and Decryption Configuration

Each of the following modes can be accelerated either through µDMA or CPU. This section provides sequence of operations which includes initialization and separate steps for µDMA and CPU data transfer.

20.3.1 CBC-MAC (Cipher Block Chaining-Message Authentication Code)

The fastest way to accelerate CBC-MAC is to upload the next plaintext during the current encryption.

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- AUTOCFG:
  - AESSRC = TXTXBUF
  - TRGAES = WRBUF3 (Write to BUF3 triggers AES)
  - BUSHALT = EN
- Write 0 to TXT0-TXT3

Cipher mode with µDMA:

- µDMA channel A moves m[1:x] into BUF when a new AES operation starts:
  - ADRCHA = BUF0
  - TRGCHA = AESSTART
- START: CPU writes 0x1 to TRG.DMACHA to start CBC-MAC
- END : CPU waits for µDMA done and STA.STATE = IDLE, then reads result/TAG/MIC from TXT0-TXT3

Cipher mode with CPU:

- for i = 1; i<=x, increment i:
  - Write m[i] to BUF
- Wait until STA.STATE = IDLE
- Read result/TAG/MIC from TXT0-TXT3

20.3.2 CBC (Cipher Block Chaining) Encryption

The fastest way to accelerate this cipher mode is to upload the next plaintext during the current encryption.

An Initialization Vector (IV) is used to randomize the encryption so that distinct ciphertexts are produced even if the same plaintext is encrypted multiple times. Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- AUTOCFG
  - AESSRC = TXTXBUF
  - TRGAES = RDTXT3 | WRBUF3S (the first encryption starts by writing BUF3, the successive ones by reading TXT3)
- Write IV to TXT0-TXT3

Cipher mode with µDMA:

Assumes CHA has written new plaintext to BUF before reading ciphertext.

- µDMA channel A moves m[1:x] into BUF when a new encryption starts
  - ADRCHA = BUF0
  - TRGCHA = AESSTART
  - DONEACT = GATE_TRGAES_ON_CHA_DEL (to avoid spurious last AES operation).In case of single block encryption, configure DONEACT = GATE_TRGAES_ON_CHA
- µDMA channel B moves ciphertext[1:x] to memory when AES completes
  - ADRCHB = TXT0
  - TRGCHB = AESDONE
- START: CPU writes 0x1 to TRG.DMACHA to start CBC encryption. µDMA moves N x 16B.
- END : CPU waits for µDMA to signal 'done' and STA.STATE = IDLE, then reads result/TAG/MIC from TXT0-TXT3.

Cipher mode with CPU:

- Writes m[1] to BUF (triggers AES)
- for i = 1; i<x, increment i:
  - Prepares m[i+1]
  - Wait until STA.STATE = BUSY || use interrupt (This can be skipped since AES is immediately triggered)
  - Writes m[i+1] to BUF
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[i] from TXT
- Last m(x):
  - Set AUTOCFG.TRGAES = DISABLE
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[x] from TXT

Note

The loop can run over i=1:x, but then an additional AES encryption is triggered on the last read of TXT3. This can be aborted immediately after completing the x-th iteration of the for-loop.

20.3.3 CBC Decryption

CBC decryption is not supported.

20.3.4 CTR (Counter) Encryption/Decryption

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- AUTOCFG
  - AESSRC = BUF
  - TRGAES = RDTXT3 | WRBUF3S (the first encryption starts by writing BUF3, the successive ones by reading TXT3)
  - CTRSIZE = CTR8/CTR16/CTR32/CTR64/CTR128

Cipher mode with µDMA:

- µDMA channel A moves m[1:x] into TXTX when AES completes
  - ADRCHA = TXTX0
  - TRGCHA = AESDONE
  - DONEACT = GATE_TRGAES_ON_CHA (to avoid spurious last AES using µDMA)
- µDMA channel B moves ciphertext[1:x] to memory after channel A has written TXTX3
  - ADRCHB = TXT0
  - TRGCHB = WRTXT3
- START: SW initializes BUF with data corresponding to nonce, flags, and counter. This triggers first AES operation

- END : CPU waits for µDMA to signal 'done'

Cipher mode with CPU:

- Initializes BUF with data corresponding to nonce, flags, and counter. This triggers first AES operation
- for i=1; i<x; increment i:
  - Waits for STA.STATE = IDLE || use interrupt
  - Writes plaintext[i] to TXTX0-TXTX3
  - Reads ciphertext[i]
- Set AUTOCFG.TRGAES =DISABLE
- Waits for STA.STATE = IDLE || use interrupt
- Writes plaintext[i] to TXTX0-TXTX3
- Reads ciphertext[i]

Note

The loop can run over i=1:x, but then an additional AES operation is triggered on the last read of TXT3. This can be aborted immediately after completing the x-th iteration of the for-loop.

20.3.5 ECB (Electronic Code Book) Encryption

Assuming initialization from reset state and that CHA has written new plaintext to BUF before reading ciphertext, denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- Set AUTOCFG:
  - AESSRC = BUF
  - TRGAES = RDTXT3 | WRBUF3S

Cipher mode with µDMA:

- µDMA channel A moves m[1:x] into BUF when AES operation starts
  - ADRCHA = BUF0
  - TRGCHA = AESSTART
  - DONEACT = GATE_TRGAES_ON_CHA_DEL (to avoid spurious last AES operation). In case of single block encryption, configure DONEACT = GATE_TRGAES_ON_CHA.
- µDMA channel B moves ciphertext[1:x] to memory when AES completes.
  - ADRCHB = TXT0
  - TRGCHB = AESDONE
- START: CPU writes 0x1 to TRG.DMACHA
- END : CPU waits for µDMA 'done'

Cipher mode with CPU:

- Writes m[1] to BUF (triggers AES operation)
- for i = 1; i<x, increment i:
  - Prepares m[i+1]
  - Wait until STA.STATE = BUSY || use interrupt (This can be skipped since AES is immediately triggered)
  - Writes m[i+1] to BUF
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[i] from TXT
- Last m(x):
  - Set AUTOCFG.TRGAES = DISABLE
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[x] from TXT

Note

The loop can run over i=1:x, but then an additional AES operation is triggered on the last read of TXT3. This can be aborted immediately after completing the x-th iteration of the for-loop.

20.3.6 ECB Decryption

ECB decryption is not supported.

20.3.7 CFB (Cipher Feedback) Encryption

Below are the steps for CFB encryption with 16-byte block size.

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- SW initializes TXT with (Initialization Vector) IV
- AUTOCFG
  - AESSRC = TXT
  - TRGAES = RDTXT3 (reading TXTXBUF3 also causes trigger, see register information)
  - TRGTXT = RDTXTXBUF3

Cipher mode with µDMA:

Assumes CHA has written new plaintext to BUF before reading ciphertext:

- µDMA channel A moves m[1:x] into BUF when AES starts
  - ADRCHA = BUF0
  - TRGCHA = AESSTART
  - DONEACT = GATE_TRGAES_ON_CHA(to avoid spurious last AES using µDMA)
- µDMA channel B gets ciphertext[1:x] by reading TXTXBUF when AES completes.
  - ADRCHB = TXTXBUF0
  - TRGCHB = AESDONE
- START: CPU writes 'TXT' to TRG.OP to start first AES.
- END: CPU waits for µDMA to signal 'done'.

Cipher mode with CPU:

- Writes 'TXT' to TRG.OP to start first AES.
- for i = 1; i<x, increment i:
  - Waits until STA.STATE = BUSY || use interrupt (This can be skipped since AES is immediately triggered)
  - Writes m[i] to BUF
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[i] from TXTXBUF (TXT <= TXT XOR BUF (what was just read), triggers new encryption)
- Last m(x):
  - Set AUTOCFG.TRGAES = DISABLE
  - Waits until STA.STATE = BUSY || use interrupt (This can be skipped since AES is immediately triggered)
  - Writes m[i] to BUF
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[x] from TXTXBUF

Note

The loop can run over i=1:x, but then an additional AES encryption is triggered on the last read of TXT3. This can be aborted immediately after completing the x-th iteration of the for-loop.

20.3.8 CFB Decryption

Below are the steps for CFB decryption with 16-byte block size.

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- SW initializes TXT
- AUTOCFG
  - AESSRC = BUF (automatically triggered AES operations use the BUF content as plaintext)
  - TRGAES = RDTXT3 (reading TXTXBUF3 also causes trigger, see register information)

Cipher mode with µDMA:

Assumes CHA has written new plaintext to BUF before reading ciphertext:

- µDMA channel A moves m[1:x] into BUF when AES starts
  - ADRCHA = BUF0
  - TRGCHA = AESSTART
  - DONEACT = GATE_TRGAES_ON_CHA (to avoid spurious last AES using µDMA)
- µDMA channel B gets ciphertext[1:x] by reading TXTXBUF when AES completes
  - ADRCHB = TXTXBUF0
  - TRGCHB = AESDONE
- START: CPU write 'TXT' to TRG.AESOP to trigger first AES(K,TXT)
- END:
  - CPU waits for µDMA to signal 'done'
  - CPU optionally aborts the spurious AES by writing 0x1 to ABORT.AES

Cipher mode with CPU:

CPU implements the µDMA behavior. CPU needs to wait for STA.STATE = BUSY before CPU can update BUF with ciphertext[i].

20.3.9 OFB (Open Feedback) Encryption

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- SW initializes TXT with IV
- AUTOCFG
  - AESSRC = TXT
  - TRGAES = RDTXT3

Cipher mode with µDMA:

Assumes CHA has written new plaintext to BUF before reading ciphertext:

- µDMA channel A moves m[1:x] into BUF when AES starts
  - ADRCHA = BUF0
  - TRGCHA = AESSTART
  - DONEACT = GATE_TRGAES_ON_CHA (to avoid spurious last AES using µDMA)
- µDMA channel B gets ciphertext[1:x] by reading TXTXBUF when AES completes
  - ADRCHB = TXTXBUF0
  - TRGCHB = AESDONE
- START: SW write 'TXT' to TRG.AESOP to trigger first AES(K,TXT)
- END :
  - CPU waits for µDMA to signal 'done'
  - CPU optionally aborts the spurious AES by writing 0x1 to ABORT.AES

Cipher mode with CPU:

CPU implements the µDMA behavior. CPU needs to wait for STA.STATE = BUSY before CPU can update BUF with ciphertext[i].

20.3.10 OFB Decryption

Assuming initialization from reset state and denoting plaintext as an array, m[1:x].

The same steps are carried out as for encryption, with the exception that plaintext and ciphertext are swapped.

20.3.11 PCBC (Propagating Cipher Block Chaining) Encryption

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3
- AUTOCFG
  - AESSRC = TXTXBUF
  - TRGAES = WRBUF3
  - TRGTXT = RDTXT3
- Write IV to TXT

Cipher mode with µDMA:

- µDMA channel A moves m[1:x] into BUF on TXT3 read.
  - ADRCHA = BUF0
  - TRGCHA = RDTXT3
  - DONEACT = GATE_TRGAES_ON_CHA (to avoid spurious last AES using µDMA)
- µDMA channel B gets ciphertext[1:x] by reading TXT when AES completes.
  - ADRCHB = TXT0
  - TRGCHB = AESDONE (Completion of each burst updates TXT <= TXT XOR BUF, and triggers channel A)
- START: SW starts the process by writing 0x1 to TRG.DMACHA
- END: SW waits for µDMA to signal 'done'.

Cipher mode with CPU:

- for i = 1; i<x, increment i:
  - Write m[i] to BUF
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[i] from TXT
- Last m(x):
  - Set AUTOCFG.TRGAES = DISABLE
  - Writes m[x] to BUF
  - Waits for STA.STATE = IDLE || use interrupt
  - Reads ciphertext[x] from TXT

Note

The loop can run over i=1:x, but then an additional AES encryption is triggered on the last read of TXT3. This can be aborted immediately after completing the x-th iteration of the for-loop.

20.3.12 PCBC Decryption

PCBC decryption is not supported.

20.3.13 CTR-DRBG (Counter-Deterministic Random Bit Generator)

Assuming initialization from reset state and denoting plaintext as an array, m[1:x]:

Initialization:

- Write KEY0-KEY3

- Write BUF with data corresponding to nonce, flags, and counter.

Cipher mode with µDMA:

The following can be useful if many random numbers need to be generated and stored:

- AUTOCFG
  - CTRSIZE = CTR8/CTR16/CTR32/CTR64/CTR128
- µDMA channel A triggers blockcipher.
  - µDMA configuration: µDMA CH A shall write TRG.AESOP = BUF all the times, single transfer per arbitration cycle, R=0.
  - TRGCHA = RDTXT3
- µDMA channel B moves ciphertext[1:x]/random numbers to memory after channel A has triggered AES.
  - ADRCHB = TXT0
  - TRGCHB = AESDONE
- START: CPU writes 1 to TRG.DMACHA
- END: CPU waits for RIS.CHBDONE

Cipher mode with CPU:

The following is useful if a single or few random numbers are needed:

Initialization:

AUTOCFG

- CTRSIZE = CTR8/CTR16/CTR32/CTR64/CTR128

Operation:

- CPU writes 1 to TRG.AESOP = BUF
- CPU waits for AES to complete.
- CPU reads the result

20.3.14 CCM

CCM can be realized using 16 + 2(Nonce + Packet and Payload header) blocks of CBC-MAC to calculate authentication block and 16 + 1(Authentication Tag) blocks of CTR to perform encryption/decryption. CTR uses the same 16 blocks of plaintext as CBC-MAC.

20.4 AES Registers

Table 20-1 lists the memory-mapped registers for the AES registers. All register offset addresses not listed in Table 20-1 should be considered as reserved locations and the register contents should not be modified.

Table 20-1. AES Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register.	Section 20.4.1
10h	TRG	Trigger	Section 20.4.2
14h	ABORT	Abort	Section 20.4.3
18h	CLR	Clear	Section 20.4.4
1Ch	STA	Status	Section 20.4.5
20h	DMA	Direct Memory Access	Section 20.4.6
24h	DMACHA	DMA Channel A data transfer	Section 20.4.7
28h	DMACHB	DMA Channel B data transfer	Section 20.4.8
2Ch	AUTOCFG	Automatic Configuration	Section 20.4.9
50h	KEY0	Key Word 0	Section 20.4.10
54h	KEY1	Key Word 1	Section 20.4.11
58h	KEY2	Key Word 2	Section 20.4.12
5Ch	KEY3	Key Word 3	Section 20.4.13
70h	TXT0	Text Word 0	Section 20.4.14
74h	TXT1	Text Word 1	Section 20.4.15
78h	TXT2	Text Word 2	Section 20.4.16
7Ch	TXT3	Text Word 3	Section 20.4.17
80h	TXTX0	Text Word 0 XOR	Section 20.4.18
84h	TXTX1	Text Word 1 XOR	Section 20.4.19
88h	TXTX2	Text Word 2 XOR	Section 20.4.20
8Ch	TXTX3	Text Word 3 XOR	Section 20.4.21
90h	BUF0	Buffer Word 0	Section 20.4.22
94h	BUF1	Buffer Word 1	Section 20.4.23
98h	BUF2	Buffer Word 2	Section 20.4.24
9Ch	BUF3	Buffer Word 3	Section 20.4.25
A0h	TXTXBUF0	Text Word 0 XOR Buffer Word 0	Section 20.4.26
A4h	TXTXBUF1	Text Word 1 XOR Buffer Word 1	Section 20.4.27
A8h	TXTXBUF2	Text Word 2 XOR Buffer Word 2	Section 20.4.28
ACh	TXTXBUF3	Text Word 3 XOR Buffer Word3	Section 20.4.29
104h	IMASK	Interrupt Mask register	Section 20.4.30
108h	RIS	Raw Interrupt Status register	Section 20.4.31
10Ch	MIS	Masked Interrupt Status register	Section 20.4.32
110h	ISET	Interrupt Set register	Section 20.4.33
114h	ICLR	Interrupt Clear register	Section 20.4.34
118h	IMSET	Interrupt Mask Set register	Section 20.4.35
11Ch	IMCLR	Interrupt Mask Clear register	Section 20.4.36

Complex bit access types are encoded to fit into small table cells. Table 20-2 shows the codes that are used for access types in this section.

Table 20-2. AES Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

20.4.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 20-3.

Return to the Summary Table.

Description Register. ; This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 20-3. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6B42h	Module Identifier; This register is used to uniquely identify this IP.
15-12	STDIPOFF	R	4h	Standard IP MMR block offset ; Standard IP MMRs are the set from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist.;0x1-0xF: Standard IP MMRs begin at offset of 64*STDIPOFF from the base IP address.
11-8	INSTIDX	R	0h	IP Instance ID number ; If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15)
3-0	MINREV	R	0h	Minor Revision of IP(0-15)

20.4.2 TRG Register (Offset = 10h) [Reset = 00000000h]

TRG is shown in Table 20-4.

Return to the Summary Table.

Trigger;This register is used to manually trigger operations.

Table 20-4. TRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	DMACHA	W	0h	Manually trigger channel A request 0h = Writing 0 has no effect 1h = Triggers channel A request
2	DMACHB	W	0h	Manually trigger channel B request 0h = Writing 0 has no effect 1h = Triggers channel B request
1-0	AESOP	W	0h	AES Operation;Write an enumerated value to this field when STA.STATE = IDLE to manually trigger an AES operation. If condition is not met, the trigger is ignored. Non-enumerated values are ignored. ;Enumerated value indicates source of AES operation 1h = TXT = AES(KEY,TXT) 2h = TXT = AES(KEY,BUF) 3h = TXT = AES(KEY, TXT XOR BUF)

20.4.3 ABORT Register (Offset = 14h) [Reset = 00000000h]

ABORT is shown in Table 20-5.

Return to the Summary Table.

Abort;This register is used to abort current AES operation.

Table 20-5. ABORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ABORTAES	W	0h	Abort AES operation;Abort an ongoing AES operation. An abort will clear TXT, BUF, DMA, AUTOCFG registers 0h = Writing 0 has no effect 1h = Aborts an ongoing AES operation

20.4.4 CLR Register (Offset = 18h) [Reset = 00000000h]

CLR is shown in Table 20-6.

Return to the Summary Table.

Clear;This register is used to clear contents of TXT and BUF when STA.STATE = IDLE. If condition is not met, the contents remain unchanged.

Table 20-6. CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TXT	W	0h	Clear TXT 0h = Writing 0 has no effect 1h = Clears TXT
0	BUF	W	0h	Clear BUF 0h = Writing 0 has no effect 1h = Clears BUF

20.4.5 STA Register (Offset = 1Ch) [Reset = 00000000h]

STA is shown in Table 20-7.

Return to the Summary Table.

Status;This register provides information on AES accellerator state and BUF status.

Table 20-7. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-3	KEYINTID	R	0h	KEY Initiator ID;ID of the most recent AHB Initiator which has written into one of the KEY0 to KEY3 registers 0h = KEY was last written by CM33 3h = KEY was last written by HSM
2	KEYSTATE	R	0h	KEY State;Indicates whether data in KEY0 to KEY3 is valid or not. AES operations are not allowed until KEY is valid 0h = KEY0 to KEY3 are partially written or empty. Hence they do not have valid KEY value. ;AES operations are not allowed 1h = KEY0 to KEY3 are completely written by same AHB Initiator . Hence they have valid KEY value. ;AES operations are allowed.
1	BUFSTA	R	0h	BUF Status ;Field gives the status of BUF, indicating EMPTY or FULL, when AUTOCFG.TRGAES = WRBUF3. ;If AUTOCFG.TRGAES != WRBUF3, then STA.BUFSTA will hold the value 0.;Note : Useful for CBC-MAC 0h = Data stored in BUF is already consumed by the AES engine and next block of data can be written in BUF. 1h = Data stored in BUF is not yet consumed by the AES engine. Next block of data cannot be written into BUF until STA.STATE = IDLE.
0	STATE	R	0h	State;Field gives the state of the AES engine. 0h = AES engine is IDLE 1h = AES operation active

20.4.6 DMA Register (Offset = 20h) [Reset = 00000000h]

DMA is shown in Table 20-8.

Return to the Summary Table.

Direct Memory Access;This register controls the conditions that will generate burst requests on each DMA channel.

Table 20-8. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	DONEACT	R/W	0h	Done Action;This field determines the side effects of DMA done. It is allowed to configure this field with an OR-combination of supported enums, with the exception that GATE_TRGAES_ON_CHA and GATE_TRGAES_ON_CHA_DEL must be mutually exclusive 0h = DMA done has no side effect 1h = Triggers defined in AUTOCFG.TRGAES are gated when RIS.CHADONE = SET 2h = Delayed gating of triggers defined in AUTOCFG.TRGAES; Due to the pipelining of BUF writes, in certain modes, DMA CHA Done appears before the last but one AES operation has completed. Setting this bit, will gate the triggers defined in AUTOCFG.TRGAES only after the last write by CHA is consumed by AES FSM. Used in ECB,CBC,CBC-MAC modes (having multiple blocks encryption/ decryption) to avoid spurious AES operation triggered on last read by CHB. For single mode operation, DMA.GATE_TRGAES_ON_CHA must be used. 4h = DMA channel A done event clears TXT0 thru TXT3 if STA.STATE = IDLE. Event is ignored if condition is not met. 8h = DMA channel B done event clears TXT0 thru TXT3 if STA.STATE = IDLE. Event is ignored if condition is not met.
15-14	RESERVED	R	0h	Reserved
13-12	ADRCHB	R/W	0h	Channel B Read Write Address;The DMA accesses DMACHB to read or write contents of TXT and BUF as a response to a burst request. This field specifes the start address of the first DMA transfer that follows the burst request. The internal address gets incremented automatically for subsequent accesses. The DMA can transfer 8-bit, 16-bit, or 32-bit words, and must always complete a 16-byte transfer before re-arbitration. 0h = Start address is TXT0 1h = Start address is TXTX0 2h = Start address is BUF0 3h = Start address is TXTXBUF0
11	RESERVED	R	0h	Reserved
10-8	TRGCHB	R/W	0h	Channel B Trigger;Select the condition that triggers DMA channel B request. Non-enumerated values are not supported and ignored. 0h = DMA requests are disabled 1h = Start of AES operation triggers request 2h = Completion of AES operation triggers request 3h = Writes to TXT3, TXTX3, or TXTXBUF3 trigger request 4h = Reads of TXT3, or TXTXBUF3 trigger request
7-6	RESERVED	R	0h	Reserved
5-4	ADRCHA	R/W	0h	Channel A Read Write Address;The DMA accesses DMACHA to read or write contents of TXT and BUF as a response to a burst request. This field specifes the start address of the first DMA transfer that follows the burst request. The internal address gets incremented automatically for subsequent accesses. The DMA can transfer 8-bit, 16-bit, or 32-bit words, and must always complete a 16-byte transfer before re-arbitration. 0h = Start address is TXT0 1h = Start address is TXTX0 2h = Start address is BUF0 3h = Start address is TXTXBUF0

Table 20-8. DMA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0h	Reserved
2-0	TRGCHA	R/W	0h	Channel A Trigger;Select the condition that triggers DMA channel A request. Non-enumerated values are not supported and ignored. 0h = DMA requests are disabled 1h = Start of AES operation triggers request 2h = Completion of AES operation triggers request 3h = Writes to TXT3 or TXTX3 trigger request 4h = Reads of TXT3 or TXTXBUF3 trigger request

20.4.7 DMACHA Register (Offset = 24h) [Reset = 00000000h]

DMACHA is shown in Table 20-9.

Return to the Summary Table.

DMA Channel A data transfer;DMA accesses this register to read or write contents from sequential addresses specifed by DMA.ADRCHA.

Table 20-9. DMACHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Value transferred through DMA Channel A

20.4.8 DMACHB Register (Offset = 28h) [Reset = 00000000h]

DMACHB is shown in Table 20-10.

Return to the Summary Table.

DMA Channel B data transfer;DMA accesses this register to read or write contents from sequential addresses specifed by DMA.ADRCHB.

Table 20-10. DMACHB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Value transferred through DMA Channel B

20.4.9 AUTOCFG Register (Offset = 2Ch) [Reset = 00000000h]

AUTOCFG is shown in Table 20-11.

Return to the Summary Table.

Automatic Configuration;This register configures automatic hardware updates to TXT and BUF. Configure this register to reduce software overhead during cipher modes.

Table 20-11. AUTOCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	CHBDNCLR	R/W	0h	This field enable auto-clear of RIS.CHBDONE interrupt on read/write of TXT3/BUF3/TXTX3/TXTXBUF3 . ; 0h = Disable auto-clear of RIS.CHBDONE interrupt 1h = Enable auto-clear of RIS.CHBDONE interrupt
27	CHADNCLR	R/W	0h	This field enables auto-clear of RIS.CHADONE interrupt on read/write of TXT3/BUF3/TXTX3/TXTXBUF3 . ; 0h = Disable auto-clear of RIS.CHADONE interrupt 1h = Enable auto-clear of RIS.CHADONE interrupt
26	CLRAESST	R/W	0h	Clear AES Start;This field enables auto-clear of RIS.AESSTART interrupt on read/write of TXT3/BUF3/TXTX3/TXTXBUF3 . 0h = Disable auto-clear of RIS.AESSTART interrupt 1h = Enable auto-clear of RIS.AESSTART interrupt
25	CLRAESDN	R/W	0h	Clear AES Done ;This field enables auto-clear of RIS.AESDONE interrupt on read/write of TXT3/BUF3/TXTX3/TXTXBUF3 . ; 0h = Disable auto-clear of RIS.AESDONE interrupt 1h = Enable auto-clear of RIS.AESDONE interrupt
24	BUSHALT	R/W	0h	Bus Halt;This field decides if bus halts on access to KEY, TXT, BUF, TXTX and TXTXBUF when STA.STATE = BUSY. 0h = Disable bus halt;When STA.STATE = BUSY, writes to KEY, TXT, TXTX are ignored, reads from TXT, TXTXBUF return zero.;When STA.STATE = BUSY and if either STA.BUFSTA = FULL or AUTOCFG.CTRSIZE != DISABLE, writes to BUF are ignored, reads return zero. 1h = Enable bus halt;When STA.STATE = BUSY, access to KEY, TXT, TXTX, TXTXBUF halt the bus until STA.STATE = IDLE.;When STA.STATE = BUSY and if either STA.BUFSTA = FULL or AUTOCFG.CTRSIZE != DISABLE, access to BUF halts the bus until STA.STATE = IDLE.
23-22	RESERVED	R	0h	Reserved
21-19	CTRSIZE	R/W	0h	Counter Size;Configures size of counter as either 8,16,32,64 or 128;Non-enumerated values are not supported and ignored 0h = Disable CTR operation 1h = Configures counter size as 8-bit 2h = Configures counter size as 16-bit 3h = Configures counter size as 32-bit 4h = Configures counter size as 64-bit 5h = Configures counter size as 128-bit
18	CTRALIGN	R/W	0h	Counter Alignment;Specifies alignment of counter 0h = Indicates Left Aligned Counter;Not applicable for 128-bit counter size. ;For 128-bit counter, all octets will be considered;When left aligned,,octet 0-7 will be considered , based on counter size and endianness 1h = Indicates right aligned counter;Not applicable when counter size is 128-bit;For 128-bit counter, all octets will be considered;If right aligned, octet 8-15 will be considered based on endianness and counter size
17	CTRENDN	R/W	0h	Counter Endianness;Specifies Endianness of counter 0h = Specifies Little Endian Counter;Carry will flow from octet 'n' to octet 'n+1' 1h = Specifies Big Endian Counter;Carry will flow from octet 'n' to octet 'n-1'

Table 20-11. AUTOCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-10	RESERVED	R	0h	Reserved
9-8	TRGTXT	R/W	0h	Trigger for TXT;This field determines if and when hardware automatically XORs BUF into TXT. Non-enumerated values are not supported and ignored. It is allowed to configure this field with an OR-combination of supported enums. 0h = No hardware update of TXT 1h = Hardware XORs content of BUF into TXT upon read of TXT3 2h = Hardware XORs content of BUF into TXT upon read of TXTXBUF3
7-6	RESERVED	R	0h	Reserved
5-4	AESSRC	R/W	0h	AES Source;This field specifies the data source to hardware-triggered AES operations. Non-enumerated values are not supported and ignored. 1h = TXT = AES(KEY,TXT) 2h = TXT = AES(KEY,BUF) 3h = TXT = AES(KEY, TXT XOR BUF)
3-0	TRGAES	RH/W	0h	Trigger Electronic Codebook;This field specifies one or more actions that indirectly trigger AES operation. ;It is allowed to configure this field with an OR-combination of supported enums. 0h = No user action indirectly triggers AES operation 1h = All writes to TXT3 or TXTX3 trigger action, only when STA.STATE = IDLE 2h = All reads of TXT3 or TXTXBUF3 trigger action, only when STA.STATE = IDLE 4h = All writes to BUF3 will schedule to trigger action once STA.STATE is or becomes IDLE, only when AUTOCFG.CTRSIZE = DIS 8h = Write to BUF3 will schedule to trigger single action once STA.STATE is or becomes IDLE. Subsequent writes do not trigger action unless this setting is written again to this field.

20.4.10 KEY0 Register (Offset = 50h) [Reset = 00000000h]

KEY0 is shown in Table 20-12.

Return to the Summary Table.

Key Word 0;Write KEY0 through KEY3 to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-12. KEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value of KEY[31:0]

20.4.11 KEY1 Register (Offset = 54h) [Reset = 00000000h]

KEY1 is shown in Table 20-13.

Return to the Summary Table.

Key Word 1;Write KEY0 through KEY3 to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-13. KEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value of KEY[63:32]

20.4.12 KEY2 Register (Offset = 58h) [Reset = 00000000h]

KEY2 is shown in Table 20-14.

Return to the Summary Table.

Key Word 2;Write KEY0 through KEY3 to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-14. KEY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value of KEY[95:64]

20.4.13 KEY3 Register (Offset = 5Ch) [Reset = 00000000h]

KEY3 is shown in Table 20-15.

Return to the Summary Table.

Key Word 3;Write KEY0 through KEY3 to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-15. KEY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value of KEY[127:96]

20.4.14 TXT0 Register (Offset = 70h) [Reset = 00000000h]

TXT0 is shown in Table 20-16.

Return to the Summary Table.

Text Word 0;TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-16. TXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of TXT[31:0]

20.4.15 TXT1 Register (Offset = 74h) [Reset = 00000000h]

TXT1 is shown in Table 20-17.

Return to the Summary Table.

Text Word 1;TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-17. TXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of TXT[63:32]

20.4.16 TXT2 Register (Offset = 78h) [Reset = 00000000h]

TXT2 is shown in Table 20-18.

Return to the Summary Table.

Text Word 2;TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-18. TXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of TXT[95:64]

20.4.17 TXT3 Register (Offset = 7Ch) [Reset = 00000000h]

TXT3 is shown in Table 20-19.

Return to the Summary Table.

Text Word 3;TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-19. TXT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of TXT[127:96];AUTOCFG.TRGAES decides if a write to or a read of this field triggers an AES operation.

20.4.18 TXTX0 Register (Offset = 80h) [Reset = 00000000h]

TXTX0 is shown in Table 20-20.

Return to the Summary Table.

Text Word 0 XOR;Write data to this register to XOR data with contents in TXT0.VAL.

Table 20-20. TXTX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value in TXT0 will be TXT0.VAL = VAL XOR TXT0.VAL

20.4.19 TXTX1 Register (Offset = 84h) [Reset = 00000000h]

TXTX1 is shown in Table 20-21.

Return to the Summary Table.

Text Word 1 XOR;Write data to this register to XOR data with contents in TXT1.VAL.

Table 20-21. TXTX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value in TXT1 will be TXT1.VAL = VAL XOR TXT1.VAL

20.4.20 TXTX2 Register (Offset = 88h) [Reset = 00000000h]

TXTX2 is shown in Table 20-22.

Return to the Summary Table.

Text Word 2 XOR;Write data to this register to XOR data with contents in TXT2.VAL.

Table 20-22. TXTX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value in TXT2 will be TXT2.VAL = VAL XOR TXT2.VAL

20.4.21 TXTX3 Register (Offset = 8Ch) [Reset = 00000000h]

TXTX3 is shown in Table 20-23.

Return to the Summary Table.

Text Word 3 XOR;Write data to this register to XOR data with contents in TXT3.VAL. ;AUTOCFG.TRGAES decides if a write to or a read of this field triggers an AES operation.

Table 20-23. TXTX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Value in TXT3 will be TXT3.VAL = VAL XOR TXT3.VAL

20.4.22 BUF0 Register (Offset = 90h) [Reset = 00000000h]

BUF0 is shown in Table 20-24.

Return to the Summary Table.

Buffer Word 0;BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.

Table 20-24. BUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of BUF[31:0]

20.4.23 BUF1 Register (Offset = 94h) [Reset = 00000000h]

BUF1 is shown in Table 20-25.

Return to the Summary Table.

Buffer Word 1;BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.

Table 20-25. BUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of BUF[63:32]

20.4.24 BUF2 Register (Offset = 98h) [Reset = 00000000h]

BUF2 is shown in Table 20-26.

Return to the Summary Table.

Buffer Word 2;BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.

Table 20-26. BUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of BUF[95:64]

20.4.25 BUF3 Register (Offset = 9Ch) [Reset = 00000000h]

BUF3 is shown in Table 20-27.

Return to the Summary Table.

Buffer Word 3;BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.;AUTOCFG.TRGAES decides if a write to this field triggers an AES operation.

Table 20-27. BUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	RH/W	0h	Value of BUF[127:96]

20.4.26 TXTXBUF0 Register (Offset = A0h) [Reset = 00000000h]

TXTXBUF0 is shown in Table 20-28.

Return to the Summary Table.

Text Word 0 XOR Buffer Word 0;Read this register to obtain plaintext during CFB decryption.

Table 20-28. TXTXBUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Value read will be TXT0.VAL XOR BUF0.VAL

20.4.27 TXTXBUF1 Register (Offset = A4h) [Reset = 00000000h]

TXTXBUF1 is shown in Table 20-29.

Return to the Summary Table.

Text Word 1 XOR Buffer Word 1;Read this register to obtain plaintext during CFB decryption.

Table 20-29. TXTXBUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Value read will be TXT1.VAL XOR BUF1.VAL

20.4.28 TXTXBUF2 Register (Offset = A8h) [Reset = 00000000h]

TXTXBUF2 is shown in Table 20-30.

Return to the Summary Table.

Text Word 2 XOR Buffer Word 2;Read this register to obtain plaintext during CFB decryption.

Table 20-30. TXTXBUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Value read will be TXT2.VAL XOR BUF2.VAL

20.4.29 TXTXBUF3 Register (Offset = ACh) [Reset = 00000000h]

TXTXBUF3 is shown in Table 20-31.

Return to the Summary Table.

Text Word 3 XOR Buffer Word3;Read this register to obtain plaintext during CFB decryption.

Table 20-31. TXTXBUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Value read will be TXT3.VAL XOR BUF3.VAL

20.4.30 IMASK Register (Offset = 104h) [Reset = 00000000h]

IMASK is shown in Table 20-32.

Return to the Summary Table.

Interrupt Mask register

Table 20-32. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	R/W	0h	DMA Channel B Done interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
2	CHADONE	R/W	0h	DMA Channel A Done interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
1	AESSTART	R/W	0h	AES Start interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
0	AESDONE	R/W	0h	AES Done interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask

20.4.31 RIS Register (Offset = 108h) [Reset = 00000000h]

RIS is shown in Table 20-33.

Return to the Summary Table.

Raw Interrupt Status register

Table 20-33. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	R	0h	Raw Interrupt Status for DMA Channel B Done 0h = Interrupt did not occur 1h = Interrupt occurred
2	CHADONE	R	0h	Raw Interrupt Status for DMA Channel A Done 0h = Interrupt did not occur 1h = Interrupt occurred
1	AESSTART	R	0h	Raw Interrupt Status for AES Start 0h = Interrupt did not occur 1h = Interrupt occurred
0	AESDONE	R	0h	Raw Interrupt Status for AES Done 0h = Interrupt did not occur 1h = Interrupt occurred

20.4.32 MIS Register (Offset = 10Ch) [Reset = 00000000h]

MIS is shown in Table 20-34.

Return to the Summary Table.

Masked Interrupt Status register

Table 20-34. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	R	0h	Masked Interrupt Status for DMA Channel B Done 0h = Interrupt did not occur 1h = Interrupt occurred
2	CHADONE	R	0h	Masked Interrupt Status for DMA Channel A Done 0h = Interrupt did not occur 1h = Interrupt occurred
1	AESSTART	R	0h	Masked Interrupt Status for AES Start 0h = Interrupt did not occur 1h = Interrupt occurred
0	AESDONE	R	0h	Masked Interrupt Status for AES Done 0h = Interrupt did not occur 1h = Interrupt occurred

20.4.33 ISET Register (Offset = 110h) [Reset = 00000000h]

ISET is shown in Table 20-35.

Return to the Summary Table.

Interrupt Set register

Table 20-35. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	W	0h	Set DMA Channel B Done interrupt 0h = Writing 0 has no effect 1h = Set interrupt
2	CHADONE	W	0h	Set DMA Channel A Done interrupt 0h = Writing 0 has no effect 1h = Set interrupt
1	AESSTART	W	0h	Set AES Start interrupt 0h = Writing 0 has no effect 1h = Set interrupt
0	AESDONE	W	0h	Set AES Done interrupt 0h = Writing 0 has no effect 1h = Set interrupt

20.4.34 ICLR Register (Offset = 114h) [Reset = 00000000h]

ICLR is shown in Table 20-36.

Return to the Summary Table.

Interrupt Clear register

Table 20-36. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	W	0h	Clear DMA Channel B Done interrupt 0h = Writing 0 has no effect 1h = Clear interrupt
2	CHADONE	W	0h	Clear DMA Channel A Done interrupt 0h = Writing 0 has no effect 1h = Clear interrupt
1	AESSTART	W	0h	Clear AES Start interrupt 0h = Writing 0 has no effect 1h = Clear interrupt
0	AESDONE	W	0h	Clear AES Done interrupt 0h = Writing 0 has no effect 1h = Clear interrupt

20.4.35 IMSET Register (Offset = 118h) [Reset = 00000000h]

IMSET is shown in Table 20-37.

Return to the Summary Table.

Interrupt Mask Set register

Table 20-37. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	W	0h	Set DMA Channel B Done interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
2	CHADONE	W	0h	Set DMA Channel A Done interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
1	AESSTART	W	0h	Set AES Start interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
0	AESDONE	W	0h	Set AES Done interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask

20.4.36 IMCLR Register (Offset = 11Ch) [Reset = 00000000h]

IMCLR is shown in Table 20-38.

Return to the Summary Table.

Interrupt Mask Clear register

Table 20-38. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CHBDONE	W	0h	Clear DMA Channel B Done interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
2	CHADONE	W	0h	Clear DMA Channel A Done interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
1	AESSTART	W	0h	Clear AES Start interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
0	AESDONE	W	0h	Clear AES Done interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask

20.5 CRYPTO Registers

Table 20-39 lists the memory-mapped registers for the CRYPTO registers. All register offset addresses not listed in Table 20-39 should be considered as reserved locations and the register contents should not be modified.

Table 20-39. CRYPTO Registers

Offset	Acronym	Register Name	Section
0h	DESC	Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.	Section 20.5.1
10h	TRG	Trigger This register is used to manually trigger operations.	Section 20.5.2
14h	ABORT	Abort This register is used to abort current AES operation.	Section 20.5.3
18h	CLR	Clear This register is used to clear contents of TXT and BUF when [STA.STATE] = IDLE. If condition is not met, the contents remain unchanged.	Section 20.5.4
1Ch	STA	Status This register provides information on AES accellerator state and BUF status.	Section 20.5.5
20h	DMA	Direct Memory Access This register controls the conditions that will generate burst requests on each DMA channel.	Section 20.5.6
24h	DMACHA	DMA Channel A data transfer DMA accesses this register to read or write contents from sequential addresses specifed by [DMA.ADRCHA].	Section 20.5.7
28h	DMACHB	DMA Channel B data transfer DMA accesses this register to read or write contents from sequential addresses specifed by [DMA.ADRCHB].	Section 20.5.8
2Ch	AUTOCFG	Automatic Configuration This register configures automatic hardware updates to TXT and BUF. Configure this register to reduce software overhead during cipher modes.	Section 20.5.9
50h	KEY0	Key Word 0 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.	Section 20.5.10
54h	KEY1	Key Word 1 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.	Section 20.5.11
58h	KEY2	Key Word 2 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.	Section 20.5.12
5Ch	KEY3	Key Word 3 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.	Section 20.5.13
70h	TXT0	Text Word 0 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.	Section 20.5.14

Table 20-39. CRYPTO Registers (continued)

Offset	Acronym	Register Name	Section
74h	TXT1	Text Word 1 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.	Section 20.5.15
78h	TXT2	Text Word 2 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.	Section 20.5.16
7Ch	TXT3	Text Word 3 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.	Section 20.5.17
80h	TXTX0	Text Word 0 XOR Write data to this register to XOR data with contents in [TXT0.VAL].	Section 20.5.18
84h	TXTX1	Text Word 1 XOR Write data to this register to XOR data with contents in [TXT1.VAL].	Section 20.5.19
88h	TXTX2	Text Word 2 XOR Write data to this register to XOR data with contents in [TXT2.VAL].	Section 20.5.20
8Ch	TXTX3	Text Word 3 XOR Write data to this register to XOR data with contents in [TXT3.VAL]. [AUTOCFG.TRGAES] decides if a write to or a read of this field triggers an AES operation.	Section 20.5.21
90h	BUF0	Buffer Word 0 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.	Section 20.5.22
94h	BUF1	Buffer Word 1 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.	Section 20.5.23
98h	BUF2	Buffer Word 2 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.	Section 20.5.24
9Ch	BUF3	Buffer Word 3 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes. [AUTOCFG.TRGAES] decides if a write to this field triggers an AES operation.	Section 20.5.25
A0h	TXTXBUF0	Text Word 0 XOR Buffer Word 0 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.	Section 20.5.26
A4h	TXTXBUF1	Text Word 1 XOR Buffer Word 1 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.	Section 20.5.27
A8h	TXTXBUF2	Text Word 2 XOR Buffer Word 2 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.	Section 20.5.28
ACh	TXTXBUF3	Text Word 3 XOR Buffer Word3 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.	Section 20.5.29
104h	IMASK	Interrupt Mask register	Section 20.5.30
108h	RIS	Raw Interrupt Status register	Section 20.5.31
10Ch	MIS	Masked Interrupt Status register	Section 20.5.32
110h	ISET	Interrupt Set register	Section 20.5.33

Table 20-39. CRYPTO Registers (continued)

Offset	Acronym	Register Name	Section
114h	ICLR	Interrupt Clear register	Section 20.5.34
118h	IMSET	Interrupt Mask Set register	Section 20.5.35
11Ch	IMCLR	Interrupt Mask Clear register	Section 20.5.36

Complex bit access types are encoded to fit into small table cells. Table 20-40 shows the codes that are used for access types in this section.

Table 20-40. CRYPTO Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

20.5.1 DESC Register (Offset = 0h) [Reset = XXXX000Xh]

DESC is shown in Table 20-41.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 20-41. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	X	Module Identifier This register is used to uniquely identify this IP.
15-12	STDIPOFF	R	0h	Standard IP MMR block offset Standard IP MMRs are the set from aggregated IRQ registers till DTB. 0: Standard IP MMRs do not exist. 0x1-0xF: Standard IP MMRs begin at offset of 64*STDIPOFF from the base IP address.
11-8	INSTIDX	R	0h	IP Instance ID number If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	0h	Major revision of IP (0-15)
3-0	MINREV	R	X	Minor Revision of IP(0-15)

20.5.2 TRG Register (Offset = 10h) [Reset = 0000000Xh]

TRG is shown in Table 20-42.

Return to the Summary Table.

Trigger This register is used to manually trigger operations.

Table 20-42. TRG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	DMACHA	W	0h	Manually trigger channel A request 0h = Writing 0 has no effect 1h = Triggers channel A request
2	DMACHB	W	0h	Manually trigger channel B request 0h = Writing 0 has no effect 1h = Triggers channel B request
1-0	AESOP	W	X	AES Operation Write an enumerated value to this field when STATE = IDLE to manually trigger an AES operation. If condition is not met, the trigger is ignored. Non-enumerated values are ignored. Enumerated value indicates source of AES operation 1h = TXT = AES(KEY,TXT) 2h = TXT = AES(KEY,BUF) 3h = TXT = AES(KEY, TXT XOR BUF)

20.5.3 ABORT Register (Offset = 14h) [Reset = 0000000Xh]

ABORT is shown in Table 20-43.

Return to the Summary Table.

Abort This register is used to abort current AES operation.

Table 20-43. ABORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	ABORTAES	W	X	Abort AES operation Abort an ongoing AES operation. An abort will clear TXT, BUF, DMA, AUTOCFG registers 0h = Writing 0 has no effect 1h = Aborts an ongoing AES operation

20.5.4 CLR Register (Offset = 18h) [Reset = 0000000Xh]

CLR is shown in Table 20-44.

Return to the Summary Table.

Clear This register is used to clear contents of TXT and BUF when STATE = IDLE. If condition is not met, the contents remain unchanged.

Table 20-44. CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	TXT	W	0h	Clear TXT 0h = Writing 0 has no effect 1h = Clears TXT
0	BUF	W	X	Clear BUF 0h = Writing 0 has no effect 1h = Clears BUF

20.5.5 STA Register (Offset = 1Ch) [Reset = 0000000Xh]

STA is shown in Table 20-45.

Return to the Summary Table.

Status This register provides information on AES accellerator state and BUF status.

Table 20-45. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-3	KEYINTID	R	0h	KEY Initiator ID ID of the most recent AHB Initiator which has written into one of the KEY0 to KEY3 registers 0h = KEY was last written by CM33 1h = KEY was last written by HSM
2	KEYSTATE	R	0h	KEY State Indicates whether data in KEY0 to KEY3 is valid or not. AES operations are not allowed until KEY is valid 0h = KEY0 to KEY3 are partially written or empty. Hence they do not have valid KEY value. AES operations are not allowed 1h = KEY0 to KEY3 are completely written by same AHB Initiator . Hence they have valid KEY value. AES operations are allowed.
1	BUFSTA	R	0h	BUF Status Field gives the status of BUF, indicating EMPTY or FULL, when TRGAES = WRBUF3. If TRGAES != WRBUF3, then BUFSTA will hold the value 0. Note : Useful for CBC-MAC 0h = Data stored in BUF is already consumed by the AES engine and next block of data can be written in BUF. 1h = Data stored in BUF is not yet consumed by the AES engine. Next block of data cannot be written into BUF until STATE = IDLE.
0	STATE	R	X	State Field gives the state of the AES engine. 0h = AES engine is IDLE 1h = AES operation active

20.5.6 DMA Register (Offset = 20h) [Reset = 0000000Xh]

DMA is shown in Table 20-46.

Return to the Summary Table.

Direct Memory Access This register controls the conditions that will generate burst requests on each DMA channel.

Table 20-46. DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	
19-16	DONEACT	R/W	0h	Done Action This field determines the side effects of DMA done. It is allowed to configure this field with an OR-combination of supported enums, with the exception that GATE_TRGAES_ON_CHA and GATE_TRGAES_ON_CHA_DEL must be mutually exclusive 0h = DMA done has no side effect 1h = Triggers defined in TRGAES are gated when CHADONE = SET 2h = Delayed gating of triggers defined in TRGAES Due to the pipelining of BUF writes, in certain modes, DMA CHA Done appears before the last but one AES operation has completed. Setting this bit, will gate the triggers defined in TRGAES only after the last write by CHA is consumed by AES FSM. Used in ECB,CBC,CBC-MAC modes (having multiple blocks encryption/decryption) to avoid spurious AES operation triggered on last read by CHB. For single mode operation, DMA.GATE_TRGAES_ON_CHA must be used. 4h = DMA channel A done event clears [TXT0.*] thru [TXT3.*] if STATE = IDLE. Event is ignored if condition is not met. 8h = DMA channel B done event clears [TXT0.*] thru [TXT3.*] if STATE = IDLE. Event is ignored if condition is not met.
15-14	RESERVED	R	0h	
13-12	ADRCHB	R/W	0h	Channel B Read Write Address The DMA accesses [DMACHB.*] to read or write contents of TXT and BUF as a response to a burst request. This field specifes the start address of the first DMA transfer that follows the burst request. The internal address gets incremented automatically for subsequent accesses. The DMA can transfer 8-bit, 16-bit, or 32-bit words, and must always complete a 16-byte transfer before re-arbitration. INTERNAL_NOTE: Upon each channel B request, the internal address counter gets re-initialized to 0. 0h = Start address is [TXT0.*] 1h = Start address is [TXTX0.*] 2h = Start address is [BUF0.*] 3h = Start address is [TXTXBUF0.*]
11	RESERVED	R	0h	
10-8	TRGCHB	R/W	0h	Channel B Trigger Select the condition that triggers DMA channel B request. Non-enumerated values are not supported and ignored. 0h = DMA requests are disabled 1h = Start of AES operation triggers request 2h = Completion of AES operation triggers request 3h = Writes to [TXT3.*], [TXTX3.*], or [TXTXBUF3.*] trigger request INTERNAL_NOTE: Useful for CFB encryption. 4h = Reads of [TXT3.*], or [TXTXBUF3.*] trigger request INTERNAL_NOTE: Useful for PCBC encryption.
7-6	RESERVED	R	0h	

Table 20-46. DMA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	ADRCHA	R/W	0h	Channel A Read Write Address The DMA accesses [DMACHA.*] to read or write contents of TXT and BUF as a response to a burst request. This field specifes the start address of the first DMA transfer that follows the burst request. The internal address gets incremented automatically for subsequent accesses. The DMA can transfer 8-bit, 16-bit, or 32-bit words, and must always complete a 16-byte transfer before re-arbitration. INTERNAL_NOTE: Upon each channel A request, the internal address counter gets re-initialized to 0. 0h = Start address is [TXT0.*] 1h = Start address is [TXTX0.*] 2h = Start address is [BUF0.*] 3h = Start address is [TXTXBUF0.*]
3	RESERVED	R	0h	
2-0	TRGCHA	R/W	X	Channel A Trigger Select the condition that triggers DMA channel A request. Non-enumerated values are not supported and ignored. 0h = DMA requests are disabled 1h = Start of AES operation triggers request 2h = Completion of AES operation triggers request 3h = Writes to [TXT3.*] or [TXTX3.*] trigger request INTERNAL_NOTE: Useful for CFB encryption. 4h = Reads of [TXT3.*] or [TXTXBUF3.*] trigger request INTERNAL_NOTE: Useful for PCBC encryption.

20.5.7 DMACHA Register (Offset = 24h) [Reset = 0000000Xh]

DMACHA is shown in Table 20-47.

Return to the Summary Table.

DMA Channel A data transfer DMA accesses this register to read or write contents from sequential addresses specifed by ADRCHA.

Table 20-47. DMACHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value transferred through DMA Channel A

20.5.8 DMACHB Register (Offset = 28h) [Reset = 0000000Xh]

DMACHB is shown in Table 20-48.

Return to the Summary Table.

DMA Channel B data transfer DMA accesses this register to read or write contents from sequential addresses specifed by ADRCHB.

Table 20-48. DMACHB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value transferred through DMA Channel B

20.5.9 AUTOCFG Register (Offset = 2Ch) [Reset = XXXX000Xh]

AUTOCFG is shown in Table 20-49.

Return to the Summary Table.

Automatic Configuration This register configures automatic hardware updates to TXT and BUF. Configure this register to reduce software overhead during cipher modes.

Table 20-49. AUTOCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	CHBDNCLR	R/W	X	This field enable auto-clear of CHBDONE interrupt on read/write of [TXT3.*]/[BUF3.*]/[TXTX3.*]/[TXTXBUF3.*] . INTERNAL_NOTE: If conditions for setting and clearing of interrupts occur at the same time, interrupt set will take priority over clear. 0h = Disable auto-clear of CHBDONE interrupt 1h = Enable auto-clear of CHBDONE interrupt
27	CHADNCLR	R/W	X	This field enables auto-clear of CHADONE interrupt on read/write of [TXT3.*]/[BUF3.*]/[TXTX3.*]/[TXTXBUF3.*] . INTERNAL_NOTE: If conditions for setting and clearing of interrupts occur at the same time, interrupt set will take priority over clear. 0h = Disable auto-clear of CHADONE interrupt 1h = Enable auto-clear of CHADONE interrupt
26	CLRAESST	R/W	X	Clear AES Start This field enables auto-clear of AESSTART interrupt on read/write of [TXT3.*]/[BUF3.*]/[TXTX3.*]/[TXTXBUF3.*] . INTERNAL_NOTE: If conditions for setting and clearing of interrupts occur at the same time, interrupt set will take priority over clear. 0h = Disable auto-clear of AESSTART interrupt 1h = Enable auto-clear of AESSTART interrupt
25	CLRAESDN	R/W	X	Clear AES Done This field enables auto-clear of AESDONE interrupt on read/write of [TXT3.*]/[BUF3.*]/[TXTX3.*]/[TXTXBUF3.*] . INTERNAL_NOTE: If conditions for setting and clearing of interrupts occur at the same time, interrupt set will take priority over clear. 0h = Disable auto-clear of AESDONE interrupt 1h = Enable auto-clear of AESDONE interrupt
24	BUSHALT	R/W	0h	Bus Halt This field decides if bus halts on access to KEY, TXT, BUF, TXTX and TXTXBUF when STATE = BUSY. 0h = Disable bus halt When STATE = BUSY, writes to KEY, TXT, TXTX are ignored, reads from TXT, TXTXBUF return zero. When STATE = BUSY and if either BUFSTA = FULL or CTRSIZE != DISABLE, writes to BUF are ignored, reads return zero. 1h = Enable bus halt When STATE = BUSY, access to KEY, TXT, TXTX, TXTXBUF halt the bus until STATE = IDLE. When STATE = BUSY and if either BUFSTA = FULL or CTRSIZE != DISABLE, access to BUF halts the bus until STATE = IDLE.
23-22	RESERVED	R	0h	
21-19	CTRSIZE	R/W	X	Counter Size Configures size of counter as either 8,16,32,64 or 128 Non-enumerated values are not supported and ignored 0h = Disable CTR operation 1h = Configures counter size as 8-bit 2h = Configures counter size as 16-bit 3h = Configures counter size as 32-bit 4h = Configures counter size as 64-bit 5h = Configures counter size as 128-bit
18	CTRALIGN	R/W	X	Counter Alignment Specifies alignment of counter 0h = Indicates Left Aligned Counter Not applicable for 128-bit counter size. For 128-bit counter, all octets will be considered When left aligned,,octet 0-7 will be considered , based on counter size and endianness 1h = Indicates right aligned counter Not applicable when counter size is 128-bit For 128-bit counter, all octets will be considered If right aligned, octet 8-15 will be considered based on endianness and counter size

Table 20-49. AUTOCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CTRENDN	R/W	0h	Counter Endianness Specifies Endianness of counter 0h = Specifies Little Endian Counter Carry will flow from octet 'n' to octet 'n+1' 1h = Specifies Big Endian Counter Carry will flow from octet 'n' to octet 'n-1'
16-10	RESERVED	R	0h	
9-8	TRGTXT	R/W	0h	Trigger for TXT This field determines if and when hardware automatically XORs BUF into TXT. Non-enumerated values are not supported and ignored. It is allowed to configure this field with an OR-combination of supported enums. 0h = No hardware update of TXT 1h = Hardware XORs content of BUF into TXT upon read of [TXT3.*] 2h = Hardware XORs content of BUF into TXT upon read of [TXTXBUF3.*]
7-6	RESERVED	R	0h	
5-4	AESSRC	R/W	0h	AES Source This field specifies the data source to hardware-triggered AES operations. Non-enumerated values are not supported and ignored. INTERNAL_NOTE: Forward AES-128 with field set to BUF or TXTXBUF will need an additional clock cycle to complete. There is room for one more data input if later identified. 1h = TXT = AES(KEY,TXT) 2h = TXT = AES(KEY,BUF) 3h = TXT = AES(KEY, TXT XOR BUF)
3-0	TRGAES	R/W	X	Trigger Electronic Codebook This field specifies one or more actions that indirectly trigger AES operation. It is allowed to configure this field with an OR-combination of supported enums. 0h = No user action indirectly triggers AES operation 1h = All writes to [TXT3.*] or [TXTX3.*] trigger action, only when STATE = IDLE 2h = All reads of [TXT3.*] or [TXTXBUF3.*] trigger action, only when STATE = IDLE 4h = All writes to [BUF3.*] will schedule to trigger action once STATE is or becomes IDLE, only when CTRSIZE = DIS INTERNAL_NOTE: Useful in CBC-MAC 8h = Write to [BUF3.*] will schedule to trigger single action once STATE is or becomes IDLE. Subsequent writes do not trigger action unless this setting is written again to this field. INTERNAL_NOTE: Useful in CBC, CTR, and CFB encryption.

20.5.10 KEY0 Register (Offset = 50h) [Reset = 0000000Xh]

KEY0 is shown in Table 20-50.

Return to the Summary Table.

Key Word 0 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-50. KEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value of KEY[31:0]

20.5.11 KEY1 Register (Offset = 54h) [Reset = 0000000Xh]

KEY1 is shown in Table 20-51.

Return to the Summary Table.

Key Word 1 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-51. KEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value of KEY[63:32]

20.5.12 KEY2 Register (Offset = 58h) [Reset = 0000000Xh]

KEY2 is shown in Table 20-52.

Return to the Summary Table.

Key Word 2 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-52. KEY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value of KEY[95:64]

20.5.13 KEY3 Register (Offset = 5Ch) [Reset = 0000000Xh]

KEY3 is shown in Table 20-53.

Return to the Summary Table.

Key Word 3 Write [KEY0.*] through [KEY3.*] to populate the 128-bit key. The key is not consumed by the hardware. It is hence not required to reload the key for subsequent block encryptions/decryptions unless required by the application.

Table 20-53. KEY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value of KEY[127:96]

20.5.14 TXT0 Register (Offset = 70h) [Reset = 0000000Xh]

TXT0 is shown in Table 20-54.

Return to the Summary Table.

Text Word 0 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-54. TXT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of TXT[31:0]

20.5.15 TXT1 Register (Offset = 74h) [Reset = 0000000Xh]

TXT1 is shown in Table 20-55.

Return to the Summary Table.

Text Word 1 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-55. TXT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of TXT[63:32]

20.5.16 TXT2 Register (Offset = 78h) [Reset = 0000000Xh]

TXT2 is shown in Table 20-56.

Return to the Summary Table.

Text Word 2 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-56. TXT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of TXT[95:64]

20.5.17 TXT3 Register (Offset = 7Ch) [Reset = 0000000Xh]

TXT3 is shown in Table 20-57.

Return to the Summary Table.

Text Word 3 TXT is the 128-bit buffer, the AES-128 algorithm performs its operations on. AES input can be written to TXT, and ciphertext can be read from TXT.

Table 20-57. TXT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of TXT[127:96] TRGAES decides if a write to or a read of this field triggers an AES operation.

20.5.18 TXTX0 Register (Offset = 80h) [Reset = 0000000Xh]

TXTX0 is shown in Table 20-58.

Return to the Summary Table.

Text Word 0 XOR Write data to this register to XOR data with contents in VAL.

Table 20-58. TXTX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value in TXT0 will be VAL = VAL XOR VAL

20.5.19 TXTX1 Register (Offset = 84h) [Reset = 0000000Xh]

TXTX1 is shown in Table 20-59.

Return to the Summary Table.

Text Word 1 XOR Write data to this register to XOR data with contents in VAL.

Table 20-59. TXTX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value in TXT1 will be VAL = VAL XOR VAL

20.5.20 TXTX2 Register (Offset = 88h) [Reset = 0000000Xh]

TXTX2 is shown in Table 20-60.

Return to the Summary Table.

Text Word 2 XOR Write data to this register to XOR data with contents in VAL.

Table 20-60. TXTX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value in TXT2 will be VAL = VAL XOR VAL

20.5.21 TXTX3 Register (Offset = 8Ch) [Reset = 0000000Xh]

TXTX3 is shown in Table 20-61.

Return to the Summary Table.

Text Word 3 XOR Write data to this register to XOR data with contents in VAL. TRGAES decides if a write to or a read of this field triggers an AES operation.

Table 20-61. TXTX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	X	Value in TXT3 will be VAL = VAL XOR VAL

20.5.22 BUF0 Register (Offset = 90h) [Reset = 0000000Xh]

BUF0 is shown in Table 20-62.

Return to the Summary Table.

Buffer Word 0 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.

Table 20-62. BUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of BUF[31:0]

20.5.23 BUF1 Register (Offset = 94h) [Reset = 0000000Xh]

BUF1 is shown in Table 20-63.

Return to the Summary Table.

Buffer Word 1 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.

Table 20-63. BUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of BUF[63:32]

20.5.24 BUF2 Register (Offset = 98h) [Reset = 0000000Xh]

BUF2 is shown in Table 20-64.

Return to the Summary Table.

Buffer Word 2 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes.

Table 20-64. BUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of BUF[95:64]

20.5.25 BUF3 Register (Offset = 9Ch) [Reset = 0000000Xh]

BUF3 is shown in Table 20-65.

Return to the Summary Table.

Buffer Word 3 BUF is a 128-bit auxiliary register that functions as a buffer, counter, or storage of operations in cipher modes. TRGAES decides if a write to this field triggers an AES operation.

Table 20-65. BUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	X	Value of BUF[127:96]

20.5.26 TXTXBUF0 Register (Offset = A0h) [Reset = 0000000Xh]

TXTXBUF0 is shown in Table 20-66.

Return to the Summary Table.

Text Word 0 XOR Buffer Word 0 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.

Table 20-66. TXTXBUF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	X	Value read will be VAL XOR VAL

20.5.27 TXTXBUF1 Register (Offset = A4h) [Reset = 0000000Xh]

TXTXBUF1 is shown in Table 20-67.

Return to the Summary Table.

Text Word 1 XOR Buffer Word 1 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.

Table 20-67. TXTXBUF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	X	Value read will be VAL XOR VAL

20.5.28 TXTXBUF2 Register (Offset = A8h) [Reset = 0000000Xh]

TXTXBUF2 is shown in Table 20-68.

Return to the Summary Table.

Text Word 2 XOR Buffer Word 2 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.

Table 20-68. TXTXBUF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	X	Value read will be VAL XOR VAL

20.5.29 TXTXBUF3 Register (Offset = ACh) [Reset = 0000000Xh]

TXTXBUF3 is shown in Table 20-69.

Return to the Summary Table.

Text Word 3 XOR Buffer Word3 Read this register to obtain plaintext during CFB decryption. INTERNAL_NOTE: The xor+mux implementatation already, add to readback mux.

Table 20-69. TXTXBUF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	X	Value read will be VAL XOR VAL

20.5.30 IMASK Register (Offset = 104h) [Reset = 0000000Xh]

IMASK is shown in Table 20-70.

Return to the Summary Table.

Interrupt Mask register

Table 20-70. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	R/W	0h	DMA Channel B Done interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
2	CHADONE	R/W	0h	DMA Channel A Done interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
1	AESSTART	R/W	0h	AES Start interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
0	AESDONE	R/W	X	AES Done interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask

20.5.31 RIS Register (Offset = 108h) [Reset = 0000000Xh]

RIS is shown in Table 20-71.

Return to the Summary Table.

Raw Interrupt Status register

Table 20-71. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	R	0h	Raw Interrupt Status for DMA Channel B Done 0h = Interrupt did not occur 1h = Interrupt occurred
2	CHADONE	R	0h	Raw Interrupt Status for DMA Channel A Done 0h = Interrupt did not occur 1h = Interrupt occurred
1	AESSTART	R	0h	Raw Interrupt Status for AES Start 0h = Interrupt did not occur 1h = Interrupt occurred
0	AESDONE	R	X	Raw Interrupt Status for AES Done 0h = Interrupt did not occur 1h = Interrupt occurred

20.5.32 MIS Register (Offset = 10Ch) [Reset = 0000000Xh]

MIS is shown in Table 20-72.

Return to the Summary Table.

Masked Interrupt Status register

Table 20-72. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	R	0h	Masked Interrupt Status for DMA Channel B Done 0h = Interrupt did not occur 1h = Interrupt occurred
2	CHADONE	R	0h	Masked Interrupt Status for DMA Channel A Done 0h = Interrupt did not occur 1h = Interrupt occurred
1	AESSTART	R	0h	Masked Interrupt Status for AES Start 0h = Interrupt did not occur 1h = Interrupt occurred
0	AESDONE	R	X	Masked Interrupt Status for AES Done 0h = Interrupt did not occur 1h = Interrupt occurred

20.5.33 ISET Register (Offset = 110h) [Reset = 0000000Xh]

ISET is shown in Table 20-73.

Return to the Summary Table.

Interrupt Set register

Table 20-73. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	W	0h	Set DMA Channel B Done interrupt 0h = Writing 0 has no effect 1h = Set interrupt
2	CHADONE	W	0h	Set DMA Channel A Done interrupt 0h = Writing 0 has no effect 1h = Set interrupt
1	AESSTART	W	0h	Set AES Start interrupt 0h = Writing 0 has no effect 1h = Set interrupt
0	AESDONE	W	X	Set AES Done interrupt 0h = Writing 0 has no effect 1h = Set interrupt

20.5.34 ICLR Register (Offset = 114h) [Reset = 0000000Xh]

ICLR is shown in Table 20-74.

Return to the Summary Table.

Interrupt Clear register

Table 20-74. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	W	0h	Clear DMA Channel B Done interrupt 0h = Writing 0 has no effect 1h = Clear interrupt
2	CHADONE	W	0h	Clear DMA Channel A Done interrupt 0h = Writing 0 has no effect 1h = Clear interrupt
1	AESSTART	W	0h	Clear AES Start interrupt 0h = Writing 0 has no effect 1h = Clear interrupt
0	AESDONE	W	X	Clear AES Done interrupt 0h = Writing 0 has no effect 1h = Clear interrupt

20.5.35 IMSET Register (Offset = 118h) [Reset = 0000000Xh]

IMSET is shown in Table 20-75.

Return to the Summary Table.

Interrupt Mask Set register

Table 20-75. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	W	0h	Set DMA Channel B Done interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
2	CHADONE	W	0h	Set DMA Channel A Done interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
1	AESSTART	W	0h	Set AES Start interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask
0	AESDONE	W	X	Set AES Done interrupt mask 0h = Writing 0 has no effect 1h = Set interrupt mask

20.5.36 IMCLR Register (Offset = 11Ch) [Reset = 0000000Xh]

IMCLR is shown in Table 20-76.

Return to the Summary Table.

Interrupt Mask Clear register

Table 20-76. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CHBDONE	W	0h	Clear DMA Channel B Done interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
2	CHADONE	W	0h	Clear DMA Channel A Done interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
1	AESSTART	W	0h	Clear AES Start interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
0	AESDONE	W	X	Clear AES Done interrupt mask 0h = Writing 0 has no effect 1h = Clear interrupt mask

Chapter 21

Analog to Digital Converter (ADC)

This chapter describes the functionality of the Analog to Digital Converter (ADC) module.

21.1 Overview

The purpose of the ADC is to measure analog signals and convert them to a digital representation with minimal CPU intervention providing for lower power and greater task integration.

The ADC supports fast 12-, 10-, and 8-bit analog-to-digital conversions. The ADC implements a 12-bit Successive Approximation Register (SAR) core, sample/conversion mode control, and up to 4 independent conversion-and-control buffers. This means the ADC allows up to 4 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

ADC features include:

- 1-Msps conversion rate at a resolution of 12 bits when reference is external or supply (VDDS)
- 200-ksps sampling rate with internal reference
- Full scale ADC operating voltage range
- 12-bit max resolution with support for 10-bit and 8-bit lower resolution modes
- Sample-and-hold with programmable sampling periods controlled by software or timers
- Two sampling trigger sources: software trigger and event trigger
- Software-selectable on-chip reference voltage of 1.4V or 2.5V
- Configurable ADC reference source: VDDS, internal reference (VREF), or external reference (VREF+/-)
- Up to 16 individually configurable analog input channels
- Internal conversion channels for temperature sensing, supply monitoring, and analog signal chain (see device-specific data sheet for availability and channel mapping)
- Configurable ADC clock source
- Different conversion modes: Single-channel, repeat-single-channel, sequence, repeat-sequence, and software requested ad-hoc single conversion modes
- Four 16-bit conversion-result storage registers (MEMRES0:3)
- Support for FIFO and non-FIFO modes for CPU and µDMA
- Data compaction within FIFO for 32-bit reads
- Window comparator with provision to configure low and high threshold values for low-power monitoring of input signals from conversion-result registers
- µDMA support with interrupt event generation on completion of transfer
- Automatic and manual power down schemes
- Unsigned binary and two's complement data format
- 10-bit sample timer with two independent sample time compare registers
- Sample time compare value selection in each memory control register
- Provision to enable window comparator in each memory control register
- Auto-next or trigger-next configuration for sequence or repeated sequence of channels operation
- Different event sources with single event output
- µDMA trigger logic and interface to work with µDMA

Figure 21-1 shows the functional block diagram of the ADC peripheral.

21.2 Block Diagram

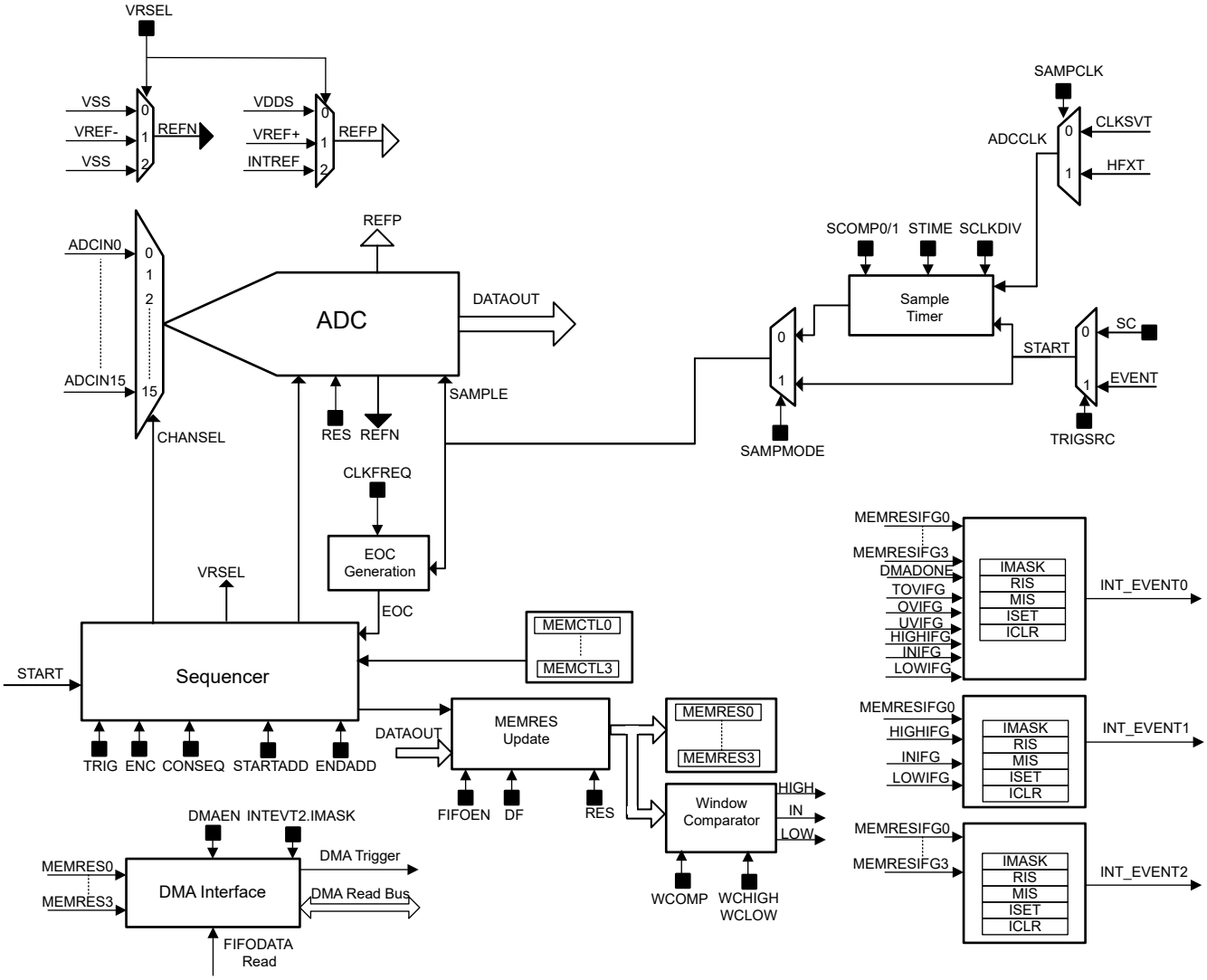


Figure 21-1. ADC Block Diagram

21.3 Functional Description

The ADC is configured with user software. The following sections describe the setup and operation of the ADC.

21.3.1 ADC Core

The ADC core converts an analog input to a digital representation. The core uses two voltage levels (V_{R+} and V_{R-}) to define the upper and lower limits of the conversion. The digital output (N_{ADC}) is full scale when the input signal is equal to or higher than V_{R+}, and is zero when the input signal is equal to or lower than V_{R-}. The input channel and the positive reference voltage level (V_{R+}) are defined in the conversion-control memory.

Equation 2 shows the conversion formula for the ADC result, N_{ADC}, for n-bit resolution mode

$$N_{ADC} = \left(2^n - 1\right) \times \frac{(V_{in} + 0.5LSB) - V_{R-}}{V_{R+} - V_{R-}} \qquad Where\ LSB = \frac{V_{R+} - V_{R-}}{2^n} \tag{2}$$

Given that V_{R-} is 0 V in this ADC, the equation for N_{ADC} becomes:

$$N_{ADC} = \left(2^n - 1\right) \times \frac{V_{in} + 0.5LSB}{V_{R+}}, \qquad Where\ LSB = \frac{V_{R+}}{2^n} \tag{3}$$

Equation 4 describes the input voltage at which the ADC output saturates:

$$V_{in} = V_{R+} - 1.5LSB \tag{4}$$

Note

The ADC is not functional in STANDBY or SHUTDOWN modes.

21.3.2 Voltage Reference Options

The ADC voltage reference (V_{R+}) can be configured through the VRSEL bits in the MEMCTL register. Different reference sources can be selected for conversion on different channels. There are three options available for supplying a reference voltage to the ADC:

1. External reference supplied to the ADC through the VREF+/- pins
2. Supply voltage (VDDS)
3. Configurable internal reference voltage of 1.4V and 2.5V (VREF)

When supplying an external reference to the ADC, the VREF+ pin is connected to the reference source with the appropriate decoupling circuitry and the VREF- pin is connected to ground.

21.3.3 Resolution Modes

The ADC supports operation in 12-bit (default), 10-bit, and 8-bit resolution modes. The resolution mode is configured using the ADC.CTL2[2:1] RES bit field.

- When 12-bit mode is selected, the conversion phase requires a total of 14 conversion clock cycles
- When 10-bit mode is selected, the conversion phase requires a total of 12 conversion clock cycles
- When 8-bit mode is selected, the conversion phase requires a total of 9 conversion clock cycles

The conversion window is based on the resolution mode and the frequency of ADCCLK. For more details, refer to Figure 21-2 and Figure 21-3.

21.3.4 ADC Clocking

The ADC peripheral clock (ADCCLK) is provided by CKMD and is used for the sampling clock (SAMPCLK). CLKSVT and HFXT are the clock sources available for ADCCLK, which can support up to 48 MHz. Refer to the device-specific data sheet for supported ADCCLK frequencies. Using CLKSVT, which is the bus clock for all peripherals, is very useful for deterministic start of sampling and simultaneous sampling. Using the HFXT as the clock source for ADCCLK is useful for when a very accurate, low-jitter, sampling period is needed. The ADC clock source can be selected by writing the CKMD.ADCCLKSEL[1:0] SRC bit field. The conversion clock is sourced from the selected ADCCLK within the digital hardware.

21.3.5 Power Down Behavior

To save power, disable the ADC when not in use. The PWRDN bit in the CTL0 register selects the ADC power down policy between AUTO and MANUAL.

Configure PWRDN based on the max ADC sampling rate required and the operational needs in different power modes.

The reset value of PWRDN is ‘0’ which has the default behavior of automatic power down of the ADC peripheral at the end of a conversion and when the next sample signal is not required to be asserted immediately. When the PWRDN bit is set to ‘1’ the bit selects manual power down behavior. In this setting, the ADC is not powered down at the end of a conversion and remains enabled.

Refer to the device-specific data sheet for specifications on the ADC wakeup/enable time.

21.3.6 Sampling Trigger Sources and Sampling Modes

Sample Triggers

There are two sampling trigger sources available which can be selected through the TRIGSRC bit in the CTL1 register; one is a software trigger and the other is an event trigger.

When the software trigger is selected as the source, the application software can set the Start Conversion (SC) bit in the CTL1 register to initiate the sample phase. When the event trigger is selected as the source, a rising edge on the selected event from the event manager initiates the sample phase. An event is always edge triggered.

Sampling Modes

There are two sampling modes available, AUTO and MANUAL, which are selected through the SAMPMODE bit in the CTL1 register.

21.3.6.1 AUTO Sampling Mode

In AUTO mode, the sample signal is generated synchronous to the sampling clock (SAMPCLK) and can be programmed using an internal sampling timer to determine the duration of the sampling window. The sample timer is 10-bit wide and there are two sample time compare registers (SCOMPx) available to account for various source impedances to measure signals from. One of these two SCOMP registers can be selected using the STIME bit in the MEMCTL register.

Figure 21-2 shows the ADC sample and conversion timing diagram when the ADC is configured in AUTO sampling mode.

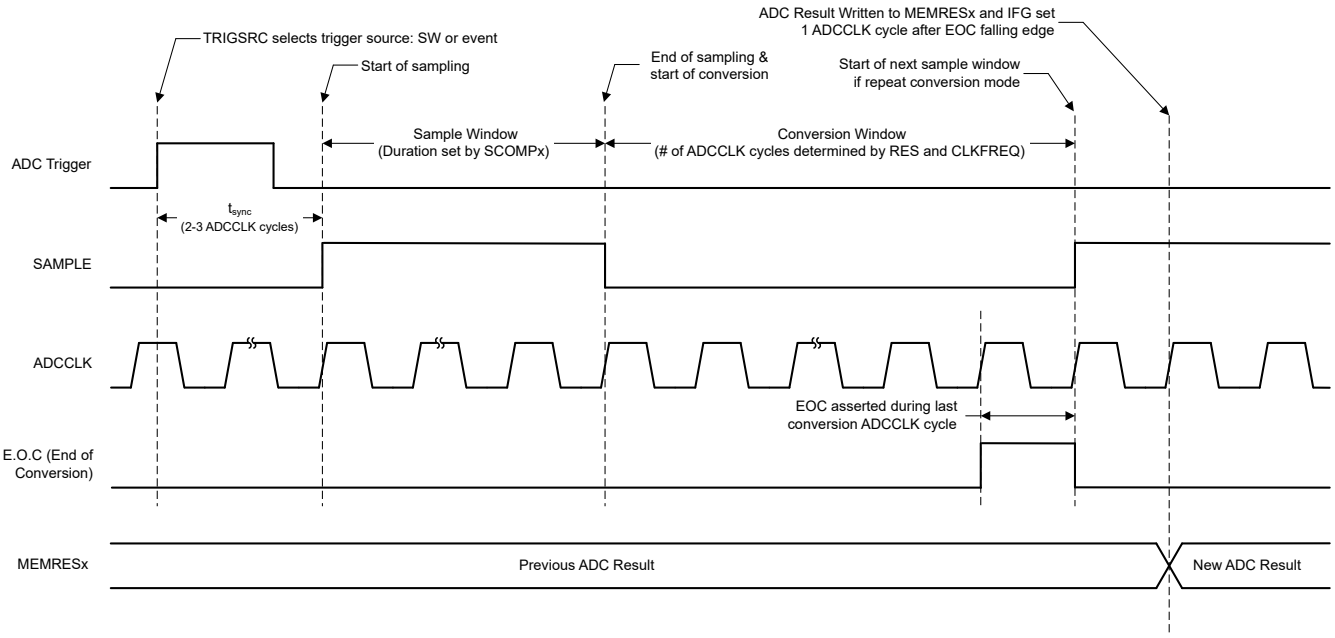


Figure 21-2. AUTO Sampling Mode - ADC Sample and Conversion Timing Diagram

Note

When the reset value of PWRDN is set as ‘0’, which has the default behavior of automatic power down, ADC wake-up time needs to be considered in each sample window. Refer to the device-specific data sheet for specifications on the ADC wake-up time. For example, if the maximum ADC wake-up time is 5 µs, then the duration set by SCOMPx is > (5 µS + Duration for sample window).

21.3.6.2 MANUAL Sampling Mode

In MANUAL mode, the sample signal is generated when the SC bit is set which can be asynchronous to the sampling clock. The duration of the sampling window is controlled by software by holding the SC bit high.

Because an event is always edge triggered, manual mode with event trigger is not supported for any of the conversion modes. Software trigger with manual sampling mode is supported only for single channel single conversion mode and is not supported for any of the other three conversion modes.

There is a 2-3 cycle synchronization latency from when the sample window ends to when the conversion window begins.

Figure 21-3 shows the ADC sample and conversion timing diagram when the ADC is configured in MANUAL sampling mode:

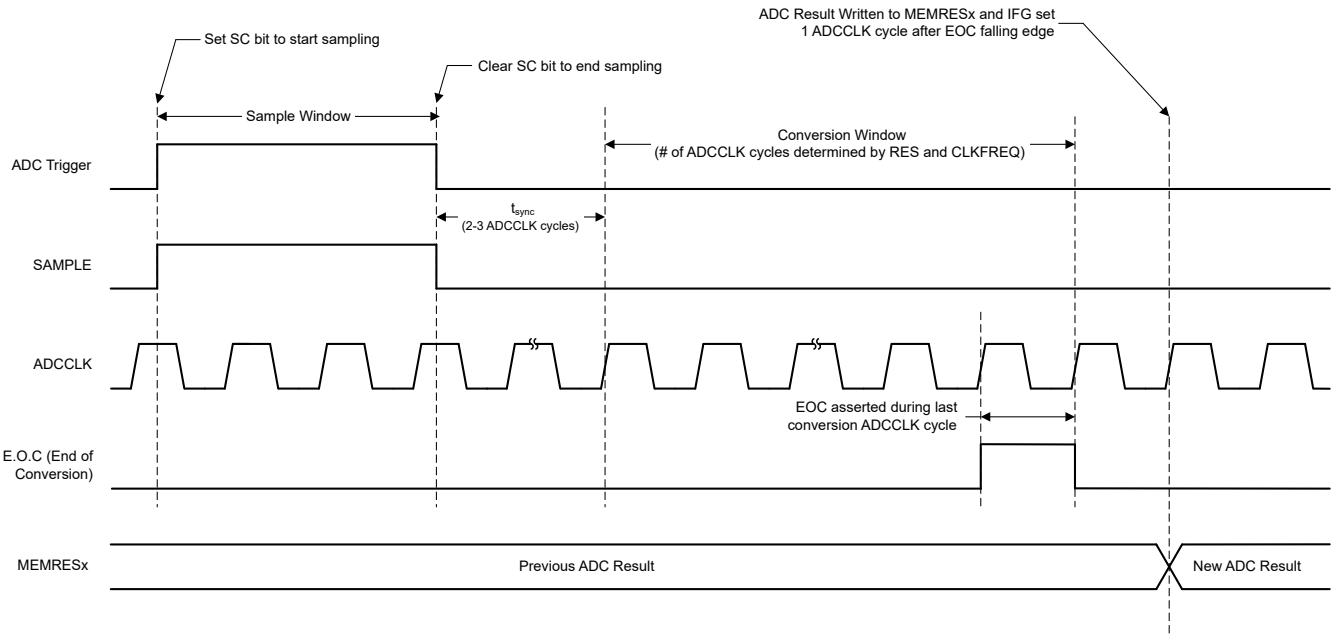


Figure 21-3. MANUAL Sampling Mode - ADC Sample and Conversion Timing Diagram

Note

When the reset value of PWRDN is set as '0' which has the default behavior of automatic power down, ADC wake-up time needs to be considered before sample window. Refer to the device-specific data sheet for specifications on the ADC wake-up time.

21.3.7 Sampling Period

The sampling clock source is selected in the CKMD module using the SRC bits in the ADCCLKSEL register.

The desired sampling period for ADC operation can be generated using the internal clock divider and/or the sample timer, which applies to AUTO sampling mode. The internal clock divider is configured using the SCLKDIV bits in the CTL0 register and has divide options of 1, 2, 4, 8, 16, 24, 32, and 48.

The duration of the sampling period can be programmed to one of two user-defined values set by the SCOMP0 and SCOMP1 sample timer registers. The value in SCOMPx configures the sampling period by defining the number of sample time clocks to set the sample window to. The default SCOMPx sample timer value translates to 1 cycle wide sample pulse which allows the sampling period to be solely based on the sample clock and SCLKDIV. In general, there are three parameters that can be used to control the sample period: SCOMPx, SCLKDIV, and the source of the sample clock.

When AUTO power down mode is selected using PWRDN=0, the module enable signal to the ADC peripheral is generated one sampling clock cycle after the sample signal is asserted. This should be considered by the user in the sample window calculation in addition to the ADC power time or settling time needs of other analog modules such as the Temperature Sensor, VREF, etc.

21.3.8 Conversion Modes

There are four conversion modes available in the ADC:

1. Single channel single conversion
   - The channel can be selected using MEMCTL
   - The selected channel is sampled and converted only once
2. Repeat single channel conversion
   - The channel can be selected using MEMCTL
   - The selected channel is repeatedly sampled and converted until ENC is cleared by software
3. Sequence of channels conversion
   - Groups of channels can be formed using STARTADD, ENDADD, and MEMCTL registers
   - Each of the channels in the group is sampled and converted only once
   - The sequence completes even if ENC is cleared in the middle of the sequence
4. Repeat sequence of channels conversion
   - Groups of channels can be formed using STARTADD, ENDADD, and MEMCTL registers
   - The group of channels are sampled and converted repeatedly until ENC is cleared by software
   - When ENC is cleared the operation stops at the end of the ongoing sequence

The following steps outline the recommended process for configuring the ADC for a desired conversion mode:

1. Use the CONSEQ bits in the CTL1 register to select the desired ADC conversion mode
2. Use the STARTADD bits in the CTL2 register to select which MEMCTLx is used for single conversion or as first MEMCTL for a sequence mode
3. If using a sequence mode, use the ENDADD bits in the CTL2 register to select which MEMCTLx is used for the last conversion of the sequence
4. Assign an ADC input channel to the appropriate MEMCTLx register using the CHANSEL bits
   - For sequence modes, ADC input channel must be assigned for each MEMCTLx that is part of the configured sequence
5. Select EVENT or SOFTWARE trigger using the TRIGSRC bit in the CTL1 register
6. Select AUTO or MANUAL sampling mode using the SAMPMODE bit in the CTL1 register
   - If using AUTO mode, program the desired sample timer value in the SCOMPx register and use the STIME bits in the MEMCTLx register to select the appropriate sample timer source (SCOMP0 or SCOMP1)
7. If using repeat single channel or sequence conversion modes, program the TRIG bit in each MEMCTLx register to indicate if a trigger is needed to step to the next MEMCTL in the sequence
8. Set the ENC bit in the CTL1 register to enable ADC conversions
9. Table 21-1 depicts the next step of ADC configuration and usage based on the selected trigger and sampling modes:

Table 21-1. Trigger and Sample Mode ADC Usage Matrix

	Software Trigger	Event Trigger
AUTO Sampling Mode	• Set SC bit to start the sample phase (duration determined by sample timer) • Conversion starts once sample phase is over • In single channel single conversion, ENC is cleared when conversion is over • SC bit is automatically cleared once the trigger is captured For repeat and sequence modes, if TRIG is set in MEMCTL, the SC bit needs to be set for the next conversion to proceed.	• EVENT trigger starts the sample phase (duration determined by sample timer) • Conversion starts once sample phase is over • In single channel single conversion, ENC is cleared when conversion is over For repeat and sequence modes, ADC waits for EVENT trigger or automatically starts the next conversion based on TRIG setting.
MANUAL Sampling Mode	• Set SC bit to start the sample phase (SC bit is not automatically reset) • Clear the SC bit to end the sample phase and start the conversion • In single channel single conversion, ENC bit is cleared when conversion is over Repeated/sequential conversion modes are NOT supported in this configuration.	ADC operation is NOT supported in this configuration

10. The ADC results are stored in the MEMRES register of the associated MEMCTL (for example, the MEMCTL0 result is stored in MEMRES0)
    - For repeat conversion modes, the result in MEMRES is updated after every associated MEMCTL conversion
11. For repeated conversion modes, clear the ENC bit to stop ADC operation

Note

In case a hardware event is being used as the sample trigger source, software must ensure that the event trigger is disabled first before clearing the ENC bit to stop ADC operations.

21.3.9 ADC Data Format

The ADC supports two data formats – unsigned binary and 2's complement signed binary. Unsigned binary results are stored right-justified in the MEMRES register or FIFO. Signed binary results are stored left justified in the MEMRES register or FIFO.

Table 21-2. ADC Data Formats

Data Format	Resolution	Result Range (decimal)	Result Range (hex)
Unsigned	8-bit	0 to 255	0000h to 00FFh
	10-bit	0 to 1023	0000h to 03FFh
	12-bit	0 to 4095	0000h to 0FFFh
Signed	8-bit	-128 to 127	8000h to 7F00h
	10-bit	-512 to 511	8000h to 7FC0h
	12-bit	-2048 to 2047	8000h to 7FF0h

21.3.10 Status Register

The ADC status register, STA, contains two bits – ASCACT and BUSY.

- BUSY equaling '1' indicates that the ADC is busy performing a sample or conversion operation
  - For **single channel single conversion**, BUSY signals that a trigger has been received and sample or conversion is ongoing. BUSY is cleared when the conversion completes

- For **repeat single conversion**, BUSY signals that repeat single operation has begun and has not ended. BUSY is cleared when ENC is written '0' and the last conversion completes
- For **sequence of channels conversion**, BUSY signals that the sequence of channels conversion has started. BUSY is cleared at the end of the sequence
- For **repeat sequence of channels conversion**, BUSY signals the repeat sequence is ongoing. BUSY is cleared when ENC is written '0' and the last conversion in the sequence completes

Note

In case of an ADC start of conversion issued by software through the SC bit, software has to wait for at least 9 CLKSVT clock cycles if polling for the BUSY status bit in the program code. This is to account for internal clock synchronization latencies before the ADC status bit is updated.

21.3.11 ADC Events

The ADC peripheral contains three event publishers and one event subscriber.

One event publisher (INT_EVENT0) manages ADC interrupt requests (IRQs) to the CPU subsystem through a static event route. The second event publisher (INT_EVENT1) can be used to publish ADC events to a subscriber through a generic event route channel. The third event publisher (INT_EVENT2) can be used as an ADC to µDMA trigger to send ADC events directly to the µDMA

The event subscriber can be used to subscribe to events which are published to the event fabric through a generic event route channel.

The ADC events are summarized in Table 21-3.

Table 21-3. ADC Events

Event	Type	Source	Destination	Configuration	Functionality
CPU interrupt event	Publisher	ADC	CPU Subsystem	INT_EVENT0 registers	Fixed interrupt route from ADC to CPU
Generic publisher event	Publisher	ADC	Generic event channel	INT_EVENT1 registers	Trigger generic event channel from ADC
µDMA trigger event	Publisher	ADC	µDMA	INT_EVENT2 registers	Fixed trigger route from ADC to µDMA
Generic subscriber event	Subscriber	Other peripherals	ADC	EVTSVT.ADCTRGSEL	ADC subscription to generic event within EVTSVT

21.3.11.1 CPU Interrupt Event Publisher (INT_EVENT0)

The ADC peripheral provides many interrupt sources which can be configured to source a CPU interrupt event. The CPU interrupt events from the ADC are given in Table 21-4.

Table 21-4. ADC CPU Interrupt Event Conditions (INT_EVENT0)

RIS (Bit Index)	Name	Description
0x0	OVIFG	Conversion overflow interrupt flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
0x1	TOVIFG	Sequence conversion time overflow interrupt flag is set when the ADC receives a new sampling trigger while the previous sample+conversion is still in progress
0x2	HIGHIFG	High threshold compare interrupt flag is set when the MEMRESx result register is higher than the WCHIGH threshold of the window comparator
0x3	LOWIFG	Low threshold compare interrupt flag is set when the MEMRESx result register is lower than the WCLOW threshold of the window comparator
0x4	INIFG	In-range comparator interrupt flag is set when the MEMRESx result register is within the range of WCLOW and WCHIGH of the window comparator
0x5	DMADONE	µDMA done interrupt flag is set when the DMA data transfer of programmed block size is completed
0x6	UVIFG	Conversion underflow interrupt flag, the UVIFG flag is set when the CPU or DMA reads the MEMRESx register before the next conversion result is available

Table 21-4. ADC CPU Interrupt Event Conditions (INT_EVENT0) (continued)

RIS (Bit Index)	Name	Description
0x7	ASC	Ad-hoc single conversion done
0x8 to 0xB	MEMRESIFG[0 to 3]	Memory register interrupt flag is set when MEMRESx is loaded with a new conversion result

The CPU interrupt event configuration is managed with the INT_EVENT0 event management registers. Interrupt (RIS) flags are cleared upon software writing to the respective ICLR register bits.

21.3.11.2 Generic Event Publisher (INT_EVENT1)

The ADC peripheral provides 4 interrupt sources, one of which can be configured to publish an event as a generic ADC event. Table 21-5 lists these interrupt sources.

Table 21-5. ADC Generic Event Publisher Conditions (INT_EVENT1)

Index	Name	Description
0x2	HIGHIFG	High threshold compare interrupt flag is set when the MEMRESx result register is higher than the WCHIGH threshold of the window comparator
0x3	LOWIFG	Low threshold compare interrupt flag is set when the MEMRESx result register is lower than the WCLOW threshold of the window comparator
0x4	INIFG	In-range comparator interrupt flag is set when the MEMRESx result register is within the range of WCLOW and WCHIGH of the window comparator
0x8	MEMRESIFG0	Memory register interrupt flag is set when MEMRES0 is loaded with a new conversion result

The generic event publisher configuration is managed with the INT_EVENT1 event management registers.

21.3.11.3 DMA Trigger Event Publisher (INT_EVENT2)

The ADC module provides many interrupt sources which can be configured to source the DMA trigger. In order of decreasing interrupt priority, the DMA trigger events from the ADC are given in Table 21-6. When the DMA channel is needed by the ADC, the DMA trigger is unmasked in the IMASK register of INT_EVENT2 and the DMA is configured as needed to support the ADC operation.

Table 21-6. ADC DMA Trigger Event Conditions (INT_EVENT2)

RIS Index	Name	Description
0x8 to 0xB	MEMRESIFG[0 to 3]	Memory register interrupt flag is set when MEMRESx is loaded with a new conversion result

The DMA trigger event configuration is managed with the INT_EVENT2 event management registers. The interrupt (RIS) flags are cleared based on ACK from DMA.

21.3.11.4 Generic Event Subscriber

The ADC peripheral supports receiving events routed through a generic channel from other peripherals via the EVTSVT.ADCTRGSEL register.

21.4 Advanced Features

The following sections describe the additional features and benefits provided with the ADC peripheral and how to leverage them in an application.

21.4.1 Window Comparator

There is one window comparator unit available in the ADC which can be used to check if the input signal is within predefined threshold values set by software. The ADC result that goes into MEMRES or FIFO is what gets checked against the threshold values of the window comparator.

Based on the comparison the window comparator can generate 3 interrupt conditions:

1. LOWIFG– Conversion result is below the Low threshold (WCLOW)

2. HIGHIFG– Conversion result is above the High threshold (WCHIGH)
3. INIFG– Conversion result is in between or equal to the Low and High thresholds

The window comparator low and high threshold values are global for all channels and the window comparison feature can be enabled for each channel as needed using the WINCOMP bit in the MEMCTL register.

When the ADC result data format (CTL2.DF) or resolution (CTL2.RES) configuration is changed, the window comparator threshold values are not reset by hardware and are retained as is. The software application is expected to reconfigure the threshold values as appropriate after changing the data format and/or resolution configuration.

21.4.2 DMA & FIFO Operation

The ADC has a dedicated interface for communicating with the µDMA. This interface is useful to offload work from the CPU by using the µDMA to store ADC results to memory automatically.

The DMAEN bit in the CTL2 register is used to enable the µDMA for ADC data transfer. The DMAEN bit is cleared by ADC hardware when the µDMA “DONE" status signal is asserted. Software is expected to re-enable the µDMA using DMAEN to arm the ADC to generate the next µDMA trigger.

The ADC also incorporates an optional First-In-First-Out buffer to provide a way for ADC results to be stored for future use, such as transferring to memory by the µDMA. Either the CPU or the µDMA can be used to move data from the ADC regardless of whether the FIFO is enabled or disabled. The memory result flags in the RIS register of the third event publisher serve as the FIFO threshold and can be unmasked to generate the µDMA trigger.

The following sections explain the details of using the ADC with µDMA or CPU in various conversion modes and with the FIFO enabled or disabled.

21.4.2.1 DMA/CPU Operation in Non-FIFO Mode (FIFOEN=0)

- Single Conversion and Repeat Single Conversion
  - Configure STARTADD bits to select the desired MEMCTLx register
    - MEMCTLx **is correlated to** MEMRESx
    - MEMRESx **is correlated to** MEMRESIFGx
  - Configure MEMCTL CHANSEL bits to select the desired ADC channel
  - Conversion data is available in MEMRESx
  - MEMRESIFGx can be set to generate a CPU interrupt or the DMA trigger
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
  - The conversion underflow flag is set when the CPU or DMA reads the MEMRESx register before the next conversion result is available
- Sequence Conversion and Repeat Sequence Conversion
  - Configure STARTADD bits to select the first MEMCTL in the sequence
  - Configure ENDADD bits to select the last MEMCTL in the sequence
    - MEMCTLx **is correlated to** MEMRESIFGx
  - Configure each MEMCTLx CHANSEL bits to select the desired ADC channels
  - Conversion data is available in MEMRESx
  - MEMRESIFGx can be set to generate a CPU interrupt or the DMA trigger
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
  - The conversion underflow flag is set when the CPU or DMA reads the MEMRESx register before the next conversion result is available

Note

For DMA based operation, the MEMCTL start address should be smaller than the end address for single sequence conversion as DMA source does not roll back. Repeat sequence conversion mode does not support DMA based data transfer because the DMA does not support circular addressing mode.

21.4.2.2 DMA/CPU Operation in FIFO Mode (FIFOEN=1)

- Single Conversion and Repeat Single Conversion
  - Configure STARTADD bits to select the desired MEMCTLx register
    - MEMCTLx **is NOT correlated to** MEMRESx
    - MEMRESx **is correlated to** MEMRESIFGx
  - Configure MEMCTL CHANSEL bits to select the desired ADC channel
  - Conversion data is loaded sequentially into MEMRES0,1,2,….N (organized as a FIFO)
  - The CPU or DMA must read ADC samples from the dedicated FIFODATA register and not from MEMRES registers directly
    - Data in the FIFO is always compacted with two samples and provided as 32-bit data upon a FIFODATA read by CPU or DMA
  - MEMRESIFGx can be used as a threshold condition to generate a CPU interrupt or DMA trigger
    - For full use of the FIFO, the last MEMRESIFG can be used
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA
  - The conversion underflow flag is set when the CPU or DMA reads the FIFODATA register before the conversion result is available in the MEMRESx registers

Note

Single conversion mode with FIFO enabled is not recommended for CPU or DMA based operation. This leads to underflow condition and unwanted 16-bit data has to be discarded by software.

- Sequence Conversion and Repeat Sequence Conversion
  - Configure STARTADD bits to select the first MEMCTL in the sequence
  - Configure ENDADD bits to select the last MEMCTL in the sequence
    - MEMCTLx **is NOT correlated to** MEMRESx
    - MEMRESx **is correlated to** MEMRESIFGx
  - Configure each MEMCTLx CHANSEL bits to select the desired ADC channels
  - Conversion data is loaded sequentially into MEMRES0,1,2,….N (organized as a FIFO)
  - The CPU or DMA must read ADC samples from the dedicated FIFODATA register and not from MEMRES registers directly
    - Data in the FIFO is always compacted with two samples and provided as 32-bit data upon a FIFODATA read by CPU or DMA
  - MEMRESIFGx can be used as a threshold condition to generate a CPU interrupt or DMA trigger
    - For full use of the FIFO, the last MEMRESIFG can be used
  - The conversion overflow flag is set when the ADC updates MEMRESx before the previous sample is read by the CPU or DMA

21.4.2.3 DMA/CPU Operation Summary Matrix

Table 21-7. DMA/CPU Operation Summary Matrix

Conversion Mode	FIFO Disabled (FIFOEN=0) Samples not compacted. Read from MEMRESx registers directly		FIFO Enabled (FIFOEN=1) Samples always compacted Read from FIFODAT register only	
	CPU Read/Write	DMA Read/Write	CPU Read/Write	DMA Read/Write
Single	Supported	Supported	Not recommended Underflow flag is set Ignore unwanted 16 bits	Not recommended Underflow flag is set Ignore unwanted 16 bits
Repeat Single	Supported	Supported	Supported MEMRESIFG=CPU interrupt FIFODATA read in 32 bits	Supported MEMRESIFG=DMA trigger FIFODATA read in 32 bits

Table 21-7. DMA/CPU Operation Summary Matrix (continued)

Conversion Mode	FIFO Disabled (FIFOEN=0) Samples not compacted. Read from MEMRESx registers directly		FIFO Enabled (FIFOEN=1) Samples always compacted Read from FIFODAT register only	
	CPU Read/Write	DMA Read/Write	CPU Read/Write	DMA Read/Write
Sequence	Supported	Supported	Supported MEMRESIFG=CPU interrupt FIFODATA read in 32 bits	Supported MEMRESIFG=DMA trigger FIFODATA read in 32 bits
Repeat Sequence	Supported	Not Supported	Supported MEMRESIFG=CPU interrupt FIFODATA read in 32 bits	Supported MEMRESIFG=DMA trigger FIFODATA read in 32 bits

21.4.3 Ad-hoc Single Conversion

A mechanism to allow ADC to perform ad-hoc single conversions (ASC) without affecting the scheduled conversions is provided. The ADC sequencer slots the ASC request at a time when it finds an idle window in the middle of scheduled conversions without affecting the timing integrity of the scheduled conversions.

This is requested via CTL3 register which has fields for specifying the ADC channel number, voltage reference option and sample period for conversion. Any write to this register is treated as ad-hoc single conversion request by the sequencer. There is a separate result register available to store the data for ad-hoc single conversion (ASCRES). This is a dedicated register for ad-hoc single conversion operation which is different than result registers/FIFO available to store results from conversion on sensor channels.

Once software writes into ASC configuration register for ad-hoc single conversion there is a status bit that indicates the ASC is active (ASCACT) and goes low once the ASC operation is completed.

When the ASC operation is completed, an interrupt flag ASC done (ASCDONE) is set that can be unmasked by software to read the ASC result in the interrupt service routine.

Software can write into ASC configuration register at any time in ad-hoc manner and that request is registered by the sequencer and serviced at a suitable time.

Figure 21-4 shows the ADC sequencer state-machine for ASC operation

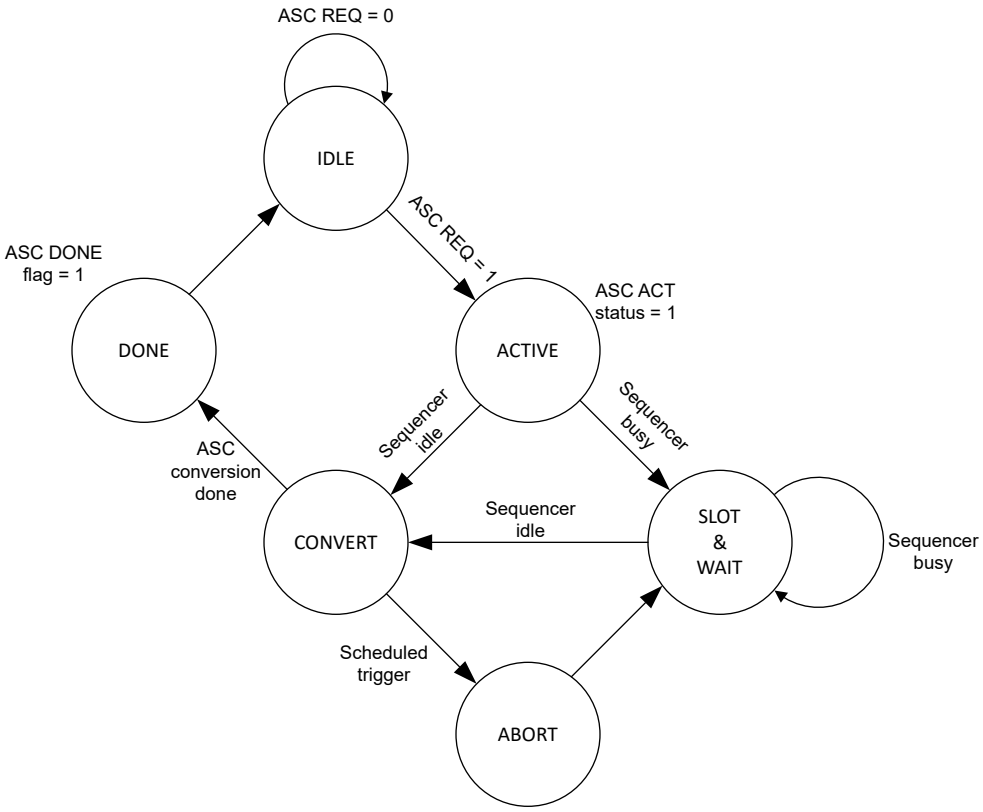


Figure 21-4. ADC Sequencer State-Machine for ASC Operation

Repeat Single Channel Mode and ASC Request

- When the sequencer operates in repeat single channel with sample trigger policy as auto-next, then the selected sensor channel is converted back to back continuously and the ASC request is pended by the sequencer and it is taken up and serviced only when the software stops repeat single channel conversion. When the sample trigger policy is trigger-next, then upon ASC request, the sequencer tries to schedule the ASC operation at the end of ongoing conversion (EOC - End of Conversion).
- It starts ASC operation and will complete it successfully if the scheduled trigger on sensor channel does not arrive in between.
- If the scheduled trigger is received in the middle of ASC operation, then ASC conversion is aborted immediately and scheduled conversion is performed.
- If sequencer is not successful in completing ASC operation in the middle of scheduled conversions, then it will be serviced only when the software stops repeat single channel conversion.

Sequence of Channels mode and ASC Request

- In the case of sequence of channels operation with sample trigger policy as auto-next for all channels in the sequence, the ASC request will be slotted at the end of sequence and completed.
- If the sample trigger policy is trigger-next for one or more channels in the sequence, then sequencer tries to schedule the ASC operation at EOC of channel with trigger next policy set.
- If it can't complete ASC conversion successfully due to arrival of scheduled trigger then ASC operation is taken up and completed at the end after conversion of all channels in the sequence are completed.

Repeat Sequence of Channels Mode and ASC Request

- In the case of repeat sequence of channels operation with sample trigger policy as auto-next for all channels in the sequence, the ASC request will be slotted and completed when repeat sequence operation is stopped by software.

- If the sample trigger policy is trigger-next for one or more channels in the sequence, then sequencer tries to schedule the ASC operation at EOC of channel with trigger next policy set.
- If it can't complete ASC conversion successfully due to arrival of scheduled trigger then ASC operation is taken up and completed when the repeat sequence operation is stopped by software.

ASC Operation Abort Due to Scheduled Trigger

- When the scheduled trigger arrives during the sample phase of ASC operation then the sequencer pulls the sample signal low immediately and applies reset to ADC SAR logic and then generates sample trigger for the scheduled conversion.
- When the scheduled trigger arrives during the conversion phase of ASC operation then sequencer applies reset to ADC SAR logic and then generates sample trigger for the scheduled conversion.
- When the ASC operation gets aborted due to arrival of scheduled trigger, the sequencer attempts to perform ASC operation automatically at the next earliest idle slot without software requiring to re-issue ASC request.
- ASC request is not pipelined which means software has to issue ASC request only when ASC active status is low.
- If ASC request is raised while previous ASC operation is not completed then that ASC request is ignored and software has to reissue ASC request when ASC active is low.

21.5 ADC Registers

Table 21-8 lists the memory-mapped registers for the ADC registers. All register offset addresses not listed in Table 21-8 should be considered as reserved locations and the register contents should not be modified.

Table 21-8. ADC Registers

Offset	Acronym	Register Name	Section
28h	IMASK0	Interrupt mask	Section 21.5.1
30h	RIS0	Raw interrupt status	Section 21.5.2
38h	MIS0	Masked interrupt status	Section 21.5.3
40h	ISET0	Interrupt set	Section 21.5.4
48h	ICLR0	Interrupt clear	Section 21.5.5
58h	IMASK1	Interrupt mask	Section 21.5.6
60h	RIS1	Raw interrupt status	Section 21.5.7
68h	MIS1	Masked interrupt status	Section 21.5.8
70h	ISET1	Interrupt set	Section 21.5.9
78h	ICLR1	Interrupt clear	Section 21.5.10
88h	IMASK2	Interrupt mask	Section 21.5.11
90h	RIS2	Raw interrupt status	Section 21.5.12
98h	MIS2	Masked interrupt status	Section 21.5.13
A0h	ISET2	Interrupt set	Section 21.5.14
A8h	ICLR2	Interrupt clear	Section 21.5.15
100h	CTL0	Control Register 0	Section 21.5.16
104h	CTL1	Control Register 1	Section 21.5.17
108h	CTL2	Control Register 2	Section 21.5.18
10Ch	CTL3	Control Register 3	Section 21.5.19
114h	SCOMP0	Sample Time Compare 0 Register	Section 21.5.20
118h	SCOMP1	Sample Time Compare 1 Register	Section 21.5.21
11Ch	REFCFG	Reference Buffer Configuration Register	Section 21.5.22
148h	WCLOW	Window Comparator Low Threshold Register	Section 21.5.23
150h	WCHIGH	Window Comparator High Threshold Register	Section 21.5.24
160h	FIFODATA	FIFO Data Register	Section 21.5.25
170h	ASCRES	ASC Result Register	Section 21.5.26
180h	MEMCTL0	Conversion Memory Control Register 0	Section 21.5.27
184h	MEMCTL1	Conversion Memory Control Register 1	Section 21.5.28
188h	MEMCTL2	Conversion Memory Control Register 2	Section 21.5.29
18Ch	MEMCTL3	Conversion Memory Control Register 3	Section 21.5.30
280h	MEMRES0	Memory Result Register 0	Section 21.5.31
284h	MEMRES1	Memory Result Register 1	Section 21.5.32
288h	MEMRES2	Memory Result Register 2	Section 21.5.33
28Ch	MEMRES3	Memory Result Register 3	Section 21.5.34
340h	STA	Status Register	Section 21.5.35
E00h	TEST0	Internal. Only to be used through TI provided API.	Section 21.5.36
E08h	TEST2	Internal. Only to be used through TI provided API.	Section 21.5.37
E0Ch	TEST3	Internal. Only to be used through TI provided API.	Section 21.5.38
E10h	TEST4	Internal. Only to be used through TI provided API.	Section 21.5.39
E14h	TEST5	Internal. Only to be used through TI provided API.	Section 21.5.40
E18h	TEST6	Internal. Only to be used through TI provided API.	Section 21.5.41

Table 21-8. ADC Registers (continued)

Offset	Acronym	Register Name	Section
E20h	DEBUG1	Internal. Only to be used through TI provided API.	Section 21.5.42
E24h	DEBUG2	Internal. Only to be used through TI provided API.	Section 21.5.43
E28h	DEBUG3	Internal. Only to be used through TI provided API.	Section 21.5.44
E2Ch	DEBUG4	Internal. Only to be used through TI provided API.	Section 21.5.45

Complex bit access types are encoded to fit into small table cells. Table 21-9 shows the codes that are used for access types in this section.

Table 21-9. ADC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

21.5.1 IMASK0 Register (Offset = 28h) [Reset = 00000000h]

IMASK0 is shown in Table 21-10.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS0 to MIS0 when the corresponding bit-fields are set to 1.

Table 21-10. IMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	R/W	0h	MEMRES3 conversion result interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
10	MEMRESIFG2	R/W	0h	MEMRES2 conversion result interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
9	MEMRESIFG1	R/W	0h	MEMRES1 conversion result interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
8	MEMRESIFG0	R/W	0h	MEMRES0 conversion result interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
7	ASCDONE	R/W	0h	Mask for ASC done raw interrupt flag. 0h = Disable interrupt mask 1h = Enable interrupt mask
6	UVIFG	R/W	0h	Conversion underflow interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
5	DMADONE	R/W	0h	DMA done interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
4	INIFG	R/W	0h	In-range comparator interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
3	LOWIFG	R/W	0h	Low threshold compare interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
2	HIGHIFG	R/W	0h	High threshold compare interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
1	TOVIFG	R/W	0h	Sequence conversion time overflow interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask
0	OVIFG	R/W	0h	Conversion overflow interrupt mask. 0h = Disable interrupt mask 1h = Enable interrupt mask

21.5.2 RIS0 Register (Offset = 30h) [Reset = 00000000h]

RIS0 is shown in Table 21-11.

Return to the Summary Table.

Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR0 register bit.

Table 21-11. RIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	R	0h	Raw interrupt status for MEMRES3.;This bit is set to 1 when MEMRES3 is loaded with a new;conversion result.;Reading MEMRES3 register will clear this bit, or when the;corresponding bit in ICLR0 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Raw interrupt status for MEMRES2.;This bit is set to 1 when MEMRES2 is loaded with a new;conversion result.;Reading MEMRES2 register will clear this bit, or when the;corresponding bit in ICLR0 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Raw interrupt status for MEMRES1.;This bit is set to 1 when MEMRES1 is loaded with a new;conversion result.;Reading MEMRES1 register will clear this bit, or when the;corresponding bit in ICLR0 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0.;This bit is set to 1 when MEMRES0 is loaded with a new;conversion result.;Reading MEMRES0 register will clear this bit, or when the;corresponding bit in ICLR0 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7	ASCDONE	R	0h	Raw interrupt flag for ASC done. 0h = Interrupt is not pending. 1h = Interrupt is pending.
6	UVIFG	R	0h	Raw interrupt flag for MEMRESx underflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	R	0h	Raw interrupt flag for DMADONE. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	R	0h	Raw interrupt status for In-range comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	R	0h	Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	R	0h	Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	R	0h	Raw interrupt flag for sequence conversion trigger overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.

Table 21-11. RIS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OVIFG	R	0h	Raw interrupt flag for MEMRESx overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.

21.5.3 MIS0 Register (Offset = 38h) [Reset = 00000000h]

MIS0 is shown in Table 21-12.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of IMASK and RIS registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 21-12. MIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	R	0h	Masked interrupt status for MEMRES3. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Masked interrupt status for MEMRES2. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Masked interrupt status for MEMRES1. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Masked interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7	ASCDONE	R	0h	Masked interrupt status for ASC done. 0h = Interrupt is not pending. 1h = Interrupt is pending.
6	UVIFG	R	0h	Masked interrupt flag for MEMRESx underflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	R	0h	Masked interrupt flag for DMADONE. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	R	0h	Mask INIFG in MIS0 register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	R	0h	Masked interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	R	0h	Masked interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	R	0h	Masked interrupt flag for sequence conversion timeout overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
0	OVIFG	R	0h	Masked interrupt flag for MEMRESx overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.

21.5.4 ISET0 Register (Offset = 40h) [Reset = 00000000h]

ISET0 is shown in Table 21-13.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 21-13. ISET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	W	0h	Set interrupt status for MEMRES3. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Set interrupt status for MEMRES2. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Set interrupt status for MEMRES1. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Set Interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7	ASCDONE	W	0h	Set interrupt for ASC done. 0h = Interrupt is not pending. 1h = Interrupt is pending.
6	UVIFG	W	0h	Set interrupt for MEMRESx underflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	W	0h	Set interrupt for DMADONE. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	W	0h	Set INIFG interrupt register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	W	0h	Set interrupt for MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	W	0h	Set Interrupt for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	W	0h	Set interrupt for sequence conversion timeout overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
0	OVIFG	W	0h	Set Interrupt for MEMRESx overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.

21.5.5 ICLR0 Register (Offset = 48h) [Reset = 00000000h]

ICLR0 is shown in Table 21-14.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 21-14. ICLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	W	0h	Clear interrupt status for MEMRES3. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Clear interrupt status for MEMRES2. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Clear interrupt status for MEMRES1. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Clear interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7	ASCDONE	W	0h	Clear ASC done flag in RIS. 0h = Interrupt is not pending. 1h = Interrupt is pending.
6	UVIFG	W	0h	Clear interrupt flag for MEMRESx underflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
5	DMADONE	W	0h	Clear interrupt flag for DMADONE. 0h = Interrupt is not pending. 1h = Interrupt is pending.
4	INIFG	W	0h	Clear INIFG in MIS0 register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	W	0h	Clear interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	W	0h	Clear interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1	TOVIFG	W	0h	Clear interrupt flag for sequence conversion timeout overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.
0	OVIFG	W	0h	Clear interrupt flag for MEMRESx overflow. 0h = Interrupt is not pending. 1h = Interrupt is pending.

21.5.6 IMASK1 Register (Offset = 58h) [Reset = 00000000h]

IMASK1 is shown in Table 21-15.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS0 to MIS0 when the corresponding bit-fields are set to 1.

Table 21-15. IMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MEMRESIFG0	R/W	0h	MEMRES0 conversion result interrupt mask. 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	Reserved
4	INIFG	R/W	0h	In-range comparator interrupt mask. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	R/W	0h	Low threshold compare interrupt mask. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	R/W	0h	High threshold compare interrupt mask. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	Reserved

21.5.7 RIS1 Register (Offset = 60h) [Reset = 00000000h]

RIS1 is shown in Table 21-16.

Return to the Summary Table.

Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR0 register bit.

Table 21-16. RIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0.;This bit is set to 1 when MEMRES0 is loaded with a new;conversion result.;Reading MEMRES0 register will clear this bit, or when the;corresponding bit in ICLR1 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	Reserved
4	INIFG	R	0h	Raw interrupt status for In-range comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	R	0h	Raw interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	R	0h	Raw interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	Reserved

21.5.8 MIS1 Register (Offset = 68h) [Reset = 00000000h]

MIS1 is shown in Table 21-17.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of IMASK and RIS registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 21-17. MIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MEMRESIFG0	R	0h	Masked interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	Reserved
4	INIFG	R	0h	Mask INIFG in MIS1 register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	R	0h	Masked interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	R	0h	Masked interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	Reserved

21.5.9 ISET1 Register (Offset = 70h) [Reset = 00000000h]

ISET1 is shown in Table 21-18.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 21-18. ISET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MEMRESIFG0	W	0h	Set Interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	Reserved
4	INIFG	W	0h	Set INIFG interrupt register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	W	0h	Set interrupt for MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	W	0h	Set Interrupt for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	Reserved

21.5.10 ICLR1 Register (Offset = 78h) [Reset = 00000000h]

ICLR1 is shown in Table 21-19.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 21-19. ICLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	MEMRESIFG0	W	0h	Clear interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7-5	RESERVED	R	0h	Reserved
4	INIFG	W	0h	Clear INIFG in MIS1 register. 0h = Interrupt is not pending. 1h = Interrupt is pending.
3	LOWIFG	W	0h	Clear interrupt flag for the MEMRESx result register being below than the WCLOWx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
2	HIGHIFG	W	0h	Clear interrupt flag for the MEMRESx result register being higher than the WCHIGHx threshold of the window comparator. 0h = Interrupt is not pending. 1h = Interrupt is pending.
1-0	RESERVED	R	0h	Reserved

21.5.11 IMASK2 Register (Offset = 88h) [Reset = 00000000h]

IMASK2 is shown in Table 21-20.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS0 to MIS0 when the corresponding bit-fields are set to 1.

Table 21-20. IMASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	R/W	0h	MEMRES3 conversion result interrupt mask. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R/W	0h	MEMRES2 conversion result interrupt mask. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R/W	0h	MEMRES1 conversion result interrupt mask. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R/W	0h	MEMRES0 conversion result interrupt mask. 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	Reserved

21.5.12 RIS2 Register (Offset = 90h) [Reset = 00000000h]

RIS2 is shown in Table 21-21.

Return to the Summary Table.

Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR0 register bit.

Table 21-21. RIS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	R	0h	Raw interrupt status for MEMRES3.;This bit is set to 1 when MEMRES3 is loaded with a new;conversion result.;Reading MEMRES3 register will clear this bit, or when the;corresponding bit in ICLR2 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Raw interrupt status for MEMRES2.;This bit is set to 1 when MEMRES2 is loaded with a new;conversion result.;Reading MEMRES2 register will clear this bit, or when the;corresponding bit in ICLR2 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Raw interrupt status for MEMRES1.;This bit is set to 1 when MEMRES1 is loaded with a new;conversion result.;Reading MEMRES1 register will clear this bit, or when the;corresponding bit in ICLR2 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Raw interrupt status for MEMRES0.;This bit is set to 1 when MEMRES0 is loaded with a new;conversion result.;Reading MEMRES0 register will clear this bit, or when the;corresponding bit in ICLR2 is set to 1 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	Reserved

21.5.13 MIS2 Register (Offset = 98h) [Reset = 00000000h]

MIS2 is shown in Table 21-22.

Return to the Summary Table.

Extension of Masked interrupt status. This register is simply a bitwise AND of the contents of IMASK and RIS registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 21-22. MIS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	R	0h	Masked interrupt status for MEMRES3. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	R	0h	Masked interrupt status for MEMRES2. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	R	0h	Masked interrupt status for MEMRES1. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	R	0h	Masked interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	Reserved

21.5.14 ISET2 Register (Offset = A0h) [Reset = 00000000h]

ISET2 is shown in Table 21-23.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 21-23. ISET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	W	0h	Set interrupt status for MEMRES3. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Set interrupt status for MEMRES2. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Set interrupt status for MEMRES1. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Set Interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	Reserved

21.5.15 ICLR2 Register (Offset = A8h) [Reset = 00000000h]

ICLR2 is shown in Table 21-24.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding RIS bit also gets cleared. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets cleared.

Table 21-24. ICLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	MEMRESIFG3	W	0h	Clear interrupt status for MEMRES3. 0h = No new data ready. 1h = A new data is ready to be read.
10	MEMRESIFG2	W	0h	Clear interrupt status for MEMRES2. 0h = No new data ready. 1h = A new data is ready to be read.
9	MEMRESIFG1	W	0h	Clear interrupt status for MEMRES1. 0h = No new data ready. 1h = A new data is ready to be read.
8	MEMRESIFG0	W	0h	Clear interrupt status for MEMRES0. 0h = No new data ready. 1h = A new data is ready to be read.
7-0	RESERVED	R	0h	Reserved

21.5.16 CTL0 Register (Offset = 100h) [Reset = 00000000h]

CTL0 is shown in Table 21-25.

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Control Register 0

Table 21-25. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	SCLKDIV	R/W	0h	Sample clock divider 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 4 3h = Divide clock source by 8 4h = Divide clock source by 16 5h = Divide clock source by 24 6h = Divide clock source by 32 7h = Divide clock source by 48
23-17	RESERVED	R	0h	Reserved
16	PWRDN	R/W	0h	Power down policy 0h = ADC is powered down on completion of a conversion if there is no pending trigger 1h = ADC remains powered on as long as it is enabled through software.
15-1	RESERVED	R	0h	Reserved
0	ENC	R/W	0h	Enable conversion 0h = Conversion disabled. ENC change from ON to OFF will abort single or repeat sequence on a MEMCTLx boundary. The current conversion will finish and result stored in corresponding MEMRESx. 1h = Conversion enabled. ADC sequencer waits for the programmed trigger (software or hardware).

21.5.17 CTL1 Register (Offset = 104h) [Reset = 00000000h]

CTL1 is shown in Table 21-26.

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Control Register 1

Table 21-26. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20	SAMPMODE	R/W	0h	Sample mode. This bit selects the source of the sampling signal. ;MANUAL option is not applicable when TRIGSRC is selected as hardware event trigger. 0h = Sample timer high phase is used as sample signal 1h = Software trigger is used as sample signal
19-18	RESERVED	R	0h	Reserved
17-16	CONSEQ	R/W	0h	Conversion sequence mode 0h = ADC channel in MEMCTLx pointed by STARTADD will be converted once 1h = ADC channel sequence pointed by STARTADD and ENDADD will be converted once 2h = ADC channel in MEMCTLx pointed by STARTADD will be converted repeatedly 3h = ADC channel sequence pointed by STARTADD and ENDADD will be converted repeatedly
15-9	RESERVED	R	0h	Reserved
8	SC	R/W	0h	Start of conversion 0h = When SAMPMODE is set to MANUAL, clearing this bit will end the sample phase and the conversion phase will start.;When SAMPMODE is set to AUTO, writing 0 has no effect. 1h = When SAMPMODE is set to MANUAL, setting this bit will start the sample phase. Sample phase will last as long as this bit is set. ;When SAMPMODE is set to AUTO, setting this bit will trigger the timer based sample time.
7-1	RESERVED	R	0h	Reserved
0	TRIGSRC	R/W	0h	Sample trigger source 0h = Software trigger 1h = Hardware event trigger

21.5.18 CTL2 Register (Offset = 108h) [Reset = 00000000h]

CTL2 is shown in Table 21-27.

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Control Register 2

Table 21-27. CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	ENDADD	R/W	0h	Sequence end address. These bits select which MEMCTLx is the last one for the sequence mode.;The value of ENDADD is 0x00 to 0x03 corresponding to MEMRES0 to MEMRES3. 0h = MEMCTL0 is selected as end address of sequence. 1h = MEMCTL1 is selected as end address of sequence. 2h = MEMCTL2 is selected as end address of sequence. 3h = MEMCTL3 is selected as end address of sequence.
23-21	RESERVED	R	0h	Reserved
20-16	STARTADD	R/W	0h	Sequencer start address. These bits select which MEMCTLx is used for single conversion or as first MEMCTL for sequence mode. ;The value of STARTADD is 0x00 to 0x17, corresponding to MEMRES0 to MEMRES23. 0h = MEMCTL0 is selected as start address of a sequence or for a single conversion. 1h = MEMCTL1 is selected as start address of a sequence or for a single conversion. 2h = MEMCTL2 is selected as start address of a sequence or for a single conversion. 3h = MEMCTL3 is selected as start address of a sequence or for a single conversion.
15-11	RESERVED	R	0h	Reserved
10	FIFOEN	R/W	0h	Enable FIFO based operation 0h = Disable 1h = Enable
9	RESERVED	R	0h	Reserved
8	DMAEN	R/W	0h	Enable DMA trigger for data transfer. ;Note: DMAEN bit is cleared by hardware based on DMA done signal at the end of data transfer. Software has to re-enable DMAEN bit for ADC to generate DMA triggers. 0h = DMA trigger not enabled 1h = DMA trigger enabled
7-3	RESERVED	R	0h	Reserved
2-1	RES	R/W	0h	Resolution. These bits define the resolutoin of ADC conversion result.;Note : A value of 3 defaults to 12-bits resolution. 0h = 12-bits resolution 1h = 10-bits resolution 2h = 8-bits resolution
0	DF	R/W	0h	Data read-back format. Data is always stored in binary unsigned format. 0h = Digital result reads as Binary Unsigned. 1h = Digital result reads Signed Binary. (2s complement), left aligned.

21.5.19 CTL3 Register (Offset = 10Ch) [Reset = 00000000h]

CTL3 is shown in Table 21-28.

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Control Register 3. This register is used to configure ADC for ad-hoc single conversion.

Table 21-28. CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-12	ASCVRSEL	R/W	0h	Selects voltage reference for ASC operation. AREF- must be connected to on-board ground when external reference option is selected.;Note: Writing value 0x3 defaults to INTREF. 0h = VDDS reference 1h = External reference from AREF+/AREF- pins 2h = Internal reference
11-9	RESERVED	R	0h	Reserved
8	ASCSTIME	R/W	0h	ASC sample time compare value select. This is used to select between SCOMP0 and SCOMP1 registers for ASC operation. 0h = Select SCOMP0 1h = Select SCOMP1
7-5	RESERVED	R	0h	Reserved
4-0	ASCCHSEL	R/W	0h	ASC channel select 0h = Selects channel 0 1h = Selects channel 1 2h = Selects channel 2 3h = Selects channel 3 4h = Selects channel 4 5h = Selects channel 5 6h = Selects channel 6 7h = Selects channel 7 8h = Selects channel 8 9h = Selects channel 9 Ah = Selects channel 10 Bh = Selects channel 11 Ch = Selects channel 12 Dh = Selects channel 13 Eh = Selects channel 14 Fh = Selects channel 15

21.5.20 SCOMP0 Register (Offset = 114h) [Reset = 00000000h]

SCOMP0 is shown in Table 21-29.

Return to the Summary Table.

Sample time compare 0 register. Specifies the sample time, in number of ADC sample clock cycles. CTL0.ENC must be set to 0 to write to this register.

Table 21-29. SCOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	VAL	R/W	0h	Specifies the number of sample clocks.;When VAL = 0 or 1, number of sample clocks = Sample clock divide value.;When VAL > 1, number of sample clocks = VAL x Sample clock divide value.;Note: Sample clock divide value is not the value written to SCLKDIV but the actual divide value (SCLKDIV = 2 implies divide value is 4).;Example: VAL = 4, SCLKDIV = 3 implies 32 sample clock cycles.

21.5.21 SCOMP1 Register (Offset = 118h) [Reset = 00000000h]

SCOMP1 is shown in Table 21-30.

Return to the Summary Table.

Sample time compare 1 register. Specifies the sample time, in number of ADC sample clock cycles. CTL0.ENC must be set to 0 to write to this register.

Table 21-30. SCOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	VAL	R/W	0h	Specifies the number of sample clocks.;When VAL = 0 or 1, number of sample clocks = Sample clock divide value.;When VAL > 1, number of sample clocks = VAL x Sample clock divide value.;Note: Sample clock divide value is not the value written to SCLKDIV but the actual divide value (SCLKDIV = 2 implies divide value is 4).;Example: VAL = 4, SCLKDIV = 3 implies 32 sample clock cycles.

21.5.22 REFCFG Register (Offset = 11Ch) [Reset = 00000000h]

REFCFG is shown in Table 21-31.

Return to the Summary Table.

Reference buffer configuration register

Table 21-31. REFCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-3	IBPROG	R/W	0h	Configures reference buffer bias current output value 0h = 1uA 1h = 0.5uA 2h = 2uA 3h = 0.67uA
2	SPARE	R/W	0h	Spare bit
1	REFVSEL	R/W	0h	Configures reference buffer output voltage 0h = REFBUF generates 2.5V output 1h = REFBUF generates 1.4V output
0	REFEN	R/W	0h	Reference buffer enable 0h = Disable 1h = Enable

21.5.23 WCLOW Register (Offset = 148h) [Reset = 00000000h]

WCLOW is shown in Table 21-32.

Return to the Summary Table.

Window Comparator Low Threshold Register.;The data format that is used to write and read WCLOW depends on the value of DF bit in CTL2 register. ;CTL0.ENC must be 0 to write to this register.;Note: Change in ADC data format or resolution does not reset WCLOW.

Table 21-32. WCLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R/W	0h	If DF = 0, unsigned binary format has to be used. ;The value based on the resolution has to be right aligned with the MSB on the left.;For 10-bits and 8-bits resolution, unused bits have to be 0s.;If DF = 1, 2s-complement format has to be used.;The value based on the resolution has to be left aligned with the LSB on the right. ;For 10-bits and 8-bits resolution, unused bits have to be 0s.

21.5.24 WCHIGH Register (Offset = 150h) [Reset = 00000000h]

WCHIGH is shown in Table 21-33.

Return to the Summary Table.

Window Comparator High Threshold Register.;The data format that is used to write and read WCHIGH depends on the value of DF bit in CTL2 register. ;CTL0.ENC must be 0 to write to this register.;Note: Change in ADC data format or resolution does not reset WCHIGH.

Table 21-33. WCHIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R/W	0h	If DF = 0, unsigned binary format has to be used.;The threshold value has to be right aligned, with the MSB on the left.;For 10-bits and 8-bits resolution, unused bit have to be 0s.;If DF = 1, 2s-complement format has to be used.;The value based on the resolution has to be left aligned with the LSB on the right. ;For 10-bits and 8-bits resolution, unused bit have to be 0s.

21.5.25 FIFODATA Register (Offset = 160h) [Reset = 00000000h]

FIFODATA is shown in Table 21-34.

Return to the Summary Table.

FIFO data register. This is a virtual register used to read from FIFO.

Table 21-34. FIFODATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	Read from this data field returns the ADC sample from FIFO.

21.5.26 ASCRES Register (Offset = 170h) [Reset = 00000000h]

ASCRES is shown in Table 21-35.

Return to the Summary Table.

ASC result register

Table 21-35. ASCRES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	Result of ADC ad-hoc single conversion.;If DF = 0, unsigned binary:;The conversion result is right aligned. In 10 and 8 bit modes, the unused MSB bits are forced to 0. ;If DF = 1, 2s-complement format:;The conversion result is left aligned. In 10 and 8 bit modes, the unused LSB bits are forced to 0.;The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back.

21.5.27 MEMCTL0 Register (Offset = 180h) [Reset = 00000000h]

MEMCTL0 is shown in Table 21-36.

Return to the Summary Table.

Conversion Memory Control Register 0. ;CTL0.ENC must be set to 0 to write to this register.

Table 21-36. MEMCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	WINCOMP	R/W	0h	Enable window comparator. 0h = Disable 1h = Enable
27-25	RESERVED	R	0h	Reserved
24	TRG	R/W	0h	Trigger policy. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence or to perform next conversion in the case of repeat single channel conversions. 0h = Next conversion is automatic 1h = Next conversion requires a trigger
23-13	RESERVED	R	0h	Reserved
12	STIME	R/W	0h	Selects the source of sample timer period between SCOMP0 and SCOMP1. 0h = Select SCOMP0 1h = Select SCOMP1
11-10	RESERVED	R	0h	Reserved
9-8	VRSEL	R/W	0h	Voltage reference selection. AREF- must be connected to on-board ground when external reference option is selected.;Note: Writing value 0x3 defaults to INTREF. 0h = VDDS reference 1h = External reference from AREF+/AREF- pins 2h = Internal reference
7-5	RESERVED	R	0h	Reserved
4-0	CHANSEL	R/W	0h	Input channel select. 0h = Selects channel 0 1h = Selects channel 1 2h = Selects channel 2 3h = Selects channel 3 4h = Selects channel 4 5h = Selects channel 5 6h = Selects channel 6 7h = Selects channel 7 8h = Selects channel 8 9h = Selects channel 9 Ah = Selects channel 10 Bh = Selects channel 11 Ch = Selects channel 12 Dh = Selects channel 13 Eh = Selects channel 14 Fh = Selects channel 15

21.5.28 MEMCTL1 Register (Offset = 184h) [Reset = 00000000h]

MEMCTL1 is shown in Table 21-37.

Return to the Summary Table.

Conversion Memory Control Register 1. ;CTL0.ENC must be set to 0 to write to this register.

Table 21-37. MEMCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	WINCOMP	R/W	0h	Enable window comparator. 0h = Disable 1h = Enable
27-25	RESERVED	R	0h	Reserved
24	TRG	R/W	0h	Trigger policy. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence or to perform next conversion in the case of repeat single channel conversions. 0h = Next conversion is automatic 1h = Next conversion requires a trigger
23-13	RESERVED	R	0h	Reserved
12	STIME	R/W	0h	Selects the source of sample timer period between SCOMP0 and SCOMP1. 0h = Select SCOMP0 1h = Select SCOMP1
11-10	RESERVED	R	0h	Reserved
9-8	VRSEL	R/W	0h	Voltage reference selection. AREF- must be connected to on-board ground when external reference option is selected.;Note: Writing value 0x3 defaults to INTREF. 0h = VDDS reference 1h = External reference from AREF+/AREF- pins 2h = Internal reference
7-5	RESERVED	R	0h	Reserved
4-0	CHANSEL	R/W	0h	Input channel select. 0h = Selects channel 0 1h = Selects channel 1 2h = Selects channel 2 3h = Selects channel 3 4h = Selects channel 4 5h = Selects channel 5 6h = Selects channel 6 7h = Selects channel 7 8h = Selects channel 8 9h = Selects channel 9 Ah = Selects channel 10 Bh = Selects channel 11 Ch = Selects channel 12 Dh = Selects channel 13 Eh = Selects channel 14 Fh = Selects channel 15

21.5.29 MEMCTL2 Register (Offset = 188h) [Reset = 00000000h]

MEMCTL2 is shown in Table 21-38.

Return to the Summary Table.

Conversion Memory Control Register 2. ;CTL0.ENC must be set to 0 to write to this register.

Table 21-38. MEMCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	WINCOMP	R/W	0h	Enable window comparator. 0h = Disable 1h = Enable
27-25	RESERVED	R	0h	Reserved
24	TRG	R/W	0h	Trigger policy. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence or to perform next conversion in the case of repeat single channel conversions. 0h = Next conversion is automatic 1h = Next conversion requires a trigger
23-13	RESERVED	R	0h	Reserved
12	STIME	R/W	0h	Selects the source of sample timer period between SCOMP0 and SCOMP1. 0h = Select SCOMP0 1h = Select SCOMP1
11-10	RESERVED	R	0h	Reserved
9-8	VRSEL	R/W	0h	Voltage reference selection. AREF- must be connected to on-board ground when external reference option is selected.;Note: Writing value 0x3 defaults to INTREF. 0h = VDDS reference 1h = External reference from AREF+/AREF- pins 2h = Internal reference
7-5	RESERVED	R	0h	Reserved
4-0	CHANSEL	R/W	0h	Input channel select. 0h = Selects channel 0 1h = Selects channel 1 2h = Selects channel 2 3h = Selects channel 3 4h = Selects channel 4 5h = Selects channel 5 6h = Selects channel 6 7h = Selects channel 7 8h = Selects channel 8 9h = Selects channel 9 Ah = Selects channel 10 Bh = Selects channel 11 Ch = Selects channel 12 Dh = Selects channel 13 Eh = Selects channel 14 Fh = Selects channel 15

21.5.30 MEMCTL3 Register (Offset = 18Ch) [Reset = 00000000h]

MEMCTL3 is shown in Table 21-39.

Return to the Summary Table.

Conversion Memory Control Register 3. ;CTL0.ENC must be set to 0 to write to this register.

Table 21-39. MEMCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	WINCOMP	R/W	0h	Enable window comparator. 0h = Disable 1h = Enable
27-25	RESERVED	R	0h	Reserved
24	TRG	R/W	0h	Trigger policy. Indicates if a trigger will be needed to step to the next MEMCTL in the sequence or to perform next conversion in the case of repeat single channel conversions. 0h = Next conversion is automatic 1h = Next conversion requires a trigger
23-13	RESERVED	R	0h	Reserved
12	STIME	R/W	0h	Selects the source of sample timer period between SCOMP0 and SCOMP1. 0h = Select SCOMP0 1h = Select SCOMP1
11-10	RESERVED	R	0h	Reserved
9-8	VRSEL	R/W	0h	Voltage reference selection. AREF- must be connected to on-board ground when external reference option is selected.;Note: Writing value 0x3 defaults to INTREF. 0h = VDDS reference 1h = External reference from AREF+/AREF- pins 2h = Internal reference
7-5	RESERVED	R	0h	Reserved
4-0	CHANSEL	R/W	0h	Input channel select. 0h = Selects channel 0 1h = Selects channel 1 2h = Selects channel 2 3h = Selects channel 3 4h = Selects channel 4 5h = Selects channel 5 6h = Selects channel 6 7h = Selects channel 7 8h = Selects channel 8 9h = Selects channel 9 Ah = Selects channel 10 Bh = Selects channel 11 Ch = Selects channel 12 Dh = Selects channel 13 Eh = Selects channel 14 Fh = Selects channel 15

21.5.31 MEMRES0 Register (Offset = 280h) [Reset = 00000000h]

MEMRES0 is shown in Table 21-40.

Return to the Summary Table.

Memory Result Register 0

Table 21-40. MEMRES0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	If DF = 0, unsigned binary:;The conversion results are right aligned. In 10 and 8 bit modes, the unused MSB bits are forced to 0. ;If DF = 1, 2s-complement format:;The conversion results are left aligned. In 10 and 8 bit modes, the unused LSB bits are forced to 0.;The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back.;

21.5.32 MEMRES1 Register (Offset = 284h) [Reset = 00000000h]

MEMRES1 is shown in Table 21-41.

Return to the Summary Table.

Memory Result Register 1

Table 21-41. MEMRES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	If DF = 0, unsigned binary:;The conversion results are right aligned. In 10 and 8 bit modes, the unused MSB bits are forced to 0. ;If DF = 1, 2s-complement format:;The conversion results are left aligned. In 10 and 8 bit modes, the unused LSB bits are forced to 0.;The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back.;

21.5.33 MEMRES2 Register (Offset = 288h) [Reset = 00000000h]

MEMRES2 is shown in Table 21-42.

Return to the Summary Table.

Memory Result Register 2

Table 21-42. MEMRES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	If DF = 0, unsigned binary:;The conversion results are right aligned. In 10 and 8 bit modes, the unused MSB bits are forced to 0. ;If DF = 1, 2s-complement format:;The conversion results are left aligned. In 10 and 8 bit modes, the unused LSB bits are forced to 0.;The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back.;

21.5.34 MEMRES3 Register (Offset = 28Ch) [Reset = 00000000h]

MEMRES3 is shown in Table 21-43.

Return to the Summary Table.

Memory Result Register 3

Table 21-43. MEMRES3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	If DF = 0, unsigned binary:;The conversion results are right aligned. In 10 and 8 bit modes, the unused MSB bits are forced to 0. ;If DF = 1, 2s-complement format:;The conversion results are left aligned. In 10 and 8 bit modes, the unused LSB bits are forced to 0.;The data is stored in the right-justified format and is converted to the left-justified 2s-complement format during read back.;

21.5.35 STA Register (Offset = 340h) [Reset = 00000000h]

STA is shown in Table 21-44.

Return to the Summary Table.

Status Register

Table 21-44. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ASCACT	R	0h	ASC active 0h = Idle or done 1h = ASC active
1	RESERVED	R	0h	Reserved
0	BUSY	R	0h	Busy. This bit indicates that an active ADC sample or conversion operation is in progress. 0h = No ADC sampling or conversion in progress. 1h = ADC sampling or conversion is in progress.

21.5.36 TEST0 Register (Offset = E00h) [Reset = 00000000h]

TEST0 is shown in Table 21-45.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-45. TEST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	ATEST0_EN	R/W	0h	Internal. Only to be used through TI provided API.
29	ATEST1_EN	R/W	0h	Internal. Only to be used through TI provided API.
28-13	RESERVED	R	0h	Reserved
12-8	ATEST1_MUXSEL	R/W	0h	Internal. Only to be used through TI provided API.
7-5	RESERVED	R	0h	Reserved
4-0	ATEST0_MUXSEL	R/W	0h	Internal. Only to be used through TI provided API.

21.5.37 TEST2 Register (Offset = E08h) [Reset = 00000000h]

TEST2 is shown in Table 21-46.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-46. TEST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CDAC_OVST_EN	R/W	0h	Internal. Only to be used through TI provided API.
30-25	RESERVED	R	0h	Reserved
24	LATCH_TRIM_EN	R/W	0h	Internal. Only to be used through TI provided API.
23-21	RESERVED	R	0h	Reserved
20	COMP_GAIN_TRIM	R/W	0h	Internal. Only to be used through TI provided API.
19-9	RESERVED	R	0h	Reserved
8	MUX_TEST_SEL	R/W	0h	Internal. Only to be used through TI provided API.
7-0	RESERVED	R	0h	Reserved

21.5.38 TEST3 Register (Offset = E0Ch) [Reset = 00000000h]

TEST3 is shown in Table 21-47.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-47. TEST3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAL_ACUML	R/W	0h	Internal. Only to be used through TI provided API.

21.5.39 TEST4 Register (Offset = E10h) [Reset = 00000000h]

TEST4 is shown in Table 21-48.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-48. TEST4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_STEP_SEL_DIS	R/W	0h	Internal. Only to be used through TI provided API.
30-25	RESERVED	R	0h	Reserved
24	CAL_MODE_EN	R/W	0h	Internal. Only to be used through TI provided API.
23-22	RESERVED	R	0h	Reserved
21-16	CAL_STEP_SEL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

21.5.40 TEST5 Register (Offset = E14h) [Reset = 00000000h]

TEST5 is shown in Table 21-49.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-49. TEST5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	CAL_CAP_CTL	R/W	0h	Internal. Only to be used through TI provided API.

21.5.41 TEST6 Register (Offset = E18h) [Reset = 00000000h]

TEST6 is shown in Table 21-50.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-50. TEST6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	ATESTSEL	R/W	0h	Internal. Only to be used through TI provided API.

21.5.42 DEBUG1 Register (Offset = E20h) [Reset = 00000000h]

DEBUG1 is shown in Table 21-51.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-51. DEBUG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CTRL	R/W	00801000h	Internal. Only to be used through TI provided API.

21.5.43 DEBUG2 Register (Offset = E24h) [Reset = 00000000h]

DEBUG2 is shown in Table 21-52.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-52. DEBUG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	VTOI_CTRL	R/W	0h	Internal. Only to be used through TI provided API.
27-25	RESERVED	R	0h	Reserved
24	VTOI_TESTMODE_EN	R/W	0h	Internal. Only to be used through TI provided API.
23-0	RESERVED	R	0h	Reserved

21.5.44 DEBUG3 Register (Offset = E28h) [Reset = 00000000h]

DEBUG3 is shown in Table 21-53.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-53. DEBUG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	DEC1_DIS	R/W	0h	Internal. Only to be used through TI provided API.
4	DEC0_DIS	R/W	0h	Internal. Only to be used through TI provided API.
3-1	RESERVED	R	0h	Reserved
0	BOOST_ENZ	R/W	0h	Internal. Only to be used through TI provided API.

21.5.45 DEBUG4 Register (Offset = E2Ch) [Reset = 00000000h]

DEBUG4 is shown in Table 21-54.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 21-54. DEBUG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ADC_CTRL0	R/W	0h	Internal. Only to be used through TI provided API.

Chapter 22

I/O Controller (IOC)

This chapter describes the input/output controller (IOC) and the general-purpose inputs and outputs (GPIOs).

22.1 Introduction

The I/O controller configures I/O pins and maps peripheral signals to physical pins (DIOx). This chapter explains the I/O controller functions and gives examples on how to map peripheral functions to the pins chosen by the user.

- Each pin can be mapped to a specific set of peripherals
- GPIO is the base function where the IOC.IOC*n*[2:0] PORTCFG bit field is set to 0x0
- DIOn (DIO0 to DIO30) are the logical names of the different I/O pins on the specific package, see the device specific data sheet for more information on package pin designation
- 8 of these DIOs also have analog capabilities
- Pins can also be mapped to the digital test bus (DTB) to bring out clocks or physical signals like interrupts
- The device-specific data sheet provides:
  - Mapping between DIOn and pins for the different packages
  - Peripheral pin mapping (with different high-drive capability)
- Refer to device specific datasheet for number of DIOs supported.

22.2 Block Diagram

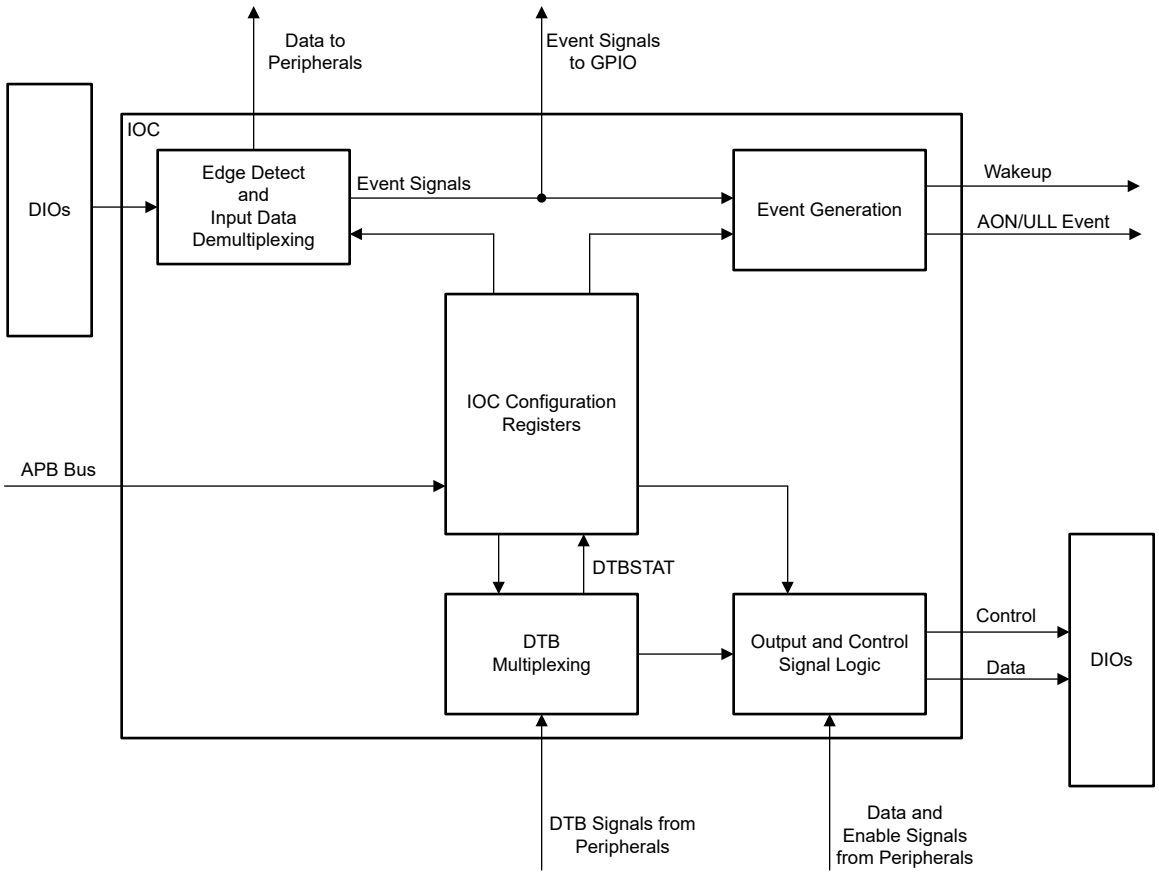

Figure 22-1. IOC Simplified Block Diagram

22.3 I/O Mapping and Configuration

Each peripheral with pin functions can be mapped to a specific set of pins. Refer to the device specific data sheet for the possible mappings.

22.3.1 Basic I/O Mapping

To map a peripheral function to a DIOn, where n can range from 0 to 22 (for the current available package) set IOC:IOCn.PORTCFG to the value that represents the target function. For example, to set DIO0 to the base function (GPIO) set IOC:IOC0.PORTCFG = 0x0.

22.3.2 Radio GPO

There are eight data output signals from the device radio named LRFDn where n is from 0 to 7. After selecting the IOC function for these signals, configure the LRFDDBELL registers GPOSEL0 or GPOSEL1 to select the source for those signals. See Chapter 28 for more information.

For example:

- Configure DIO3 for LRFD0 by setting IOC.IOC3[2:0] PORTCFG = 0x3 (See Pin Mapping)
- Select source for LRFD0 by setting LRFDDBELL.GPOSEL0[0:4] SRC0 bit field

22.3.3 Pin Mapping

See the device specific data sheet for peripheral and I/O mapping and capability.

22.3.4 DTB Muxing

Internal clocks and interrupts can be brought out to I/O pins via the digital test bus (DTB). For more information on configuring the DTB for clock or interrupt signals see Chapter 6 and Chapter 4.

Note

Due to the way data is latched into the DTBSTAT register, a single read is not always accurate. The value of DTBSTAT can only be relied on if two subsequent register reads indicate the same value.

Note

When observing clocks using the DTB the 1st clock cycle can have an incorrect duty cycle. This can also occur if the clocks that are being observed are switched, or if the internal clock divider values are updated.

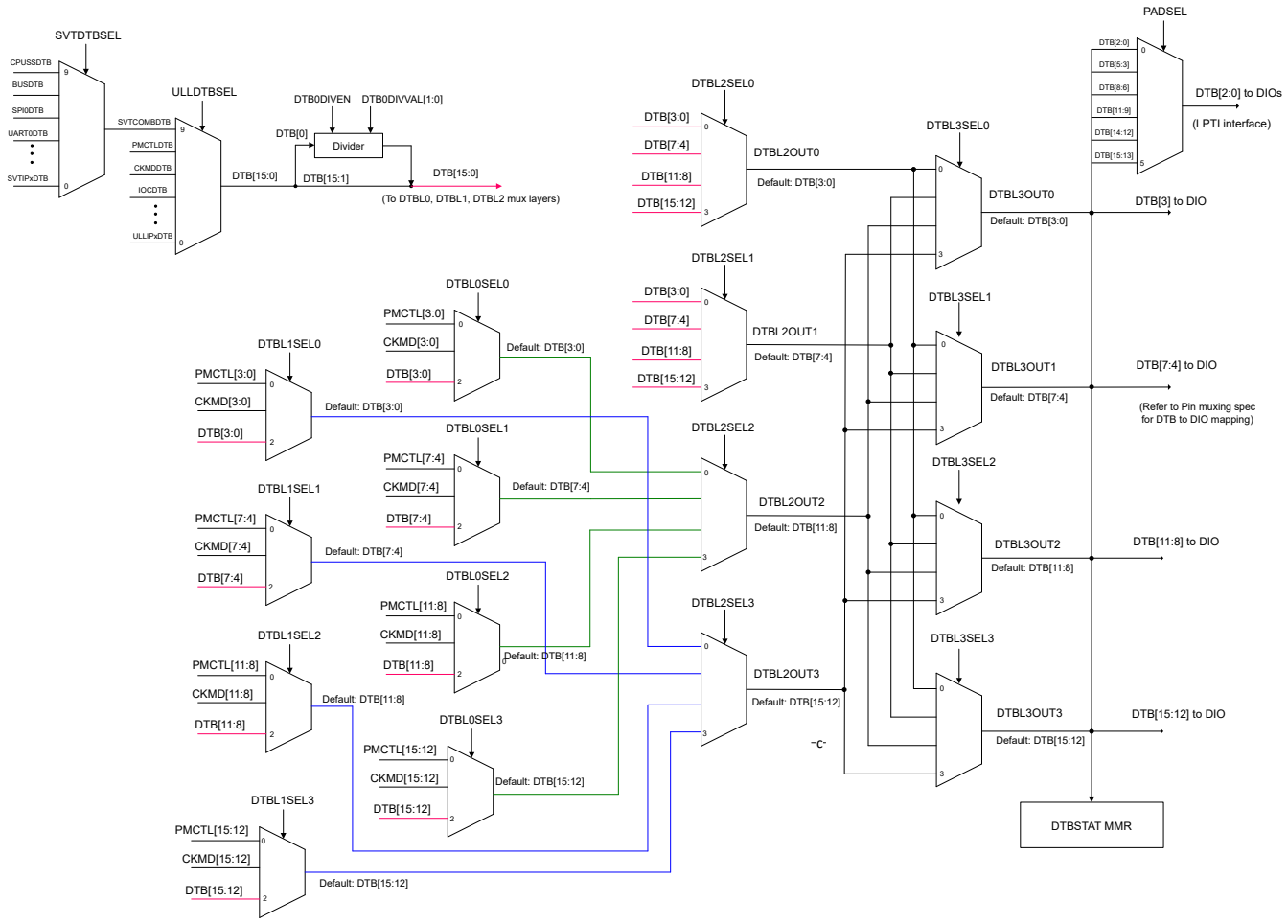

Figure 22-2. DTB Multiplexing

Table 22-1. MCU/SVT Signals Select

SVTSEL	Module
0	Disabled
1	Internal Use Only
2	Internal Use Only
3	Internal Use Only
4	Internal Use Only
5	Internal Use Only
6	Internal Use Only
7	Internal Use Only
8	Internal Use Only
9	Internal Use Only
10	Internal Use Only
11	Internal Use Only
12	Internal Use Only
13	Internal Use Only
14	EVTSVT
15	Internal Use Only
16	Internal Use Only

Table 22-1. MCU/SVT Signals Select (continued)

SVTSEL	Module
17	Internal Use Only
18	Internal Use Only

Table 22-2. AON/ULL Signals Select

ULLSEL	Module
0	SVT/MCU DTB
1	CKMD
2	EVTULL
3	Internal Use Only
4	Internal Use Only
5	Internal Use Only
6	Internal Use Only
7	Internal Use Only
8	Internal Use Only
9	Internal Use Only

22.4 Edge Detection

The IOC supports detection of rising, falling, or both rising and falling edges.

When an edge is detected on a DIO, the IOC publishes an event to the AON event fabric if IOC.EVTCFG is configured to publish the event. Only one DIOn can be selected to generate an event on the AON event fabric. The event flag is cleared by the user by clearing IOC.EVTCFG[8] EVTIFG.

The IOC can also generate a wake-up from standby signal to PMCTL on edge detection by setting IOC.IOC*n*[18] WUENSB. Any or all DIOn can be selected to generate a wake-up from standby on edge detection.

Note

Care must be taken to ensure that spurious edges are not generated while configuring edge detection feature. The recommended sequence is

1. Write all the IOC.IOC ***n*** bit fields for a DIO except for IOC.IOC ***n*** [17:16] EDGEDET and IOC.IOC ***n*** [29] INPEN. These fields are left cleared to 0.
2. Then, write the INPEN bit field
3. Finally, write the EDGET bit field

22.5 GPIO

The MCU GPIO is a general-purpose input/output module that allows software to write to and read from the DIOs. These pins are configured by the IOC module. To modify a single GPIO output value, use the GPIO.DOUT ***n*** registers. The following describes the necessary steps to set up DIO1 as a GPIO output and toggle the bit.

TI recommends using the GPIO driver in the SimpleLink™ Low Power F3 Software Development Kit (SDK) when managing general purpose I/Os.

1. Map DIO1 as a GPIO output by setting the IOC.IOC1[2:0] PORTCFG bit field to 0 (Base function - GPIO).
2. Set DIO1 as output by clearing the IOC.IOC1[29] INPEN bit. More port configurations can also be set in the IOC.IOC1 register (for more details, see Section 22.6).
3. Set the data output enable bit for DIO1 in the GPIO.DOE31_0[1] DIO1 bit field by issuing a read-modify-write operation.
4. Toggle the DIO1 output by writing a 1 to the GPIO.DOUTTGL31_0[1] DIO1 bit.

22.6 I/O Pins

The IOC allows software to configure the pins based on the requirements of the application. The software can configure different characteristic settings for any or all of the I/O pins. All of the following features, are controlled in the IOC:IOCn registers:

- **Drive Strength** (IOC:IOCFGn.IOSTR)
  - Configures the output drive strength of an I/O pin.
- **Drive Current** (IOC.IOCFGn[11:10] IOCURR)
  - Configures the maximum current of an I/O pin. See the device specific data sheet for individual I/O current capability.
- **Pull Control** (IOC:IOCn.PULLCTL)
  - Configures a weak pull on an I/O pin. The following can be set: pull-up, pull-down, or no pull. See the data sheet for specific pull-up and pull-down current.
- **Slew Control** (IOC:IOCn.SLEWRED)
  - Sets normal or reduced slew rate on an I/O pin.
- **Hysteresis** (IOC:IOCFGn.HYSTEN)
  - Enables or disables input hysteresis on an I/O pin.
- **Open-Source or Open-Drain Configuration** (IOC:IOCn.IOMODE)
  - Configures the pin as normal, open source, or open drain; all of these can be set to either inverted or normal (non-inverted).
- **Edge Detection** (IOC:IOCn.EDGEDET)
  - Enables edge detection on I/O pin. The following modes are supported:
    - Rising edge
    - Falling edge
    - Trigger on both rising and falling
    - No edge detection
  - Edge detection can be used for event generation on the AON event fabric and/or a wake from standby signal to PMCTL
- **Wake from Shutdown** (IOC:IOCn.WUCFGSD)
  - Enables wake-up from shutdown. The following modes are supported:
    - Wake on low, wake-up triggered when pin level is low
    - Wake on high, wake-up triggered when pin level is high
- **Input Driver** (IOC:IOCn.INPEN)
  - Enables or disables the I/O input driver.
- **Pin Configuration**
  - (IOC.IOCn[2:0] PORTCFG) Selects the function of the pin. See the device specific data sheet for available functionality per I/O pin.

22.7 Unused Pins

By default, the I/O driver (output) and input buffer (input) are disabled (tri-state mode) at power on or reset, and thus the I/O pin can safely be left unconnected (floating). If the I/O pin is in a tri-state condition and connected to a node with a different voltage potential, a small leakage current can go through the pin. The same applies to an I/O pin configured as input, where the pin is connected to a voltage source (for example VDD/2). The input is then an undefined value of either 0 or 1.

22.8 Debug Configuration

When the DBGSS.DBGCTL[5] SWDCEN bit is set, DIOs corresponding to the SWDIO and SWCLK pads are connected to the IceMelter wakeup circuit. SWDCEN is set to enable a debug connection. See Chapter 5 for more information on the Debug Subsystem.

When using SWD debug, configure the IOC. IOC*n*[2:0] PORTCFG bit field of the DIOs corresponding to SWDIO and SWCLK to a value 0x0 (GPIO) before setting the DBGSS.DBGCTL[5] SWDCEN bit and do not write to

GPIO.DOUT*n* and GPIO.DOE*n* registers. This prevents data from IOC interfering with IceMelter operation and SWDIO and SWCLK data from interfering with peripherals.

When DBGSS.DBGCTL[5] SWDCEN is cleared, DIOs corresponding to pads SWDIO and SWCLK are connected to IOC (instead of Icemelter). Always clear SWDCEN before using the DIOs corresponding to SWDIO and SWCLK for non-debug purposes, to avoid possible timing violations within IceMelter.

22.9 IOC Registers

Table 22-3 lists the memory-mapped registers for the IOC registers. All register offset addresses not listed in Table 22-3 should be considered as reserved locations and the register contents should not be modified.

Table 22-3. IOC Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 22.9.1
4h	DESCEX	Extended Module Description	Section 22.9.2
100h	IOC0	Configuration	Section 22.9.3
104h	IOC1	Configuration	Section 22.9.4
108h	IOC2	Configuration	Section 22.9.5
10Ch	IOC3	Configuration	Section 22.9.6
110h	IOC4	Configuration	Section 22.9.7
114h	IOC5	Configuration	Section 22.9.8
118h	IOC6	Configuration	Section 22.9.9
11Ch	IOC7	Configuration	Section 22.9.10
120h	IOC8	Configuration	Section 22.9.11
124h	IOC9	Configuration	Section 22.9.12
128h	IOC10	Configuration	Section 22.9.13
12Ch	IOC11	Configuration	Section 22.9.14
130h	IOC12	Configuration	Section 22.9.15
134h	IOC13	Configuration	Section 22.9.16
138h	IOC14	Configuration	Section 22.9.17
13Ch	IOC15	Configuration	Section 22.9.18
140h	IOC16	Configuration	Section 22.9.19
144h	IOC17	Configuration	Section 22.9.20
148h	IOC18	Configuration	Section 22.9.21
14Ch	IOC19	Configuration	Section 22.9.22
150h	IOC20	Configuration	Section 22.9.23
154h	IOC21	Configuration	Section 22.9.24
158h	IOC22	Configuration	Section 22.9.25
15Ch	IOC23	Configuration	Section 22.9.26
160h	IOC24	Configuration	Section 22.9.27
164h	IOC25	Configuration	Section 22.9.28
168h	IOC26	Configuration	Section 22.9.29
16Ch	IOC27	Configuration	Section 22.9.30
170h	IOC28	Configuration	Section 22.9.31
174h	IOC29	Configuration	Section 22.9.32
178h	IOC30	Configuration	Section 22.9.33
C00h	DTBCFG	DTB configuration	Section 22.9.34
C04h	DTBOE	DTB output enable	Section 22.9.35
C08h	EVTCFG	Event configuration	Section 22.9.36
C0Ch	TEST	Test	Section 22.9.37
C10h	DTBSTAT	DTB status	Section 22.9.38
C14h	DTBMUXCFG0	**DTB** mux configuration 0 register. This register is used to configure DTB level 0 and level 1 mux layers.	Section 22.9.39

Table 22-3. IOC Registers (continued)

Offset	Acronym	Register Name	Section
C18h	DTBMUXCFG1	**DTB** mux configuration 1 register. This register is used to configure DTB level 2 and level 3 mux layers.	Section 22.9.40

Complex bit access types are encoded to fit into small table cells. Table 22-4 shows the codes that are used for access types in this section.

Table 22-4. IOC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

22.9.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 22-5.

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Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 22-5. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	D440h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

22.9.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 22-6.

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Extended Description Register. This register provides configuration details of the IP to software drivers and end users.

Table 22-6. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	NUMDTBIO	R	Fh	Number of DTB IOs supported. Total DTB IOs supported is NUMDTBIO value +1. 0h = Smallest value Fh = Highest possible value
11-7	NUMHDIO	R	5h	Number of high drive IOs supported. Total high drive IOs supported is NUMHDIO value +1. 0h = Smallest value 1Fh = Highest possible value
6	HDIO	R	1h	High drive IO supported by IOC. 0h = HD IO not supported by IOC 1h = HD IO supported by IOC
5-0	NUMDIO	R	1Eh	Number of DIOs supported. Total DIOs supported is NUMDIO value +1. 0h = Smallest value 3Fh = Highest possible value

22.9.3 IOC0 Register (Offset = 100h) [Reset = 00000000h]

IOC0 is shown in Table 22-7.

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Configuration of DIO0

Table 22-7. IOC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO0 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.4 IOC1 Register (Offset = 104h) [Reset = 00000000h]

IOC1 is shown in Table 22-8.

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Configuration of DIO1

Table 22-8. IOC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO1 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.5 IOC2 Register (Offset = 108h) [Reset = 00000000h]

IOC2 is shown in Table 22-9.

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Configuration of DIO2

Table 22-9. IOC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12	SLEWRED	R/W	0h	Slew rate configuration 0h = Normal slew rate 1h = Reduced slew rate
11-10	IOCURR	R/W	0h	Output current configuration. Writing value 0x3 defaults to 2mA current setting. 0h = 2mA 1h = 4mA 2h = 8mA
9-8	IOSTR	R/W	0h	Drive strength configuration 0h = Automatic drive strength adjustment 1h = Minimum drive stregnth 2h = Medium drive strength 3h = Maximum drive strength
7-3	RESERVED	R	0h	Reserved

Table 22-9. IOC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PORTCFG	R/W	0h	Selects usage of DIO2 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.6 IOC3 Register (Offset = 10Ch) [Reset = 00000000h]

IOC3 is shown in Table 22-10.

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Configuration of DIO3

Table 22-10. IOC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12	SLEWRED	R/W	0h	Slew rate configuration 0h = Normal slew rate 1h = Reduced slew rate
11-10	IOCURR	R/W	0h	Output current configuration. Writing value 0x3 defaults to 2mA current setting. 0h = 2mA 1h = 4mA 2h = 8mA
9-8	IOSTR	R/W	0h	Drive strength configuration 0h = Automatic drive strength adjustment 1h = Minimum drive stregnth 2h = Medium drive strength 3h = Maximum drive strength
7-3	RESERVED	R	0h	Reserved

Table 22-10. IOC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PORTCFG	R/W	0h	Selects usage of DIO3 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.7 IOC4 Register (Offset = 110h) [Reset = 00000000h]

IOC4 is shown in Table 22-11.

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Configuration of DIO4

Table 22-11. IOC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO4 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.8 IOC5 Register (Offset = 114h) [Reset = 00000000h]

IOC5 is shown in Table 22-12.

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Configuration of DIO5

Table 22-12. IOC5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO5 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.9 IOC6 Register (Offset = 118h) [Reset = 00000000h]

IOC6 is shown in Table 22-13.

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Configuration of DIO6

Table 22-13. IOC6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO6 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.10 IOC7 Register (Offset = 11Ch) [Reset = 00000000h]

IOC7 is shown in Table 22-14.

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Configuration of DIO7

Table 22-14. IOC7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO7 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.11 IOC8 Register (Offset = 120h) [Reset = 00000000h]

IOC8 is shown in Table 22-15.

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Configuration of DIO8

Table 22-15. IOC8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO8 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.12 IOC9 Register (Offset = 124h) [Reset = 00000000h]

IOC9 is shown in Table 22-16.

Return to the Summary Table.

Configuration of DIO9

Table 22-16. IOC9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	2h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12	SLEWRED	R/W	0h	Slew rate configuration 0h = Normal slew rate 1h = Reduced slew rate
11-10	IOCURR	R/W	0h	Output current configuration. Writing value 0x3 defaults to 2mA current setting. 0h = 2mA 1h = 4mA 2h = 8mA
9-8	IOSTR	R/W	0h	Drive strength configuration 0h = Automatic drive strength adjustment 1h = Minimum drive stregnth 2h = Medium drive strength 3h = Maximum drive strength
7-3	RESERVED	R	0h	Reserved

Table 22-16. IOC9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PORTCFG	R/W	0h	Selects usage of DIO9 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.13 IOC10 Register (Offset = 128h) [Reset = 00000000h]

IOC10 is shown in Table 22-17.

Return to the Summary Table.

Configuration of DIO10

Table 22-17. IOC10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	1h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12	SLEWRED	R/W	0h	Slew rate configuration 0h = Normal slew rate 1h = Reduced slew rate
11-10	IOCURR	R/W	0h	Output current configuration. Writing value 0x3 defaults to 2mA current setting. 0h = 2mA 1h = 4mA 2h = 8mA
9-8	IOSTR	R/W	0h	Drive strength configuration 0h = Automatic drive strength adjustment 1h = Minimum drive stregnth 2h = Medium drive strength 3h = Maximum drive strength
7-3	RESERVED	R	0h	Reserved

Table 22-17. IOC10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PORTCFG	R/W	0h	Selects usage of DIO10 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.14 IOC11 Register (Offset = 12Ch) [Reset = 00000000h]

IOC11 is shown in Table 22-18.

Return to the Summary Table.

Configuration of DIO11

Table 22-18. IOC11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO11 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.15 IOC12 Register (Offset = 130h) [Reset = 00000000h]

IOC12 is shown in Table 22-19.

Return to the Summary Table.

Configuration of DIO12

Table 22-19. IOC12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO12 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.16 IOC13 Register (Offset = 134h) [Reset = 00000000h]

IOC13 is shown in Table 22-20.

Return to the Summary Table.

Configuration of DIO13

Table 22-20. IOC13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO13 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.17 IOC14 Register (Offset = 138h) [Reset = 00000000h]

IOC14 is shown in Table 22-21.

Return to the Summary Table.

Configuration of DIO14

Table 22-21. IOC14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO14 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.18 IOC15 Register (Offset = 13Ch) [Reset = 00000000h]

IOC15 is shown in Table 22-22.

Return to the Summary Table.

Configuration of DIO15

Table 22-22. IOC15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO15 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.19 IOC16 Register (Offset = 140h) [Reset = 00000000h]

IOC16 is shown in Table 22-23.

Return to the Summary Table.

Configuration of DIO16

Table 22-23. IOC16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO16 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.20 IOC17 Register (Offset = 144h) [Reset = 00000000h]

IOC17 is shown in Table 22-24.

Return to the Summary Table.

Configuration of DIO17

Table 22-24. IOC17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12	SLEWRED	R/W	0h	Slew rate configuration 0h = Normal slew rate 1h = Reduced slew rate
11-10	IOCURR	R/W	0h	Output current configuration. Writing value 0x3 defaults to 2mA current setting. 0h = 2mA 1h = 4mA 2h = 8mA
9-8	IOSTR	R/W	0h	Drive strength configuration 0h = Automatic drive strength adjustment 1h = Minimum drive stregnth 2h = Medium drive strength 3h = Maximum drive strength
7-3	RESERVED	R	0h	Reserved

Table 22-24. IOC17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PORTCFG	R/W	0h	Selects usage of DIO17 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.21 IOC18 Register (Offset = 148h) [Reset = 00000000h]

IOC18 is shown in Table 22-25.

Return to the Summary Table.

Configuration of DIO18

Table 22-25. IOC18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12	SLEWRED	R/W	0h	Slew rate configuration 0h = Normal slew rate 1h = Reduced slew rate
11-10	IOCURR	R/W	0h	Output current configuration. Writing value 0x3 defaults to 2mA current setting. 0h = 2mA 1h = 4mA 2h = 8mA
9-8	IOSTR	R/W	0h	Drive strength configuration 0h = Automatic drive strength adjustment 1h = Minimum drive stregnth 2h = Medium drive strength 3h = Maximum drive strength
7-3	RESERVED	R	0h	Reserved

Table 22-25. IOC18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	PORTCFG	R/W	0h	Selects usage of DIO18 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.22 IOC19 Register (Offset = 14Ch) [Reset = 00000000h]

IOC19 is shown in Table 22-26.

Return to the Summary Table.

Configuration of DIO19

Table 22-26. IOC19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO19 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.23 IOC20 Register (Offset = 150h) [Reset = 00000000h]

IOC20 is shown in Table 22-27.

Return to the Summary Table.

Configuration of DIO20

Table 22-27. IOC20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO20 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.24 IOC21 Register (Offset = 154h) [Reset = 00000000h]

IOC21 is shown in Table 22-28.

Return to the Summary Table.

Configuration of DIO21

Table 22-28. IOC21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO21 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.25 IOC22 Register (Offset = 158h) [Reset = 00000000h]

IOC22 is shown in Table 22-29.

Return to the Summary Table.

Configuration of DIO22

Table 22-29. IOC22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO22 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.26 IOC23 Register (Offset = 15Ch) [Reset = 00000000h]

IOC23 is shown in Table 22-30.

Return to the Summary Table.

Configuration of DIO23

Table 22-30. IOC23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO23 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.27 IOC24 Register (Offset = 160h) [Reset = 00000000h]

IOC24 is shown in Table 22-31.

Return to the Summary Table.

Configuration of DIO24

Table 22-31. IOC24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO24 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.28 IOC25 Register (Offset = 164h) [Reset = 00000000h]

IOC25 is shown in Table 22-32.

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Configuration of DIO25

Table 22-32. IOC25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO25 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.29 IOC26 Register (Offset = 168h) [Reset = 00000000h]

IOC26 is shown in Table 22-33.

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Configuration of DIO26

Table 22-33. IOC26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO26 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.30 IOC27 Register (Offset = 16Ch) [Reset = 00000000h]

IOC27 is shown in Table 22-34.

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Configuration of DIO27

Table 22-34. IOC27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO27 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.31 IOC28 Register (Offset = 170h) [Reset = 00000000h]

IOC28 is shown in Table 22-35.

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Configuration of DIO28

Table 22-35. IOC28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO28 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.32 IOC29 Register (Offset = 174h) [Reset = 00000000h]

IOC29 is shown in Table 22-36.

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Configuration of DIO29

Table 22-36. IOC29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO29 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.33 IOC30 Register (Offset = 178h) [Reset = 00000000h]

IOC30 is shown in Table 22-37.

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Configuration of DIO30

Table 22-37. IOC30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	HYSTEN	R/W	0h	This field controls input hysteresis 0h = Input hysteresis disabled 1h = Input hysteresis enabled
29	INPEN	R/W	0h	This field controls the input capability of DIO 0h = Input disabled 1h = Input enabled
28-27	RESERVED	R	0h	Reserved
26-24	IOMODE	R/W	0h	IO Mode. Setting this to value 0x6 or 0x7 will default to normal IO behavior. 0h = Normal IO 1h = Inverted IO 2h = Open Drain, normal IO 3h = Open Drain, inverted IO 4h = Open Source, normal IO 5h = Open Source, inverted IO
23-22	RESERVED	R	0h	Reserved
21-20	WUCFGSD	R/W	0h	Wakeup configuration from shutdown 0h = Wakeup disabled 1h = Wakeup disabled 2h = Wakeup triggered when pad level is low 3h = Wakeup triggered when pad level is high
19	RESERVED	R	0h	Reserved
18	WUENSB	R/W	0h	Wakeup enable from standby 0h = Wakeup disabled 1h = Wakeup enabled (effective only if EDGEDET is enabled)
17-16	EDGEDET	R/W	0h	Edge detect configuration 0h = No edge detection 1h = Negative edge detection 2h = Positive edge detection 3h = Positive and negative edge detection
15	RESERVED	R	0h	Reserved
14-13	PULLCTL	R/W	0h	Pull control. Setting this to value 0x3 disables pull. 0h = No pull 1h = Pull down enabled 2h = Pull up enabled
12-3	RESERVED	R	0h	Reserved
2-0	PORTCFG	R/W	0h	Selects usage of DIO30 0h = Base function 1h = Digital peripheral function-1 2h = Digital peripheral function-2 3h = Digital peripheral function-3 4h = Digital peripheral function-4 5h = Digital peripheral function-5 6h = Analog function 7h = Digital Test Bus function

22.9.34 DTBCFG Register (Offset = C00h) [Reset = 00000000h]

DTBCFG is shown in Table 22-38.

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DTB configuration

Table 22-38. DTBCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	DTB0DIVVAL	R/W	0h	These bits are used to configure the DTB[0] divider value. 0h = Divide by 2 1h = Divide by 4 2h = Divide by 8 3h = Divide by 16
27-24	RESERVED	R	0h	Reserved
23	DTB0DIVEN	R/W	0h	This bit is used to enable the programmable divider on DTB[0]. 0h = Disable 1h = Enable
22-19	RESERVED	R	0h	Reserved
18-16	PADSEL	R/W	0h	Selects which 3 DTB lines out of total 16 are routed to DTB pins 15 to 13. 0h = DTB[15:13] selected 1h = DTB[14:12] selected 2h = DTB[11:9] selected 3h = DTB[8:6] selected 4h = DTB[5:3] selected 5h = DTB[2:0] selected
15-13	RESERVED	R	0h	Reserved
12-8	ULLSEL	R/W	0h	ULL DTB Mux selection 0h = SVT IPs 1h = CKMDIG IP 2h = ULL Event IP 3h = PM controller IP 4h = PMUDLC IP 5h = RTC IP 6h = IO controller IP 7h = PMU digital IP 8h = Debug subsystem IP 9h = SYS0 IP
7-5	RESERVED	R	0h	Reserved
4-0	SVTSEL	R/W	0h	SVT DTB Mux selection 0h = Disable 1h = ADC IP 2h = BUS IP 3h = Clock controller IP 4h = CPU subsystem IP 5h = DMA IP 6h = GPIO IP 7h = I2C IP 8h = AES IP 9h = LGPT IP Ah = LRF IP Bh = FLASH(NVM) IP Ch = SPI IP Dh = SRAM IP Eh = SVT Event IP Fh = System timer IP 10h = Instance 0 of UART IP 11h = Instance 1 of UART IP 12h = VIMS IP

22.9.35 DTBOE Register (Offset = C04h) [Reset = 00000000h]

DTBOE is shown in Table 22-39.

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DTB output enable

Table 22-39. DTBOE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	EN15	R/W	0h	Enables DTB output 15 0h = DTB output disabled 1h = DTB output enabled
14	EN14	R/W	0h	Enables DTB output 14 0h = DTB output disabled 1h = DTB output enabled
13	EN13	R/W	0h	Enables DTB output 13 0h = DTB output disabled 1h = DTB output enabled
12	EN12	R/W	0h	Enables DTB output 12 0h = DTB output disabled 1h = DTB output enabled
11	EN11	R/W	0h	Enables DTB output 11 0h = DTB output disabled 1h = DTB output enabled
10	EN10	R/W	0h	Enables DTB output 10 0h = DTB output disabled 1h = DTB output enabled
9	EN9	R/W	0h	Enables DTB output 9 0h = DTB output disabled 1h = DTB output enabled
8	EN8	R/W	0h	Enables DTB output 8 0h = DTB output disabled 1h = DTB output enabled
7	EN7	R/W	0h	Enables DTB output 7 0h = DTB output disabled 1h = DTB output enabled
6	EN6	R/W	0h	Enables DTB output 6 0h = DTB output disabled 1h = DTB output enabled
5	EN5	R/W	0h	Enables DTB output 5 0h = DTB output disabled 1h = DTB output enabled
4	EN4	R/W	0h	Enables DTB output 4 0h = DTB output disabled 1h = DTB output enabled
3	EN3	R/W	0h	Enables DTB output 3 0h = DTB output disabled 1h = DTB output enabled
2	EN2	R/W	0h	Enables DTB output 2 0h = DTB output disabled 1h = DTB output enabled
1	EN1	R/W	0h	Enables DTB output 1 0h = DTB output disabled 1h = DTB output enabled
0	EN0	R/W	0h	Enables DTB output 0 0h = DTB output disabled 1h = DTB output enabled

22.9.36 EVTCFG Register (Offset = C08h) [Reset = 00000000h]

EVTCFG is shown in Table 22-40.

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Event configuration. This register is used to select DIO for IOC to publish event on ULL event fabric. It also contains enable bit that is used to mask the event and event flag bit.

Table 22-40. EVTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	EVTIFG	R/W	0h	Event flag. It is set when edge is detected on selected DIO.;Note: The edge detector flop is cleared for the selected DIO when EVTIFG is cleared by software. 0h = Clear ULL event 1h = Set ULL event
7	EVTEN	R/W	0h	Enables IOC to publish event on AON event fabric when EVTIFG is set. 0h = Disable 1h = Enable
6	RESERVED	R	0h	Reserved
5-0	DIOSEL	R/W	0h	This is used to select DIO for event generation. For example, DIOSEL = 0x0 selects DIO0 and DIOSEL = 0x8 selects DIO8.

22.9.37 TEST Register (Offset = C0Ch) [Reset = 00000000h]

TEST is shown in Table 22-41.

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Test register.

Table 22-41. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SEL	R/W	0h	This is used to drive SWDIO output data and output enable from debug sub-system onto TBD (TDO) pad. 0h = Output data and output enable managed by IOC 1h = Output data and output enable driven based on debug sub-system inputs

22.9.38 DTBSTAT Register (Offset = C10h) [Reset = 00000000h]

DTBSTAT is shown in Table 22-42.

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DTB status register. This register captures the value of DTBL3 mux layer output.

Table 22-42. DTBSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	This bit field captures the final 16-bit value of DTB signals provided from IOC to DTB device pins.

22.9.39 DTBMUXCFG0 Register (Offset = C14h) [Reset = 00000000h]

DTBMUXCFG0 is shown in Table 22-43.

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DTB mux configuration 0 register. This register is used to configure DTB level 0 and level 1 mux layers.

Table 22-43. DTBMUXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	DTBL1SEL3	R/W	2h	Select bits for DTBL1 fourth mux 0h = Selects PMCTL DTB[15:12] 1h = Selects CKMD DTB[15:12] 2h = Selects DTB[15:12] 3h = Defaults to selection of DTB[15:12]
27-26	RESERVED	R	0h	Reserved
25-24	DTBL1SEL2	R/W	2h	Select bits for DTBL1 third mux 0h = Selects PMCTL DTB[11:8] 1h = Selects CKMD DTB[11:8] 2h = Selects DTB[11:8] 3h = Defaults to selection of DTB[11:8]
23-22	RESERVED	R	0h	Reserved
21-20	DTBL1SEL1	R/W	2h	Select bits for DTBL1 second mux 0h = Selects PMCTL DTB[7:4] 1h = Selects CKMD DTB[7:4] 2h = Selects DTB[7:4] 3h = Defaults to selection of DTB[7:4]
19-18	RESERVED	R	0h	Reserved
17-16	DTBL1SEL0	R/W	2h	Select bits for DTBL1 first mux 0h = Selects PMCTL DTB[3:0] 1h = Selects CKMD DTB[3:0] 2h = Selects DTB[3:0] 3h = Defaults to selection of DTB[3:0]
15-14	RESERVED	R	0h	Reserved
13-12	DTBL0SEL3	R/W	2h	Select bits for DTBL0 fourth mux 0h = Selects PMCTL DTB[15:12] 1h = Selects CKMD DTB[15:12] 2h = Selects DTB[15:12] 3h = Defaults to selection of DTB[15:12]
11-10	RESERVED	R	0h	Reserved
9-8	DTBL0SEL2	R/W	2h	Select bits for DTBL0 third mux 0h = Selects PMCTL DTB[11:8] 1h = Selects CKMD DTB[11:8] 2h = Selects DTB[11:8] 3h = Defaults to selection of DTB[11:8]
7-6	RESERVED	R	0h	Reserved
5-4	DTBL0SEL1	R/W	2h	Select bits for DTBL0 second mux 0h = Selects PMCTL DTB[7:4] 1h = Selects CKMD DTB[7:4] 2h = Selects DTB[7:4] 3h = Defaults to selection of DTB[7:4]
3-2	RESERVED	R	0h	Reserved
1-0	DTBL0SEL0	R/W	2h	Select bits for DTBL0 first mux 0h = Selects PMCTL DTB[3:0] 1h = Selects CKMD DTB[3:0] 2h = Selects DTB[3:0] 3h = Defaults to selection of DTB[3:0]

22.9.40 DTBMUXCFG1 Register (Offset = C18h) [Reset = 00000000h]

DTBMUXCFG1 is shown in Table 22-44.

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DTB mux configuration 1 register. This register is used to configure DTB level 2 and level 3 mux layers.

Table 22-44. DTBMUXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-28	DTBL3SEL3	R/W	3h	Select bits for DTBL3 fourth mux 0h = Selects DTBL2 first mux output 1h = Selects DTBL2 second mux output 2h = Selects DTBL2 third mux output 3h = Selects DTBL2 fourth mux output
27-26	RESERVED	R	0h	Reserved
25-24	DTBL3SEL2	R/W	2h	Select bits for DTBL3 third mux 0h = Selects DTBL2 first mux output 1h = Selects DTBL2 second mux output 2h = Selects DTBL2 third mux output 3h = Selects DTBL2 fourth mux output
23-22	RESERVED	R	0h	Reserved
21-20	DTBL3SEL1	R/W	1h	Select bits for DTBL3 second mux 0h = Selects DTBL2 first mux output 1h = Selects DTBL2 second mux output 2h = Selects DTBL2 third mux output 3h = Selects DTBL2 fourth mux output
19-18	RESERVED	R	0h	Reserved
17-16	DTBL3SEL0	R/W	0h	Select bits for DTBL3 first mux 0h = Selects DTBL2 first mux output 1h = Selects DTBL2 second mux output 2h = Selects DTBL2 third mux output 3h = Selects DTBL2 fourth mux output
15-14	RESERVED	R	0h	Reserved
13-12	DTBL2SEL3	R/W	3h	Select bits for DTBL2 fourth mux 0h = Selects DTBL1 first mux output 1h = Selects DTBL1 second mux output 2h = Selects DTBL1 third mux output 3h = Selects DTBL1 fourth mux output
11-10	RESERVED	R	0h	Reserved
9-8	DTBL2SEL2	R/W	2h	Select bits for DTBL2 third mux 0h = Selects DTBL0 first mux output 1h = Selects DTBL0 second mux output 2h = Selects DTBL0 third mux output 3h = Selects DTBL0 fourth mux output
7-6	RESERVED	R	0h	Reserved
5-4	DTBL2SEL1	R/W	1h	Select bits for DTBL2 second mux 0h = Selects DTB[3:0] 1h = Selects DTB[7:4] 2h = Selects DTB[11:8] 3h = Selects DTB[15:12]
3-2	RESERVED	R	0h	Reserved
1-0	DTBL2SEL0	R/W	0h	Select bits for DTBL2 first mux 0h = Selects DTB[3:0] 1h = Selects DTB[7:4] 2h = Selects DTB[11:8] 3h = Selects DTB[15:12]

22.10 GPIO Registers

Table 22-45 lists the memory-mapped registers for the GPIO registers. All register offset addresses not listed in Table 22-45 should be considered as reserved locations and the register contents should not be modified.

Table 22-45. GPIO Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 22.10.1
4h	DESCEX	Module Description Extended	Section 22.10.2
44h	IMASK	Interrupt Mask	Section 22.10.3
4Ch	RIS	Raw interrupt status	Section 22.10.4
54h	MIS	Masked interrupt status	Section 22.10.5
5Ch	ISET	Interrupt set	Section 22.10.6
64h	ICLR	Interrupt clear	Section 22.10.7
6Ch	IMSET	Interrupt mask set	Section 22.10.8
74h	IMCLR	Interrupt mask clear	Section 22.10.9
100h	DOUT3_0	Alias for Data out 3 to 0	Section 22.10.10
104h	DOUT7_4	Alias for Data out 7 to 4	Section 22.10.11
108h	DOUT11_8	Alias for Data out 11 to 8	Section 22.10.12
10Ch	DOUT15_12	Alias for Data out 15 to 12	Section 22.10.13
110h	DOUT19_16	Alias for Data out 19 to 16	Section 22.10.14
114h	DOUT23_20	Alias for Data out 23 to 20	Section 22.10.15
118h	DOUT27_24	Alias for Data out 27 to 24	Section 22.10.16
11Ch	DOUT31_28	Alias for Data out 31 to 28	Section 22.10.17
200h	DOUT31_0	Data out 31 to 0	Section 22.10.18
210h	DOUTSET31_0	Data out set 31 to 0	Section 22.10.19
220h	DOUTCLR31_0	Data out clear 31 to 0	Section 22.10.20
230h	DOUTTGL31_0	Data out toggle 31 to 0	Section 22.10.21
300h	DOUTTGL3_0	Alias for Data out toggle 3 to 0	Section 22.10.22
304h	DOUTTGL7_4	Alias for Data out toggle 7 to 4	Section 22.10.23
308h	DOUTTGL11_8	Alias for Data out toggle 11 to 8	Section 22.10.24
30Ch	DOUTTGL15_12	Alias for Data out toggle 15 to 12	Section 22.10.25
310h	DOUTTGL19_16	Alias for Data out toggle 19 to 16	Section 22.10.26
314h	DOUTTGL23_20	Alias for Data out toggle 23 to 20	Section 22.10.27
318h	DOUTTGL27_24	Alias for Data out toggle 27 to 24	Section 22.10.28
31Ch	DOUTTGL31_28	Alias for Data out toggle 31 to 28	Section 22.10.29
400h	DOE3_0	Alias for Data out enable 3 to 0	Section 22.10.30
404h	DOE7_4	Alias for Data out enable 7 to 4	Section 22.10.31
408h	DOE11_8	Alias for Data out enable 11 to 8	Section 22.10.32
40Ch	DOE15_12	Alias for Data out enable 15 to 12	Section 22.10.33
410h	DOE19_16	Alias for Data out enable 19 to 16	Section 22.10.34
414h	DOE23_20	Alias for Data out enable 23 to 20	Section 22.10.35
418h	DOE27_24	Alias for Data out enable 27 to 24	Section 22.10.36
41Ch	DOE31_28	Alias for Data out enable 31 to 28	Section 22.10.37
500h	DOE31_0	Data out enable 31 to 0	Section 22.10.38
510h	DOESET31_0	Data out enable set 31 to 0	Section 22.10.39
520h	DOECLR31_0	Data out enable clear 31 to 0	Section 22.10.40
530h	DOETGL31_0	Data out enable toggle 31 to 0	Section 22.10.41

Table 22-45. GPIO Registers (continued)

Offset	Acronym	Register Name	Section
600h	DIN3_0	Alias for Data input 3 to 0	Section 22.10.42
604h	DIN7_4	Alias for Data input 7 to 4	Section 22.10.43
608h	DIN11_8	Alias for Data input 11 to 8	Section 22.10.44
60Ch	DIN15_12	Alias for Data input 15 to 12	Section 22.10.45
610h	DIN19_16	Alias for Data input 19 to 16	Section 22.10.46
614h	DIN23_20	Alias for Data input 23 to 20	Section 22.10.47
618h	DIN27_24	Alias for Data input 27 to 24	Section 22.10.48
61Ch	DIN31_28	Alias for Data input 31 to 28	Section 22.10.49
700h	DIN31_0	Data input 31 to 0	Section 22.10.50
800h	EVTCFG	Event configuration 0	Section 22.10.51
810h	EVTCFG1	Event configuration 1	Section 22.10.52

Complex bit access types are encoded to fit into small table cells. Table 22-46 shows the codes that are used for access types in this section.

Table 22-46. GPIO Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

22.10.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 22-47.

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Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 22-47. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	7C49h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set from aggregated IRQ registers till DTB.;0: Standard IP MMRs do not exist;0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

22.10.2 DESCEX Register (Offset = 4h) [Reset = 00000000h]

DESCEX is shown in Table 22-48.

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Provide IP-specific instance information

Table 22-48. DESCEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	NUMDIO	R	1Eh	This provides the total number of DIOs supported by GPIO. The number of DIOs supprted is NUMDIO + 1

22.10.3 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 22-49.

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Interrupt mask for DIO pins

Table 22-49. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	R/W	0h	Interrupt mask for DIO30 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
29	DIO29	R/W	0h	Interrupt mask for DIO29 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
28	DIO28	R/W	0h	Interrupt mask for DIO28 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
27	DIO27	R/W	0h	Interrupt mask for DIO27 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
26	DIO26	R/W	0h	Interrupt mask for DIO26 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
25	DIO25	R/W	0h	Interrupt mask for DIO25 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
24	DIO24	R/W	0h	Interrupt mask for DIO24 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
23	DIO23	R/W	0h	Interrupt mask for DIO23 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
22	DIO22	R/W	0h	Interrupt mask for DIO22 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
21	DIO21	R/W	0h	Interrupt mask for DIO21 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
20	DIO20	R/W	0h	Interrupt mask for DIO20 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
19	DIO19	R/W	0h	Interrupt mask for DIO19 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
18	DIO18	R/W	0h	Interrupt mask for DIO18 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
17	DIO17	R/W	0h	Interrupt mask for DIO17 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
16	DIO16	R/W	0h	Interrupt mask for DIO16 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
15	DIO15	R/W	0h	Interrupt mask for DIO15 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

Table 22-49. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R/W	0h	Interrupt mask for DIO14 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
13	DIO13	R/W	0h	Interrupt mask for DIO13 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
12	DIO12	R/W	0h	Interrupt mask for DIO12 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
11	DIO11	R/W	0h	Interrupt mask for DIO11 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
10	DIO10	R/W	0h	Interrupt mask for DIO10 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
9	DIO9	R/W	0h	Interrupt mask for DIO9 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
8	DIO8	R/W	0h	Interrupt mask for DIO8 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
7	DIO7	R/W	0h	Interrupt mask for DIO7 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	DIO6	R/W	0h	Interrupt mask for DIO6 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	DIO5	R/W	0h	Interrupt mask for DIO5 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	DIO4	R/W	0h	Interrupt mask for DIO4 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	DIO3	R/W	0h	Interrupt mask for DIO3 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	DIO2	R/W	0h	Interrupt mask for DIO2 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	DIO1	R/W	0h	Interrupt mask for DIO1 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	DIO0	R/W	0h	Interrupt mask for DIO0 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

22.10.4 RIS Register (Offset = 4Ch) [Reset = 00000000h]

RIS is shown in Table 22-50.

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Raw interrupt flag for DIO pins

Table 22-50. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	R	0h	Raw interrupt flag for DIO30 0h = Interrupt did not occur 1h = Interrupt occured
29	DIO29	R	0h	Raw interrupt flag for DIO29 0h = Interrupt did not occur 1h = Interrupt occured
28	DIO28	R	0h	Raw interrupt flag for DIO28 0h = Interrupt did not occur 1h = Interrupt occured
27	DIO27	R	0h	Raw interrupt flag for DIO27 0h = Interrupt did not occur 1h = Interrupt occured
26	DIO26	R	0h	Raw interrupt flag for DIO26 0h = Interrupt did not occur 1h = Interrupt occured
25	DIO25	R	0h	Raw interrupt flag for DIO25 0h = Interrupt did not occur 1h = Interrupt occured
24	DIO24	R	0h	Raw interrupt flag for DIO24 0h = Interrupt did not occur 1h = Interrupt occured
23	DIO23	R	0h	Raw interrupt flag for DIO23 0h = Interrupt did not occur 1h = Interrupt occured
22	DIO22	R	0h	Raw interrupt flag for DIO22 0h = Interrupt did not occur 1h = Interrupt occured
21	DIO21	R	0h	Raw interrupt flag for DIO21 0h = Interrupt did not occur 1h = Interrupt occured
20	DIO20	R	0h	Raw interrupt flag for DIO20 0h = Interrupt did not occur 1h = Interrupt occured
19	DIO19	R	0h	Raw interrupt flag for DIO19 0h = Interrupt did not occur 1h = Interrupt occured
18	DIO18	R	0h	Raw interrupt flag for DIO18 0h = Interrupt did not occur 1h = Interrupt occured
17	DIO17	R	0h	Raw interrupt flag for DIO17 0h = Interrupt did not occur 1h = Interrupt occured
16	DIO16	R	0h	Raw interrupt flag for DIO16 0h = Interrupt did not occur 1h = Interrupt occured
15	DIO15	R	0h	Raw interrupt flag for DIO15 0h = Interrupt did not occur 1h = Interrupt occured

Table 22-50. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R	0h	Raw interrupt flag for DIO14 0h = Interrupt did not occur 1h = Interrupt occured
13	DIO13	R	0h	Raw interrupt flag for DIO13 0h = Interrupt did not occur 1h = Interrupt occured
12	DIO12	R	0h	Raw interrupt flag for DIO12 0h = Interrupt did not occur 1h = Interrupt occured
11	DIO11	R	0h	Raw interrupt flag for DIO11 0h = Interrupt did not occur 1h = Interrupt occured
10	DIO10	R	0h	Raw interrupt flag for DIO10 0h = Interrupt did not occur 1h = Interrupt occured
9	DIO9	R	0h	Raw interrupt flag for DIO9 0h = Interrupt did not occur 1h = Interrupt occured
8	DIO8	R	0h	Raw interrupt flag for DIO8 0h = Interrupt did not occur 1h = Interrupt occured
7	DIO7	R	0h	Raw interrupt flag for DIO7 0h = Interrupt did not occur 1h = Interrupt occured
6	DIO6	R	0h	Raw interrupt flag for DIO6 0h = Interrupt did not occur 1h = Interrupt occured
5	DIO5	R	0h	Raw interrupt flag for DIO5 0h = Interrupt did not occur 1h = Interrupt occured
4	DIO4	R	0h	Raw interrupt flag for DIO4 0h = Interrupt did not occur 1h = Interrupt occured
3	DIO3	R	0h	Raw interrupt flag for DIO3 0h = Interrupt did not occur 1h = Interrupt occured
2	DIO2	R	0h	Raw interrupt flag for DIO2 0h = Interrupt did not occur 1h = Interrupt occured
1	DIO1	R	0h	Raw interrupt flag for DIO1 0h = Interrupt did not occur 1h = Interrupt occured
0	DIO0	R	0h	Raw interrupt flag for DIO0 0h = Interrupt did not occur 1h = Interrupt occured

22.10.5 MIS Register (Offset = 54h) [Reset = 00000000h]

MIS is shown in Table 22-51.

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Masked interrupt flag for DIO pins

Table 22-51. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	R	0h	Masked interrupt flag for DIO30 0h = Interrupt did not occur 1h = Interrupt occured
29	DIO29	R	0h	Masked interrupt flag for DIO29 0h = Interrupt did not occur 1h = Interrupt occured
28	DIO28	R	0h	Masked interrupt flag for DIO28 0h = Interrupt did not occur 1h = Interrupt occured
27	DIO27	R	0h	Masked interrupt flag for DIO27 0h = Interrupt did not occur 1h = Interrupt occured
26	DIO26	R	0h	Masked interrupt flag for DIO26 0h = Interrupt did not occur 1h = Interrupt occured
25	DIO25	R	0h	Masked interrupt flag for DIO25 0h = Interrupt did not occur 1h = Interrupt occured
24	DIO24	R	0h	Masked interrupt flag for DIO24 0h = Interrupt did not occur 1h = Interrupt occured
23	DIO23	R	0h	Masked interrupt flag for DIO23 0h = Interrupt did not occur 1h = Interrupt occured
22	DIO22	R	0h	Masked interrupt flag for DIO22 0h = Interrupt did not occur 1h = Interrupt occured
21	DIO21	R	0h	Masked interrupt flag for DIO21 0h = Interrupt did not occur 1h = Interrupt occured
20	DIO20	R	0h	Masked interrupt flag for DIO20 0h = Interrupt did not occur 1h = Interrupt occured
19	DIO19	R	0h	Masked interrupt flag for DIO19 0h = Interrupt did not occur 1h = Interrupt occured
18	DIO18	R	0h	Masked interrupt flag for DIO18 0h = Interrupt did not occur 1h = Interrupt occured
17	DIO17	R	0h	Masked interrupt flag for DIO17 0h = Interrupt did not occur 1h = Interrupt occured
16	DIO16	R	0h	Masked interrupt flag for DIO16 0h = Interrupt did not occur 1h = Interrupt occured
15	DIO15	R	0h	Masked interrupt flag for DIO15 0h = Interrupt did not occur 1h = Interrupt occured

Table 22-51. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R	0h	Masked interrupt flag for DIO14 0h = Interrupt did not occur 1h = Interrupt occured
13	DIO13	R	0h	Masked interrupt flag for DIO13 0h = Interrupt did not occur 1h = Interrupt occured
12	DIO12	R	0h	Masked interrupt flag for DIO12 0h = Interrupt did not occur 1h = Interrupt occured
11	DIO11	R	0h	Masked interrupt flag for DIO11 0h = Interrupt did not occur 1h = Interrupt occured
10	DIO10	R	0h	Masked interrupt flag for DIO10 0h = Interrupt did not occur 1h = Interrupt occured
9	DIO9	R	0h	Masked interrupt flag for DIO9 0h = Interrupt did not occur 1h = Interrupt occured
8	DIO8	R	0h	Masked interrupt flag for DIO8 0h = Interrupt did not occur 1h = Interrupt occured
7	DIO7	R	0h	Masked interrupt flag for DIO7 0h = Interrupt did not occur 1h = Interrupt occured
6	DIO6	R	0h	Masked interrupt flag for DIO6 0h = Interrupt did not occur 1h = Interrupt occured
5	DIO5	R	0h	Masked interrupt flag for DIO5 0h = Interrupt did not occur 1h = Interrupt occured
4	DIO4	R	0h	Masked interrupt flag for DIO4 0h = Interrupt did not occur 1h = Interrupt occured
3	DIO3	R	0h	Masked interrupt flag for DIO3 0h = Interrupt did not occur 1h = Interrupt occured
2	DIO2	R	0h	Masked interrupt flag for DIO2 0h = Interrupt did not occur 1h = Interrupt occured
1	DIO1	R	0h	Masked interrupt flag for DIO1 0h = Interrupt did not occur 1h = Interrupt occured
0	DIO0	R	0h	Masked interrupt flag for DIO0 0h = Interrupt did not occur 1h = Interrupt occured

22.10.6 ISET Register (Offset = 5Ch) [Reset = 00000000h]

ISET is shown in Table 22-52.

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Set interrupt flag in RIS by writing a one

Table 22-52. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Set DIO30 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
29	DIO29	W	0h	Set DIO29 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
28	DIO28	W	0h	Set DIO28 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
27	DIO27	W	0h	Set DIO27 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
26	DIO26	W	0h	Set DIO26 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
25	DIO25	W	0h	Set DIO25 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
24	DIO24	W	0h	Set DIO24 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
23	DIO23	W	0h	Set DIO23 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
22	DIO22	W	0h	Set DIO22 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
21	DIO21	W	0h	Set DIO21 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
20	DIO20	W	0h	Set DIO20 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
19	DIO19	W	0h	Set DIO19 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
18	DIO18	W	0h	Set DIO18 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
17	DIO17	W	0h	Set DIO17 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
16	DIO16	W	0h	Set DIO16 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
15	DIO15	W	0h	Set DIO15 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt

Table 22-52. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Set DIO14 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
13	DIO13	W	0h	Set DIO13 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
12	DIO12	W	0h	Set DIO12 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
11	DIO11	W	0h	Set DIO11 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
10	DIO10	W	0h	Set DIO10 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
9	DIO9	W	0h	Set DIO9 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
8	DIO8	W	0h	Set DIO8 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
7	DIO7	W	0h	Set DIO7 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
6	DIO6	W	0h	Set DIO6 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
5	DIO5	W	0h	Set DIO5 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
4	DIO4	W	0h	Set DIO4 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
3	DIO3	W	0h	Set DIO3 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
2	DIO2	W	0h	Set DIO2 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
1	DIO1	W	0h	Set DIO1 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt
0	DIO0	W	0h	Set DIO0 in RIS 0h = Writing 0 has no effect 1h = Set Interrupt

22.10.7 ICLR Register (Offset = 64h) [Reset = 00000000h]

ICLR is shown in Table 22-53.

Return to the Summary Table.

Clear interrupt flag in RIS by writing a one

Table 22-53. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Clears DIO30 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
29	DIO29	W	0h	Clears DIO29 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
28	DIO28	W	0h	Clears DIO28 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
27	DIO27	W	0h	Clears DIO27 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
26	DIO26	W	0h	Clears DIO26 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
25	DIO25	W	0h	Clears DIO25 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
24	DIO24	W	0h	Clears DIO24 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
23	DIO23	W	0h	Clears DIO23 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
22	DIO22	W	0h	Clears DIO22 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
21	DIO21	W	0h	Clears DIO21 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
20	DIO20	W	0h	Clears DIO20 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
19	DIO19	W	0h	Clears DIO19 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
18	DIO18	W	0h	Clears DIO18 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
17	DIO17	W	0h	Clears DIO17 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
16	DIO16	W	0h	Clears DIO16 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
15	DIO15	W	0h	Clears DIO15 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt

Table 22-53. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Clears DIO14 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
13	DIO13	W	0h	Clears DIO13 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
12	DIO12	W	0h	Clears DIO12 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
11	DIO11	W	0h	Clears DIO11 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
10	DIO10	W	0h	Clears DIO10 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
9	DIO9	W	0h	Clears DIO9 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
8	DIO8	W	0h	Clears DIO8 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
7	DIO7	W	0h	Clears DIO7 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
6	DIO6	W	0h	Clears DIO6 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
5	DIO5	W	0h	Clears DIO5 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
4	DIO4	W	0h	Clears DIO4 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
3	DIO3	W	0h	Clears DIO3 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
2	DIO2	W	0h	Clears DIO2 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
1	DIO1	W	0h	Clears DIO1 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt
0	DIO0	W	0h	Clears DIO0 in RIS 0h = Writing 0 has no effect 1h = Clear Interrupt

22.10.8 IMSET Register (Offset = 6Ch) [Reset = 00000000h]

IMSET is shown in Table 22-54.

Return to the Summary Table.

Set interrupt mask in IMASK by writing a one

Table 22-54. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Sets DIO30 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
29	DIO29	W	0h	Sets DIO29 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
28	DIO28	W	0h	Sets DIO28 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
27	DIO27	W	0h	Sets DIO27 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
26	DIO26	W	0h	Sets DIO26 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
25	DIO25	W	0h	Sets DIO25 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
24	DIO24	W	0h	Sets DIO24 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
23	DIO23	W	0h	Sets DIO23 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
22	DIO22	W	0h	Sets DIO22 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
21	DIO21	W	0h	Sets DIO21 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
20	DIO20	W	0h	Sets DIO20 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
19	DIO19	W	0h	Sets DIO19 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
18	DIO18	W	0h	Sets DIO18 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
17	DIO17	W	0h	Sets DIO17 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
16	DIO16	W	0h	Sets DIO16 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
15	DIO15	W	0h	Sets DIO15 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask

Table 22-54. IMSET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Sets DIO14 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
13	DIO13	W	0h	Sets DIO13 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
12	DIO12	W	0h	Sets DIO12 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
11	DIO11	W	0h	Sets DIO11 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
10	DIO10	W	0h	Sets DIO10 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
9	DIO9	W	0h	Sets DIO9 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
8	DIO8	W	0h	Sets DIO8 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
7	DIO7	W	0h	Sets DIO7 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
6	DIO6	W	0h	Sets DIO6 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
5	DIO5	W	0h	Sets DIO5 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
4	DIO4	W	0h	Sets DIO4 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
3	DIO3	W	0h	Sets DIO3 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
2	DIO2	W	0h	Sets DIO2 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
1	DIO1	W	0h	Sets DIO1 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask
0	DIO0	W	0h	Sets DIO0 in IMASK 0h = Writing 0 has no effect 1h = Set interrupt mask

22.10.9 IMCLR Register (Offset = 74h) [Reset = 00000000h]

IMCLR is shown in Table 22-55.

Return to the Summary Table.

Clear interrupt mask in IMASK by writing a one

Table 22-55. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Clears DIO30 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
29	DIO29	W	0h	Clears DIO29 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
28	DIO28	W	0h	Clears DIO28 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
27	DIO27	W	0h	Clears DIO27 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
26	DIO26	W	0h	Clears DIO26 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
25	DIO25	W	0h	Clears DIO25 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
24	DIO24	W	0h	Clears DIO24 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
23	DIO23	W	0h	Clears DIO23 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
22	DIO22	W	0h	Clears DIO22 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
21	DIO21	W	0h	Clears DIO21 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
20	DIO20	W	0h	Clears DIO20 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
19	DIO19	W	0h	Clears DIO19 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
18	DIO18	W	0h	Clears DIO18 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
17	DIO17	W	0h	Clears DIO17 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
16	DIO16	W	0h	Clears DIO16 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
15	DIO15	W	0h	Clears DIO15 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask

Table 22-55. IMCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Clears DIO14 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
13	DIO13	W	0h	Clears DIO13 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
12	DIO12	W	0h	Clears DIO12 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
11	DIO11	W	0h	Clears DIO11 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
10	DIO10	W	0h	Clears DIO10 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
9	DIO9	W	0h	Clears DIO9 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
8	DIO8	W	0h	Clears DIO8 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
7	DIO7	W	0h	Clears DIO7 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
6	DIO6	W	0h	Clears DIO6 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
5	DIO5	W	0h	Clears DIO5 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
4	DIO4	W	0h	Clears DIO4 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
3	DIO3	W	0h	Clears DIO3 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
2	DIO2	W	0h	Clears DIO2 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
1	DIO1	W	0h	Clears DIO1 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask
0	DIO0	W	0h	Clears DIO0 in IMASK 0h = Writing 0 has no effect 1h = Clear interrupt mask

22.10.10 DOUT3_0 Register (Offset = 100h) [Reset = 00000000h]

DOUT3_0 is shown in Table 22-56.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[3:0] bits.

Table 22-56. DOUT3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO3	R/W	0h	Data output for DIO3 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO2	R/W	0h	Data output for DIO2 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO1	R/W	0h	Data output for DIO1 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO0	R/W	0h	Data output for DIO0 0h = Output is set to 0 1h = Output is set to 1

22.10.11 DOUT7_4 Register (Offset = 104h) [Reset = 00000000h]

DOUT7_4 is shown in Table 22-57.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[7:4] bits

Table 22-57. DOUT7_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO7	R/W	0h	Data output for DIO7 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO6	R/W	0h	Data output for DIO6 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO5	R/W	0h	Data output for DIO5 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO4	R/W	0h	Data output for DIO4 0h = Output is set to 0 1h = Output is set to 1

22.10.12 DOUT11_8 Register (Offset = 108h) [Reset = 00000000h]

DOUT11_8 is shown in Table 22-58.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[11:8] bits

Table 22-58. DOUT11_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO11	R/W	0h	Data output for DIO11 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO10	R/W	0h	Data output for DIO10 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO9	R/W	0h	Data output for DIO9 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO8	R/W	0h	Data output for DIO8 0h = Output is set to 0 1h = Output is set to 1

22.10.13 DOUT15_12 Register (Offset = 10Ch) [Reset = 00000000h]

DOUT15_12 is shown in Table 22-59.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[15:12] bits

Table 22-59. DOUT15_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO15	R/W	0h	Data output for DIO15 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO14	R/W	0h	Data output for DIO14 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO13	R/W	0h	Data output for DIO13 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO12	R/W	0h	Data output for DIO12 0h = Output is set to 0 1h = Output is set to 1

22.10.14 DOUT19_16 Register (Offset = 110h) [Reset = 00000000h]

DOUT19_16 is shown in Table 22-60.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[19:16] bits

Table 22-60. DOUT19_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO19	R/W	0h	Data output for DIO19 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO18	R/W	0h	Data output for DIO18 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO17	R/W	0h	Data output for DIO17 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO16	R/W	0h	Data output for DIO16 0h = Output is set to 0 1h = Output is set to 1

22.10.15 DOUT23_20 Register (Offset = 114h) [Reset = 00000000h]

DOUT23_20 is shown in Table 22-61.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[23:20] bits

Table 22-61. DOUT23_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO23	R/W	0h	Data output for DIO23 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO22	R/W	0h	Data output for DIO22 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO21	R/W	0h	Data output for DIO21 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO20	R/W	0h	Data output for DIO20 0h = Output is set to 0 1h = Output is set to 1

22.10.16 DOUT27_24 Register (Offset = 118h) [Reset = 00000000h]

DOUT27_24 is shown in Table 22-62.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[27:24] bits

Table 22-62. DOUT27_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO27	R/W	0h	Data output for DIO27 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	R	0h	Reserved
16	DIO26	R/W	0h	Data output for DIO26 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO25	R/W	0h	Data output for DIO25 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO24	R/W	0h	Data output for DIO24 0h = Output is set to 0 1h = Output is set to 1

22.10.17 DOUT31_28 Register (Offset = 11Ch) [Reset = 00000000h]

DOUT31_28 is shown in Table 22-63.

Return to the Summary Table.

Alias register for byte access to DOUT31_0[31:28] bits

Table 22-63. DOUT31_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	DIO30	R/W	0h	Data output for DIO30 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	R	0h	Reserved
8	DIO29	R/W	0h	Data output for DIO29 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	R	0h	Reserved
0	DIO28	R/W	0h	Data output for DIO28 0h = Output is set to 0 1h = Output is set to 1

22.10.18 DOUT31_0 Register (Offset = 200h) [Reset = 00000000h]

DOUT31_0 is shown in Table 22-64.

Return to the Summary Table.

Data Output for DIO 31 to 0 pins.

Table 22-64. DOUT31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	R/W	0h	Data output for DIO30 0h = Output is set to 0 1h = Output is set to 1
29	DIO29	R/W	0h	Data output for DIO29 0h = Output is set to 0 1h = Output is set to 1
28	DIO28	R/W	0h	Data output for DIO28 0h = Output is set to 0 1h = Output is set to 1
27	DIO27	R/W	0h	Data output for DIO27 0h = Output is set to 0 1h = Output is set to 1
26	DIO26	R/W	0h	Data output for DIO26 0h = Output is set to 0 1h = Output is set to 1
25	DIO25	R/W	0h	Data output for DIO25 0h = Output is set to 0 1h = Output is set to 1
24	DIO24	R/W	0h	Data output for DIO24 0h = Output is set to 0 1h = Output is set to 1
23	DIO23	R/W	0h	Data output for DIO23 0h = Output is set to 0 1h = Output is set to 1
22	DIO22	R/W	0h	Data output for DIO22 0h = Output is set to 0 1h = Output is set to 1
21	DIO21	R/W	0h	Data output for DIO21 0h = Output is set to 0 1h = Output is set to 1
20	DIO20	R/W	0h	Data output for DIO20 0h = Output is set to 0 1h = Output is set to 1
19	DIO19	R/W	0h	Data output for DIO19 0h = Output is set to 0 1h = Output is set to 1
18	DIO18	R/W	0h	Data output for DIO18 0h = Output is set to 0 1h = Output is set to 1
17	DIO17	R/W	0h	Data output for DIO17 0h = Output is set to 0 1h = Output is set to 1
16	DIO16	R/W	0h	Data output for DIO16 0h = Output is set to 0 1h = Output is set to 1
15	DIO15	R/W	0h	Data output for DIO15 0h = Output is set to 0 1h = Output is set to 1

Table 22-64. DOUT31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R/W	0h	Data output for DIO14 0h = Output is set to 0 1h = Output is set to 1
13	DIO13	R/W	0h	Data output for DIO13 0h = Output is set to 0 1h = Output is set to 1
12	DIO12	R/W	0h	Data output for DIO12 0h = Output is set to 0 1h = Output is set to 1
11	DIO11	R/W	0h	Data output for DIO11 0h = Output is set to 0 1h = Output is set to 1
10	DIO10	R/W	0h	Data output for DIO10 0h = Output is set to 0 1h = Output is set to 1
9	DIO9	R/W	0h	Data output for DIO9 0h = Output is set to 0 1h = Output is set to 1
8	DIO8	R/W	0h	Data output for DIO8 0h = Output is set to 0 1h = Output is set to 1
7	DIO7	R/W	0h	Data output for DIO7 0h = Output is set to 0 1h = Output is set to 1
6	DIO6	R/W	0h	Data output for DIO6 0h = Output is set to 0 1h = Output is set to 1
5	DIO5	R/W	0h	Data output for DIO5 0h = Output is set to 0 1h = Output is set to 1
4	DIO4	R/W	0h	Data output for DIO4 0h = Output is set to 0 1h = Output is set to 1
3	DIO3	R/W	0h	Data output for DIO3 0h = Output is set to 0 1h = Output is set to 1
2	DIO2	R/W	0h	Data output for DIO2 0h = Output is set to 0 1h = Output is set to 1
1	DIO1	R/W	0h	Data output for DIO1 0h = Output is set to 0 1h = Output is set to 1
0	DIO0	R/W	0h	Data output for DIO0 0h = Output is set to 0 1h = Output is set to 1

22.10.19 DOUTSET31_0 Register (Offset = 210h) [Reset = 00000000h]

DOUTSET31_0 is shown in Table 22-65.

Return to the Summary Table.

Alias regiser to set the corresponding bits of DOUT31_0 register.

Table 22-65. DOUTSET31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Set bit DOUT31_0.DIO30 0h = No effect 1h = Set
29	DIO29	W	0h	Set bit DOUT31_0.DIO29 0h = No effect 1h = Set
28	DIO28	W	0h	Set bit DOUT31_0.DIO28 0h = No effect 1h = Set
27	DIO27	W	0h	Set bit DOUT31_0.DIO27 0h = No effect 1h = Set
26	DIO26	W	0h	Set bit DOUT31_0.DIO26 0h = No effect 1h = Set
25	DIO25	W	0h	Set bit DOUT31_0.DIO25 0h = No effect 1h = Set
24	DIO24	W	0h	Set bit DOUT31_0.DIO24 0h = No effect 1h = Set
23	DIO23	W	0h	Set bit DOUT31_0.DIO23 0h = No effect 1h = Set
22	DIO22	W	0h	Set bit DOUT31_0.DIO22 0h = No effect 1h = Set
21	DIO21	W	0h	Set bit DOUT31_0.DIO21 0h = No effect 1h = Set
20	DIO20	W	0h	Set bit DOUT31_0.DIO20 0h = No effect 1h = Set
19	DIO19	W	0h	Set bit DOUT31_0.DIO19 0h = No effect 1h = Set
18	DIO18	W	0h	Set bit DOUT31_0.DIO18 0h = No effect 1h = Set
17	DIO17	W	0h	Set bit DOUT31_0.DIO17 0h = No effect 1h = Set
16	DIO16	W	0h	Set bit DOUT31_0.DIO16 0h = No effect 1h = Set
15	DIO15	W	0h	Set bit DOUT31_0.DIO15 0h = No effect 1h = Set

Table 22-65. DOUTSET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Set bit DOUT31_0.DIO14 0h = No effect 1h = Set
13	DIO13	W	0h	Set bit DOUT31_0.DIO13 0h = No effect 1h = Set
12	DIO12	W	0h	Set bit DOUT31_0.DIO12 0h = No effect 1h = Set
11	DIO11	W	0h	Set bit DOUT31_0.DIO11 0h = No effect 1h = Set
10	DIO10	W	0h	Set bit DOUT31_0.DIO10 0h = No effect 1h = Set
9	DIO9	W	0h	Set bit DOUT31_0.DIO9 0h = No effect 1h = Set
8	DIO8	W	0h	Set bit DOUT31_0.DIO8 0h = No effect 1h = Set
7	DIO7	W	0h	Set bit DOUT31_0.DIO7 0h = No effect 1h = Set
6	DIO6	W	0h	Set bit DOUT31_0.DIO6 0h = No effect 1h = Set
5	DIO5	W	0h	Set bit DOUT31_0.DIO5 0h = No effect 1h = Set
4	DIO4	W	0h	Set bit DOUT31_0.DIO4 0h = No effect 1h = Set
3	DIO3	W	0h	Set bit DOUT31_0.DIO3 0h = No effect 1h = Set
2	DIO2	W	0h	Set bit DOUT31_0.DIO2 0h = No effect 1h = Set
1	DIO1	W	0h	Set bit DOUT31_0.DIO1 0h = No effect 1h = Set
0	DIO0	W	0h	Set bit DOUT31_0.DIO0 0h = No effect 1h = Set

22.10.20 DOUTCLR31_0 Register (Offset = 220h) [Reset = 00000000h]

DOUTCLR31_0 is shown in Table 22-66.

Return to the Summary Table.

Alias regiser to clear the corresponding bits of DOUT31_0 register.

Table 22-66. DOUTCLR31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Clear bit DOUT31_0.DIO30 0h = No effect 1h = Clear
29	DIO29	W	0h	Clear bit DOUT31_0.DIO29 0h = No effect 1h = Clear
28	DIO28	W	0h	Clear bit DOUT31_0.DIO28 0h = No effect 1h = Clear
27	DIO27	W	0h	Clear bit DOUT31_0.DIO27 0h = No effect 1h = Clear
26	DIO26	W	0h	Clear bit DOUT31_0.DIO26 0h = No effect 1h = Clear
25	DIO25	W	0h	Clear bit DOUT31_0.DIO25 0h = No effect 1h = Clear
24	DIO24	W	0h	Clear bit DOUT31_0.DIO24 0h = No effect 1h = Clear
23	DIO23	W	0h	Clear bit DOUT31_0.DIO23 0h = No effect 1h = Clear
22	DIO22	W	0h	Clear bit DOUT31_0.DIO22 0h = No effect 1h = Clear
21	DIO21	W	0h	Clear bit DOUT31_0.DIO21 0h = No effect 1h = Clear
20	DIO20	W	0h	Clear bit DOUT31_0.DIO20 0h = No effect 1h = Clear
19	DIO19	W	0h	Clear bit DOUT31_0.DIO19 0h = No effect 1h = Clear
18	DIO18	W	0h	Clear bit DOUT31_0.DIO18 0h = No effect 1h = Clear
17	DIO17	W	0h	Clear bit DOUT31_0.DIO17 0h = No effect 1h = Clear
16	DIO16	W	0h	Clear bit DOUT31_0.DIO16 0h = No effect 1h = Clear
15	DIO15	W	0h	Clear bit DOUT31_0.DIO15 0h = No effect 1h = Clear

Table 22-66. DOUTCLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Clear bit DOUT31_0.DIO14 0h = No effect 1h = Clear
13	DIO13	W	0h	Clear bit DOUT31_0.DIO13 0h = No effect 1h = Clear
12	DIO12	W	0h	Clear bit DOUT31_0.DIO12 0h = No effect 1h = Clear
11	DIO11	W	0h	Clear bit DOUT31_0.DIO11 0h = No effect 1h = Clear
10	DIO10	W	0h	Clear bit DOUT31_0.DIO10 0h = No effect 1h = Clear
9	DIO9	W	0h	Clear bit DOUT31_0.DIO9 0h = No effect 1h = Clear
8	DIO8	W	0h	Clear bit DOUT31_0.DIO8 0h = No effect 1h = Clear
7	DIO7	W	0h	Clear bit DOUT31_0.DIO7 0h = No effect 1h = Clear
6	DIO6	W	0h	Clear bit DOUT31_0.DIO6 0h = No effect 1h = Clear
5	DIO5	W	0h	Clear bit DOUT31_0.DIO5 0h = No effect 1h = Clear
4	DIO4	W	0h	Clear bit DOUT31_0.DIO4 0h = No effect 1h = Clear
3	DIO3	W	0h	Clear bit DOUT31_0.DIO3 0h = No effect 1h = Clear
2	DIO2	W	0h	Clear bit DOUT31_0.DIO2 0h = No effect 1h = Clear
1	DIO1	W	0h	Clear bit DOUT31_0.DIO1 0h = No effect 1h = Clear
0	DIO0	W	0h	Clear bit DOUT31_0.DIO0 0h = No effect 1h = Clear

22.10.21 DOUTTGL31_0 Register (Offset = 230h) [Reset = 00000000h]

DOUTTGL31_0 is shown in Table 22-67.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0 register.

Table 22-67. DOUTTGL31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Toggles bit DOUT31_0.DIO30 0h = No effect 1h = Toggle
29	DIO29	W	0h	Toggles bit DOUT31_0.DIO29 0h = No effect 1h = Toggle
28	DIO28	W	0h	Toggles bit DOUT31_0.DIO28 0h = No effect 1h = Toggle
27	DIO27	W	0h	Toggles bit DOUT31_0.DIO27 0h = No effect 1h = Toggle
26	DIO26	W	0h	Toggles bit DOUT31_0.DIO26 0h = No effect 1h = Toggle
25	DIO25	W	0h	Toggles bit DOUT31_0.DIO25 0h = No effect 1h = Toggle
24	DIO24	W	0h	Toggles bit DOUT31_0.DIO24 0h = No effect 1h = Toggle
23	DIO23	W	0h	Toggles bit DOUT31_0.DIO23 0h = No effect 1h = Toggle
22	DIO22	W	0h	Toggles bit DOUT31_0.DIO22 0h = No effect 1h = Toggle
21	DIO21	W	0h	Toggles bit DOUT31_0.DIO21 0h = No effect 1h = Toggle
20	DIO20	W	0h	Toggles bit DOUT31_0.DIO20 0h = No effect 1h = Toggle
19	DIO19	W	0h	Toggles bit DOUT31_0.DIO19 0h = No effect 1h = Toggle
18	DIO18	W	0h	Toggles bit DOUT31_0.DIO18 0h = No effect 1h = Toggle
17	DIO17	W	0h	Toggles bit DOUT31_0.DIO17 0h = No effect 1h = Toggle
16	DIO16	W	0h	Toggles bit DOUT31_0.DIO16 0h = No effect 1h = Toggle
15	DIO15	W	0h	Toggles bit DOUT31_0.DIO15 0h = No effect 1h = Toggle

Table 22-67. DOUTTGL31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Toggles bit DOUT31_0.DIO14 0h = No effect 1h = Toggle
13	DIO13	W	0h	Toggles bit DOUT31_0.DIO13 0h = No effect 1h = Toggle
12	DIO12	W	0h	Toggles bit DOUT31_0.DIO12 0h = No effect 1h = Toggle
11	DIO11	W	0h	Toggles bit DOUT31_0.DIO11 0h = No effect 1h = Toggle
10	DIO10	W	0h	Toggles bit DOUT31_0.DIO10 0h = No effect 1h = Toggle
9	DIO9	W	0h	Toggles bit DOUT31_0.DIO9 0h = No effect 1h = Toggle
8	DIO8	W	0h	Toggles bit DOUT31_0.DIO8 0h = No effect 1h = Toggle
7	DIO7	W	0h	Toggles bit DOUT31_0.DIO7 0h = No effect 1h = Toggle
6	DIO6	W	0h	Toggles bit DOUT31_0.DIO6 0h = No effect 1h = Toggle
5	DIO5	W	0h	Toggles bit DOUT31_0.DIO5 0h = No effect 1h = Toggle
4	DIO4	W	0h	Toggles bit DOUT31_0.DIO4 0h = No effect 1h = Toggle
3	DIO3	W	0h	Toggles bit DOUT31_0.DIO3 0h = No effect 1h = Toggle
2	DIO2	W	0h	Toggles bit DOUT31_0.DIO2 0h = No effect 1h = Toggle
1	DIO1	W	0h	Toggles bit DOUT31_0.DIO1 0h = No effect 1h = Toggle
0	DIO0	W	0h	Toggles bit DOUT31_0.DIO0 0h = No effect 1h = Toggle

22.10.22 DOUTTGL3_0 Register (Offset = 300h) [Reset = 00000000h]

DOUTTGL3_0 is shown in Table 22-68.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[3:0] register.

Table 22-68. DOUTTGL3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO3	W	0h	Toggles bit DOUT31_0.DIO3 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO2	W	0h	Toggles bit DOUT31_0.DIO2 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO1	W	0h	Toggles bit DOUT31_0.DIO1 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO0	W	0h	Toggles bit DOUT31_0.DIO0 0h = No effect 1h = Toggle

22.10.23 DOUTTGL7_4 Register (Offset = 304h) [Reset = 00000000h]

DOUTTGL7_4 is shown in Table 22-69.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[7:4] register.

Table 22-69. DOUTTGL7_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO7	W	0h	Toggles bit DOUT31_0.DIO7 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO6	W	0h	Toggles bit DOUT31_0.DIO6 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO5	W	0h	Toggles bit DOUT31_0.DIO5 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO4	W	0h	Toggles bit DOUT31_0.DIO4 0h = No effect 1h = Toggle

22.10.24 DOUTTGL11_8 Register (Offset = 308h) [Reset = 00000000h]

DOUTTGL11_8 is shown in Table 22-70.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[11:8] register.

Table 22-70. DOUTTGL11_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO11	W	0h	Toggles bit DOUT31_0.DIO11 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO10	W	0h	Toggles bit DOUT31_0.DIO10 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO9	W	0h	Toggles bit DOUT31_0.DIO9 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO8	W	0h	Toggles bit DOUT31_0.DIO8 0h = No effect 1h = Toggle

22.10.25 DOUTTGL15_12 Register (Offset = 30Ch) [Reset = 00000000h]

DOUTTGL15_12 is shown in Table 22-71.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[15:12] register.

Table 22-71. DOUTTGL15_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO15	W	0h	Toggles bit DOUT31_0.DIO15 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO14	W	0h	Toggles bit DOUT31_0.DIO14 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO13	W	0h	Toggles bit DOUT31_0.DIO13 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO12	W	0h	Toggles bit DOUT31_0.DIO12 0h = No effect 1h = Toggle

22.10.26 DOUTTGL19_16 Register (Offset = 310h) [Reset = 00000000h]

DOUTTGL19_16 is shown in Table 22-72.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[19:16] register.

Table 22-72. DOUTTGL19_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO19	W	0h	Toggles bit DOUT31_0.DIO19 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO18	W	0h	Toggles bit DOUT31_0.DIO18 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO17	W	0h	Toggles bit DOUT31_0.DIO17 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO16	W	0h	Toggles bit DOUT31_0.DIO16 0h = No effect 1h = Toggle

22.10.27 DOUTTGL23_20 Register (Offset = 314h) [Reset = 00000000h]

DOUTTGL23_20 is shown in Table 22-73.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[23:20] register.

Table 22-73. DOUTTGL23_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO23	W	0h	Toggles bit DOUT31_0.DIO23 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO22	W	0h	Toggles bit DOUT31_0.DIO22 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO21	W	0h	Toggles bit DOUT31_0.DIO21 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO20	W	0h	Toggles bit DOUT31_0.DIO20 0h = No effect 1h = Toggle

22.10.28 DOUTTGL27_24 Register (Offset = 318h) [Reset = 00000000h]

DOUTTGL27_24 is shown in Table 22-74.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[27:24] register.

Table 22-74. DOUTTGL27_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO27	W	0h	Toggles bit DOUT31_0.DIO27 0h = No effect 1h = Toggle
23-17	RESERVED	R	0h	Reserved
16	DIO26	W	0h	Toggles bit DOUT31_0.DIO26 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO25	W	0h	Toggles bit DOUT31_0.DIO25 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO24	W	0h	Toggles bit DOUT31_0.DIO24 0h = No effect 1h = Toggle

22.10.29 DOUTTGL31_28 Register (Offset = 31Ch) [Reset = 00000000h]

DOUTTGL31_28 is shown in Table 22-75.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOUT31_0[31:28] register.

Table 22-75. DOUTTGL31_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	DIO30	W	0h	Toggles bit DOUT31_0.DIO30 0h = No effect 1h = Toggle
15-9	RESERVED	R	0h	Reserved
8	DIO29	W	0h	Toggles bit DOUT31_0.DIO29 0h = No effect 1h = Toggle
7-1	RESERVED	R	0h	Reserved
0	DIO28	W	0h	Toggles bit DOUT31_0.DIO28 0h = No effect 1h = Toggle

22.10.30 DOE3_0 Register (Offset = 400h) [Reset = 00000000h]

DOE3_0 is shown in Table 22-76.

Return to the Summary Table.

Alias register for byte access to DOE31_0[3:0] bits.

Table 22-76. DOE3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO3	R/W	0h	Data output enable for DIO3 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO2	R/W	0h	Data output enable for DIO2 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO1	R/W	0h	Data output enable for DIO1 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO0	R/W	0h	Data output enable for DIO0 0h = Output disabled 1h = Output enabled

22.10.31 DOE7_4 Register (Offset = 404h) [Reset = 00000000h]

DOE7_4 is shown in Table 22-77.

Return to the Summary Table.

Alias register for byte access to DOE31_0[7:4] bits.

Table 22-77. DOE7_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO7	R/W	0h	Data output enable for DIO7 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO6	R/W	0h	Data output enable for DIO6 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO5	R/W	0h	Data output enable for DIO5 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO4	R/W	0h	Data output enable for DIO4 0h = Output disabled 1h = Output enabled

22.10.32 DOE11_8 Register (Offset = 408h) [Reset = 00000000h]

DOE11_8 is shown in Table 22-78.

Return to the Summary Table.

Alias register for byte access to DOE31_0[11:8] bits.

Table 22-78. DOE11_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO11	R/W	0h	Data output enable for DIO11 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO10	R/W	0h	Data output enable for DIO10 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO9	R/W	0h	Data output enable for DIO9 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO8	R/W	0h	Data output enable for DIO8 0h = Output disabled 1h = Output enabled

22.10.33 DOE15_12 Register (Offset = 40Ch) [Reset = 00000000h]

DOE15_12 is shown in Table 22-79.

Return to the Summary Table.

Alias register for byte access to DOE31_0[15:12] bits.

Table 22-79. DOE15_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO15	R/W	0h	Data output enable for DIO15 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO14	R/W	0h	Data output enable for DIO14 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO13	R/W	0h	Data output enable for DIO13 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO12	R/W	0h	Data output enable for DIO12 0h = Output disabled 1h = Output enabled

22.10.34 DOE19_16 Register (Offset = 410h) [Reset = 00000000h]

DOE19_16 is shown in Table 22-80.

Return to the Summary Table.

Alias register for byte access to DOE31_0[19:16] bits.

Table 22-80. DOE19_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO19	R/W	0h	Data output enable for DIO19 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO18	R/W	0h	Data output enable for DIO18 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO17	R/W	0h	Data output enable for DIO17 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO16	R/W	0h	Data output enable for DIO16 0h = Output disabled 1h = Output enabled

22.10.35 DOE23_20 Register (Offset = 414h) [Reset = 00000000h]

DOE23_20 is shown in Table 22-81.

Return to the Summary Table.

Alias register for byte access to DOE31_0[23:20] bits.

Table 22-81. DOE23_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO23	R/W	0h	Data output enable for DIO23 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO22	R/W	0h	Data output enable for DIO22 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO21	R/W	0h	Data output enable for DIO21 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO20	R/W	0h	Data output enable for DIO20 0h = Output disabled 1h = Output enabled

22.10.36 DOE27_24 Register (Offset = 418h) [Reset = 00000000h]

DOE27_24 is shown in Table 22-82.

Return to the Summary Table.

Alias register for byte access to DOE31_0[24:27] bits.

Table 22-82. DOE27_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO27	R/W	0h	Data output enable for DIO27 0h = Output disabled 1h = Output enabled
23-17	RESERVED	R	0h	Reserved
16	DIO26	R/W	0h	Data output enable for DIO26 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO25	R/W	0h	Data output enable for DIO25 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO24	R/W	0h	Data output enable for DIO24 0h = Output disabled 1h = Output enabled

22.10.37 DOE31_28 Register (Offset = 41Ch) [Reset = 00000000h]

DOE31_28 is shown in Table 22-83.

Return to the Summary Table.

Alias register for byte access to DOE31_0[31:28] bits.

Table 22-83. DOE31_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	DIO30	R/W	0h	Data output enable for DIO30 0h = Output disabled 1h = Output enabled
15-9	RESERVED	R	0h	Reserved
8	DIO29	R/W	0h	Data output enable for DIO29 0h = Output disabled 1h = Output enabled
7-1	RESERVED	R	0h	Reserved
0	DIO28	R/W	0h	Data output enable for DIO28 0h = Output disabled 1h = Output enabled

22.10.38 DOE31_0 Register (Offset = 500h) [Reset = 00000000h]

DOE31_0 is shown in Table 22-84.

Return to the Summary Table.

Data output enable for DIO 31 to 0 pins.

Table 22-84. DOE31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	R/W	0h	Data output enable for DIO30 0h = Output disabled 1h = Output enabled
29	DIO29	R/W	0h	Data output enable for DIO29 0h = Output disabled 1h = Output enabled
28	DIO28	R/W	0h	Data output enable for DIO28 0h = Output disabled 1h = Output enabled
27	DIO27	R/W	0h	Data output enable for DIO27 0h = Output disabled 1h = Output enabled
26	DIO26	R/W	0h	Data output enable for DIO26 0h = Output disabled 1h = Output enabled
25	DIO25	R/W	0h	Data output enable for DIO25 0h = Output disabled 1h = Output enabled
24	DIO24	R/W	0h	Data output enable for DIO24 0h = Output disabled 1h = Output enabled
23	DIO23	R/W	0h	Data output enable for DIO23 0h = Output disabled 1h = Output enabled
22	DIO22	R/W	0h	Data output enable for DIO22 0h = Output disabled 1h = Output enabled
21	DIO21	R/W	0h	Data output enable for DIO21 0h = Output disabled 1h = Output enabled
20	DIO20	R/W	0h	Data output enable for DIO20 0h = Output disabled 1h = Output enabled
19	DIO19	R/W	0h	Data output enable for DIO19 0h = Output disabled 1h = Output enabled
18	DIO18	R/W	0h	Data output enable for DIO18 0h = Output disabled 1h = Output enabled
17	DIO17	R/W	0h	Data output enable for DIO17 0h = Output disabled 1h = Output enabled
16	DIO16	R/W	0h	Data output enable for DIO16 0h = Output disabled 1h = Output enabled
15	DIO15	R/W	0h	Data output enable for DIO15 0h = Output disabled 1h = Output enabled

Table 22-84. DOE31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R/W	0h	Data output enable for DIO14 0h = Output disabled 1h = Output enabled
13	DIO13	R/W	0h	Data output enable for DIO13 0h = Output disabled 1h = Output enabled
12	DIO12	R/W	0h	Data output enable for DIO12 0h = Output disabled 1h = Output enabled
11	DIO11	R/W	0h	Data output enable for DIO11 0h = Output disabled 1h = Output enabled
10	DIO10	R/W	0h	Data output enable for DIO10 0h = Output disabled 1h = Output enabled
9	DIO9	R/W	0h	Data output enable for DIO9 0h = Output disabled 1h = Output enabled
8	DIO8	R/W	0h	Data output enable for DIO8 0h = Output disabled 1h = Output enabled
7	DIO7	R/W	0h	Data output enable for DIO7 0h = Output disabled 1h = Output enabled
6	DIO6	R/W	0h	Data output enable for DIO6 0h = Output disabled 1h = Output enabled
5	DIO5	R/W	0h	Data output enable for DIO5 0h = Output disabled 1h = Output enabled
4	DIO4	R/W	0h	Data output enable for DIO4 0h = Output disabled 1h = Output enabled
3	DIO3	R/W	0h	Data output enable for DIO3 0h = Output disabled 1h = Output enabled
2	DIO2	R/W	0h	Data output enable for DIO2 0h = Output disabled 1h = Output enabled
1	DIO1	R/W	0h	Data output enable for DIO1 0h = Output disabled 1h = Output enabled
0	DIO0	R/W	0h	Data output enable for DIO0 0h = Output disabled 1h = Output enabled

22.10.39 DOESET31_0 Register (Offset = 510h) [Reset = 00000000h]

DOESET31_0 is shown in Table 22-85.

Return to the Summary Table.

Alias regiser to set the corresponding bits of DOE31_0 register.

Table 22-85. DOESET31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Sets bit DOE31_0.DIO30 0h = No effect 1h = Set
29	DIO29	W	0h	Sets bit DOE31_0.DIO29 0h = No effect 1h = Set
28	DIO28	W	0h	Sets bit DOE31_0.DIO28 0h = No effect 1h = Set
27	DIO27	W	0h	Sets bit DOE31_0.DIO27 0h = No effect 1h = Set
26	DIO26	W	0h	Sets bit DOE31_0.DIO26 0h = No effect 1h = Set
25	DIO25	W	0h	Sets bit DOE31_0.DIO25 0h = No effect 1h = Set
24	DIO24	W	0h	Sets bit DOE31_0.DIO24 0h = No effect 1h = Set
23	DIO23	W	0h	Sets bit DOE31_0.DIO23 0h = No effect 1h = Set
22	DIO22	W	0h	Sets bit DOE31_0.DIO22 0h = No effect 1h = Set
21	DIO21	W	0h	Sets bit DOE31_0.DIO21 0h = No effect 1h = Set
20	DIO20	W	0h	Sets bit DOE31_0.DIO20 0h = No effect 1h = Set
19	DIO19	W	0h	Sets bit DOE31_0.DIO19 0h = No effect 1h = Set
18	DIO18	W	0h	Sets bit DOE31_0.DIO18 0h = No effect 1h = Set
17	DIO17	W	0h	Sets bit DOE31_0.DIO17 0h = No effect 1h = Set
16	DIO16	W	0h	Sets bit DOE31_0.DIO16 0h = No effect 1h = Set
15	DIO15	W	0h	Sets bit DOE31_0.DIO15 0h = No effect 1h = Set

Table 22-85. DOESET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Sets bit DOE31_0.DIO14 0h = No effect 1h = Set
13	DIO13	W	0h	Sets bit DOE31_0.DIO13 0h = No effect 1h = Set
12	DIO12	W	0h	Sets bit DOE31_0.DIO12 0h = No effect 1h = Set
11	DIO11	W	0h	Sets bit DOE31_0.DIO11 0h = No effect 1h = Set
10	DIO10	W	0h	Sets bit DOE31_0.DIO10 0h = No effect 1h = Set
9	DIO9	W	0h	Sets bit DOE31_0.DIO9 0h = No effect 1h = Set
8	DIO8	W	0h	Sets bit DOE31_0.DIO8 0h = No effect 1h = Set
7	DIO7	W	0h	Sets bit DOE31_0.DIO7 0h = No effect 1h = Set
6	DIO6	W	0h	Sets bit DOE31_0.DIO6 0h = No effect 1h = Set
5	DIO5	W	0h	Sets bit DOE31_0.DIO5 0h = No effect 1h = Set
4	DIO4	W	0h	Sets bit DOE31_0.DIO4 0h = No effect 1h = Set
3	DIO3	W	0h	Sets bit DOE31_0.DIO3 0h = No effect 1h = Set
2	DIO2	W	0h	Sets bit DOE31_0.DIO2 0h = No effect 1h = Set
1	DIO1	W	0h	Sets bit DOE31_0.DIO1 0h = No effect 1h = Set
0	DIO0	W	0h	Sets bit DOE31_0.DIO0 0h = No effect 1h = Set

22.10.40 DOECLR31_0 Register (Offset = 520h) [Reset = 00000000h]

DOECLR31_0 is shown in Table 22-86.

Return to the Summary Table.

Alias regiser to clear the corresponding bits of DOE31_0 register.

Table 22-86. DOECLR31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Clears bit DOE31_0.DIO30 0h = No effect 1h = Clear
29	DIO29	W	0h	Clears bit DOE31_0.DIO29 0h = No effect 1h = Clear
28	DIO28	W	0h	Clears bit DOE31_0.DIO28 0h = No effect 1h = Clear
27	DIO27	W	0h	Clears bit DOE31_0.DIO27 0h = No effect 1h = Clear
26	DIO26	W	0h	Clears bit DOE31_0.DIO26 0h = No effect 1h = Clear
25	DIO25	W	0h	Clears bit DOE31_0.DIO25 0h = No effect 1h = Clear
24	DIO24	W	0h	Clears bit DOE31_0.DIO24 0h = No effect 1h = Clear
23	DIO23	W	0h	Clears bit DOE31_0.DIO23 0h = No effect 1h = Clear
22	DIO22	W	0h	Clears bit DOE31_0.DIO22 0h = No effect 1h = Clear
21	DIO21	W	0h	Clears bit DOE31_0.DIO21 0h = No effect 1h = Clear
20	DIO20	W	0h	Clears bit DOE31_0.DIO20 0h = No effect 1h = Clear
19	DIO19	W	0h	Clears bit DOE31_0.DIO19 0h = No effect 1h = Clear
18	DIO18	W	0h	Clears bit DOE31_0.DIO18 0h = No effect 1h = Clear
17	DIO17	W	0h	Clears bit DOE31_0.DIO17 0h = No effect 1h = Clear
16	DIO16	W	0h	Clears bit DOE31_0.DIO16 0h = No effect 1h = Clear
15	DIO15	W	0h	Clears bit DOE31_0.DIO15 0h = No effect 1h = Clear

Table 22-86. DOECLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Clears bit DOE31_0.DIO14 0h = No effect 1h = Clear
13	DIO13	W	0h	Clears bit DOE31_0.DIO13 0h = No effect 1h = Clear
12	DIO12	W	0h	Clears bit DOE31_0.DIO12 0h = No effect 1h = Clear
11	DIO11	W	0h	Clears bit DOE31_0.DIO11 0h = No effect 1h = Clear
10	DIO10	W	0h	Clears bit DOE31_0.DIO10 0h = No effect 1h = Clear
9	DIO9	W	0h	Clears bit DOE31_0.DIO9 0h = No effect 1h = Clear
8	DIO8	W	0h	Clears bit DOE31_0.DIO8 0h = No effect 1h = Clear
7	DIO7	W	0h	Clears bit DOE31_0.DIO7 0h = No effect 1h = Clear
6	DIO6	W	0h	Clears bit DOE31_0.DIO6 0h = No effect 1h = Clear
5	DIO5	W	0h	Clears bit DOE31_0.DIO5 0h = No effect 1h = Clear
4	DIO4	W	0h	Clears bit DOE31_0.DIO4 0h = No effect 1h = Clear
3	DIO3	W	0h	Clears bit DOE31_0.DIO3 0h = No effect 1h = Clear
2	DIO2	W	0h	Clears bit DOE31_0.DIO2 0h = No effect 1h = Clear
1	DIO1	W	0h	Clears bit DOE31_0.DIO1 0h = No effect 1h = Clear
0	DIO0	W	0h	Clears bit DOE31_0.DIO0 0h = No effect 1h = Clear

22.10.41 DOETGL31_0 Register (Offset = 530h) [Reset = 00000000h]

DOETGL31_0 is shown in Table 22-87.

Return to the Summary Table.

Alias regiser to toggle the corresponding bits of DOE31_0 register.

Table 22-87. DOETGL31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	W	0h	Toggles bit DOE31_0.DIO30 0h = No effect 1h = Toggle
29	DIO29	W	0h	Toggles bit DOE31_0.DIO29 0h = No effect 1h = Toggle
28	DIO28	W	0h	Toggles bit DOE31_0.DIO28 0h = No effect 1h = Toggle
27	DIO27	W	0h	Toggles bit DOE31_0.DIO27 0h = No effect 1h = Toggle
26	DIO26	W	0h	Toggles bit DOE31_0.DIO26 0h = No effect 1h = Toggle
25	DIO25	W	0h	Toggles bit DOE31_0.DIO25 0h = No effect 1h = Toggle
24	DIO24	W	0h	Toggles bit DOE31_0.DIO24 0h = No effect 1h = Toggle
23	DIO23	W	0h	Toggles bit DOE31_0.DIO23 0h = No effect 1h = Toggle
22	DIO22	W	0h	Toggles bit DOE31_0.DIO22 0h = No effect 1h = Toggle
21	DIO21	W	0h	Toggles bit DOE31_0.DIO21 0h = No effect 1h = Toggle
20	DIO20	W	0h	Toggles bit DOE31_0.DIO20 0h = No effect 1h = Toggle
19	DIO19	W	0h	Toggles bit DOE31_0.DIO19 0h = No effect 1h = Toggle
18	DIO18	W	0h	Toggles bit DOE31_0.DIO18 0h = No effect 1h = Toggle
17	DIO17	W	0h	Toggles bit DOE31_0.DIO17 0h = No effect 1h = Toggle
16	DIO16	W	0h	Toggles bit DOE31_0.DIO16 0h = No effect 1h = Toggle
15	DIO15	W	0h	Toggles bit DOE31_0.DIO15 0h = No effect 1h = Toggle

Table 22-87. DOETGL31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	Toggles bit DOE31_0.DIO14 0h = No effect 1h = Toggle
13	DIO13	W	0h	Toggles bit DOE31_0.DIO13 0h = No effect 1h = Toggle
12	DIO12	W	0h	Toggles bit DOE31_0.DIO12 0h = No effect 1h = Toggle
11	DIO11	W	0h	Toggles bit DOE31_0.DIO11 0h = No effect 1h = Toggle
10	DIO10	W	0h	Toggles bit DOE31_0.DIO10 0h = No effect 1h = Toggle
9	DIO9	W	0h	Toggles bit DOE31_0.DIO9 0h = No effect 1h = Toggle
8	DIO8	W	0h	Toggles bit DOE31_0.DIO8 0h = No effect 1h = Toggle
7	DIO7	W	0h	Toggles bit DOE31_0.DIO7 0h = No effect 1h = Toggle
6	DIO6	W	0h	Toggles bit DOE31_0.DIO6 0h = No effect 1h = Toggle
5	DIO5	W	0h	Toggles bit DOE31_0.DIO5 0h = No effect 1h = Toggle
4	DIO4	W	0h	Toggles bit DOE31_0.DIO4 0h = No effect 1h = Toggle
3	DIO3	W	0h	Toggles bit DOE31_0.DIO3 0h = No effect 1h = Toggle
2	DIO2	W	0h	Toggles bit DOE31_0.DIO2 0h = No effect 1h = Toggle
1	DIO1	W	0h	Toggles bit DOE31_0.DIO1 0h = No effect 1h = Toggle
0	DIO0	W	0h	Toggles bit DOE31_0.DIO0 0h = No effect 1h = Toggle

22.10.42 DIN3_0 Register (Offset = 600h) [Reset = 00000000h]

DIN3_0 is shown in Table 22-88.

Return to the Summary Table.

Alias register for byte access to DIN31_0[3:0] bits.

Table 22-88. DIN3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO3	R	0h	Data input from DIO3 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO2	R	0h	Data input from DIO2 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO1	R	0h	Data input from DIO1 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO0	R	0h	Data input from DIO0 0h = Input value is 0 1h = Input value is 1

22.10.43 DIN7_4 Register (Offset = 604h) [Reset = 00000000h]

DIN7_4 is shown in Table 22-89.

Return to the Summary Table.

Alias register for byte access to DIN31_0[7:4] bits.

Table 22-89. DIN7_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO7	R	0h	Data input from DIO7 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO6	R	0h	Data input from DIO6 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO5	R	0h	Data input from DIO5 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO4	R	0h	Data input from DIO4 0h = Input value is 0 1h = Input value is 1

22.10.44 DIN11_8 Register (Offset = 608h) [Reset = 00000000h]

DIN11_8 is shown in Table 22-90.

Return to the Summary Table.

Alias register for byte access to DIN31_0[11:8] bits.

Table 22-90. DIN11_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO11	R	0h	Data input from DIO11 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO10	R	0h	Data input from DIO10 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO9	R	0h	Data input from DIO9 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO8	R	0h	Data input from DIO8 0h = Input value is 0 1h = Input value is 1

22.10.45 DIN15_12 Register (Offset = 60Ch) [Reset = 00000000h]

DIN15_12 is shown in Table 22-91.

Return to the Summary Table.

Alias register for byte access to DIN31_0[15:12] bits.

Table 22-91. DIN15_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO15	R	0h	Data input from DIO15 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO14	R	0h	Data input from DIO14 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO13	R	0h	Data input from DIO13 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO12	R	0h	Data input from DIO12 0h = Input value is 0 1h = Input value is 1

22.10.46 DIN19_16 Register (Offset = 610h) [Reset = 00000000h]

DIN19_16 is shown in Table 22-92.

Return to the Summary Table.

Alias register for byte access to DIN31_0[19:16] bits.

Table 22-92. DIN19_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO19	R	0h	Data input from DIO19 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO18	R	0h	Data input from DIO18 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO17	R	0h	Data input from DIO17 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO16	R	0h	Data input from DIO16 0h = Input value is 0 1h = Input value is 1

22.10.47 DIN23_20 Register (Offset = 614h) [Reset = 00000000h]

DIN23_20 is shown in Table 22-93.

Return to the Summary Table.

Alias register for byte access to DIN31_0[23:20] bits.

Table 22-93. DIN23_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO23	R	0h	Data input from DIO23 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO22	R	0h	Data input from DIO22 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO21	R	0h	Data input from DIO21 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO20	R	0h	Data input from DIO20 0h = Input value is 0 1h = Input value is 1

22.10.48 DIN27_24 Register (Offset = 618h) [Reset = 00000000h]

DIN27_24 is shown in Table 22-94.

Return to the Summary Table.

Alias register for byte access to DIN31_0[24:27] bits.

Table 22-94. DIN27_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	DIO27	R	0h	Data input from DIO27 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	Reserved
16	DIO26	R	0h	Data input from DIO26 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO25	R	0h	Data input from DIO25 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO24	R	0h	Data input from DIO24 0h = Input value is 0 1h = Input value is 1

22.10.49 DIN31_28 Register (Offset = 61Ch) [Reset = 00000000h]

DIN31_28 is shown in Table 22-95.

Return to the Summary Table.

Alias register for byte access to DIN31_0[31:28] bits.

Table 22-95. DIN31_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	DIO30	R	0h	Data input from DIO30 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	Reserved
8	DIO29	R	0h	Data input from DIO29 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	Reserved
0	DIO28	R	0h	Data input from DIO28 0h = Input value is 0 1h = Input value is 1

22.10.50 DIN31_0 Register (Offset = 700h) [Reset = 00000000h]

DIN31_0 is shown in Table 22-96.

Return to the Summary Table.

Data input from DIO 31 to 0 pins.

Table 22-96. DIN31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	DIO30	R	0h	Data input from DIO30 0h = Input value is 0 1h = Input value is 1
29	DIO29	R	0h	Data input from DIO29 0h = Input value is 0 1h = Input value is 1
28	DIO28	R	0h	Data input from DIO28 0h = Input value is 0 1h = Input value is 1
27	DIO27	R	0h	Data input from DIO27 0h = Input value is 0 1h = Input value is 1
26	DIO26	R	0h	Data input from DIO26 0h = Input value is 0 1h = Input value is 1
25	DIO25	R	0h	Data input from DIO25 0h = Input value is 0 1h = Input value is 1
24	DIO24	R	0h	Data input from DIO24 0h = Input value is 0 1h = Input value is 1
23	DIO23	R	0h	Data input from DIO23 0h = Input value is 0 1h = Input value is 1
22	DIO22	R	0h	Data input from DIO22 0h = Input value is 0 1h = Input value is 1
21	DIO21	R	0h	Data input from DIO21 0h = Input value is 0 1h = Input value is 1
20	DIO20	R	0h	Data input from DIO20 0h = Input value is 0 1h = Input value is 1
19	DIO19	R	0h	Data input from DIO19 0h = Input value is 0 1h = Input value is 1
18	DIO18	R	0h	Data input from DIO18 0h = Input value is 0 1h = Input value is 1
17	DIO17	R	0h	Data input from DIO17 0h = Input value is 0 1h = Input value is 1
16	DIO16	R	0h	Data input from DIO16 0h = Input value is 0 1h = Input value is 1
15	DIO15	R	0h	Data input from DIO15 0h = Input value is 0 1h = Input value is 1

Table 22-96. DIN31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R	0h	Data input from DIO14 0h = Input value is 0 1h = Input value is 1
13	DIO13	R	0h	Data input from DIO13 0h = Input value is 0 1h = Input value is 1
12	DIO12	R	0h	Data input from DIO12 0h = Input value is 0 1h = Input value is 1
11	DIO11	R	0h	Data input from DIO11 0h = Input value is 0 1h = Input value is 1
10	DIO10	R	0h	Data input from DIO10 0h = Input value is 0 1h = Input value is 1
9	DIO9	R	0h	Data input from DIO9 0h = Input value is 0 1h = Input value is 1
8	DIO8	R	0h	Data input from DIO8 0h = Input value is 0 1h = Input value is 1
7	DIO7	R	0h	Data input from DIO7 0h = Input value is 0 1h = Input value is 1
6	DIO6	R	0h	Data input from DIO6 0h = Input value is 0 1h = Input value is 1
5	DIO5	R	0h	Data input from DIO5 0h = Input value is 0 1h = Input value is 1
4	DIO4	R	0h	Data input from DIO4 0h = Input value is 0 1h = Input value is 1
3	DIO3	R	0h	Data input from DIO3 0h = Input value is 0 1h = Input value is 1
2	DIO2	R	0h	Data input from DIO2 0h = Input value is 0 1h = Input value is 1
1	DIO1	R	0h	Data input from DIO1 0h = Input value is 0 1h = Input value is 1
0	DIO0	R	0h	Data input from DIO0 0h = Input value is 0 1h = Input value is 1

22.10.51 EVTCFG Register (Offset = 800h) [Reset = 00000000h]

EVTCFG is shown in Table 22-97.

Return to the Summary Table.

Event configuration 0. This register is used to select DIO for GPIO to publish event on SVT event fabric. It also contains enable bit that is used to mask the event.

Table 22-97. EVTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	EVTEN	R/W	0h	Enables GPIO to publish edge qualified selected DIO event on SVT event fabric. ;Design note: The edge detector flop is cleared automatically for the selected DIO once the event is published. 0h = Disable 1h = Enable
7-6	RESERVED	R	0h	Reserved
5-0	DIOSEL	R/W	0h	This is used to select DIO for event generation. For example, DIOSEL = 0x0 selects DIO0 and DIOSEL = 0x8 selects DIO8. 0h = Minimum value 3Fh = Maximum value

22.10.52 EVTCFG1 Register (Offset = 810h) [Reset = 00000000h]

EVTCFG1 is shown in Table 22-98.

Return to the Summary Table.

Event configuration 1. This register is used to select DIO for GPIO to publish event on SVT event fabric. It also contains enable bit that is used to mask the event.

Table 22-98. EVTCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	EVTEN	R/W	0h	Enables GPIO to publish edge qualified selected DIO event on SVT event fabric. ;Design note: The edge detector flop is cleared automatically for the selected DIO once the event is published. 0h = Disable 1h = Enable
7-6	RESERVED	R	0h	Reserved
5-0	DIOSEL	R/W	0h	This is used to select DIO for event generation. For example, DIOSEL = 0x0 selects DIO0 and DIOSEL = 0x8 selects DIO8. 0h = Minimum value 3Fh = Maximum value

Chapter 23

Universal Asynchronous Receiver/Transmitter (UART-LIN)

This chapter describes the features and functions of the Universal Asynchronous Receiver/Transmitter (UART-LIN).

23.1 Introduction

The UART-LIN supports the following features:

- Programmable baud rate generator allowing speeds up to 3Mbps
- Separate 8 × 8 transmit (TX) and 8 × 12 receive (RX) first-in first-out (FIFO) buffers to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of ¼, ½, ¾.
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity bit generation and detection
  - 1 or 2 stop-bit generation
- FIFO, RX FIFO RX time-out, modem status, and error conditions
- Standard FIFO-level and end-of-transmission interrupts
- Efficient transfers using micro direct memory access controller (µDMA):
  - Separate channels for transmit and receive.
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level.
  - Transmit single request is asserted when there is space in the FIFO; burst request is asserted at programmed FIFO level.
- Programmable hardware flow control
- Support for standard IrDA and low power IrDA modes.
- Provision to combine both TX and RX FIFOs in transmit mode.
- LIN protocol and features for data transmission and reception.
- In case of transmit operation, it support generation of break or break and synch fields.
- It generate break field with 13 bits (zeros) followed by delimiter and synch field with value 0x55.
- In case of receive operation, it detect break field and is able to automatically update baud rate based on synch field.
- TXBRK control bit is used for generation of wake up signal on LIN bus.
- There shall is a control bit for transmission of break and synch fields (TXBRKSYNC).
- The control bits for break (TXBRK) and break/synch transmission (TXBRKSYNC) in LIN mode are automatically reset after transmission of break and break/synch fields respectively.
- Configuration bits to generate delimiter bit times of 1, 2, 3 and 4 (DELIMx).
- Configuration bit to enable automatic baud rate detection (ABDEN).
- Detect break field when 11 or more zeros are received.
- Generate break flag (LINBRK) when break field is successfully received.
- The break flag will be cleared by hardware when the data register is read.
- Generate break time out error flag (LINBTOE) when break field length exceeds 22 bit times.
- Generate synch time out error flag (LINSTOE) when length of synch field exceeds measurable time.
- When dormant mode is disabled, break and synch data are loaded to RX FIFO and associated interrupt flags shall be set as in normal UART operation.
- When dormant mode is enabled, break and synch data are not be loaded to RX FIFO and RX FIFO shall be updated with actual data (PID) only after successful reception of break/synch fields.
- When automatic baud rate detection is enabled, the minimum baud rate to be supported is 50 baud and maximum baud rate to be supported is 3M baud. LIN communication speed: 1kbps to 20kbps.
- Support proper reception of data while break or break/synch fields are transmitted (master role).
- Support transmission of data while receiving break/synch fields but transmission baud rate can change potentially due to automatic baud rate adjustment (slave role).
- UART is configured by software with 8 bit data, LSB first, no parity and 1 stop bit for operation in LIN mode.

23.2 Block Diagram

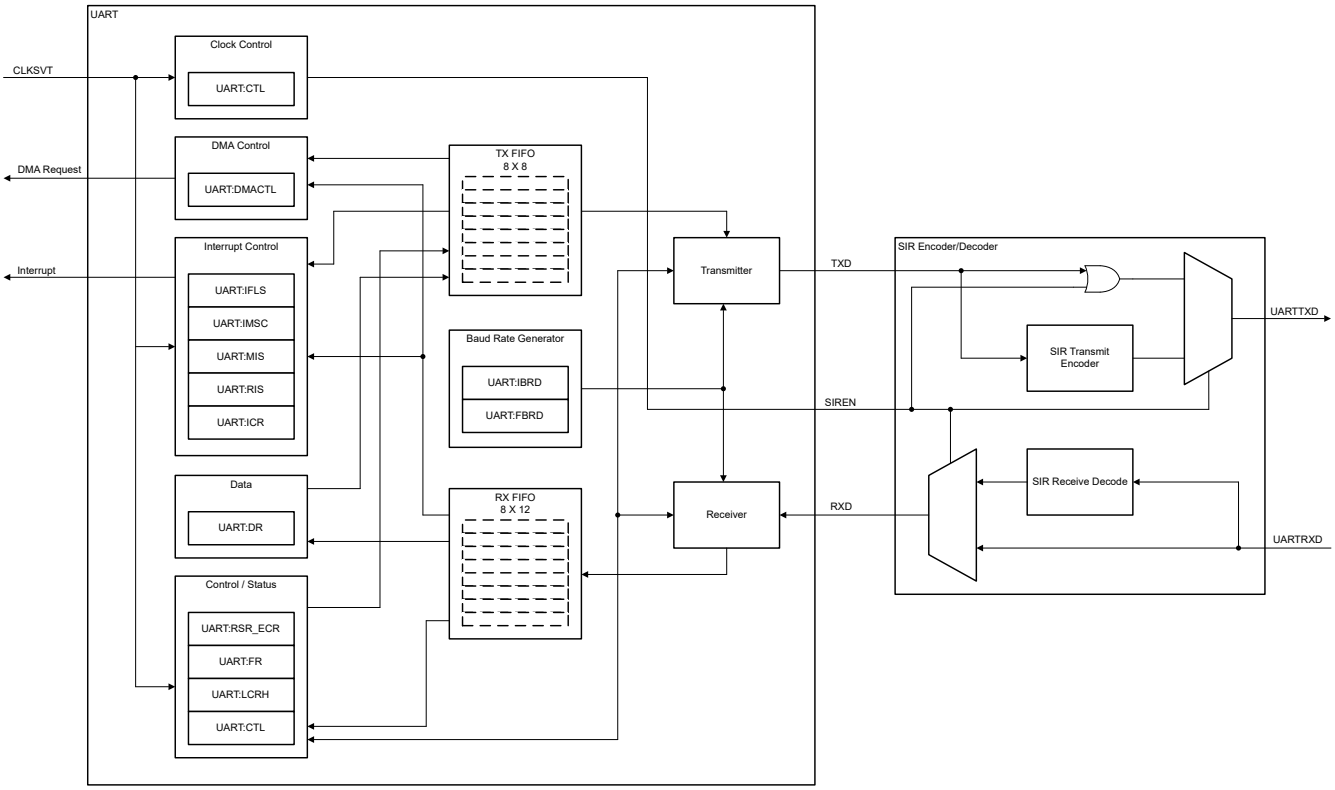

Figure 23-1. UART Block Diagram

23.3 UART Functional Description

The CC27XX UART performs the functions of parallel-to-serial and serial-to-parallel conversions. The CC27XX UART is similar in functionality to a 16C550 UART, but is not register compatible. The UART is configured for transmit and receive through the UART Control Register (UART:CTL) TXE and RXE bits. Transmit and receive are both enabled out of reset. Before any control registers are programmed, the UART must be disabled by clearing the UART:CTL UARTEN register bit. If the UART is disabled during a transmit or receive operation, the current transaction completes before the UART stops.

23.3.1 Transmit and Receive Logic

The transmit logic performs parallel-to-serial conversion on the data read from the TX FIFO. The control logic outputs the serial bit stream beginning with a start bit and followed by the data bits (LSB first), parity bit, and the stop bits, according to the programmed configuration in the control registers. For details, see Figure 23-2

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse is detected. Overrun, parity, frame error checking, and line-break detection are also performed, and their status accompanies the data written to the RX FIFO.

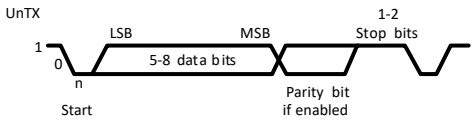

Figure 23-2. UART Character Frame

23.3.2 Baud Rate Generation

The baud rate divisor (BRD) is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part. The number formed by these two values is used by the baud rate generator to determine the bit period. Having a fractional baud rate divider allows the UART to generate all standard baud rates.

The 16-bit integer is loaded through the UART Integer Baud Rate Divisor Register (UART.IBRD), and the 6-bit fractional part is loaded with the UART Fractional Baud Rate Divisor Register (UART.FBRD).

Equation 5 shows the relationship of the BRD and the system clock.

$$BRD = BRDI + BRDF = CLKSVT / (ClkDiv \times Baud\ Rate) \quad (5)$$

where:

- BRDI is the integer part of the BRD
- BRDF is the fractional part, separated by a decimal place
- CLKSVT is the system clock connected to the UART
- ClkDiv is 16

The 6-bit fractional number that is loaded into the UART:FBRD.DIVFRAC bit field can be calculated by taking the fractional part of the baud rate divisor, multiplying by 64, and adding 0.5 to account for rounding errors, as shown by Equation 6

$$UART.FBRD[5:0]\ DIVFRAC = integer\ (BRDF \times 64 + 0.5) \quad (6)$$

Along with the UART Line Control High Byte Register (UART.LCRH), the UART.IBRD and the UART.FBRD registers form an internal 30-bit register. This internal register is updated only when a write operation to the UART.LCRH register is performed, so a write to the UART.LCRH register must follow any changes to the BRD for the changes to take effect.

The four possible sequences to update the baud-rate registers are as follows:

- UART.IBRD write, UART.FBRD write, and UART.LCRH write
- UART.FBRD write, UART.IBRD write, and UART.LCRH write
- UART.IBRD write and UART.LCRH write
- UART.FBRD write and UART.LCRH write

For an example calculation see Section 23.6.

23.3.3 FIFO Operation

The UART has two 8-entry FIFOs. One FIFO for transmit and one FIFO for receive. Both FIFOs are accessed through the UART Data Register, UART.DR. Read operations of the UART.DR register return a 12-bit value consisting of 8 data bits and 4 error flags, while write operations place 8-bit data in the TX FIFO.

Out of reset, both FIFOs are disabled and act as 1-byte-deep holding registers. The FIFOs are enabled by setting the UART.LCRH[4] FEN bit.

FIFO status can be monitored through the UART Flag Register, UART.FR and the UART Receive Status Register, UART.RSR_ECR. Hardware monitors empty, full, and overrun conditions. The UART.FR register contains empty and full flags (TXFE, TXFF, RXFE, and RXFF bits), and the UART.RSR_ECR register shows overrun status through the OE bit. If the FIFOs are disabled, the empty and full flags are set according to the status of the 1-byte deep holding registers.

The trigger points at which the FIFOs generate interrupts are controlled through the UART Interrupt FIFO Level Select Register (UART:IFLS). Both FIFOs can be individually configured to trigger interrupts at different levels. Available configurations include ¼, ½ and ¾. For example, if the ¼ option is selected for the receive FIFO, the UART generates a receive interrupt after 4 data bytes are received. Out of reset, both FIFOs are configured to trigger an interrupt at the ½ mark.

23.3.3.1 FIFO Remapping

The UART supports concatenation of TX and RX FIFOs in TX only mode - leading to 16 TX entries. Remapping and concatenation for RX only mode is not supported. This mode is enabled by setting the UART.CTL[6] FCEN bit to 1.

23.3.4 Data Transmission

Data received or transmitted is stored in two FIFOs, though the RX FIFO has an extra 4 bits per character for status information. For transmission, data is written into the TX FIFO. If the UART is enabled, a dataframe starts transmitting with the parameters indicated in the UART.LCRH register. Data transmission continues until no data is left in the TX FIFO. The UART Flag Register (UART.FR) BUSY bit is asserted as soon as data is written to the TX FIFO (that is, if the FIFO is not empty), and remains asserted while data is transmitting. The BUSY bit is negated only when the TX FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. The UART can indicate that it is busy even if the UART is no longer be enabled.

When the receiver is idle (the UARTRXD signal is continuously 1), and the data input goes low (a start bit was received), the receive counter begins running and data is sampled.

The start bit is valid and recognized if the UARTRXD signal is still low on the eighth cycle of the baud rate clock otherwise the start bit is ignored. After a valid start bit is detected, successive data bits are sampled on every sixteenth cycle of the baud rate clock. The parity bit is then checked if parity mode is enabled. Data length and parity are defined in the UART:LCRH register.

Lastly, a valid stop bit is confirmed if the UARTRXD signal is high; otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO with any error bits associated with that word.

23.3.5 Flow Control

Flow control can be accomplished by hardware and the following sections describe the implementation method. Hardware flow control between two devices is accomplished by connecting the RTS (Request-to-send) output to the CTS (Clear-to-send) input on the receiving device, and connecting the RTS output on the receiving device to the CTS input. The RTS output signal is low active, the CTS input expects a low signal on a send request as shown in Figure 23-3.

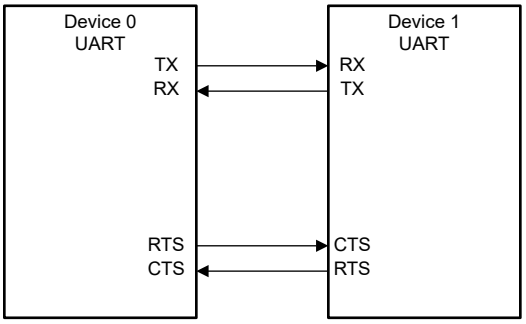

Figure 23-3. UART Flow Control

The CTS input controls the transmitter, the Device 0 and Device 1 transmitter can only transmit data when their CTS input is asserted low. When RTS flow control is enabled, the RTS output signal indicates the state of the receive FIFO. For example, the CTS of the Device 1 remains asserted low until the preprogrammed RX FIFO level of Device 0 is reached, indicating that the receive FIFO of Device 0 has no space to store additional characters.

The UART:CTL register bits CTSEN and RTSEN specify the flow control mode as shown in following table.

CTSEN	RTSEN	Description
1	1	RTS and CTS flow control enabled
1	0	Only CTS flow control enabled
0	1	Only RTS flow control enabled

0	0	RTS and CTS flow control disabled

When RTSEN is set to 1, the value of the UART:CTL.RTS bit is ignored and the RTS output signal is generated by the hardware trigger levels as described below. When RTSEN bit is cleared, the RTS signal output is controlled by the UART:CTL.RTS bit for SW control.

RTS Flow Control

The RTS flow control logic is linked to the programmable receive FIFO trigger levels. The trigger level can be configured using the UART.IFLS register. When RTS flow control is enabled, the RTS is asserted (low) until the receive FIFO is filled up to the trigger level. When the receive FIFO trigger level is reached, the RTS signal is de-asserted (high), indicating that there is no more room to receive any more data. The transmission of data is expected to cease after the current character has been transmitted. The RTS signal is reasserted (low) when data has been read out of the receive FIFO so that the FIFO is filled to less than the trigger level. If RTS flow control is disabled and the UART is still enabled, then data is received until the receive FIFO is full, or no more data is transmitted.

The RTS signal is de-asserted when the FIFO trigger level is reached by putting the last received character into the FIFO. This means that on a back-to-back transmit, another character transfer can already be started by the sender prior to the RTS signal be de-asserted. In such cases the trigger level needs to be set to one level lower so that all data can be received and added into the FIFO.

CTS Flow Control

If CTS flow control is enabled, then the transmitter checks the CTS signal before transmitting the next byte. If the CTS signal is asserted (low), it transmits the byte otherwise transmission does not occur. The data continues to be transmitted while CTS is asserted (low), and the transmit FIFO is not empty. If the transmit FIFO is empty and the CTS signal is asserted (low) no data is transmitted. If the CTS signal is de-asserted (high) and CTS flow control is enabled, then the current character transmission is completed before stopping. If CTS flow control is disabled and the UART is enabled, then the data continues to be transmitted until the transmit FIFO is empty.

Software Flow Control

Software flow control between two devices is accomplished by using interrupts to indicate the status of the UART. Interrupts can be generated for the CTS signal by setting the UART.IMSC[1] CTSMIM bit. The raw and masked interrupt status can be checked using the UART.RIS and UART.MIS registers. These interrupts can be cleared using the UART.ICR register.

23.3.6 IrDA Encoding and Decoding

When the UART.CTL[1] SIREN bit is set, the IrDA (SIR) encoder and decoder are enabled and provide hardware bit shaping for IrDA communication. In this protocol, from the transmitter perspective, a zero is transmitted as a high pulse and a one is transmitted as a zero.

The width of the pulse is specified as 3/16th of the selected bit period. The SIR decoder converts the IrDA compliant receive signal into a bit stream for the UART core. The SIR receive logic interprets a high state as a logic one and low pulses as logic zeros. For more details please refer to the SIR Physical Layer Link Specification Version 1.1

Setting the UART.CTL SIRLP[2] bit enables low power mode. In the low power mode, the width of the pulse is set to 3 times the time period of the IrLPBaud16 signal. The IrLPBaud16 signal is generated by dividing down the CLKSVT (48MHz) according to the low-power divisor value written to the UARTILPR register. The low-power divisor value is calculated as follows:

low-power divisor (ILPDVSR) = (CLKSVT / (FIrLPBaud16 * 3)) (7)

where FIrLPBaud16 is nominally 1.8432 MHz.

The divisor must be selected such that 1.42 MHz < FIrLPBaud16 < 2.12 MHz, results in a low-power pulse duration of 1.41-2.11µs (three times the period of IrLPBaud16).

Note

In low-power IrDA mode the UART rejects random noise on the received serial data input by ignoring SIRIN pulses that are less than 3 periods of IrLPBaud16.

The time period of the nSIROUT bit stream is still equal to the programmed bit period and is governed by the period of the Baud16 signal.

In the low power mode, there is an upper limit on the allowable bit rate if the integrity of the IrDA pulse stream is to be maintained. The upper limit is determined by the requirement that the width of 3 times the period of the IrLPBaud16 signal is less than one bit period. With a nominal IrLPBaud16 frequency of 2 MHz, this translates to a maximum allowable baud rate of 666.6 Kbps. This is not a problem since the specification states that the UART is to support bit rates of only up to 115.2 Kbps for the SIR endec.

If the low power mode of the IrDA is used, there is also a lower limit on the frequency of CLKSVT. The reload value for the IrLPBaud16 counter can be a minimum of 1. Given that IrLPBaud16 needs to have a minimum frequency of 1.42 MHz to satisfy IrDA requirements, CLKSVT needs to be at least 1.42 MHz to meet the minimum pulse width requirement. In the case of transmission, the IrLPBaud16 signal is used to control the width of the transmit pulse stream only in the low power mode. On the other hand, in the case of reception, the IrLPBaud16 signal is used to sample the pulses in the input SIRIN stream both in the normal mode and in the low power mode. Thus, the IrLPBaud16 signal is generated irrespective of whether the IrDA section is programmed to operate in the normal mode or in the low power mode but the signal is not generated when both IrDA modes are disabled.

The SIR receiver section contains a 4-bit binary counter, which operates on CLKSVT in the normal mode with the Baud16 signal as an enable signal. When the input SIRIN signal is high, the decoded output signal, RXD, is driven high to indicate a 1. A low on the SIRIN line is sampled multiple times on IrLPBaud16 for glitch rejection and converted into a low on the RXD line. The time period for which the RXD line is pulled low corresponds to approximately one bit period at the programmed bit rate. After the counter rolls over, input sampling restarts. The SIRLPSync signal is the CLKSVT-synchronised version of the SIRLP mode selection bit in the UART.CTL register. This signal determines the IrDA encoding strategy i.e. whether the IrDA transmitter block is to operate in the normal mode or in the low power mode. The SIRENSync signal is the SIREN bit in the UART.CTL register, which has been synchronised to CLKSVT. This signal enables / disables the SIR section.

23.3.7 Interrupts

The UART can generate interrupts when the following conditions are observed:

- Overrun error
- Break error
- Parity error
- Framing error
- Receive time-out
- Transmit (when the condition defined in the UART:IFLS TXSEL register bit is met)
- Receive (when the condition defined in the UART:IFLS RXSEL register bit is met)
- End of transmission (when no data on TX line and TX FIFO underflow
- RX DMA Done
- TX DMA Done

All of the interrupt events are ORed together before being sent to the MCU event fabric, so the UART can only generate a single interrupt request at any given time. Software can service multiple interrupt events in a single interrupt service routine (ISR) by reading the UART Masked Interrupt Status Register (UART.MIS).

The interrupt events that can trigger a controller-level interrupt are defined in the UART Interrupt Mask Register (UART.IMSC) by setting the corresponding bits. If interrupts are not used, the raw interrupt status is always visible through the UART Raw Interrupt Status Register (UART.RIS).

Interrupts can be cleared (for the UART.MIS and UART.RIS registers) by setting the corresponding bit in the UART Interrupt Clear Register (UART.ICR).

The receive time-out interrupt is asserted when the RX FIFO is not empty, and no further data is received over a 32-bit period. The receive time-out interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when the corresponding bit in the UART.ICR register is set.

The UART module provides the possibility of setting and clearing masks for every individual interrupt source using the UART Interrupt Mask Set/Clear Register (UART.IMSC). The five events that can cause combined interrupts to CPU are:

- RX: The receive interrupt changes state when one of the following events occurs:
  - If the FIFOs are enabled and the receive FIFO reaches the programmed trigger level. When this happens, the receive interrupt is asserted high. The receive interrupt is cleared by reading data from the receive FIFO until it becomes less than the trigger level, or by clearing the interrupt.
  - If the FIFOs are disabled (have a depth of one location) and data is received, thereby filling the location, the receive interrupt is asserted high. The receive interrupt is cleared by performing a single read of the receive FIFO, or by clearing the interrupt.
- TX: The transmit interrupt changes state when one of the following events occurs:
  - If the FIFOs are enabled and the transmit FIFO is equal to or lower than the programmed trigger level, then the transmit interrupt is asserted high. The transmit interrupt is cleared by writing data to the transmit FIFO until it becomes greater than the trigger level, or by clearing the interrupt.
  - If the FIFOs are disabled (have a depth of one location) and there is no data present in the transmitters single location, the transmit interrupt is asserted high. The interrupt is cleared by performing a single write to the transmit FIFO, or by clearing the interrupt.
- RX time-out: The receive time-out interrupt is asserted when the receive FIFO is not empty, and no more data is received during a 32-bit period. The receive time-out interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when 1 is written to the corresponding bit of the Interrupt Clear Register (UART:ICR).
- Modem status: The modem status interrupt is asserted if the modem status signal CTS toggles. It can be cleared using the corresponding clear bit in the UART.ICR register.
- Error: The error interrupt is asserted when an error occurs in the reception of data by the UART. The interrupt can be caused by a number of different error conditions:
  - framing
  - parity
  - break
  - overrun

The cause of the interrupt can be determined by reading the UART.RIS register or the UART.MIS register. The interrupt can be cleared by writing to the relevant bits of the UART.ICR register.

In addition to the five events produced by the UART module, two additional events are ORed to the interrupt line:

- RX DMA done: Indicates that the receiver µDMA task has completed. This is a level interrupt provided by the µDMA module
- TX DMA done: Indicates that the transmit µDMA task has completed. This is a level interrupt provided by the µDMA module

23.3.8 Loopback Operation

The UART can be placed into an internal loopback mode for diagnostic or debug work by setting the UART:CTL.LBE register bit. In loopback mode, data transmitted on the UARTTXD output is received on the UARTRXD input. The LBE bit must be set before the UART is enabled.

23.4 UART-LIN Specification

23.4.1 Break transmission in UART mode

- When TXBRK is set in LCRH and UART is idle, TXD pin is driven low and kept low until SW clears TXBRK bit.
- When TXBRK is set when transmission is active, ongoing data packet will be sent out and thenTXD pin is driven low and kept low until TXBRK is cleared by SW.
- If TXFIFO contains data, transmission will resume once TXBRK is cleared by SW.
- SW recommendation is to keep TXBRK set for two times the length of data packet for proper break operation.

23.4.2 Break reception in UART mode

- When RXD goes low, counter is started with preload value equal to length of data packet (start + data + parity + stop).
- Slave baud rate setting will be used to define bit time.
- If RXD goes high before counter expires, counter is cleared and break condition is ignored.
- If RXD is low until counter expires, break error condition is detected (set BE flag) and value 0 is moved to RX FIFO.

23.4.3 Break/Synch transmission in LIN mode

- UART and LIN modes have to be enabled.
- Master baud rate and desired delimiter value should be configured by SW.
- SW needs to set TXBRKSYNC bit in LCRH for break/synch transmission (TXBRKSYNC is redundant in UART mode).
- This should start break transmission if UART is idle else it completes ongoing transmission and starts break/synch transmission right after.
- Counter is preloaded with value 12 and decremented to achieve break duration of 13-bit time.
- Delimit duration should be based on delimit value configured.
- Synch field 0x55 transmission should begin automatically (start, 8-bit data and stop bit).
- When synch transmission is completed, TXBRKSYNC bit should be reset automatically by HW.
- SW can write PID value into TXFIFO immediately after setting the TXBRKSYNC.
- HW after synch transmission will check TXFE and if TXFE = 1 it does not transmit anything and if TXFE = 0 it transmits data from TXFIFO (In LIN mode it is only one-bytePID that will be written).

23.4.4 Break/Synch reception in LIN mode

- UART, LIN and ABD modes have to be enabled.
- Slave baud rate is configured to desired value by SW.
- When RXD pin goes low, counter is preloaded with value 21 and decremented on bit clock.
- If RXD goes high within 11-bittimes, counter is reset and break is ignored.
- If RXD goes high within 12 to 21-bittimes, stop counter and regard it as valid break field (set LINBRK).
- If RXD does not go high until counter expiry, generate break error condition (set LINBTOE).
- Start a counter on fall edge of synch field and count up to 5 edges (measurement is from first to last falling edges of synch field).
- Integer and fractional counters are started at first fall edge of synch field and stopped at last fall edge.
- Captured integer and fractional counters values are adjusted by suitable scaling factor and used to update baud rate register values.
- When the integer counter overflows during synch field baud rate measurement, synch timeout error flag is set.
- Calculate min and max baud rate that can be detected in LIN mode.
- LINBRK flag to be cleared upon read from DR (data register).

23.4.5 Dormant mode operation

- This mode is relevant onlyin LIN mode operation (LINEN = 1) else takes no effect.
- When disabled, break and synch data will be loaded to RX FIFO and related interrupt flags will be set (as in normal operation).
- When enabled, break only (wake signal) or break and synch data will not be loaded to RX FIFO.
- In this case RX FIFO will be updated with actual data (PID) after successful reception of break/synch fields.

23.4.6 Wakeup signal generation

- Master or slave node can generate wakeup signal on LIN cluster.
- Header alone can be transmitted as wake up signal.
- When TXBRK bit is set in LIN mode, break field alone is transmitted (13-bittimes of value 0).
- Configured baud rate shall be used for break field transmission.
- TXBRK bit shall be auto cleared at the end of break field transmission
- Expected software sequence for LIN master:
  - Set LIN mode, configure baud rate
  - Set TXBRK for wakeup signal generation
  - Once TXBRK is auto cleared, SW can set TXBRKSYNC
  - This starts break/synch sequence in hardware
  - After setting TXBRKSYNC, SW can write PID into TXFIFO
  - Once synch field is transmitted out, hardware clears TXBRKSYNC bit and starts transmitting PID from TXFIFO

23.4.7 Wakeup signal detection when device is in active/idle modes

- When RXD pin goes low, counter is started to detect break condition.
- If the break field duration is longer than 11-bittimes LINBRK will be set.
- If the break field duration is longer than 21-bit times LINBTOE will be set.
- If the break field duration is shorter than 11-bit times (minimum can be 150us as per LIN protocol) breakcondition is treated invalid and ignored.
- This will be fine since the purpose of wake signal transmission is to wake up the device only and, in this case, device is already in active/idle state and UART is ready to receive break/synch fields.
- If necessary DIO based interrupt on RXD pin can also be generated for software use.
- RXD pin will not glitch as it is generated by the LIN transceiver.

23.4.8 Wakeup signal detection when device is in standby mode

- Software has to configure RXD pin for fall edge-basedwake fromstandby.
- When RXD pin goes low, IOC triggers PMCTL for standby exit.
- Software has to reconfigure UART as necessary for LIN mode operation.
- UART is then ready to receive break/sync fields.
- Wake condition will not be detected within UART module through LINBRK or LINBTOE bits.
- This will be fine since the purpose of wake signal transmission is to wake up the device only.

23.5 Interface to µDMA

This UART provide an interface to connect to the µDMA controller. Figure 23-4 shows the interface between the µDMA and UART.

- This interface contains four µDMA requests as outputs (UART0_RX_DMASREQ, UART0_RX_DMABREQ, UART0_TX_DMASREQ, and UART0_TX_DMABREQ). The µDMA interface also has two µDMA request clears as inputs (for clearing TX and RX µDMA requests).
- Each µDMA request signal remains asserted until the relevant µDMA clear signal is asserted. After the µDMA clear signal is deasserted, a request signal can become active again, if conditions are setup correctly. The µDMA clear signal must be connected to the µDMA active signal from the µDMA module. This signal is asserted when µDMA is granted access and is active. The µDMA active signal is deasserted when the µDMA transfer completes. Connecting the µDMA active signal from µDMA to the µDMA request clear input of the UART module ensures that no requests are generated by the UART module while the µDMA is active.
- The burst transfer and single transfer request signals are not mutually exclusive, and both can be asserted at the same time. For example, when there is more data than the watermark level in the receive FIFO, the burst transfer request and the single transfer request are asserted.
- The single and burst requests cannot be masked separately by the UART module and if corresponding µDMA (RX or TX) is enabled, both of these requests are sent to the µDMA.
- All request signals are deasserted if the UART is disabled or if the relevant µDMA enable bit (TXDMAE or RXDMAE) in the µDMA Control Register (UART:DMACTL) is cleared.

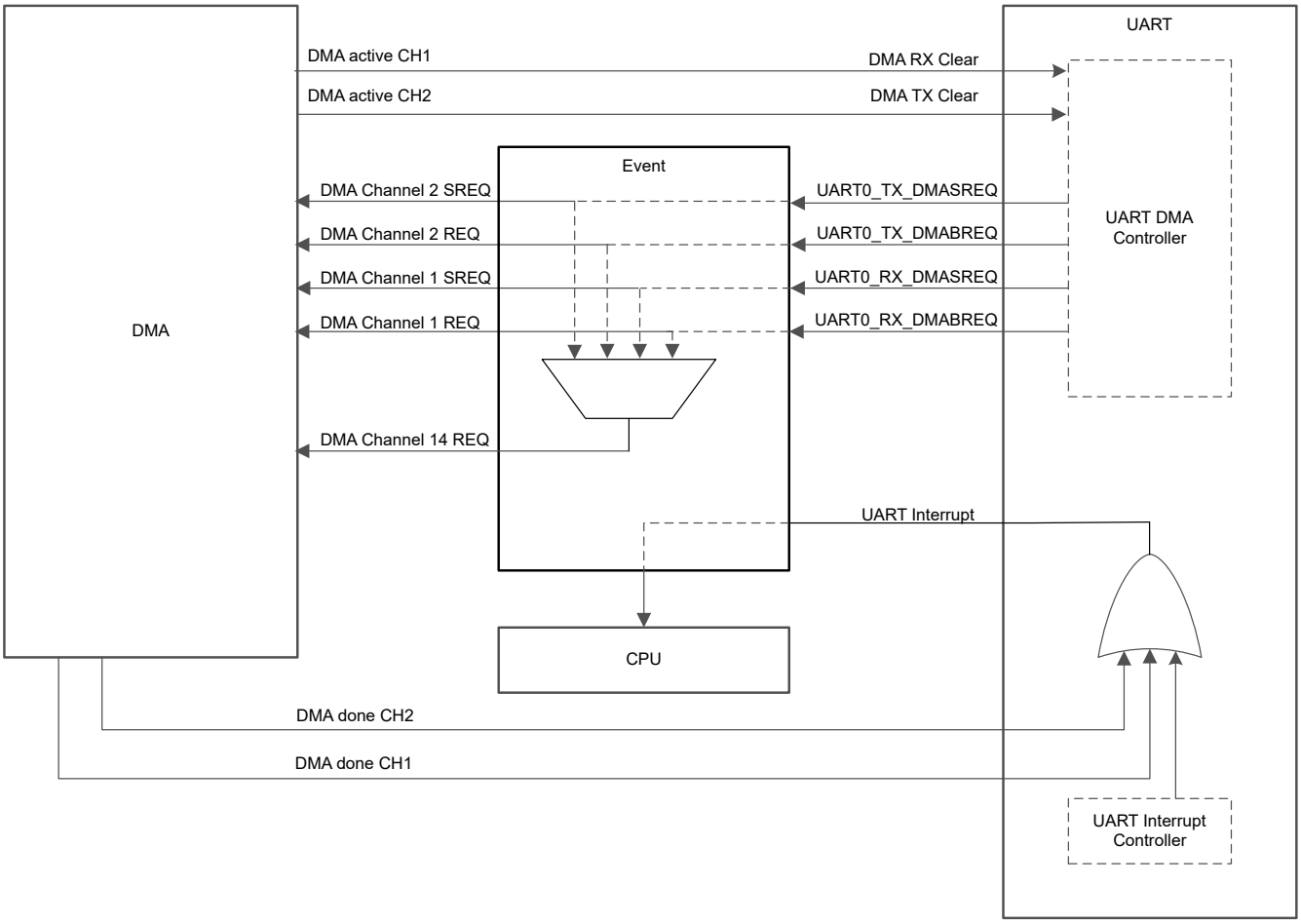

Figure 23-4. µDMA Example

When the UART is in the FIFO enabled mode, data transfers can be made by either single or burst transfers depending on the programmed watermark level and the amount of data in the FIFO. Table 23-1 lists the trigger points for the transmit and receive FIFOs. In addition, if the UART.DMACTL[2] DMAONERR bit is set, the µDMA receive request outputs (for single and burst requests) are disabled when the UART error interrupt is asserted (more specifically if any of the error interrupts in the RIS register, PE, BE, FE or OE are asserted). The µDMA receive request outputs remain inactive until the error bit is cleared. The µDMA transmit request outputs are unaffected.

Table 23-1. µDMA Trigger Points for the Transmit and Receive FIFOs

Watermark Level	Transmit Burst Length (number of empty locations)	Receive Burst Length (number of filled locations)
1/4	6	2
1/2	4	4
3/4	2	6

Sequence for Using µDMA Triggers

- Configure the EVTSVT.DMACH2SEL[2:0] IPID bit field for selecting UARTTXD as trigger source for µDMA
- Configure the EVTSVT.DMACH3SEL[2:0] IPID bit field for selecting UARTRXD as trigger source for µDMA
- Enable Transmit and Receive µDMA Enable by setting the UART.DMACTL TXDMAE[1] bit and UART.DMACTL[0] RXDMA to 1
- Enable the µDMA clock by setting CLKCTL.CLKENSET0[17] µDMA bit to 1

- Configure the dedicated µDMA channels for UARTTXD and UARTRXD through µDMA registers for setting the Source and Destination addresses, Arbitration size and Data size (see Chapter 19 for more details)
- Set the µDMA.CFG[0] MASTERENABLE bit
- Configure the UART.IMSC[12] TXDMADONEIM bit and UART:IMSC[13] RXDMADONEIM bit to trigger the interrupts for µDMA Done

Enable the UART by setting the UART.CTL[0] UARTEN bit

23.6 Initialization and Configuration

The UART module provides four I/O signals to be routed to the DIOs. The following signals are selected through the IOCFGn registers in the IOC module.

- Inputs: RXD, CTS
- Outputs: TXD, RTS

CTS and RTS lines are active low.

Note

IOC must be configured before enabling the UART to avoid unwanted transitions on the input being processed as UART signals. When IOC is configured as UART-specific I/Os (RXD, CTS, TXD, or RTS), IOC sets static output driver enable to the DIO (output driver enable = 1 for output TXD and RTS and output driver enable = 0 for inputs RXD and CTS).

To enable and initialize the UART, use the following steps:

1. Enable the UART module in the CLKCTRL module by writing to the CLKCTRL.CLKENSET0[2] UART0 bit to 1. This enables the clock to UART.
2. Configure the IOC module to map UART signals to the correct GPIO pins. For more information on pin connections, see Chapter 22.

This section discusses the steps required to use a UART module. For this example, the UART clock is assumed to be 48 MHz, and the desired UART configuration is the following:

- Baud rate: 115 200
- Data length of 8 bits
- One stop bit
- No parity
- FIFOs disabled
- No interrupts

The first thing to consider when programming the UART is the BRD because the UART.IBRD and UART.FBRD registers must be written before the UART.LCRH register. The BRD can be calculated using the equation described in Section 23.3.2

$$BRD = 48\,000\,000 / (16 \times 115\,200) = 26.0416 \quad (8)$$

The result of previous equation indicates that the UART.IBRD[15:0] DIVINT bit field must be set to 26 decimal or 0x1A.

$$UART.FBRD[5:0]\ DIVFRAC = integer\ (0.0416 \times 64 + 0.5) = 3 \quad (9)$$

the previous equation calculates the value to be loaded into the UART.FBRD register.

With the BRD values available, the UART configuration is written to the module in the following order:

1. Disable the UART by clearing the UART.CTL[0] UARTEN bit
2. Write the integer portion of the BRD to the UART.IBRD register
3. Write the fractional portion of the BRD to the UART.FBRD register
4. Write the desired serial parameters to the UART.LCRH register (in this case, a value of 0x0000 0060)

5. Enable the UART by setting the UART.CTL[0] UARTEN bit

23.7 UART Registers

Table 23-2 lists the memory-mapped registers for the UART registers. All register offset addresses not listed in Table 23-2 should be considered as reserved locations and the register contents should not be modified.

Table 23-2. UART Registers

Offset	Acronym	Register Name	Section
0h	DR	Data	Section 23.7.1
4h	RSR_ECR	Status	Section 23.7.2
18h	FR	Flag	Section 23.7.3
20h	UARTILPR	IrDA Low-Power Counter Register	Section 23.7.4
24h	IBRD	Integer Baud-Rate Divisor	Section 23.7.5
28h	FBRD	Fractional Baud-Rate Divisor	Section 23.7.6
2Ch	LCRH	Line Control	Section 23.7.7
30h	CTL	Control	Section 23.7.8
34h	IFLS	Interrupt FIFO Level Select	Section 23.7.9
38h	IMSC	Interrupt Mask Set/Clear	Section 23.7.10
3Ch	RIS	Raw Interrupt Status	Section 23.7.11
40h	MIS	Masked Interrupt Status	Section 23.7.12
44h	ICR	Interrupt Clear	Section 23.7.13
48h	DMACTL	DMA Control	Section 23.7.14

Complex bit access types are encoded to fit into small table cells. Table 23-3 shows the codes that are used for access types in this section.

Table 23-3. UART Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

23.7.1 DR Register (Offset = 0h) [Reset = 00000000h]

DR is shown in Table 23-4.

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Data;For words to be transmitted:; - if the FIFOs are enabled (LCRH.FEN = 1), data written to this location is pushed onto the transmit FIFO; - if the FIFOs are not enabled (LCRH.FEN = 0), data is stored in the transmitter holding register (the bottom word of the transmit FIFO).;The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit (if parity is enabled), and a stop bit.;The resultant word is then transmitted.;For received words:; - if the FIFOs are enabled (LCRH.FEN = 1), the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive FIFO ; - if the FIFOs are not enabled (LCRH.FEN = 0), the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO).;The received data byte is read by performing reads from this register along with the corresponding status information. The status information can also be read by a read of the RSR_ECR register.

Table 23-4. DR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	OE	R	0h	UART Overrun Error:;This bit is set to 1 if data is received and the receive FIFO is already full. The FIFO contents remain valid because no more data is written when the FIFO is full, only the contents of the shift register are overwritten.;This is cleared to 0 once there is an empty space in the FIFO and a new character can be written to it.
10	BE	R	0h	UART Break Error:;This bit is set to 1 if a break condition was detected, indicating that the received data input (UARTRXD input pin) was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits).;In FIFO mode, this error is associated with the character at the top of the FIFO (i.e., the oldest received data character since last read). When a break occurs, a 0 character is loaded into the FIFO. The next character is enabled after the receive data input (UARTRXD input pin) goes to a 1 (marking state), and the next valid start bit is received.
9	PE	R	0h	UART Parity Error:;When set to 1, it indicates that the parity of the received data character does not match the parity that the LCRH.EPS and LCRH.SPS select.;In FIFO mode, this error is associated with the character at the top of the FIFO (i.e., the oldest received data character since last read).
8	FE	R	0h	UART Framing Error:;When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1).;In FIFO mode, this error is associated with the character at the top of the FIFO (i.e., the oldest received data character since last read).
7-0	DATA	R/W	0h	Data transmitted or received:;On writes, the transmit data character is pushed into the FIFO.;On reads, the oldest received data character since the last read is returned.

23.7.2 RSR_ECR Register (Offset = 4h) [Reset = 00000000h]

RSR_ECR is shown in Table 23-5.

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Status;This register is mapped to the same address as ECR register. Reads from this address are associated with RSR_ECR register and return the receive status. Writes to this address are associated with ECR register and clear the receive status flags (framing, parity, break, and overrun errors).;If the status is read from this register, then the status information for break, framing and parity corresponds to the data character read from the Data Register DR, prior to reading the RSR_ECR. The status information for overrun is set immediately when an overrun condition occurs.

Table 23-5. RSR_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	OE	R/W	0h	UART Overrun Error:;This bit is set to 1 if data is received and the receive FIFO is already full. The FIFO contents remain valid because no more data is written when the FIFO is full, only the contents of the shift register are overwritten.;This is cleared to 0 once there is an empty space in the FIFO and a new character can be written to it. 0h = Error flag is not set 1h = Clears error flag if error is set. Write value is not important.
2	BE	R/W	0h	UART Break Error:;This bit is set to 1 if a break condition was detected, indicating that the received data input (UARTRXD input pin) was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits).;When a break occurs, a 0 character is loaded into the FIFO. The next character is enabled after the receive data input (UARTRXD input pin) goes to a 1 (marking state), and the next valid start bit is received. 0h = Error flag is not set 1h = Clears error flag if error is set. Write value is not important.
1	PE	R/W	0h	UART Parity Error:;When set to 1, it indicates that the parity of the received data character does not match the parity that the LCRH.EPS and LCRH.SPS select. 0h = Error flag is not set 1h = Clears error flag if error is set. Write value is not important.
0	FE	R/W	0h	UART Framing Error:;When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1). 0h = Error flag is not set 1h = Clears error flag if error is set. Write value is not important.

23.7.3 FR Register (Offset = 18h) [Reset = 00000000h]

FR is shown in Table 23-6.

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Flag;Reads from this register return the UART flags.

Table 23-6. FR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	TXFE	R	1h	UART Transmit FIFO Empty:;The meaning of this bit depends on the state of LCRH.FEN .; - If the FIFO is disabled, this bit is set when the transmit holding register is empty.; - If the FIFO is enabled, this bit is set when the transmit FIFO is empty.;This bit does not indicate if there is data in the transmit shift register.
6	RXFF	R	0h	UART Receive FIFO Full: ;The meaning of this bit depends on the state of LCRH.FEN.; - If the FIFO is disabled, this bit is set when the receive holding register is full.; - If the FIFO is enabled, this bit is set when the receive FIFO is full.
5	TXFF	R	0h	UART Transmit FIFO Full:;Transmit FIFO full. The meaning of this bit depends on the state of LCRH.FEN.; - If the FIFO is disabled, this bit is set when the transmit holding register is full.; - If the FIFO is enabled, this bit is set when the transmit FIFO is full.
4	RXFE	R	1h	UART Receive FIFO Empty:;Receive FIFO empty. The meaning of this bit depends on the state of LCRH.FEN.; - If the FIFO is disabled, this bit is set when the receive holding register is empty.; - If the FIFO is enabled, this bit is set when the receive FIFO is empty.
3	BUSY	R	0h	UART Busy: ;If this bit is set to 1, the UART is busy transmitting data. This bit remains set until the complete byte, including all the stop bits, has been sent from the shift register.;This bit is set as soon as the transmit FIFO becomes non-empty, regardless of whether the UART is enabled or not.
2-1	RESERVED	R	0h	Reserved
0	CTS	R	1h	Clear To Send: ;This bit is the complement of the active-low UART CTS input pin.;That is, the bit is 1 when CTS input pin is LOW.

23.7.4 UARTILPR Register (Offset = 20h) [Reset = 00000000h]

UARTILPR is shown in Table 23-7.

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IrDA Low-Power Counter Register.;This is an 8-bit register that stores the low-power counter divisor value used to generate the IrLPBaud16 signal by dividing down of UARTCLK.

Table 23-7. UARTILPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	ILPDVSR	R/W	0h	8 bit low-power divisor value. In low-power IrDA mode the UART rejects random noise on the received serial data;input by ignoring SIRIN pulses that are less than 3 periods of IrLPBaud16.

23.7.5 IBRD Register (Offset = 24h) [Reset = 00000000h]

IBRD is shown in Table 23-8.

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Integer Baud-Rate Divisor;If this register is modified while trasmission or reception is on-going, the baudrate will not be updated until transmission or reception of the current character is complete.

Table 23-8. IBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DIVINT	R/W	0h	The integer baud rate divisor:;The baud rate divisor is calculated using the formula below:;Baud rate divisor = (UART reference clock frequency) / (16 * Baud rate);Baud rate divisor must be minimum 1 and maximum 65535. ;That is, DIVINT=0 does not give a valid baud rate. ;Similarly, if DIVINT=0xFFFF, any non-zero values in FBRD.DIVFRAC will be illegal.;A valid value must be written to this field before the UART can be used for RX or TX operations.

23.7.6 FBRD Register (Offset = 28h) [Reset = 00000000h]

FBRD is shown in Table 23-9.

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Fractional Baud-Rate Divisor;If this register is modified while trasmission or reception is on-going, the baudrate will not be updated until transmission or reception of the current character is complete.

Table 23-9. FBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DIVFRAC	R/W	0h	Fractional Baud-Rate Divisor:;The baud rate divisor is calculated using the formula below:;Baud rate divisor = (UART reference clock frequency) / (16 * Baud rate);Baud rate divisor must be minimum 1 and maximum 65535. ;That is, IBRD.DIVINT=0 does not give a valid baud rate. ;Similarly, if IBRD.DIVINT=0xFFFF, any non-zero values in DIVFRAC will be illegal.;A valid value must be written to this field before the UART can be used for RX or TX operations.

23.7.7 LCRH Register (Offset = 2Ch) [Reset = 00000000h]

LCRH is shown in Table 23-10.

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Line Control

Table 23-10. LCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-9	DELIM	R/W	0h	In UART LIN defines the length of DELIM field that has to be sent 0h = 0 1h = 1 2h = 2 3h = 3
8	TXBRKSYNC	R/W	0h	UART LIN mode TXBRKSYNC:;0: In LIN mode TXBRKSYNC will not be sent.;1: In LIN mode send TXBRKSYNC field and reset the LCRH.TXBRKSYNC bit.;This bit has no effect when PEN disables parity checking and generation.
7	SPS	R/W	0h	UART Stick Parity Select:;0: Stick parity is disabled;1: The parity bit is transmitted and checked as invert of EPS field (i.e. the parity bit is transmitted and checked as 1 when EPS = 0).;This bit has no effect when PEN disables parity checking and generation.
6-5	WLEN	R/W	0h	UART Word Length:;These bits indicate the number of data bits transmitted or received in a frame. 0h = Word Length 5 bits 1h = Word Length 6 bits 2h = Word Length 7 bits 3h = Word Length 8 bits
4	FEN	R/W	0h	UART Enable FIFOs 0h = FIFOs are disabled (character mode) that is, the FIFOs become 1-byte-deep holding registers. 1h = Transmit and receive FIFO buffers are enabled (FIFO mode)
3	STP2	R/W	0h	UART Two Stop Bits Select:;If this bit is set to 1, two stop bits are transmitted at the end of the frame. The receive logic does not check for two stop bits being received.
2	EPS	R/W	0h	UART Even Parity Select 0h = Odd parity: The UART generates or checks for an odd number of 1s in the data and parity bits. 1h = Even parity: The UART generates or checks for an even number of 1s in the data and parity bits.
1	PEN	R/W	0h	UART Parity Enable;This bit controls generation and checking of parity bit. 0h = Parity is disabled and no parity bit is added to the data frame 1h = Parity checking and generation is enabled.
0	BRK	R/W	0h	UART Send Break;If this bit is set to 1, a low-level is continually output on the UARTTXD output pin, after completing transmission of the current character. For the proper execution of the break command, the;software must set this bit for at least two complete frames. For normal use, this bit must be cleared to 0.

23.7.8 CTL Register (Offset = 30h) [Reset = 00000000h]

CTL is shown in Table 23-11.

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Control

Table 23-11. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CTSEN	R/W	0h	CTS hardware flow control enable 0h = CTS hardware flow control disabled 1h = CTS hardware flow control enabled
14	RTSEN	R/W	0h	RTS hardware flow control enable 0h = RTS hardware flow control disabled 1h = RTS hardware flow control enabled
13-12	RESERVED	R	0h	Reserved
11	RTS	R/W	0h	Request to Send;This bit is the complement of the active-low UART RTS output. That is, when the bit is programmed to a 1 then RTS output on the pins is LOW.
10	RESERVED	R	0h	Reserved
9	RXE	R/W	1h	UART Receive Enable;If the UART is disabled in the middle of reception, it completes the current character before stopping. 0h = UART Receive disabled 1h = UART Receive enabled
8	TXE	R/W	1h	UART Transmit Enable;If the UART is disabled in the middle of transmission, it completes the current character before stopping. 0h = UART Transmit disabled 1h = UART Transmit enabled
7	LBE	R/W	0h	UART Loop Back Enable;Enabling the loop-back mode connects the UARTTXD output from the UART to UARTRXD input of the UART. 0h = Loop Back disabled 1h = Loop Back enabled
6	FCEN	R/W	0h	UART FIFO Concatenation Enable;Enabling the FIFO concatenation in TX mode resulting in 16 TX buffers. 0h = UART FIFO Concatenation disabled 1h = UART FIFO Concatenation enabled
5	DORMEN	R/W	0h	DORMEN bit is only functionally makes sense for LIN mode of operation.;When dormant mode is disabled, break and synch data shall be loaded to RX FIFO and associated interrupt flags shall be set as in normal UART operation.;When dormant mode is enabled, break and synch data shall not be loaded to RX FIFO and RX FIFO shall be updated with actual data (PID) only after successful reception of break/synch fields. 0h = 0 1h = 1
4	ABDEN	R/W	0h	This configuration bit defines whether we want automatic baud rate detection enabled or not in the LIN mode of operation. 0h = 0 1h = 1
3	LINEN	R/W	0h	This is the LIN Mode of operation configuration bit. 0h = 0 1h = 1

Table 23-11. CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SIRLP	R/W	0h	SIR low power IrDA mode;This bit selects the IrDA encoding mode 0h = Low-level bits are transmitted as active high with a 3/16th period width, 1h = Low-level bits are transmitted with a pulse width of 3 times the period of IrLPBaud16(which has a frequency of (UARTCLK frequency)/UARTILP.ILPDVSR), regardless of the selected bit rate.;In low-power IrDA mode the UART rejects random noise on the received serial data;input by ignoring SIRIN pulses that are less than 3 periods of IrLPBaud16.
1	SIREN	R/W	0h	SIR Enable;This bit has no effect if UARTEN bit disables the UART. 0h = IrDA SIR ENDEC is disabled 1h = IrDA SIR ENDEC is enabled. Data is transmitted and received via nSIROUT and SIRIN.
0	UARTEN	R/W	0h	UART Enable 0h = UART disabled 1h = UART enabled

23.7.9 IFLS Register (Offset = 34h) [Reset = 00000000h]

IFLS is shown in Table 23-12.

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Interrupt FIFO Level Select

Table 23-12. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-3	RXSEL	R/W	2h	Receive interrupt FIFO level select:;This field sets the trigger points for the receive interrupt. Values 0b101-0b111 are reserved. 1h = Receive FIFO becomes >= 1/4 full 2h = Receive FIFO becomes >= 1/2 full 3h = Receive FIFO becomes >= 3/4 full
2-0	TXSEL	R/W	2h	Transmit interrupt FIFO level select:;This field sets the trigger points for the transmit interrupt. Values 0b101-0b111 are reserved. 1h = Transmit FIFO becomes <= 1/4 full 2h = Transmit FIFO becomes <= 1/2 full 3h = Transmit FIFO becomes <= 3/4 full

23.7.10 IMSC Register (Offset = 38h) [Reset = 00000000h]

IMSC is shown in Table 23-13.

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Interrupt Mask Set/Clear

Table 23-13. IMSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LINSYNCTOE	R/W	0h	LIN Sync Time out error interrupt mask. A read returns the current mask for UART's LINSYNCTOE interrupt. On a write of 1, the mask of the LINSYNCTOE interrupt is set which means the interrupt state will be reflected in MIS.LINSYNCTOE. A write of 0 clears the mask which means MIS.LINSYNCTOE will not reflect the interrupt.
15	LINBRKTOE	R/W	0h	LIN Break field Time out error interrupt mask. A read returns the current mask for UART's LINBRKTOE interrupt. On a write of 1, the mask of the LINBRKTOE interrupt is set which means the interrupt state will be reflected in MIS.LINBRKTOE. A write of 0 clears the mask which means MIS.LINBRKTOE will not reflect the interrupt.
14	LINBRK	R/W	0h	LIN Break field recieved/detected interrupt mask. A read returns the current mask for UART's LINBRK interrupt. On a write of 1, the mask of the LINBRK interrupt is set which means the interrupt state will be reflected in MIS.LINBRK. A write of 0 clears the mask which means MIS.LINBRK will not reflect the interrupt.
13	RXDMADONE	R/W	0h	RX DMA done interrupt mask. A read returns the current mask for UART's RXDMADONE interrupt. On a write of 1, the mask of the RXDMADONE interrupt is set which means the interrupt state will be reflected in MIS.RXDMADONE. A write of 0 clears the mask which means MIS.RXDMADONE will not reflect the interrupt.
12	TXDMADONE	R/W	0h	TX DMA done interrupt mask. A read returns the current mask for UART's TXDMADONE interrupt. On a write of 1, the mask of the TXDMADONE interrupt is set which means the interrupt state will be reflected in MIS.TXDMADONE. A write of 0 clears the mask which means MIS.TXDMADONE will not reflect the interrupt.
11	EOT	R/W	0h	End of Transmission interrupt mask. A read returns the current mask for UART's EoT interrupt. On a write of 1, the mask of the EoT interrupt is set which means the interrupt state will be reflected in MIS.EOT. A write of 0 clears the mask which means MIS.EOT will not reflect the interrupt.
10	OE	R/W	0h	Overrun error interrupt mask. A read returns the current mask for UART's overrun error interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.OE. A write of 0 clears the mask which means MIS.OE will not reflect the interrupt.
9	BE	R/W	0h	Break error interrupt mask. A read returns the current mask for UART's break error interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.BE. A write of 0 clears the mask which means MIS.BE will not reflect the interrupt.
8	PE	R/W	0h	Parity error interrupt mask. A read returns the current mask for UART's parity error interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.PE. A write of 0 clears the mask which means MIS.PE will not reflect the interrupt.
7	FE	R/W	0h	Framing error interrupt mask. A read returns the current mask for UART's framing error interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.FE. A write of 0 clears the mask which means MIS.FE will not reflect the interrupt.

Table 23-13. IMSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RT	R/W	0h	Receive timeout interrupt mask. A read returns the current mask for UART's receive timeout interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.RT. A write of 0 clears the mask which means this bitfield will not reflect the interrupt. ;The raw interrupt for receive timeout RIS.RT cannot be set unless the mask is set (RT = 1). This is because the mask acts as an enable for power saving. That is, the same status can be read from MIS.RT and RIS.RT.
5	TX	R/W	0h	Transmit interrupt mask. A read returns the current mask for UART's transmit interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.TX. A write of 0 clears the mask which means MIS.TX will not reflect the interrupt.
4	RX	R/W	0h	Receive interrupt mask. A read returns the current mask for UART's receive interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.RX. A write of 0 clears the mask which means MIS.RX will not reflect the interrupt.
3-2	RESERVED	R	0h	Reserved
1	CTSM	R/W	0h	Clear to Send (CTS) modem interrupt mask. A read returns the current mask for UART's clear to send interrupt. On a write of 1, the mask of the overrun error interrupt is set which means the interrupt state will be reflected in MIS.CTSM. A write of 0 clears the mask which means MIS.CTSM will not reflect the interrupt.
0	RESERVED	R	0h	Reserved

23.7.11 RIS Register (Offset = 3Ch) [Reset = 00000000h]

RIS is shown in Table 23-14.

Return to the Summary Table.

Raw Interrupt Status

Table 23-14. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LINSYNCTOE	R	0h	LIN SYNC field time out interrupt status:;This field returns the raw interrupt state of whether sync field is measurable in UART's LIN mode of operation. This is set when the timer measuring the SYNC field overflows.
15	LINBRKTOE	R	0h	LIN BRK field time out interrupt status:;This field returns the raw interrupt state of whether break field is measurable in UART's LIN mode of operation. This is set when the timer measuring the Break field overflows.
14	LINBRK	R	0h	LIN BRK detected interrupt status:;This field returns the raw interrupt state of whether break field is recieved/detected in UART's LIN mode of operation.
13	RXDMADONE	R	0h	RX DMA done interrupt status:;This field returns the raw interrupt state of UART's RX DMA done interrupt. RX DMA done flag is set when you recieve RX DMA done status from dma module.
12	TXDMADONE	R	0h	TX DMA done interrupt status:;This field returns the raw interrupt state of UART's TX DMA done interrupt. TX DMA done flag is set when you recieve TX DMA done status from dma module.
11	EOT	R	0h	End of Transmission interrupt status:;This field returns the raw interrupt state of UART's end of transmission interrupt. End of transmission flag is set when all the Transmit data in the FIFO and on the TX Line is tranmitted.
10	OE	R	0h	Overrun error interrupt status: ;This field returns the raw interrupt state of UART's overrun error interrupt. Overrun error occurs if data is received and the receive FIFO is full.
9	BE	R	0h	Break error interrupt status:;This field returns the raw interrupt state of UART's break error interrupt. Break error is set when a break condition is detected, indicating that the received data input (UARTRXD input pin) was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits).
8	PE	R	0h	Parity error interrupt status:;This field returns the raw interrupt state of UART's parity error interrupt. Parity error is set if the parity of the received data character does not match the parity that the LCRH.EPS and LCRH.SPS select.
7	FE	R	0h	Framing error interrupt status:;This field returns the raw interrupt state of UART's framing error interrupt. Framing error is set if the received character does not have a valid stop bit (a valid stop bit is 1).
6	RT	R	0h	Receive timeout interrupt status:;This field returns the raw interrupt state of UART's receive timeout interrupt. The receive timeout interrupt is asserted when the receive FIFO is not empty, and no more data is received during a 32-bit period. The receive timeout interrupt is cleared either when the FIFO becomes empty through reading all the data, or when a 1 is written to ICR.RT.;The raw interrupt for receive timeout cannot be set unless the mask is set (IMSC.RT = 1). This is because the mask acts as an enable for power saving. That is, the same status can be read from MIS.RT and RT.

Table 23-14. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX	R	0h	Transmit interrupt status: ;This field returns the raw interrupt state of UART's transmit interrupt.;When FIFOs are enabled (LCRH.FEN = 1), the transmit interrupt is asserted if the number of bytes in transmit FIFO is equal to or lower than the programmed trigger level (IFLS.TXSEL). The transmit interrupt is cleared by writing data to the transmit FIFO until it becomes greater than the trigger level, or by clearing the interrupt through ICR.TX.;When FIFOs are disabled (LCRH.FEN = 0), that is they have a depth of one location, the transmit interrupt is asserted if there is no data present in the transmitters single location. It is cleared by performing a single write to the transmit FIFO, or by clearing the interrupt through ICR.TX.
4	RX	R	0h	Receive interrupt status:;This field returns the raw interrupt state of UART's receive interrupt. ;When FIFOs are enabled (LCRH.FEN = 1), the receive interrupt is asserted if the receive FIFO reaches the programmed trigger;level (IFLS.RXSEL). The receive interrupt is cleared by reading data from the receive FIFO until it becomes less than the trigger level, or by clearing the interrupt through ICR.RX.;When FIFOs are disabled (LCRH.FEN = 0), that is they have a depth of one location, the receive interrupt is asserted if data is received;thereby filling the location. The receive interrupt is cleared by performing a single read of the receive FIFO, or by clearing the interrupt through ICR.RX.
3-2	RESERVED	R	0h	Reserved
1	CTSM	R	0h	Clear to Send (CTS) modem interrupt status: ;This field returns the raw interrupt state of UART's clear to send interrupt.
0	RESERVED	R	0h	Reserved

23.7.12 MIS Register (Offset = 40h) [Reset = 00000000h]

MIS is shown in Table 23-15.

Return to the Summary Table.

Masked Interrupt Status

Table 23-15. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LINSYNCTOE	R	0h	LIN sync field time out error interrupt status:;This field returns the masked interrupt state of the LIN sync timeout error interrupt which is the AND product of raw interrupt state RIS.LINSYNCTOERIS and the mask setting IMSC.LINSYNCTOEIM.
15	LINBRKTOE	R	0h	LIN BRK field time out error interrupt status:;This field returns the masked interrupt state of the LIN BRK timeout error interrupt which is the AND product of raw interrupt state RIS.LINBRKTOERIS and the mask setting IMSC.LINBRKTOEIM.
14	LINBRK	R	0h	LIN BRK field detected interrupt status:;This field returns the masked interrupt state of the LIN BRK detected interrupt which is the AND product of raw interrupt state RIS.LINBRKRIS and the mask setting IMSC.LINBRKIM.
13	RXDMADONE	R	0h	RX DMA done interrupt status:;This field returns the masked interrupt state of the RX DMA done interrupt which is the bitiwse AND product of raw interrupt state RIS.RXDMADONE and the mask setting IMSC.RXDMADONE.
12	TXDMADONE	R	0h	TX DMA done interrupt status:;This field returns the masked interrupt state of the TX DMA done interrupt which is the bitwise AND product of raw interrupt state RIS.TXDMADONE and the mask setting IMSC.TXDMADONE.
11	EOT	R	0h	End of Transmission interrupt status:;This field returns the masked interrupt state of the End of transmission interrupt which is the bitwise AND product of raw interrupt state RIS.EOT and the mask setting IMSC.EOT.
10	OE	R	0h	Overrun error masked interrupt status: ;This field returns the masked interrupt state of the overrun interrupt which is the bitwise AND product of raw interrupt state RIS.OE and the mask setting IMSC.OE.
9	BE	R	0h	Break error masked interrupt status: ;This field returns the masked interrupt state of the break error interrupt which is the bitiwse AND product of raw interrupt state RIS.BE and the mask setting IMSC.BE.
8	PE	R	0h	Parity error masked interrupt status:;This field returns the masked interrupt state of the parity error interrupt which is the bitiwise AND product of raw interrupt state RIS.PE and the mask setting IMSC.PE.
7	FE	R	0h	Framing error masked interrupt status: Returns the masked interrupt state of the framing error interrupt which is the bitiwse AND product of raw interrupt state RIS.FE and the mask setting IMSC.FE.
6	RT	R	0h	Receive timeout masked interrupt status: ;Returns the masked interrupt state of the receive timeout interrupt.;The raw interrupt for receive timeout cannot be set unless the mask is set (IMSC.RT = 1). This is because the mask acts as an enable for power saving. That is, the same status can be read from MIS.RT and RIS.RT.
5	TX	R	0h	Transmit masked interrupt status: ;This field returns the masked interrupt state of the transmit interrupt which is the bitiwse AND product of raw interrupt state RIS.TX and the mask setting IMSC.TX.
4	RX	R	0h	Receive masked interrupt status:;This field returns the masked interrupt state of the receive interrupt which is the bitwise AND product of raw interrupt state RIS.RX and the mask setting IMSC.RX.
3-2	RESERVED	R	0h	Reserved

Table 23-15. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CTSM	R	0h	Clear to Send (CTS) modem masked interrupt status:;This field returns the masked interrupt state of the clear to send interrupt which is the bitwise AND product of raw interrupt state RIS.CTS and the mask setting IMSC.CTS.
0	RESERVED	R	0h	Reserved

23.7.13 ICR Register (Offset = 44h) [Reset = 00000000h]

ICR is shown in Table 23-16.

Return to the Summary Table.

Interrupt Clear;On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

Table 23-16. ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LINSYNCTOE	W	0h	LIN SYNC timeout interrupt clear:;Writing 1 to this field clears the rxdma done interrupt (RIS.LINSYNCTOE). Writing 0 has no effect.
15	LINBRKTOE	W	0h	LIN BRK field timeout interrupt clear:;Writing 1 to this field clears the rxdma done interrupt (RIS.LINBRKTOE). Writing 0 has no effect.
14	LINBRK	W	0h	LIN BRK field detected interrupt clear:;Writing 1 to this field clears the rxdma done interrupt (RIS.LINBRK). Writing 0 has no effect.
13	RXDMADONE	W	0h	RX DMA Done interrupt clear:;Writing 1 to this field clears the RX DMA done interrupt (RIS.RXDMADONE). Writing 0 has no effect.
12	TXDMADONE	W	0h	TX DMA Done interrupt clear:;Writing 1 to this field clears the TX DMA done interrupt (RIS.TXDMADONE). Writing 0 has no effect.
11	EOT	W	0h	End of Transmission interrupt clear:;Writing 1 to this field clears the End of Transmission interrupt (RIS.EOT). Writing 0 has no effect.
10	OE	W	0h	Overrun error interrupt clear:;Writing 1 to this field clears the overrun error interrupt (RIS.OE). Writing 0 has no effect.
9	BE	W	0h	Break error interrupt clear:;Writing 1 to this field clears the break error interrupt (RIS.BE). Writing 0 has no effect.
8	PE	W	0h	Parity error interrupt clear:;Writing 1 to this field clears the parity error interrupt (RIS.PE). Writing 0 has no effect.
7	FE	W	0h	Framing error interrupt clear:;Writing 1 to this field clears the framing error interrupt (RIS.FE). Writing 0 has no effect.
6	RT	W	0h	Receive timeout interrupt clear:;Writing 1 to this field clears the receive timeout interrupt (RIS.RT). Writing 0 has no effect.
5	TX	W	0h	Transmit interrupt clear:;Writing 1 to this field clears the transmit interrupt (RIS.TX). Writing 0 has no effect.
4	RX	W	0h	Receive interrupt clear:;Writing 1 to this field clears the receive interrupt (RIS.RX). Writing 0 has no effect.
3-2	RESERVED	R	0h	Reads to this field return zero, writes to this field are ignored. Write 0
1	CTSM	W	0h	Clear to Send (CTS) modem interrupt clear:;Writing 1 to this field clears the clear to send interrupt (RIS.CTS). Writing 0 has no effect.
0	RESERVED	R	0h	Reads to this field return zero, writes to this field are ignored. Write 0.

23.7.14 DMACTL Register (Offset = 48h) [Reset = 00000000h]

DMACTL is shown in Table 23-17.

Return to the Summary Table.

DMA Control

Table 23-17. DMACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	DMAONERR	R/W	0h	DMA on error. If this bit is set to 1, the DMA receive request outputs (for single and burst requests) are disabled when the UART error interrupt is asserted (more specifically if any of the error interrupts RIS.PERIS, RIS.BERIS, RIS.FERIS or RIS.OERIS are asserted).
1	TXDMAE	R/W	0h	Transmit DMA enable. If this bit is set to 1, DMA for the transmit FIFO is enabled.
0	RXDMAE	R/W	0h	Receive DMA enable. If this bit is set to 1, DMA for the receive FIFO is enabled.

Chapter 24

Serial Peripheral Interface (SPI)

This chapter describes the Serial Peripheral Interface (SPI) module.

24.1 Overview

The Serial Peripheral Interface (SPI) module provides a standardized serial interface to transfer data to and from external devices using the SPI protocol (such as sensors, memories, ADCs or DACs).

24.1.1 Features

The SPI module has the following features:

- Programmable interface operation for Motorola SPI (3-wire and 4-wire), MICROWIRE, or TI Synchronous Serial format
- Configurable as a controller or a peripheral on the interface
- Programmable clock bit rate and prescaler
- CRC8-CCITT or CRC16-CCITT CRC capability
- Separate transmit (TX) and receive (RX) first-in first-out buffers (FIFOs)
  - If Data Size Select (DSS) is 4 to 8 bits, FIFOs are 16 locations, 8 bits wide
  - If Data Size Select (DSS) is 9 to 16 bits, FIFOs are 8 locations, 16 bits wide
- Programmable data frame size from 4 bits to 16 bits (controller mode) or 7 to 16 bits (peripheral mode)
- Internal loop-back test mode for diagnostic and debug testing
- Interrupts for transmit and receive FIFOs, overrun and time-out interrupts, completed DMA interrupts
- Efficient data transfers using micro direct memory access controller (µDMA):
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains a configurable number of entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when FIFO contains a configurable number of entries

24.1.2 Block Diagram

Figure 24-1 shows the SPI block diagram.

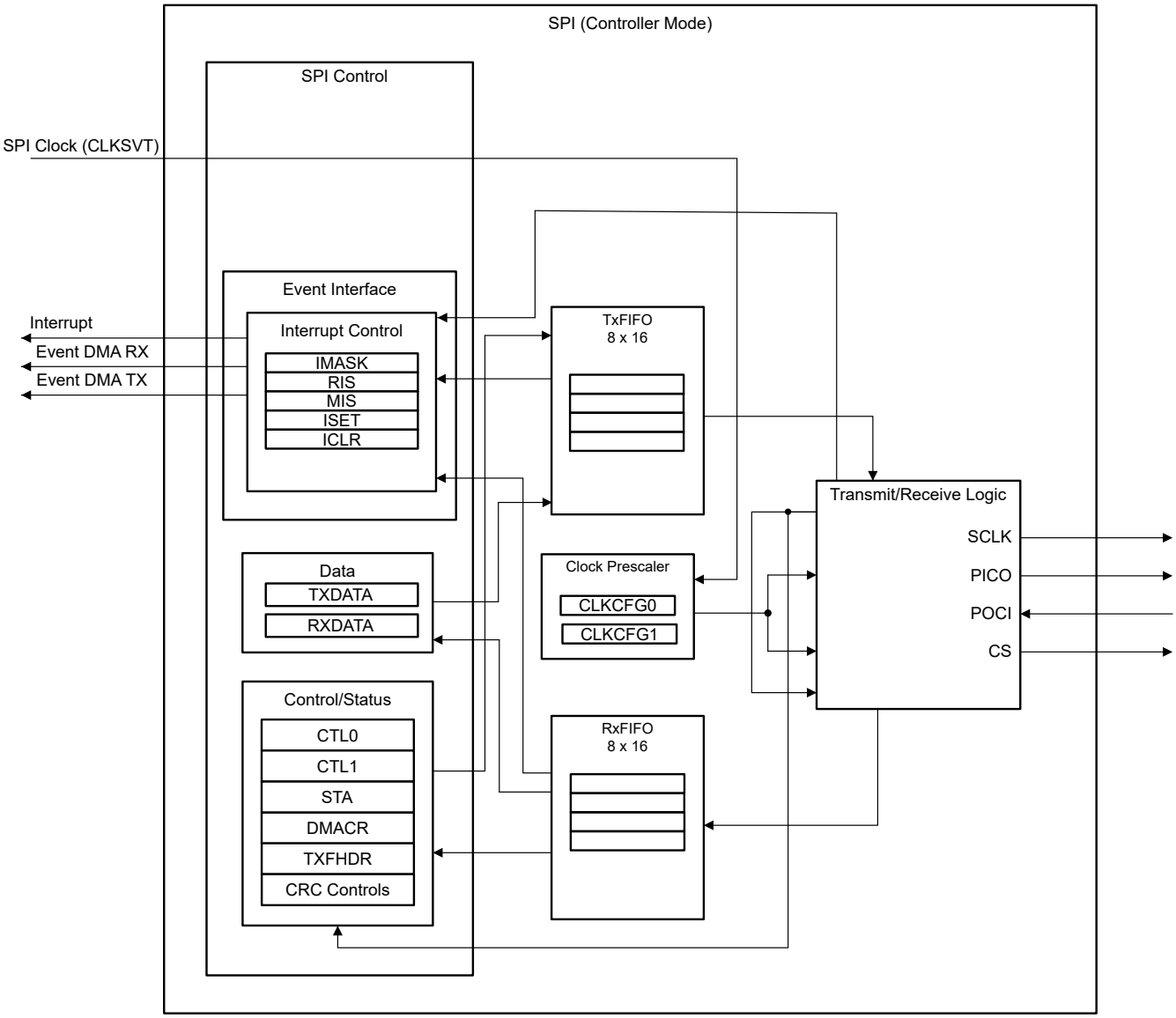


Figure 24-1. SPI Block Diagram

24.2 Signal Description

Table 24-1 lists the external SPI signals and describes the function of each. The SPI signals are selected in the IOC module through the IOCFGn registers. For more information on configuration of DIOs, see Chapter 22.

Table 24-1. SPI Signal Description

Signal Name	Pin Number	Description
SCLK	Assigned in I/O Controller	**SPI Clock** Controller Mode: SCLK is an output Peripheral Mode: SCLK is an input
CS		**SPI Chip Select** Controller Mode: CS is an output Peripheral Mode: CS is an input
PICO		**Peripheral In, Controller Out** Controller mode: PICO is the data output line Peripheral mode: PICO is the data input line
POCI		**Peripheral Out, Controller In** Controller mode: POCI is the data input line Peripheral mode: POCI is the data output line

24.3 Functional Description

SPI performs serial-to-parallel conversion on data received from a peripheral device. The CPU accesses data, control, and status information. Internal FIFO memories buffer the transmit and receive paths, allowing independent storage of up to eight 16-bit values in both transmit and receive modes. The SPI also supports the µDMA interface. The TX and RX FIFOs can be programmed as destination or source addresses in the µDMA module. The µDMA operation is enabled by setting the appropriate bits in the SPI:DMACR register. The SPI module also includes a CRC engine that can be used for data checking during SPI transmission. If SPI is not being used, this can act as a general-purpose CRC engine. Additional capability is added to enable the SPI module to be used efficiently with an external controller in a transceiver setup by allowing atomic operations to update header information in the FIFO, including atomic FIFO pointers' reset capability.

24.3.1 Clock Control

The SPI includes a programmable bit rate clock divider and prescaler to generate the serial output clock.

The serial bit rate is derived by dividing down the input clock, CLKSVT (48MHz).

First, the clock is divided by a division PRESC from 1 to 8, which is programmed in SPI.CLKCFG0 (1 means that the clock is not divided). The clock is further divided by a value from 1 to 1024, which is 1 + SCR, where SCR is the value programmed in SPI.CLKCFG1.

Equation 10 defines the frequency of the output clock SCLK.

$$SCLK = CLKSVT / [PRESC \times (1 + SCR)] \quad (10)$$

Note

For both peripheral and controller modes, the core clock (CLKSVT) must be at least two times faster than SCLK.

The maximum SPI frequency supported with controller and peripheral modes depends on the device clock option and IO option. Please refer to the specific data sheet specification for more information.

24.3.2 FIFO Operation

24.3.2.1 Transmit FIFO

The common TX FIFO is a 16-bit wide, 8 location deep, first-in first-out memory buffer given the selected SPI data frame size is greater than 8 bits. The organization of this FIFO is modified dynamically if the selected SPI data frame size is greater than 8 bits, the common TX FIFO is a 16-bit wide, 8 location deep, first-in first-out

memory buffer. The CPU writes data to the FIFO via the SPI.TXDATA register and data is stored in the FIFO until the data is read out by the transmission logic.

When configured as a controller (or a peripheral), parallel data is written into the TX FIFO before serial conversion and transmission to the attached peripheral (or controller) through the PICO (or POCI) pin.

In peripheral mode, the SPI transmits data each time the controller initiates a transaction. If the TX FIFO is empty and the controller initiates a transaction, the peripheral will transmit garbage data. User or software is responsible for making valid data available in the FIFO as needed. The SPI can be configured to generate an interrupt when a configurable level within the FIFO is selected via SPI:IFLS, or a µDMA request when the FIFO is not FULL.

24.3.2.2 Repeated Transmit Operation

Using the SPI.CTL1[23:16] REPTX bit field, the last data frame transmitted can be repeated as many times as configured within the field. The SPI transfer can be started by writing data once into the TX FIFO. This feature then transmits the same data repeatedly as if the data were written into the TXFIFO [*SPI.CTL1[23:16] REPTX bit field*] a number of times. The repeated transfer operation can be used to clean a transfer or to pull a certain amount of data from a peripheral. A value of 0 in the SPI.CTL1[23:16] REPTX bit field disables this mode. This function is only available in controller mode.

When repeated transmit is used, the function needs to be aligned with the data in the FIFO. The following sequence is used when setting up the repeated transmit operation:

- Check and wait till FIFO is empty
- Setup REPTX
- Write to TXDATA / TXFIFO
- Wait till requested data has been received

24.3.2.3 Receive FIFO

If the selected SPI data frame size is greater than 8 bits, the common RX FIFO is a 16-bit wide, 8 location deep, first-in first-out memory buffer. The organization of this FIFO is modified dynamically if the selected data size is less than or equal to 8 bits, and for better FIFO utilization behaves as an 8-bit wide, 16 locations deep FIFO. Received data from the serial interface is stored in the buffer until read out by the CPU, which accesses the read FIFO by reading the SPI.RXDATA register.

When configured as a controller (or peripheral), serial data received through the POCI (or PICO) pin is registered prior to parallel loading into the RX FIFO.

24.3.2.4 FIFO Flush

SPI includes a feature to reset the TX and RX FIFO pointers to flush FIFOs. This must be triggered when no SPI transactions are in progress. If a FIFO flush is triggered when a transaction is in progress, then a second FIFO flush is needed when no operations are ongoing, before restarting new SPI transfers.

The FIFO flush operation is atomic. When CPU writes into SPI.CTL0[11] FIFORST register bit, the SPI hardware internally ensures that TX and RX FIFO pointers are set to zero, and auto-clears the FIFORST bit after 4 CLKSVT clock cycles. CPU can poll the FIFORST bit to identify when the FIFO pointer reset operation has completed.

Note

FIFO pointers also get reset when SPI is disabled after the SPI.CTL1[0] EN bit toggles from 0x1 to 0x0.

24.3.3 Interrupts

The SPI can generate interrupts when the following conditions are observed:

- TX FIFO service (with the TX FIFO level configured via the SPI.IFLS[2:0] TXSEL bit field)
- RX FIFO service (with the RX FIFO level configured via the SPI.IFLS[10:8] RXSEL bit field)

- RX FIFO timeout
- RX FIFO overrun
- TX FIFO empty
- TX DMA done/RX DMA done
- Idle
- Parity error

All interrupt events are ORed together before being sent to the SVT event fabric, thus the SPI generates a single interrupt request regardless of the number of active interrupts. The interrupt conditions listed above can be masked by setting the appropriate bit in the SPI.IMASK register. Setting the appropriate mask bit in the SPI.IMASK register enables the interrupt. SPI.IMSET and SPI.IMCLR are alias registers which can be used to set and clear individual bits of SPI:IMASK register.

The status of the individual interrupt sources can be read from the SPI Raw Interrupt Status register (SPI.RIS) and the SPI Masked Interrupt Status register (SPI.MIS). SPI.ICLR can be used to clear interrupt flags within RIS and MIS. SPI.ISET can be used to set these interrupt flags for debug or test purposes.

The transmit FIFO service interrupt request SPI.RIS[4] TX bit is not gated with the SPI enable signal, which allows data to be written to the transmit FIFO before enabling the SPI by an interrupt service routine (ISR).

Note

TX and RX FIFO interrupts are best serviced by µDMA rather than CPU. In case CPU services TX and RX FIFO interrupts, TXEMPTY and RXOVF can be configured as well, so that if the FIFO interrupt is missed by the CPU in corner cases, these act as a fail-safe.

The receive FIFO overflow interrupt SPI.RIS[0] RXOVF is asserted when the FIFO is already full and an additional data frame is received, causing an overflow of the FIFO. Data is overwritten in the receive shift register, but not in the FIFO.

The parity error interrupt SPI.RIS[1] PER bit is set when a parity error is detected. SPI.CTL1[5] PEN bit can be written to enable the parity check, where the last bit received is used as parity to test the integrity of the previous bits. SPI.CTL1[7] PBS bit selects the parity mode as even or odd. When a parity fault is detected, the interrupt flag SPI.RIS[1] PER bit is set (to mark the data as invalid).

The idle interrupt SPI.RIS[6] IDLE is set when the SPI transmission has concluded and SPI module moves back to idle mode. This is set when SPI.STA[4] BUSY goes low.

The SPI Receive Timeout interrupt is set when SPI is in peripheral mode and has not been receiving data for the number of functional clock cycles (CLKSVT) configured within SPI.CTL1[29:24] RTOUT bit field. A value of 0 disables this function. The countdown is started when SPI is in the peripheral mode and the first SCLK positive edge is detected and the countdown is restarted on each subsequent SCLK positive edge. A timeout error is asserted if the count reaches zero before the next SCLK toggles.

24.3.4 Data Format

Each data frame is between 4 and 16 bits long, depending on the size of the data programmed. The control bit SPI.CTL1[4] MSB field can be programmed to define the direction of the data input and output as most-significant-bit (MSB) or least-significant-bit (LSB) first. If parity is enabled, the parity bit is always received as the last bit.

With SPI.CTL0[3:0] DSS bit field, the bit length per transfer is defined between 4 – 16 bits for controller mode and 7 – 16 bits for peripheral mode.

24.3.5 Delayed Data Sampling

In cases when the input data arrives at the POCI pin with additional delay due to run-time conditions or path delays, on the following input data sampling stage, the previous data can be sampled at the sampling clock edge. To compensate for this, sampling of input data in controller mode can be delayed using the SPI.CLKCFG1[19:16] DSAMPLE bit field. The delayed sampling is only available in controller mode. The delay can be adjusted in steps of undivided SPI input clocks (CLKSVT) programmed within the SPI.CLKCFG1[19:16]

DSAMPLE bit field. The range of values of DSAMPLE is 0 to SCR+1. Typically, values of 1 and 2 are sufficient even for the highest supported SPI frequencies.

24.3.6 Chip Select Control

SPI can be configured to controller mode by setting the SPI.CTL1[2] MS bit to 1, and to peripheral mode by clearing the SPI.CTL1[2] MS bit.

The chip select signal needs to be provided by the controller in Motorola 4-wire mode.

Regardless of the configuration of PHA or POL, SPI includes a feature to keep the CS active low until all data has been transferred from TXFIFO in controller mode and Motorola 4-wire frame format. This feature is enabled by the SPI.CTL0[10] HWCSN bit. If SPI.CTL0[14] AUTOCRC is set, then CS is kept low until the CRC has been transferred as well.

In peripheral mode, the clock is provided by the controller and used by the SPI to capture the data. The peripheral has the option to operate in 3-wire or 4-wire mode. 4-wire mode only accepts data transfers if the CS is activated.

When SPI is in peripheral mode and the SPI.CTL0[12] CSCLR bit is set, the receive shift register is cleared automatically when CS goes to inactive state.

24.3.7 Command Data Control

When using the Motorola 3-wire frame format with the SPI.CTL0[3:0] DSS bit field programmed for 8 bits, the SPI.CTL1[11] CDEN bit can be set to use the CS line as a signal to distinguish between Command and Data information. This is often used for LCD or data storage devices.

- CS level low: command function
- CS level high: data function

The SPI.CTL1[15:12] CDMODE bit field can be written with a value of 1-14 to specify the number of bytes the CS line is set low for, starting with the next value to be transmitted. After the number of bytes are transmitted, CS is set high automatically. If a value of 0xF is set, CS stays low permanently. A value of 0 sets the CS line to high immediately after the current data byte has been transmitted.

This option is only available in controller mode. The SPI.CTL1[11] CDEN bit can only be updated when the SPI module is disabled. SPI.CTL1[15:12] CDMODE can be updated between the different data packages. The counter is reset with CDEN or SPI ENABLE set to disabled. Before setting a new value in CTL1.CDMODE, check that the FIFO is empty and that SPI is in IDLE state (SPI.STA[4] BUSY bit is cleared to 0).

When writing a new value into the SPI.CTL1[15:12] CDMODE bit field, the internal counter is reset and the new value is used for counting. If the counter counts down to 0 and another command package is sent, the CDMODE needs to be set again. Otherwise the next frames are sent as data with the CS pin signaling data mode.

24.3.8 Protocol Descriptions

The protocol format mode can be selected by using the SPI.CTL0[6:5] FRF bit field. The supported options include Motorola 3-wire, Motorola 4-wire, Texas Instruments Synchronous and MICROWIRE.

24.3.8.1 Motorola SPI Frame Format

The Motorola SPI is a 4-wire interface where the CS signal behaves as a peripheral select. In the 3-wire mode the CS signal is not required and the module behaves as if always selected. The main feature of the Motorola SPI format is that the inactive state and phase of the SCLK signal can be programmed through the SPO and SPH bits in the SPI.CTL0 control register.

SPO Clock Polarity Bit

If the SPI.CTL0[8] SPO clock polarity control bit is cleared, the SCLK pin outputs a steady-state low value when data is not being transferred. If the SPI.CTL0[8] SPO bit is set, the SCLK pin outputs a steady-state high value when data is not being transferred.

SPH Phase-Control Bit

The SPI.CTL0[9] SPH phase-control bit selects the clock edge that captures data. The state of this bit has the most impact on the first bit transmitted, by either allowing or not allowing a clock transition before the first data capture edge. If the SPI.CTL0[9] SPH phase-control bit is cleared, data is captured on the first clock edge transition. If the SPH bit is set, data is captured on the second clock edge transition.

Note

For all combinations of SPO and SPH, the minimum CS inactive period (where CS is held high) must be at least one SCLK period wide.

Motorola SPI Frame Format with SPO = 0 and SPH = 0

Figure 24-2 shows signal sequences for Motorola SPI format with SPO = 0 and SPH = 0.

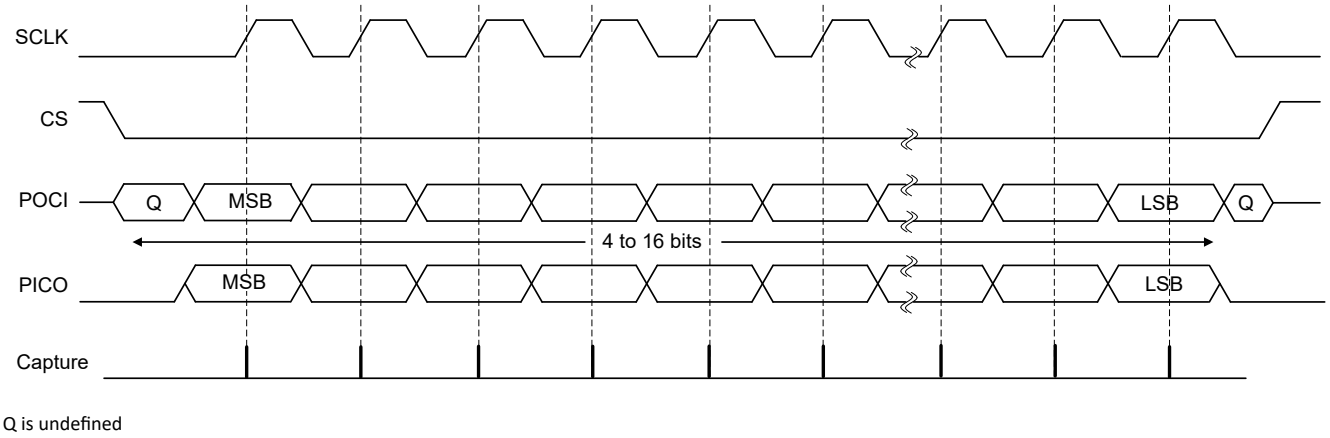


Figure 24-2. Motorola SPI Frame Format with SPO=0 and SPH=0

In this configuration, the following occurs during idle periods:

- SCLK is forced low
- CS is forced high
- The transmit data line PICO is forced low
- When the SPI is configured as a controller, the SCLK pin is enabled
- When the SPI is configured as a peripheral, the SCLK pin is disabled

If the SPI is enabled and valid data is in the TX FIFO, the CS controller signal is driven low at the start of transmission which causes enabling of peripheral data onto the POCI input line of the controller. The controller PICO output pin is enabled.

One-half SCLK period later, valid controller data is transferred to the PICO pin. Once both the controller and peripheral data is set, the SCLK controller clock pin goes high after an additional one-half SCLK period. The data is now captured on the rising edges and propagated on the falling edges of the SCLK signal.

For a single-word transmission after all bits of the data frame are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS signal must pulse high between each data word transfer because the peripheral-select pin freezes the data in the serial peripheral register and does not allow altering of the data if the SPH bit is clear. The controller device must raise the CS pin of the peripheral device between each data transfer to enable the serial peripheral data write. SPI.CTL0[10] HWCSN described in Section 24.3.6 can be used to override this behavior. When the continuous transfer completes, the CS pin is returned to the IDLE state one SCLK period after the last bit is captured.

Motorola SPI Frame Format with SPO = 0 and SPH = 1

Figure 24-3 shows the signal sequence for Motorola SPI format with SPO = 0 and SPH = 1.

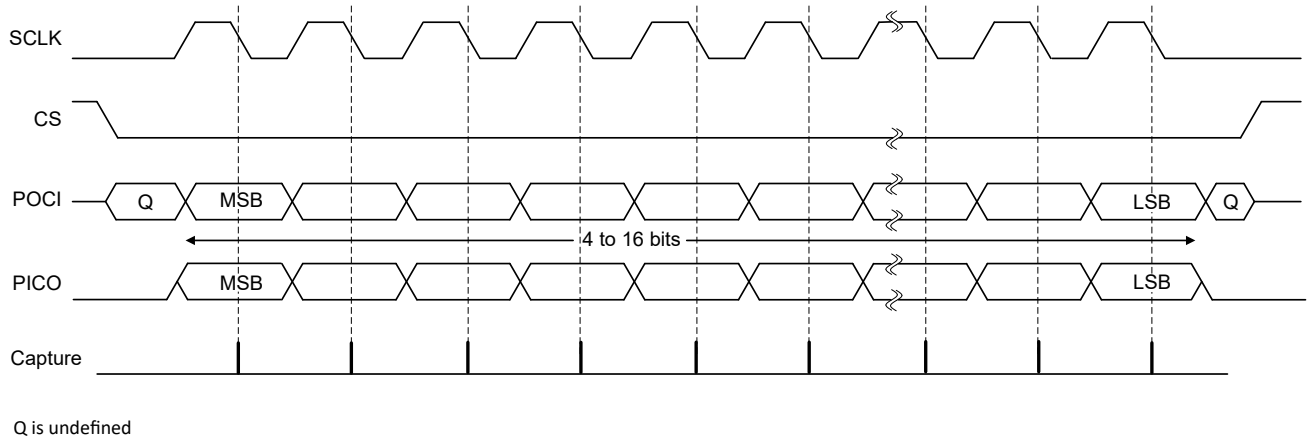


Figure 24-3. Motorola SPI Frame Format with SPO=0 and SPH=1

If the SPI is enabled and valid data is in the TX FIFO, the CS controller signal goes low at the start of transmission. The controller PICO output is enabled. After an additional one-half SCLK period, both controller and peripheral valid data are enabled onto their respective transmission lines. At the same time, SCLK is enabled with a rising-edge transition. Data is then captured on the falling edges and propagated on the rising edges of the SCLK signal.

For a single-word transfer, after all bits are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transfers, the CS pin is held low between successive data words and terminates like a single-word transfer.

Motorola SPI Frame Format with SPO = 1 and SPH = 0

Figure 24-4 shows signal sequences for Motorola SPI format with SPO = 1 and SPH = 0.

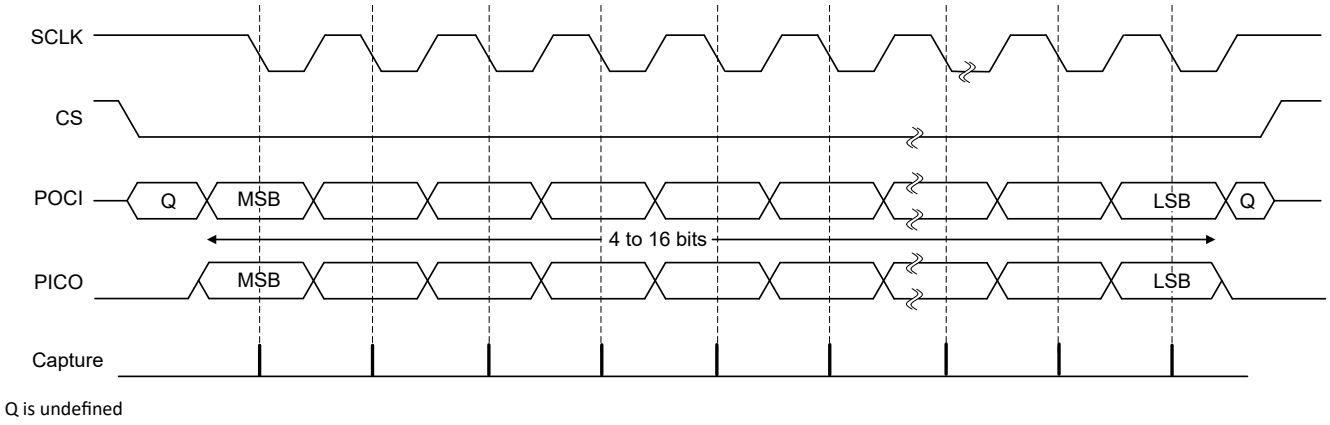


Figure 24-4. Motorola SPI Frame Format with SPO=1 and SPH=0

In this configuration, the following occurs during idle periods:

- SCLK is forced high
- CS is forced high
- The transmit data line PICO is forced low
- When the SPI is configured as a controller, the SCLK pin is enabled
- When the SPI is configured as a peripheral, the SCLK pin is disabled

If the SPI is enabled and valid data is in the TX FIFO, the SPI CS controller signal goes low at the start of transmission and transfers peripheral data onto the POCI line of the controller immediately. The controller PICO output pin is enabled.

One-half SCLK period later, valid controller data is transferred to the PICO line. When both the controller and peripheral data have been set, the SCLK controller clock pin becomes low after one additional half SCLK period. Data is captured on the falling edges and propagated on the rising edges of the SCLK signal.

For a single-word transmission after all bits of the data word are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS signal must pulse high between each data word transfer as the peripheral-select pin freezes the data in the serial peripheral register and keeps it from being altered if the SPH bit is clear. The controller device must raise the CS pin of the peripheral device between each data transfer to enable the serial peripheral data write. SPI.CTL0[10] HWCSN described in Section 24.3.6 can be used to override this behavior. When the continuous transfer completes, the CS pin returns to its IDLE state one SCLK period after the last bit is captured.

Motorola SPI Frame Format with SPO = 1 and SPH = 1

Figure 24-5 shows the signal sequence for Motorola SPI format with SPO = 1 and SPH = 1.

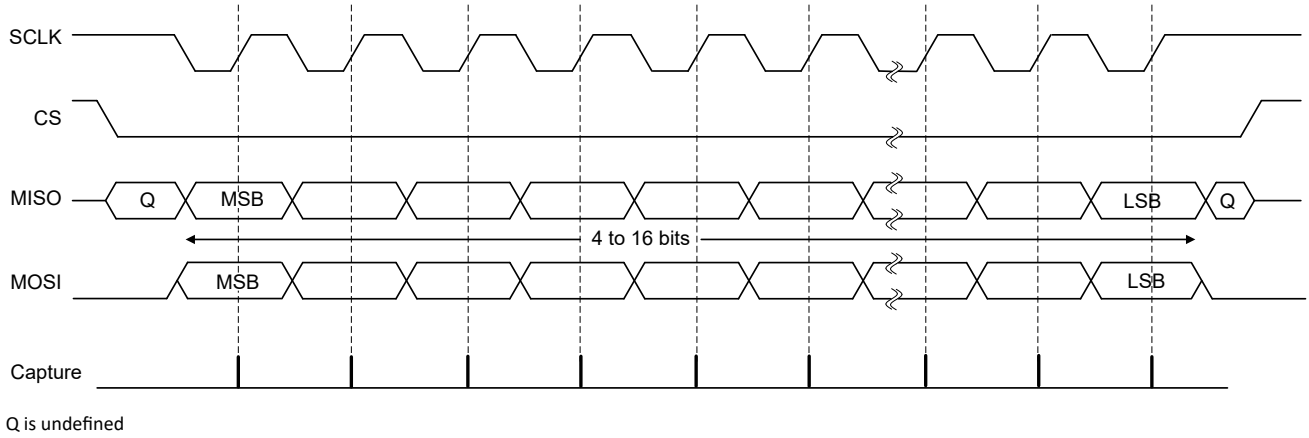


Figure 24-5. Motorola SPI Frame Format with SPO=1 and SPH=1

In this configuration, the following occurs during idle periods:

- SCLK is forced high
- CS is forced high
- The transmit data line PICO is forced low
- When the SPI is configured as a controller, the SCLK pin is enabled
- When the SPI is configured as a peripheral, the SCLK pin is disabled

If the SPI is enabled and valid data is in the TX FIFO, the start of transmission is signified by the CS controller signal going low. The controller PICO output pin is enabled. After an additional one-half SCLK period, both controller and peripheral data are enabled onto their respective transmission lines. At the same time, SCLK is enabled with a falling-edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SCLK signal.

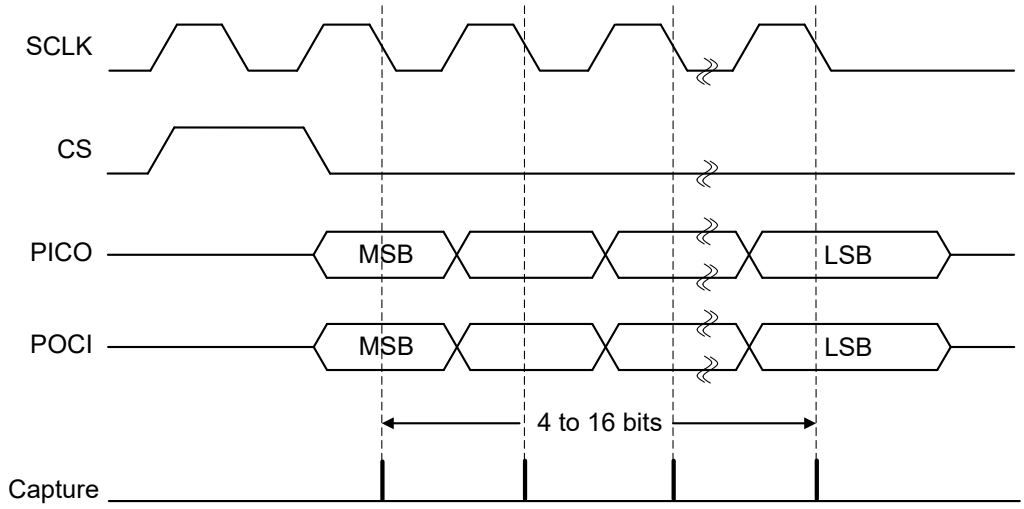
For a single word transmission, after all bits are transferred, the CS line returns to its IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS pin remains in its active low state until the final bit of the last word is captured and then returns to its IDLE state. For continuous back-to-back transfers, the CS pin is held low between successive data words and terminates like a single-word transfer.

The serial clock (SCLK) is held inactive while the SPI is idle and SCLK transitions at the programmed frequency only during active transmission or reception of data. The IDLE state of SCLK provides a receive timeout indication that occurs when the RX FIFO still contains data after a timeout period.

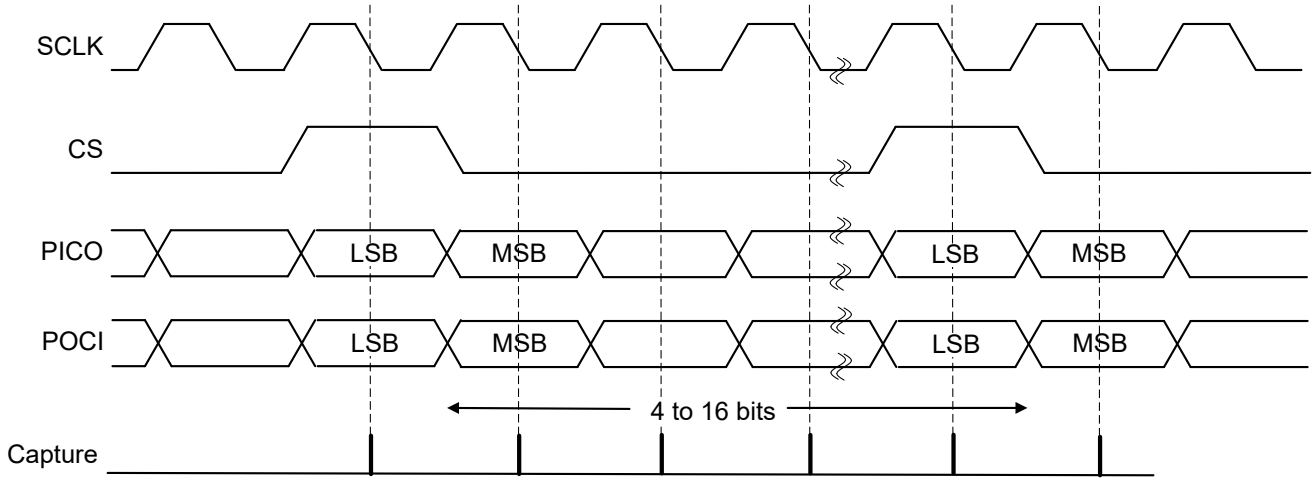
24.3.8.2 Texas Instruments Synchronous Serial Frame Format

The SPI module is compatible with Texas Instruments Synchronous Serial frame format.

Figure 24-6 shows the TI synchronous serial frame format for a single and continuous transmitted frame.



Single Transmission Signal Sequences



Continuous Transmission Signal Sequences

Figure 24-6. TI Synchronous Serial Frame Format

SCLK and CS are forced low and the transmit data line PICO is put in tristate whenever the SPI is idle. When the TX FIFO contains data, CS is pulsed high for one SCLK period. The transmitted value is also transferred from the TX FIFO to the serial shift register of the transmit logic. On the next rising edge of SCLK, the MSB of the 4- to 16-bit data frame is shifted out on the PICO pin. Likewise, the MSB of the received data is shifted onto the POCI pin by the off-chip serial peripheral device. Both the SPI and the off-chip serial peripheral device then

clock each data bit into their serial shifter on each falling edge of SCLK. The received data is transferred from the serial shifter to the RX FIFO on the first rising edge of SCLK after the least significant bit (LSB) is latched.

The serial clock (SCLK) is held inactive while the SPI is idle and SCLK transitions at the programmed frequency only during active transmission or reception of data. The IDLE state of SCLK provides a receive time-out indication that occurs when the RX FIFO still contains data after a time-out period.

24.3.8.3 MICROWIRE Frame Format

Figure 24-7 shows the MICROWIRE frame format for a single frame. Figure 24-8 shows the same format when back-to-back frames are transmitted.

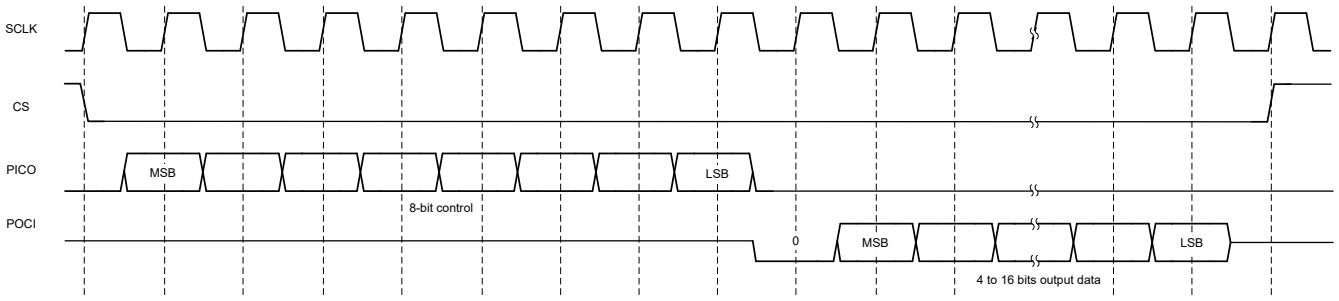


Figure 24-7. MICROWIARE Frame Format (Single Frame)

MICROWIRE format is similar to SPI format, except that transmission is half-duplex and uses a controller-peripheral message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SPI to the off-chip peripheral device. During this transmission, the SPI does not receive incoming data. After the message is sent, the off-chip peripheral decodes the message and waits one serial clock after the last bit of the 8-bit control message is sent. The off-chip peripheral then responds with the required data. The returned data is 4 to 16 bits long, making the total frame length anywhere from 13 to 25 bits.

In this configuration, the following occurs during idle periods:

- SCLK is forced low
- CS is forced high
- The transmit data line, PICO, is typically forced low

Writing a control byte to the TX FIFO triggers a transmission. The falling edge of CS transfers the value of the TX FIFO to the serial shift register of the transmit logic and shifts the MSB of the 8-bit control frame out onto the PICO pin. CS remains low for the duration of the frame transmission. The POCI pin remains in the tri-state condition during this transmission.

The off-chip serial peripheral device latches each control bit into the serial shifter on each rising edge of SCLK. After the last bit is latched by the peripheral device, the control byte is decoded during a one clock wait state and the peripheral responds by transmitting data back to the SPI. Each bit is driven onto the POCI line on the falling edge of SCLK. The SPI latches each bit on the rising edge of SCLK. At the end of the frame for single transfers, the CS signal is pulled high one clock period after the last bit is latched in the receive serial shifter transferring the data to the RX FIFO.

Note

The off-chip peripheral device can place the receive line in a tri-state condition either on the falling edge of SCLK (after the LSB has been latched by the receive shifter), or when the CS pin goes high.

For continuous transfers, data transmission begins and ends like a single transfer, but the CS line is held low and data transmits back-to-back. The control byte of the next frame follows the LSB of the received data from the current frame. After the LSB of the frame is latched into the SPI, each received value is transferred from the receive shifter on the falling edge of SCLK.

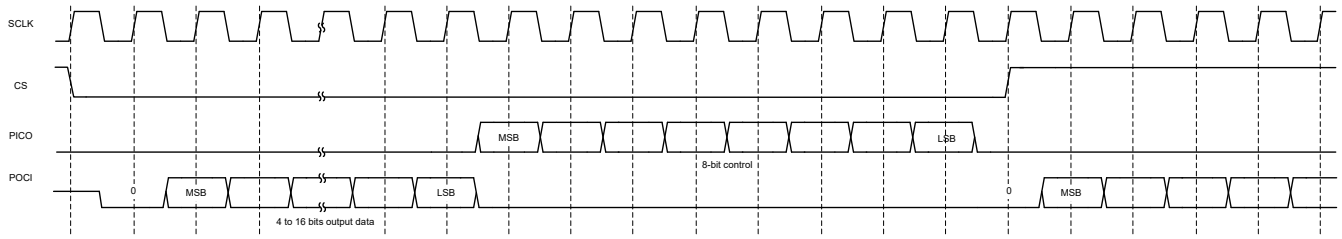


Figure 24-8. MICROWIRE Frame Format (Continuous Transfer)

In the MICROWIRE mode, the SPI peripheral samples the first bit of receive data on the rising edge of SCLK after CS has gone low. Controllers driving a free-running SCLK must ensure that the CS signal has sufficient setup and hold margins with respect to the rising edge of SCLK.

24.3.9 CRC Configuration

- CRC8-CCITT and CRC16-CCITT schemes are implemented in the SPI module independently for transmit and receive operations.
- CRC functionality shall be enabled by application when SPI frame size is only 8-bits or 16-bits.
- This is a software guideline and no specific check is done in hardware based on frame size configuration.
- For 8-bit transfers, CRC8 or CRC16 schemes can be selected by application.
- For 16-bit transfers, CRC16 scheme has to be selected.
- The CRC on TX and RX paths are always active and there is no need to enable CRC functionality explicitly in software.

Transmitter side operation (CRC8/CR16) :

- The TX CRC block is logically located between the SPI.TXDATA register and TXFIFO in the design.
- Select CRC polynomial (8 or 16) based on SPI data frame size (selection applies to both TX and RX CRC units).
- TX side CRC state register resets to the seed value of 0xFF or 0xFFFF.
- When the bus controller (CPU or µDMA) writes data into SPI.TXDATA register, the data is written into the TXFIFO and at the same time used to update the SPI.TXCRC register by hardware logic.
- Data from TXFIFO gets loaded into shift register and transmitted out.
- After the required amount of data has been written into SPI.TXDATA register, the software has to read the SPI.TXCRC state register.
- Software must write the obtained CRC checksum into the SPI.TXDATA register for transmission.
- Initialize SPI.TXCRC state register and repeat this sequence for every block of SPI data transmission.

Receiver side operation (CRC8/CRC16) :

- The RX CRC block is logically located between RXDATA and RXFIFO in the design.
- Select CRC polynomial (8 or 16) based on the SPI data frame size (selection applies to both TX and RX CRC units).
- The RX side CRC state register resets to the seed value of 0xFF or 0xFFFF.
- Data is received into shift register and gets loaded into RXFIFO during receive operation.
- When the bus controller (CPU or µDMA) reads data from the SPI.RXDATA register, the data is returned from RXFIFO and at the same time used to update the SPI.RXCRC state register by hardware logic.
- After the required amount of data have been read from SPI.RXDATA, software can either:
  - Read out the received checksum and then check the SPI.RXCRC state which is zero if there are no errors
  - Read out the SPI.RXCRC state and then read out the checksum through SPI.RXDATA and compare the two values
- Initialize SPI.RXCRC state register and repeat this sequence for every block of SPI data reception.

In case SPI functionality is not being used, the CRC engine can be used as a general-purpose CRC generator.

CTL0.GPCRCEN register bit can be set to enable this functionality. The transmit side CRC can then be used by application software when SPI enable is zero.

24.3.10 Auto CRC Functionality

The SPI includes a feature to automatically insert CRC when the TX FIFO underflows. This feature can be enabled by the SPI.CTL0[14] AUTOCRC bit.

When this bit is set, SPI module loads the calculated CRC checksum into the TX FIFO after all bytes are transmitted when TXFIFO underflow is signaled. This causes the CRC to be transmitted out automatically at the end of the data block.

There is no need for software to read and load this CRC value into the FIFO via a TXDATA register write.

Software must read the SPI.TXCRC[31] AUTOINS bit to reinitialize the TX CRC engine to a seed of all ones after the transfer of data and CRC is done.

Similarly, after reading all the received data via SPI.RXDATA register, software must read the SPI.RXCRC register to obtain the CRC value and auto-initialize the RX CRC engine to a seed value of all ones.

Note

Care must be taken to ensure that the TXFIFO does not empty and signal an underflow if FIFO filling and SPI transmission are occurring in parallel. This can lead to a CRC being automatically inserted at an unwanted instant. When operating at SPI rates 8 MHz or higher, it is advisable to ensure that the TXFIFO is loaded with all the required data (or at least two data frames) before enabling SPI transfers with Auto CRC enabled.

Note

In MICROWIRE frame format, the AUTOCRC feature only supports CRC8 configuration in controller mode.

24.3.11 Auto Header Functionality

When SPI is to be used within a transceiver setting with strict timing requirements in peripheral mode response, the software overhead associated with loading/transmitting data can, in some cases, be limiting.

In order to ensure that the latest data (for example FIFO level, RSSI value, event flags etc.) is contained in the peripheral header, a mechanism to atomically update the FIFO with header data several times before the external controller starts a SPI transmission is included.

In transceiver applications, commonly the peripheral header will contain some type of status data which needs to be kept as updated as possible, as the utility of the data might decay in usefulness when stale - for example, signal strength and FIFO levels etc. In such cases every time a newer update to the data is available, the old values would need to be flushed from the FIFO and newer values updated. This would take several write and poll operations when run by the CPU. The header update feature combines a lot of these steps and provides an atomic operation which can be triggered from the CPU to increase throughput.

SPI.TXFHDR32, SPI.TXFHDR24, SPI.TXFHDR16, and SPI.TXFHDR8 registers are included within the SPI module. When any of these registers are written:

- The write is ignored if the external controller has already started transmission by pulling the CS low
- If no active SPI transmission is ongoing, the RXFIFO and TXFIFO pointers are reset
- The TX CRC engine is reset to a value of all ones
- Depending on whether TXFHDR8, TXFHDR16, TXFHDR24, TXFHDR32 registers are written – 1, 2, 3 or 4 bytes of data are written into the TXFIFO in consecutive CLKSVT cycles
- µDMA and CPU interrupts are blocked until the written header is committed on the POCI, after the controller starts SPI transmissions, so that no active CPU or µDMA jobs fill up the TXFIFO at the same time as the header gets updated by this feature.

The SPI.TXFHDRC register is included to control this feature. The SPI.TXFHDRC register contains these fields:

- HDREN – This bit has to be set to enable atomic header feature when CSGATE is set to BLK. Otherwise, any write to TXFHDR registers sets this bit automatically

- HDRCMT – This bit is set when the external controller pulls the CS low and the peripheral commits the header written into the FIFO on the POCI. This bit continues to be set till cleared by software. The hold on CPU or µDMA interrupt lines is released when this bit is set.
- HDRIGN – This bit is set when a write to header registers occurs after the HDRCMT is set. This bit can be polled by software to figure out whether the last payload was written to the TXFIFO or not.
- CSGATE – This is set to UNBLK by default. The first header write can occur even when CS is low (active). When CSGATE is set to BLK, the header writes must occur only when CS is inactive.

SPI.CTL0[17] IDLEPOCI register bit is included to drive a configurable high/low value of the POCI pin to ease signaling to the controller about a change in the peripheral readiness. If the MSB of header data written into the FIFO is opposite to the IDLEPOCI, the external controller can detect the same by polling the POCI pin.

24.3.12 SPI Status

The external controller is supposed to always send the number of clocks equal to the DSS value written, before de-asserting CS and ending transmission. In case CS is deactivated before the entire data frame has been sent out by the peripheral, then CSD error bit is set and can be read within SPI.STA[5] CSD. This bit, once set, must be cleared by software.

The TX FIFO full level indicating the number of entries written into the TXFIFO can be read out via the SPI.STA[13:8] TXFIFOLVL bit field.

Additional status bits related to peripheral mode transfer complete, SPI busy indication, TX and RX FIFO flags can be read out from the SPI.STA register. The peripheral mode transfer complete indication bit, once set, must be cleared by software.

24.3.13 Debug Halt

Debug halt is available in the SPI module and is controlled by the SPI.EMU register. When the SPI.EMU[0] HALT bit is set to 1, the SPI module freezes operations as described below.

- If SPI is configured in Controller mode, then debug halt freezes SPI operations at the next DSS boundary.
- If SPI is configured in Peripheral mode, then debug halt freezes SPI operations immediately.
- FIFO pointers are not incremented if RXDATA read is attempted during debug halt.

24.4 µDMA Operation

The SPI module provides an interface to the µDMA controller with separate channels for transmit and receive. The SPI DMA Control register (SPI.DMACR) allows the µDMA to operate with the SPI. When µDMA operation is enabled, the SPI asserts a µDMA request on the receive or transmit channel when the associated FIFO can transfer data. For the receive channel, a single transfer request is asserted whenever any data is in the RX FIFO. Whenever data in the RX FIFO reaches the configured level set in the SPI.IFLS[10:8] RXSEL bit field, a burst transfer request is asserted. The supported settings for RX FIFO are: ¼, ½ (default), ¾, full, and at least one location is available in the FIFO. For the transmit channel, a single transfer request is asserted whenever at least one empty location is in the TX FIFO. Whenever the TX FIFO reaches the configured level set via SPI.IFLS[2:0] TXSEL, the burst request is asserted. The supported settings for TX FIFO are: ¼, ½ (default), ¾, empty, at least one location is available in the FIFO. The µDMA controller handles the single and burst µDMA transfer requests automatically depending on how the µDMA channel is configured.

Note

Software must avoid ¾ threshold selection for µDMA operation.

To enable µDMA operation for the receive channel, set the SPI.DMACR[0] RXEN bit. To enable µDMA operation for the transmit channel, set the SPI.DMACR[8] TXEN register bit. If the µDMA is enabled and appropriate bits are cleared in the DMA Done Mask register (DMA.DONEMASK) the µDMA controller triggers an interrupt when a transfer completes. This interrupt can be chosen as one of the sources of the combined SPI interrupt. If interrupts are used for SPI operation and the µDMA is enabled, the SPI interrupt handler must be designed to handle the µDMA completion interrupt. The status of TX and RX DMA done interrupts can be read from the Channel Request Done register (DMA.REQDONE). They can also be read from SPI.RIS[8] DMATX bit and

the SPI.RIS[7] DMARX bit. For clearing the TX and RX DMA done interrupts, the corresponding bits in the DMA.REQDONE register must be set to 1.

For more details about programming the µDMA controller, see Chapter 19

24.5 Initialization and Configuration

The following describes the necessary steps to enable and initialize the SPI.

TI recommends using the SPI driver in the SimpleLink™ Low Power F3 Software Development Kit (SDK) when using the SPI.

1. Ensure the SVT power domain is powered up properly.

2. Enable the SPI module clock in CLKCTL by setting the CLKCTL.CLKCFG0[10] SPI0 bit.

3. Configure the IOC module to route the PICO, POCI, CS, and SCLK functionality from I/Os to the SPI module. IOCFGn.PORTCFG must be written to the correct IDs.

For each of the frame formats, the SPI is configured using the following steps:

1. Make sure that the SPI.CTL1[0] ENABLE bit is cleared before making any configuration changes
2. Configure the clock pre-scaler divisor by writing to the SPI.CLKCFG0[2:0] PRESC and SPI.CLKCFG1[9:0] SCR bit fields
3. Write the SPI.CTL0 register with the following configuration:
   a. Desired clock phase and polarity, if using Motorola™ SPI mode (SPH and SPO)
   b. The protocol mode: Motorola SPI (4-wire or 3-wire) , TI SSF, MICROWIRE (FRF)
   c. The data size (DSS)
4. Select whether the SPI is a controller or peripheral:
   a. For controller operations, SPI.CTL1[2] MS is 1
   b. For peripheral mode (output enabled), SPI.CTL1[2] MS bit is 0
   c. For peripheral mode (output disabled), clear the SPI.CTL1[2] MS bit to 0 and set the SPI.CTL1[3] POD bit to 1
5. Optionally, configure the µDMA channel (see Chapter 19) and enable the µDMA options in the SPI.DMACR register
6. Enable the SPI by setting the EN bit in the SPI.CTL1 register

As an example, assume that the SPI configuration is required to operate with the following parameters:

- Controller operation
- Texas Instruments Synchronous SPI mode
- 1-Mbps bit rate
- 8 data bits

Assuming the system clock is 48 MHz, the bit-rate calculation is shown in Equation 11

$$SCLK = CLKSVT / [PRESC \times (1 + SCR)] \quad (11)$$

Example: 1000000 bps = 48000000 Hz / [2 × (1 + 23)]

In this case, if PRESC = 0x2, SCR must be 0x17.

The configuration sequence is:

- Verify that the EN bit in the SPI.CTL1 register is cleared
- Write the SPI.CLKCFG0 register with a value of 0x00000002
- Write the SPI.CLKCFG1 register with a value of 0x00000017
- Write the SPI.CTL0 register with a value of 0x00000047
- Write the SPI.CTL1 register with a value of 0x00000004
- The SPI is then enabled by setting the EN bit in the SPI.CTL1 register

24.6 SPI Registers

Table 24-2 lists the memory-mapped registers for the SPI registers. All register offset addresses not listed in Table 24-2 should be considered as reserved locations and the register contents should not be modified.

Table 24-2. SPI Registers

Offset	Acronym	Register Name	Section
0h	DESC	Module Description	Section 24.6.1
44h	IMASK	Interrupt mask	Section 24.6.2
48h	RIS	Raw interrupt status	Section 24.6.3
4Ch	MIS	Masked interrupt status	Section 24.6.4
50h	ISET	Interrupt set	Section 24.6.5
54h	ICLR	Interrupt clear	Section 24.6.6
58h	IMSET	Interrupt mask set	Section 24.6.7
5Ch	IMCLR	Interrupt mask clear	Section 24.6.8
60h	EMU	Emulation	Section 24.6.9
64h	DTB	Digital Test Bus	Section 24.6.10
100h	CTL0	Control 0	Section 24.6.11
104h	CTL1	Control 1	Section 24.6.12
108h	CLKCFG0	Clock configuration 0	Section 24.6.13
10Ch	CLKCFG1	Clock configuration 1	Section 24.6.14
110h	IFLS	Interrupt FIFO Level Select	Section 24.6.15
114h	DMACR	DMA control	Section 24.6.16
118h	RXCRC	Receive CRC	Section 24.6.17
11Ch	TXCRC	Transmit CRC	Section 24.6.18
120h	TXFHDR32	Header write for 32bits	Section 24.6.19
124h	TXFHDR24	Header write for 24bits	Section 24.6.20
128h	TXFHDR16	Header write for 16bits	Section 24.6.21
12Ch	TXFHDR8	Header write for 8bits	Section 24.6.22
130h	TXFHDRC	Atomic header control	Section 24.6.23
140h	RXDATA	Receive data	Section 24.6.24
150h	TXDATA	Transmit data	Section 24.6.25
160h	STA	Status	Section 24.6.26

Complex bit access types are encoded to fit into small table cells. Table 24-3 shows the codes that are used for access types in this section.

Table 24-3. SPI Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

24.6.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 24-4.

Return to the Summary Table.

Description Register. This register provides IP module ID, revision information, instance index and standard MMR registers offset.

Table 24-4. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	604Dh	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB. 0: Standard IP MMRs do not exist 0x1-0xF: Standard IP MMRs begin at offset of (64*STDIPOFF from the base IP address)
11-8	INSTIDX	R	0h	IP Instance ID number. If multiple instances of IP exist in the device, this field can identify the instance number (0-15).
7-4	MAJREV	R	1h	Major revision of IP (0-15).
3-0	MINREV	R	0h	Minor revision of IP (0-15).

24.6.2 IMASK Register (Offset = 44h) [Reset = 00000000h]

IMASK is shown in Table 24-5.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from [RIS.*] to [MIS.*] when the corresponding bit-fields are set to 1.

Table 24-5. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	R/W	0h	DMA Done TX event mask. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	DMARX	R/W	0h	DMA Done RX event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	IDLE	R/W	0h	SPI Idle event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	TXEMPTY	R/W	0h	Transmit FIFO Empty event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	TX	R/W	0h	Transmit FIFO event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	RX	R/W	0h	Receive FIFO event. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	RTOUT	R/W	0h	SPI Receive Time-Out event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	PER	R/W	0h	Parity error event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	RXOVF	R/W	0h	RXFIFO overflow event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

24.6.3 RIS Register (Offset = 48h) [Reset = 00000000h]

RIS is shown in Table 24-6.

Return to the Summary Table.

Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 24-6. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	R	0h	DMA Done event for TX. This interrupt is set if the TX DMA channel sends the DONE signal. This allows the handling of the TX DMA event inside SPI. 0h = Interrupt did not occur 1h = Interrupt occurred
7	DMARX	R	0h	DMA Done event for RX. This interrupt is set if the RX DMA channel sends the DONE signal. This allows handling of the DMA RX event inside SPI. 0h = Interrupt did not occur 1h = Interrupt occurred
6	IDLE	R	0h	SPI has completed transfers and moved to IDLE mode. This bit is set when BUSY goes low. 0h = Interrupt did not occur 1h = Interrupt occurred
5	TXEMPTY	R	0h	Transmit FIFO Empty interrupt mask. This interrupt is set when all data in the Transmit FIFO has been moved to the shift register. 0h = Interrupt did not occur 1h = Interrupt occurred
4	TX	R	0h	Transmit FIFO event. This interrupt is set if the selected Transmit FIFO level has been reached. 0h = Interrupt did not occur 1h = Interrupt occurred
3	RX	R	0h	Receive FIFO event. This interrupt is set if the selected Receive FIFO level has been reached 0h = Interrupt did not occur 1h = Interrupt occurred
2	RTOUT	R	0h	SPI Receive Time-Out event. This interrupt is set if no activity is detected on the input clock line within the time period dictated by RTOUT value. This is applicable only in peripheral mode. 0h = Interrupt did not occur 1h = Interrupt occurred
1	PER	R	0h	Parity error event. This bit is set if a Parity error has been detected 0h = Interrupt did not occur 1h = Interrupt occurred
0	RXOVF	R	0h	RXFIFO overflow event. This interrupt is set if an RX FIFO overflow has been detected. 0h = Interrupt did not occur 1h = Interrupt occurred

24.6.4 MIS Register (Offset = 4Ch) [Reset = 00000000h]

MIS is shown in Table 24-7.

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Masked interrupt status. This register is simply a bitwise AND of the contents of [IMASK.*] and [RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding [ICLR.*] register bit.

Table 24-7. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	R	0h	Masked DMA Done event for TX. 0h = Interrupt did not occur 1h = Interrupt occurred
7	DMARX	R	0h	Masked DMA Done event for RX. 0h = Interrupt did not occur 1h = Interrupt occurred
6	IDLE	R	0h	Masked SPI IDLE event. 0h = Interrupt did not occur 1h = Interrupt occurred
5	TXEMPTY	R	0h	Masked Transmit FIFO Empty event. 0h = Interrupt did not occur 1h = Interrupt occurred
4	TX	R	0h	Masked Transmit FIFO event. 0h = Interrupt did not occur 1h = Interrupt occurred
3	RX	R	0h	Masked Receive FIFO event. 0h = Interrupt did not occur 1h = Interrupt occurred
2	RTOUT	R	0h	Masked SPI Receive Time-Out event. 0h = Interrupt did not occur 1h = Interrupt occurred
1	PER	R	0h	Masked Parity error event. 0h = Interrupt did not occur 1h = Interrupt occurred
0	RXOVF	R	0h	Masked RXFIFO overflow event. 0h = Interrupt did not occur 1h = Interrupt occurred

24.6.5 ISET Register (Offset = 50h) [Reset = 00000000h]

ISET is shown in Table 24-8.

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Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding [RIS.*] bit also gets set. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets set.

Table 24-8. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	W	0h	Set DMA Done event for TX. 0h = Writing 0 has no effect 1h = Set Interrupt
7	DMARX	W	0h	Set DMA Done event for RX. 0h = Writing 0 has no effect 1h = Set Interrupt
6	IDLE	W	0h	Set SPI IDLE event. 0h = Writing 0 has no effect 1h = Set Interrupt
5	TXEMPTY	W	0h	Set Transmit FIFO Empty event. 0h = Writing 0 has no effect 1h = Set Interrupt
4	TX	W	0h	Set Transmit FIFO event. 0h = Writing 0 has no effect 1h = Set Interrupt
3	RX	W	0h	Set Receive FIFO event. 0h = Writing 0 has no effect 1h = Set Interrupt
2	RTOUT	W	0h	Set SPI Receive Time-Out Event. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
1	PER	W	0h	Set Parity error event. 0h = Writing 0 has no effect 1h = Set Interrupt
0	RXOVF	W	0h	Set RXFIFO overflow event. 0h = Writing 0 has no effect 1h = Set Interrupt

24.6.6 ICLR Register (Offset = 54h) [Reset = 00000000h]

ICLR is shown in Table 24-9.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts. Writing a 1 to a bit in this register will clear the event and the corresponding [RIS.*] bit also gets cleared. If the corresponding [IMASK.*] bit is set, then the corresponding [MIS.*] register bit also gets cleared.

Table 24-9. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	W	0h	Clear DMA Done event for TX. 0h = Writing 0 has no effect 1h = Clear Interrupt
7	DMARX	W	0h	Clear DMA Done event for RX. 0h = Writing 0 has no effect 1h = Clear Interrupt
6	IDLE	W	0h	Clear SPI IDLE event. 0h = Writing 0 has no effect 1h = Clear Interrupt
5	TXEMPTY	W	0h	Clear Transmit FIFO Empty event. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	TX	W	0h	Clear Transmit FIFO event. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	RX	W	0h	Clear Receive FIFO event. 0h = Writing 0 has no effect 1h = Clear Interrupt
2	RTOUT	W	0h	Clear SPI Receive Time-Out Event. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
1	PER	W	0h	Clear Parity error event. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	RXOVF	W	0h	Clear RXFIFO overflow event. 0h = Writing 0 has no effect 1h = Clear Interrupt

24.6.7 IMSET Register (Offset = 58h) [Reset = 00000000h]

IMSET is shown in Table 24-10.

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Interrupt mask set register. Writing a 1 to a bit in this register will set the corresponding [IMASK.*] bit.

Table 24-10. IMSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	W	0h	Set DMA Done for TX event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
7	DMARX	W	0h	Set DMA Done for RX event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
6	IDLE	W	0h	Set SPI IDLE event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
5	TXEMPTY	W	0h	Set Transmit FIFO Empty event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
4	TX	W	0h	Set Transmit FIFO event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
3	RX	W	0h	Set Receive FIFO event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
2	RTOUT	W	0h	Set SPI Receive Time-Out event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
1	PER	W	0h	Set Parity error event mask 0h = Writing 0 has no effect 1h = Set interrupt mask
0	RXOVF	W	0h	Set RXFIFO overflow event mask 0h = Writing 0 has no effect 1h = Set interrupt mask

24.6.8 IMCLR Register (Offset = 5Ch) [Reset = 00000000h]

IMCLR is shown in Table 24-11.

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Interrupt mask clear register. Writing a 1 to a bit in this register will clear the corresponding [IMASK.*] bit.

Table 24-11. IMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	DMATX	W	0h	Clear DMA Done for TX event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
7	DMARX	W	0h	Clear DMA Done for RX event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
6	IDLE	W	0h	Clear SPI IDLE event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
5	TXEMPTY	W	0h	Clear Transmit FIFO Empty event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
4	TX	W	0h	Clear Transmit FIFO event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
3	RX	W	0h	Clear Receive FIFO event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
2	RTOUT	W	0h	Clear SPI Receive Time-Out event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
1	PER	W	0h	Clear Parity error event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask
0	RXOVF	W	0h	Clear RXFIFO overflow event mask 0h = Writing 0 has no effect 1h = Clear interrupt mask

24.6.9 EMU Register (Offset = 60h) [Reset = 00000000h]

EMU is shown in Table 24-12.

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Emulation control register. This register controls the behavior of the IP related to core halted input.

Table 24-12. EMU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	HALT	R/W	0h	Halt control 0h = Free run option. The IP ignores the state of the core halted input. 1h = Freeze option. The IP freezes functionality when the core halted input is asserted, and resumes when it is deasserted. The freeze can either be immediate or after the IP has reached a boundary (end of word boundary, based on DSS configuration) from where it can resume without corruption.

24.6.10 DTB Register (Offset = 64h) [Reset = 00000000h]

DTB is shown in Table 24-13.

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Digital test bus control register. This register can be used to bring out IP internal signals to the pads for observation. 16 signals can be observed per select value.

Table 24-13. DTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2-0	SEL	R/W	0h	Digital test bus selection mux control. Non-zero select values output a 16 bit selected group of signals per value.

24.6.11 CTL0 Register (Offset = 100h) [Reset = 00000000h]

CTL0 is shown in Table 24-14.

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SPI control register 0

Table 24-14. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	
17	IDLEPOCI	R/W	0h	The Idle value of POCI - when TXFIFO is empty and before data is written into TXFIFO - can be controlled by this field. 0h (R/W) = POCI output idle value of '0' 1h (R/W) = POCI outputs idle value of '1'
16	GPCRCEN	R/W	0h	General purpose CRC enable. This bit enables transmit side CRC unit for general purpose use by software when SPI is disabled (EN = 0). This bit must be 0 when SPI is enabled. 0h = Transmit side CRC unit is not available for general purpose software use 1h = Transmit side CRC unit is available for general purpose software use
15	CRCPOLY	R/W	0h	CRC polynomial selection. 0h = Selects 8-bit CCITT CRC polynomial 1h = Selects 16-bit CCITT CRC polynomial
14	AUTOCRC	R/W	0h	Auto insert CRC 0h (R/W) = Do not insert CRC into TXFIFO upon TXFIFO underflow 1h (R/W) = Insert CRC into TXFIFO upon TXFIFO underflow
13	CRCEND	R/W	0h	CRC16 Endianness 0h (R/W) = Auto-insertion of CRC16 is most-significant byte first 1h (R/W) = Auto-insertion of CRC16 is least-significant byte first
12	CSCLR	R/W	0h	Clear shift register counter on CS inactive. This bit is relevant only in the peripheral mode, when MS=0. 0h = Disable automatic clear of shift register when CS goes inactive. 1h = Enable automatic clear of shift register when CS goes inactive.
11	FIFORST	R/W	0h	This bit is used to reset transmit and receive FIFO pointers. This bit is auto cleared once the FIFO pointer reset operation is completed. 0h = FIFO pointers reset completed when 0 is read 1h = Trigger FIFO pointers reset when written to 1.
10	HWCSN	R/W	0h	Hardware controlled chip select (CS) value. When set CS is zero till TX FIFO is empty, as in - a. CS is de-asserted b. All data bytes are transmitted c. CS is asserted 0h (R/W) = HWCSN Disable 1h (R/W) = HWCSN Enable
9	SPH	R/W	0h	SCLK phase (Motorola SPI frame format only). This bit selects the clock edge that captures data and enables it to change state. It has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture clock edge. 0h = Data is captured on the first clock edge transition. 1h = Data is captured on the second clock edge transition.
8	SPO	R/W	0h	SCLK polarity (Motorola SPI frame format only). 0h = SPI produces a steady state LO value on the SCLK 1h = SPI produces a steady state HI value on the SCLK
7	RESERVED	R	0h	
6-5	FRF	R/W	0h	Frame format select 0h = Motorola SPI frame format (3-wire mode) 1h = Motorola SPI frame format (4-wire mode) 2h = TI synchronous serial frame format 3h = MICROWIRE frame format
4	RESERVED	R	0h	

Table 24-14. CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DSS	R/W	0h	Data size select. The applicable DSS values for controller mode operation are 0x3 to 0xF and for peripheral mode operation are 0x6 to 0xF. DSS values 0x0 to 0x2 are reserved and must not be used. 3h (R/W) = 4-bits data size 4h (R/W) = 5-bits data size 5h (R/W) = 6-bits data size 6h (R/W) = 7-bits data size 7h (R/W) = 8-bits data size 8h (R/W) = 9-bits data size 9h (R/W) = 10-bits data size Ah (R/W) = 11-bits data size Bh (R/W) = 12-bits data size Ch (R/W) = 13-bits data size Dh (R/W) = 14-bits data size Eh (R/W) = 15-bits data size Fh (R/W) = 16-bits data size

24.6.12 CTL1 Register (Offset = 104h) [Reset = 00000004h]

CTL1 is shown in Table 24-15.

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SPI control register 1

Table 24-15. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	
29-24	RTOUT	R/W	0h	Receive Timeout (only for Peripheral mode) Defines the number of CLKSVT clock cycles after which the Receive Timeout flag RTOUT is set. A value of 0 disables this function.
23-16	REPTX	R/W	0h	Counter to repeat last transfer (only in controller mode) 0: repeat last transfer is disabled. x: repeat the last transfer with the provided value. The transfer will be started with writing a data into the TX FIFO. Sending the data will be repeated REPTX number of times, so the data will be transferred x+1 times in total. It can be used to clean a transfer or to pull a certain amount of data by a peripheral.
15-12	CDMODE	R/W	0h	Command Data Mode. This bit field value determines the behavior of C/D or CS signal when CDEN = 1. CS pin held low indicates command phase and CS pin held high indicates data phase. When CDMODE = 0x0, the CS pin is always held high during transfer indicating data phase only operation (manual mode). When CDMODE = 0xF, the CS pin is always held low during transfer indicating command phase only operation (manual mode). When CDMODE = 0x1 to 0xE, the CS pin is held low for the number of bytes indicated by CDMODE value for the command phase and held high for the remaining transfers in the data phase (automatic mode). When CDMODE is set to value 0x1 to 0xE, reading CDMODE during operation indicates the remaining bytes to be transferred in the command phase. 0h = Manual mode: Data Fh = Manual mode: Command
11	CDEN	R/W	0h	Command/Data mode enable. This feature is applicable only in controller mode and for 8-bit transfers (DSS = 7). The chip select pin is used for command/data signaling in Motorola SPI frame format (3-wire) operation. 0h = C/D Mode Disable 1h = C/D Mode Enable
10-8	RESERVED	R	0h	
7	PBS	R/W	0h	Parity bit select 0h = Bit 0 is used for Parity 1h = Bit 1 is used for Parity, Bit 0 is ignored
6	PES	R/W	0h	Even parity select. 0h = Odd Parity mode 1h = Even Parity mode
5	PEN	R/W	0h	Parity enable. If enabled the last bit will be used as parity to evaluate the correct reception of the previous bits. In case of parity mismatch the parity error flag PER will be set. This feature is available only in SPI controller mode. 0h = Disable Parity function 1h = Enable Parity function
4	MSB	R/W	0h	MSB first select. Controls the direction of receive and transmit shift register. MSB first configuration (MSB = 1) must be selected when CRC feature is used for SPI communication. 0h = LSB first 1h = MSB first

Table 24-15. CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	POD	R/W	0h	Peripheral data output disable. This bit is relevant only in the peripheral mode, MS=1. In multiple-peripheral systems, it is possible for a SPI controller to broadcast a message to all peripherals in the system while ensuring that only one peripheral drives data onto its serial output line. In such systems the POCI lines from multiple peripherals could be tied together. To operate in such systems, this bit field can be set if the SPI peripheral is not supposed to drive the POCI output. 0h = SPI can drive the POCI output in peripheral mode. 1h = SPI cannot drive the POCI output in peripheral mode.
2	MS	R/W	1h	Controller or peripheral mode select. This bit can be modified only when SPI is disabled, EN=0. 0h = Select Peripheral mode 1h = Select Controller mode
1	LBM	R/W	0h	Loop back mode control 0h = Disable loopback mode. Normal serial port operation enabled. 1h = Enable loopback mode. Output of transmit serial shifter is connected to input of receive serial shifter internally.
0	EN	R/W	0h	SPI enable. NOTE: This bit field must be set to 1 using a separate write access, after the other bit fields have been configured. 0h = SPI is disabled 1h = SPI Enabled and released for operation.

24.6.13 CLKCFG0 Register (Offset = 108h) [Reset = 00000000h]

CLKCFG0 is shown in Table 24-16.

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Clock configuration register 0. This register is used to configure the clock prescaler.

Table 24-16. CLKCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2-0	PRESC	R/W	0h	Prescaler configuration 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

24.6.14 CLKCFG1 Register (Offset = 10Ch) [Reset = 00000000h]

CLKCFG1 is shown in Table 24-17.

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Clock configuration register 1. This register is used to configure serial clock rate and clock count for delayed sampling in controller mode.

Table 24-17. CLKCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	
19-16	DSAMPLE	R/W	0h	Delayed sampling. In controller mode the data on the POCI pin will be delayed sampled by the defined CLKSVT clock cycles. DSAMPLE values can range from 0 to SCR+1. Typically, values of 1 or 2 would suffice.
15-10	RESERVED	R	0h	
9-0	SCR	R/W	0h	Serial clock divider. This is used to generate the transmit and receive bit rate of the SPI. The SPI bit rate: (SPI functional clock frequency)/((SCR+1)*PRESC). SCR value can be from 0 to 1023.

24.6.15 IFLS Register (Offset = 110h) [Reset = 00000202h]

IFLS is shown in Table 24-18.

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Interrupt FIFO level select register. This register can be used to define the levels at which the TX, RX flags are triggered. The interrupts are generated based on FIFO level. Out of reset, the TXSEL and RXSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

Table 24-18. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	
10-8	RXSEL	R/W	2h	Receive FIFO Level Select. The trigger points for the receive interrupt are as follows: 0h = Reserved 1h = RX FIFO >= 1/4 full 2h = RX FIFO >= 1/2 full (default) 3h = RX FIFO >= 3/4 full 4h = Reserved 5h = RX FIFO is full 6h = Reserved 7h = Trigger when RX FIFO contains >= 1 byte
7-3	RESERVED	R	0h	
2-0	TXSEL	R/W	2h	Transmit FIFO Level Select. The trigger points for the transmit interrupt are as follows: 0h = Reserved 1h = TX FIFO <= 3/4 empty 2h = TX FIFO <= 1/2 empty (default) 3h = TX FIFO <= 1/4 empty 4h = Reserved 5h = TX FIFO is empty 6h = Reserved 7h = Trigger when TX FIFO has >= 1 byte free

24.6.16 DMACR Register (Offset = 114h) [Reset = 00000000h]

DMACR is shown in Table 24-19.

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uDMA Control Register

Table 24-19. DMACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	TXEN	R/W	0h	Transmit DMA enable. If this bit is set to 1, DMA for the transmit FIFO is enabled. 0h = Disable TX DMA 1h = Enable TX DMA
7-1	RESERVED	R	0h	
0	RXEN	R/W	0h	Receive DMA enable. If this bit is set to 1, DMA for the receive FIFO is enabled. 0h = Disable RX DMA 1h = Enable RX DMA

24.6.17 RXCRC Register (Offset = 118h) [Reset = 00000000h]

RXCRC is shown in Table 24-20.

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Receive CRC register. Reading this register provides the computed CRC value from the receive side CRC unit. Reading this register or writing to this register with any value auto initializes the seed. The seed value is 0xFF when CRCPOLY = 0 and 0xFFFF when CRCPOLY = 1 for CCITT CRC polynomials. Bits[15:8] are don't care when CRCPOLY = 0.

Table 24-20. RXCRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R/W	0h	CRC value SW should read RXCRC register at the end of data transmission to reinitialize the seed value to all ones

24.6.18 TXCRC Register (Offset = 11Ch) [Reset = 00000000h]

TXCRC is shown in Table 24-21.

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Transmit CRC register. Reading this register provides the computed CRC value from the transmit side CRC unit. Reading this register or writing to this register with any value auto initializes the seed. The seed value is 0xFF when CRCPOLY = 0 and 0xFFFF when CRCPOLY = 1 for CCITT CRC polynomials. Bits[15:8] are don't care when CRCPOLY = 0.

Table 24-21. TXCRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTOCRCINS	RC	0h	Status to indicate if Auto CRC has been inserted into TXFIFO. This is applicable only if AUTOCRC enable bit is set. SW should read TXCRC register to clear auto inserted CRC at the end of the transfer. 0h (R) = Auto CRC not yet inserted 1h (R) = Auto CRC inserted
30-16	RESERVED	R	0h	
15-0	DATA	R/W	0h	CRC value

24.6.19 TXFHDR32 Register (Offset = 120h) [Reset = 00000000h]

TXFHDR32 is shown in Table 24-22.

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Header update register for 32 bits of header data into the TXFIFO.

Table 24-22. TXFHDR32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write four bytes of header data into the TXFIFO

24.6.20 TXFHDR24 Register (Offset = 124h) [Reset = 00000000h]

TXFHDR24 is shown in Table 24-23.

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Header update register for 24 bits of header data into the TXFIFO.

Table 24-23. TXFHDR24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write three bytes of header data into the TXFIFO.

24.6.21 TXFHDR16 Register (Offset = 128h) [Reset = 00000000h]

TXFHDR16 is shown in Table 24-24.

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Header update register for 16 bits of data into the TXFIFO.

Table 24-24. TXFHDR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write two bytes of header data into the TXFIFO.

24.6.22 TXFHDR8 Register (Offset = 12Ch) [Reset = 00000000h]

TXFHDR8 is shown in Table 24-25.

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Header update register for 8 bits of header data into the TXFIFO.

Table 24-25. TXFHDR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This field can be used to write one byte of header data into the TXFIFO.

24.6.23 TXFHDRC Register (Offset = 130h) [Reset = 00000000h]

TXFHDRC is shown in Table 24-26.

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Atomic Header Control register

Table 24-26. TXFHDRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CSGATE	R/W	0h	Chip Select Gating control register. If this bit is set, header update register writes are blocked when chip select (CS) is active low, and HDRIGN bit is set. This bit resets to 0. 0h = The first header update register write is not blocked based on CS active status (low). If no header update occurred when CS was high (inactive), the first header update is allowed when CS is low (active), and the HDRCMT bit is set. The use case is for the external controller to ensure that the SCLK is not driven during this header update. If the header is already updated when CS is high and inactive, HDRCMT is set immediately when CS drops to active low state, and header writes when CS is low are ignored even if this UNBLK bit is set. 1h = Header update register writes are blocked when CS is active (low)
2	HDRCMT	R/W	0h	Header Committed field. This bit is set when the HDREN bit is set and CS is sampled low. This bit remains 0 otherwise. When set, this bit can be written to a value of 0 to clear. 0h = Header update is not committed 1h = Header update is committed
1	HDRIGN	R/W	0h	Header Ignored field. When CSGATE is set to BLK, this bit is set when the last Header update register [TXFHDRn.*] is written when CS is low or HDRCMT is already set. When CSGATE is set to UNBLK, this bit is set only when the header update register is written when HDRCMT is already set. This bit remains 0 otherwise. When set, this bit can be written to a value of 0 to clear. 0h = Header update is not ignored 1h = Header update is ignored
0	HDREN	R/W	0h	Header enable field. When CSGATE is set to BLK, this bit has to be set by software to enable atomic header feature. When CSGATE is set to UNBLK, this field is set automatically whenever a write to header update registers [TXFHDRn.*] occurs. 0h = Atomic header update feature disable 1h = Atomic header update feature enable

24.6.24 RXDATA Register (Offset = 140h) [Reset = 00000000h]

RXDATA is shown in Table 24-27.

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RXDATA Register. Reading this register returns first value in the RX FIFO. If the FIFO is empty the last read value is returned. Writing has no effect and is ignored.

Table 24-27. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	Received Data. When read, the entry in the receive FIFO, pointed to by the current FIFO read pointer is accessed. As data values are read by the receive logic from the incoming data frame, they are placed into the entry in the receive FIFO, pointed to by the current RX FIFO write pointer. Received data less than 16 bits is automatically right-justified in the receive buffer.

24.6.25 TXDATA Register (Offset = 150h) [Reset = 00000000h]

TXDATA is shown in Table 24-28.

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TXDATA Register. Writing a value in this register puts the data into the TX FIFO. Reading this register returns the last written value.

Table 24-28. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R/W	0h	Transmit Data. When read, the last entry in the transmit FIFO, pointed to by the current FIFO write pointer is accessed. When written, the entry in the TX FIFO pointed to by the write pointer, is written to. Data values are read from the transmit FIFO by the transmit logic. It is loaded into the transmit serial shifter, then serially shifted out onto the output pin at the programmed bit rate. When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. The transmit logic ignores the unused bits.

24.6.26 STA Register (Offset = 160h) [Reset = 00000000h]

STA is shown in Table 24-29.

Return to the Summary Table.

Status Register

Table 24-29. STA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	
13-8	TXFIFOLVL	R	0h	Indicates how many locations of TXFIFO are currently filled with data
7	RESERVED	R	0h	
6	TXDONE	R/W	0h	Transmit done. Indicates whether the last bit has left the Shift register after a transmission 0h (R/W) = Last bit has not yet left the Shift register, and the transmission is ongoing. 1h (R/W) = Last bit has been shifted out, and the transmission is done
5	CSD	R/W	0h	Detection of CS deassertion in the middle of a data frame transmission results in this error being set. This feature is only available in the peripheral mode. 0h (R/W) = No CS posedge is detected before the entire data frame has been transmitted. 1h (R/W) = An error is generated when CS posedge (deassertion) is detected before the entire data frame is transmitted.
4	BUSY	R	0h	SPI Busy status 0h = SPI is in idle mode. 1h = SPI is currently transmitting and/or receiving data, or transmit FIFO is not empty.
3	RNF	R	1h	Receive FIFO not full status. 0h = Receive FIFO is full. 1h = Receive FIFO is not full.
2	RFE	R	1h	Receive FIFO empty status. 0h = Receive FIFO is not empty. 1h = Receive FIFO is empty.
1	TNF	R	1h	Transmit FIFO not full status. 0h = Transmit FIFO is full. 1h = Transmit FIFO is not full.
0	TFE	R	1h	Transmit FIFO empty status. 0h = Transmit FIFO is not empty. 1h = Transmit FIFO is empty.

Chapter 25

Inter-Integrated Circuit (I^2C)

This chapter describes the inter-integrated circuit (I^2C) interface.

25.1 Introduction

The I2C bus provides bidirectional data transfer through a 2-wire design, a serial data line (SDA) and a serial clock line (SCL), and interfaces to external I2C devices such as serial memory (RAM and ROM), networking devices, LCDs, tone generators, and so on. The I2C bus can also be used for system testing and diagnostic purposes in product development and manufacture.

The I2C module has following features:

- Devices on the I2C bus can be designated as either a controller or a target:
  - Supports both transmitting and receiving data as either a controller or a target
  - Supports one transaction after another
- Four I2C modes:
  - Controller transmit
  - Controller receive
  - Target transmit
  - Target receive
- Two transmission speeds: standard (100 kbps) and fast (400 kbps)
- Controller and target interrupt generation:
  - Controller generates interrupts when a transmit or receive operation completes (or aborts due to an error).
  - Target generates interrupts when data has been transferred or requested by a controller or when a Start or Stop condition is detected.
- Controller with arbitration and clock synchronization, multicontroller support, and 7-bit addressing mode
- Glitch filter to suppress glitches lesser than 50 ns on both SDA and SCL

25.2 Block Diagram

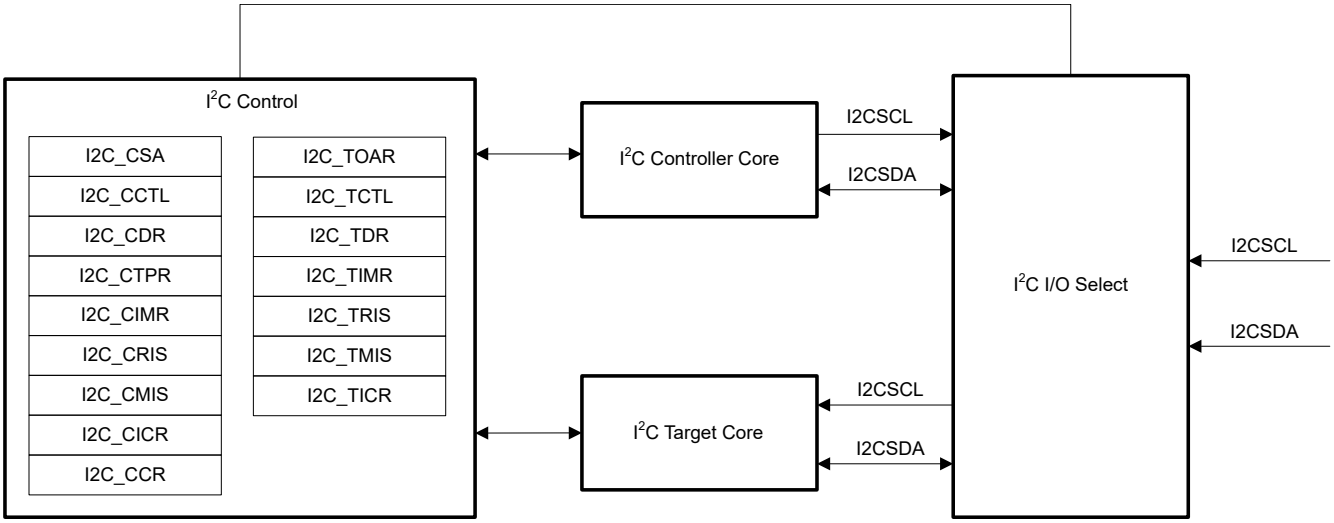


Figure 25-1. I2C Block Diagram

25.3 Functional Description

The I2C module is comprised of both controller and target functions. For proper operation, the SDA pin must be configured as an open-drain signal. See Chapter 22 for more information on configuring pin functions. Figure 25-2 shows a typical I2C bus configuration.

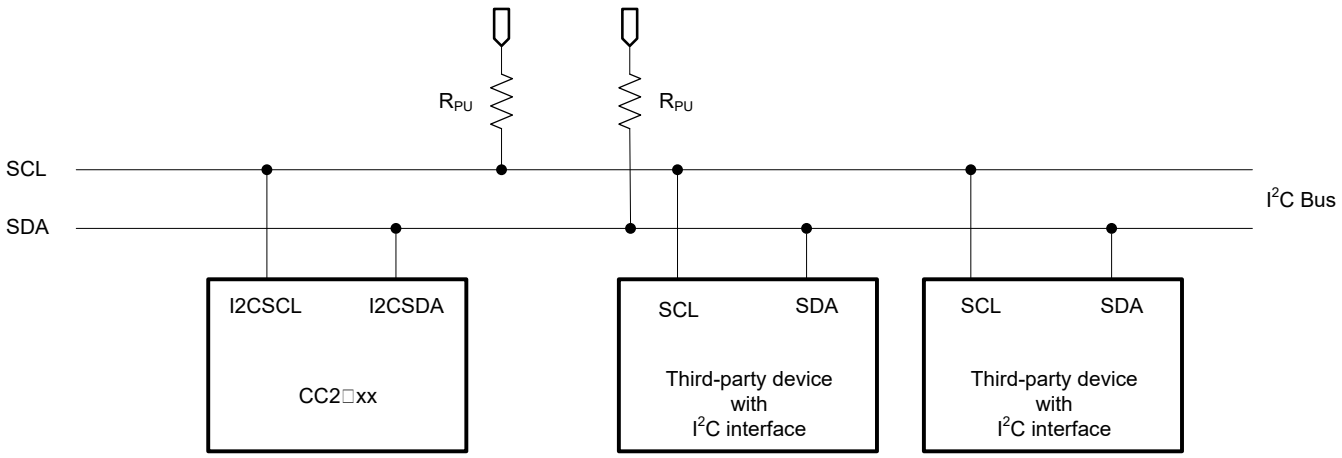


Figure 25-2. I2C Bus Configuration

25.3.1 Functional Overview

The I2C bus uses only two signals: SDA and SCL. SDA is the bidirectional serial data line and SCL line is the bidirectional serial clock line. The bus is considered idle when both lines are high.

Every transaction on the I2C bus is 9 bits long, consisting of 8 data bits and 1 acknowledge bit. A transfer is defined as the time between a valid start and stop condition, see Section 25.3.1.1. The number of bytes per transfer is unrestricted, an acknowledge bit must follow each byte, and data must be transferred by the MSB first. When a receiver cannot receive another complete byte, the receiver can hold the clock line SCL low and force the transmitter into a wait state. The data transfer continues when the receiver releases the clock SCL.

25.3.1.1 Start and Stop Conditions

The protocol of the I2C bus defines two states to begin and end a transaction: Start and Stop. A high-to-low transition on the SDA line while the SCL is high is defined as a Start condition, and a low-to-high transition on the SDA line while the SCL line is high is defined as a Stop condition. The bus is considered busy after a Start condition and free after a Stop condition (see Figure 25-3).

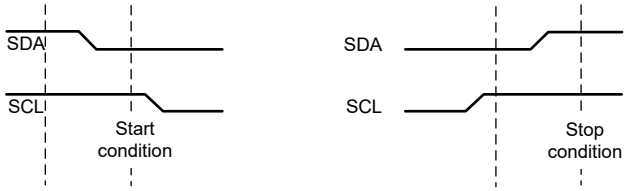


Figure 25-3. Start and Stop Conditions

The STOP bit determines if the cycle stops at the end of the data cycle or continues on to a Repeated Start condition. To generate a single transmit cycle, the I2C Controller Target Address I2C.CSA register is written with the desired address, the R/S bit is cleared, and the control register, I2C.CCTL, is written with ACK = X (0 or 1), STOP = 1, START = 1, and RUN = 1 to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt becomes active and the data is readable from the I2C Controller Data I2C.CDR register. When the I2C module operates in controller receiver mode, the ACK bit is normally set, causing the I2C bus controller to transmit an acknowledge automatically after each byte. When the I2C bus controller requires no further data transmission from the target transmitter, the ACK bit must be cleared.

When operating in target mode, 2 bits in the I2C Target Raw Interrupt Status I2C:TRIS register indicate detection of Start and Stop conditions on the bus, while 2 bits in the I2C Target Masked Interrupt Status I2C:TMIS register allow promotion of Start and Stop conditions to controller interrupts (when interrupts are enabled).

25.3.1.2 Data Format with 7-Bit Address

Data transfers follow the format shown in Figure 25-4. After the Start condition, a target address is transmitted. This address is 7 bits long followed by an eighth bit, which is a data direction bit (the RS bit in the I2C:CSA register). If the RS bit is clear, the operation is a transmit (send), and if the RS bit is set, the operation is a request for data (receive). A data transfer is always terminated by a Stop condition generated by the controller; however, a controller can initiate communications with another device on the bus, by generating a Repeated Start condition and addressing another target without first generating a Stop condition. Various combinations of receive and transmit formats are then possible within a single transfer.

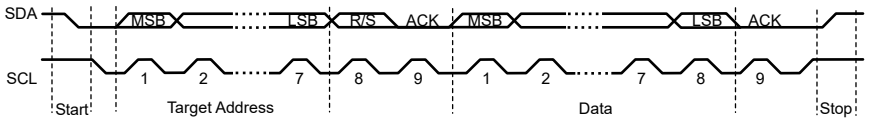


Figure 25-4. Complete Data Transfer with a 7-Bit Address

The first 7 bits of the first byte comprise the target address (see Figure 25-5). The eighth bit determines the direction of the message. A 0 in the R/S position of the first byte means that the controller transmits (sends) data to the selected target, and a 1 in this position means that the controller receives data from the target.

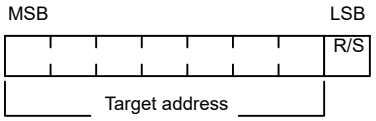


Figure 25-5. R/S Bit in First Byte

25.3.1.3 Data Validity

The SDA line must contain stable data during the high period of the clock, and the data line can change only when SCL is low (see Figure 25-6).

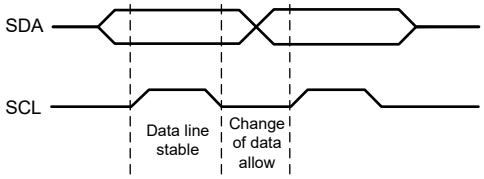


Figure 25-6. Data Validity During Bit Transfer on the I^2C Bus

25.3.1.4 Acknowledge

All bus transactions have a required acknowledge clock cycle generated by the controller. During the acknowledge cycle, the transmitter (controller or target) releases the SDA line. To acknowledge the transaction, the receiver must pull down SDA during the acknowledge clock cycle. The data transmitted by the receiver during the acknowledge cycle must comply with the data validity requirements described in Section 25.3.1.3.

When a target receiver does not acknowledge the target address, the target must leave SDA high so that the controller can generate a Stop condition and abort the current transfer. If the controller device is acting as a receiver during a transfer, the controller is responsible for acknowledging each transfer made by the target. Because the controller controls the number of bytes in the transfer, the controller signals the end of data to the target transmitter by not generating an acknowledge on the last data byte. The target transmitter must then release SDA to let the controller generate a Stop or a Repeated Start condition.

25.3.1.5 Arbitration

A controller can start a transfer only if the bus is idle. However in some cases, two or more controllers can generate a Start condition at a similar time. During the transfer, all controllers constantly monitor the SCL and SDA lines. All controllers that detect SDA as low when the controllers expect SDA to be high (as driven by them)

acknowledge that another controller has won the arbitration and immediately stop transfers, and retire until the bus is idle again.

Arbitration can occur over several bits. The first stage of arbitration is a comparison of address bits; if both controllers are trying to address the same device, arbitration continues to the comparison of data bits.

25.3.2 Available Speed Modes

The I2C bus can run in either standard mode (100 kbps) or fast mode (400 kbps). The selected mode must match the speed of the other I2C devices on the bus.

Standard and Fast Modes

Standard and fast modes are selected using a value in the I2C Controller Timer Period I2C.CTPR register that results in an SCL frequency of 100 kbps for standard mode, or 400 kbps for fast mode.

The I2C clock rate is determined by the parameters CLK_PRD, TPR, SCL_LP, and SCL_HP where:

- CLK_PRD is the CLKSVT period.
- TPR is the programmed value in the I2C.CTPR register.
- SCL_LP is the low phase of SCL (fixed at 6).
- SCL_HP is the high phase of SCL (fixed at 4). The I2C clock period is calculated as follows:

$$SCL\_PERIOD = 2 \times (1 + TPR) \times (SCL\_LP + SCL\_HP) \times CLK\_PRD \quad (12)$$

25.3.3 Interrupts

The I2C can generate interrupts when the following conditions are observed:

- Controller transaction completed
- Controller arbitration lost
- Controller transaction error
- Controller bus time-out
- Target transaction received
- Target transaction requested
- Stop condition on bus detected
- Start condition on bus detected

The I2C controller and I2C target modules have separate interrupt signals. While both modules can generate interrupts for multiple conditions, the signals are bitwise ORed together so only a single interrupt signal is sent to the MCU event fabric.

25.3.3.1 I2C Controller Interrupts

The I2C controller module generates an interrupt when a transaction completes (either transmit or receive), when arbitration is lost, or when an error occurs during a transaction. To enable the I2C controller interrupt, software must set the IM bit in the I2C Controller Interrupt Mask register, I2C.CIMR. When an interrupt condition is met, software must check the I2C.CSTAT[4] ARBLST and I2C.CSTAT[1] ERR bits to verify that an error did not occur during the last transaction, and to check that arbitration has not been lost. An error condition is asserted if the last transaction was not acknowledged by the target. If an error is not detected and the controller has not lost arbitration, the application can proceed with the transfer. The interrupt is cleared by setting the IC bit in the I2C Controller Interrupt Clear register (I2C:CICR) to 1.

If the application does not require the use of interrupts, the raw interrupt status is always visible through the I2C Controller Raw Interrupt Status register (I2C:CRIS).

25.3.3.2 I2C Target Interrupts

The target module can generate an interrupt when data is received or requested. This interrupt is enabled by setting the I2C Target Interrupt Mask register (I2C.TIMR). Software determines whether the module must write (transmit) or read (receive) data from the I2C Target Data register, I2C.TDR[7:0] DATA bit field and by checking

the I2C.TSTAT[0] RREQ and I2C.TSTAT[1] TREQ bits. If the target module is in receive mode and the first byte of a transfer is received, the I2C.TSTAT[2] FBR and I2C.TSTAT[0] RREQ bits are set. The interrupt is cleared by setting the I2C Target Interrupt Clear register I2C.TICR[0] DATAIC bit.

In addition, the target module generates an interrupt when a Start and a Stop condition is detected. These interrupts are enabled by setting the I2C.TIMR[1] STARTIM and I2C.TIMR[2] STOPIM bits; these interrupts are cleared by setting the I2C.TICR[1] STARTIC and I2C.TICR[2] STOPIC bits to 1.

If the application does not require the use of interrupts, the raw interrupt status is always visible through the I2C Target Raw Interrupt Status register (I2C.TRIS).

25.3.4 Loopback Operation

The I^2C modules can be placed into an internal-loopback mode for diagnostic or debug purposes by setting the I2C Controller Configuration register I2C.CCR[0] LPBK bit. In loopback mode, the SDA and SCL signals from the controller and target modules are tied together.

25.3.5 Command Sequence Flow Charts

This section details the steps required to perform the various I^2C transfer types in both the controller and target modes. To do this, the SDA and SCL signal configuration must be done in the IOC.IOC ***n*** registers.

25.3.5.1 I^2C Controller Command Sequences

Figure 25-7 through Figure 25-12 show the command sequences available for the I^2C controller.

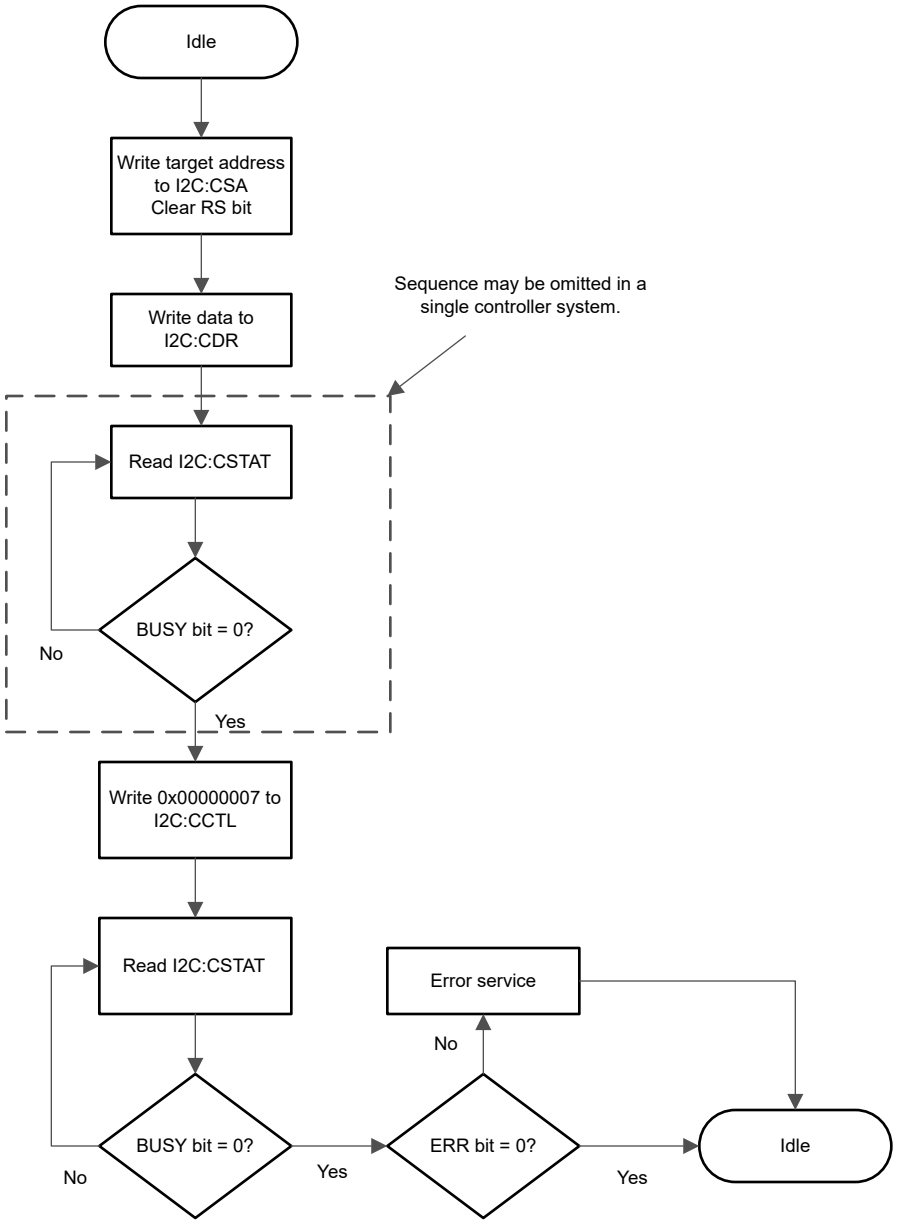


Figure 25-7. Controller Single Transmit

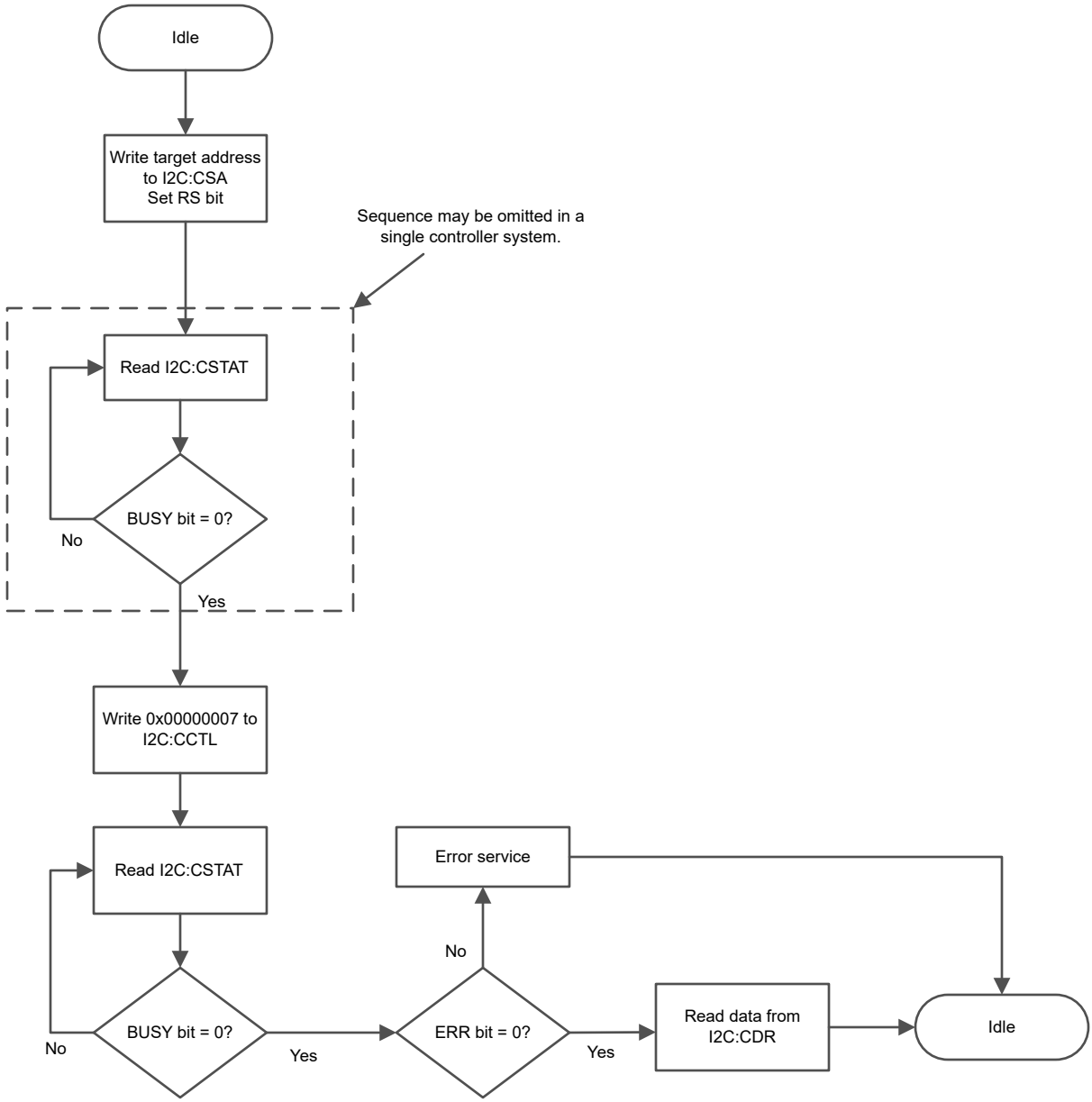


Figure 25-8. Controller Single Receive

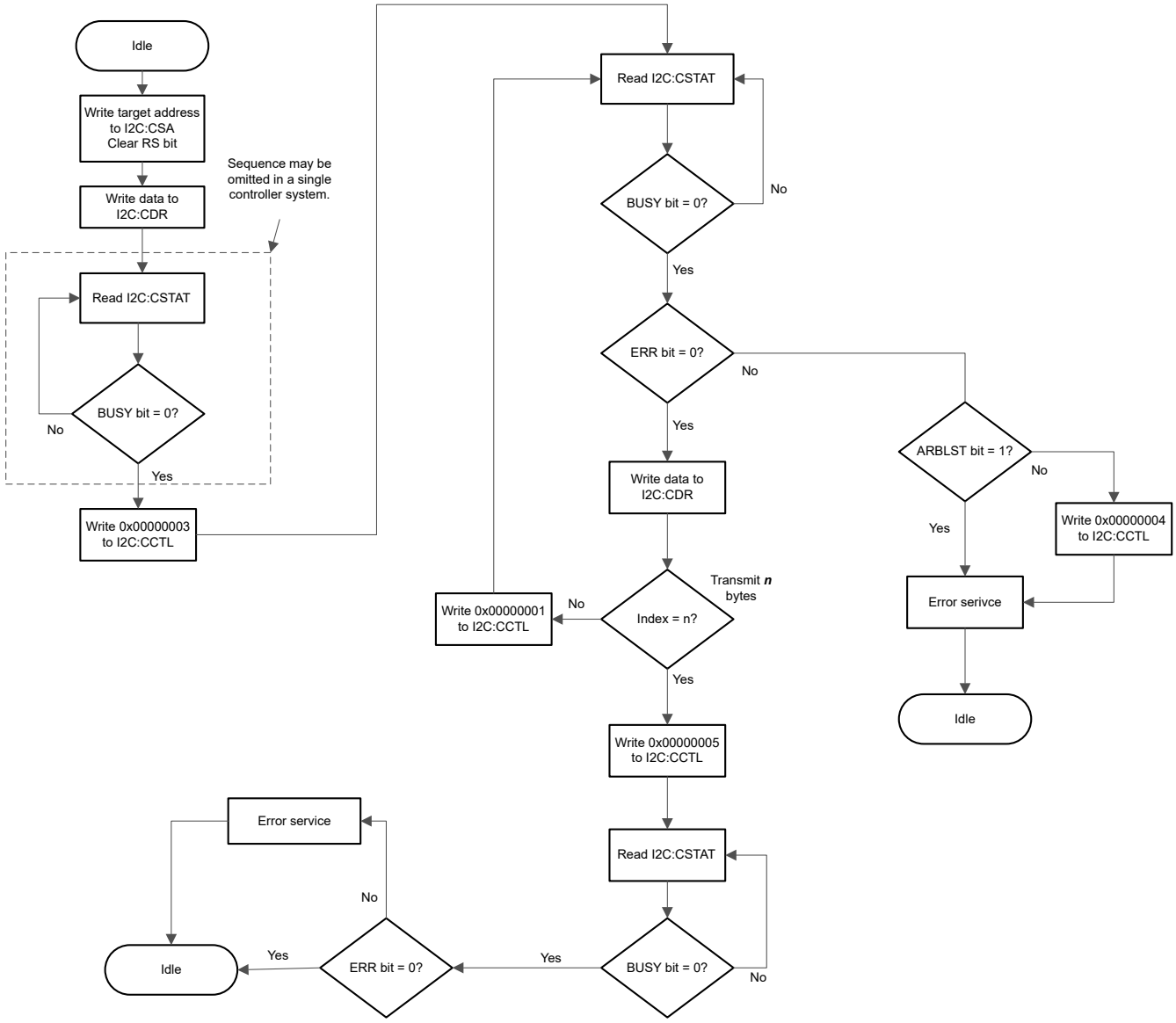


Figure 25-9. Controller Transmit with Repeated Start Condition

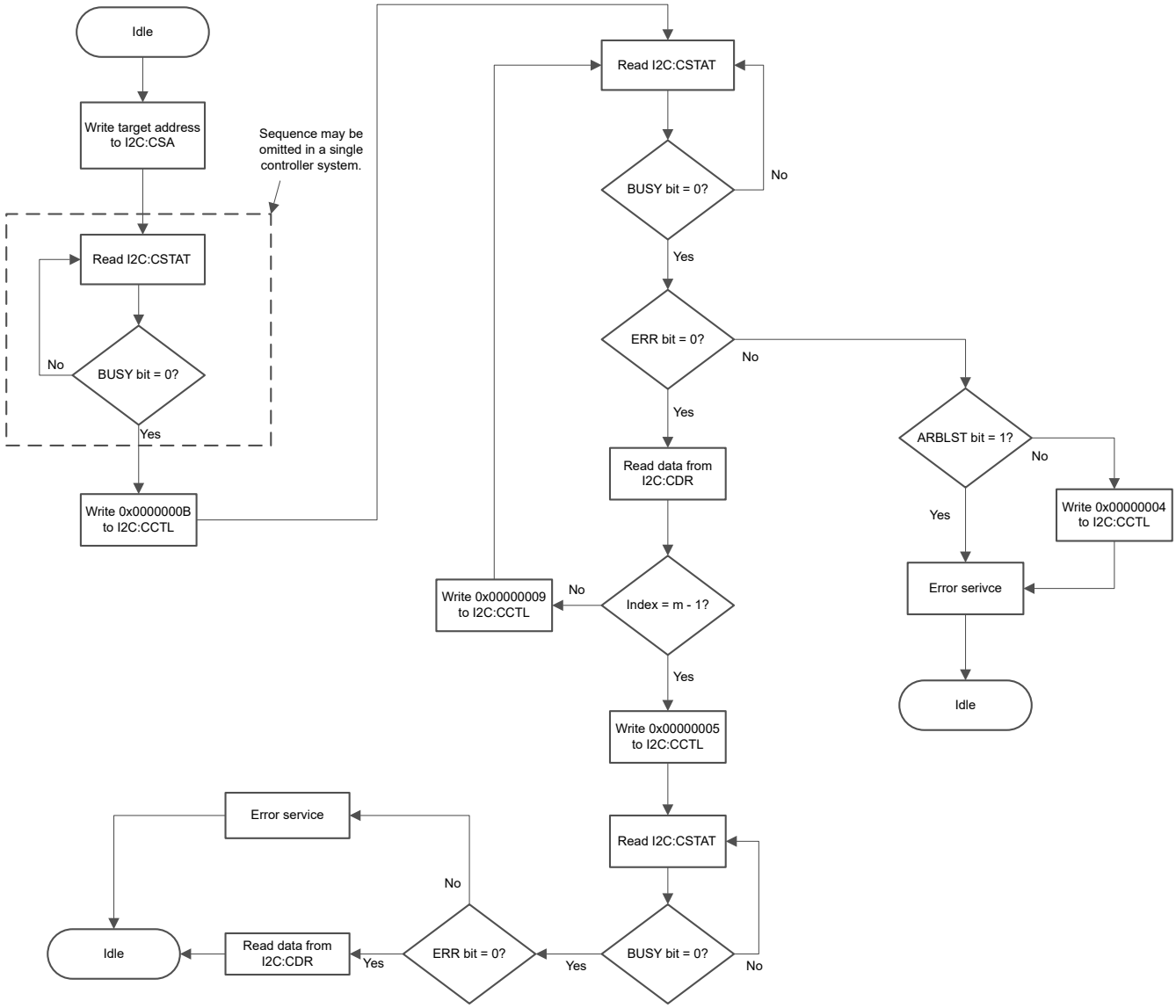


Figure 25-10. Controller Receive with Repeated Start Condition

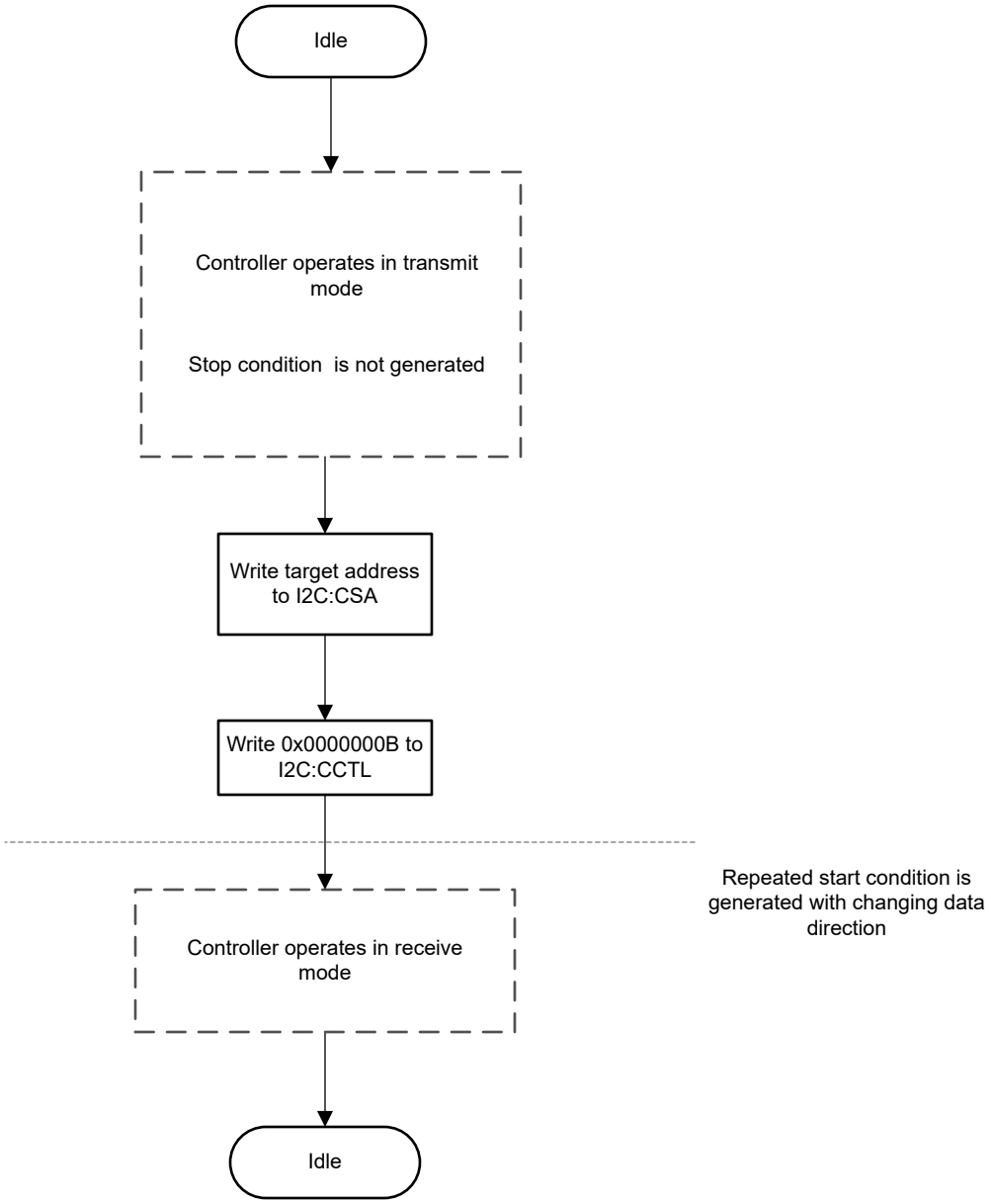


Figure 25-11. Controller Receive with Repeated Start after Transmit with Repeated Start Condition

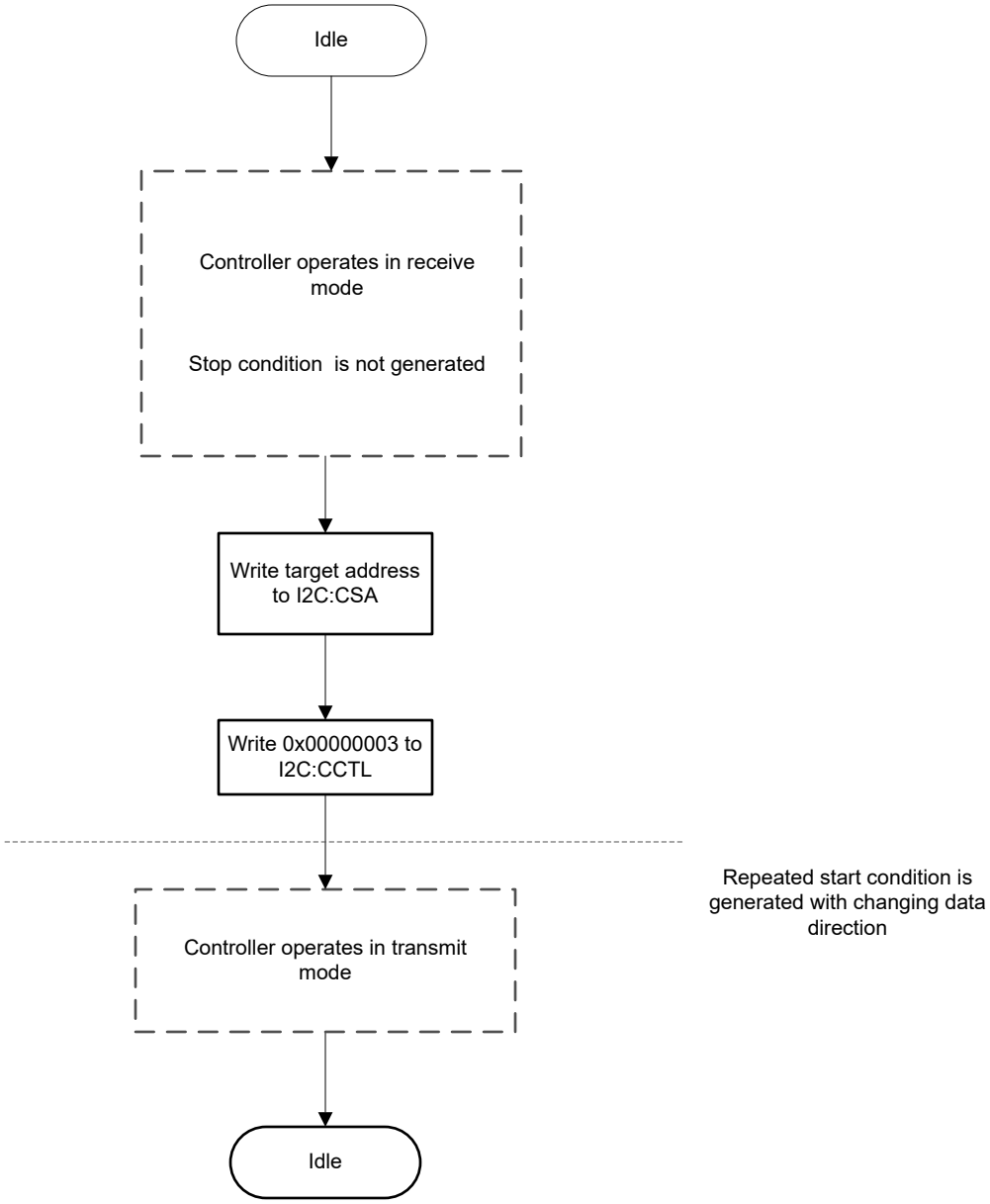


Figure 25-12. Controller Transmit with Repeated Start after Receive with Repeated Start Condition

25.3.5.2 I2C Target Command Sequences

Figure 25-13 shows the command sequence available for the I2C target.

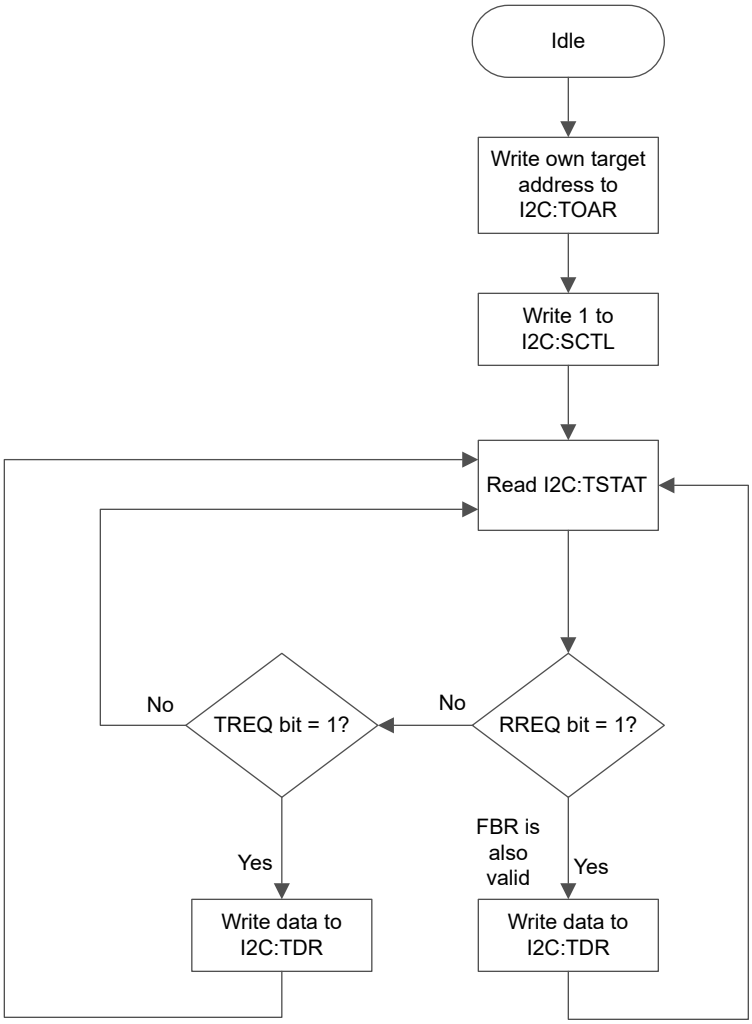


Figure 25-13. Target Command Sequence

25.4 Initialization and Configuration

The following example shows how to configure the I^2C module to transmit a single byte as a controller, assuming that the system clock is 48 MHz.

- Enable the serial power domain and enable the I^2C module in CLKCTL by setting the CLKCTL.CLKENSET0[6] I2C0 bit.
- Configure the IOC module to route the SDA and SCL signals from I/Os to the I^2C and configure the pins for open-drain. See Chapter 22 for more information.
- Initialize the I^2C controller by writing the I2C:CCR register with a value of 0x0010
- Set the desired SCL clock speed of 100 kbps by writing the I2C.CTPR register with the correct value. The value written to the I2C.CTPR register represents the number of system clock periods in one SCL clock period. The TPR value is determined by Equation 13,Equation 14, and Equation 15

$$TPR = [CLKSVT / (2 \times (SCL\_LP + SCL\_HP) \times SCL\_FREQ)] - 1 \quad (13)$$

$$TPR = [48\ MHz / (2 \times (6 + 4) \times 100000)] - 1 \quad (14)$$

$$TPR = 23 \quad (15)$$

Write the I2C:CTPR register with the value of 0x0000 0017.

- Specify the target address of the controller and that the next operation is a transmit by writing the I2C.CSA register with a value of 0x0000 0076, which sets the target address to 0x3B.
- Place data (byte) to be transmitted in the data register by writing the I2C:CDR register with the desired data.
- Initiate a single-byte transmit of the data from controller to target by writing the I2C.CCTL register with a value of 0x0000 0007 (Stop, Start, Run).
- Wait until the transmission completes by polling the I2C.CSTAT[6] BUSBSY bit until the bit is cleared.
- Check the I2C.CSTAT[1] ERR bit to confirm the transmit was acknowledged.

25.5 I2C Registers

Table 25-1 lists the memory-mapped registers for the I2C registers. All register offset addresses not listed in Table 25-1 should be considered as reserved locations and the register contents should not be modified.

Table 25-1. I2C Registers

Offset	Acronym	Register Name	Section
0h	TOAR	Target Own Address	Section 25.5.1
4h	TSTA	Target Control and Status	Section 25.5.2
4h	TCTL	Target control	Section 25.5.3
8h	TDR	Target Data	Section 25.5.4
Ch	TIMR	Target Interrupt Mask	Section 25.5.5
10h	TRIS	Target Raw Interrupt Status	Section 25.5.6
14h	TMIS	Target Masked Interrupt Status	Section 25.5.7
18h	TICR	Target Interrupt Clear	Section 25.5.8
800h	CTA	Controller Target Address	Section 25.5.9
804h	CSTA	Controller Control and Status	Section 25.5.10
804h	CCTL	Controller control	Section 25.5.11
808h	CDR	Controller Data	Section 25.5.12
80Ch	CTPR	Controller Timer Period	Section 25.5.13
810h	CIMR	Controller Interrupt Mask	Section 25.5.14
814h	CRIS	Controller Raw Interrupt Status	Section 25.5.15
818h	CMIS	Controller Masked Interrupt Status	Section 25.5.16
81Ch	CICR	Controller Interrupt Clear	Section 25.5.17
820h	CCR	Controller Configuration	Section 25.5.18

Complex bit access types are encoded to fit into small table cells. Table 25-2 shows the codes that are used for access types in this section.

Table 25-2. I2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

25.5.1 TOAR Register (Offset = 0h) [Reset = 00000000h]

TOAR is shown in Table 25-3.

Return to the Summary Table.

Target Own Address;This register consists of seven address bits that identify this I2C device on the I2C bus.

Table 25-3. TOAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6-0	OAR	R/W	0h	Target own address. This field specifies bits a6 through a0 of the target address.

25.5.2 TSTA Register (Offset = 4h) [Reset = 00000000h]

TSTA is shown in Table 25-4.

Return to the Summary Table.

Target status;This register functions as a status register of the target.

Table 25-4. TSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	FBR	R	0h	First byte received.;This bit is only applicable when the TSTA.RREQ bit is set and is automatically cleared when data has been read from the TDR register.;Note: This bit is not used for target transmit operations. 0h = The first byte following the target's own address has not been received 1h = The first byte following the target's own address has been received.
1	TREQ	R	0h	This field reflects the transmit request status 0h = No outstanding transmit request 1h = The I2C has been addressed as a target transmitter and is using clock stretching to delay the controller until data has been written to the TDR register
0	RREQ	R	0h	This field reflects the receive request status. 0h = No outstanding receive data 1h = The target has outstanding receive data from the external controller and is using clock stretching to delay the controller until data has been read from the TDR register

25.5.3 TCTL Register (Offset = 4h) [Reset = 00000000h]

TCTL is shown in Table 25-5.

Return to the Summary Table.

Target control;This registers functions as a target control register

Table 25-5. TCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
0	DA	W	0h	This field sets the device active control 0h = Disable the target operation 1h = Enable the target operation

25.5.4 TDR Register (Offset = 8h) [Reset = 00000000h]

TDR is shown in Table 25-6.

Return to the Summary Table.

Target data register ;This register contains the data to be transmitted when in the target transmit state, and the data received;when in the target receive state.

Table 25-6. TDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-0	DATA	R/W	0h	Data for transfer. This field contains the data for transfer during a target receive or a transmit operation. When written, the register data is used as transmit data. When read, this register returns the last data received. Data is stored until next update, either by a system write to the controller for transmit or by an external controller to the target for receive.

25.5.5 TIMR Register (Offset = Ch) [Reset = 00000000h]

TIMR is shown in Table 25-7.

Return to the Summary Table.

Target interrupt mask;This register controls whether a raw interrupt is promoted to a controller interrupt

Table 25-7. TIMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	STOPIM	R/W	0h	Stop condition interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
1	STARTIM	R/W	0h	Start condition interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask
0	DATAIM	R/W	0h	Data interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask

25.5.6 TRIS Register (Offset = 10h) [Reset = 00000000h]

TRIS is shown in Table 25-8.

Return to the Summary Table.

Target raw interrupt status;This register shows the unmasked interrupt status.

Table 25-8. TRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	STOPRIS	R	0h	Stop condition raw interrupt status;This bit is cleared by writing a 1 to TICR.STOPIC. 0h = Interrupt did not occur 1h = Interrupt occured
1	STARTRIS	R	0h	Start condition raw interrupt status;This bit is cleared by writing a 1 to TICR.STARTIC. 0h = Interrupt did not occur 1h = Interrupt occured
0	DATARIS	R	0h	Data raw interrupt status;This bit is cleared by writing a 1 to TICR.DATAIC. 0h = Interrupt did not occur 1h = Interrupt occured

25.5.7 TMIS Register (Offset = 14h) [Reset = 00000000h]

TMIS is shown in Table 25-9.

Return to the Summary Table.

Target Masked Interrupt Status;This register shows which interrupt is active (based on result from TRIS and TIMR registers).

Table 25-9. TMIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	STOPMIS	R	0h	Stop condition masked interrupt status;This bit is cleared by writing a 1 to TICR.STOPIC. 0h = Masked interrupt did not occur 1h = Masked interrupt occured
1	STARTMIS	R	0h	Start condition masked interrupt status;This bit is cleared by writing a 1 to TICR.STARTIC. 0h = Masked interrupt did not occur 1h = Masked interrput occured
0	DATAMIS	R	0h	Start condition masked interrupt status;This bit is cleared by writing a 1 to TICR.DATAIC. 0h = Masked interrupt did not occur 1h = Masked interrupt occured

25.5.8 TICR Register (Offset = 18h) [Reset = 00000000h]

TICR is shown in Table 25-10.

Return to the Summary Table.

Target Interrupt Clear;This register clears the raw interrupt TRIS

Table 25-10. TICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
2	STOPIC	W	0h	Stop condition interrupt clear 0h = No effect 1h = Clear interrupt;Writing 1 to this bit clears TRIS.STOPRIS and TMIS.STOPMIS
1	STARTIC	W	0h	Start condition interrupt clear 0h = No effect 1h = Clear interrupt;Writing 1 to this bit clears TRIS.STARTRIS and TMIS.STARTMIS
0	DATAIC	W	0h	Data interrupt clear 0h = No effect 1h = Clear interrupt;Writing 1 to this bit clears TRIS.DATARIS and TMIS.DATAMIS

25.5.9 CTA Register (Offset = 800h) [Reset = 00000000h]

CTA is shown in Table 25-11.

Return to the Summary Table.

Controller target address;This register contains seven address bits of the target to be accessed by the controller (a6-a0), and an CTA.RS bit determining if the next operation is a receive or transmit

Table 25-11. CTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-1	SA	R/W	0h	Controller target address;Defines which target is addressed for the transaction in controller mode
0	RS	R/W	0h	Receive or Send;This bit-field specifies the next operation with addressed target CTA.SA. 0h = Transmit/send data to target 1h = Receive data from target

25.5.10 CSTA Register (Offset = 804h) [Reset = 00000000h]

CSTA is shown in Table 25-12.

Return to the Summary Table.

Controller status;This register functions as a controller status register

Table 25-12. CSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
6	BUSBSY	R	0h	Bus busy;Note:The bit changes based on the CCTRL.START and CCTRL.STOP conditions. 0h = The bus is idle. 1h = The bus is busy.
5	IDLE	R	1h	This field specifies whether I2C is idle or not 0h = The controller is not idle. 1h = The controller is idle.
4	ARBLST	R	0h	The filed specifies the arbitration status 0h = The controller won arbitration. 1h = The controller lost arbitration.
3	DATACKN	R	0h	This field contains Data acknowledge status 0h = The transmitted data was acknowledged 1h = The transmitted data was not acknowledged
2	ADRACKN	R	0h	This field reflects the address acknowledge status 0h = The transmitted address was acknowledged 1h = The transmitted address was not acknowledged
1	ERR	R	0h	This field reflects the error status 0h = No error was detected on the last operation 1h = An error occurred with the last operation
0	BUSY	R	0h	This field reflects the I2C busy status;Note: The I2C controller requires four CLKSVT clock cycles to assert the BUSY status after I2C controller operation has been initiated through a write into CCTL register.;Hence after programming CCTL register, application is requested to wait for four CLKSVT clock cycles before issuing a controller status inquiry through a read from CSTA register. Any prior inquiry would result in wrong status being reported. 0h = The controller is idle 1h = The controller is busy

25.5.11 CCTL Register (Offset = 804h) [Reset = 00000000h]

CCTL is shown in Table 25-13.

Return to the Summary Table.

Controller control;This register functions as a controller control register

Table 25-13. CCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
3	ACK	W	0h	This field is to enable the data acknowledge.;Note:This bit-field must be cleared when the I2C bus controller requires no further data to be transmitted from the target transmitter. 0h = The received data byte is not acknowledged automatically by the controller 1h = The received data byte is acknowledged automatically by the controller
2	STOP	W	0h	This field is to set stop condition .;Note: This bit-field determines if the cycle stops at the end of the data cycle or continues on to a repeated start condition. 0h = The controller does not generate the stop condition 1h = The controller generates the stop condition
1	START	W	0h	This field is to set start or repeated start condition. 0h = The controller does not generate the start condition 1h = The controller generates the start condition.
0	RUN	W	0h	This field is to set the controller enable. 0h = The controller is disabled. 1h = The controller is enabled to transmit or receive data

25.5.12 CDR Register (Offset = 808h) [Reset = 00000000h]

CDR is shown in Table 25-14.

Return to the Summary Table.

Controller data;This register contains the data to be transmitted when in the controller transmit state and the data received when in the controller receive state.

Table 25-14. CDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7-0	DATA	R/W	0h	When Read: Last RX Data is returned;When Written: Data is transferred during TX transaction

25.5.13 CTPR Register (Offset = 80Ch) [Reset = 00000000h]

CTPR is shown in Table 25-15.

Return to the Summary Table.

Controller timer period;This register specifies the period of the SCL clock.

Table 25-15. CTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
7	TPR_7	R/W	0h	Must be set to 0 to set CTPR.TPR. If set to 1, a write to CTPR.TPR will be ignored.
6-0	TPR	R/W	1h	SCL clock period;This field specifies the period of the SCL clock.;SCL_PRD = 2*(1+TPR)*(SCL_LP + SCL_HP)*CLK_PRD, where:;SCL_PRD is the SCL line period (I2C clock).;TPR is the timer period register value (range of 1 to 127);SCL_LP is the SCL low period (fixed at 6).;SCL_HP is the SCL high period (fixed at 4).;CLK_PRD is the CLKSVT period in ns.

25.5.14 CIMR Register (Offset = 810h) [Reset = 00000000h]

CIMR is shown in Table 25-16.

Return to the Summary Table.

Controller interrupt mask;This register controls whether a raw interrupt is promoted to a controller interrupt.

Table 25-16. CIMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
0	IM	R/W	0h	Interrupt mask 0h = Disable interrupt mask 1h = Enable interrupt mask

25.5.15 CRIS Register (Offset = 814h) [Reset = 00000000h]

CRIS is shown in Table 25-17.

Return to the Summary Table.

Controller raw interrupt status;This register shows the unmasked interrupt status.

Table 25-17. CRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
0	RIS	R	0h	Raw interrupt status;This bit is cleared by writing 1 to CICR.IC bit. 0h = Interrupt did not occur 1h = Interrupt occured

25.5.16 CMIS Register (Offset = 818h) [Reset = 00000000h]

CMIS is shown in Table 25-18.

Return to the Summary Table.

Controller masked interrupt status;This register shows which interrupt is active (based on result from CRIS and CIMR registers).

Table 25-18. CMIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
0	MIS	R	0h	Masked interrupt status;This bit is cleared by writing 1 to CICR.IC bit. 0h = Masked interrupt did not occur 1h = Masked interrupt occured

25.5.17 CICR Register (Offset = 81Ch) [Reset = 00000000h]

CICR is shown in Table 25-19.

Return to the Summary Table.

Controller interrupt clear;This register clears the raw and masked interrupt.

Table 25-19. CICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
0	IC	W	0h	Interrupt clear 0h = No effect 1h = Clear Interrupt;Writing 1 to this bit clears CRIS.RIS and CMIS.MIS.

25.5.18 CCR Register (Offset = 820h) [Reset = 00000000h]

CCR is shown in Table 25-20.

Return to the Summary Table.

Controller Configuration;This register configures the mode (Controller or Target) and sets the interface for test mode loopback.

Table 25-20. CCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
5	TFE	R/W	0h	I2C target function enable; 0h = Target mode disabled 1h = Target mode enabled
4	CFE	R/W	0h	I2C controller function enable 0h = Controller mode disabled 1h = Controller mode enabled
3-1	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
0	LPBK	R/W	0h	I2C loopback 0h = Test mode (Loopback operation) disabled 1h = Test mode (Loopback operation) enabled

Chapter 26

Inter-IC Sound (I^2S)

This section describes the Inter-IC Sound (I^2S) module.

26.1 Introduction

The I^2S module provides a standardized serial interface to transfer audio samples between the CC27xx device platform and the external audio devices.

The I^2S module has the following features:

- One or two data pins, which can be configured independently as input or output
- I^2S, left-justified (LJF), and right-justified (RJF) serial interface formats that support up to two audio channels per data pin
- Single phased DSP serial interface format that supports up to eight audio channels per data pin
- Up to 32-bit sample word length, with truncation or zero-padding if not matching
- Serial interface to transfer audio samples between BLE devices and external audio devices (Codec or DAC or ADC)
- Support interfacing with PDM digital microphones and generation of PCM samples through software based decimation filtering
- Receive audio source clock from CKMDIG and generate MCLK, BCLK and WCLK using local audio clock generator
- Separate clock enable control bits, one for MCLK and another for BCLK and WCLK
- Two audio channels per data pin (left and right channels) in dual phased communication modes
- Bus master with data buffering for each of the channels and built-in DMA capabilities
- Slave port accesses and master port transactions at 96MHz
- Performs direct 32-bit read/write transactions on the master port when sample size is more than 16-bits
  - Adds 8 zeros at LSB for write to SRAM and remove 8 LSB bits for read from SRAM when 32-bit DMA transfer type is selected
- Error detection for DMA and audio clock signal integrity
- Samplestamp generator to maintain correct and constant audio latency between I^2S nodes on the wireless network
  - Samplestamp capture interrupt condition for event based capture operation
- System bus is clocked in SoC idle mode when I^2S module is enabled (through CLKCTL module)
- I^2S have idle/hold request interface with CLKCTL module.

26.2 Block Diagram

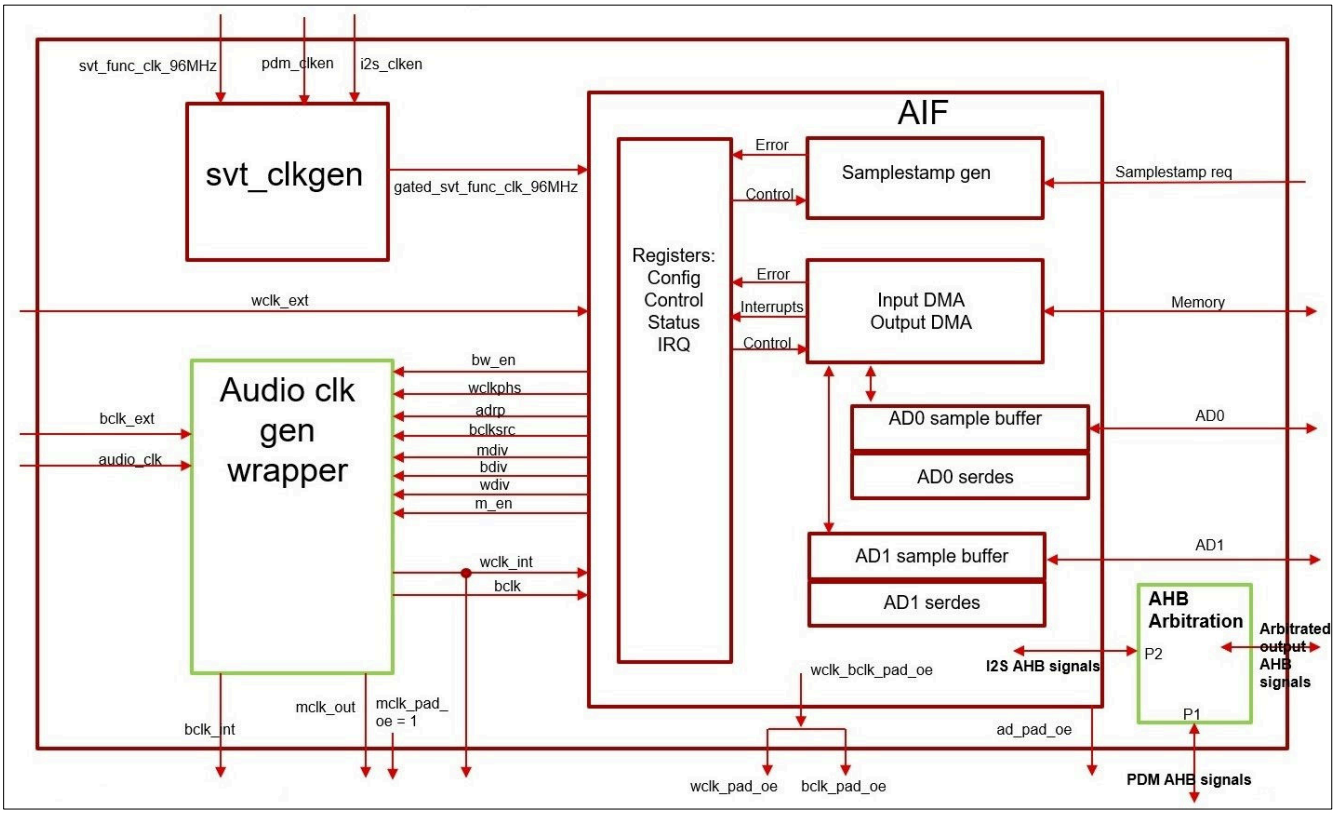


Figure 26-1. I²S Block Diagram

26.3 Clock Architecture

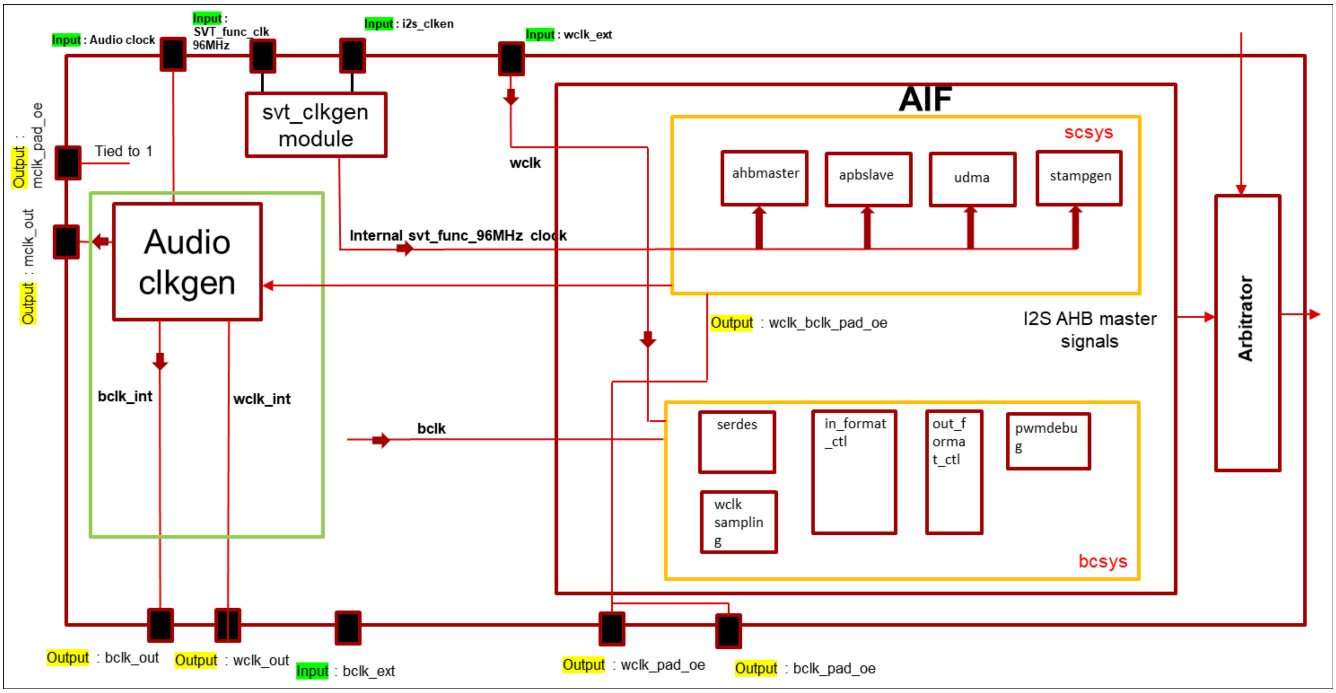


Figure 26-2. I²S Clock Architecture

26.4 Signal Descriptions

- The serial audio interface consists of two or three clock signals and one or two data signals(AD0,AD1), depending on how the I^2S module is used. The clock signals(MCLK,BCLK,WCLK) can be generated either internally (by the PRCM module) or externally (by the audio device or another clock source).
- The ADx pins cannot be dynamically placed in a tri-state condition. Therefore, TDM mode is supported for ADx input pins where only external audio devices drive these signals, but TDM mode is not supported for ADx output pins.

26.5 Functional Description

26.5.1 Pin Configuration

The AIFDIRCFG register configures whether each ADx signal is input, output, or unused. Each used I^2S signal must be mapped to a physical I/O pin.

26.5.2 Serial Format Configuration

The WCLK and ADx signals are updated on one edge of the BCLK and sampled on the opposite edge. The sample words transferred on the ADx pins are aligned with the WCLK signal, according to the configured serial interface format. The first WCLK edge of a sample word is either rising or falling, depending on the configured serial interface format. The period from the first WCLK edge of an audio sample (one or more channels) to the first WCLK edge of the next audio sample is called a frame. A frame consists of either one or two phases. A phase is divided into the following intervals:

- Data delay (optional): The BCLK periods between the first WCLK edge and MSB of the (first) audio channel data transferred during the phase
- Word: The BCLK periods during which sample words are transferred on the ADx pin or pins
  - For single-phase, from 1 to 8 sample words are transferred back-to-back.
  - For dual-phase, one sample word is transferred. The least significant bit (LSB) of the sample word can extend into the data delay interval of the next phase.
- Idle (optional): The BCLK periods between the word interval and the next phase

  A sample word on the serial interface can contain from 8 to 32 bits.

26.5.3 I^2S Format Schematic

I^2S is a dual-phase format with a 50% WCLK duty cycle and the start of an MSB of each sample word aligned with each edge of WCLK + one BCLK period. For any given frame, the left channel is transferred first when WCLK is low, and the right channel is transferred next when WCLK is high. Figure shows the I^2S serial format. Data is sampled on the rising edge of BCLK and updated on the falling edge of BCLK. The I^2S format is unique in the sense that the BLE High device platform can automatically detect the number of BCLK periods per WCLK period. Therefore, I^2S supports any BCLK rate from an external audio clock source and also variable sample word length:

- If the configured sample word length is higher than the number of bits per WCLK period, the sample words are truncated.
- If the configured sample word length is lower than the number of bits per WCLK period, the sample words are zero-padded.

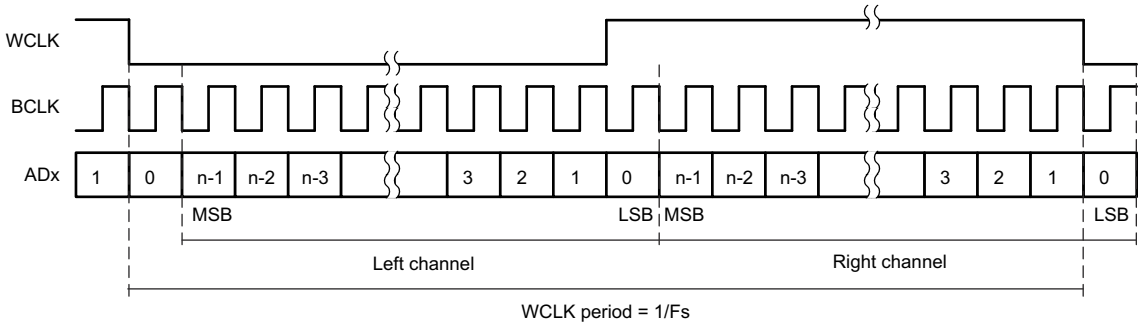


Figure 26-3. I^2S Serial Format

26.5.3.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 1
- AIFFMTCFG.DUAL_PHASE = 1
- AIFFMTCFG.SMPL_EDGE = 1
- AIFFMTCFG.WORD_LEN = Maximum number of bits per sample word
- AIFFMTCFG.DATA_DELAY = 1

26.5.4 Left-Justified (LJF)

LJF is a dual-phase format with a 50% WCLK duty cycle and the start of an MSB of each sample word aligned with each edge of WCLK. For any given frame, the left channel is transferred first when WCLK is high, and the right channel is transferred next when WCLK is low. Data is sampled on the rising edge of BCLK and updated on the falling edge of BCLK. The below figure shows the LJF serial format.

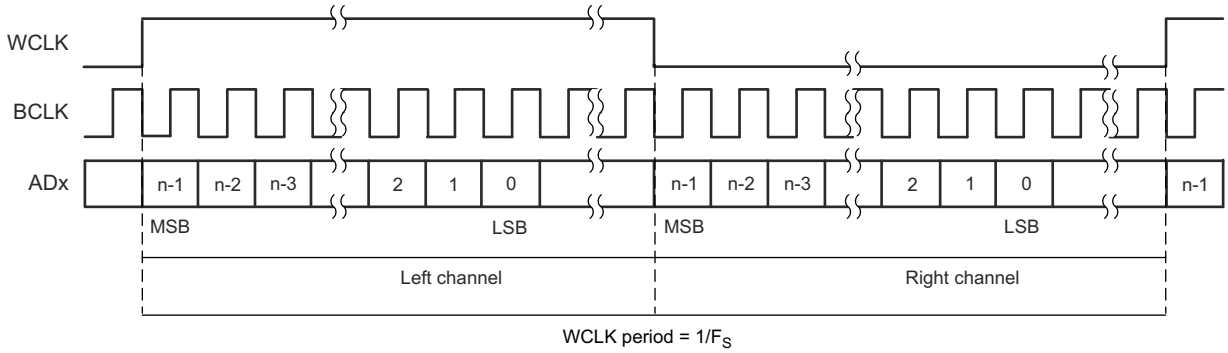


Figure 26-4.

26.5.4.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 0
- AIFFMTCFG.DUAL_PHASE = 1
- AIFFMTCFG.SMPL_EDGE = 1
- AIFFMTCFG.WORD_LEN = Maximum number of bits per sample word
- AIFFMTCFG.DATA_DELAY = 0

WORD_LEN must be equal to or less than the number of BCLK periods per phase.

26.5.5 Right-Justified (RJF)

RJF is a dual-phase format with a 50% WCLK duty cycle and the end of an LSB of each sample word aligned with each edge of WCLK. For any given frame, the left channel is transferred first when WCLK is high, and the

right channel is transferred next when WCLK is low. Data is sampled on the rising edge of BCLK and updated on the falling edge of BCLK. The below figure showsthe RJF serial format.

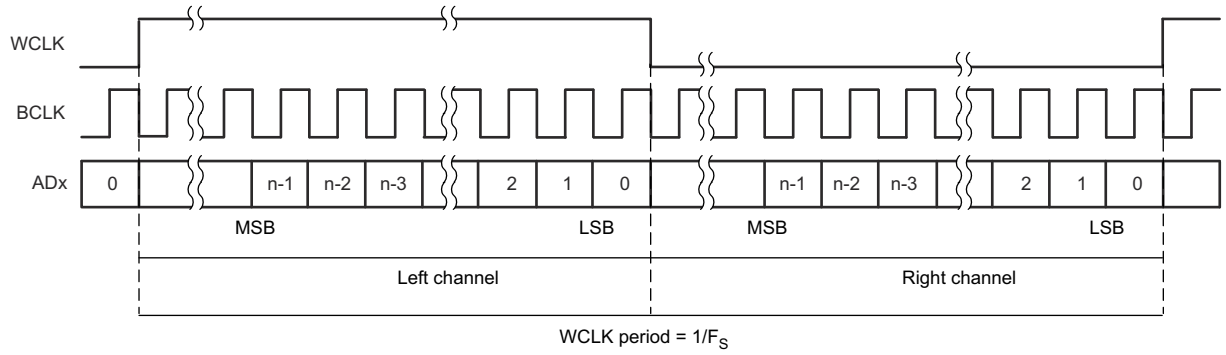


Figure 26-5.

26.5.5.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 0
- AIFFMTCFG.DUAL_PHASE = 1
- AIFFMTCFG.SMPL_EDGE = 1
- AIFFMTCFG.WORD_LEN = Exact number of bits per sample word
- AIFFMTCFG.DATA_DELAY = Number of BCLK periods per phase minus the value of I2S:AIFFMTCFG.WORD_LEN

DATA_DELAY + WORD_LEN must be equal to or less than the number of BCLK periods per phase.

26.5.6 DSP

DSP is a single-phase format where WCLK is high for one BCLK period, and the MSB of the first sample word is typically aligned with this WCLK pulse, or it follows in the next BCLK period. Sample words for subsequent audio channels are then transferred back-to-back, followed by an idle period until the next phase or frame begins. Data is sampled on the falling edge of BCLK and updated on the rising edge of BCLK. The below figure shows the DSP serial format with zero data delay.

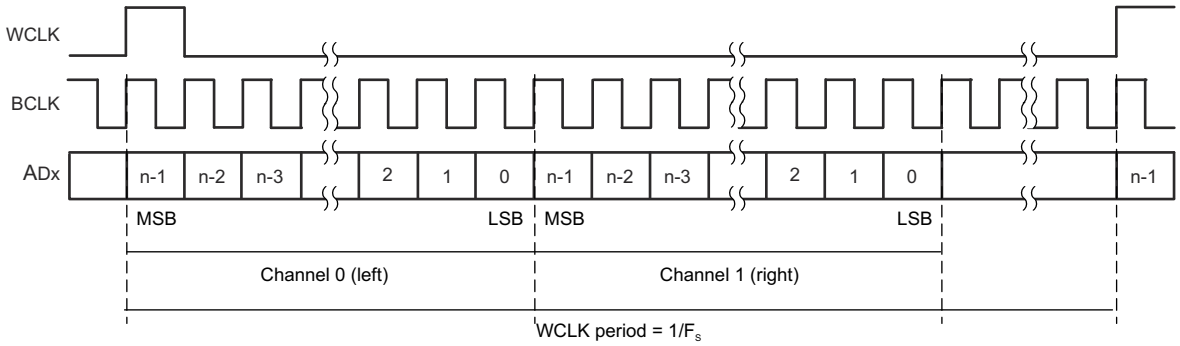


Figure 26-6.

26.5.6.1 Register Configuration

The register configuration follows:

- AIFWCLKSRC.WCLK_INV = 0
- AIFFMTCFG.DUAL_PHASE = 0
- AIFFMTCFG.SMPL_EDGE = 0
- AIFFMTCFG.WORD_LEN = Exact number of bits per sample word

- AIFFMTCFG.DATA_DELAY = 0 or 1

DATA_DELAY + (WORD_LEN × channel count) must be equal to or less than the number of BCLK periods per phase.

The channel count is determined by the MSB set in the I2S:AIFWMASK0 and I2S:AIFWMASK1 registers.

26.5.7 Clock Configuration

The audio clocks signals, MCLK, BCLK, and WCLK, can be generated either internally by the PRCM module or by an external clock source. The internally generated audio clock signals might not be suitable for all applications for the reasons that follow:• Jitter performance• Clock configuration only provides support for frequencies that can be divided down from 96 MHz.• Frequency that cannot be tuned to maintain constant audio latency

Internal audio clock source: AIFWCLKSRC = 2

External audio clock source: AIFWCLKSRC = 1

26.6 Memory Interface

The integrated direct memory access controller (DMA) independently handles input samples (from one or two ADx pins to RAM) and output samples (from RAM or flash to one or two ADx pins). There is one shift-register and one sample word buffer for each ADx pin. The DMA stores input sample words to memory while the next sample words are received, and it loads output sample words from memory while the last loaded sample words are transmitted. The DMA operates on blocks of memory. While the DMA works on one block of memory, software mustwrite the start address of the next memory block to AIFINPTRNEXT for input samples and to AIFOUTPTRNEXT for output samples.

26.6.1 Sample word length

The sample word length in memory (16 or 32 bits) is configured independently of sample word length on the serial interface (8 to 32 bits). Sample words are truncated when the destination is shorter than the source and zero-padded when the destination is longer than the source. The AIFFMTCFG.MEM_LEN_32 field configures whether sample words in memory are 16 bit or 32 bit:

- 0: Each 16-bit sample word is moved to or from memory using one 16-bit transfer. The DMA pointers written to the AIFINPTRNEXT and AIFOUTPTRNEXT registers must be halfword aligned.
- 1: Each 32-bit sample word is moved to or from memory using one 32-bit transfer. The DMA pointers written to the AIFINPTRNEXT and AIFOUTPTRNEXT registers do not need to be aligned to any memory size.

26.6.2 Padding Mechanism

Padding mechanism:

- **Data Reception**:
  - word len = 24 and mem len = 16; transfer only 16 MSB bits to the memory from DMA and drop 8 LSB bits.
  - 16<=word len<=24 and mem len = 16; transfer only 16 MSB bits to the memory from DMA.
  - 8<=word len < 16 and mem len = 16; Pad the remaining MSB bits with zeros and make a 16 bit data and transfer it to the memory
  - word len = 24 and mem len = 32; Pad additional 8 bits at the LSB with zeros to make a 32-bit data and transfer it to the memory.
  - 8<=word len<=24 and mem len = 32; Pad all the remaining bits at the LSB with zero to make a 32-bit data and transfer it to the memory.
- **Data transmission** :
  - mem len = 16; Add 8 zeros at the LSB to generate a 24-bit packet for serializer buffer. Depending upon the word len configuration same number of bits will be transferred over AD pins.
  - mem len = 32; Drop the LSB 8-bits and generate a 24-bit packet for serializer buffer. Depending upon the word len configuration same number of bits will be transferred over AD pins.

26.6.3 Channel Mapping

For each ADx pin, the corresponding AIFWMASKx register determines which sample words are present in memory:

- For each frame when AIFFMTCFG.DUAL_PHASE = 0 (DSP format):
  - Input: The AIFWMASKx.MASK register determines whether or not channels are stored to memory.
  - Output: The AIFWMASKx.MASK register determines whether or not channels are fetched from memory. The ADx output is low for excluded channels.
- For each frame when AIFFMTCFG.DUAL_PHASE = 1 (I2S, LJF, and RJF formats):
  - Mono: AIFWMASKx.MASK = 0x01
- Input: Left (0) channel is stored to memory.
- Output: Left (0) channel is fetched from memory and is repeated for the right channel.
  - Stereo: AIFWMASKx.MASK = 0x03
- Input: Left (0) and right (1) channels are stored to memory.
- Output: Left (0) and right (1) channels are fetched from memory.

26.6.4 Sample Storage in Memory

Sample words are stored to memory in little-endian byte order, meaning that the least significant byte (LSByte) is stored at the lower byte address, and the most significant byte (MSByte) is stored at the higher byte address. If both ADx pins are configured as input or both ADx pins are configured as output, the sample words for each audio channel are stored AD0 first and AD1 last.

PICTURES TO BE UPDATED

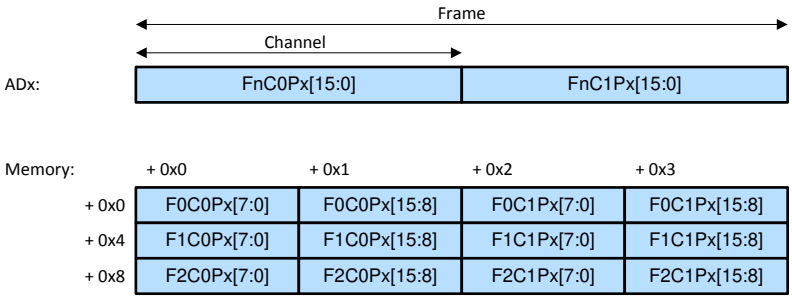


Figure 26-7. 16-Bit Mono I2S, LJF, and RJF Formats on One ADx Pin, Showing Six Frames in Memory

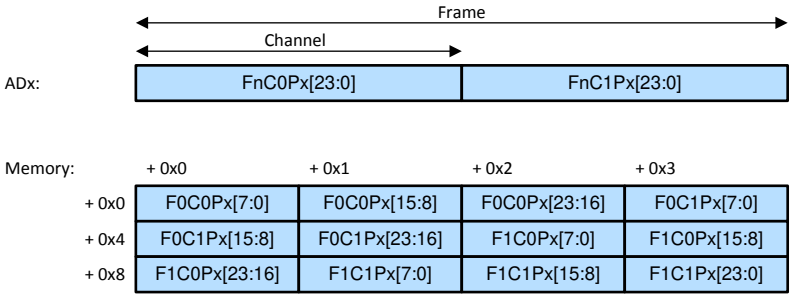


Figure 26-8. 16-Bit Stereo I2S, LJF, and RJF Formats on One ADx Pin, Showing Three Frames in Memory

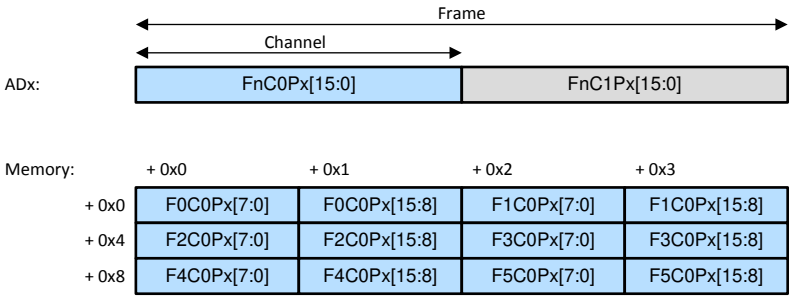


Figure 26-9. 24-Bit Stereo I^2S, LJF, and RJF Formats on One ADx Pin, Showing Two Frames in Memory

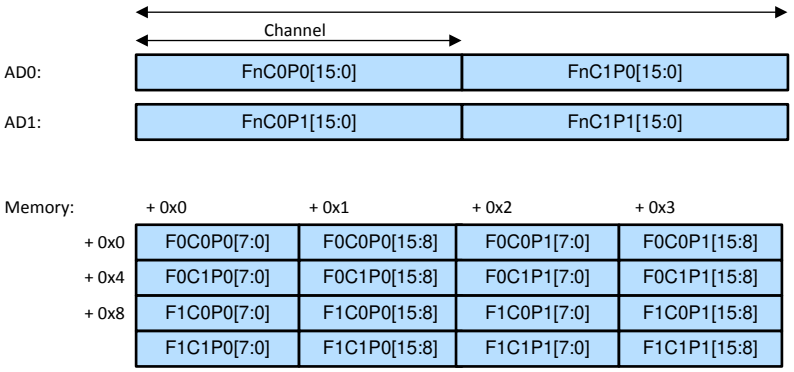


Figure 26-10. 16-Bit I^2S Format on AD0 and AD1 Pins, Showing Two Frames in Memory

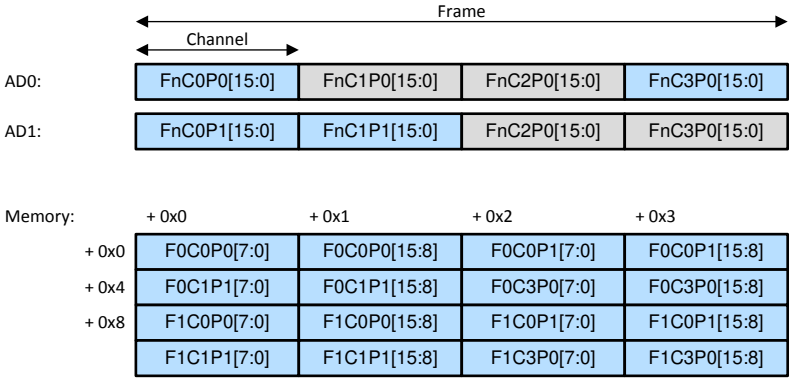


Figure 26-11. 16-Bit DSP Format on AD0 and AD1 Pins, Showing Two Frames in Memory

26.6.5 DMA Operation

The DMA operates on blocks of memory. Each input and output DMA memory block contains the input and output sample words, respectively, for AIFDMACFG.END_FRAME_IDX + 1 frames.

Writing a nonzero value to AIFDMACFG.END_FRAME_IDX initializes the DMA and prepares it to be started. Writing zero to AIFDMACFG.END_FRAME_IDX disables the DMA and resets the serial audio interface.

If input ADx pins are used, software must write memory block start addresses for input DMA to AIFINPTRNEXT. The current input DMA memory location can be observed in AIFINPTR.

If output ADx pins are used, software must write memory block start addresses for output DMA to AIFOUTPTRNEXT. The current output DMA memory location can be observed in AIFOUTPTR.

This writing operation or DMA operation allows the software to implement sample block ring buffers in memory with an arbitrary number of blocks for input and output samples.

26.6.5.1 Start-Up

All other audio interface-related register configuration (pins, serial format, clocks, sample word sizes, and channel mapping) must be completed before writing a nonzero value to theAIFDMACFG.END_FRAME_IDX register. To prepare input and output DMA for start-up, the software must preload the first and second DMA pointers to be used and must arm the DMA:

- Write the first memory block start addresses to be used to AIFINPTRNEXT and (or) AIFOUTPTRNEXT
- Set AIFDMACFG.END_FRAME_IDX = the number of frames per block minus one.
  - This loads AIFINPTRNEXT into AIFINPTR, and AIFOUTPTRNEXT into AIFOUTPTR, and the output DMA will immediately prefetch sample words for the first two audio channels.
- Write the second memory block start addresses to be used to AIFINPTRNEXT and (or) AIFOUTPTRNEXT.

26.6.5.2 Operation

To maintain DMA operation, software must provide new memory block start addresses each time a memory block is finished. When a block is finished, the following occurs:

- For the input memory interface block:
  - AIFINPTR = AIFINPTRNEXT
  - AIFINPTRNEXT = 0x0000 0000
  - IRQFLAGS.AIF_DMA_IN is set to generate an I2S_IRQ interrupt.
- For the output memory interface block:
  - AIFOUTPTR = AIFOUTPTRNEXT
  - AIFOUTPTRNEXT = 0x0000 0000
  - IRQFLAGS.AIF_DMA_OUT is set to generate an I2S_IRQ interrupt.

To handle this operation, software must either poll if the AIFINPTRNEXT and (or) AIFOUTPTRNEXT registers are zero, or use the IRQFLAGS.AIF_DMA_IN and (or) IRQFLAGS.AIF_DMA_OUT interrupt requests.

Software must write the new memory block start addresses to AIFINPTRNEXT and (or) AIFOUTPTRNEXT before the running block finishes. If the running block finishes while AIFINPTRNEXT and (or) AIFOUTPTRNEXT are zero, the affected DMA channels stop and IRQFLAGS.PTR_ERR is set.

26.6.5.3 Shutdown

Before DMA shutdown, all output external audio devices (for example, a DAC) should be muted, or silence should the transmitted on output ADx pins. The DMA must not be stopped while there could be an ongoing DMA memory transfer.. When using the internal audio clock source or an external audio clock source that cannot stop unexpectedly, software should use the following procedure to stop the DMA:

- Stop writing to the AIFINPTRNEXT and/or AIFOUTPTRNEXT registers.
- Optional: Wait for IRQFLAGS.PTR_ERR to occur.
- Wait for AIFINPTRNEXT and AIFOUTPTRNEXT to become zero.
- Write AIFDMACFG.END_FRAME_IDX = 0.

When using an external audio clock source that can stop unexpectedly, software should use the following procedure to stop the DMA:

- Stop writing to the AIFINPTRNEXT and (or) AIFOUTPTRNEXT registers.
- Stop the external audio clock source.
- Wait for IRQFLAGS.WCLK_TIMEOUT to occur, or for AIFINPTRNEXT and AIFOUTPTRNEXT to become zero, whichever happens first.
- Write AIFDMACFG.END_FRAME_IDX = 0.

26.7 Samplestamp Generator

The samplestamp generator is used to start input and output DMA operation. The samplestamp generator is also used to synchronize I^2S modules over a wireless network, so correct and fixed audio latency can be achieved.

Synchronization over a wireless network is an optional feature that can be bypassed. The samplestamp generator is enabled and is running while STMPCTL.STMP_EN = 1. Counter and capture registers are reset when software writes STMPCTL.STMP_EN = 0.

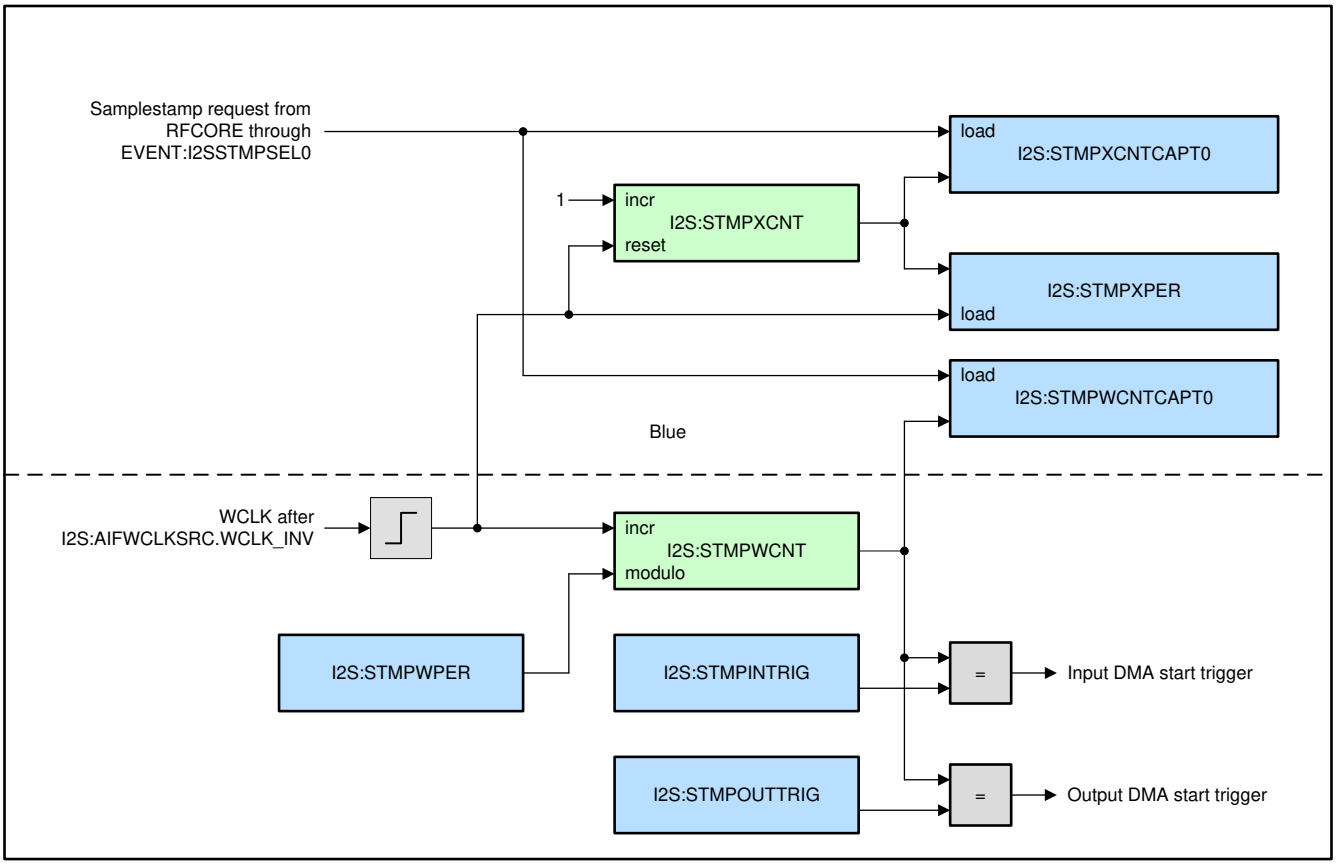


Figure 26-12. Samplestamp Generator

26.7.1 Samplestamp Counters

The samplestamp generator counts frames (WCLK periods) and 96 MHz clock cycles (crystal oscillator periods) within each frame:

- STMPWCNT increments at the first WCLK edge of each frame, module the period value STMPWPER.
- STMPXCNT resets to 0 at the first WCLK edge of each frame, and then increments by 1 for each 96 MHz clock cycle. Reading STMPWCNT latches the read value of STMPXCNT.

Software can modify the value of STMPWCNT by writing an absolute value to STMPWSET or a relative value to STMPWADD.

26.7.2 Start-Up Triggers

The STMPINTRIG and STMPOUTTRIG registers contain STMPWCNT compare values that are used to start the input and output DMA, respectively:

- When STMPWCNT equals STMPINTRIG, the input DMA begins storing sample words to memory in the next frame: (STMPINTRIG + 1) % STMPWPER
- When STMPWCNT equals STMPOUTTRIG, the output DMA begins outputting sample words from memory in the next frame: (STMPOUTTRIG + 1) % STMPWPER

To avoid false start-up triggers, STMPINTRIG and STMPOUTTRIG must initially be equal to or higher than STMPWPER.

The STMPCTL.IN_RDY and STMPCTL.OUT_RDY status bits are set when the input and output DMA are ready to be started and cleared when DMA start triggers have occurred.

26.7.3 Samplestamp Capture

A capture request signal can be routed from RFCORE to trigger samplestamp capture. Whenever the event - samplestamp request(pulse detection inside the IP) signal is high:

- The current value of STMPXCNT is copied into STMPXCNTCAPT0.
- The current value of STMPWCNT is copied into STMPWCNTCAPT0.

Also, on the first WCLK edge of each frame, the current value of STMPXCNT is captured in STMPXPER, and STMPXCNT then restarts counting from 0.

Using these values, a fixed-point samplestamp value can be calculated:

STMPWCNTCAPT0 + (STMPXCNTCAPT0 / STMPXPER)

Notice that the value of STMPXPER will not normally be captured at the same time as the other values. Therefore, STMPXPER can be less than STMPXCNTCAPT0.

26.7.4 Achieving constant audio latency

The following actions can be taken to achieve the same constant audio latency in either direction over a wireless network (from the I2S pins on one BLE device platform to the I^2S pins on another BLE device platform):

- One node must be defined as audio clock master and the other node must be defined as audio clock slave. The slave must use an external audio clock source with adjustable rate.
- For both nodes, set STMPWPER = N × (AIFDMACFG.END_FRAME_IDX + 1), where N is a whole number.
  - The value of STMPWPER equals audio latency in number of frames.
  - The value of STMPWPER also equals the memory buffer size in number of samples.
- Perform samplestamp capture on the master when it transmits the RF packet synchronization word, and include the value of the fixed-point samplestamp in the transmitted packet.
- Perform samplestamp capture on the slave when it receives the RF packet synchronization word, and store the samplestamp value of the master in the RF packet. Calculate the difference between the samplestamp values of the master and slave, which is used to:
  - Initially offset the STMPWCNT counter of the slave so that it matches the samplestamp value of the master.
  - While running, adjust the external audio clock source rate so that the difference between the samplestamp values of the slave and the master approach 0.
- For both nodes, set up DMA pointers and DMA start triggers so that the value of STMPWCNT represents the input and output buffer positions of the current frame on the ADx pins.

26.8 Error detection

The I^2S module can detect errors related to the following:

- DMA operation
- Audio clock signal integrity

The following errors are detected:

- WCLK frequency error (STMPXPERMIN:VALUE)
- Noise on the WCLK signal (IRQFLAGS:WCLK_ERR)
- Audio clock loss (IRQFLAGS:WCLK_TIMEOUT)
- DMA pointer not loaded in time (IRQFLAGS:PTR_ERR)
- DMA transfer not completed in time (IRQFLAGS:BUS_ERR)

26.9 Usage

26.9.1 Start-Up Sequence

Perform the following steps in the indicated order to begin I^2S module operation:

1. Set up dependencies
2. Configure the pins
3. Configure the serial format
4. Configure the clock
5. Configure the sample word length
6. Configure the channel mapping
7. Perform the DMA start-up sequence
8. Set up the samplestamp generator:
    a. Set the STMPWPER register.
    b. Set the STMPINTRIG and STMPOUTTRIG > STMPWPER to avoid false DMA start triggers.
    c. Set STMPCTL.EN = 1
    d. If needed, follow the guidelines for achieving constant audio latency.
    e. Otherwise, just set STMPINTRIG and STMPOUTTRIG to match the current (STMPWCNT + 2) % STMPWPER.

NOTE: DMA interrupts will begin after the DMA has completed the first sample block or blocks.

26.9.2 Shutdown Sequence

Perform the following steps in the indicated order to end I^2S module operation:

1. DMA shutdown sequence
2. Set STMPCTL.EN = 0
3. Disable the internal or external audio clock source
4. Disable dependencies

26.10 I^2S configuration guideline

1. Reset being pulled low which will initialize all the MMRs to their default value and at reset de-assertion none of the clocks are applied/running (audio clock/svt clock all will be disabled)
2. Enable the svt clock and pull the I^2S clock enable high to configure the MMRs. Don't configure the audio clock generation MMR inside ckmdig at this point.
3. For I^2S BCLK loop back configure the loopback pad as Input for BCLK to pass through
4. Configuration Sequence of I^2S MMR:
    a. All the general configurations of I^2S to be done (pins, serial format, clocks, sample word sizes, channel mapping, div values for audio clock gen)
    b. Once the I^2S audio clock gen unit related configuration is done, configure the audio clock MMR in ckmdig. [Note: Optional if internally generated clocks are to be used for I^2S operation.]
    c. Make AIFCLKCTL.WB_EN = 1 to enable the generation of wclk and bclk. [Note: Optional if we want to enable the internal generation of clocks.]
    d. AIFWCLKSRC.WCLK_SRC can be configured to select either internal or external clock generator source. After this, bclk will be provided to bclk domain and its configuration cannot change. Otherwise, it will lead to metastability issues.
    e. Configure the DMA sequence. This will enable the AIF module.
    f. Configure the MMRs related with the samplestamp generator.

26.11 I2S Registers

Table 26-1 lists the memory-mapped registers for the I2S registers. All register offset addresses not listed in Table 26-1 should be considered as reserved locations and the register contents should not be modified.

Table 26-1. I2S Registers

Offset	Acronym	Register Name	Section
0h	WCLKSRC	This register configures the **WCLK** Source	Section 26.11.1
4h	DMACFG	This register configures DMA buffer size	Section 26.11.2
8h	DIRCFG	This register configures the direction of data pins(**AD0**/ **AD1**)	Section 26.11.3
Ch	FMTCFG	This register configures the serial interface format	Section 26.11.4
10h	WMASK0	This register configures the word selection dit mask for data pin 0(**AD0**)	Section 26.11.5
14h	WMASK1	This register configures the word selection dit mask for data pin 1(**AD1**)	Section 26.11.6
20h	INPTRNXT	This register configures DMA input buffer next pointer	Section 26.11.7
24h	INPTR	This register configures the DMA input buffer current pointer	Section 26.11.8
28h	OUTPTRNXT	This register configures DMA output buffer next pointer	Section 26.11.9
2Ch	OUTPTR	This register configures DMA output buffer current pointer	Section 26.11.10
34h	STMPCTL	This register controls the samplestamp generator.	Section 26.11.11
38h	STMPXCNTCAPT0	This register gives the captured **XOSC** counter value, capture channel 0	Section 26.11.12
3Ch	STMPXPER	The register gives the XOSC period value	Section 26.11.13
40h	STMPWCNTCAPT0	This register gives the captured **WCLK** counter value, capture channel 0	Section 26.11.14
44h	STMPWPER	This register configures **WCLK** counter period value	Section 26.11.15
48h	STMPINTRIG	This register configures **WCLK** counter trigger value for input pins	Section 26.11.16
4Ch	STMPOUTTRIG	This register configures **WCLK** counter trigger value for output pins	Section 26.11.17
50h	STMPWSET	This register confiures **WCLK** counter set operation	Section 26.11.18
54h	STMPWADD	This register configures WCLK counter add operation	Section 26.11.19
58h	STMPXPERMIN	This register configures **XOSC** minimum period value	Section 26.11.20
5Ch	STMPWCNT	This register gives the current value of **WLCK** counter	Section 26.11.21
60h	STMPXCNT	This register gives the current value **XOSC** counter	Section 26.11.22
70h	IRQMASK	Interrupt Mask Register	Section 26.11.23
74h	IRQFLAGS	This registers gives the raw interrupt status	Section 26.11.24
78h	IRQSET	Interrupt Set Register. This register can be used by software for diagnostics and safety checking purposes.	Section 26.11.25
7Ch	IRQCLR	Interrupt clear register. This register allows software to clear interrupts.	Section 26.11.26
80h	MCLKDIV	This field configures **MCLK** division ratio	Section 26.11.27
84h	BCLKDIV	This field configures **BCLK** division ratio	Section 26.11.28
88h	WCLKDIV	This field configures **WCLK** division ratio	Section 26.11.29
8Ch	CLKCTL	This register controls internal audio clock	Section 26.11.30
90h	DTB	Digital test bus control	Section 26.11.31

Complex bit access types are encoded to fit into small table cells. Table 26-2 shows the codes that are used for access types in this section.

Table 26-2. I2S Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

26.11.1 WCLKSRC Register (Offset = 0h) [Reset = 00000000h]

WCLKSRC is shown in Table 26-3.

Return to the Summary Table.

This register configures the WCLK Source

Table 26-3. WCLKSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	WCLKINV	R/W	0h	This field Inverts WCLK source (pad or internal). 0h = Source is not intverted 1h = Source is inverted
1-0	WBCLKSRC	R/W	0h	This field selects WCLK/BCLK source for I2S. 0h = None ('0') 1h = External WCLK generator, from pad 2h = Internal WCLK generator, from module PRCM 3h = Not supported. Will give same WCLK as 'NONE' ('00')

26.11.2 DMACFG Register (Offset = 4h) [Reset = 00000000h]

DMACFG is shown in Table 26-4.

Return to the Summary Table.

This register configures DMA buffer size

Table 26-4. DMACFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	ENDFRMIDX	R/W	0h	This field defines the length of the DMA buffer. Writing a non-zero value to this register field enables and initializes I2S. ;Note that before doing so, all other configuration must have been done, and INPTRNXT/OUTPTRNXT must have been loaded.

26.11.3 DIRCFG Register (Offset = 8h) [Reset = 00000000h]

DIRCFG is shown in Table 26-5.

Return to the Summary Table.

This register configures the direction of data pins(AD0/AD1)

Table 26-5. DIRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-4	AD1	R/W	0h	The field configures the AD1 data pin direction 0h = Not in use (disabled) 1h = Input 2h = Output 3h = Reserved
3-2	RESERVED	R	0h	Reserved
1-0	AD0	R/W	0h	The field configures the AD0 data pin direction 0h = Not in use (disabled) 1h = Input 2h = Output 3h = Reserved

26.11.4 FMTCFG Register (Offset = Ch) [Reset = 00000000h]

FMTCFG is shown in Table 26-6.

Return to the Summary Table.

This register configures the serial interface format

Table 26-6. FMTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	DATADLY	R/W	1h	This field configures the number of BCLK periods between a WCLK edge and MSB of the first word in a phase;Note: When 0, MSB of the next word will be output in the idle period between LSB of the previous word and the start of the next word. Otherwise logical 0 will be output until the data delay has expired. 0h = Zero BCLK periods - LJF and DSP formats 1h = One BCLK periods - I2S and DSP formats 2h = Two(Min) BCLK periods - RJF format FFh = Max(255) BCLK periods - RJF format
7	MEMLEN32	R/W	0h	This register configures the size of each word stored to or loaded from memory 0h = 16-bit (one 16 bit access per sample) 1h = 32-bit(one 32-bit access per sample)
6	SMPLEDGE	R/W	1h	This field configures the sample edge/ transfer edge of data (and WCLK) on BCLK 0h = Data is sampled on the negative edge and clocked out on the positive edge. 1h = Data is sampled on the positive edge and clocked out on the negative edge.
5	DUALPHASE	R/W	1h	This field selects between dual-phase or single-phase format 0h = Single-phase: DSP format 1h = Dual-phase: I2S, LJF and RJF formats
4-0	WORDLEN	R/W	10h	Number of bits per word (8-24):;In single-phase format, this is the exact number of bits per word. ;In dual-phase format, this is the maximum number of bits per word.;Values below 8 and above 24 give undefined behavior. Data written to memory is always aligned to 16 or 24 bits as defined by MEMLEN32. Bit widths that differ from this alignment will either be truncated or zero padded.

26.11.5 WMASK0 Register (Offset = 10h) [Reset = 00000000h]

WMASK0 is shown in Table 26-7.

Return to the Summary Table.

This register configures the word selection dit mask for data pin 0(AD0)

Table 26-7. WMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MASK	R/W	3h	Bit-mask indicating valid channels in a frame on AD0.;In single-phase mode, each bit represents one channel, starting with LSB for the first word in the frame. A frame can contain up to 8 channels. Channels that are not included in the mask will not be sampled and stored in memory, and clocked out as '0'.;In dual-phase mode, only the two LSBs are considered. For a stereo configuration, set both bits. For a mono configuration, set bit 0 only. In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated when clocked out.;In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated in the second phase when clocked out.;If all bits are zero, no input words will be stored to memory, and the output data lines will be constant '0'. This can be utilized when PWM debug output is desired without any actively used output pins.

26.11.6 WMASK1 Register (Offset = 14h) [Reset = 00000000h]

WMASK1 is shown in Table 26-8.

Return to the Summary Table.

This register configures the word selection dit mask for data pin 1(AD1)

Table 26-8. WMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MASK	R/W	3h	Bit-mask indicating valid channels in a frame on AD1.;In single-phase mode, each bit represents one channel, starting with LSB for the first word in the frame. A frame can contain up to 8 channels. Channels that are not included in the mask will not be sampled and stored in memory, and clocked out as '0'.;In dual-phase mode, only the two LSBs are considered. For a stereo configuration, set both bits. For a mono configuration, set bit 0 only. In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated when clocked out.;In mono mode, only channel 0 will be sampled and stored to memory, and channel 0 will be repeated in the second phase when clocked out.;If all bits are zero, no input words will be stored to memory, and the output data lines will be constant '0'. This can be utilized when PWM debug output is desired without any actively used output pins.

26.11.7 INPTRNXT Register (Offset = 20h) [Reset = 00000000h]

INPTRNXT is shown in Table 26-9.

Return to the Summary Table.

This register configures DMA input buffer next pointer

Table 26-9. INPTRNXT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R/W	0h	Pointer to the first byte in the next DMA input buffer.;The read value equals the last written value until the currently used DMA input buffer is completed, and then becomes null when the last written value is transferred to the DMA controller to start on the next buffer. This event is signalized by IRQFLAGS.DMAIN. ;At startup, the value must be written once before and once after configuring the DMA buffer size in DMACFG.;The next pointer must be written to this register while the DMA function uses the previously written pointer. If not written in time, IRQFLAGS.PTRERR will be raised and all input pins will be disabled.

26.11.8 INPTR Register (Offset = 24h) [Reset = 00000000h]

INPTR is shown in Table 26-10.

Return to the Summary Table.

This register configures the DMA input buffer current pointer

Table 26-10. INPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R	0h	Value of the DMA input buffer pointer currently used by the DMA controller. Incremented by 1 (byte) or 2 (word) for each AHB access.

26.11.9 OUTPTRNXT Register (Offset = 28h) [Reset = 00000000h]

OUTPTRNXT is shown in Table 26-11.

Return to the Summary Table.

This register configures DMA output buffer next pointer

Table 26-11. OUTPTRNXT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R/W	0h	Pointer to the first byte in the next DMA output buffer.;The read value equals the last written value until the currently used DMA output buffer is completed, and then becomes null when the last written value is transferred to the DMA controller to start on the next buffer. This event is signalized by IRQFLAGS.DMAOUT. ;At startup, the value must be written once before and once after configuring the DMA buffer size in DMACFG. At this time, the first two samples will be fetched from memory.;The next pointer must be written to this register while the DMA function uses the previously written pointer. If not written in time, IRQFLAGS.PTRERR will be raised and all output pins will be disabled.

26.11.10 OUTPTR Register (Offset = 2Ch) [Reset = 00000000h]

OUTPTR is shown in Table 26-12.

Return to the Summary Table.

This register configures DMA output buffer current pointer

Table 26-12. OUTPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTR	R	0h	Value of the DMA output buffer pointer currently used by the DMA controller Incremented by 1 (byte) or 2 (word) for each AHB access.

26.11.11 STMPCTL Register (Offset = 34h) [Reset = 00000000h]

STMPCTL is shown in Table 26-13.

Return to the Summary Table.

This register controls the samplestamp generator.

Table 26-13. STMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	OUTRDY	R	0h	This field is low until the output pins are ready to be started by the samplestamp generator. When started (that is STMPOUTTRIG equals the WCLK counter) the bit goes back low.
1	INRDY	R	0h	This field is low until the input pins are ready to be started by the samplestamp generator. When started (that is STMPINTRIG equals the WCLK counter) the bit goes back low.
0	STMPEN	R/W	0h	This field configures the samplestamp generator. The samplestamp generator must only be enabled after it has been properly configured.;When cleared, all samplestamp generator counters and capture values are cleared. 0h = Disable the samplestamp generator 1h = Enable the samplestamp generator

26.11.12 STMPXCNTCAPT0 Register (Offset = 38h) [Reset = 00000000h]

STMPXCNTCAPT0 is shown in Table 26-14.

Return to the Summary Table.

This register gives the captured XOSC counter value, capture channel 0

Table 26-14. STMPXCNTCAPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CAPTVALUE	R	0h	The value of the samplestamp XOSC counter (STMPXCNT.CURRVALUE) last time an event was pulsed. This number corresponds to the number of 24 MHz clock cycles since the last positive edge of the selected WCLK.;The value is cleared when STMPCTL.STMPEN = 0.;Note: Due to buffering and synchronization, WCLK is delayed by a small number of BCLK periods and clk periods.;Note: When calculating the fractional part of the sample stamp, STMPXPER may be less than this bit field.

26.11.13 STMPXPER Register (Offset = 3Ch) [Reset = 00000000h]

STMPXPER is shown in Table 26-15.

Return to the Summary Table.

The register gives the XOSC period value

Table 26-15. STMPXPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	The number of 24 MHz clock cycles in the previous WCLK period (that is - the next value of the XOSC counter at the positive WCLK edge, had it not been reset to 0).;The value is cleared when STMPCTL.STMPEN = 0.

26.11.14 STMPWCNTCAPT0 Register (Offset = 40h) [Reset = 00000000h]

STMPWCNTCAPT0 is shown in Table 26-16.

Return to the Summary Table.

This register gives the captured WCLK counter value, capture channel 0

Table 26-16. STMPWCNTCAPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CAPT_VALUE	R	0h	The value of the samplestamp WCLK counter (STMPWCNT.CURRVALUE) last time an event was pulsed. This number corresponds to the number of positive WCLK edges since the samplestamp generator was enabled (not taking modification through STMPWADD/STMPWSET into account).;The value is cleared when STMPCTL.STMPEN = 0.

26.11.15 STMPWPER Register (Offset = 44h) [Reset = 00000000h]

STMPWPER is shown in Table 26-17.

Return to the Summary Table.

This register configures WCLK counter period value

Table 26-17. STMPWPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	0h	This field defines when STMPWCNT is to be reset so number of WCLK edges are found for the size of the sample buffer. This is thus a modulo value for the WCLK counter. This number must correspond to the size of the sample buffer used by the system (that is the index of the last sample plus 1).

26.11.16 STMPINTRIG Register (Offset = 48h) [Reset = 00000000h]

STMPINTRIG is shown in Table 26-18.

Return to the Summary Table.

This register configures WCLK counter trigger value for input pins

Table 26-18. STMPINTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	INSTARTWCNT	R/W	0h	This field configures the compare value used to start the incoming audio streams.;This bit field shall equal the WCLK counter value during the WCLK period in which the first input word(s) are sampled and stored to memory (that is the sample at the start of the very first DMA input buffer).;The value of this register takes effect when the following conditions are met:;- One or more pins are configured as inputs in DIRCFG.;- DMACFG has been configured for the correct buffer size, and at least 32 BCLK cycle ticks have happened.;Note: To avoid false triggers, this bit field should be set higher than STMPWPER.VALUE.

26.11.17 STMPOUTTRIG Register (Offset = 4Ch) [Reset = 00000000h]

STMPOUTTRIG is shown in Table 26-19.

Return to the Summary Table.

This register configures WCLK counter trigger value for output pins

Table 26-19. STMPOUTTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	OUTSTARTWCNT	R/W	0h	This field cofnigures the compare value used to start the outgoing audio streams.;This bit field must equal the WCLK counter value during the WCLK period in which the first output word(s) read from memory are clocked out (that is the sample at the start of the very first DMA output buffer).;The value of this register takes effect when the following conditions are met:;- One or more pins are configured as outputs in DIRCFG.;- DMACFG has been configured for the correct buffer size, and 32 BCLK cycle ticks have happened.;- 2 samples have been preloaded from memory (examine the OUTPTR register if necessary). ;Note: The memory read access is only performed when required, that is channels 0/1 must be selected in WMASK0/WMASK1.;Note: To avoid false triggers, this bit field should be set higher than STMPWPER.VALUE.

26.11.18 STMPWSET Register (Offset = 50h) [Reset = 00000000h]

STMPWSET is shown in Table 26-20.

Return to the Summary Table.

This register confiures WCLK counter set operation

Table 26-20. STMPWSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	W	0h	Sets the running WCLK counter equal to the written value.

26.11.19 STMPWADD Register (Offset = 54h) [Reset = 00000000h]

STMPWADD is shown in Table 26-21.

Return to the Summary Table.

This register configures WCLK counter add operation

Table 26-21. STMPWADD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUEINC	W	0h	Adds the written value to the running WCLK counter. If a positive edge of WCLK occurs at the same time as the operation, this will be taken into account.;To add a negative value, write "STMPWPER.VALUE - value".;

26.11.20 STMPXPERMIN Register (Offset = 58h) [Reset = 00000000h]

STMPXPERMIN is shown in Table 26-22.

Return to the Summary Table.

This register configures XOSC minimum period value;Minimum Value of STMPXPER

Table 26-22. STMPXPERMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R/W	FFFFh	Each time STMPXPER is updated, the value is also loaded into this register, provided that the value is smaller than the current value in this register.;When written, the register is reset to 0xFFFF (65535), regardless of the value written.;The minimum value can be used to detect extra WCLK pulses (this registers value will be significantly smaller than STMPXPER.VALUE).

26.11.21 STMPWCNT Register (Offset = 5Ch) [Reset = 00000000h]

STMPWCNT is shown in Table 26-23.

Return to the Summary Table.

This register gives the current value of WLCK counter

Table 26-23. STMPWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CURRVALUE	R	0h	Current value of the WCLK counter

26.11.22 STMPXCNT Register (Offset = 60h) [Reset = 00000000h]

STMPXCNT is shown in Table 26-24.

Return to the Summary Table.

This register gives the current value XOSC counter

Table 26-24. STMPXCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CURRVALUE	R	0h	Current value of the XOSC counter, latched when reading STMPWCNT.

26.11.23 IRQMASK Register (Offset = 70h) [Reset = 00000000h]

IRQMASK is shown in Table 26-25.

Return to the Summary Table.

Interrupt Mask Register;Selects mask states of the flags in IRQFLAGS that contribute to the I2S_IRQ event.

Table 26-25. IRQMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCAPT	R/W	0h	IRQFLAGS.XCNTCAPT interrupt mask 0h = Disable the interrupt mask 1h = Enable the interrupt mask
5	DMAIN	R/W	0h	IRQFLAGS.DMAIN interrupt mask 0h = Disable the interrupt mask 1h = Enable the interrupt mask
4	DMAOUT	R/W	0h	IRQFLAGS.DMAOUT interrupt mask 0h = Disable the interrupt mask 1h = Enable the interrupt mask
3	WCLKTIMEOUT	R/W	0h	IRQFLAGS.WCLKTIMEOUT interrupt mask 0h = Disable the interrupt mask 1h = Enable the interrupt mask
2	BUSERR	R/W	0h	IRQFLAGS.BUSERR interrupt mask 0h = Disable the interrupt mask 1h = Enable the interrupt mask
1	WCLKERR	R/W	0h	IRQFLAGS.WCLKERR interrupt mask 0h = Disable the interrupt mask 1h = Enable the interrupt mask
0	PTRERR	R/W	0h	IRQFLAGS.PTRERR interrupt mask. 0h = Disable the interrupt mask 1h = Enable the interrupt mask

26.11.24 IRQFLAGS Register (Offset = 74h) [Reset = 00000000h]

IRQFLAGS is shown in Table 26-26.

Return to the Summary Table.

This registers gives the raw interrupt status

Table 26-26. IRQFLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCAPT	R	0h	This interrupt is set when xcnt counter is captured either by events or software. ;Needs to be cleared by software. 0h = Interrupt did not occur 1h = Interrupt occured
5	DMAIN	R	0h	This interrupt is set when condition for this bit field event occurs (auto cleared when input pointer is updated - AIFINPTRNEXT), see description of AIFINPTRNEXT register for details. 0h = Interrupt did not occur 1h = Interrupt occured
4	DMAOUT	R	0h	This interrupt is set when condition for this bit field event occurs (auto cleared when output pointer is updated - OUTPTRNXT), see description of OUTPTRNXT register for details 0h = Interrupt did not occur 1h = Interrupt occured
3	WCLKTIMEOUT	R	0h	Set when the sample stamp generator does not detect a positive WCLK edge for 65535 clk periods. This signalizes that the internal or external BCLK and WCLK generator source has been disabled.;The bit is sticky and may only be cleared by software (by writing '1' to IRQCLR.WCLKTIMEOUT). 0h = Interrupt did not occur 1h = Interrupt occured
2	BUSERR	R	0h	This interrupt set when a DMA operation is not completed in time (that is audio output buffer underflow, or audio input buffer overflow). ;This error requires a complete restart since word synchronization has been lost. The bit is sticky and may only be cleared by software (by writing '1' to IRQCLR.BUSERR).;Note that DMA initiated transactions to illegal addresses will not trigger an interrupt. The response to such transactions is undefined. 0h = Interrupt did not occur 1h = Interrupt occured
1	WCLKERR	R	0h	This interrupt is set when: ;- An unexpected WCLK edge occurs during the data delay period of a phase. Note unexpected WCLK edges during the word and idle periods of the phase are not detected.;- In dual-phase mode, when two WCLK edges are less than 4 BCLK cycles apart.;- In single-phase mode, when a WCLK pulse occurs before the last channel.;This error requires a complete restart since word synchronization has been lost. The bit is sticky and may only be cleared by software (by writing '1' to IRQCLR.WCLKERR). 0h = Interrupt did not occur 1h = Interrupt occured
0	PTRERR	R	0h	This interrupt set when INPTRNXT or OUTPTRNXT has not been loaded with the next block address in time. ;This error requires a complete restart since word synchronization has been lost. The bit is sticky and may only be cleared by software (by writing '1' to IRQCLR.PTRERR). 0h = Interrupt did not occur 1h = Interrupt occured

26.11.25 IRQSET Register (Offset = 78h) [Reset = 00000000h]

IRQSET is shown in Table 26-27.

Return to the Summary Table.

Interrupt Set Register. This register can be used by software for diagnostics and safety checking purposes.

Table 26-27. IRQSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCAPT	W	0h	This field sets the interrupt IRQFLAGS.XCNTCAPT (unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt
5	DMAIN	W	0h	This field sets the interrupt IRQFLAGS.DMAIN (unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt
4	DMAOUT	W	0h	This field sets the interrupt IRQFLAGS.DMAOUT (unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt
3	WCLKTIMEOUT	W	0h	This field sets the interrupt IRQFLAGS.WCLKTIMEOUT(unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt
2	BUSERR	W	0h	1: Sets the interrupt of IRQFLAGS.BUSERR(unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt
1	WCLKERR	W	0h	This field sets the interrupt IRQFLAGS.WCLKERR(unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt
0	PTRERR	W	0h	This field sets the interrupt IRQFLAGS.PTRERR(unless a auto clear criteria was given at the same time, in which the set will be ignored) 0h = Writing 0 has no effect 1h = Set interrupt

26.11.26 IRQCLR Register (Offset = 7Ch) [Reset = 00000000h]

IRQCLR is shown in Table 26-28.

Return to the Summary Table.

Interrupt clear register. This register allows software to clear interrupts.

Table 26-28. IRQCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	XCNTCAPT	W	0h	Ths field clears the interrupt IRQFLAGS.XCNTCAPT (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt
5	DMAIN	W	0h	This field clears the interrupt of IRQFLAGS.DMAIN (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt
4	DMAOUT	W	0h	This field clears the interrupt IRQFLAGS.DMAOUT (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt
3	WCLKTIMEOUT	W	0h	1: Clears the interrupt of IRQFLAGS.WCLKTIMEOUT (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt
2	BUSERR	W	0h	This field clears the interrupt IRQFLAGS.BUSERR (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt
1	WCLKERR	W	0h	This field clears the interrupt IRQFLAGS.WCLKERR (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt
0	PTRERR	W	0h	This field clears the interrupt IRQFLAGS.PTRERR (unless a set criteria was given at the same time in which the clear will be ignored) 0h = Writing 0 has no effect 1h = Clear interrupt

26.11.27 MCLKDIV Register (Offset = 80h) [Reset = 00000000h]

MCLKDIV is shown in Table 26-29.

Return to the Summary Table.

This field configures MCLK division ratio

Table 26-29. MCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	MDIV	R/W	0h	An unsigned factor of the division ratio used to generate MCLK [2-1024]:; MCLK = MCUCLK/MDIV[Hz] MCUCLK is upto 96MHz. ; A value of 0 is interpreted as 1024.; A value of 1 is invalid. ; If MDIV is odd the low phase of the clock is one MCUCLK period longer than the high phase.

26.11.28 BCLKDIV Register (Offset = 84h) [Reset = 00000000h]

BCLKDIV is shown in Table 26-30.

Return to the Summary Table.

This field configures BCLK division ratio

Table 26-30. BCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BDIV	R/W	0h	An unsigned factor of the division ratio used to generate BCLK [2-1024]:; BCLK = MCUCLK/BDIV[Hz] MCUCLK can be upto 96MHz. ; A value of 0 is interpreted as 1024.; A value of 1 is invalid. ; If BDIV is odd and FMTCFG.SMPLEDGE = 0, the low phase of the clock is one MCUCLK period longer than the high phase. ; If BDIV is odd and FMTCFG.SMPLEDGE = 1 , the high phase of the clock is one MCUCLK period longer than the low phase.

26.11.29 WCLKDIV Register (Offset = 88h) [Reset = 00000000h]

WCLKDIV is shown in Table 26-31.

Return to the Summary Table.

This field configures WCLK division ratio

Table 26-31. WCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Software should not rely on the value of a reserved. Writing any other value than the reset value may result in undefined behavior.
15-0	WDIV	R/W	0h	If CLKCTL.WCLKPHASE = 0, Single phase. WCLK is high one BCLK period and low WDIV[9:0] (unsigned, [1-1023]) BCLK periods. ; WCLK = MCUCLK / BDIV*(WDIV[9:0] + 1) [Hz] MCUCLK upto 96MHz. ; If WCLKPHASE = 1, Dual phase. Each phase on WCLK (50% duty cycle) is WDIV[9:0] (unsigned, [1-1023]) BCLK periods. ; **WCLK **= **MCUCLK **/ BDIV*(2*WDIV[9:0]) [Hz] ; If WCLKPHASE = 2, User defined. WCLK is high WDIV[7:0] (unsigned, [1-255]) BCLK periods and low WDIV[15:8] (unsigned, [1-255]) BCLK periods.; WCLK = **MCUCLK **/ (BDIV*(WDIV[7:0] + WDIV[15:8]) [Hz]

26.11.30 CLKCTL Register (Offset = 8Ch) [Reset = 00000000h]

CLKCTL is shown in Table 26-32.

Return to the Summary Table.

This register controls internal audio clock

Table 26-32. CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MEN	R/W	0h	This field configures the MCLK generation 0h = Disable the generation 1h = Enable the generation
2-1	WCLKPHASE	R/W	0h	The field configures how the WCLK division ratio is calculated and used to generate different duty cycles (See WCLKDIV.WDIV)
0	WBEN	R/W	0h	This field configures WCLK/BCLK generation 0h = Disables the generation 1h = Enable the generation

26.11.31 DTB Register (Offset = 90h) [Reset = 00000000h]

DTB is shown in Table 26-33.

Return to the Summary Table.

Digital test bus control

Table 26-33. DTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SEL	R/W	0h	The field controls the select of DTB 0h = None is selected 1h = Samplestamp WCNT(16 bits) 2h = Samplestamp XCNT(16 bits) 3h = {12{1'b0},aif_words_sampled, aif_word_loaded, aif_output_en, aif_input_en}

Chapter 27

CAN-FD

This section describes the CAN-FD interface module.

27.1 Introduction

The CAN-FD module is implemented for primarily automotive applications. The module has 4KB of message RAM and supports CAN-FD operation up to 5Mbps and 64 bytes of payload. The message RAM has ECC implementation. Two event publishers and two dedicated DMA trigger interfaces are implemented.

27.2 Functions

CAN-FD module on CC27xx supports the following functional requirements:

- Designed based on Bosch MCAN IP
- Supports classic CAN and CAN-FD protocols
- Conform with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- CAN-FD module is certified according to ISO 16845
- Supports AUTOSAR and SAE J1939
- Supports Bosch CAN 2.0 A/B protocol with up to 8 message bytes
- Supports Bosch CAN-FD protocol with up to 64 message bytes
- Supports up to 1Mbps communication rate in CAN2.0 mode
- Supports up to 5Mbps communication rate in CAN-FD mode
- Supports up to 32 dedicated transmit buffers
- Supports configurable transmit FIFO for up to 32 elements
- Supports configurable transmit queue for up to 32 elements
- Supports configurable transmit event FIFO for up to 32 elements
- Supports up to 64 dedicated receive buffers
- Supports two configurable receive FIFOs for up to 64 elements each
- Supports up to 128 filter elements
- 4KB embedded SRAM for message buffering
- Supports SECDED ECC (single error correction double error detection) mechanism on message SRAM
- Supports internal and external loop back mode for self-test
- Supports time stamp counters
- Supports clock stop and wakeup feature
- Possiblity to access message RAM and MCAN registers from debugger when MCAN operation is suspended due to CPU halt
- Responds within 50ms to a wakeup CAN message
- Supports all necessary interrupt conditions as implemented in MCAN core IP
- Implementation of 2 DMA triggers for system DMA based data transfer with MCAN
- Have two clock domains - bus interface clock domain (HCLK) and CAN functional clock (CCLK) for bit timing
- The bus interface clock (HCLK) have be same or higher frequency than CAN functional clock (CCLK)
- Have internal clock prescaler to generate lower functional clock frequencies for operation at lower bit rates
- Maintain clock continuity while transitioning between data rates
- CAN interface clock is 96MHz and provided by CLKCTL module when MCAN is enabled
- CAN functional clock is 80MHz and provided by CKMDIG module
- CAN-FD module is operational only in SoC active and idle modes
- Ability to operate alongside RF radio in regards to hardware implementation as well as software handling
- AHB slave bus interface is running at core clock speed of 96 MHz
- Have idle/hold request interface with CLKCTL module

27.3 MCAN Subsystem

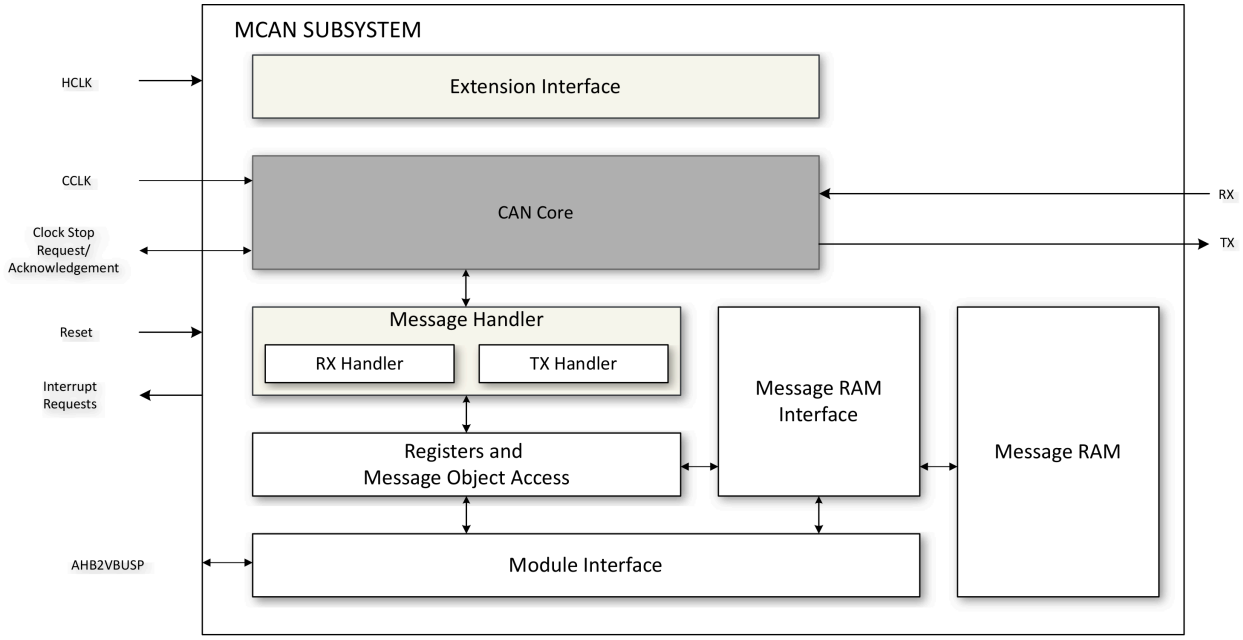


Figure 27-1. MCAN SUBSYSTEM

27.4 MCAN Functional Description

27.4.1 Operating Modes

27.4.1.1 Software Initialization

Software initialization is started by setting bit CCCR.INIT, either by software or by a hardware reset, when an uncorrected bit error is detected in the Message RAM, or by going Bus_Off. While CCCR.INIT is set, message transfer from and to the CAN bus is stopped, the status of the CAN bus output m_can_tx is recessive (HIGH). The counters of the Error Management Logic EML are unchanged. Setting CCCR.INIT does not change any configuration register. Resetting CCCR.INIT finishes the software initialization. Afterwards the Bit Stream Processor BSP synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive recessive bits (≡ Bus_Idle) before it can take part in bus activities and start the message transfer.

Access to the M_CAN configuration registers is only enabled when both bits CCCR.INIT and CCCR.CCE are set (protected write).

CCCR.CCE can only be set/reset while CCCR.INIT = ‘1’. CCCR.CCE is automatically reset when CCCR.INIT is reset.

The following registers are reset when CCCR.CCE is set

- HPMS - High Priority Message Status
- RXF0S - Rx FIFO 0 Status
- RXF1S - Rx FIFO 1 Status
- TXFQS - Tx FIFO/Queue Status
- TXBRP - Tx Buffer Request Pending
- TXBTO - Tx Buffer Transmission Occurred
- TXBCF - Tx Buffer Cancellation Finished
- TXEFS - Tx Event FIFO Status

The Timeout Counter value TOCV.TOC is preset to the value configured by TOCC.TOP when CCCR.CCE is set.

In addition the state machines of the Tx Handler and Rx Handler are held in idle state while CCCR.CCE = ‘1’.

The following registers are only writeable while CCCR.CCE = ‘0’

- TXBAR - Tx Buffer Add Request
- TXBCR - Tx Buffer Cancellation Request

CCCR.TEST and CCCR.MON can only be set by the Host while CCCR.INIT = ‘1’ and CCCR.CCE = ‘1’. Both bits may be reset at any time. CCCR.DAR can only be set/reset while CCCR.INIT = ‘1’ and CCCR.CCE = ‘1’.

Note

In case the Message RAM is equipped with parity or ECC functionality, it is recommended to initialize the Message RAM after hardware reset by writing e.g. 0x00000000 to each Message RAM word to create valid parity/ECC checksums. This avoids that reading from uninitialized Message RAM sections will activate interrupt IR.BEC (Bit Error Corrected) or IR.BEU (Bit Error Uncorrected).

27.4.1.2 Normal Operation

Once the M_CAN is initialized and CCCR.INIT is reset to zero, the M_CAN synchronizes itself to the CAN bus and is ready for communication.

After passing the acceptance filtering, received messages including Message ID and DLC are stored into a dedicated Rx Buffer or into Rx FIFO 0 or Rx FIFO 1.

For messages to be transmitted dedicated Tx Buffers and/or a Tx FIFO or a Tx Queue can be initialized or updated. Automated transmission on reception of remote frames is not implemented.

27.4.1.3 CAN FD Operation

There are two variants in the CAN FD frame transmission, first the CAN FD frame without bit rate switching. The second variant is the CAN FD frame where control field, data field, and CRC field are transmitted with a higher bit rate than the beginning and the end of the frame.

The previously reserved bit in CAN frames with 11-bit identifiers and the first previously reserved bit in CAN frames with 29-bit identifiers will now be decoded as FDF bit (FD Format indicator). FDF = recessive signifies a CAN FD frame, FDF = dominant signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF, res and BRS, decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by res = dominant and BRS = recessive. The coding of res = recessive is reserved for future expansion of the protocol. In case the M_CAN receives a frame with FDF = recessive and res = recessive, it will signal a Protocol Exception Event by setting bit PSR.PXE. When Protocol Exception Handling is enabled (CCCR.PXHD = ‘0’), this causes the operation state to change from Receiver (PSR.ACT = “10”) to Integrating (PSR.ACT = “00”) at the next sample point. In case Protocol Exception Handling is disabled (CCCR.PXHD = ‘1’), the M_CAN will treat a recessive res bit as an form error and will respond with an error frame.

CAN FD operation is enabled by programming CCCR.FDOE. In case CCCR.FDOE = ‘1’, transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured via bit FDF in the respective Tx Buffer element. With CCCR.FDOE = ‘0’, received frames are interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if bit FDF of a Tx Buffer element is set. CCCR.FDOE and CCCR.BRSE can only be changed while CCCR.INIT and CCCR.CCE are both set.

With CCCR.FDOE = ‘0’, the setting of bits FDF and BRS is ignored and frames are transmitted in Classic CAN format. With CCCR.FDOE = ‘1’ and CCCR.BRSE = ‘0’, only bit FDF of a Tx Buffer element is evaluated. With CCCR.FDOE = ‘1’ and CCCR.BRSE = ‘1’, transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with bits FDF and BRS set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significant higher than in the CAN FD arbitration phase. In this case disable the CAN FD bit rate switching option for transmissions.

- During system startup all nodes are transmitting Classic CAN messages until it is verified that they are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wake-up messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD capable. Non CAN FD nodes are held in Silent mode until programming has completed. Then all nodes switch back to Classic CAN communication.

In the CAN FD format, the coding of the DLC differs from the standard CAN format. The DLC codes 0 to 8 have the same coding as in standard CAN, the codes 9 to 15, which in standard CAN all code a data field of 8 bytes, are coded according to Table 26-1 below.

Table 27-1. Coding of DLC in CAN FD

DLC	9	10	11	12	13	14	15
Number of Data Bytes	12	16	20	24	32	48	64

In CAN FD frames, the bit timing will be switched inside the frame, after the BRS (Bit Rate Switch) bit, if this bit is recessive. Before the BRS bit, in the CAN FD arbitration phase, the nominal CAN bit timing is used as defined by the Nominal Bit Timing & Prescaler Register NBTP. In the following CAN FD data phase, the data phase bit timing is used as defined by the Data Bit Timing & Prescaler Register DBTP. The bit timing is switched back from the data phase timing at the CRC delimiter or when an error is detected, whichever occurs first.

The maximum configurable bit rate in the CAN FD data phase depends on the CAN clock frequency (m_can_cclk). Example: with a CAN clock frequency of 20MHz and the shortest configurable bit time of 4 tq, the bit rate in the data phase is 5 Mbit/s.

In both data frame formats, CAN FD and CAN FD with bit rate switching, the value of the bit ESI (Error Status Indicator) is determined by the transmitter's error state at the start of the transmission. If the transmitter is error passive, ESI is transmitted recessive, else it is transmitted dominant.

27.4.1.4 Transmitter Delay Compensation

During the data phase of a CAN FD transmission only one node is transmitting, all others are receivers. The length of the bus line has no impact. When transmitting via pin m_can_tx the M_CAN receives the transmitted data from its local CAN transceiver via pin m_can_rx. The received data is delayed by the transmitter delay. In case this delay is greater than TSEG1 (time segment before sample point), a bit error is detected. In order to enable a data phase bit time that is even shorter than the transmitter delay, the delay compensation is introduced. Without transmitter delay compensation, the bit rate in the data phase of a CAN FD frame is limited by the transmitter delay.

27.4.1.4.1 Description

The M_CAN's protocol unit has implemented a delay compensation mechanism to compensate the transmitter delay, thereby enabling transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver.

To check for bit errors during the data phase of transmitting nodes, the delayed transmit data is compared against the received data at the Secondary Sample Point SSP. If a bit error is detected, the transmitter will react on this bit error at the next following regular sample point. During arbitration phase the delay compensation is always disabled.

The transmitter delay compensation enables configurations where the data bit time is shorter than the transmitter delay, it is described in detail in ISO 11898-1:2015. It is enabled by setting bit DBTP.TDC.

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the M_CAN's transmit output m_can_tx through the transceiver to the receive input m_can_rx plus the transmitter delay compensation offset as configured by TDCR.TDCO. The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (e.g. half of the bit time in the data phase). The position of the secondary sample point is rounded down to the next integer number of mtq.

PSR.TDCV shows the actual transmitter delay compensation value. PSR.TDCV is cleared when CCCR.INIT is set and is updated at each transmission of an FD frame while DBTP.TDC is set.

The following boundary conditions have to be considered for the transmitter delay compensation implemented in the M_CAN:

- The sum of the measured delay from m_can_tx to m_can_rx and the configured transmitter delay compensation offset TDCR.TDCO has to be less than 6 bit times in the data phase.
- The sum of the measured delay from m_can_tx to m_can_rx and the configured transmitter delay compensation offset TDCR.TDCO has to be less or equal 127 mtq. In case this sum exceeds 127 mtq, the maximum value of 127 mtq is used for transmitter delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs

27.4.1.4.2 Transmitter Delay Compensation Measurement

If transmitter delay compensation is enabled by programming DBTP.TDC = '1', the measurement is started within each transmitted CAN FD frame at the falling edge of bit FDF to bit res. The measurement is stopped when this edge is seen at the receive input m_can_rx of the transmitter. The resolution of this measurement is one mtq.

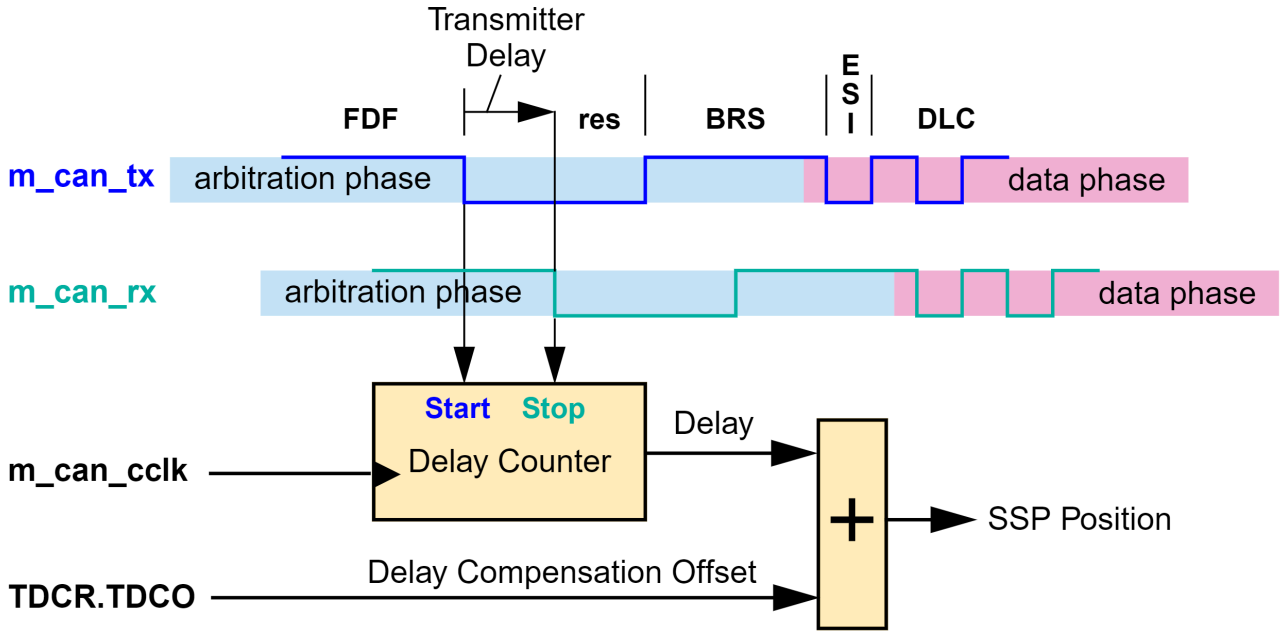


Figure 27-2. Transmitter Delay Measurement

To avoid that a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in a to early SSP position, the use of a transmitter delay compensation filter window can be enabled by programming TDCR.TDCF.

This defines a minimum value for the SSP position. Dominant edges on m_can_rx, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least TDCR.TDCF AND m_can_rx is low.

27.4.1.5 Restricted Operation Mode

In Restricted Operation Mode, the node is able to receive data and remote frames and acknowledge valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The error counters (ECR.REC, ECR.TEC) are frozen while Error Logging (ECR.CEL) is active. The Host can set the M_CAN into Restricted Operation mode by

setting bit CCCR.ASM. The bit can only be set by the Host when both CCCR.CCE and CCCR.INIT are set to ‘1’. The bit can be reset by the Host at any time.

Restricted Operation Mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM.

The Restricted Operation Mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation Mode after it has received a valid frame.

If the M_CAN is connected to a Clock Calibration, CCCR.ASM is controlled by input m_can_cok. In case m_can_cok switches to ‘0’, bit CCCR.ASM is set. When m_can_cok switches back to ‘1’, bit CCCR.ASM returns to the previously written value.When there is no Clock Calibration on CAN unit connected input m_can_cok is hardwired to ‘1’.

Note

The Restricted Operation Mode must not be combined with the Loop Back Mode (internal or external).

27.4.1.6 Bus Monitoring Mode

The M_CAN is set in Bus Monitoring Mode by programming CCCR.MON to one. In Bus Monitoring Mode (see ISO 11898-1:2015, 10.14 Bus monitoring), the M_CAN is able to receive valid data frames and valid remote frames, but cannot start a transmission. In this mode, it sends only recessive bits on the CAN bus. If the M_CAN is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the M_CAN monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring Mode register TXBRP is held in reset state.

The Bus Monitoring Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. Figure 5 shows the connection of signals m_can_tx and m_can_rx to the M_CAN in Bus Monitoring Mode.

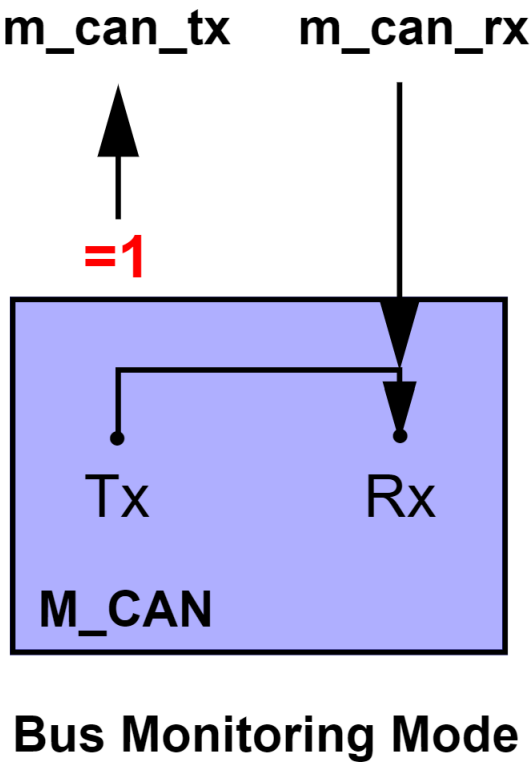


Figure 27-3. Pin Control in Bus Monitoring Mode

27.4.1.7 Disabled Automatic Retransmission

According to the CAN Specification (see ISO 11898-1:2015, 8.3.4 Recovery Management), the M_CAN provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled. To support time-triggered communication as described in ISO 11898-1:2015, chapter 9.2, the automatic retransmission may be disabled via CCCR.DAR.

27.4.1.7.1 Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending bit TXBRP.TRPx is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

- Successful transmission:

  Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set

  Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx not set
- Successful transmission in spite of cancellation:

  Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set

  Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set
- Arbitration lost or frame transmission disturbed:

  Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx not set

Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = “10” (transmission in spite of cancellation).

27.4.1.8 Power Down (Sleep Mode)

The M_CAN can be set into power down mode controlled by input signal m_can_clkstop_req or via CC Control Register CCCR.CSR. As long as the clock stop request signal m_can_clkstop_req is active, bit CCCR.CSR is read as one.

When all pending transmission requests have completed, the M_CAN waits until bus idle state is detected. Then the M_CAN sets then CCCR.INIT to one to prevent any further CAN transfers. Now the M_CAN acknowledges that it is ready for power down by setting output signal m_can_clkstop_ack to one and CCCR.CSA to one. In this state, before the clocks are switched off, further register accesses can be made. A write access to CCCR.INIT will have no effect. Now the module clock inputs m_can_hclk and m_can_cclk may be switched off.

To leave power down mode, the application has to turn on the module clocks before resetting signal m_can_clkstop_req resp. CC Control Register flag CCCR.CSR. The M_CAN will acknowledge this by resetting output signal m_can_clkstop_ack and resetting CCCR.CSA. Afterwards, the application can restart CAN communication by resetting bit CCCR.INIT.

27.4.1.8.1 MCAN clock stop and wake operations

Clock stop in functional mode with wakeup request disabled (WAKEUPREQEN =0)

- When MCANSS_CLKCTL.STOPREQ bit is set the clock stop request is asserted at MCAN core input.
- MCAN module completes any ongoing communication and asserts clock stop ack signal at its output.
- The clock stop logic in the MCANSS can use the clock stop ack signal to gate off both HCLK and CCLK to MCAN. MCAN core sets CCCR.INIT bit to 1 while asserting clock stop ack signal.
- Clock stop ack signal when high sets MCANSS_CLKSTS.CLKSTOP_ACKSTS bit to 1.
- In this state, MCAN module is fully clock gated and will not be able to receive any data from RXD pin when MCANSS_CTRL.WAKEUPREQEN bit is 0.
- Software has to clear MCANSS_CLKCTL.STOPREQ bit when needed which will de-assert clock stop request upon which both HCLK and CCLK are ungated to MCAN core.
- Then MCAN core de-asserts clock stop ack signal which is used to clear MCANSS_CLKSTS.CLKSTOP_ACKSTS bit.
- Software can clear CCCR.INIT to 0 when necessary and put the MCAN module back in operation.

Clock stop in functional mode with wakeup request enabled (WAKEUPREQEN = 1, AUTOWAKEUP = 0)

- When MCANSS_CLKCTL.STOPREQ is set by software with MCANSS_CTRL.WAKEUPREQEN = 1 and MCANSS_CTRL.AUTOWAKEUP = 0 then the clock stop request is asserted.
- MCAN sets CCCR.INIT = 1 once it becomes idle and then provides clock stop ack signal for gating the HCLK and CCLK.
- Clock stop ack signal when high sets MCANSS_CLKSTS.CLKSTOP_ACKSTS bit to 1.
- Now when there is any 1 to 0 transition detected on RXD pin (which is filtered if glitch filter is enabled) while clocks are gated, MCAN asserts clock stop wake request to MCANSS.
- This signal when high clears MCANSS_CLKCTL.STOPREQ bit and sets MCANSS_CLKSTS.STOPREQ_HW_OVR bit. The purpose is to let software know that stop request was cleared due to hardware override mechanism.
- When clock stop request is de-asserted, HCLK and CCLK are ungated to MCANSS. MCANSS_CLKSTS.CLKSTOP_ACKSTS bit is cleared once clock stop ack signal is de-asserted from MCANSS.
- MCANSS_CLKSTS.STOPREQ_HW_OVR bit will be cleared by hardware when software sets MCANSS_CLKCTL.STOPREQ bit next time for module low power state.
- Clock stop wake request can be used to trigger an interrupt when MCANSS_CLKCTL.WAKE_INT_EN bit is set.
- Software can clear CCCR.INIT to 0 and put the MCAN module back in operation.

Clock stop in functional mode with auto wakeup feature enabled (WAKEUPREQEN = 1, AUTOWAKEUP = 1)

- MCAN operation in the case of clock stop and auto wake up with MCANSS_CTRL.WAKEUPREQEN = 1 and MCANSS_CTRL.AUTOWAKEUP = 1 configuration is similar to MCANSS_CTRL.WAKEUPREQEN = 1 and MCANSS_CTRL.AUTOWAKEUP = 0 except that CCCR.INIT bit will be cleared automatically by the read-modify-write logic in MCANSS.
- When the clocks are ungated due to clock stop wake request upon RXD pin activity, MCAN de-asserts the clock stop ack signal and the hardware mechanism in MCANSS clears CCCR.INIT bit when the clock stop ack signal goes low.
- The CAN bus is a 2-wire differential bus using non-return-to-zero (NRZ) encoding and has two states:

  – Recessive state (logical 1)

  – Dominant state (logical 0)

  In idle state the CAN bus is in Recessive state. The RXD pin activity is considered when this bus goes to dominant state.
- MCAN module is re-enabled automatically by hardware in this scenario and there is no need for software to clear the CCCR.INIT bit.

The wakeup scenarios discussed here are related to device active or idle modes only and not related to standby mode. In active or idle modes the HCLK and CCLK are available at the input of CANFD and gated off inside the module during sleep. When the wakeup condition is received, these clocks are ungated to resume module operation.

In the case of standby scenario, we need to take an interrupt from an IOC/GPIO based on Rx falling edge to wake up the SoC from standby and then reenable clock source like AFOSC and then reconfigure the CANFD registers before the module is put back in operation. This guideline is same as how any other serial communication module is handled for standby exit scenario.

Note

There is no retention of CANFD registers so all register configuration data is lost upon standby entry. CANFD registers have to be reinitialized after wake from standby before the module is put back in operation.

27.4.1.8.2 MCAN debug suspend operation

- The MCAN module implements debug suspend feature. The module operation will suspend when the CPU is halted for debug with MCANSS_CTRL.DBGSUSP_FREE = 0.
- When CPU halt signal is asserted to MCAN and if MCANSS_CTRL.DBGSUSP_FREE bit is set to 0, the clock stop request is asserted to MCANSS.
- MCAN completes pending operations and sets CCCR.INIT = 1 once the CAN bus becomes idle and subsequently asserts clock stop ack signal.
- This clock stop ack status is captured in the CCCR.CSA bit but it is not captured in the MCANSS_CLKSTS.CLKSTOP_ACKSTS bit within the MCANSS.
- The clock stop ack status in the MCANSS status register is masked based on the clock stop request bit in the MCANSS_CLKCTL register.
- Both HCLK and CCLK continue to run and they are not gated under this condition. This allows debugger accesses to message RAM and CAN registers when the module is stopped.
- When the CPU comes out of debug halt, the clock stop request is de-asserted to MCAN core. CAN core de-asserts clock stop ack signal once the clock stop request is de-asserted.
- At this stage, if MCANSS_STRL.AUTOWAKEUP = 1 then the read-modify-write mechanism in the MCANSS will automatically make CCCR.INIT = 0 and re-enables MCAN operation.
- If MCANSS_STRL.AUTOWAKEUP = 0 when cock stop ack signal is de-asserted due to CPU coming out of debug halt, then MCAN operation should be re-enabled by software by clearing the CCCR.INIT bit.

- If there is any activity on RXD pin while MCAN is stopped due to CPU debug halt and if the MCANSS_CTRL.WAKEUPREQEN = 1 then clock stop wake signal will be asserted by MCAN core.
- But this will not take any effect on clock stop request as that is controlled based on debug halt. Clock stop request is de-asserted only when CPU comes out of debug halt.
- Clock stop wake interrupt will not be generated even if CANSS_CLKCTL.WAKE_INT_EN = 1 in this scenario as clock stop wake output from Bosch CAN controller is masked based on the clock stop request bit in the MCANSS_CLKCTL register.
- When CPU halt signal is asserted to MCAN and if MCANSS_CTRL.DBGSUSP_FREE bit is set to 1, the clock stop request is not asserted and MCAN continues to remain in operational state. The reset value of MCANSS_CTRL.DBGSUSP_FREE bit is 1 which keeps MCAN operational when CPU halt is asserted.
- During suspend mode the auto-clear feature is disabled. The following register fields have an auto-clear feature:
  - MCAN_ECR.CEL
  - MCAN_PSR.LEC
  - MCAN_PSR.DLEC
  - MCAN_PSR.RESI
  - MCAN_PSR.RBRS
  - MCAN_PSR.RFDF
  - MCAN_PSR.PXE

27.4.1.9 Test Modes

To enable write access to register TEST (see Section 2.3.5), bit CCCR.TEST has to be set to one. This allows the configuration of the test modes and test functions.

Four output functions are available for the CAN transmit pin m_can_tx by programming TEST.TX. Additionally to its default function – the serial data output – it can drive the CAN Sample Point signal to monitor the M_CAN's bit timing and it can drive constant dominant or recessive values. The actual value at pin m_can_rx can be read from TEST.RX. Both functions can be used to check the CAN bus' physical layer.

Due to the synchronization mechanism between CAN clock and Host clock domain, there may be a delay of several Host clock periods between writing to TEST.TX until the new configuration is visible at output pin m_can_tx. This applies also when reading input pin m_can_rx via TEST.RX.

Note

Test modes should be used for production tests or self test only. The software control for pin m_can_tx interferes with all CAN protocol functions. It is not recommended to use test modes for application.

27.4.1.9.1 External Loop Back Mode

The M_CAN can be set in External Loop Back Mode by programming TEST.LBCK to one. In Loop Back Mode, the M_CAN treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into an Rx Buffer or an Rx FIFO. Figure 5 shows the connection of signals m_can_tx and m_can_rx to the M_CAN in External Loop Back Mode.

This mode is provided for hardware self-test. To be independent from external stimulation, the M_CAN ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop Back Mode. In this mode the M_CAN performs an internal feedback from its Tx output to its Rx input. The actual value of the m_can_rx input pin is disregarded by the M_CAN. The transmitted messages can be monitored at the m_can_tx pin.

27.4.1.9.2 Internal Loop Back Mode

Internal Loop Back Mode is entered by programming bits TEST.LBCK and CCCR.MON to one. This mode can be used for a "Hot Selftest", meaning the M_CAN can be tested without affecting a running CAN system connected to the pins m_can_tx and m_can_rx. In this mode pin m_can_rx is disconnected from the M_CAN

and pin m_can_tx is held recessive. Figure 5 shows the connection of m_can_tx and m_can_rx to the M_CAN in case of Internal Loop Back Mode.

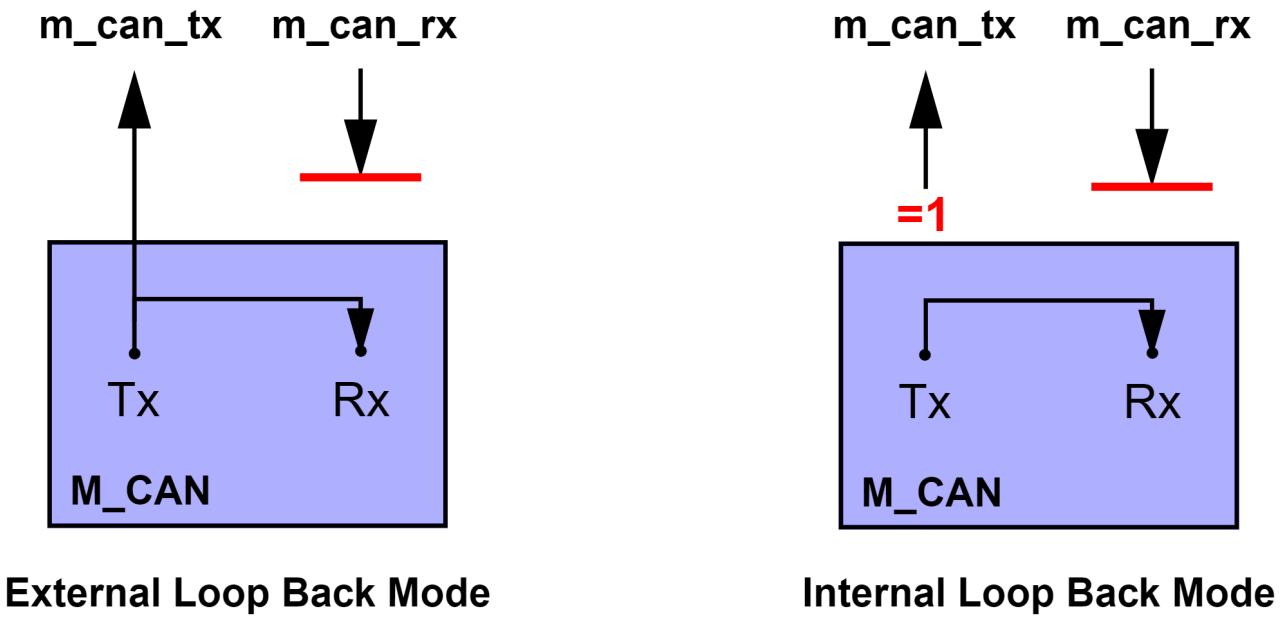


Figure 27-4. Pin Control in Loop Back Modes

27.4.2 Timestamp Generation

The MCAN module has integrated a 16-bit wrap-around counter for timestamp generation. The timestamp counter prescaler MCAN_TSCC.TCP field can be configured to clock the counter in multiples of CAN bit times (1-16). The counter is readable by way of the MCAN_TSCV.TSC field. A write access to the MCAN_TSCV register resets the counter to zero. When the timestamp counter wraps around the interrupt MCAN_IR.TSW flag is set. On start of a frame reception/transmission the counter value is captured and stored into the timestamp section of an Rx Buffer/Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element.

The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = “01”, the Timestamp Counter is incremented in multiples of CAN bit times [1…16] depending on the configuration of TSCC.TCP. A wraparound sets interrupt flag IR.TSW.

Write access resets the counter to zero. When TSCC.TSS = “10”, TSC reflects the external Timestamp Counter value. A write access has no impact.

The TSW bit shows the the wraparound for the timer(internal/external) selected for time stamping the Rx/Tx message while EXT_TS_CNTR_OVFL is exclusively for external timestamp counter only.

27.4.2.1 External Timestamp Counter

For CAN FD operation mode the MCAN core requires an external timestamp counter. An externally generated 16-bit vector may substitute the integrated 16-bit CAN bit time counter (internal timestamp counter) for receive and transmit timestamp generation. An external 16-bit timestamp counter can be used by programming the MCAN_TSCC.TSS field.

The external timestamp counter uses the interface clock (MCANx_ICLK) as a reference clock. The MCAN core accepts a 16-bit timestamp. A 24-bit prescaler provides a programmable resolution for the timestamp (see MCANSS_EXT_TS_PRESCALER.PRESCALER bit field). The external timestamp counter can be enabled or disabled through the MCANSS_CTRL.EXT_TS_CNTR_EN bit. When disabled, the counter is reset back to zero.

While enabled, the counter keeps incrementing. When the timestamp rolls over, the MCAN_IRQ_TS interrupt is generated.

When the timestamp rolls over, the MCANSS_IRS register is set. The MCANSS_IE register can be affected by writing to the MCANSS_IESS register to set or to the MCANSS_IECS register to clear. The MCANSS_IESS register is a shadow register mapped to the same address as the MCANSS_IE register. The level interrupt is a reflection of both MCANSS_IRS and MCANSS_IE being set. The MCANSS_IES register reflects the level interrupt. When an rollover event occurs, the interrupt counter is incremented. Writing to the MCANSS_ICS register to clear the MCANSS_IRS register will also decrement the interrupt counter. Writing to the MCANSS_EOI register will issue another pulse if the interrupt counter is not zero.

The rollover event can be artificially simulated by software through writing to the Interrupt Set Shadow register (MCANSS_ISS). The MCANSS_ISS register is a shadow register mapped to the same address as the MCANSS_IRS register.

27.4.2.2 Block Diagram

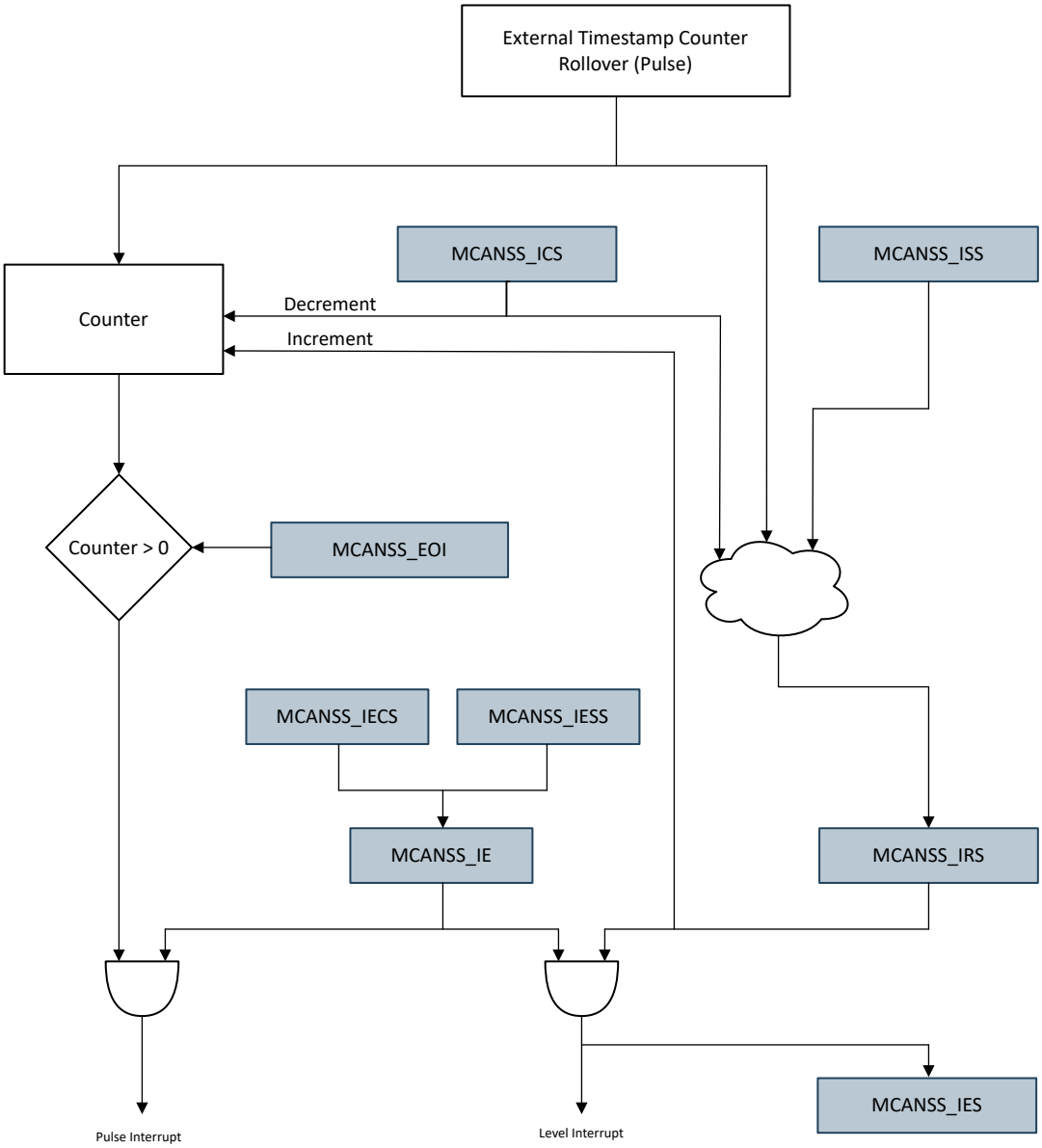


Figure 27-5. External Timestamp Counter Interrupt

27.4.3 Timeout Counter

To signal timeout conditions for Rx FIFO 0, Rx FIFO 1, and the Tx Event FIFO the M_CAN supplies a 16-bit Timeout Counter. It operates as down-counter and uses the same prescaler controlled by TSCC.TCP as the Timestamp Counter. The Timeout Counter is configured via register TOCC. The actual counter value can be read from TOCV.TOC. The Timeout Counter can only be started while CCCR.INIT = '0'. It is stopped when CCCR.INIT = '1', e.g. when the M_CAN enters Bus_Off state.

The operation mode is selected by TOCC.TOS. When operating in Continuous Mode, the counter starts when CCCR.INIT is reset. Awr ite to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting.

When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. Writing to TOCV has no effect.

When the counter reaches zero, interrupt flag IR.TOO is set. In Continuous Mode, the counter is immediately restarted at TOCC.TOP.

Note

The clock signal for the Timeout Counter is derived from the CAN Core's sample point signal. Therefore the point in time where the Timeout Counter is decremented may vary due to the synchronization / re-synchronization mechanism of the CAN Core. If the bit rate switch feature in CAN FD is used, the timeout counter is clocked differently in arbitration and data field.

27.4.4 Rx Handling

The Rx Handler controls the acceptance filtering, the transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs, as well as the Rx FIFO's Put and Get Indices.

27.4.4.1 Acceptance Filtering

The M_CAN offers the possibility to configure two sets of acceptance filters, one for standard identifiers and one for extended identifiers. These filters can be assigned to an Rx Buffer or to Rx FIFO 0,1. For acceptance filtering each list of filters is executed from element #0 until the first matching element. Acceptance filtering stops at the first matching element. The following filter elements are not evaluated for this message.

The main features are:

- Each filter element can be configured as
  - range filter (from - to)
  - filter for one or two dedicated IDs
  - classic bit mask filter
- Each filter element is configurable for acceptance or rejection filtering
- Each filter element can be enabled / disabled individually
- Filters are checked sequentially, execution stops with the first matching filter element

Related configuration registers are:

- Global Filter Configuration GFC
- Standard ID Filter Configuration SIDFC
- Extended ID Filter Configuration XIDFC
- Extended ID AND Mask XIDAM

Depending on the configuration of the filter element (SFEC/EFEC) a match triggers one of the following actions:

- Store received frame in FIFO 0 or FIFO 1
- Store received frame in Rx Buffer
- Store received frame in Rx Buffer and generate pulse at filter event pin
- Reject received frame

- Set High Priority Message interrupt flag IR.HPM
- Set High Priority Message interrupt flag IR.HPM and store received frame in FIFO 0 or FIFO 1

Acceptance filtering is started after the complete identifier has been received. After acceptance filtering has completed, and if a matching Rx Buffer or Rx FIFO has been found, the Message Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If the CAN protocol controller has detected an error condition (e.g. CRC error), this message is discarded with the following impact on the affected Rx Buffer or Rx FIFO:

Rx Buffer

New Data flag of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data. For error type see PSR.LEC respectively PSR.DLEC.

Rx FIFO

Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data. For error type see PSR.LEC respectively PSR.DLEC. In case the matching Rx FIFO is operated in overwrite mode, the boundary conditions described in Section 3.4.2.2 have to be considered.

Note

When an accepted message is written to one of the two Rx FIFOs, or into an Rx Buffer, the unmodified received identifier is stored independent of the filter(s) used. The result of the acceptance filter process is strongly depending on the sequence of configured filter elements.

27.4.4.1.1 Range Filter

The filter matches for all received frames with Message IDs in the range defined by SF1ID/SF2ID resp. EF1ID/EF2ID.

There are two possibilities when range filtering is used together with extended frames:

- EFT = “00”: The Message ID of received frames is ANDed with the Extended ID AND Mask (XIDAM) before the range filter is applied
- EFT = “11”: The Extended ID AND Mask (XIDAM) is not used for range filtering

27.4.4.1.2 Filter for specific IDs

Afilter element can be configured to filter for one or two specific Message IDs. To filter for one specific Message ID, the filter element has to be configured with SF1ID = SF2ID resp. EF1ID = EF2ID.

27.4.4.1.3 Classic Bit Mask Filter

Classic bit mask filtering is intended to filter groups of Message IDs by masking single bits of a received Message ID.With classic bit mask filtering SF1ID/EF1ID is used as Message ID filter, while SF2ID/EF2ID is used as filter mask.

A zero bit at the filter mask will mask out the corresponding bit position of the configured ID filter, e.g. the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are one are relevant for acceptance filtering.

In case all mask bits are one, a match occurs only when the received Message ID and the Message ID filter are identical. If all mask bits are zero, all Message IDs match.

27.4.4.1.4 Standard Message ID Filtering

Figure 6 below shows the flow for standard Message ID (11-bit Identifier) filtering. The Standard Message ID Filter element is described in Section 2.4.5.

Controlled by the Global Filter Configuration GFC and the Standard ID Filter Configuration SIDFC Message ID, Remote Transmission Request bit (RTR), and the Identifier Extension bit (IDE) of received frames are compared against the list of configured filter elements.

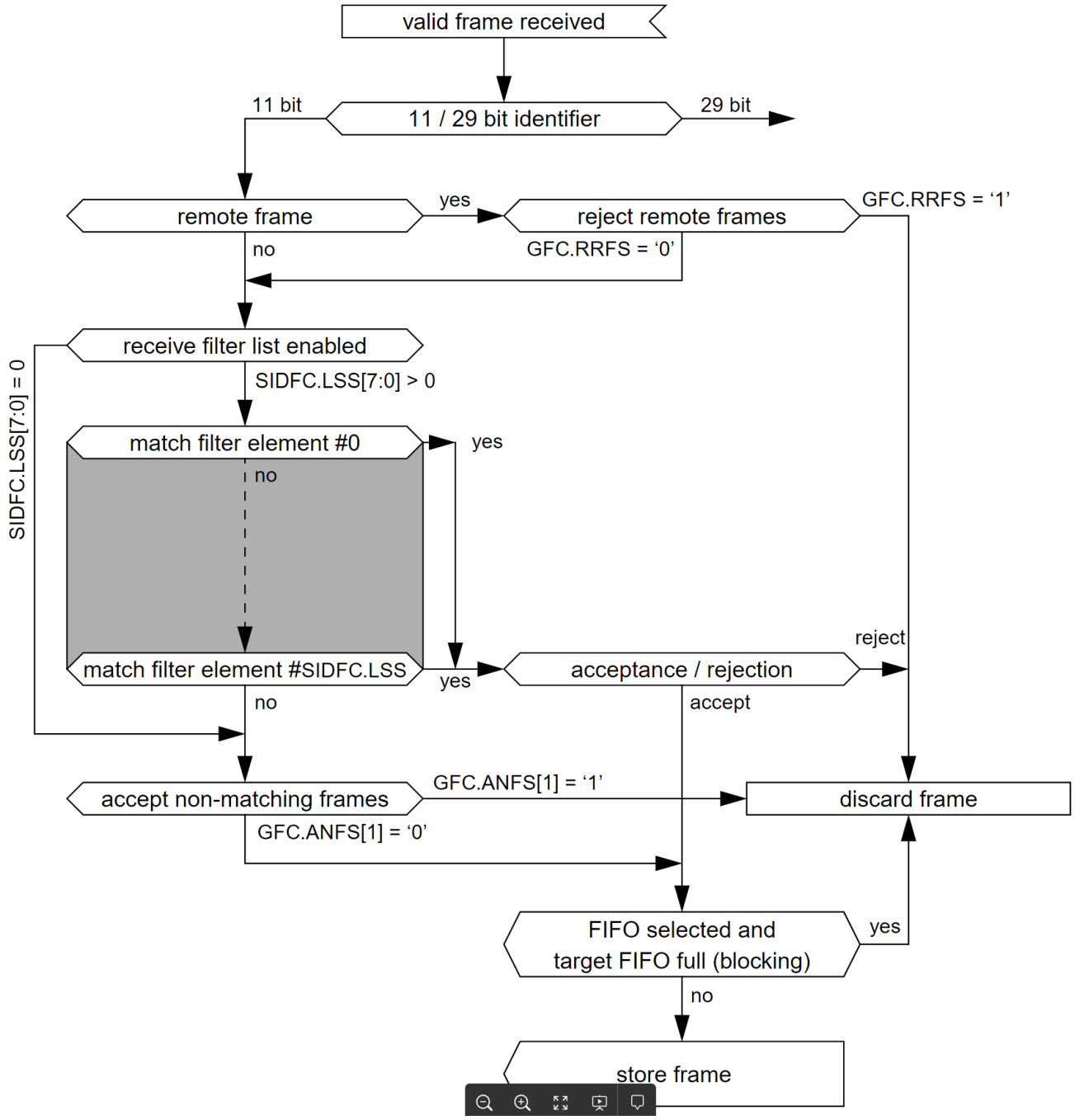


Figure 27-6. Standard Message ID Filter Path

27.4.4.1.5 Extended Message ID Filtering

Figure 7 below shows the flow for extended Message ID (29-bit Identifier) filtering. The Extended Message ID Filter element is described in Section 2.4.6.

Controlled by the Global Filter Configuration GFC and the Extended ID Filter Configuration XIDFC Message ID, Remote Transmission Request bit (RTR), and the Identifier Extension bit (IDE) of received frames are compared against the list of configured filter elements.

The Extended ID AND Mask XIDAM is ANDed with the received identifier before the filter list is executed.

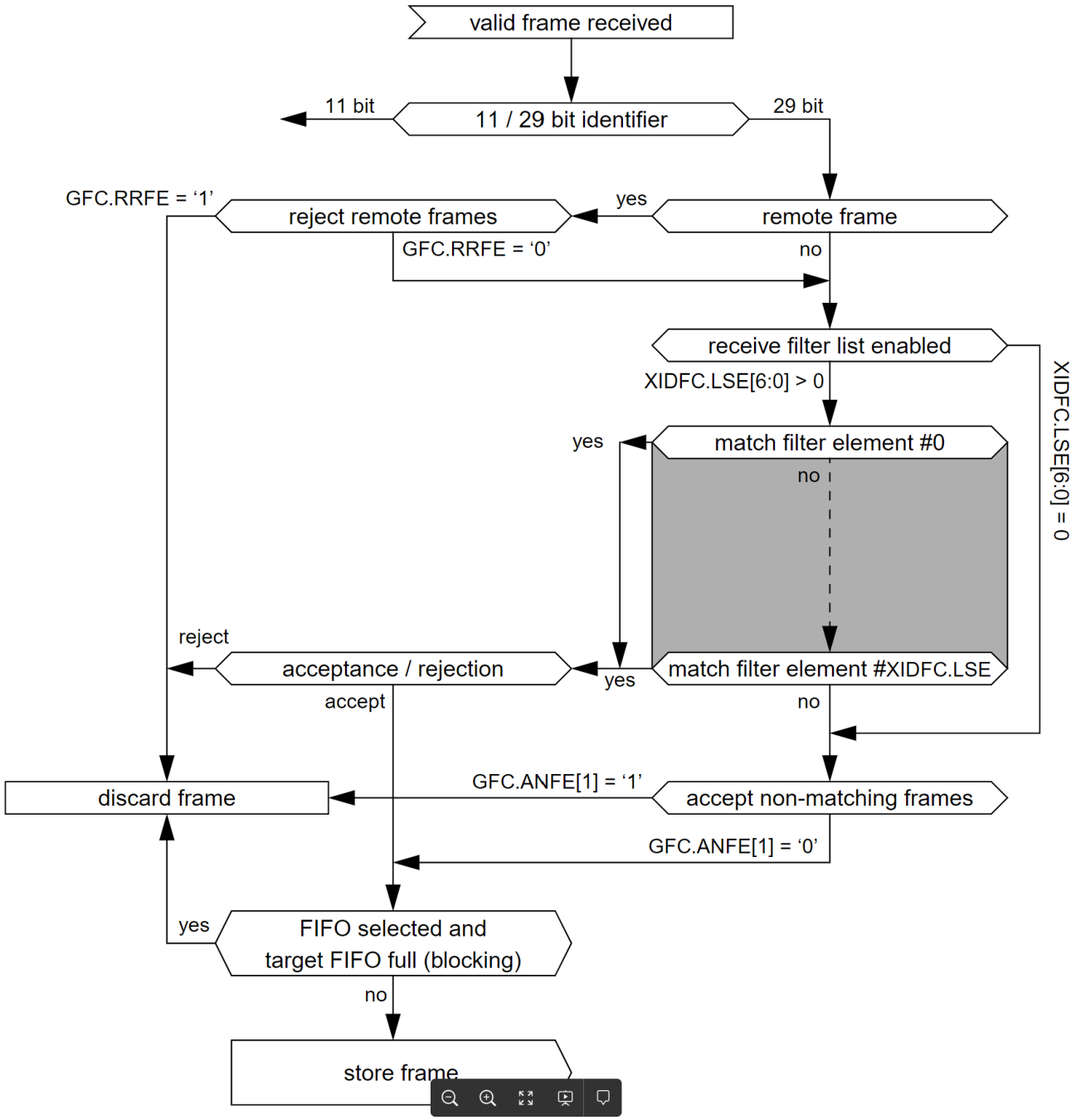


Figure 27-7. Extended Message ID Filter Path

27.4.4.2 Rx FIFOs

Rx FIFO 0 and Rx FIFO 1 can be configured to hold up to 64 elements each. Configuration of the two Rx FIFOs is done via registers RXF0C and RXF1C.

Received messages that passed acceptance filtering are transferred to the Rx FIFO as configured by the matching filter element. For a description of the filter mechanisms available for Rx FIFO 0 and Rx FIFO 1 see Section 3.4.1. The Rx FIFO element is described in Section 2.4.2.

To avoid an Rx FIFO overflow, the Rx FIFO watermark can be used. When the Rx FIFO fill level reaches the Rx FIFO watermark configured by RXFnC.FnWM, interrupt flag IR.RFnW is set. When the Rx FIFO Put Index reaches the Rx FIFO Get Index an Rx FIFO Full condition is signalled by RXFnS.FnF. In addition interrupt flag IR.RFnF is set.

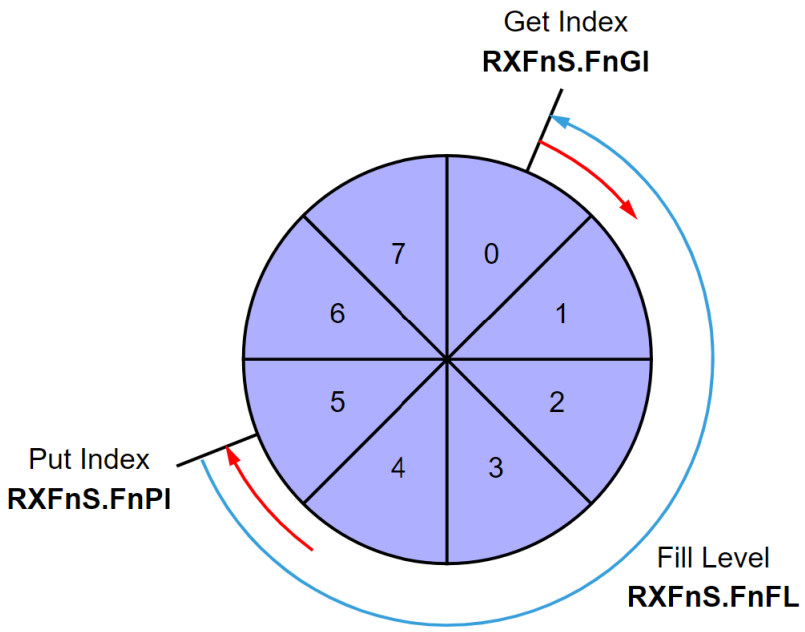


Figure 27-8. Rx FIFO Status

When reading from an Rx FIFO, Rx FIFO Get Index RXFnS.FnGI • FIFO Element Size has to be added to the corresponding Rx FIFO start address RXFnC.FnSA.

Table 27-2. Rx Buffer / FIFO Element Size

RXESC.RBDS[2:0] RXESC.FnDS[2:0]	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

27.4.4.2.1 Rx FIFO Blocking Mode

The Rx FIFO blocking mode is configured by RXFnC.FnOM = ‘0’. This is the default operation mode for the Rx FIFOs.

When an Rx FIFO full condition is reached (RXFnS.FnPI = RXFnS.FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signalled by RXFnS.FnF = '1'. In addition interrupt flag IR.RFnF is set.

In case a message is received while the corresponding Rx FIFO is full, this message is discarded and the message lost condition is signalled by RXFnS.RFnL = '1'. In addition interrupt flag IR.RFnL is set.

27.4.4.2.2 Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by RXFnC.FnOM = '1'.

When an Rx FIFO full condition (RXFnS.FnPI = RXFnS.FnGI) is signalled by RXFnS.FnF = '1', the next message accepted for the FIFO will overwrite the oldest FIFO message. Put and get index are both incremented by one.

When an Rx FIFO is operated in overwrite mode and an Rx FIFO full condition is signalled, reading of the Rx FIFO elements should start at least at get index + 1. The reason for that is, that it might happen, that a received message is written to the Message RAM (put index) while the CPU is reading from the Message RAM (get index). In this case inconsistent data may be read from the respective Rx FIFO element. Adding an offset to the get index when reading from the Rx FIFO avoids this problem. The offset depends on how fast the CPU accesses the Rx FIFO. Figure 9 shows an offset of two with respect to the get index when reading the Rx FIFO. In this case the two messages stored in element 1 and 2 are lost.

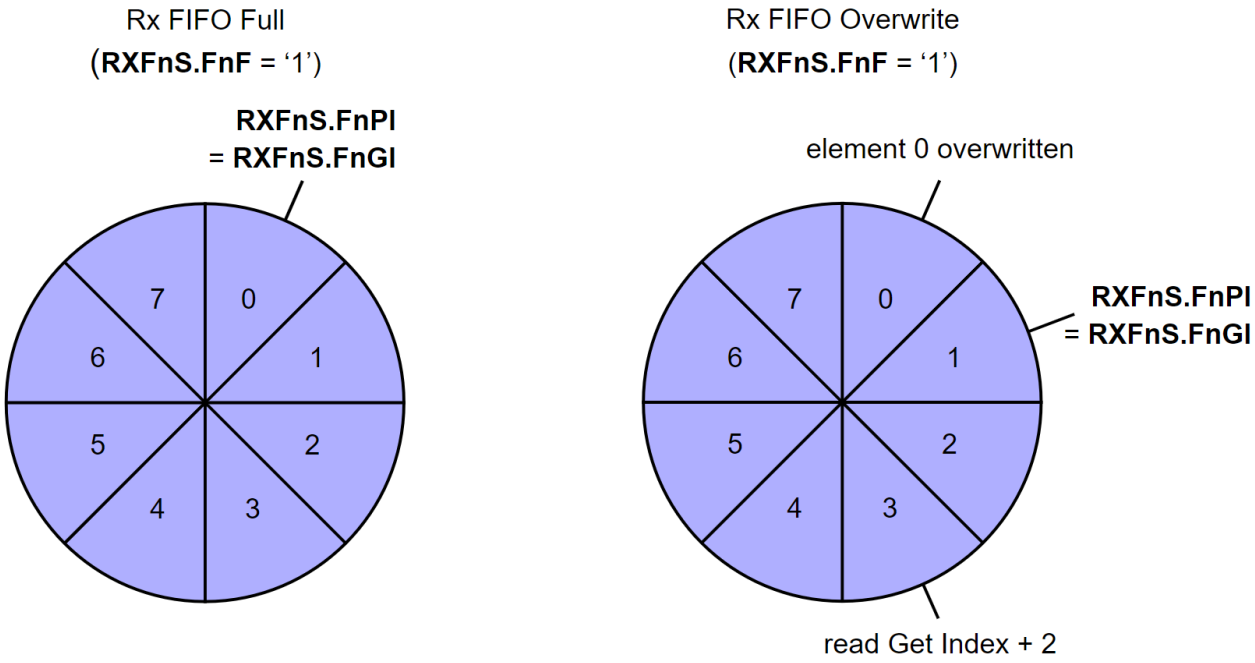


Figure 27-9. Rx FIFO Overflow Handling

After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index RXFnA.FnA. This increments the get index to that element number. In case the put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (RXFnS.FnF = '0').

27.4.4.3 Dedicated Rx Buffers

The M_CAN supports up to 64 dedicated Rx Buffers. The start address of the dedicated Rx Buffer section is configured via RXBC.RBSA.

For each Rx Buffer a Standard or Extended Message ID Filter Element with SFEC / EFEC = “111” and SFID2 / EFID2[10:9] = “00” has to be configured (see Section 2.4.5 and Section 2.4.6).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element. The format is the same as for an Rx FIFO element. In addition the flag IR.DRX (Message stored in Dedicated Rx Buffer) in the interrupt register is set.

Table 27-3. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register NDAT1,2 is set. As long as the New Data flag is set, the respective Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the Host by writing a ‘1’ to the respective bit position.

While an Rx Buffer’s New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements may cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message may be rejected, depending on filter configuration.

27.4.4.3.1 Rx Buffer Handling

- Reset interrupt flag IR.DRX
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

27.4.4.4 Debug on CAN Support

Debug messages are stored into Rx Buffers. For debug handling three consecutive Rx buffers (e.g. #61, #62, #63) have to be used for storage of debug messages A, B, and C. The format is the same as for an Rx Buffer or an Rx FIFO element (see M_CAN User’s Manual section 2.4.2).

Advantage: Fixed start address for the DMA transfers (relative to RXBC.RBSA), no additional configuration required.

For filtering of debug messages Standard / Extended Filter Elements with SFEC / EFEC = “111” have to be set up. Messages matching these filter elements are stored into the Rx Buffers addressed by SFID2 / EFID2[5:0].

After message C has been stored, the DMA request output m_can_dma_req is activated and the three messages can be read from the Message RAM under DMA control. The RAM words holding the debug messages will not be changed by the M_CAN while m_can_dma_req is activated. The behaviour is similar to that of an Rx Buffers with its New Data flag set.

After the DMA has completed the DMA unit sets m_can_dma_ack. This resets m_can_dma_req. Now the M_CAN is prepared to receive the next set of debug messages.

27.4.4.4.1 Filtering for Debug Messages

Filtering for debug messages is done by configuring one Standard / Extended Message ID Filter Element for each of the three debug messages. To enable a filter element to filter for debug messages SFEC / EFEC has to be programmed to “111”. In this case fields SFID1 / SFID2 and EFID1 / EFID2 have a different meaning (see Section 2.4.5 and Section 2.4.6). While SFID2 / EFID2[10:9] controls the debug message handling state machine, SFID2 / EFID2[5:0] controls the location for storage of a received debug message.

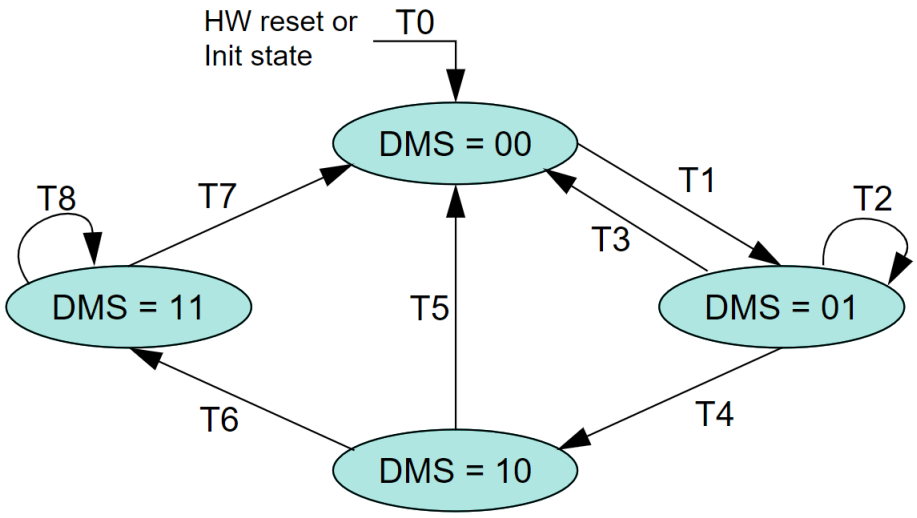
When a debug message is stored, neither the respective New Data flag nor IR.DRX are set. The reception of debug messages can be monitored via RXF1S.DMS.

Table 27-4. Example Filter Configuration for Debug Messages

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID debug message A	01	11 1101
1	ID debug message B	10	11 1110
2	ID debug message C	11	11 111

27.4.4.4.2 Debug Message Handling

The debug message handling state machine assures that debug messages are stored to three consecutive Rx Buffers in correct order. In case of missing messages the process is restarted. The DMArequest is activated only when all three debug messages A, B, C have been received in correct order.



T0: reset m_can_dma_req output, enable reception of debug messages A, B, and C

T1: reception of debug message A

T2: reception of debug message A

T3: reception of debug message C

T4: reception of debug message B

T5: reception of debug messages A, B

T6: reception of debug message C

T7: DMA transfer completed

T8: reception of debug message A,B,C (message rejected)

Figure 27-10. Debug Message Handling State Machine

27.4.5 Tx Handling

The Tx Handler handles transmission requests for the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue. It controls the transfer of transmit messages to the CAN Core, the Put and Get Indices, and the Tx Event FIFO. Up

to 32 Tx Buffers can be set up for message transmission. The CAN mode for transmission (Classic CAN or CAN FD) can be configured separately for each Tx Buffer element. The Tx Buffer element is described in Section 2.4.3. Table 58 below describes the possible configurations for frame transmission.

Table 27-5. Possible Configurations for Frame Transmission

CCCR		Tx Buffer Element		Frame Transmission
BRSE	FDOE	FDF	BRS	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	FD without bit rate switching
1	1	1	1	FD with bit rate switching

Note

AUTOSAR requires at least three Tx Queue Buffers and support of transmit cancellation.

The Tx Handler starts a Tx scan to check for the highest priority pending Tx request (Tx Buffer with lowest Message ID) when the Tx Buffer Request Pending register TXBRP is updated, or when a transmission has been started.

27.4.5.1 Transmit Pause

The transmit pause feature is intended for use in CAN systems where the CAN message identifiers are (permanently) specified to specific values and cannot easily be changed. These message identifiers may have a higher CAN arbitration priority than other defined messages, while in a specific application their relative arbitration priority should be inverse. This may lead to a case where one ECU sends a burst of CAN messages that cause another ECU's CAN messages to be delayed because that other messages have a lower CAN arbitration priority.

If e.g. CAN ECU-1 has the transmit pause feature enabled and is requested by its application software to transmit four messages, it will, after the first successful message transmission, wait for two CAN bit times of bus idle before it is allowed to start the next requested message. If there are other ECUs with pending messages, those messages are started in the idle time, they would not need to arbitrate with the next message of ECU-1. After having received a message, ECU-1 is allowed to start its next transmission as soon as the received message releases the CAN bus.

The transmit pause feature is controlled by bit CCCR.TXP. If the bit is set, the M_CAN will, each time it has successfully transmitted a message, pause for two CAN bit times before starting the next transmission. This enables other CAN nodes in the network to transmit messages even if their messages have lower prior identifiers. Default is transmit pause disabled (CCCR.TXP = '0').

This feature looses up burst transmissions coming from a single node and it protects against "babbling idiot" scenarios where the application program erroneously requests too many transmissions.

27.4.5.2 Dedicated Tx Buffers

Dedicated Tx Buffers are intended for message transmission under complete control of the Host CPU. Each Dedicated Tx Buffer is configured with a specific Message ID. In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

If the data section has been updated, a transmission is requested by an Add Request via TXBAR.ARn. The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

A Dedicated Tx Buffer allocates Element Size 32-bit words in the Message RAM (see Table 59). Therefore the start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index (0…31) • Element Size to the Tx Buffer Start Address TXBC.TBSA.

Table 27-6. Tx Buffer / FIFO / Queue Element Size

TXESC.TBDS[2:0]	Data Field [bytes]	Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

27.4.5.3 Tx FIFO

Tx FIFO operation is configured by programming TXBC.TFQM to ‘0’. Messages stored in the Tx FIFO are transmitted starting with the message referenced by the Get Index TXFQS.TFGI. After each transmission the Get Index is incremented cyclically until the Tx FIFO is empty. The Tx FIFO enables transmission of messages with the same Message ID from different Tx Buffers in the order these messages have been written to the Tx FIFO. The M_CAN calculates the Tx FIFO Free Level TXFQS.TFFL as difference between Get and Put Index. It indicates the number of available (free) Tx FIFO elements.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index TXFQS.TFQPI. An Add Request increments the Put Index to the next free Tx FIFO element. When the Put Index reaches the Get Index, Tx FIFO Full (TXFQS.TFQF = ‘1’) is signalled. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

When a single message is added to the Tx FIFO, the transmission is requested by writing a ‘1’ to the TXBAR bit related to the Tx Buffer referenced by the Tx FIFO’s Put Index.

When multiple (n) messages are added to the Tx FIFO, they are written to n consecutive Tx Buffers starting with the Put Index. The transmissions are then requested via TXBAR. The Put Index is then cyclically incremented by n. The number of requested Tx buffers should not exceed the number of free Tx Buffers as indicated by the Tx FIFO Free Level.

When a transmission request for the Tx Buffer referenced by the Get Index is cancelled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level is recalculated. When transmission cancellation is applied to any other Tx Buffer, the Get Index and the FIFO Free Level remain unchanged.

ATx FIFO element allocates Element Size 32-bit words in the Message RAM (see Table 59). Therefore the start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI (0…31) • Element Size to the Tx Buffer Start Address TXBC.TBSA.

27.4.5.4 Tx Queue

Tx Queue operation is configured by programming TXBC.TFQM to ‘1’. Messages stored in the Tx Queue are transmitted starting with the message with the lowest Message ID (highest priority). In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New messages have to be written to the Tx Buffer referenced by the Put Index TXFQS.TFQPI. A n Add Request cyclically increments the Put Index to the next free Tx Buffer. In case that the Tx Queue is full (TXFQS.TFQF

= ’1’), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been cancelled.

The application may use register TXBRP instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

ATx Queue Buffer allocates Element Size 32-bit words in the Message RAM (see Table 59). Therefore the start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI (0…31) • Element Size to the Tx Buffer Start Address TXBC.TBSA.

27.4.5.5 Mixed Dedicated Tx Buffers / Tx FIFO

In this case the Tx Buffers section in the Message RAM is subdivided into a set of Dedicated Tx Buffers and a Tx FIFO. The number of Dedicated Tx Buffers is configured by TXBC.NDTB. The number of Tx Buffers assigned to the Tx FIFO is configured by TXBC.TFQS. In case TXBC.TFQS is programmed to zero, only Dedicated Tx Buffers are used.

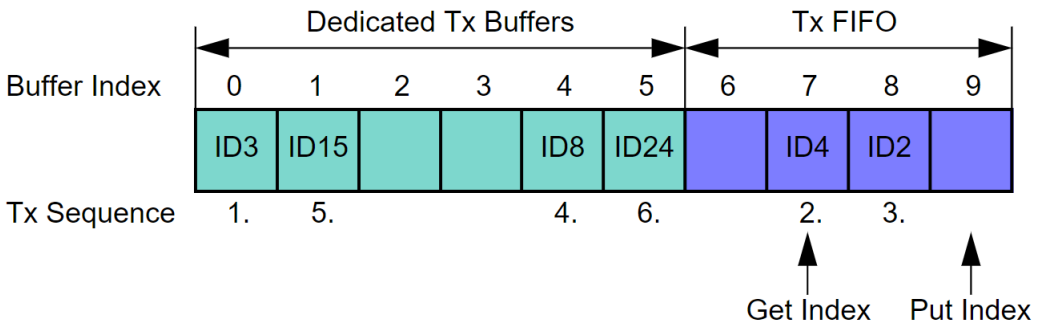


Figure 27-11. Example of mixed Configuration Dedicated Tx Buffers / Tx FIFO

Tx prioritization:

- Scan Dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by TXFS.TFGI)
- Buffer with lowest Message ID gets highest priority and is transmitted next

27.4.5.6 Mixed Dedicated Tx Buffers / Tx Queue

In this case the Tx Buffers section in the Message RAM is subdivided into a set of Dedicated Tx Buffers and a Tx Queue. The number of Dedicated Tx Buffers is configured by TXBC.NDTB. The number of Tx Queue Buffers is configured by TXBC.TFQS. In case TXBC.TFQS is programmed to zero, only Dedicated Tx Buffers are used.

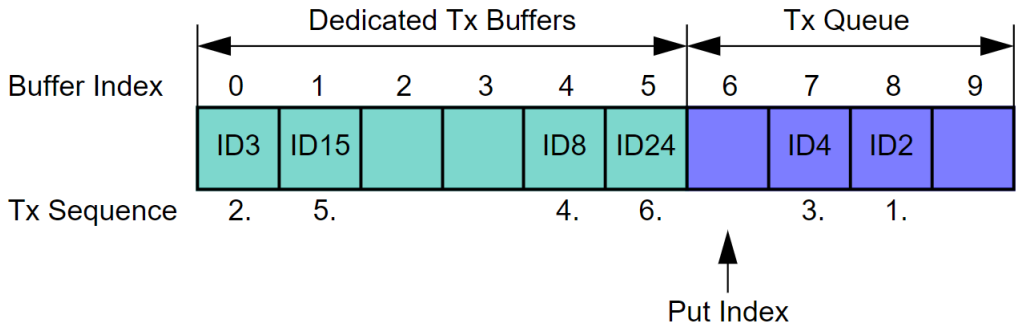


Figure 27-12. Example of mixed Configuration Dedicated Tx Buffers / Tx Queue

Tx prioritization:

- Scan all Tx Buffers with activated transmission request
- Tx Buffer with lowest Message ID gets highest priority and is transmitted next

27.4.5.7 Transmit Cancellation

The M_CAN supports transmit cancellation. This feature is especially intended for gateway applications and AUTOSAR based applications. To cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer the Host has to write a '1' to the corresponding bit position (=number of Tx Buffer) of register TXBCR. Transmit cancellation is not intended for Tx FIFO operation.

Successful cancellation is signalled by setting the corresponding bit of register TXBCF to '1'.

In case a transmit cancellation is requested while a transmission from a Tx Buffer is already ongoing, the corresponding TXBRP bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding TXBTO and TXBCF bits are set. If the transmission was not successful, it is not repeated and only the corresponding TXBCF bit is set.

Note

In case a pending transmission is cancelled immediately before this transmission could have been started, there follows a short time window where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message which may have a lower priority than the second message in this node.

27.4.5.8 Tx Event Handling

To support Tx event handling the M_CAN has implemented a Tx Event FIFO. After the M_CAN has transmitted a message on the CAN bus, Message ID and timestamp are stored in a Tx Event FIFO element. To link a Tx event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

The Tx Event FIFO can be configured to a maximum of 32 elements. The Tx Event FIFO element is described in Section 2.4.4.

The purpose of the Tx Event FIFO is to decouple handling transmit status information from transmit message handling i.e. a Tx Buffer holds only the message to be transmitted, while the transmit status is stored separately in the Tx Event FIFO. This has the advantage, especially when operating a dynamically managed transmit queue, that a Tx Buffer can be used for a new message immediately after successful transmission. There is no need to save transmit status information from a Tx Buffer before overwriting that Tx Buffer.

When a Tx Event FIFO full condition is signalled by IR.TEFF, no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented. In case a Tx event occurs while the Tx Event FIFO is full, this event is discarded and interrupt flag IR.TEFL is set.

To avoid a Tx Event FIFO overflow, the Tx Event FIFO watermark can be used. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by TXEFC.EFWM, interrupt flag IR.TEFW is set.

When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index TXEFS.EFGI has to be added to the Tx Event FIFO start address TXEFC.EFSA.

27.4.6 FIFO Acknowledge Handling

The Get Indices of Rx FIFO 0, Rx FIFO 1, and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (see Section 2.3.29, Section 2.3.33, and Section 2.3.47). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level. There are two use cases:

When only a single element has been read from the FIFO (the one being pointed to by the Get Index), this Get Index value is written to the FIFO Acknowledge Index.

When a sequence of elements has been read from the FIFO, it is sufficient to write the FIFO Acknowledge Index only once at the end of that read sequence (value: Index of the last element read), to update the FIFO's Get Index.

Due to the fact that the CPU has free access to the M_CAN's Message RAM, special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This might be useful when reading a High Priority Message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also alters the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

Note

The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The M_CAN does not check for erroneous values.

27.4.7 MCAN Message RAM

For storage of Rx/Tx messages and for storage of the filter configuration a single- or dual-ported Message RAM has to be connected to the M_CAN module.

Note

In case the MessageRAMis equipped with parity or ECC functionality, it is recommended to initialize the Message RAM after hardware reset by writing e.g. 0x00000000 to each Message RAM word to create valid parity/ECC checksums. This avoids that reading from uninitialized Message RAM sections will activate interrupt IR.BEC (Bit Error Corrected) or IR.BEU (Bit Error Uncorrected).

27.4.7.1 Message RAM Configuration

The Message RAM has a width of 32 bits. In case parity checking or ECC is used a respective number of bits has to be added to each word. The M_CAN module can be configured to allocate up to 4352 words in the Message RAM. It is not necessary to configure each of the sections listed in Figure below, nor is there any restriction with respect to the sequence of the sections.

When operated in CAN FD mode the required Message RAM size strongly depends on the element size configured for Rx FIFO0, Rx FIFO1, Rx Buffers, and Tx Buffers via RXESC.F0DS, RXESC.F1DS, RXESC.RBDS, and TXESC.TBDS.

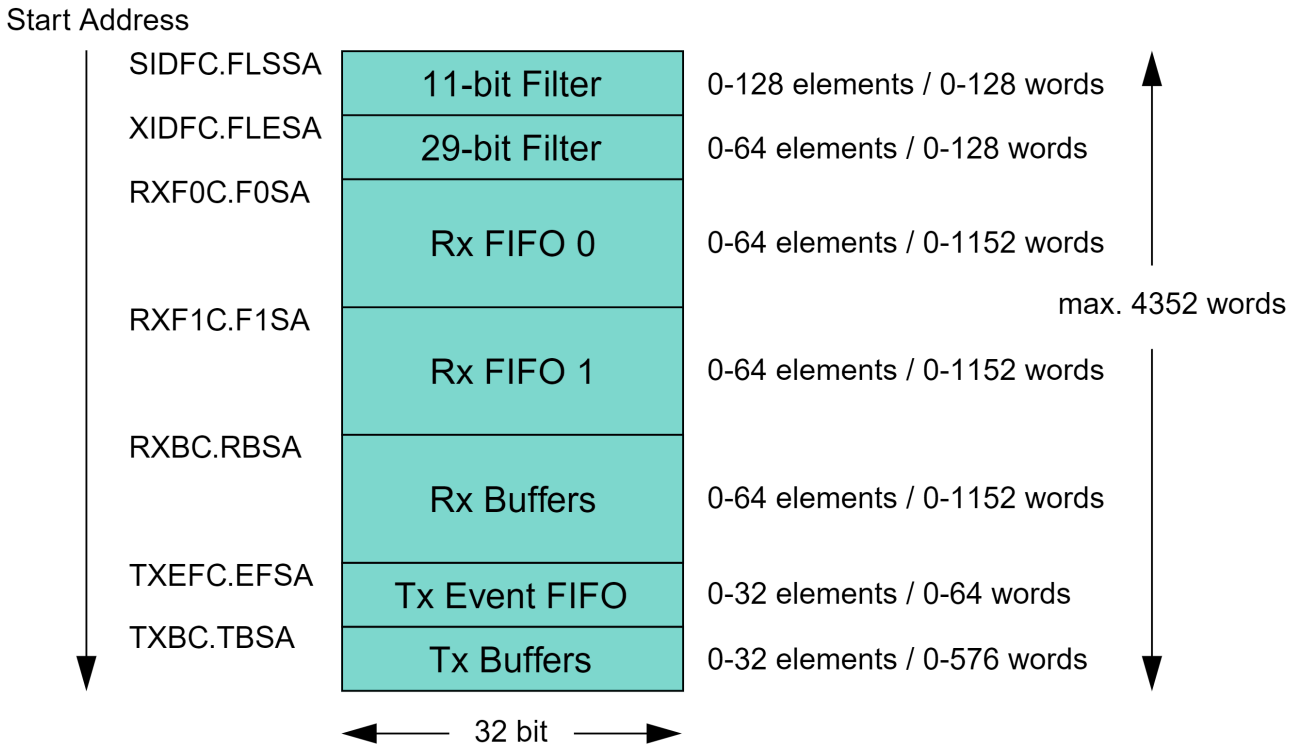


Figure 27-13. MCAN_Message_RAM_Configuration

When the M_CAN addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored.

Note

The M_CAN does not check for erroneous configuration of the Message RAM. Especially the configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully to avoid falsification or loss of data.

27.4.7.2 Rx Buffer and FIFO Element

Up to 64 Rx Buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The structure of a Rx Buffer / FIFO element is shown in Table 49 below. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via register RXESC.

Table 27-7. Rx Buffer and FIFO Element

Rx Buffer/FIFO	Bit	Name	Description
R0	31	ESI	Error State Indicator 0= Transmitting node is error active 0= Transmitting node is error active
	30	XTD	Extended Identifier Signals to the Host whether the received frame has a standard or extended identifier. 0= 11-bit standard identifier 1= 29-bit extended identifier
	29	RTR	Remote Transmission Request Signals to the Host whether the received frame is a data frame or a remote frame. 0= Received frame is a data frame 1= Received frame is a remote frame Note: There are no remote frames in CAN FD format. In CAN FD frames (FDF = 1'), the dominant RRS (Remote Request Substitution) bit replaces bit RTR (Remote Transmission Request).
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on bit XTD. Astandard identifier is stored into ID[28:18].
R1	31	ANMF	Accepted Non-matching Frame Acceptance of non-matching frames may be enabled via GFC.ANFS and GFC.ANFE. 0= Received frame matching filter index FIDX 1= Received frame did not match any Rx filter element
	30:24	FIDX[6:0]	Filter Index 0-127=Index of matching Rx acceptance filter element (invalid if ANMF = '1'). Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
	21	FDF	FD Format 0= Standard frame format 1= CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch 0= Frame received without bit rate switching 1= Frame received with bit rate switching
	19:16	DLC[3:0]	Data Length Code 0-8= CAN + CAN FD: received frame has 0-8 data bytes 9-15= CAN: received frame has 8 data bytes 9-15= CAN FD: received frame has 12/16/20/24/32/48/64 data bytes
	15:0	RXTS[15:0]	Rx Timestamp Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP.
R2	31:24	DB3[7:0]	Data Byte 3
	23:16	DB2[7:0]	Data Byte 2
	15:8	DB1[7:0]	Data Byte 1
	7:0	DB0[7:0]	Data Byte 0

Table 27-7. Rx Buffer and FIFO Element (continued)

Rx Buffer/FIFO	Bit	Name	Description
R3	31:24	DB7[7:0]	Data Byte 7
	23:16	DB6[7:0]	Data Byte 6
	15:8	DB5[7:0]	Data Byte 5
	7:0	DB4[7:0]	Data Byte 4
...	...	...	...
Rn	31:24	DBm[7:0]	Data Byte m
	23:16	DBm-1[7:0]	Data Byte m-1
	15:8	DBm-2[7:0]	Data Byte m-2
	7:0	DBm-3[7:0]	Data Byte m-3

Note

Depending on the configuration of the element size (RXESC), between two and sixteen 32-bit words (Rn = 3 ..17) are used for storage of a CAN message's data field.

27.4.7.3 Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO / Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO / Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler distinguishes between dedicated Tx Buffers and Tx FIFO / Tx Queue by evaluating the Tx Buffer configuration TXBC.TFQS and TXBC.NDTB. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via register TXESC.

Table 27-8. Tx Buffer Element

Tx Buffer	Bit	Name	Description
T0	31	ESI	Error State Indicator 0= ESI bit in CAN FD format depends only on error passive flag 1= ESI bit in CAN FD format transmitted recessive Note: The ESI bit of the transmit buffer is or'ed with the error passive flag to decide the value of the ESI bit in the transmitted FD frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the ESI bit recessive, but an error passive node will always transmit the ESI bit recessive
	30	TXD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier
	29	RTR	Remote Transmission Request 0= Transmit data frame 1= Transmit remote frame Note: WhenRTR = 1, the M_CAN transmits a remote frame according to ISO 11898-1:2015, even if CCCR.FDOE enables the transmission in CAN FD format.
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on bit XTD. Astandard identifier has to be written to ID[28:18].

Table 27-8. Tx Buffer Element (continued)

Tx Buffer	Bit	Name	Description
T1	31:24	MM[7:0]	Message Marker Written by CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status.
	23	EFC	Event FIFO Control 0= Don't store Tx events 1= Store Tx events
	21	FDF	FD Format 0= Frame transmitted in Classic CAN format 1= Frame transmitted in CAN FD format
	20	BRS	Bit Rat Switching 0= CAN FD frames transmitted without bit rate switching 1= CAN FD frames transmitted with bit rate switching Note: Bits ESI, FDF, and BRS are only evaluated when CAN FD operation is enabled CCCR.FDOE = 1'. Bit BRS is only evaluated when in addition CCCR.BRSE = '1'.
	19:16	DLC[3:0]	Data Length Code 0-8= CAN + CAN FD: transmit frame has 0-8 data bytes 9-15= CAN: transmit frame has 8 data bytes 9-15= CAN FD: transmit frame has 12/16/20/24/32/48/64 data bytes
T2	31:24	DB3[7:0]	Data Byte 3
	23:16	DB2[7:0]	Data Byte 2
	15:8	DB1[7:0]	Data Byte 1
	7:0	DB0[7:0]	Data Byte 0
T3	31:24	DB7[7:0]	Data Byte 7
	23:16	DB6[7:0]	Data Byte 6
	15:8	DB5[7:0]	Data Byte 5
	7:0	DB4[7:0]	Data Byte 4
...	...	...	...
Tn	31:24	DBm[7:0]	Data Byte m
	23:16	DBm-1[7:0]	Data Byte m-1
	15:8	DBm-2[7:0]	Data Byte m-2
	7:0	DBm-3[7:0]	Data Byte m-3

Note

Depending on the configuration of the element size (TXESC), between two and sixteen 32-bit words (Tn = 3 ..17) are used for storage of a CAN message's data field.

27.4.7.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from register TXEFS.

Table 27-9. Tx Event FIFO Element

Tx Event	Bit	Name	Description
E0	31	ESI	Error State Indicator 0= Transmitting node is error active 1= Transmitting node is error passive
	30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier
	29	RTR	Remote Transmission Request 0= Data frame transmitted 1= Remote frame transmitted
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on bit XTD. Astandard identifier is stored into ID[28:18].
E1	31:24	MM[7:0]	Message Marker Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status.
	23:22	ET[1:0]	Event Type 00= Reserved 01= Tx event 10= Transmission in spite of cancellation (always set for transmissions in DAR mode) 11= Reserved
	21	FDF	FD Format 0= Standard frame format 1= CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch 0= Frame transmitted without bit rate switching 1= Frame transmitted with bit rate switching
	19:16	DLC[3:0]	Data Length Code 0-8= CAN + CAN FD: frame with 0-8 data bytes transmitted 9-15= CAN: frame with 8 data bytes transmitted 9-15= CAN FD: frame with 12/16/20/24/32/48/64 data bytes transmitted
	15:0	TXTS[15:0]	Tx Timestamp Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP.

27.4.7.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address SIDFC.FLSSA plus the index of the filter element (0…127).

Table 27-10. Standard Message ID Filter Element

Standard Message	Bit	Name	Description
S0	31:30	SFT[1:0]	Standard Filter Type 00= Range filter from SFID1 to SFID2 (SFID2 ≥ SFID1) 01= Dual ID filter for SFID1 or SFID2 10= Classic filter: SFID1 = filter, SFID2 = mask 11= Filter element disabled Note: With SFT = “11” the filter element is disabled and the acceptance filtering continues (same behaviour as with SFEC = “000”)
	29:27	SFEC[2:0]	Standard Filter Element Configuration All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match. 000= Disable filter element 001= Store in Rx FIFO 0 if filter matches 010= Store in Rx FIFO 1 if filter matches 011= Reject ID if filter matches 100= Set priority if filter matches 101= Set priority and store in FIFO 0 if filter matches 110= Set priority and store in FIFO 1 if filter matches 111= Store into Rx Buffer or as debug message, configuration of SFT[1:0] ignored
	26:16	SFID1[10:0]	Standard Filter ID 1 First ID of standard ID filter element. When filtering for Rx Buffers or for debug messages this field defines the ID of a standard message to be stored. The received identifiers must match exactly, no masking mechanism is used.
	10:0	SFID2[10:0]	Standard Filter ID 2 This bit field has a different meaning depending on the configuration of SFEC: 1) SFEC = “001”...”110” Second ID of standard ID filter element 2) SFEC = “111” Filter for Rx Buffers or for debug messages SFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. 00= Store message into an Rx Buffer 01= Debug Message A 10= Debug Message B 11= Debug Message C SFID2[8:6] is used to control the filter event pins m_can_fe[2:0] at the Extension Interface. Aone at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one m_can_hclk period in case the filter matches. SFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

27.4.7.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address XIDFC.FLESA plus two times the index of the filter element (0…63).

Table 27-11. Extended Message ID Filter Element

Filter Element	Bit	Name	Description
F0	31:29	EFEC[2:0]	Extended Filter Element Configuration All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match. 000= Disable filter element 001= Store in Rx FIFO 0 if filter matches 010= Store in Rx FIFO 1 if filter matches 011= Reject ID if filter matches 100= Set priority if filter matches 101= Set priority and store in FIFO 0 if filter matches 110= Set priority and store in FIFO 1 if filter matches 111= Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored
	28:0	EFID1[28:0]	Extended Filter ID 1 First ID of extended ID filter element. When filtering for Rx Buffers or for debug messages this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism (see Section 3.4.1.5, Extended Message ID Filtering) is used.
F1	31:30	EFT[1:0]	Extended Filter Type 00= Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) 01= Dual ID filter for EFID1 or EFID2 10= Classic filter: EFID1 = filter, EFID2 = mask 11= Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), XIDAM mask not applied
	28:0	EFID2[28:0]	Extended Filter ID 2 This bit field has a different meaning depending on the configuration of EFEC: 1) EFEC = “001”...”110” Second ID of extended ID filter element 2) EFEC = “111” Filter for Rx Buffers or for debug messages EFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. 00= Store message into an Rx Buffer 01= Debug Message A 10= Debug Message B 11= Debug Message C EFID2[8:6] is used to control the filter event pins m_can_fe[2:0] at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one m_can_hclk period in case the filter matches. EFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA for storage of a matching message.

27.4.8 Interrupt Requests

The MCAN module provides interrupt and DMA requests. They are configured via the Host CPU. The Suspend Mode is requesting or forcing (based on MCANSS_CTRL[3] DBGSUSP_FREE bit) the MCAN module to go into initialization mode (see MCAN_CCCR[0] INIT bit) in which new interrupts and DMA requests will not be issued, that is to prevents the interrupt and DMA requests from propagating to the Host CPU.

The MCAN module has two interrupt lines. There are 30 internal interrupt sources. Each source can be configured to drive one of the two interrupt lines. The interrupts are 'level high' interrupts.

The MCAN core provides two interrupt requests (for Line 0 and Line 1). For more information, see the following registers:

- Interrupt Register (MCAN_IR)
- Interrupt Enable (MCAN_IE)
- Interrupt Line Select (MCAN_ILS)
- Interrupt Line Enable (MCAN_ILE)

To clear IRQ_INT0, IRQ_INT1 and TS_WAKE interrupts, write to the EOI bit field for the corresponding interrupt number that is described in the MCANSS_EOI register.

The MCAN module is capable of issuing ECC interrupts. After clearing the ECC interrupt source, the application software must also write 1 to EOI register (MCANSS_ECC_SEC_EOI_REG/MCANSS_ECC_DED_EOI_REG). For more information, see *ECC Aggregator*.

The MCAN module supports External Timestamp Counter. When the External Timestamp Counter rolls over it produces an interrupt (see *External Timestamp Counter*). For more information, see the following registers:

- Interrupt Clear Shadow Register (MCANSS_ICS)
- Interrupt Raw Status Register (MCANSS_IRS)
- Interrupt Enable Clear Shadow Register (MCANSS_IECS)
- Interrupt Enable Register (MCANSS_IE)
- Interrupt Enable Status Register (MCANSS_IES)
- End Of Interrupt Register (MCANSS_EOI)
- External Timestamp Prescaler Register (MCANSS_EXT_TS_PRESCALER)
- External Timestamp Unserviced Interrupts Counter Register (MCANSS_EXT_TS_UNSERVICED_INTR_CNTR)

27.5 CC27xx MCAN Wrapper

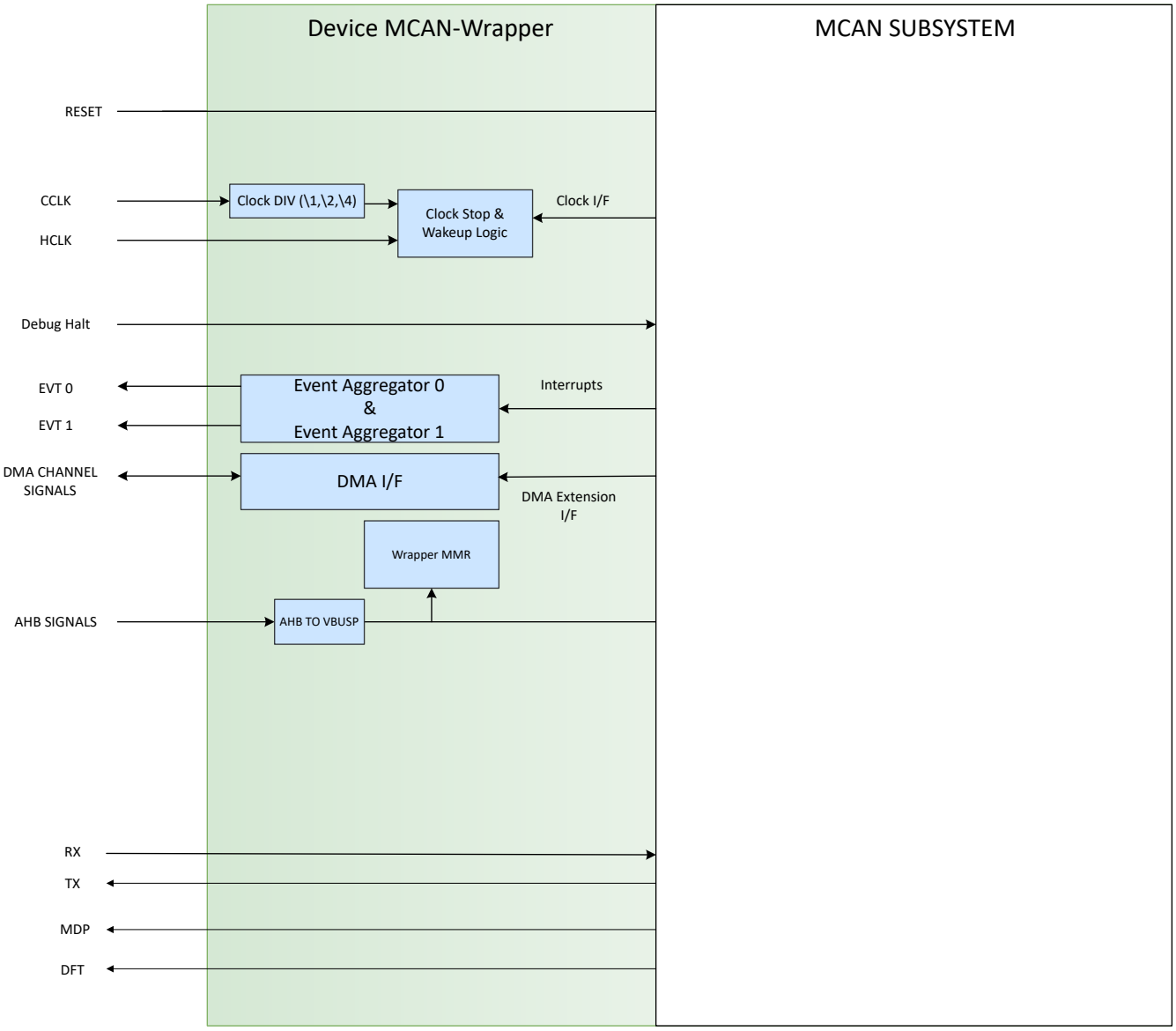


Figure 27-14. MCAN Wrapper

27.6 MCAN clock enable

- HMCAN and HCANOPT[1:0] bits are defined in CLKCTRL HWOPT1 register.
- MCAN bit is defined in CLKCTRL CLKCFG register. MCAN bit needs to be programmed by user application to enable the MCAN module.
- When HMCAN bit is 1, the clock enable signal will be asserted when MCAN bit is set in the CLKCFG register.
- When HMCAN bit is set to 0, the clock enable signal will be permanently de-asserted and the MCAN bit in CLKCFG register will always read 0.
- When the clock enable input is low, HCLK is gated to MMRs and RAM and CCLK is gated to MCAN core.
- When the clock enable and HCANOPT[1] are high, HCLK is ungated to MMRs and RAM and CCLK is also ungated to MCAN core.
- When the clock enable is high and HCANOPT[1] is low, HCLK is ungated only to RAM while HCLK to MMRs is gated. CCLK is also gated to MCAN core.
- AFOSC and HFOSC can both be used as CAN functional clock. For better accuracy use AFOSC. Refer to Section 6.6.3.2 and Section 6.6.4.2 for further details.

Clock enable	HCANOPT[1]	Behavior
0	X	HCLK gated to MMRs HCLK gated to CANRAM CCLK gated to MCAN core
1	1	HCLK running to MMRs HCLK running to CANRAM CCLK running to CAN core
1	0	HCLK gated to MMRs HCLK running to CANRAM CCLK gated to CAN core

27.7 Additional notes

MCAN RAM ECC errors:

- The correctable and uncorrectable ECC error flags for CAN message RAM are available in the MCAN wrapper interrupt registers. They can be unmasked to trigger SEC or DED interrupt to CPU.
- The uncorrectable ECC error is also captured in the interrupt registers of Bosch CAN controller but the correctable ECC error is available only in the CC27XX MCAN wrapper interrupt registers. It is possible for application to either unmask the ECC uncorrectable interrupt flag in the Bosch CAN controller or in the CC27XX MCAN wrapper to service it.
- When the uncorrectable ECC error is triggered the Tx/Rx operation is disabled by the Bosch CAN IP after handling the ECC uncorrectable error condition.

Accessing MCAN ERR registers:

- This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

  Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the MCANERR_VECTOR.ECC_VECTOR field, together with the MCANERR_VECTOR.RD_SVBUS trigger and MCANERR_VECTOR.RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the MCANERR_VECTOR.RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address.
- MCANSS_IES provides the masked interrupt status. It is the logical AND of IRS and IE for the respective bits.

MCAN RAM initialization:

- MCAN RAM goes through hardware-based auto initialization sequence whenever SVT domain reset is released in scenarios like device cold powerup, chip reset or standby/shutdown wake.
- There is a status bit MEM_INIT_DONE in MCANSS_STAT register that needs to be polled or checked by application software before performing any read or writes to MCAN message RAM.
- If this recommendation is violated, then writes to MCAN RAM will be ignored and reads will provide unpredictable data. Design note: Read in such case returns value on the internal read data path which can be 0 or last read value from any of the MMRs.

MCAN ECC implementation:

- ECC SECDED is implemented only for the CAN 4KB message RAM. It is not available for the TX DMA BRP. Though the NUM_RAMS value is set to 2 in MCANERR_STAT register it is only the CAN message RAM that is considered for ECC functionality and diagnostics.
- The TX DMA BRP specific bit has been removed from MCANERR_DED_STATUS, MCANERR_DED_ENABLE_SET and MCANERR_DED_ENABLE_CLR registers.

27.8 CANFD Registers

Table 27-12 lists the memory-mapped registers for the CANFD registers. All register offset addresses not listed in Table 27-12 should be considered as reserved locations and the register contents should not be modified.

Table 27-12. CANFD Registers

Offset	Acronym	Register Name	Section
0h	MCAN_CREL	MCAN Core Release Register	Section 27.8.1
4h	MCAN_ENDN	MCAN Endian Register	Section 27.8.2
Ch	MCAN_DBTP	MCAN Data Bit Timing and Prescaler Register	Section 27.8.3
10h	MCAN_TEST	MCAN Test Register	Section 27.8.4
14h	MCAN_RWD	MCAN RAM Watchdog	Section 27.8.5
18h	MCAN_CCCR	MCAN CC Control Register	Section 27.8.6
1Ch	MCAN_NBTP	MCAN Nominal Bit Timing and Prescaler Register	Section 27.8.7
20h	MCAN_TSCC	MCAN Timestamp Counter Configuration	Section 27.8.8
24h	MCAN_TSCV	MCAN Timestamp Counter Value	Section 27.8.9
28h	MCAN_TOCC	MCAN Timeout Counter Configuration	Section 27.8.10
2Ch	MCAN_TOCV	MCAN Timeout Counter Value	Section 27.8.11
40h	MCAN_ECR	MCAN Error Counter Register	Section 27.8.12
44h	MCAN_PSR	MCAN Protocol Status Register	Section 27.8.13
48h	MCAN_TDCR	MCAN Transmitter Delay Compensation Register	Section 27.8.14
50h	MCAN_IR	MCAN Interrupt Register	Section 27.8.15
54h	MCAN_IE	MCAN Interrupt Enable	Section 27.8.16
58h	MCAN_ILS	MCAN Interrupt Line Select	Section 27.8.17
5Ch	MCAN_ILE	MCAN Interrupt Line Enable	Section 27.8.18
80h	MCAN_GFC	MCAN Global Filter Configuration	Section 27.8.19
84h	MCAN_SIDFC	MCAN Standard ID Filter Configuration	Section 27.8.20
88h	MCAN_XIDFC	MCAN Extended ID Filter Configuration	Section 27.8.21
90h	MCAN_XIDAM	MCAN Extended ID and Mask	Section 27.8.22
94h	MCAN_HPMS	MCAN High Priority Message Status	Section 27.8.23
98h	MCAN_NDAT1	MCAN New Data 1	Section 27.8.24
9Ch	MCAN_NDAT2	MCAN New Data 2	Section 27.8.25
A0h	MCAN_RXF0C	MCAN Rx FIFO 0 Configuration	Section 27.8.26
A4h	MCAN_RXF0S	MCAN Rx FIFO 0 Status	Section 27.8.27
A8h	MCAN_RXF0A	MCAN Rx FIFO 0 Acknowledge	Section 27.8.28
ACh	MCAN_RXBC	MCAN Rx Buffer Configuration	Section 27.8.29
B0h	MCAN_RXF1C	MCAN Rx FIFO 1 Configuration	Section 27.8.30
B4h	MCAN_RXF1S	MCAN Rx FIFO 1 Status	Section 27.8.31
B8h	MCAN_RXF1A	MCAN Rx FIFO 1 Acknowledge	Section 27.8.32
BCh	MCAN_RXESC	MCAN Rx Buffer / FIFO Element Size Configuration	Section 27.8.33
C0h	MCAN_TXBC	MCAN Tx Buffer Configuration	Section 27.8.34
C4h	MCAN_TXFQS	MCAN Tx FIFO / Queue Status	Section 27.8.35
C8h	MCAN_TXESC	MCAN Tx Buffer Element Size Configuration	Section 27.8.36
CCh	MCAN_TXBRP	MCAN Tx Buffer Request Pending	Section 27.8.37
D0h	MCAN_TXBAR	MCAN Tx Buffer Add Request	Section 27.8.38
D4h	MCAN_TXBCR	MCAN Tx Buffer Cancellation Request	Section 27.8.39
D8h	MCAN_TXBTO	MCAN Tx Buffer Transmission Occurred	Section 27.8.40
DCh	MCAN_TXBCF	MCAN Tx Buffer Cancellation Finished	Section 27.8.41

Table 27-12. CANFD Registers (continued)

Offset	Acronym	Register Name	Section
E0h	MCAN_TXBTIE	MCAN Tx Buffer Transmission Interrupt Enable	Section 27.8.42
E4h	MCAN_TXBCIE	MCAN Tx Buffer Cancellation Finished Interrupt Enable	Section 27.8.43
F0h	MCAN_TXEFC	MCAN Tx Event FIFO Configuration	Section 27.8.44
F4h	MCAN_TXEFS	MCAN Tx Event FIFO Status	Section 27.8.45
F8h	MCAN_TXEFA	MCAN Tx Event FIFO Acknowledge	Section 27.8.46
200h	MCANSS_PID	MCAN Subsystem Revision Register	Section 27.8.47
204h	MCANSS_CTRL	MCAN Subsystem Control Register	Section 27.8.48
208h	MCANSS_STAT	MCAN Subsystem Status Register	Section 27.8.49
20Ch	MCANSS_ICS	MCAN Subsystem Interrupt Clear Shadow Register	Section 27.8.50
210h	MCANSS_IRS	MCAN Subsystem Interrupt Raw Satus Register	Section 27.8.51
214h	MCANSS_IECS	MCAN Subsystem Interrupt Enable Clear Shadow Register	Section 27.8.52
218h	MCANSS_IE	MCAN Subsystem Interrupt Enable Register	Section 27.8.53
21Ch	MCANSS_IES	MCAN Subsystem Masked Interrupt Status	Section 27.8.54
220h	MCANSS_EOI	MCAN Subsystem End of Interrupt	Section 27.8.55
224h	MCANSS_EXT_TS_PRESCALER	MCAN Subsystem External Timestamp Prescaler 0	Section 27.8.56
228h	MCANSS_EXT_TS_UNSERVICED_INTR_CNTR	MCAN Subsystem External Timestamp Unserviced Interrupts Counter	Section 27.8.57
400h	MCANERR_REV	MCAN Error Aggregator Revision Register	Section 27.8.58
408h	MCANERR_VECTOR	MCAN ECC Vector Register	Section 27.8.59
40Ch	MCANERR_STAT	MCAN Error Misc Status	Section 27.8.60
410h	MCANERR_WRAP_REV	MCAN ECC Wrapper Revision Register	Section 27.8.61
414h	MCANERR_CTRL	MCAN ECC Control	Section 27.8.62
418h	MCANERR_ERR_CTRL1	MCAN ECC Error Control 1 Register	Section 27.8.63
41Ch	MCANERR_ERR_CTRL2	MCAN ECC Error Control 2 Register	Section 27.8.64
420h	MCANERR_ERR_STAT1	MCAN ECC Error Status 1 Register	Section 27.8.65
424h	MCANERR_ERR_STAT2	MCAN ECC Error Status 2 Register	Section 27.8.66
428h	MCANERR_ERR_STAT3	MCAN ECC Error Status 3 Register	Section 27.8.67
43Ch	MCANERR_SEC_EOI	MCAN Single Error Corrected End of Interrupt Register	Section 27.8.68
440h	MCANERR_SEC_STATUS	MCAN Single Error Corrected Interrupt Status Register	Section 27.8.69
480h	MCANERR_SEC_ENABLE_SET	MCAN Single Error Corrected Interrupt Enable Set Register	Section 27.8.70
4C0h	MCANERR_SEC_ENABLE_CLR	MCAN Single Error Corrected Interrupt Enable Clear Register	Section 27.8.71
53Ch	MCANERR_DED_EOI	MCAN Double Error Detected End of Interrupt Register	Section 27.8.72
540h	MCANERR_DED_STATUS	MCAN Double Error Detected Interrupt Status Register	Section 27.8.73
580h	MCANERR_DED_ENABLE_SET	MCAN Double Error Detected Interrupt Enable Set Register	Section 27.8.74
5C0h	MCANERR_DED_ENABLE_CLR	MCAN Double Error Detected Interrupt Enable Clear Register	Section 27.8.75
600h	MCANERR_AGGR_ENABLE_SET	MCAN Error Aggregator Enable Set Register	Section 27.8.76
604h	MCANERR_AGGR_ENABLE_CLR	MCAN Error Aggregator Enable Clear Register	Section 27.8.77
608h	MCANERR_AGGR_STATUS_SET	MCAN Error Aggregator Status Set Register	Section 27.8.78
60Ch	MCANERR_AGGR_STATUS_CLR	MCAN Error Aggregator Status Clear Register	Section 27.8.79
800h	DESC	Description	Section 27.8.80
844h	IMASK0	Interrupt mask	Section 27.8.81
848h	RIS0	Raw interrupt status	Section 27.8.82

Table 27-12. CANFD Registers (continued)

Offset	Acronym	Register Name	Section
84Ch	MIS0	Masked interrupt status	Section 27.8.83
850h	ISET0	Interrupt set	Section 27.8.84
854h	ICLR0	Interrupt clear	Section 27.8.85
864h	DTB	Digital Test Bus	Section 27.8.86
868h	IMASK1	Interrupt mask	Section 27.8.87
86Ch	RIS1	Raw interrupt status	Section 27.8.88
870h	MIS1	Masked interrupt status	Section 27.8.89
874h	ISET1	Interrupt set	Section 27.8.90
878h	ICLR1	Interrupt clear	Section 27.8.91
904h	MCANSS_CLKDIV	Clock divider	Section 27.8.92
908h	MCANSS_CLKCTL	MCAN-SS clock stop control register	Section 27.8.93
90Ch	MCANSS_CLKSTS	MCANSS clock stop status register	Section 27.8.94
924h	MCANSS_DMA0_CTL	MCANSS Fixed DMA0 Control Register	Section 27.8.95
92Ch	MCANSS_DMA1_CTL	MCANSS Fixed DMA1 Control Register	Section 27.8.96
938h	RXDMA_TTO_FE0_BA	Rx buffer [x] base address - most significant word	Section 27.8.97
948h	RXDMA_TTO_FE1_BA	Rx buffer [x+1] base address - most significant word	Section 27.8.98
950h	RXDMA_TTO_NDAT1	Rx Buffer two-to-one DMA mode, hardware NDAT1 value register.	Section 27.8.99

Complex bit access types are encoded to fit into small table cells. Table 27-13 shows the codes that are used for access types in this section.

Table 27-13. CANFD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WD	W D	Write Decrement. Decrements the specified bit field by the amount written.
WI	W I	Write Increment. Increments the specified bit field by the amount written.
WQ	W Q	Write Qualified. A condition must be met for this operation to occur.
Reset or Default Value		
-n		Value after reset or the default value

27.8.1 MCAN_CREL Register (Offset = 0h) [Reset = 00000000h]

MCAN_CREL is shown in Table 27-14.

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MCAN Core Release Register

Table 27-14. MCAN_CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REL	R	3h	Core Release. One digit, BCD-coded.
27-24	STEP	R	2h	Step of Core Release. One digit, BCD-coded.
23-20	SUBSTEP	R	3h	Sub-Step of Core Release. One digit, BCD-coded.
19-16	YEAR	R	8h	Time Stamp Year. One digit, BCD-coded.
15-8	MON	R	6h	Time Stamp Month. Two digits, BCD-coded.
7-0	DAY	R	8h	Time Stamp Day. Two digits, BCD-coded.

27.8.2 MCAN_ENDN Register (Offset = 4h) [Reset = 00000000h]

MCAN_ENDN is shown in Table 27-15.

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MCAN Endian Register

Table 27-15. MCAN_ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ETV	R	87654321h	Endianess Test Value. Reading the constant value maintained in this register allows software to determine the endianess of the host CPU.

27.8.3 MCAN_DBTP Register (Offset = Ch) [Reset = 00000000h]

MCAN_DBTP is shown in Table 27-16.

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This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 m_can_cclk periods. tq = (DBRP + 1) mtq.;DTSEG1 is the sum of Prop_Seg and Phase_Seg1. DTSEG2 is Phase_Seg2.;Therefore the length of the bit time is (programmed values) (DTSEG1 + DTSEG2 + 3) tq or (functional values) (Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2) tq.;The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Table 27-16. MCAN_DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	TDC	R/WQ	0h	Transmitter Delay Compensation; 0 Transmitter Delay Compensation disabled; 1 Transmitter Delay Compensation enabled
22-21	RESERVED	R	0h	Reserved
20-16	DBRP	R/WQ	0h	Data Bit Rate Prescaler. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-13	RESERVED	R	0h	Reserved
12-8	DTSEG1	R/WQ	Ah	Data Time Segment Before Sample Point. Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7-4	DTSEG2	R/WQ	3h	Data Time Segment After Sample Point. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-0	DSJW	R/WQ	3h	Data Resynchronization Jump Width. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.4 MCAN_TEST Register (Offset = 10h) [Reset = 00000000h]

MCAN_TEST is shown in Table 27-17.

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Write access to the Test Register has to be enabled by setting bit CCCR.TEST to '1'. All Test Register functions are set to their reset values when bit CCCR.TEST is reset.;Loop Back Mode and software control of the internal CAN TX pin are hardware test modes. Programming of;TX ? "00" may disturb the message transfer on the CAN bus.

Table 27-17. MCAN_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RX	R	0h	Receive Pin. Monitors the actual value of the CAN receive pin.; 0 The CAN bus is dominant (CAN RX pin = '0'); 1 The CAN bus is recessive (CAN RX pin = '1')
6-5	TX	R/WQ	0h	Control of Transmit Pin; 00 CAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time; 01 Sample Point can be monitored at CAN TX pin; 10 Dominant ('0') level at CAN TX pin; 11 Recessive ('1') at CAN TX pin; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
4	LBCK	R/WQ	0h	Loop Back Mode; 0 Reset value, Loop Back Mode is disabled; 1 Loop Back Mode is enabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-0	RESERVED	R	0h	Reserved

27.8.5 MCAN_RWD Register (Offset = 14h) [Reset = 00000000h]

MCAN_RWD is shown in Table 27-18.

Return to the Summary Table.

MCAN RAM Watchdog

Table 27-18. MCAN_RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	WDV	R	0h	Watchdog Value. Acutal Message RAM Watchdog Counter Value.; ;The RAM Watchdog monitors the READY output of the Message RAM. A Message RAM access via the MCAN's Generic Master Interface starts the Message RAM Watchdog Counter with the value configured by the WDC field. The counter is reloaded with WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag MCAN_IR.WDI is set. The RAM Watchdog Counter is clocked by the host (system) clock.
7-0	WDC	R/WQ	0h	Watchdog Configuration. Start value of the Message RAM Watchdog Counter. With the reset value of "00" the counter is disabled.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.6 MCAN_CCCR Register (Offset = 18h) [Reset = 00000000h]

MCAN_CCCR is shown in Table 27-19.

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MCAN CC Control Register

Table 27-19. MCAN_CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NISO	R/WQ	0h	Non ISO Operation. If this bit is set, the MCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0.; 0 CAN FD frame format according to ISO 11898-1:2015; 1 CAN FD frame format according to Bosch CAN FD Specification V1.0
14	TXP	R/WQ	0h	Transmit Pause. If this bit is set, the MCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame.; 0 Transmit pause disabled; 1 Transmit pause enabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
13	EFBI	R/WQ	0h	Edge Filtering during Bus Integration; 0 Edge filtering disabled; 1 Two consecutive dominant tq required to detect an edge for hard synchronization; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
12	PXHD	R/WQ	0h	Protocol Exception Handling Disable; 0 Protocol exception handling enabled; 1 Protocol exception handling disabled;Note: When protocol exception handling is disabled, the MCAN will transmit an error frame when it detects a protocol exception condition.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
11-10	RESERVED	R	0h	Reserved
9	BRSE	R/WQ	0h	Bit Rate Switch Enable; 0 Bit rate switching for transmissions disabled; 1 Bit rate switching for transmissions enabled;Note: When CAN FD operation is disabled FDOE = '0', BRSE is not evaluated.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
8	FDOE	R/WQ	0h	Flexible Datarate Operation Enable; 0 FD operation disabled; 1 FD operation enabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	TEST	R/WQ	0h	Test Mode Enable; 0 Normal operation, register TEST holds reset values; 1 Test Mode, write access to register TEST enabled; ;Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
6	DAR	R/WQ	0h	Disable Automatic Retransmission; 0 Automatic retransmission of messages not transmitted successfully enabled; 1 Automatic retransmission disabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
5	MON	R/WQ	0h	Bus Monitoring Mode. Bit MON can only be set by SW when both CCE and INIT are set to '1'. The bit can be reset by SW at any time.; 0 Bus Monitoring Mode is disabled; 1 Bus Monitoring Mode is enabled; ;Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
4	CSR	R/W	0h	Clock Stop Request; 0 No clock stop is requested; 1 Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0h	Clock Stop Acknowledge; 0 No clock stop acknowledged; 1 MCAN may be set in power down by stopping the Host and CAN clocks
2	ASM	R/WQ	0h	Restricted Operation Mode. Bit ASM can only be set by SW when both CCE and INIT are set to '1'. The bit can be reset by SW at any time.; 0 Normal CAN operation; 1 Restricted Operation Mode active; ;Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

Table 27-19. MCAN_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CCE	R/WQ	0h	Configuration Change Enable; 0 The CPU has no write access to the protected configuration registers; 1 The CPU has write access to the protected configuration registers (while CCCR.INIT = '1'); ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	INIT	R/W	1h	Initialization; 0 Normal Operation; 1 Initialization is started;Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to INIT can be read back. Therefore the programmer has to assure that the previous value written to INIT has been accepted by reading INIT before setting INIT to a new value.

27.8.7 MCAN_NBTP Register (Offset = 1Ch) [Reset = 00000000h]

MCAN_NBTP is shown in Table 27-20.

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This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 m_can_cclk periods. tq = (NBRP + 1) mtq.;NTSEG1 is the sum of Prop_Seg and Phase_Seg1. NTSEG2 is Phase_Seg2.;Therefore the length of the bit time is (programmed values) (NTSEG1 + NTSEG2 + 3) tq or (functional values) (Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2) tq.;The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.;Note: With a CAN clock of 8 MHz, the reset value of 0x06000A03 configures the MCAN for a bit rate of 500 kBit/s.

Table 27-20. MCAN_NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	NSJW	R/WQ	3h	Nominal (Re)Synchronization Jump Width. Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
24-16	NBRP	R/WQ	0h	Nominal Bit Rate Prescaler. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-8	NTSEG1	R/WQ	Ah	Nominal Time Segment Before Sample Point. Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R	0h	Reserved
6-0	NTSEG2	R/WQ	3h	Nominal Time Segment After Sample Point. Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.8 MCAN_TSCC Register (Offset = 20h) [Reset = 00000000h]

MCAN_TSCC is shown in Table 27-21.

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MCAN Timestamp Counter Configuration

Table 27-21. MCAN_TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	TCP	R/WQ	0h	Timestamp Counter Prescaler. Configures the timestamp and timeout counters time unit in multiples of CAN bit times. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.; ;Note: With CAN FD an external counter is required for timestamp generation (TSS = "10").; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	RESERVED	R	0h	Reserved
1-0	TSS	R/WQ	0h	Timestamp Select; 00 Timestamp counter value always 0x0000; 01 Timestamp counter value incremented according to TCP; 10 External timestamp counter value used; 11 Same as "00"; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.9 MCAN_TSCV Register (Offset = 24h) [Reset = 00000000h]

MCAN_TSCV is shown in Table 27-22.

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MCAN Timestamp Counter Value

Table 27-22. MCAN_TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TSC	R/W	0h	Timestamp Counter. The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = "01", the Timestamp Counter is incremented in multiples of CAN bit times, (1...16), depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = "10", TSC reflects the External Timestamp Counter value, and a write access has no impact.; ;Note: A "wrap around" is a change of the Timestamp Counter value from non-zero to zero not;caused by write access to MCAN_TSCV.

27.8.10 MCAN_TOCC Register (Offset = 28h) [Reset = 00000000h]

MCAN_TOCC is shown in Table 27-23.

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MCAN Timeout Counter Configuration

Table 27-23. MCAN_TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TOP	R/WQ	FFFFh	Timeout Period. Start value of the Timeout Counter (down-counter). Configures the Timeout Period.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-3	RESERVED	R	0h	Reserved
2-1	TOS	R/WQ	0h	Timeout Select. When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored.; 00 Continuous operation; 01 Timeout controlled by Tx Event FIFO; 10 Timeout controlled by Rx FIFO 0; 11 Timeout controlled by Rx FIFO 1; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	ETOC	R/WQ	0h	Enable Timeout Counter; 0 Timeout Counter disabled; 1 Timeout Counter enabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.11 MCAN_TOCV Register (Offset = 2Ch) [Reset = 00000000h]

MCAN_TOCV is shown in Table 27-24.

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MCAN Timeout Counter Value

Table 27-24. MCAN_TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TOC	R/W	FFFFh	Timeout Counter. The Timeout Counter is decremented in multiples of CAN bit times, (1...16), depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS.

27.8.12 MCAN_ECR Register (Offset = 40h) [Reset = 00000000h]

MCAN_ECR is shown in Table 27-25.

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MCAN Error Counter Register

Table 27-25. MCAN_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	CEL	R	0h	CAN Error Logging. The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO.; ;Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.
15	RP	R	0h	Receive Error Passive; 0 The Receive Error Counter is below the error passive level of 128; 1 The Receive Error Counter has reached the error passive level of 128
14-8	REC	R	0h	Receive Error Counter. Actual state of the Receive Error Counter, values between 0 and 127.; ;Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.
7-0	TEC	R	0h	Transmit Error Counter. Actual state of the Transmit Error Counter, values between 0 and 255.; ;Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.

27.8.13 MCAN_PSR Register (Offset = 44h) [Reset = 00000000h]

MCAN_PSR is shown in Table 27-26.

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MCAN Protocol Status Register

Table 27-26. MCAN_PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	TDCV	R	0h	Transmitter Delay Compensation Value. Position of the secondary sample point, defined by the sum of the measured delay from the internal CAN TX signal to the internal CAN RX signal and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.
15	RESERVED	R	0h	Reserved
14	PXE	R	0h	Protocol Exception Event; 0 No protocol exception event occurred since last read access; 1 Protocol exception event occurred
13	RFDF	R	0h	Received a CAN FD Message. This bit is set independent of acceptance filtering.; 0 Since this bit was reset by the CPU, no CAN FD message has been received; 1 Message in CAN FD format with FDF flag set has been received
12	RBRS	R	0h	BRS Flag of Last Received CAN FD Message. This bit is set together with RFDF, independent of acceptance filtering.; 0 Last received CAN FD message did not have its BRS flag set; 1 Last received CAN FD message had its BRS flag set
11	RESI	R	0h	ESI Flag of Last Received CAN FD Message. This bit is set together with RFDF, independent of acceptance filtering.; 0 Last received CAN FD message did not have its ESI flag set; 1 Last received CAN FD message had its ESI flag set
10-8	DLEC	R	7h	Data Phase Last Error Code. Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	BO	R	0h	Bus_Off Status; 0 The M_CAN is not Bus_Off; 1 The M_CAN is in Bus_Off state
6	EW	R	0h	Warning Status; 0 Both error counters are below the Error_Warning limit of 96; 1 At least one of error counter has reached the Error_Warning limit of 96
5	EP	R	0h	Error Passive; 0 The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected; 1 The M_CAN is in the Error_Passive state
4-3	ACT	R	0h	Node Activity. Monitors the module's CAN communication state.; 00 Synchronizing - node is synchronizing on CAN communication; 01 Idle - node is neither receiver nor transmitter; 10 Receiver - node is operating as receiver; 11 Transmitter - node is operating as transmitter; ;Note: ACT is set to "00" by a Protocol Exception Event.

Table 27-26. MCAN_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LEC	R	7h	Last Error Code. The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error.; 0 No Error: No error occurred since LEC has been reset by successful reception or transmission.; 1 Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.; 2 Form Error: A fixed format part of a received frame has the wrong format.; 3 AckError: The message transmitted by the MCAN was not acknowledged by another node.; 4 Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.; 5 Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value '0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).; 6 CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.; 7 NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register.; ;Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in DLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. Note: The Bus_Off recovery sequence (see ISO 11898-1:2015) cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

27.8.14 MCAN_TDCR Register (Offset = 48h) [Reset = 00000000h]

MCAN_TDCR is shown in Table 27-27.

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MCAN Transmitter Delay Compensation Register

Table 27-27. MCAN_TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-8	TDCO	R/WQ	0h	Transmitter Delay Compensation Offset. Offset value defining the distance between the measured delay from the internal CAN TX signal to the internal CAN RX signal and the secondary sample point. Valid values are 0 to 127 mtq.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R	0h	Reserved
6-0	TDCF	R/WQ	0h	Transmitter Delay Compensation Filter Window Length. Defines the minimum value for the SSP position, dominant edges on the internal CAN RX signal that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.15 MCAN_IR Register (Offset = 50h) [Reset = 00000000h]

MCAN_IR is shown in Table 27-28.

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The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. Aflag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. Ahard reset will clear the register. The configuration of IE controls whether an interrupt is generated. The configuration of ILS controls on which interrupt line an interrupt is signalled.

Table 27-28. MCAN_IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	ARA	R/W	0h	Access to Reserved Address; 0 No access to reserved address occurred; 1 Access to reserved address occurred
28	PED	R/W	0h	Protocol Error in Data Phase (Data Bit Time is used); 0 No protocol error in data phase; 1 Protocol error in data phase detected (PSR.DLEC ? 0,7)
27	PEA	R/W	0h	Protocol Error in Arbitration Phase (Nominal Bit Time is used); 0 No protocol error in arbitration phase; 1 Protocol error in arbitration phase detected (PSR.LEC ? 0,7)
26	WDI	R/W	0h	Watchdog Interrupt; 0 No Message RAM Watchdog event occurred; 1 Message RAM Watchdog event due to missing READY
25	BO	R/W	0h	Bus_Off Status; 0 Bus_Off status unchanged; 1 Bus_Off status changed
24	EW	R/W	0h	Warning Status; 0 Error_Warning status unchanged; 1 Error_Warning status changed
23	EP	R/W	0h	Error Passive; 0 Error_Passive status unchanged; 1 Error_Passive status changed
22	ELO	R/W	0h	Error Logging Overflow; 0 CAN Error Logging Counter did not overflow; 1 Overflow of CAN Error Logging Counter occurred
21	BEU	R/W	0h	Bit Error Uncorrected. Message RAM bit error detected, uncorrected. This bit is set when a double bit error is detected by the ECC aggregator attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data.; 0 No bit error detected when reading from Message RAM; 1 Bit error detected, uncorrected (e.g. parity logic)
20	RESERVED	R	0h	Reserved
19	DRX	R/W	0h	Message Stored to Dedicated Rx Buffer. The flag is set whenever a received message has been stored into a dedicated Rx Buffer.; 0 No Rx Buffer updated; 1 At least one received message stored into an Rx Buffer
18	TOO	R/W	0h	Timeout Occurred; 0 No timeout; 1 Timeout reached

Table 27-28. MCAN_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	MRAF	R/W	0h	Message RAM Access Failure. The flag is set, when the Rx Handler:; - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message.; - was not able to write a message to the Message RAM. In this case message storage is aborted.; ;In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location.; ;The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM.; 0 No Message RAM access failure occurred; 1 Message RAM access failure occurred
16	TSW	R/W	0h	Timestamp Wraparound; 0 No timestamp counter wrap-around; 1 Timestamp counter wrapped around
15	TEFL	R/W	0h	Tx Event FIFO Element Lost; 0 No Tx Event FIFO element lost; 1 Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W	0h	Tx Event FIFO Full; 0 Tx Event FIFO not full; 1 Tx Event FIFO full
13	TEFW	R/W	0h	Tx Event FIFO Watermark Reached; 0 Tx Event FIFO fill level below watermark; 1 Tx Event FIFO fill level reached watermark
12	TEFN	R/W	0h	Tx Event FIFO New Entry; 0 Tx Event FIFO unchanged; 1 Tx Handler wrote Tx Event FIFO element
11	TFE	R/W	0h	Tx FIFO Empty; 0 Tx FIFO non-empty; 1 Tx FIFO empty
10	TCF	R/W	0h	Transmission Cancellation Finished; 0 No transmission cancellation finished; 1 Transmission cancellation finished
9	TC	R/W	0h	Transmission Completed; 0 No transmission completed; 1 Transmission completed
8	HPM	R/W	0h	High Priority Message; 0 No high priority message received; 1 High priority message received
7	RF1L	R/W	0h	Rx FIFO 1 Message Lost; 0 No Rx FIFO 1 message lost; 1 Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	RF1F	R/W	0h	Rx FIFO 1 Full; 0 Rx FIFO 1 not full; 1 Rx FIFO 1 full
5	RF1W	R/W	0h	Rx FIFO 1 Watermark Reached; 0 Rx FIFO 1 fill level below watermark; 1 Rx FIFO 1 fill level reached watermark
4	RF1N	R/W	0h	Rx FIFO 1 New Message; 0 No new message written to Rx FIFO 1; 1 New message written to Rx FIFO 1
3	RF0L	R/W	0h	Rx FIFO 0 Message Lost; 0 No Rx FIFO 0 message lost; 1 Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W	0h	Rx FIFO 0 Full; 0 Rx FIFO 0 not full; 1 Rx FIFO 0 full
1	RF0W	R/W	0h	Rx FIFO 0 Watermark Reached; 0 Rx FIFO 0 fill level below watermark; 1 Rx FIFO 0 fill level reached watermark
0	RF0N	R/W	0h	Rx FIFO 0 New Message; 0 No new message written to Rx FIFO 0; 1 New message written to Rx FIFO 0

27.8.16 MCAN_IE Register (Offset = 54h) [Reset = 00000000h]

MCAN_IE is shown in Table 27-29.

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MCAN Interrupt Enable

Table 27-29. MCAN_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	ARAE	R/W	0h	Access to Reserved Address Enable
28	PEDE	R/W	0h	Protocol Error in Data Phase Enable
27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Enable
26	WDIE	R/W	0h	Watchdog Interrupt Enable
25	BOE	R/W	0h	Bus_Off Status Enable
24	EWE	R/W	0h	Warning Status Enable
23	EPE	R/W	0h	Error Passive Enable
22	ELOE	R/W	0h	Error Logging Overflow Enable
21	BEUE	R/W	0h	Bit Error Uncorrected Enable
20	RESERVED	R	0h	Reserved
19	DRXE	R/W	0h	Message Stored to Dedicated Rx Buffer Enable
18	TOOE	R/W	0h	Timeout Occurred Enable
17	MRAFE	R/W	0h	Message RAM Access Failure Enable
16	TSWE	R/W	0h	Timestamp Wraparound Enable
15	TEFLE	R/W	0h	Tx Event FIFO Element Lost Enable
14	TEFFE	R/W	0h	Tx Event FIFO Full Enable
13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Enable
12	TEFNE	R/W	0h	Tx Event FIFO New Entry Enable
11	TFEE	R/W	0h	Tx FIFO Empty Enable
10	TCFE	R/W	0h	Transmission Cancellation Finished Enable
9	TCE	R/W	0h	Transmission Completed Enable
8	HPME	R/W	0h	High Priority Message Enable
7	RF1LE	R/W	0h	Rx FIFO 1 Message Lost Enable
6	RF1FE	R/W	0h	Rx FIFO 1 Full Enable
5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Enable
4	RF1NE	R/W	0h	Rx FIFO 1 New Message Enable
3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Enable
2	RF0FE	R/W	0h	Rx FIFO 0 Full Enable
1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Enable
0	RF0NE	R/W	0h	Rx FIFO 0 New Message Enable

27.8.17 MCAN_ILS Register (Offset = 58h) [Reset = 00000000h]

MCAN_ILS is shown in Table 27-30.

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The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

Table 27-30. MCAN_ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	ARAL	R/W	0h	Access to Reserved Address Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
28	PEDL	R/W	0h	Protocol Error in Data Phase Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
26	WDIL	R/W	0h	Watchdog Interrupt Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
25	BOL	R/W	0h	Bus_Off Status Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
24	EWL	R/W	0h	Warning Status Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
23	EPL	R/W	0h	Error Passive Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
22	ELOL	R/W	0h	Error Logging Overflow Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
21	BEUL	R/W	0h	Bit Error Uncorrected Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
20	RESERVED	R	0h	Reserved
19	DRXL	R/W	0h	Message Stored to Dedicated Rx Buffer Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
18	TOOL	R/W	0h	Timeout Occurred Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
17	MRAFL	R/W	0h	Message RAM Access Failure Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
16	TSWL	R/W	0h	Timestamp Wraparound Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
15	TEFLL	R/W	0h	Tx Event FIFO Element Lost Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
14	TEFFL	R/W	0h	Tx Event FIFO Full Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
12	TEFNL	R/W	0h	Tx Event FIFO New Entry Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
11	TFEL	R/W	0h	Tx FIFO Empty Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
10	TCFL	R/W	0h	Transmission Cancellation Finished Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
9	TCL	R/W	0h	Transmission Completed Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1

Table 27-30. MCAN_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	HPML	R/W	0h	High Priority Message Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
7	RF1LL	R/W	0h	Rx FIFO 1 Message Lost Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
6	RF1FL	R/W	0h	Rx FIFO 1 Full Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
4	RF1NL	R/W	0h	Rx FIFO 1 New Message Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
2	RF0FL	R/W	0h	Rx FIFO 0 Full Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Line; 0 Interrupt source is assigned to Interrupt Line 0; 1 Interrupt source is assigned to Interrupt Line 1

27.8.18 MCAN_ILE Register (Offset = 5Ch) [Reset = 00000000h]

MCAN_ILE is shown in Table 27-31.

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MCAN Interrupt Line Enable

Table 27-31. MCAN_ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	EINT1	R/W	0h	Enable Interrupt Line 1; 0 Interrupt Line 1 is disabled; 1 Interrupt Line 1 is enabled
0	EINT0	R/W	0h	Enable Interrupt Line 0; 0 Interrupt Line 0 is disabled; 1 Interrupt Line 0 is enabled

27.8.19 MCAN_GFC Register (Offset = 80h) [Reset = 00000000h]

MCAN_GFC is shown in Table 27-32.

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MCAN Global Filter Configuration

Table 27-32. MCAN_GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-4	ANFS	R/WQ	0h	Accept Non-matching Frames Standard. Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated.; 00 Accept in Rx FIFO 0; 01 Accept in Rx FIFO 1; 10 Reject; 11 Reject; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-2	ANFE	R/WQ	0h	Accept Non-matching Frames Extended. Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated.; 00 Accept in Rx FIFO 0; 01 Accept in Rx FIFO 1; 10 Reject; 11 Reject; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1	RRFS	R/WQ	0h	Reject Remote Frames Standard; 0 Filter remote frames with 11-bit standard IDs; 1 Reject all remote frames with 11-bit standard IDs; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	RRFE	R/WQ	0h	Reject Remote Frames Extended; 0 Filter remote frames with 29-bit extended IDs; 1 Reject all remote frames with 29-bit extended IDs; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.20 MCAN_SIDFC Register (Offset = 84h) [Reset = 00000000h]

MCAN_SIDFC is shown in Table 27-33.

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MCAN Standard ID Filter Configuration

Table 27-33. MCAN_SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	LSS	R/WQ	0h	List Size Standard; 0 No standard Message ID filter; 1-128 Number of standard Message ID filter elements; >128 Values greater than 128 are interpreted as 128
15-2	FLSSA	R/WQ	0h	Filter List Standard Start Address. Start address of standard Message ID filter list (32-bit word address).
1-0	RESERVED	R	0h	Reserved

27.8.21 MCAN_XIDFC Register (Offset = 88h) [Reset = 00000000h]

MCAN_XIDFC is shown in Table 27-34.

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MCAN Extended ID Filter Configuration

Table 27-34. MCAN_XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	LSE	R/WQ	0h	List Size Extended; 0 No extended Message ID filter; 1-64 Number of extended Message ID filter elements; >64 Values greater than 64 are interpreted as 64; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	FLESA	R/WQ	0h	Filter List Extended Start Address. Start address of extended Message ID filter list (32-bit word address).; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R	0h	Reserved

27.8.22 MCAN_XIDAM Register (Offset = 90h) [Reset = 00000000h]

MCAN_XIDAM is shown in Table 27-35.

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MCAN Extended ID and Mask

Table 27-35. MCAN_XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-0	EIDM	R/WQ	1FFFFFFFh	Extended ID Mask. For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.23 MCAN_HPMS Register (Offset = 94h) [Reset = 00000000h]

MCAN_HPMS is shown in Table 27-36.

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This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Table 27-36. MCAN_HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	FLST	R	0h	Filter List. Indicates the filter list of the matching filter element.; 0 Standard Filter List; 1 Extended Filter List
14-8	FIDX	R	0h	Filter Index. Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7-6	MSI	R	0h	Message Storage Indicator; 00 No FIFO selected; 01 FIFO message lost; 10 Message stored in FIFO 0; 11 Message stored in FIFO 1
5-0	BIDX	R	0h	Buffer Index. Index of Rx FIFO element to which the message was stored. Only valid when MSI(1) = '1'.

27.8.24 MCAN_NDAT1 Register (Offset = 98h) [Reset = 00000000h]

MCAN_NDAT1 is shown in Table 27-37.

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MCAN New Data 1

Table 27-37. MCAN_NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND31	R/W	0h	New Data RX Buffer 31; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
30	ND30	R/W	0h	New Data RX Buffer 30; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
29	ND29	R/W	0h	New Data RX Buffer 29; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
28	ND28	R/W	0h	New Data RX Buffer 28; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
27	ND27	R/W	0h	New Data RX Buffer 27; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
26	ND26	R/W	0h	New Data RX Buffer 26; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
25	ND25	R/W	0h	New Data RX Buffer 25; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
24	ND24	R/W	0h	New Data RX Buffer 24; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
23	ND23	R/W	0h	New Data RX Buffer 23; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
22	ND22	R/W	0h	New Data RX Buffer 22; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
21	ND21	R/W	0h	New Data RX Buffer 21; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
20	ND20	R/W	0h	New Data RX Buffer 20; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
19	ND19	R/W	0h	New Data RX Buffer 19; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
18	ND18	R/W	0h	New Data RX Buffer 18; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
17	ND17	R/W	0h	New Data RX Buffer 17; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
16	ND16	R/W	0h	New Data RX Buffer 16; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
15	ND15	R/W	0h	New Data RX Buffer 15; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
14	ND14	R/W	0h	New Data RX Buffer 14; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
13	ND13	R/W	0h	New Data RX Buffer 13; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
12	ND12	R/W	0h	New Data RX Buffer 12; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
11	ND11	R/W	0h	New Data RX Buffer 11; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
10	ND10	R/W	0h	New Data RX Buffer 10; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
9	ND9	R/W	0h	New Data RX Buffer 9; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message

Table 27-37. MCAN_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ND8	R/W	0h	New Data RX Buffer 8; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
7	ND7	R/W	0h	New Data RX Buffer 7; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
6	ND6	R/W	0h	New Data RX Buffer 6; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
5	ND5	R/W	0h	New Data RX Buffer 5; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
4	ND4	R/W	0h	New Data RX Buffer 4; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
3	ND3	R/W	0h	New Data RX Buffer 3; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
2	ND2	R/W	0h	New Data RX Buffer 2; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
1	ND1	R/W	0h	New Data RX Buffer 1; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
0	ND0	R/W	0h	New Data RX Buffer 0; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message

27.8.25 MCAN_NDAT2 Register (Offset = 9Ch) [Reset = 00000000h]

MCAN_NDAT2 is shown in Table 27-38.

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MCAN New Data 2

Table 27-38. MCAN_NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND63	R/W	0h	New Data RX Buffer 63; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
30	ND62	R/W	0h	New Data RX Buffer 62; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
29	ND61	R/W	0h	New Data RX Buffer 61; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
28	ND60	R/W	0h	New Data RX Buffer 60; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
27	ND59	R/W	0h	New Data RX Buffer 59; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
26	ND58	R/W	0h	New Data RX Buffer 58; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
25	ND57	R/W	0h	New Data RX Buffer 57; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
24	ND56	R/W	0h	New Data RX Buffer 56; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
23	ND55	R/W	0h	New Data RX Buffer 55; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
22	ND54	R/W	0h	New Data RX Buffer 54; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
21	ND53	R/W	0h	New Data RX Buffer 53; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
20	ND52	R/W	0h	New Data RX Buffer 52; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
19	ND51	R/W	0h	New Data RX Buffer 51; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
18	ND50	R/W	0h	New Data RX Buffer 50; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
17	ND49	R/W	0h	New Data RX Buffer 49; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
16	ND48	R/W	0h	New Data RX Buffer 48; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
15	ND47	R/W	0h	New Data RX Buffer 47; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
14	ND46	R/W	0h	New Data RX Buffer 46; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
13	ND45	R/W	0h	New Data RX Buffer 45; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
12	ND44	R/W	0h	New Data RX Buffer 44; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
11	ND43	R/W	0h	New Data RX Buffer 43; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
10	ND42	R/W	0h	New Data RX Buffer 42; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
9	ND41	R/W	0h	New Data RX Buffer 41; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message

Table 27-38. MCAN_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ND40	R/W	0h	New Data RX Buffer 40; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
7	ND39	R/W	0h	New Data RX Buffer 39; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
6	ND38	R/W	0h	New Data RX Buffer 38; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
5	ND37	R/W	0h	New Data RX Buffer 37; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
4	ND36	R/W	0h	New Data RX Buffer 36; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
3	ND35	R/W	0h	New Data RX Buffer 35; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
2	ND34	R/W	0h	New Data RX Buffer 34; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
1	ND33	R/W	0h	New Data RX Buffer 33; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message
0	ND32	R/W	0h	New Data RX Buffer 32; 0 Rx Buffer not updated; 1 Rx Buffer updated from new message

27.8.26 MCAN_RXF0C Register (Offset = A0h) [Reset = 00000000h]

MCAN_RXF0C is shown in Table 27-39.

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MCAN Rx FIFO 0 Configuration

Table 27-39. MCAN_RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/WQ	0h	FIFO 0 Operation Mode. FIFO 0 can be operated in blocking or in overwrite mode.; 0 FIFO 0 blocking mode; 1 FIFO 0 overwrite mode; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
30-24	F0WM	R/WQ	0h	Rx FIFO 0 Watermark; 0 Watermark interrupt disabled; 1-64 Level for Rx FIFO 0 watermark interrupt (IR.RF0W); >64 Watermark interrupt disabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23	RESERVED	R	0h	Reserved
22-16	F0S	R/WQ	0h	Rx FIFO 0 Size. The Rx FIFO 0 elements are indexed from 0 to F0S-1.; 0 No Rx FIFO 0; 1-64 Number of Rx FIFO 0 elements; >64 Values greater than 64 are interpreted as 64; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	F0SA	R/WQ	0h	Rx FIFO 0 Start Address. Start address of Rx FIFO 0 in Message RAM (32-bit word address).; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R	0h	Reserved

27.8.27 MCAN_RXF0S Register (Offset = A4h) [Reset = 00000000h]

MCAN_RXF0S is shown in Table 27-40.

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MCAN Rx FIFO 0 Status

Table 27-40. MCAN_RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	RF0L	R	0h	Rx FIFO 0 Message Lost. This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset.; 0 No Rx FIFO 0 message lost; 1 Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero; ;Note: Overwriting the oldest message when RXF0C.F0OM = '1' will not set this flag.
24	F0F	R	0h	Rx FIFO 0 Full; 0 Rx FIFO 0 not full; 1 Rx FIFO 0 full
23-22	RESERVED	R	0h	Reserved
21-16	F0PI	R	0h	Rx FIFO 0 Put Index. Rx FIFO 0 write index pointer, range 0 to 63.
15-14	RESERVED	R	0h	Reserved
13-8	F0GI	R	0h	Rx FIFO 0 Get Index. Rx FIFO 0 read index pointer, range 0 to 63.
7	RESERVED	R	0h	Reserved
6-0	F0FL	R	0h	Rx FIFO 0 Fill Level. Number of elements stored in Rx FIFO 0, range 0 to 64.

27.8.28 MCAN_RXF0A Register (Offset = A8h) [Reset = 00000000h]

MCAN_RXF0A is shown in Table 27-41.

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MCAN Rx FIFO 0 Acknowledge

Table 27-41. MCAN_RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index. After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

27.8.29 MCAN_RXBC Register (Offset = ACh) [Reset = 00000000h]

MCAN_RXBC is shown in Table 27-42.

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MCAN Rx Buffer Configuration

Table 27-42. MCAN_RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	RBSA	R/WQ	0h	Rx Buffer Start Address. Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address).; ;+I466
1-0	RESERVED	R	0h	Reserved

27.8.30 MCAN_RXF1C Register (Offset = B0h) [Reset = 00000000h]

MCAN_RXF1C is shown in Table 27-43.

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MCAN Rx FIFO 1 Configuration

Table 27-43. MCAN_RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/WQ	0h	FIFO 1 Operation Mode. FIFO 1 can be operated in blocking or in overwrite mode.; 0 FIFO 1 blocking mode; 1 FIFO 1 overwrite mode; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
30-24	F1WM	R/WQ	0h	Rx FIFO 1 Watermark; 0 Watermark interrupt disabled; 1-64 Level for Rx FIFO 1 watermark interrupt (IR.RF1W); >64 Watermark interrupt disabled; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23	RESERVED	R	0h	Reserved
22-16	F1S	R/WQ	0h	Rx FIFO 1 Size. The Rx FIFO 1 elements are indexed from 0 to F1S - 1.; 0 No Rx FIFO 1; 1-64 Number of Rx FIFO 1 elements; >64 Values greater than 64 are interpreted as 64; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	F1SA	R/WQ	0h	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address).
1-0	RESERVED	R	0h	Reserved

27.8.31 MCAN_RXF1S Register (Offset = B4h) [Reset = 00000000h]

MCAN_RXF1S is shown in Table 27-44.

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MCAN Rx FIFO 1 Status

Table 27-44. MCAN_RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DMS	R	0h	Debug Message Status; 00 Idle state, wait for reception of debug messages, DMA request is cleared; 01 Debug message A received; 10 Debug messages A, B received; 11 Debug messages A, B, C received, DMA request is set
29-26	RESERVED	R	0h	Reserved
25	RF1L	R	0h	Rx FIFO 1 Message Lost. This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset.; 0 No Rx FIFO 1 message lost; 1 Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero; ;Note: Overwriting the oldest message when RXF1C.F1OM = '1' will not set this flag.
24	F1F	R	0h	Rx FIFO 1 Full; 0 Rx FIFO 1 not full; 1 Rx FIFO 1 full
23-22	RESERVED	R	0h	Reserved
21-16	F1PI	R	0h	Rx FIFO 1 Put Index. Rx FIFO 1 write index pointer, range 0 to 63.
15-14	RESERVED	R	0h	Reserved
13-8	F1GI	R	0h	Rx FIFO 1 Get Index. Rx FIFO 1 read index pointer, range 0 to 63.
7	RESERVED	R	0h	Reserved
6-0	F1FL	R	0h	Rx FIFO 1 Fill Level. Number of elements stored in Rx FIFO 1, range 0 to 64.

27.8.32 MCAN_RXF1A Register (Offset = B8h) [Reset = 00000000h]

MCAN_RXF1A is shown in Table 27-45.

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MCAN Rx FIFO 1 Acknowledge

Table 27-45. MCAN_RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	F1AI	R/W	0h	Rx FIFO 1 Acknowledge Index. After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

27.8.33 MCAN_RXESC Register (Offset = BCh) [Reset = 00000000h]

MCAN_RXESC is shown in Table 27-46.

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Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Table 27-46. MCAN_RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	RBDS	R/WQ	0h	Rx Buffer Data Field Size; 000 8 byte data field; 001 12 byte data field; 010 16 byte data field; 011 20 byte data field; 100 24 byte data field; 101 32 byte data field; 110 48 byte data field; 111 64 byte data field; ;Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R	0h	Reserved
6-4	F1DS	R/WQ	0h	Rx FIFO 1 Data Field Size; 000 8 byte data field; 001 12 byte data field; 010 16 byte data field; 011 20 byte data field; 100 24 byte data field; 101 32 byte data field; 110 48 byte data field; 111 64 byte data field; ;Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3	RESERVED	R	0h	Reserved
2-0	F0DS	R/WQ	0h	Rx FIFO 0 Data Field Size; 000 8 byte data field; 001 12 byte data field; 010 16 byte data field; 011 20 byte data field; 100 24 byte data field; 101 32 byte data field; 110 48 byte data field; 111 64 byte data field; ;Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.34 MCAN_TXBC Register (Offset = C0h) [Reset = 00000000h]

MCAN_TXBC is shown in Table 27-47.

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MCAN Tx Buffer Configuration

Table 27-47. MCAN_TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	TFQM	R/WQ	0h	Tx FIFO/Queue Mode; 0 Tx FIFO operation; 1 Tx Queue operation; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
29-24	TFQS	R/WQ	0h	Transmit FIFO/Queue Size; 0 No Tx FIFO/Queue; 1-32 Number of Tx Buffers used for Tx FIFO/Queue; >32 Values greater than 32 are interpreted as 32; ;Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23-22	RESERVED	R	0h	Reserved
21-16	NDTB	R/WQ	0h	Number of Dedicated Transmit Buffers; 0 No Dedicated Tx Buffers; 1-32 Number of Dedicated Tx Buffers; >32 Values greater than 32 are interpreted as 32; ;Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	TBSA	R/WQ	0h	Tx Buffers Start Address. Start address of Tx Buffers section in Message RAM (32-bit word address).; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R	0h	Reserved

27.8.35 MCAN_TXFQS Register (Offset = C4h) [Reset = 00000000h]

MCAN_TXFQS is shown in Table 27-48.

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The Tx FIFO/Queue status is related to the pending Tx requests listed in register TXBRP. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (TXBRP not yet updated).

Table 27-48. MCAN_TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	TFQF	R	0h	Tx FIFO/Queue Full; 0 Tx FIFO/Queue not full; 1 Tx FIFO/Queue full
20-16	TFQP	R	0h	Tx FIFO/Queue Put Index. Tx FIFO/Queue write index pointer, range 0 to 31.; ;Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.
15-13	RESERVED	R	0h	Reserved
12-8	TFGI	R	0h	Tx FIFO Get Index. Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1').; ;Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.
7-6	RESERVED	R	0h	Reserved
5-0	TFFL	R	0h	Tx FIFO Free Level. Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1').

27.8.36 MCAN_TXESC Register (Offset = C8h) [Reset = 00000000h]

MCAN_TXESC is shown in Table 27-49.

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Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Table 27-49. MCAN_TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	TBDS	R/WQ	0h	Tx Buffer Data Field Size; 000 8 byte data field; 001 12 byte data field; 010 16 byte data field; 011 20 byte data field; 100 24 byte data field; 101 32 byte data field; 110 48 byte data field; 111 64 byte data field; ;Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as "0xCC" (padding bytes).; ;Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

27.8.37 MCAN_TXBRP Register (Offset = CCh) [Reset = 00000000h]

MCAN_TXBRP is shown in Table 27-50.

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MCAN Tx Buffer Request Pending

Table 27-50. MCAN_TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRP31	R	0h	Transmission Request Pending 31. See description for bit 0.
30	TRP30	R	0h	Transmission Request Pending 30. See description for bit 0.
29	TRP29	R	0h	Transmission Request Pending 29. See description for bit 0.
28	TRP28	R	0h	Transmission Request Pending 28. See description for bit 0.
27	TRP27	R	0h	Transmission Request Pending 27. See description for bit 0.
26	TRP26	R	0h	Transmission Request Pending 26. See description for bit 0.
25	TRP25	R	0h	Transmission Request Pending 25. See description for bit 0.
24	TRP24	R	0h	Transmission Request Pending 24. See description for bit 0.
23	TRP23	R	0h	Transmission Request Pending 23. See description for bit 0.
22	TRP22	R	0h	Transmission Request Pending 22. See description for bit 0.
21	TRP21	R	0h	Transmission Request Pending 21. See description for bit 0.
20	TRP20	R	0h	Transmission Request Pending 20. See description for bit 0.
19	TRP19	R	0h	Transmission Request Pending 19. See description for bit 0.
18	TRP18	R	0h	Transmission Request Pending 18. See description for bit 0.
17	TRP17	R	0h	Transmission Request Pending 17. See description for bit 0.
16	TRP16	R	0h	Transmission Request Pending 16. See description for bit 0.
15	TRP15	R	0h	Transmission Request Pending 15. See description for bit 0.
14	TRP14	R	0h	Transmission Request Pending 14. See description for bit 0.
13	TRP13	R	0h	Transmission Request Pending 13. See description for bit 0.
12	TRP12	R	0h	Transmission Request Pending 12. See description for bit 0.
11	TRP11	R	0h	Transmission Request Pending 11. See description for bit 0.
10	TRP10	R	0h	Transmission Request Pending 10. See description for bit 0.
9	TRP9	R	0h	Transmission Request Pending 9. See description for bit 0.
8	TRP8	R	0h	Transmission Request Pending 8. See description for bit 0.
7	TRP7	R	0h	Transmission Request Pending 7. See description for bit 0.
6	TRP6	R	0h	Transmission Request Pending 6. See description for bit 0.
5	TRP5	R	0h	Transmission Request Pending 5. See description for bit 0.
4	TRP4	R	0h	Transmission Request Pending 4. See description for bit 0.
3	TRP3	R	0h	Transmission Request Pending 3. See description for bit 0.
2	TRP2	R	0h	Transmission Request Pending 2. See description for bit 0.
1	TRP1	R	0h	Transmission Request Pending 1. See description for bit 0.

Table 27-50. MCAN_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TRP0	R	0h	Transmission Request Pending 0.; ;Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR.; ;TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).; ;A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset.; ;After a cancellation has been requested, a finished cancellation is signalled via TXBCF;- after successful transmission together with the corresponding TXBTO bit;- when the transmission has not yet been started at the point of cancellation;- when the transmission has been aborted due to lost arbitration;- when an error occurred during frame transmission; ;In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions.; 0 No transmission request pending; 1 Transmission request pending; ;Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding TXBRP bit is reset.

27.8.38 MCAN_TXBAR Register (Offset = D0h) [Reset = 00000000h]

MCAN_TXBAR is shown in Table 27-51.

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MCAN Tx Buffer Add Request

Table 27-51. MCAN_TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AR31	R/WQ	0h	Add Request 31. See description for bit 0.
30	AR30	R/WQ	0h	Add Request 30. See description for bit 0.
29	AR29	R/WQ	0h	Add Request 29. See description for bit 0.
28	AR28	R/WQ	0h	Add Request 28. See description for bit 0.
27	AR27	R/WQ	0h	Add Request 27. See description for bit 0.
26	AR26	R/WQ	0h	Add Request 26. See description for bit 0.
25	AR25	R/WQ	0h	Add Request 25. See description for bit 0.
24	AR24	R/WQ	0h	Add Request 24. See description for bit 0.
23	AR23	R/WQ	0h	Add Request 23. See description for bit 0.
22	AR22	R/WQ	0h	Add Request 22. See description for bit 0.
21	AR21	R/WQ	0h	Add Request 21. See description for bit 0.
20	AR20	R/WQ	0h	Add Request 20. See description for bit 0.
19	AR19	R/WQ	0h	Add Request 19. See description for bit 0.
18	AR18	R/WQ	0h	Add Request 18. See description for bit 0.
17	AR17	R/WQ	0h	Add Request 17. See description for bit 0.
16	AR16	R/WQ	0h	Add Request 16. See description for bit 0.
15	AR15	R/WQ	0h	Add Request 15. See description for bit 0.
14	AR14	R/WQ	0h	Add Request 14. See description for bit 0.
13	AR13	R/WQ	0h	Add Request 13. See description for bit 0.
12	AR12	R/WQ	0h	Add Request 12. See description for bit 0.
11	AR11	R/WQ	0h	Add Request 11. See description for bit 0.
10	AR10	R/WQ	0h	Add Request 10. See description for bit 0.
9	AR9	R/WQ	0h	Add Request 9. See description for bit 0.
8	AR8	R/WQ	0h	Add Request 8. See description for bit 0.
7	AR7	R/WQ	0h	Add Request 7. See description for bit 0.
6	AR6	R/WQ	0h	Add Request 6. See description for bit 0.
5	AR5	R/WQ	0h	Add Request 5. See description for bit 0.
4	AR4	R/WQ	0h	Add Request 4. See description for bit 0.
3	AR3	R/WQ	0h	Add Request 3. See description for bit 0.
2	AR2	R/WQ	0h	Add Request 2. See description for bit 0.
1	AR1	R/WQ	0h	Add Request 1. See description for bit 0.
0	AR0	R/WQ	0h	Add Request 0.; ;Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed.; 0 No transmission request added; 1 Transmission requested added; ;Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored.; ;Qualified Write is possible only with CCCR.CCE='0'

27.8.39 MCAN_TXBCR Register (Offset = D4h) [Reset = 00000000h]

MCAN_TXBCR is shown in Table 27-52.

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MCAN Tx Buffer Cancellation Request

Table 27-52. MCAN_TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CR31	R/WQ	0h	Cancellation Request 31. See description for bit 0.
30	CR30	R/WQ	0h	Cancellation Request 30. See description for bit 0.
29	CR29	R/WQ	0h	Cancellation Request 29. See description for bit 0.
28	CR28	R/WQ	0h	Cancellation Request 28. See description for bit 0.
27	CR27	R/WQ	0h	Cancellation Request 27. See description for bit 0.
26	CR26	R/WQ	0h	Cancellation Request 26. See description for bit 0.
25	CR25	R/WQ	0h	Cancellation Request 25. See description for bit 0.
24	CR24	R/WQ	0h	Cancellation Request 24. See description for bit 0.
23	CR23	R/WQ	0h	Cancellation Request 23. See description for bit 0.
22	CR22	R/WQ	0h	Cancellation Request 22. See description for bit 0.
21	CR21	R/WQ	0h	Cancellation Request 21. See description for bit 0.
20	CR20	R/WQ	0h	Cancellation Request 20. See description for bit 0.
19	CR19	R/WQ	0h	Cancellation Request 19. See description for bit 0.
18	CR18	R/WQ	0h	Cancellation Request 18. See description for bit 0.
17	CR17	R/WQ	0h	Cancellation Request 17. See description for bit 0.
16	CR16	R/WQ	0h	Cancellation Request 16. See description for bit 0.
15	CR15	R/WQ	0h	Cancellation Request 15. See description for bit 0.
14	CR14	R/WQ	0h	Cancellation Request 14. See description for bit 0.
13	CR13	R/WQ	0h	Cancellation Request 13. See description for bit 0.
12	CR12	R/WQ	0h	Cancellation Request 12. See description for bit 0.
11	CR11	R/WQ	0h	Cancellation Request 11. See description for bit 0.
10	CR10	R/WQ	0h	Cancellation Request 10. See description for bit 0.
9	CR9	R/WQ	0h	Cancellation Request 9. See description for bit 0.
8	CR8	R/WQ	0h	Cancellation Request 8. See description for bit 0.
7	CR7	R/WQ	0h	Cancellation Request 7. See description for bit 0.
6	CR6	R/WQ	0h	Cancellation Request 6. See description for bit 0.
5	CR5	R/WQ	0h	Cancellation Request 5. See description for bit 0.
4	CR4	R/WQ	0h	Cancellation Request 4. See description for bit 0.
3	CR3	R/WQ	0h	Cancellation Request 3. See description for bit 0.
2	CR2	R/WQ	0h	Cancellation Request 2. See description for bit 0.
1	CR1	R/WQ	0h	Cancellation Request 1. See description for bit 0.
0	CR0	R/WQ	0h	Cancellation Request 0.; ;Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset.; 0 No cancellation pending; 1 Cancellation pending; ;Qualified Write is possible only with CCCR.CCE='0'

27.8.40 MCAN_TXBTO Register (Offset = D8h) [Reset = 00000000h]

MCAN_TXBTO is shown in Table 27-53.

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MCAN Tx Buffer Transmission Occurred

Table 27-53. MCAN_TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TO31	R	0h	Transmission Occurred 31. See description for bit 0.
30	TO30	R	0h	Transmission Occurred 30. See description for bit 0.
29	TO29	R	0h	Transmission Occurred 29. See description for bit 0.
28	TO28	R	0h	Transmission Occurred 28. See description for bit 0.
27	TO27	R	0h	Transmission Occurred 27. See description for bit 0.
26	TO26	R	0h	Transmission Occurred 26. See description for bit 0.
25	TO25	R	0h	Transmission Occurred 25. See description for bit 0.
24	TO24	R	0h	Transmission Occurred 24. See description for bit 0.
23	TO23	R	0h	Transmission Occurred 23. See description for bit 0.
22	TO22	R	0h	Transmission Occurred 22. See description for bit 0.
21	TO21	R	0h	Transmission Occurred 21. See description for bit 0.
20	TO20	R	0h	Transmission Occurred 20. See description for bit 0.
19	TO19	R	0h	Transmission Occurred 19. See description for bit 0.
18	TO18	R	0h	Transmission Occurred 18. See description for bit 0.
17	TO17	R	0h	Transmission Occurred 17. See description for bit 0.
16	TO16	R	0h	Transmission Occurred 16. See description for bit 0.
15	TO15	R	0h	Transmission Occurred 15. See description for bit 0.
14	TO14	R	0h	Transmission Occurred 14. See description for bit 0.
13	TO13	R	0h	Transmission Occurred 13. See description for bit 0.
12	TO12	R	0h	Transmission Occurred 12. See description for bit 0.
11	TO11	R	0h	Transmission Occurred 11. See description for bit 0.
10	TO10	R	0h	Transmission Occurred 10. See description for bit 0.
9	TO9	R	0h	Transmission Occurred 9. See description for bit 0.
8	TO8	R	0h	Transmission Occurred 8. See description for bit 0.
7	TO7	R	0h	Transmission Occurred 7. See description for bit 0.
6	TO6	R	0h	Transmission Occurred 6. See description for bit 0.
5	TO5	R	0h	Transmission Occurred 5. See description for bit 0.
4	TO4	R	0h	Transmission Occurred 4. See description for bit 0.
3	TO3	R	0h	Transmission Occurred 3. See description for bit 0.
2	TO2	R	0h	Transmission Occurred 2. See description for bit 0.
1	TO1	R	0h	Transmission Occurred 1. See description for bit 0.
0	TO0	R	0h	Transmission Occurred 0.; ;Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR.; 0 No transmission occurred; 1 Transmission occurred

27.8.41 MCAN_TXBCF Register (Offset = DCh) [Reset = 00000000h]

MCAN_TXBCF is shown in Table 27-54.

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MCAN Tx Buffer Cancellation Finished

Table 27-54. MCAN_TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CF31	R	0h	Cancellation Finished 31. See description for bit 0.
30	CF30	R	0h	Cancellation Finished 30. See description for bit 0.
29	CF29	R	0h	Cancellation Finished 29. See description for bit 0.
28	CF28	R	0h	Cancellation Finished 28. See description for bit 0.
27	CF27	R	0h	Cancellation Finished 27. See description for bit 0.
26	CF26	R	0h	Cancellation Finished 26. See description for bit 0.
25	CF25	R	0h	Cancellation Finished 25. See description for bit 0.
24	CF24	R	0h	Cancellation Finished 24. See description for bit 0.
23	CF23	R	0h	Cancellation Finished 23. See description for bit 0.
22	CF22	R	0h	Cancellation Finished 22. See description for bit 0.
21	CF21	R	0h	Cancellation Finished 21. See description for bit 0.
20	CF20	R	0h	Cancellation Finished 20. See description for bit 0.
19	CF19	R	0h	Cancellation Finished 19. See description for bit 0.
18	CF18	R	0h	Cancellation Finished 18. See description for bit 0.
17	CF17	R	0h	Cancellation Finished 17. See description for bit 0.
16	CF16	R	0h	Cancellation Finished 16. See description for bit 0.
15	CF15	R	0h	Cancellation Finished 15. See description for bit 0.
14	CF14	R	0h	Cancellation Finished 14. See description for bit 0.
13	CF13	R	0h	Cancellation Finished 13. See description for bit 0.
12	CF12	R	0h	Cancellation Finished 12. See description for bit 0.
11	CF11	R	0h	Cancellation Finished 11. See description for bit 0.
10	CF10	R	0h	Cancellation Finished 10. See description for bit 0.
9	CF9	R	0h	Cancellation Finished 9. See description for bit 0.
8	CF8	R	0h	Cancellation Finished 8. See description for bit 0.
7	CF7	R	0h	Cancellation Finished 7. See description for bit 0.
6	CF6	R	0h	Cancellation Finished 6. See description for bit 0.
5	CF5	R	0h	Cancellation Finished 5. See description for bit 0.
4	CF4	R	0h	Cancellation Finished 4. See description for bit 0.
3	CF3	R	0h	Cancellation Finished 3. See description for bit 0.
2	CF2	R	0h	Cancellation Finished 2. See description for bit 0.
1	CF1	R	0h	Cancellation Finished 1. See description for bit 0.
0	CF0	R	0h	Cancellation Finished 0.; ;Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR.; 0 No transmit buffer cancellation; 1 Transmit buffer cancellation finished

27.8.42 MCAN_TXBTIE Register (Offset = E0h) [Reset = 00000000h]

MCAN_TXBTIE is shown in Table 27-55.

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MCAN Tx Buffer Transmission Interrupt Enable

Table 27-55. MCAN_TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TIE31	R/W	0h	Transmission Interrupt Enable 31. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
30	TIE30	R/W	0h	Transmission Interrupt Enable 30. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
29	TIE29	R/W	0h	Transmission Interrupt Enable 29. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
28	TIE28	R/W	0h	Transmission Interrupt Enable 28. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
27	TIE27	R/W	0h	Transmission Interrupt Enable 27. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
26	TIE26	R/W	0h	Transmission Interrupt Enable 26. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
25	TIE25	R/W	0h	Transmission Interrupt Enable 25. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
24	TIE24	R/W	0h	Transmission Interrupt Enable 24. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
23	TIE23	R/W	0h	Transmission Interrupt Enable 23. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
22	TIE22	R/W	0h	Transmission Interrupt Enable 22. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
21	TIE21	R/W	0h	Transmission Interrupt Enable 21. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
20	TIE20	R/W	0h	Transmission Interrupt Enable 20. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
19	TIE19	R/W	0h	Transmission Interrupt Enable 19. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
18	TIE18	R/W	0h	Transmission Interrupt Enable 18. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
17	TIE17	R/W	0h	Transmission Interrupt Enable 17. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
16	TIE16	R/W	0h	Transmission Interrupt Enable 16. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable

Table 27-55. MCAN_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	TIE15	R/W	0h	Transmission Interrupt Enable 15. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
14	TIE14	R/W	0h	Transmission Interrupt Enable 14. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
13	TIE13	R/W	0h	Transmission Interrupt Enable 13. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
12	TIE12	R/W	0h	Transmission Interrupt Enable 12. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
11	TIE11	R/W	0h	Transmission Interrupt Enable 11. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
10	TIE10	R/W	0h	Transmission Interrupt Enable 10. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
9	TIE9	R/W	0h	Transmission Interrupt Enable 9. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
8	TIE8	R/W	0h	Transmission Interrupt Enable 8. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
7	TIE7	R/W	0h	Transmission Interrupt Enable 7. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
6	TIE6	R/W	0h	Transmission Interrupt Enable 6. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
5	TIE5	R/W	0h	Transmission Interrupt Enable 5. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
4	TIE4	R/W	0h	Transmission Interrupt Enable 4. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
3	TIE3	R/W	0h	Transmission Interrupt Enable 3. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
2	TIE2	R/W	0h	Transmission Interrupt Enable 2. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
1	TIE1	R/W	0h	Transmission Interrupt Enable 1. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable
0	TIE0	R/W	0h	Transmission Interrupt Enable 0. Each Tx Buffer has its own Transmission Interrupt Enable bit.; 0 Transmission interrupt disabled; 1 Transmission interrupt enable

27.8.43 MCAN_TXBCIE Register (Offset = E4h) [Reset = 00000000h]

MCAN_TXBCIE is shown in Table 27-56.

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MCAN Tx Buffer Cancellation Finished Interrupt Enable

Table 27-56. MCAN_TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFIE31	R/W	0h	Cancellation Finished Interrupt Enable 31. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
30	CFIE30	R/W	0h	Cancellation Finished Interrupt Enable 30. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
29	CFIE29	R/W	0h	Cancellation Finished Interrupt Enable 29. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
28	CFIE28	R/W	0h	Cancellation Finished Interrupt Enable 28. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
27	CFIE27	R/W	0h	Cancellation Finished Interrupt Enable 27. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
26	CFIE26	R/W	0h	Cancellation Finished Interrupt Enable 26. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
25	CFIE25	R/W	0h	Cancellation Finished Interrupt Enable 25. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
24	CFIE24	R/W	0h	Cancellation Finished Interrupt Enable 24. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
23	CFIE23	R/W	0h	Cancellation Finished Interrupt Enable 23. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
22	CFIE22	R/W	0h	Cancellation Finished Interrupt Enable 22. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
21	CFIE21	R/W	0h	Cancellation Finished Interrupt Enable 21. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
20	CFIE20	R/W	0h	Cancellation Finished Interrupt Enable 20. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
19	CFIE19	R/W	0h	Cancellation Finished Interrupt Enable 19. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
18	CFIE18	R/W	0h	Cancellation Finished Interrupt Enable 18. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
17	CFIE17	R/W	0h	Cancellation Finished Interrupt Enable 17. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
16	CFIE16	R/W	0h	Cancellation Finished Interrupt Enable 16. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled

Table 27-56. MCAN_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	CFIE15	R/W	0h	Cancellation Finished Interrupt Enable 15. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
14	CFIE14	R/W	0h	Cancellation Finished Interrupt Enable 14. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
13	CFIE13	R/W	0h	Cancellation Finished Interrupt Enable 13. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
12	CFIE12	R/W	0h	Cancellation Finished Interrupt Enable 12. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
11	CFIE11	R/W	0h	Cancellation Finished Interrupt Enable 11. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
10	CFIE10	R/W	0h	Cancellation Finished Interrupt Enable 10. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
9	CFIE9	R/W	0h	Cancellation Finished Interrupt Enable 9. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
8	CFIE8	R/W	0h	Cancellation Finished Interrupt Enable 8. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
7	CFIE7	R/W	0h	Cancellation Finished Interrupt Enable 7. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
6	CFIE6	R/W	0h	Cancellation Finished Interrupt Enable 6. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
5	CFIE5	R/W	0h	Cancellation Finished Interrupt Enable 5. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
4	CFIE4	R/W	0h	Cancellation Finished Interrupt Enable 4. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
3	CFIE3	R/W	0h	Cancellation Finished Interrupt Enable 3. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
2	CFIE2	R/W	0h	Cancellation Finished Interrupt Enable 2. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
1	CFIE1	R/W	0h	Cancellation Finished Interrupt Enable 1. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled
0	CFIE0	R/W	0h	Cancellation Finished Interrupt Enable 0. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.; 0 Cancellation finished interrupt disabled; 1 Cancellation finished interrupt enabled

27.8.44 MCAN_TXEFC Register (Offset = F0h) [Reset = 00000000h]

MCAN_TXEFC is shown in Table 27-57.

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MCAN Tx Event FIFO Configuration

Table 27-57. MCAN_TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	EFWM	R/WQ	0h	Event FIFO Watermark; 0 Watermark interrupt disabled; 1-32 Level for Tx Event FIFO watermark interrupt (IR.TEFW); >32 Watermark interrupt disabled
23-22	RESERVED	R	0h	Reserved
21-16	EFS	R/WQ	0h	Event FIFO Size. The Tx Event FIFO elements are indexed from 0 to EFS - 1.; 0 Tx Event FIFO disabled; 1-32 Number of Tx Event FIFO elements; >32 Values greater than 32 are interpreted as 32
15-2	EFSA	R/WQ	0h	Event FIFO Start Address. Start address of Tx Event FIFO in Message RAM (32-bit word address).
1-0	RESERVED	R	0h	Reserved

27.8.45 MCAN_TXEFS Register (Offset = F4h) [Reset = 00000000h]

MCAN_TXEFS is shown in Table 27-58.

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MCAN Tx Event FIFO Status

Table 27-58. MCAN_TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	TEFL	R	0h	Tx Event FIFO Element Lost. This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset.; 0 No Tx Event FIFO element lost; 1 Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	EFF	R	0h	Event FIFO Full; 0 Tx Event FIFO not full; 1 Tx Event FIFO full
23-21	RESERVED	R	0h	Reserved
20-16	EFPI	R	0h	Event FIFO Put Index.Tx Event FIFO write index pointer, range 0 to 31.
15-13	RESERVED	R	0h	Reserved
12-8	EFGI	R	0h	Event FIFO Get Index. Tx Event FIFO read index pointer, range 0 to 31.
7-6	RESERVED	R	0h	Reserved
5-0	EFFL	R	0h	Event FIFO Fill Level. Number of elements stored in Tx Event FIFO, range 0 to 32.

27.8.46 MCAN_TXEFA Register (Offset = F8h) [Reset = 00000000h]

MCAN_TXEFA is shown in Table 27-59.

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MCAN Tx Event FIFO Acknowledge

Table 27-59. MCAN_TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	EFAI	R/W	0h	Event FIFO Acknowledge Index. After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL.

27.8.47 MCANSS_PID Register (Offset = 200h) [Reset = 00000000h]

MCANSS_PID is shown in Table 27-60.

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MCAN Subsystem Revision Register

Table 27-60. MCANSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	BU	R	2h	Business Unit: 0x2 = Processors
27-16	MODULE_ID	R	8E0h	Module Identification Number
15-11	RTL	R	9h	RTL revision. Will vary depending on release
10-8	MAJOR	R	1h	Major Revision of the MCAN Subsystem
7-6	CUSTOM	R	0h	Custom Value
5-0	MINOR	R	1h	Minor Revision of the MCAN Subsystem

27.8.48 MCANSS_CTRL Register (Offset = 204h) [Reset = 00000000h]

MCANSS_CTRL is shown in Table 27-61.

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MCAN Subsystem Control Register

Table 27-61. MCANSS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	EXT_TS_CNTR_EN	R/W	0h	External Timestamp Counter Enable. When disabled, the counter is reset back to zero.While enabled, the counter keeps incrementing.; 0 External timestamp counter disabled; 1 External timestamp counter enabled
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable. Enables the MCANSS to automatically clear the MCAN CCCR.INIT bit, fully waking the MCAN up, on an enabled wakeup request.; 0 Disable the automatic write to CCCR.INIT; 1 Enable the automatic write to CCCR.INIT
4	WAKEUPREQEN	R/W	0h	Wakeup Request Enable. Enables the MCANSS to wakeup on CAN RXD activity.; 0 Disable wakeup request; 1 Enables wakeup request
3	DBGSUSP_FREE	R/W	1h	Debug Suspend Free Bit. Enables debug suspend.; 0 Disable debug suspend; 1 Enable debug suspend
2-0	RESERVED	R	0h	Reserved

27.8.49 MCANSS_STAT Register (Offset = 208h) [Reset = 00000000h]

MCANSS_STAT is shown in Table 27-62.

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MCAN Subsystem Status Register

Table 27-62. MCANSS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ENABLE_FDOE	R	0h	Flexible Datarate Operation Enable. Determines whether CAN FD operation can be enabled via the MCAN core CCCR.FDOE bit (bit 8) or if only standard CAN operation is possible with this instance of the MCAN.; 0 MCAN is only capable of standard CAN communication; 1 MCAN may be configured to perform CAN FD communication
1	MEM_INIT_DONE	R	0h	Memory Initialization Done.; 0 Message RAM initialization is in progress; 1 Message RAM is initialized for use
0	RESERVED	R	0h	Reserved

27.8.50 MCANSS_ICS Register (Offset = 20Ch) [Reset = 00000000h]

MCANSS_ICS is shown in Table 27-63.

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MCAN Subsystem Interrupt Clear Shadow Register

Table 27-63. MCANSS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_TS_CNTR_OVFL	R-0/W	0h	External Timestamp Counter Overflow Interrupt Status Clear. Reads always return a 0.; 0 Write of '0' has no effect; 1 Write of '1' clears the MCANSS_IRS.EXT_TS_CNTR_OVFL bit

27.8.51 MCANSS_IRS Register (Offset = 210h) [Reset = 00000000h]

MCANSS_IRS is shown in Table 27-64.

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MCAN Subsystem Interrupt Raw Status Register

Table 27-64. MCANSS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W	0h	External Timestamp Counter Overflow Interrupt Status. This bit is set by HW or by a SW write of '1'. To clear, use the MCANSS_ICS.EXT_TS_CNTR_OVFL bit.; 0 External timestamp counter has not overflowed; 1 External timestamp counter has overflowed; ;When this bit is set to '1' by HW or SW, the MCANSS_EXT_TS_UNSERVICED_INTR_CNTR.EXT_TS_INTR_CNTR bit field will increment by 1.

27.8.52 MCANSS_IECS Register (Offset = 214h) [Reset = 00000000h]

MCANSS_IECS is shown in Table 27-65.

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MCAN Subsystem Interrupt Enable Clear Shadow Register

Table 27-65. MCANSS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_TS_CNTR_OVFL	R-0/W	0h	External Timestamp Counter Overflow Interrupt Enable Clear. Reads always return a 0.; 0 Write of '0' has no effect; 1 Write of '1' clears the MCANSS_IES.EXT_TS_CNTR_OVFL bit

27.8.53 MCANSS_IE Register (Offset = 218h) [Reset = 00000000h]

MCANSS_IE is shown in Table 27-66.

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MCAN Subsystem Interrupt Enable Register

Table 27-66. MCANSS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_TS_CNTR_OVFL	R/W	0h	External Timestamp Counter Overflow Interrupt Enable. A write of '0' has no effect. A write of '1' unmasks the MCAN_IRS.EXT_EVT_CNTR_OVFLW and reflects the unmasked IRS value in MCAN_IES.EXT_TS_CNTR_OVFL

27.8.54 MCANSS_IES Register (Offset = 21Ch) [Reset = 00000000h]

MCANSS_IES is shown in Table 27-67.

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MCAN Subsystem Masked Interrupt Status. It is the logical AND of IRS and IE for the respecitve bits.

Table 27-67. MCANSS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_TS_CNTR_OVFL	R	0h	External Timestamp Counter Overflow masked interrupt status.; 0 External timestamp counter overflow interrupt is cleared; 1 External timestamp counter overflow interrupt is set

27.8.55 MCANSS_EOI Register (Offset = 220h) [Reset = 00000000h]

MCANSS_EOI is shown in Table 27-68.

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MCAN Subsystem End of Interrupt

Table 27-68. MCANSS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	EOI	R-0/W	0h	End of Interrupt. A write to this register will clear the associated interrupt. If the unserviced interrupt counter is > 1, another interrupt is generated.; 0x00 External TS Interrupt is cleared; 0x01 MCAN(0) interrupt is cleared; 0x02 MCAN(1) interrupt is cleared; Other writes are ignored.

27.8.56 MCANSS_EXT_TS_PRESCALER Register (Offset = 224h) [Reset = 00000000h]

MCANSS_EXT_TS_PRESCALER is shown in Table 27-69.

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MCAN Subsystem External Timestamp Prescaler 0

Table 27-69. MCANSS_EXT_TS_PRESCALER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	PRESCALER	R/W	Xh	External Timestamp Prescaler Reload Value. The external timestamp count rate is the host (system) clock rate divided by this value, except in the case of 0. A zero value in this bit field will act identically to a value of 0x000001.

27.8.57 MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register (Offset = 228h) [Reset = 00000000h]

MCANSS_EXT_TS_UNSERVICED_INTR_CNTR is shown in Table 27-70.

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MCAN Subsystem External Timestamp Unserviced Interrupts Counter

Table 27-70. MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	EXT_TS_INTR_CNTR	R	0h	External Timestamp Counter Unserviced Rollover Interrupts. If this value is > 1, an MCANSS_EOI write of '1' to bit 0 will issue another interrupt.; ;The status of this bit field is affected by the MCANSS_IRS.EXT_TS_CNTR_OVFL bit field.

27.8.58 MCANERR_REV Register (Offset = 400h) [Reset = 00000000h]

MCANERR_REV is shown in Table 27-71.

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MCAN Error Aggregator Revision Register

Table 27-71. MCANERR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	BU	R	2h	Business Unit: 0x2 = Processors
27-16	MODULE_ID	R	6A0h	Module Identification Number
15-11	REVRTL	R	1Dh	RTL revision. Will vary depending on release
10-8	REVMAJ	R	2h	Major Revision of the Error Aggregator
7-6	REVCUSTOM	R	0h	Custom Revision of the Error Aggregator
5-0	REVMIN	R	0h	Minor Revision of the Error Aggregator

27.8.59 MCANERR_VECTOR Register (Offset = 408h) [Reset = 00000000h]

MCANERR_VECTOR is shown in Table 27-72.

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Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the ECC_VECTOR field, together with the RD_SVBUS trigger and RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address.

Table 27-72. MCANERR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R	0h	Read Completion Flag
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address Offset
15	RD_SVBUS	R-0/W	0h	Read Trigger
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID. Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the ECC_VECTOR field, together with the RD_SVBUS trigger and RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address.; 0x000 Message RAM ECC controller is selected; Others Reserved (do not use); ;Subsequent writes through the SVBUS (offsets 0x10 - 0x3B) have a delayed completion. To avoid conflicts, perform a read back of a register within this range after writing.

27.8.60 MCANERR_STAT Register (Offset = 40Ch) [Reset = 00000000h]

MCANERR_STAT is shown in Table 27-73.

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MCAN Error Misc Status

Table 27-73. MCANERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	2h	Number of RAMs. Number of ECC RAMs serviced by the aggregator.

27.8.61 MCANERR_WRAP_REV Register (Offset = 410h) [Reset = 00000000h]

MCANERR_WRAP_REV is shown in Table 27-74.

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This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-74. MCANERR_WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	BU	R	2h	Business Unit: 0x2 = Processors
27-16	MODULE_ID	R	6A4h	Module Identification Number
15-11	REVRTL	R	Dh	RTL revision. Will vary depending on release
10-8	REVMAJ	R	2h	Major Revision of the Error Aggregator
7-6	REVCUSTOM	R	0h	Custom Revision of the Error Aggregator
5-0	REVMIN	R	2h	Minor Revision of the Error Aggregator

27.8.62 MCANERR_CTRL Register (Offset = 414h) [Reset = 00000000h]

MCANERR_CTRL is shown in Table 27-75.

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This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-75. MCANERR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	Enables Serial VBUS timeout mechanism
7	CHECK_PARITY	R/W	1h	Enables parity checking on internal data
6	ERROR_ONCE	R/W	0h	If this bit is set, the FORCE_SEC/FORCE_DED will inject an error to the specified row only once. The FORCE_SEC bit will be cleared once a writeback happens. If writeback is not enabled, this error will be cleared the cycle following the read when the data is corrected. For double-bit errors, the FORCE_DED bit will be cleared the cycle following the double-bit error. Any subsequent reads will not force an error.
5	FORCE_N_ROW	R/W	0h	Enable single/double-bit error on the next RAM read, regardless of the MCANERR_ERR_CTRL1.ECC_ROW setting. For write through mode, this applies to writes as well as reads.
4	FORCE_DED	R/W	0h	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is asserted. For write through mode, this applies to writes as well as reads. MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2 should be configured prior to setting this bit.
3	FORCE_SEC	R/W	0h	Force single-bit error. Cleared on a writeback or the cycle following the error if ERROR_ONCE is asserted. For write through mode, this applies to writes as well as reads. MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2 should be configured prior to setting this bit.
2	ENABLE_RMW	R/W	1h	Enable read-modify-write on partial word writes
1	ECC_CHECK	R/W	1h	Enable ECC Check. ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are '0'.
0	ECC_ENABLE	R/W	1h	Enable ECC Generation

27.8.63 MCANERR_ERR_CTRL1 Register (Offset = 418h) [Reset = 00000000h]

MCANERR_ERR_CTRL1 is shown in Table 27-76.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-76. MCANERR_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R/W	0h	Row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set.

27.8.64 MCANERR_ERR_CTRL2 Register (Offset = 41Ch) [Reset = 00000000h]

MCANERR_ERR_CTRL2 is shown in Table 27-77.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-77. MCANERR_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT2	R/W	0h	Second column/data bit that needs to be flipped when FORCE_DED is set
15-0	ECC_BIT1	R/W	0h	Column/Data bit that needs to be flipped when FORCE_SEC or FORCE_DED is set

27.8.65 MCANERR_ERR_STAT1 Register (Offset = 420h) [Reset = 00000000h]

MCANERR_ERR_STAT1 is shown in Table 27-78.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-78. MCANERR_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R	0h	ECC Error Bit Position. Indicates the bit position in the RAM data that is in error on an SEC error. Only valid on an SEC error.; 0 Bit 0 is in error; 1 Bit 1 is in error; 2 Bit 2 is in error; 3 Bit 3 is in error; ...; 31 Bit 31 is in error; >32 Invalid
15	CLR_CTRL_REG_ERRO R	R/W	0h	Writing a '1' clears the CTRL_REG_ERROR bit
14-13	CLR_PARITY_ERROR	R/WD	0h	Clear Parity Error. A write of a non-zero value to this bit field decrements the PARITY_ERROR bit field by the value provided.
12	CLR_ECC_OTHER	R/W	0h	Writing a '1' clears the ECC_OTHER bit.
11-10	CLR_ECC_DED	R/WD	0h	Clear ECC_DED. A write of a non-zero value to this bit field decrements the ECC_DED bit field by the value provided.
9-8	CLR_ECC_SEC	R/WD	0h	Clear ECC_SEC. A write of a non-zero value to this bit field decrements the ECC_SEC bit field by the value provided.
7	CTRL_REG_ERROR	R/W	0h	Control Register Error. A bit field in the control register is in an ambiguous state. This means that the redundancy registers have detected a state where not all values are the same and has defaulted to the reset state. S/W needs to re-write these registers to a known state. A write of 1 will set this interrupt flag.
6-5	PARITY_ERROR	R/WI	0h	Parity Error Status. A 2-bit saturating counter of the number of parity errors that have occurred since last cleared.; ; 0 No parity error detected; 1 One parity error was detected; 2 Two parity errors were detected; 3 Three parity errors were detected; ;A write of a non-zero value to this bit field increments it by the value provided.
4	ECC_OTHER	R/W	0h	SEC While Writeback Error Status; 0 No SEC error while writeback pending; 1 Indicates that successive single-bit errors have occurred while a writeback is still pending
3-2	ECC_DED	R/WI	0h	Double Bit Error Detected Status. A 2-bit saturating counter of the number of DED errors that have occurred since last cleared.; ; 0 No double-bit error detected; 1 One double-bit error was detected; 2 Two double-bit errors were detected; 3 Three double-bit errors were detected; ;A write of a non-zero value to this bit field increments it by the value provided.
1-0	ECC_SEC	R/WI	0h	Single Bit Error Corrected Status. A 2-bit saturating counter of the number of SEC errors that have occurred since last cleared.; ; 0 No single-bit error detected; 1 One single-bit error was detected and corrected; 2 Two single-bit errors were detected and corrected; 3 Three single-bit errors were detected and corrected; ;A write of a non-zero value to this bit field increments it by the value provided.

27.8.66 MCANERR_ERR_STAT2 Register (Offset = 424h) [Reset = 00000000h]

MCANERR_ERR_STAT2 is shown in Table 27-79.

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This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-79. MCANERR_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R	0h	Indicates the row address where the single or double-bit error occurred. This value is address offset/4.

27.8.67 MCANERR_ERR_STAT3 Register (Offset = 428h) [Reset = 00000000h]

MCANERR_ERR_STAT3 is shown in Table 27-80.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Table 27-80. MCANERR_ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	CLR_SVBUS_TIMEOUT	R-0/W	0h	Write 1 to clear the Serial VBUS Timeout Flag
8-2	RESERVED	R	0h	Reserved
1	SVBUS_TIMEOUT	R-0/W	0h	Serial VBUS Timeout Flag. Write 1 to set.
0	WB_PEND	R	0h	Delayed Write Back Pending Status; 0 No write back pending; 1 An ECC data correction write back is pending

27.8.68 MCANERR_SEC_EOI Register (Offset = 43Ch) [Reset = 00000000h]

MCANERR_SEC_EOI is shown in Table 27-81.

Return to the Summary Table.

MCAN Single Error Corrected End of Interrupt Register

Table 27-81. MCANERR_SEC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R-0/W	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host.; ;Note that a write to the MCANERR_ERR_STAT1.CLR_ECC_SEC goes through the SVBUS and has a delayed completion. To avoid an additional interrupt, read the MCANERR_ERR_STAT1 register back prior to writing to this bit field.

27.8.69 MCANERR_SEC_STATUS Register (Offset = 440h) [Reset = 00000000h]

MCANERR_SEC_STATUS is shown in Table 27-82.

Return to the Summary Table.

MCAN Single Error Corrected Interrupt Status Register

Table 27-82. MCANERR_SEC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGMEM_PEND	R-0/W	0h	Message RAM SEC Interrupt Pending; 0 No SEC interrupt is pending; 1 SEC interrupt is pending

27.8.70 MCANERR_SEC_ENABLE_SET Register (Offset = 480h) [Reset = 00000000h]

MCANERR_SEC_ENABLE_SET is shown in Table 27-83.

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MCAN Single Error Corrected Interrupt Enable Set Register

Table 27-83. MCANERR_SEC_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGMEM_ENABLE_SET	R/W	0h	Message RAM SEC Interrupt Pending Enable Set. Writing a 1 to this bit enables the Message RAM SEC error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

27.8.71 MCANERR_SEC_ENABLE_CLR Register (Offset = 4C0h) [Reset = 00000000h]

MCANERR_SEC_ENABLE_CLR is shown in Table 27-84.

Return to the Summary Table.

MCAN Single Error Corrected Interrupt Enable Clear Register

Table 27-84. MCANERR_SEC_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGMEM_ENABLE_CLR	R/W	0h	Message RAM SEC Interrupt Pending Enable Clear. Writing a 1 to this bit disables the Message RAM SEC error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

27.8.72 MCANERR_DED_EOI Register (Offset = 53Ch) [Reset = 00000000h]

MCANERR_DED_EOI is shown in Table 27-85.

Return to the Summary Table.

MCAN Double Error Detected End of Interrupt Register

Table 27-85. MCANERR_DED_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R-0/W	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host.; ;Note that a write to the MCANERR_ERR_STAT1.CLR_ECC_DED goes through the SVBUS and has a delayed completion. To avoid an additional interrupt, read the MCANERR_ERR_STAT1 register back prior to writing to this bit field.

27.8.73 MCANERR_DED_STATUS Register (Offset = 540h) [Reset = 00000000h]

MCANERR_DED_STATUS is shown in Table 27-86.

Return to the Summary Table.

MCAN Double Error Detected Interrupt Status Register

Table 27-86. MCANERR_DED_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGMEM_PEND	R-0/W	0h	Message RAM DED Interrupt Pending; 0 No DED interrupt is pending; 1 DED interrupt is pending

27.8.74 MCANERR_DED_ENABLE_SET Register (Offset = 580h) [Reset = 00000000h]

MCANERR_DED_ENABLE_SET is shown in Table 27-87.

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MCAN Double Error Detected Interrupt Enable Set Register

Table 27-87. MCANERR_DED_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGMEM_ENABLE_SET	R/W	0h	Message RAM DED Interrupt Pending Enable Set. Writing a 1 to this bit enables the Message RAM DED error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

27.8.75 MCANERR_DED_ENABLE_CLR Register (Offset = 5C0h) [Reset = 00000000h]

MCANERR_DED_ENABLE_CLR is shown in Table 27-88.

Return to the Summary Table.

MCAN Double Error Detected Interrupt Enable Clear Register

Table 27-88. MCANERR_DED_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MSGMEM_ENABLE_CLR	R/W	0h	Message RAM DED Interrupt Pending Enable Clear. Writing a 1 to this bit disables the Message RAM DED error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

27.8.76 MCANERR_AGGR_ENABLE_SET Register (Offset = 600h) [Reset = 00000000h]

MCANERR_AGGR_ENABLE_SET is shown in Table 27-89.

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MCAN Error Aggregator Enable Set Register

Table 27-89. MCANERR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	ENABLE_TIMEOUT_SET	R/W	0h	Write 1 to enable timeout errors. Reads return the corresponding enable bit's current value.
0	ENABLE_PARITY_SET	R/W	0h	Write 1 to enable parity errors. Reads return the corresponding enable bit's current value.

27.8.77 MCANERR_AGGR_ENABLE_CLR Register (Offset = 604h) [Reset = 00000000h]

MCANERR_AGGR_ENABLE_CLR is shown in Table 27-90.

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MCAN Error Aggregator Enable Clear Register

Table 27-90. MCANERR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	ENABLE_TIMEOUT_CLR	R/W	0h	Write 1 to disable timeout errors. Reads return the corresponding enable bit's current value.
0	ENABLE_PARITY_CLR	R/W	0h	Write 1 to disable parity errors. Reads return the corresponding enable bit's current value.

27.8.78 MCANERR_AGGR_STATUS_SET Register (Offset = 608h) [Reset = 00000000h]

MCANERR_AGGR_STATUS_SET is shown in Table 27-91.

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MCAN Error Aggregator Status Set Register

Table 27-91. MCANERR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	SVBUS_TIMEOUT	R/WI	0h	Aggregator Serial VBUS Timeout Error Status; ;2-bit saturating counter of the number of SVBUS timeout errors that have occurred since last cleared.; 0 No timeout errors have occurred; 1 One timeout error has occurred; 2 Two timeout errors have occurred; 3 Three timeout errors have occurred; ;A write of a non-zero value to this bit field increments it by the value provided.
1-0	AGGR_PARITY_ERR	R/WI	0h	Aggregator Parity Error Status; ;2-bit saturating counter of the number of parity errors that have occurred since last cleared.; 0 No parity errors have occurred; 1 One parity error has occurred; 2 Two parity errors have occurred; 3 Three parity errors have occurred; ;A write of a non-zero value to this bit field increments it by the value provided.

27.8.79 MCANERR_AGGR_STATUS_CLR Register (Offset = 60Ch) [Reset = 00000000h]

MCANERR_AGGR_STATUS_CLR is shown in Table 27-92.

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MCAN Error Aggregator Status Clear Register

Table 27-92. MCANERR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	SVBUS_TIMEOUT	R/WD	0h	Aggregator Serial VBUS Timeout Error Status; ;2-bit saturating counter of the number of SVBUS timeout errors that have occurred since last cleared.; 0 No timeout errors have occurred; 1 One timeout error has occurred; 2 Two timeout errors have occurred; 3 Three timeout errors have occurred; ;A write of a non-zero value to this bit field decrements it by the value provided.
1-0	AGGR_PARITY_ERR	R/WD	0h	Aggregator Parity Error Status; ;2-bit saturating counter of the number of parity errors that have occurred since last cleared.; 0 No parity errors have occurred; 1 One parity error has occurred; 2 Two parity errors have occurred; 3 Three parity errors have occurred; ;A write of a non-zero value to this bit field decrements it by the value provided.

27.8.80 DESC Register (Offset = 800h) [Reset = 00000000h]

DESC is shown in Table 27-93.

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Description;Shows module version and module ID

Table 27-93. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	C64Fh	Module identifier MODID[15:0]. Used to uniquely identify this IP.
15-12	STDIPOFF	R	0h	64 B standard IP MMR block (beginning with aggregated IRQ registers) ;0: STDIP MMRs do not exist;1:15: These MMRs begin at offset 64*STDIPOFF from IP base address
11-8	INSTIDX	R	0h	If multiple instances of IP exists in SOC, this field can identify the instance number 0-15
7-4	MAJREV	R	0h	Major revision of IP 0-15
3-0	MINREV	R	0h	Minor revision of IP 0-15 (typically revision is 1.0 for a verified new IP)

27.8.81 IMASK0 Register (Offset = 844h) [Reset = 00000000h]

IMASK0 is shown in Table 27-94.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 27-94. IMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	R/W	0h	DMA DONE channel 1 interrupt mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	DMA_DONE0	R/W	0h	DMA DONE channel 0 interrupt mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	FE2	R/W	0h	Filter event 2 interrupt mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	EXT_TS_OR_WAKE	R/W	0h	External Timestamp Counter Overflow interrupt mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	DED	R/W	0h	Message RAM DED interrupt mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SEC	R/W	0h	Message RAM SEC interrupt mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INTL1	R/W	0h	MCAN Interrupt Line1 mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	INTL0	R/W	0h	MCAN Interrupt Line 0 mask for MIS0. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

27.8.82 RIS0 Register (Offset = 848h) [Reset = 00000000h]

RIS0 is shown in Table 27-95.

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Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS0 register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 27-95. RIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	R	0h	Raw Interrupt Status for DMA Done interrupt of DMA channel1. 0h = Interrupt did not occur 1h = Interrupt occured
6	DMA_DONE0	R	0h	Raw Interrupt Status for DMA Done interrupt of DMA channel0. 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Raw Interrupt Status for Filter Event 2 interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
4	EXT_TS_OR_WAKE	R	0h	Raw Interrupt Status for External Timestamp Counter Overflow interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Raw Interrupt Status for Message RAM DED interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Raw Interrupt status for Message RAM SEC interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Raw Interrupt status for MCAN Interrupt Line 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Raw Interrupt status for MCAN Interrupt Line 0. 0h = Interrupt did not occur 1h = Interrupt occured

27.8.83 MIS0 Register (Offset = 84Ch) [Reset = 00000000h]

MIS0 is shown in Table 27-96.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 27-96. MIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	R	0h	Mask interrupt status for DMA DONE interrupt of DMA channel1. 0h = Interrupt did not occur 1h = Interrupt occured
6	DMA_DONE0	R	0h	Mask interrupt status for DMA DONE interrupt of DMA channel0. 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Masked Interrupt status for Filter event 2 interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
4	EXT_TS_OR_WAKE	R	0h	Masked Interrupt status for External Timestamp counter Overflow interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Masked Interrupt status for Message RAM DED interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Masked Interrupt status for Message RAM SEC interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Mask interrupt status for MCAN Interrupt Line 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Mask interrupt status for MCAN Interrupt Line 0. 0h = Interrupt did not occur 1h = Interrupt occured

27.8.84 ISET0 Register (Offset = 850h) [Reset = 00000000h]

ISET0 is shown in Table 27-97.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET0 will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 27-97. ISET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	W	0h	Sets DMA DONE for DMA channel 1 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
6	DMA_DONE0	W	0h	Sets DMA DONE for DMA channel 0 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
5	FE2	W	0h	Sets Filter event 2 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
4	EXT_TS_OR_WAKE	W	0h	Sets External Time stamp counter Overflow interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
3	DED	W	0h	Sets Message RAM DED interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
2	SEC	W	0h	Sets Message RAM SEC interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
1	INTL1	W	0h	Sets MCAN Interrupt Line 1 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt
0	INTL0	W	0h	Sets MCAN Interrupt Line 0 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Sets interrupt

27.8.85 ICLR0 Register (Offset = 854h) [Reset = 00000000h]

ICLR0 is shown in Table 27-98.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 27-98. ICLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	W	0h	Clears DMA DONE interrupt for DMA channel 1 in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
6	DMA_DONE0	W	0h	Clears DMA DONE interrupt for DMA channel 0 in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
5	FE2	W	0h	Clears Filter Event 2 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
4	EXT_TS_OR_WAKE	W	0h	Clears External Time stamp counter Overflow in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
3	DED	W	0h	Clears Message RAM DED interrupt in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
2	SEC	W	0h	Clears Message RAM SEC interrupt in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
1	INTL1	W	0h	Clears MCAN Interrupt Line 1 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event
0	INTL0	W	0h	Clears MCAN Interrupt Line 0 interrupt in RIS0. 0h = Writing 0 has no effect 1h = Clears the Event

27.8.86 DTB Register (Offset = 864h) [Reset = 00000000h]

DTB is shown in Table 27-99.

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Digital Test Bus. This register is used to bring out some internal signals of the peripheral on digital test bus (DTB).

Table 27-99. DTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	SEL	R/W	0h	This bit field is used to select DTB mux digital output signals. 0h = DTB output from peripheral is 0x0. 1h = Selects test group 1 2h = Selects test group 2 3h = Selects test group 3 4h = Selects test group 4 5h = Selects test group 5 6h = Selects test group 6 7h = Selects test group 7

27.8.87 IMASK1 Register (Offset = 868h) [Reset = 00000000h]

IMASK1 is shown in Table 27-100.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Table 27-100. IMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	R/W	0h	DMA DONE channel 1 interrupt mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
6	DMA_DONE0	R/W	0h	DMA DONE channel 0 interrupt mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
5	FE2	R/W	0h	Filter event 2 interrupt mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	EXT_TS_OR_WAKE	R/W	0h	External Timestamp Counter Overflow interrupt mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	DED	R/W	0h	Message RAM DED interrupt mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SEC	R/W	0h	Message RAM SEC interrupt mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INTL1	R/W	0h	MCAN Interrupt Line1 mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	INTL0	R/W	0h	MCAN Interrupt Line 0 mask for MIS1. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

27.8.88 RIS1 Register (Offset = 86Ch) [Reset = 00000000h]

RIS1 is shown in Table 27-101.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS0 register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 27-101. RIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	R	0h	Raw Interrupt Status for DMA Done interrupt of DMA channel1. 0h = Interrupt did not occur 1h = Interrupt occured
6	DMA_DONE0	R	0h	Raw Interrupt Status for DMA Done interrupt of DMA channel0. 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Raw Interrupt Status for Filter Event 2 interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
4	EXT_TS_OR_WAKE	R	0h	Raw Interrupt Status for External Timestamp Counter Overflow interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Raw Interrupt Status for Message RAM DED interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Raw Interrupt status for Message RAM SEC interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Raw Interrupt status for MCAN Interrupt Line 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Raw Interrupt status for MCAN Interrupt Line 0. 0h = Interrupt did not occur 1h = Interrupt occured

27.8.89 MIS1 Register (Offset = 870h) [Reset = 00000000h]

MIS1 is shown in Table 27-102.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 27-102. MIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	R	0h	Mask interrupt status for DMA DONE interrupt of DMA channel1. 0h = Interrupt did not occur 1h = Interrupt occured
6	DMA_DONE0	R	0h	Mask interrupt status for DMA DONE interrupt of DMA channel0. 0h = Interrupt did not occur 1h = Interrupt occured
5	FE2	R	0h	Masked Interrupt status for Filter event 2 interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
4	EXT_TS_OR_WAKE	R	0h	Masked Interrupt status for External Timestamp counter Overflow interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Masked Interrupt status for Message RAM DED interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Masked Interrupt status for Message RAM SEC interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Mask interrupt status for MCAN Interrupt Line 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Mask interrupt status for MCAN Interrupt Line 0. 0h = Interrupt did not occur 1h = Interrupt occured

27.8.90 ISET1 Register (Offset = 874h) [Reset = 00000000h]

ISET1 is shown in Table 27-103.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET0 will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Table 27-103. ISET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	W	0h	Sets DMA DONE for DMA channel 1 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
6	DMA_DONE0	W	0h	Sets DMA DONE for DMA channel 0 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
5	FE2	W	0h	Sets Filter event 2 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
4	EXT_TS_OR_WAKE	W	0h	Sets External Time stamp counter Overflow interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
3	DED	W	0h	Sets Message RAM DED interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
2	SEC	W	0h	Sets Message RAM SEC interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
1	INTL1	W	0h	Sets MCAN Interrupt Line 1 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt
0	INTL0	W	0h	Sets MCAN Interrupt Line 0 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Sets interrupt

27.8.91 ICLR1 Register (Offset = 878h) [Reset = 00000000h]

ICLR1 is shown in Table 27-104.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 27-104. ICLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DMA_DONE1	W	0h	Clears DMA DONE interrupt for DMA channel 1 in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
6	DMA_DONE0	W	0h	Clears DMA DONE interrupt for DMA channel 0 in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
5	FE2	W	0h	Clears Filter Event 2 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
4	EXT_TS_OR_WAKE	W	0h	Clears External Time stamp counter Overflow in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
3	DED	W	0h	Clears Message RAM DED interrupt in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
2	SEC	W	0h	Clears Message RAM SEC interrupt in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
1	INTL1	W	0h	Clears MCAN Interrupt Line 0 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event
0	INTL0	W	0h	Clears MCAN Interrupt Line 0 interrupt in RIS1. 0h = Writing 0 has no effect 1h = Clears the Event

27.8.92 MCANSS_CLKDIV Register (Offset = 904h) [Reset = 00000000h]

MCANSS_CLKDIV is shown in Table 27-105.

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Clock Divider. Configuring Clock divider setting for MCAN functional clock.

Table 27-105. MCANSS_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	RATIO	R/W	0h	Clock divide ratio specification. Enables configuring clock divide settings for the MCAN functional clock input to the MCAN-SS. 0h = Divides input clock by 1 1h = Divides input clock by 2 2h = Divides input clock by 4

27.8.93 MCANSS_CLKCTL Register (Offset = 908h) [Reset = 00000000h]

MCANSS_CLKCTL is shown in Table 27-106.

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MCANSS clock stop control MMR.

Table 27-106. MCANSS_CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	WKUP_GLTFLT_EN	R/W	0h	Setting this bit enables the glitch filter on MCAN RXD input, which wakes up the MCAN controller to exit clock gating. 0h = Disable glitch filter enable on RXD input when MCAN is in clock stop mode (waiting for event on RXD input for clock stop wakeup). 1h = Enable glitch filter enable on RXD input when MCAN is in clock stop mode (waiting for event on RXD input for clock stop wakeup).
7-5	RESERVED	R	0h	Reserved
4	WAKEUP_INT_EN	R/W	0h	This bit contols enabling or disabling the MCAN IP clock stop wakeup interrupt (when MCANSS_CTRL.WAKEUPREQEN wakeup request is enabled to wakeup MCAN IP upon CAN RXD activity) 0h = Disable MCAN IP clock stop wakeup interrupt 1h = Enable MCAN IP clock stop wakeup interrupt
3-1	RESERVED	R	0h	Reserved
0	STOPREQ	R/W	0h	This bit is used to enable/disable MCAN clock (both host clock and functional clock) gating request.;Note: This bit can be reset by HW by Clock-Stop Wake-up via CAN RX Activity. 0h = Disable MCAN-SS clock stop request 1h = Enable MCAN-SS clock stop request

27.8.94 MCANSS_CLKSTS Register (Offset = 90Ch) [Reset = 00000000h]

MCANSS_CLKSTS is shown in Table 27-107.

Return to the Summary Table.

MCANSS clock stop status register to indicate status of clock stop mechanism

Table 27-107. MCANSS_CLKSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	STOPREQ_HW_OVR	R	0h	MCANSS clock stop HW override status bit. ;This bit indicates when the MCANSS_CLKCTL.STOPREQ bit has been cleared by HW when a clock-stop wake-up event via CAN RX activity is trigged. 0h = MCANSS_CLKCTL.STOPREQ bit has not been cleared by HW. 1h = MCANSS_CLKCTL.STOPREQ bit has been cleared by HW.
3-1	RESERVED	R	0h	Reserved
0	CLKSTOP_ACKSTS	R	0h	Clock stop acknowledge status from MCAN IP 0h = No clock stop acknowledged. 1h = MCAN-SS may be clock gated by stopping both the CAN host and functional clocks.

27.8.95 MCANSS_DMA0_CTL Register (Offset = 924h) [Reset = 00000000h]

MCANSS_DMA0_CTL is shown in Table 27-108.

Return to the Summary Table.

MCANSS fixed DMA0 control and configuration register

Table 27-108. MCANSS_DMA0_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RX_BUF_TTO_OFFST	R/W	0h	Indicates the Rx-buffer (index x) to be mapped to FE_0 (FE001) and automatically maps and Rx buffer (index x+1) to FE_1 (FE010);Valid range: Rxbuffer (0) to Rxbuffer (30) 0h = Minimum index value: 0 1Eh = Maximum index value: 30;Note: RX_FE_TTO_SEL Rx buffer index selection for FE01 cannot be 31, as Rxbuffer (index +1) maps to 32, which requires updating NDAT1 and NDAT2 value, which is not supported.
26-25	RESERVED	R	0h	Reserved
24	RX_FE_OTO_SEL	R/W	0h	RX_FE_OTO_SEL is used to select the MCAN RX buffer filter event signal mapped to trigger fixed MCANSS DMA channel trigger 0h = Filter Event 0 1h = Filter Event 1
23-22	RESERVED	R	0h	Reserved
21-16	TX_BRP_MTO_NUM	R/W	2h	Number of TX buffer request pending (BRP) signals for multi-to-one DMA trigger mapping sequence, starting from the buffer offset number selected by TX_BRP_MTO_OFFST bits 2h = Min number for TX BRP multi-to-one DMA trigger mapping sequence is 2 20h = Max number for TX BRP multi-to-one DMA trigger mapping sequence is 32
15	RESERVED	R	0h	Reserved

Table 27-108. MCANSS_DMA0_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-10	TX_BRP_MTO_OFFST	R/W	0h	TX_BRP_MTO_OFFST selects the Tx buffer offset number for the multi-to-one round robin DMA trigger mode. 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
9	RESERVED	R	0h	Reserved

Table 27-108. MCANSS_DMA0_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-4	TX_BRP_OTO_SEL	R/W	0h	TX_BRP_OTO_SEL is used to select the MCAN TX buffer request pending (BRP) signal mapped to trigger fixed MCANSS DMA channel trigger 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
3-2	DMA_TRIG_SEL	R/W	0h	DMA trigger select bits used to select between MCAN TX one-to-one mapping, MCAN TX multi-to-one round robin mapping and MCAN Rx one-to-one mapping options 0h = MCAN TX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 1h = MCAN TX Buffer multi-to-one round robin, Tx BRP (buffer request pending) triggers to DMA channel select 2h = MCAN RX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 3h = Rx buffer two-to-one DMA trigger
1	RESERVED	R	0h	Reserved
0	DMA_TRIG_EN	R/W	0h	DMA_TRIG_EN is used to enable/disable MCAN RX, TX triggers to MCANSS fixed DMA channel. ;<Note to design> check if this bit is needed depending on if similar functionality is enabled in the EXT_DMA aperture. 0h = MCANSS fixed DMA channel trigger is disabled. 1h = MCANSS fixed DMA channel trigger is enabled.

27.8.96 MCANSS_DMA1_CTL Register (Offset = 92Ch) [Reset = 00000000h]

MCANSS_DMA1_CTL is shown in Table 27-109.

Return to the Summary Table.

MCANSS fixed DMA1 control and configuration register

Table 27-109. MCANSS_DMA1_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RX_BUF_TTO_OFFST	R/W	0h	Indicates the Rx-buffer (index x) to be mapped to FE_0 (FE001) and automatically maps and Rx buffer (index x+1) to FE_1 (FE010);Valid range: Rxbuffer (0) to Rxbuffer (30) 0h = Minimum index value: 0 1Eh = Maximum index value: 30;Note: RX_FE_TTO_SEL Rx buffer index selection for FE01 cannot be 31, as Rxbuffer (index +1) maps to 32, which requires updating NDAT1 and NDAT2 value, which is not supported.
26-25	RESERVED	R	0h	Reserved
24	RX_FE_OTO_SEL	R/W	0h	RX_FE_OTO_SEL is used to select the MCAN RX buffer filter event signal mapped to trigger fixed MCANSS DMA channel trigger 0h = Filter Event 0 1h = Filter Event 1
23-22	RESERVED	R	0h	Reserved
21-16	TX_BRP_MTO_NUM	R/W	2h	Number of TX buffer request pending (BRP) signals for multi-to-one DMA trigger mapping sequence, starting from the buffer offset number selected by TX_BRP_MTO_OFFST bits 2h = Min number for TX BRP multi-to-one DMA trigger mapping sequence is 2 20h = Max number for TX BRP multi-to-one DMA trigger mapping sequence is 32
15	RESERVED	R	0h	Reserved

Table 27-109. MCANSS_DMA1_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-10	TX_BRP_MTO_OFFST	R/W	0h	TX_BRP_MTO_OFFST selects the Tx buffer offset number for the multi-to-one round robin DMA trigger mode. 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
9	RESERVED	R	0h	Reserved

Table 27-109. MCANSS_DMA1_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-4	TX_BRP_OTO_SEL	R/W	0h	TX_BRP_OTO_SEL is used to select the MCAN TX buffer request pending (BRP) signal mapped to trigger fixed MCANSS DMA channel trigger 0h = TX Buffer Request Pending 0 1h = TX Buffer Request Pending 1 2h = TX Buffer Request Pending 2 3h = TX Buffer Request Pending 3 4h = TX Buffer Request Pending 4 5h = TX Buffer Request Pending 5 6h = TX Buffer Request Pending 6 7h = TX Buffer Request Pending 7 8h = TX Buffer Request Pending 8 9h = TX Buffer Request Pending 9 Ah = TX Buffer Request Pending 10 Bh = TX Buffer Request Pending 11 Ch = TX Buffer Request Pending 12 Dh = TX Buffer Request Pending 13 Eh = TX Buffer Request Pending 14 Fh = TX Buffer Request Pending 15 10h = TX Buffer Request Pending 16 11h = TX Buffer Request Pending 17 12h = TX Buffer Request Pending 18 13h = TX Buffer Request Pending 19 14h = TX Buffer Request Pending 20 15h = TX Buffer Request Pending 21 16h = TX Buffer Request Pending 22 17h = TX Buffer Request Pending 23 18h = TX Buffer Request Pending 24 19h = TX Buffer Request Pending 25 1Ah = TX Buffer Request Pending 26 1Bh = TX Buffer Request Pending 27 1Ch = TX Buffer Request Pending 28 1Dh = TX Buffer Request Pending 29 1Eh = TX Buffer Request Pending 30 1Fh = TX Buffer Request Pending 31
3-2	DMA_TRIG_SEL	R/W	0h	DMA trigger select bits used to select between MCAN TX one-to-one mapping, MCAN TX multi-to-one round robin mapping and MCAN Rx one-to-one mapping options 0h = MCAN TX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 1h = MCAN TX Buffer multi-to-one round robin Tx BRP (buffer request pending) triggers to DMA channel select 2h = MCAN RX Buffer one-to-one Tx BRP (buffer request pending) trigger to DMA channel select 3h = Rx buffer two-to-one DMA trigger
1	RESERVED	R	0h	Reserved
0	DMA_TRIG_EN	R/W	0h	DMA_TRIG_EN is used to enable/disable MCAN RX, TX triggers to MCANSS fixed DMA channel. ;<Note to design> check if this bit is needed depending on if similar functionality is enabled in the EXT_DMA aperture. 0h = MCANSS fixed DMA channel trigger is disabled. 1h = MCANSS fixed DMA channel trigger is enabled.

27.8.97 RXDMA_TTO_FE0_BA Register (Offset = 938h) [Reset = 00000000h]

RXDMA_TTO_FE0_BA is shown in Table 27-110.

Return to the Summary Table.

Rx buffer (index x) base address. ;<Internal: Absolute address within MCAN IP: 0x7938>;Applicable to Rx buffer DMA two-to-one mode mapped to FE001 trigger: ;>> LS bits 0:1 in this MMR are reserved and read as '0' as the MCAN SRAM is 4 byte data addressable. ;>> Index x is selected using MCANSS_DMAn_CTL.RX_FE_TTO_SEL bits.

Table 27-110. RXDMA_TTO_FE0_BA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-2	BASE_ADDR	R/W	0h	FE0 Rx Buf x Base adddress (14:2). ;Address should be compited based on the 14-bit RBSA (Rx buffer start address) + offset (depending on Rx buffer element index value and data length code (DLC) for all the buffer elements before the Rx buffer element (x)) 0h = Min address offset within MCANSS SRAM: 0x0 1FFFh = Max address offset within MCANSS SRAM: 0x1fff
1-0	RESERVED	R	0h	Reserved

27.8.98 RXDMA_TTO_FE1_BA Register (Offset = 948h) [Reset = 00000000h]

RXDMA_TTO_FE1_BA is shown in Table 27-111.

Return to the Summary Table.

Rx buffer (index x+1) base address;<Internal: Absolute address within MCAN IP: 0x7948>;Applicable to Rx buffer DMA two-to-one mode mapped to FE010 trigger: ;>> LS bits 0:1 in this MMR are reserved and read as '0' as the MCAN SRAM is 4 byte data addressable. ;>> Index x is selected using MCANSS_DMAn_CTL.RX_FE_TTO_SEL bits.

Table 27-111. RXDMA_TTO_FE1_BA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-2	BASE_ADDR	R/W	0h	FE010 Rx Buf x Base adddress (14:2). ;Address should be compited based on the 14-bit RBSA (Rx buffer start address) + offset (depending on Rx buffer element index value and data length code (DLC) for all the buffer elements before the Rx buffer element (x+1)) 0h = Min address offset within MCANSS SRAM: 0x0 1FFFh = Max address offset within MCANSS SRAM: 0x1fff
1-0	RESERVED	R	0h	Reserved

27.8.99 RXDMA_TTO_NDAT1 Register (Offset = 950h) [Reset = 00000000h]

RXDMA_TTO_NDAT1 is shown in Table 27-112.

Return to the Summary Table.

Rx Buffer two-to-one DMA mode, hardware NDAT1 value register. ;The address of this register is programmed as the DMA source address register for moving NDAT1 value during DMA operation. ;This register is automatically updated on the fly depending on FE001/FE010 (Rxbuf(x)/Rxbuf(x+1)) ongoing transfer.

Table 27-112. RXDMA_TTO_NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NDAT1_VAL	R	0h	NDAT1 value to be programmed onto MCAN.NDAT1 MMR. ;Automatically updated by HW. 0h = Min value = 0x0 (not bits set) 80000000h = max value = (bit 31 set) = 0x80000000

Chapter 28
Radio

This section describes the operation of the 2.4 GHz radio.

28.1 Introduction

The 2.4 GHz radio supports several formats. The radio provides significant baseband automation such as analog radio control, modulation, demodulation, address checking, CRC-calculation and checking. The customer application interfaces with the radio through RCL (Radio Control Layer), which is a software layer provided in the SimpleLink Low Power F3 Software Development Kit (SDK), and documented in the SDK. Alternatively, the customer application interfaces with the TI provided stack (Bluetooth® Low Energy or IEEE), and the stack then uses the RCL to interface with the radio. The documentation provided here is to give an overview of the radio structure and usage model.

28.2 Block Diagram

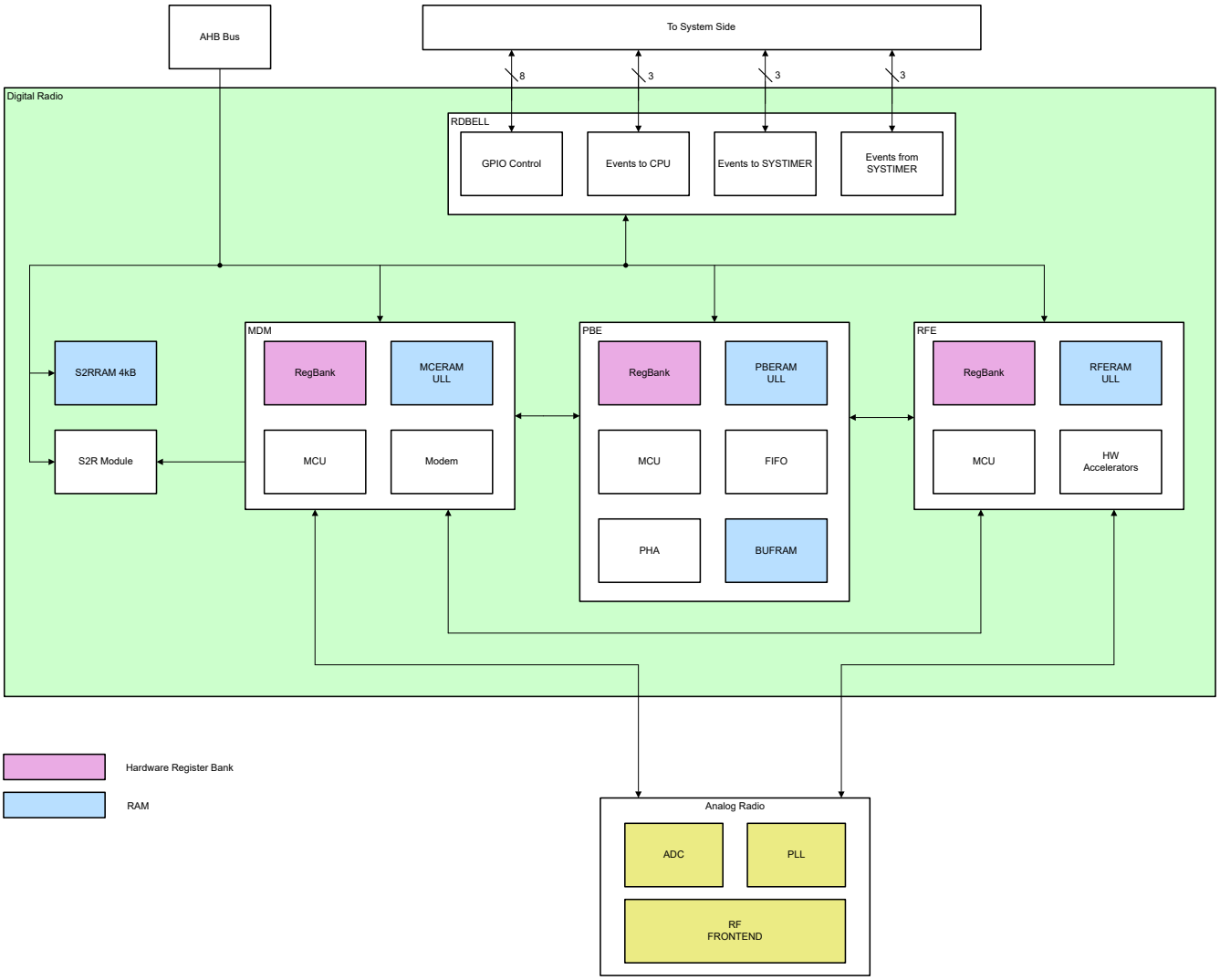

Figure 28-1. Radio Block Diagram

28.3 Overview

28.3.1 Radio Sub-domains

The digital part of the radio consists of three main sub-domains: Modem (MDM), Packet Build Engine (PBE), and RF Engine (RFE). Each of these sub-domains have their own internal processor and program memories for storing FW images (MCERAM, PBERAM, RFERAM). They also have separate register blocks for configuration of HW and various HW accelerators. The different sub domains have different responsibilities:

Modem (MDM)

The MDM domain is responsible for:

- Conversion from information/data bits to TX-symbols including:
  - Preamble and sync word insertion
  - Direct Sequence Spread Spectrum (DSSS)
  - Forward Error Correction (FEC) encoding
- Demodulation including:
  - Timing recovery
  - Frequency offset estimation/compensation
  - Rate offset estimation/compensation
  - FEC decoding

Packet build engine (PBE)

The PBE domain is responsible for:

- Packet timing
- Composition and de-composition of radio packets
- FIFO handling
- Packet Handling Accelerator (PHA) for CRC and whitening
- Address checking

RF Engine (RFE)

The RFE domain is responsible for:

- Sequencing of analog modules
- PLL calibration algorithm
- Modulation/Shaping of the transmitted data
- Received Signal Strength Indication (RSSI) estimation
- Automatic Gain Control (AGC) algorithms

28.3.2 Radio RAMs

The RAMs marked with ULL in Figure 28-1, which are used for storing firmware images, have ultra low leakage (ULL). ULL supports low power consumption while retaining the contents of these memories when entering standby. This avoids having to reprogram the firmware images after each standby. The other memories (S2RRAM, BUFRAM) have higher leakage and the power consumption of having retention on these in standby is higher. The S2RRAM is reserved for future use, and the BUFRAM is used for data that usually have a short lifespan, so retaining the contents of these is not necessary.

Note

The Samples-to-RAM (S2R) module and S2RRAM are reserved for future use by RCL. Do not use S2RRAM as this can conflict with future features.

28.3.3 Doorbell (DBELL)

The DBELL module has clock control registers, GPIO signals to and from the radio, and also controls events to and from the system side. This chapter gives an overview, see the LRFDDBELL register descriptions for details.

28.3.3.1 Interrupts

The radio has three interrupts to the system side. Each of the interrupts have the same 32 possible sources internally in the radio. Settings in the interrupt mask registers LRFDDBELL.IMASK ***n*** are used to configure the radio internal events to be the trigger sources for the three individual interrupts.. The raw state of the internal interrupt sources can be read from LRFDDBELL.RIS ***n*** , and the masked interrupt source status can be read

from LRFDDBELL.MIS ***n*** . If any of the bits in the LRFDDBELL.MIS ***n*** registers are set then the corresponding interrupt line to the system side is triggered. To clear the interrupt source, set the corresponding bit in the LRFDDBELL.ICLR ***n*** register. An internal interrupt source flag can be set by setting the corresponding bit in the LRFDDBELL:ISET ***n*** register.

28.3.3.2 GPIO Control

The radio has 8 general purpose outputs (GPO) and 8 general purpose inputs (GPI). Each of the eight individual output lines can be independently configured to output various internal signals. The selection of output source is done in the LRFDDBELL:GPOSEL0 and LRFDDBELL:GPOSEL1 registers. The GPO signals originating in MDM, PBE and RFE are all fully firmware driven. Different use cases have different features mapped to the GPO. Uses for the GPO include control of external switches, LNAs, PAs, and handshaking with other devices. Any control of GPO is documented in the SDK.

The GPI lines are all routed to the MDM, PBE, and RFE for use by the processors in these sub-domains.

28.3.3.3 SYSTIM Interface

There are three SYSTIM channels assigned to the radio. The radio receives compare events from the SYSTIM which are routed to the MDM, PBE, and RFE. These are used to trigger time start or stop commands. The radio can also be configured to output capture events to the SYSTIM, the selection of what event triggers the SYSTIM capture is done in the LRFDDBELL.SYSTIMOEV register. The normal use case is that RCL sets up and uses the SYSTIM interface.

If the radio is not in use (or not using SYSTIM interface), SYSTIM capture events can be captured from software by writing to the LRFDDBELL.SYSTDMATRIG register.

28.4 Radio Usage Model

The RCL automates the low-level operation of the radio for the user, but a description of the usage model is included here for reference. The behavior of the radio is to a large degree firmware defined. The description in this section describes the typical usage model, but other usage models are possible. Before any radio operation can be attempted the radio needs to be configured, this includes:

- Enable the necessary clocks
- Write the firmware images to the radio internal RAMs
- Configure hardware registers
- Apply device specific trims

The configuration is considered static, and does not need to change when changing RF frequency, switching between TX and RX, etc. The configurations for different PHYs can be exported from SmartRF™ Studio, a Windows application that helps in generation of the RF configuration register values and commands, as well as practical testing and debugging of the RF system. A set of predefined configurations for PHYs that are documented in the data sheet are available, and these configurations can be modified in SmartRF Studio to fit the use case. The PHY cannot be changed at run time.

After the radio has been configured, the RCL sends an API command to the PBE. Any parameters that change depending on frequency, role, and packet contents are passed as command parameters. These parameters are setup in the BUFRAM and various HW registers, the FIFO is populated if needed, and then the API command ID is passed to the PBE.

The PBE then uses the command ID and the command parameters and does further sequencing with the MDM and RFE. As the command executes, the radio generates data, events and interrupts that can be used by the rest of the system. Once the command finishes execution, the MCE and RFE report that they are done to the PBE, and then the PBE signals to the system side that the command is completed.

28.4.1 CRC and Whitening

Many proprietary radio systems require a specific CRC and/or whitening algorithm. This is done through the static configuration which can be exported from SmartRF™ Studio. The registers and fields in the following description can only be manipulated with SmartRF Studio. However to be able to configure the relevant registers

correctly a detailed explanation of the implementation is included here for reference. The CRC and whitening are done using the Packet Handling Accelerator (PHA). The PHA is implemented as linear-feedback shift registers (LFSRs) with programmable polynomials.

LFSR sub-engine

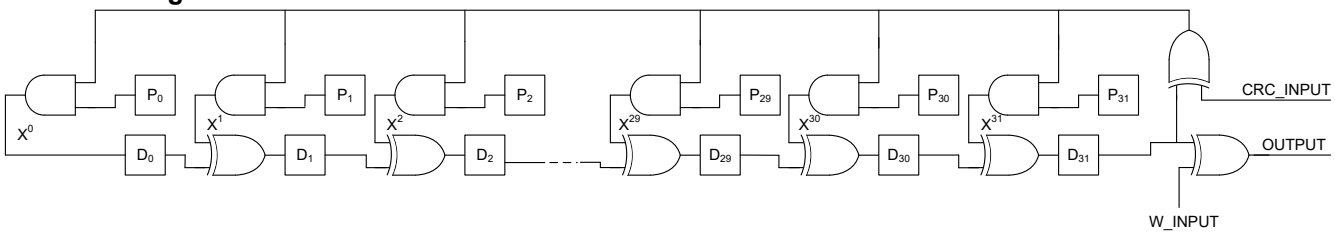

Figure 28-2. LFSR Logic

There are 2 LSFR cores, numbered 0 and 1. In the description below, the value *k* is used to identify the core. Each LSFR core consists of two 32-bit registers: One is the 32-bit polynomial POLY*k*[31:0], identified as p0–p31 in Figure 28-2; POLY*k*[*n*] corresponds to p*n*. The other is the 32-bit value register LFSR*k*VAL[31:0], identified as d0–d31 in Figure 28-2; LFSR*k*VAL[*n*] corresponds to d*n*.

The LFSR0 core can be in CRC mode or whitener mode. LFSR1 can only be in CRC mode. The mode of LFSR0 is selected through the PHACFG MODE0 bit.

An LFSR core is assumed to be operated in a bit-serial way. For each new bit, the shift register d0–d31 is clocked once as shown in the block diagram above. In CRC mode, the *crc_input* line corresponds to the bit that is entered, while output is ignored so that *w_input* is don't-care. In whitener mode, *w_input* corresponds to the bit that is entered, while *crc_input* is always 0. The polynomial register p0–p31 defines where there are taps in the shift register. A C equivalent of the operation is given below:

LFSR pseudocode

```
int j, fb;

fb = crc_input ^ LFSRVAL[31];                          /* feedback */

for (j = 31; j >= 1; j--)
{
    LFSRVAL[j] = LFSRVAL[j-1] ^ (fb & POLY[j]);    /* LFSRVAL[j-1] XOR (fb AND POLY[j]) */
}

LFSRVAL[0] = fb & POLY[0];                          /* fb AND POLY[0] */

output = w_input ^ fb;                                 /* w_input XOR fb */
```

Combination of two LFSRs

Two LFSRs can be run in parallel or in a chain. This is configured through the bits PHACFG[0:1] MODE1 bit field. If MODE1[1:0] is 00, the operation of LFSR 0 and LFSR 1 shall be independent.

If MODE*1*[1:0] is 01, the output of LFSR0 shall be input to LFSR1 in addition to the output register, and LFSR1 shall be clocked whenever a bit is output from LFSR0. This mode is only allowed when LFSR0 is in whitener mode.

If MODE*1*[1:0] is 10, the input to LFSR0 shall also be input to LFSR1, and the both these LFSR cores shall be clocked whenever a bit is input to LFSR0. This mode is allowed regardless of the mode of LFSR0.

CRC and whitening usage scenarios

This section describes how the PHA can be configured to implement certain common CRC and whitening schemes.

CRC

The PHA can support any CRC up to 32 bits. A 32-bit CRC polynomial can be described by the polynomial $x^{32} + a_{31} x^{31} + \ldots + a_1 x^1 + 1$, where all *an* are 0 or 1. To represent this, each POLY*k*[*n*] bit in the register POLY*k* are set to *an*, and POLY*k* [0] is set to 1. For a polynomial of order *m*, described by $x^m + a_{m-1} x^{m-1} + \ldots + a_1 x^1 + 1$, POLY*k*[32−*m*+*n*] are set to *an*, for all *n*=1..*m*−1, POLY*k*[32−*m*] are set to 1, and POLY*k*[31−*m*:0] are set to all zeros.

Together with the polynomial the start state of the LFSR also needs to be defined. This is done through RCL, see SDK documentation for details. Bit ordering through the CRC calculation is also handled by the radio firmware, and is controlled through the RCL.

Some CRCs used in different systems

Table 28-1.

System	Bit ordering	CRC	POLY*k*[31:0]	Initialization of LFSR*k*[31:0]
nRF24L01+ 8-bit CRC	msb first	CRC-8-ATM $x^8 + x^2 + x + 1$	0x0700 0000	0xFF00 0000
CC85xx (first CRC byte)	msb first	CRC-8-CCITT $x^8 + x^7 + x^3 + x^2 + 1$	0x8D00 0000	0xFF00 0000
NextGen (CC2500 etc.)	msb first	CRC-16 $x^{16} + x^{15} + x^2 + 1$	0x8005 0000	0xFFFF 0000
CC2525;CC85xx (last part of CRC);nRF24L01+ 16-bit CRC	msb first	CRC-16-CCITT $x^{16} + x^{12} + x^5 + 1$	0x1021 0000	0xFFFF 0000
IEEE 802.15.4 [7]	lsb first	CRC-16-CCITT $x^{16} + x^{12} + x^5 + 1$	0x1021 0000	0x0000 0000
BLE [6]	lsb first	CRC-24-BLE $x^{24} + x^{10} + x^9 + x^6 + x^4 + x^3 + x + 1$	0x0006 5B00	0x5555 5500 (on advertising channels)
		CRC-32-IEEE 802.3 $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	0x04C1 1DB7	0xFFFF FFFF (for example)

Whitening

Each LFSR can be used to generate pseudo-random bit sequences, LFSR0 which supports whitener mode can collect the output in a vector. The LFSR supports generator polynomials up to order 32. A 32-bit generator polynomial can be described by the equation $x^{32} + a_{31} x^{31} + \ldots + a_1 x^1 + 1$, where all a_n are 0 or 1.
To represent this, each POLY*k*[*n*] bit in the register POLY*k* is set to *an*, and POLY*k*[0] is be set to 1. For a polynomial of order *m*, described by $x^m + a_{m-1} x^{m-1} + \ldots + a_1 x^1 + 1$, POLY*k* [32−*m*+*n*] are set to *an*, for all *n*=1..*m*−1, POLY*k*[32−*m*] are set to 1, and POLY*k*[32−*m*:0] are set to all zeros.

In whitener mode, the output of the shift register is XORed with the input bit sequence.

The LFSRs use a Galois structure. Many whitening specifications assume a Fibonacci structure. These are equivalent, but the initialization value for the shift registers must be different to get the same start point of the

sequence. The whitener initialization state is handled by the radio firmware, see the SDK documentation for details.

Whitener examples

In Bluetooth Low Energy, a whitener with polynomial $x^7 + x^4 + 1$ is specified. The whitener is specified with a Galois structure and with an initialization as follows:

Position 0 is set to one.

Positions 1 to 6 are set to the channel index of the channel used when transmitting or receiving, from the most significant bit in position 1 to the least significant bit in position 6.

This whitening scheme can be obtained by setting POLY*k* to 0x22000000 and initializing the register by writing the channel index OR'ed by 0x40 into LFSR*k*BR.

28.5 LRFDDBELL Registers

Table 28-2 lists the memory-mapped registers for the LRFDDBELL registers. All register offset addresses not listed in Table 28-2 should be considered as reserved locations and the register contents should not be modified.

Table 28-2. LRFDDBELL Registers

Offset	Acronym	Register Name	Section
0h	DESC	This register identifies the peripheral and its exact version.	Section 28.5.1
4h	CLKCTL	Clock control	Section 28.5.2
8h	DMACFG	DMA Configuration	Section 28.5.3
Ch	SYSTIMOEV	Controls routing of internal events to the three systimer output events	Section 28.5.4
10h	SYSTDMATRIG	Manual trigging of systimer capture event	Section 28.5.5
14h	GPOSEL0	GPO control	Section 28.5.6
18h	GPOSEL1	GPO control	Section 28.5.7
44h	IMASK0	Interrupt mask	Section 28.5.8
48h	RIS0	Raw interrupt status	Section 28.5.9
4Ch	MIS0	Masked interrupt status	Section 28.5.10
50h	ISET0	Interrupt set	Section 28.5.11
54h	ICLR0	Interrupt clear	Section 28.5.12
84h	IMASK1	Interrupt mask	Section 28.5.13
88h	RIS1	Raw interrupt status	Section 28.5.14
8Ch	MIS1	Masked interrupt status	Section 28.5.15
90h	ISET1	Interrupt set	Section 28.5.16
94h	ICLR1	Interrupt clear	Section 28.5.17
C4h	IMASK2	Interrupt mask	Section 28.5.18
C8h	RIS2	Raw interrupt status	Section 28.5.19
CCh	MIS2	Masked interrupt status	Section 28.5.20
D0h	ISET2	Interrupt set	Section 28.5.21
D4h	ICLR2	Interrupt clear	Section 28.5.22

Complex bit access types are encoded to fit into small table cells. Table 28-3 shows the codes that are used for access types in this section.

Table 28-3. LRFDDBELL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.5.1 DESC Register (Offset = 0h) [Reset = 00000000h]

DESC is shown in Table 28-4.

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Description.;This register identifies the peripheral and its exact version.

Table 28-4. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	141h	Module identifier used to uniquely identify this IP.
15-12	STDIPOFF	R	1h	Standard IP MMR block offset. Standard IP MMRs are the set of from aggregated IRQ registers till DTB. 0h = STDIP MMRs do not exist 1h = These MMRs begin at offset 64*STDIPOFF from IP base address
11-8	INSTNUM	R	0h	IP Instance Number. If multiple instances of IP exist in the device, this field can identify the instance number
7-4	MAJREV	R	1h	Major rev of the IP
3-0	MINREV	R	0h	Minor rev of the IP

28.5.2 CLKCTL Register (Offset = 4h) [Reset = 00000000h]

CLKCTL is shown in Table 28-5.

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Systimer Output Event Control Register.;Controls the functional clock gates for the individual sub-modules.

Table 28-5. CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	IQRAM	R/W	0h	Enable the clock to the demodulator 0h = The bit is 0 1h = The bit is 1
13	DEM	R/W	0h	Enable the clock to the demodulator. The modem will request this clock automatically. This bit is to force the clock to be free running 0h = Clock not requested 1h = Clock is requested
12	MOD	R/W	0h	Enable the clock to the modulator. Modem will request this clock automatically, this bit is to force the modulator clock to be free running. 0h = Clock not requested 1h = Clock is requested
11	S2RRAM	R/W	0h	Enable the clock to the S2R RAM 0h = Clock not requested 1h = The bit is 1
10	BUFRAM	R/W	0h	Enable the clock to the BUFRAM 0h = Clock not requested 1h = Clock is requested
9	DSBRAM	R/W	0h	Enable the clock to the DSB RAM 0h = Clock not requested 1h = Clock is requested
8	RFERAM	R/W	0h	Enable the clock to the RFE RAM 0h = Clock not requested 1h = Clock is requested
7	MCERAM	R/W	0h	Enable the clock to the MCE RAM 0h = Clock not requested 1h = Clock is requested
6	PBERAM	R/W	0h	Enable the clock to the PBE RAM 0h = Clock not requested 1h = Clock is requested
5	TRC	R/W	0h	Enable the clock to the Tracer 0h = Clock not requested 1h = Clock is requested
4	S2R	R/W	0h	Enable the clock to Samples2RAM 0h = Clock not requested 1h = Clock is requested
3	RFE	R/W	0h	Enable the clock to the RFE 0h = Clock not requested 1h = Clock is requested
2	MDM	R/W	0h	Enable the clock to the Modem 0h = Clock not requested 1h = Clock is requested
1	PBE	R/W	0h	Enable the clock to the PBE 0h = Clock not requested 1h = Clock is requested
0	BRIDGE	R/W	1h	Clock enable to AHB bridge. The bridge will request it's own clock, this bit it to override that feature to have a free running clock. 0h = Clock not requested 1h = Clock is requested

28.5.3 DMACFG Register (Offset = 8h) [Reset = 00000000h]

DMACFG is shown in Table 28-6.

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DMA Configuration

Table 28-6. DMACFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-1	TRIGSRC	R/W	0h	Select DMA trigger source 0h = The DMA is triggered by the PBE FW trigger 1h = The DMA is triggered by the MCE FW trigger 2h = The DMA is triggered by the MCE FW trigger 3h = The DMA is triggered from the FIFO. See the FIFO configration register for what FIFO event will generate the trigger
0	EN	R/W	0h	Enables the DMA interface 0h = Disable DMA interface, no activity on interface 1h = Enable DMA interface. The triggers are able to give activity on the interface

28.5.4 SYSTIMOEV Register (Offset = Ch) [Reset = 00000000h]

SYSTIMOEV is shown in Table 28-7.

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Systimer Output Event Control Register. Controls routing of internal events to the three systimer output events

Table 28-7. SYSTIMOEV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	SRC2	R/W	0h	Select source of systimer output event 2 (capture source) 0h = Output not enabled, always 0. 1h = RFE FW systimer capture event 0 2h = RFE FW systimer capture event 1 3h = RFE FW systimer capture event 2 4h = MCE FW systimer capture event 0 5h = MCE FW systimer capture event 1 6h = MCE FW systimer capture event 2 7h = MDM HW event 0 8h = MDM HW event 1 9h = MDM HW event 2 Ah = PBE FW systimer capture event 0 Bh = PBE FW systimer capture event 1 Ch = PBE FW systimer capture event 2
7-4	SRC1	R/W	0h	Select source of systimer output event 1 (capture source) 0h = Output not enabled, always 0. 1h = RFE FW systimer capture event 0 2h = RFE FW systimer capture event 1 3h = RFE FW systimer capture event 2 4h = MCE FW systimer capture event 0 5h = MCE FW systimer capture event 1 6h = MCE FW systimer capture event 2 7h = MDM HW event 0 8h = MDM HW event 1 9h = MDM HW event 2 Ah = PBE FW systimer capture event 0 Bh = PBE FW systimer capture event 1 Ch = PBE FW systimer capture event 2
3-0	SRC0	R/W	0h	Select source of systimer output event 0 (capture source) 0h = Output not enabled, always 0. 1h = RFE FW systimer capture event 0 2h = RFE FW systimer capture event 1 3h = RFE FW systimer capture event 2 4h = MCE FW systimer capture event 0 5h = MCE FW systimer capture event 1 6h = MCE FW systimer capture event 2 7h = MDM HW event 0 8h = MDM HW event 1 9h = MDM HW event 2 Ah = PBE FW systimer capture event 0 Bh = PBE FW systimer capture event 1 Ch = PBE FW systimer capture event 2

28.5.5 SYSTDMATRIG Register (Offset = 10h) [Reset = 00000000h]

SYSTDMATRIG is shown in Table 28-8.

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System DMA Trigger.;Manual triggering of systimer capture event or DMA trigger;This comes on top of any HW driven sources configured in SYSTIMOEV

Table 28-8. SYSTDMATRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	DMA	W	0h	Trigger a DMA request from the Radio 0h = DMA not manually triggered 1h = DMA request manually triggered
2	SYST2	W	0h	Trigger a capture event on systimer event 0 from the radio 0h = Not capture event triggered 1h = Capture event triggered
1	SYST1	W	0h	Trigger a capture event on systimer event 0 from the radio 0h = Not capture event triggered 1h = Capture event triggered
0	SYST0	W	0h	Trigger a capture event on systimer event 0 from the radio 0h = Not capture event triggered 1h = Capture event triggered

28.5.6 GPOSEL0 Register (Offset = 14h) [Reset = 00000000h]

GPOSEL0 is shown in Table 28-9.

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Controls routing of GPO signals from MDM, RFE and PBE to the radio GPO lines

Table 28-9. GPOSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	SRC3	R/W	0h	Select source of radio GPO line 3 0h = Output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 3
23-21	RESERVED	R	0h	Reserved
20-16	SRC2	R/W	0h	Select source of radio GPO line 2 0h = Output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 2

Table 28-9. GPOSEL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	SRC1	R/W	0h	Select source of radio GPO line 1 0h = Output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 1
7-5	RESERVED	R	0h	Reserved
4-0	SRC0	R/W	0h	Select source of radio GPO line 0 0h = Output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 0

28.5.7 GPOSEL1 Register (Offset = 18h) [Reset = 00000000h]

GPOSEL1 is shown in Table 28-10.

Return to the Summary Table.

Controls routing of GPO signals from MDM, RFE and PBE to the radio GPO lines

Table 28-10. GPOSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	SRC7	R/W	0h	Select source of radio GPO line 7 0h = No output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 7
23-21	RESERVED	R	0h	Reserved
20-16	SRC6	R/W	0h	Select source of radio GPO line 6 0h = No output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Selevt RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 6

Table 28-10. GPOSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	SRC5	R/W	0h	Select source of radio GPO line 5 0h = No output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 5
7-5	RESERVED	R	0h	Reserved
4-0	SRC4	R/W	0h	Select source of radio GPO line 4 0h = No output not enabled 1h = Select PBE GPO line 0 2h = Select PBE GPO line 1 3h = Select PBE GPO line 2 4h = Select PBE GPO line 3 5h = Select PBE GPO line 4 6h = Select PBE GPO line 5 7h = Select PBE GPO line 6 8h = Select PBE GPO line 7 9h = Select MCE GPO line 0 Ah = Select MCE GPO line 1 Bh = Select MCE GPO line 2 Ch = Select MCE GPO line 3 Dh = Select MCE GPO line 4 Eh = Select MCE GPO line 5 Fh = Select MCE GPO line 6 10h = Select MCE GPO line 7 11h = Select RFE GPO line 0 12h = Select RFE GPO line 1 13h = Select RFE GPO line 2 14h = Select RFE GPO line 3 15h = Select RFE GPO line 4 16h = Select RFE GPO line 5 17h = Select RFE GPO line 6 18h = Select RFE GPO line 7 19h = Select RFCTRC GPO line 4

28.5.8 IMASK0 Register (Offset = 44h) [Reset = 00000000h]

IMASK0 is shown in Table 28-11.

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Interrupt mask. ;This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 28-11. IMASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R/W	0h	SYSTIM2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
30	SYSTIM1	R/W	0h	SYSTIM1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
29	SYSTIM0	R/W	0h	SYSTIM0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
28	MDMDONE	R/W	0h	MDMDONE event 0h = Disable interrupt mask 1h = Enable interrupt mask
27	MDMIN	R/W	0h	MDMIN event 0h = Disable interrupt mask 1h = Enable interrupt mask
26	MDMOUT	R/W	0h	MDMOUT event 0h = Disable interrupt mask 1h = Enable interrupt mask
25	MDMSOFT2	R/W	0h	MDMSOFT2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
24	MDMSOFT1	R/W	0h	MDMSOFT1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
23	MDMSOFT0	R/W	0h	MDMSOFT0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
22	RFEDONE	R/W	0h	RFEDONE event 0h = Disable interrupt mask 1h = Enable interrupt mask
21	RFESOFT1	R/W	0h	RFESOFT1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
20	RFESOFT0	R/W	0h	RFESOFT0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
19	LOCK	R/W	0h	LOCK event 0h = Disable interrupt mask 1h = Enable interrupt mask
18	LOL	R/W	0h	LOSS_OF_LOCK event 0h = Disable interrupt mask 1h = Enable interrupt mask
17	TXFIFO	R/W	0h	TXFIFO event 0h = Disable interrupt mask 1h = Enable interrupt mask
16	RXFIFO	R/W	0h	RXFIFO event 0h = Disable interrupt mask 1h = Enable interrupt mask

Table 28-11. IMASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R/W	0h	PBE15 event 0h = Disable interrupt mask 1h = Enable interrupt mask
14	PBE14	R/W	0h	PBE14 event 0h = Disable interrupt mask 1h = Enable interrupt mask
13	PBE13	R/W	0h	PBE13 event 0h = Disable interrupt mask 1h = Enable interrupt mask
12	PBE12	R/W	0h	PBE12 event 0h = Disable interrupt mask 1h = Enable interrupt mask
11	PBE11	R/W	0h	PBE11 event 0h = Disable interrupt mask 1h = Enable interrupt mask
10	PBE10	R/W	0h	PBE10 event 0h = Disable interrupt mask 1h = Enable interrupt mask
9	PBE9	R/W	0h	PBE9 event 0h = Disable interrupt mask 1h = Enable interrupt mask
8	PBE8	R/W	0h	PBE8 event 0h = Disable interrupt mask 1h = Enable interrupt mask
7	PBE7	R/W	0h	PBE7 event 0h = Disable interrupt mask 1h = Enable interrupt mask
6	PBE6	R/W	0h	PBE6 event 0h = Disable interrupt mask 1h = Enable interrupt mask
5	PBE5	R/W	0h	PBE5 event 0h = Disable interrupt mask 1h = Enable interrupt mask
4	PBE4	R/W	0h	PBE4 event 0h = Disable interrupt mask 1h = Enable interrupt mask
3	PBE3	R/W	0h	PBE3 event 0h = Disable interrupt mask 1h = Enable interrupt mask
2	PBE2	R/W	0h	PBE2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
1	PBE1	R/W	0h	PBE1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
0	PBE0	R/W	0h	PBE0 event 0h = Disable interrupt mask 1h = Enable interrupt mask

28.5.9 RIS0 Register (Offset = 48h) [Reset = 00000000h]

RIS0 is shown in Table 28-12.

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Raw interrupt status. This register reflects the state of all pending interrupts, regardless of masking. This register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 28-12. RIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R	0h	SYSTIM2 event 0h = Interrupt did not occur 1h = Interrupt occurred
30	SYSTIM1	R	0h	SYSTIM1 event 0h = Interrupt did not occur 1h = Interrupt occurred
29	SYSTIM0	R	0h	SYSTIM0 event 0h = Interrupt did not occur 1h = Interrupt occurred
28	MDMDONE	R	0h	MDMDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
27	MDMIN	R	0h	MDMIN event 0h = Interrupt did not occur 1h = Interrupt occurred
26	MDMOUT	R	0h	MDMOUT event 0h = Interrupt did not occur 1h = Interrupt occurred
25	MDMSOFT2	R	0h	MDMSOFT2 event 0h = Interrupt did not occur 1h = Interrupt occurred
24	MDMSOFT1	R	0h	MDMSOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
23	MDMSOFT0	R	0h	MDMSOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
22	RFEDONE	R	0h	RFEDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
21	RFESOFT1	R	0h	RFESOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
20	RFESOFT0	R	0h	RFESOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
19	LOCK	R	0h	LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
18	LOL	R	0h	LOSS_OF_LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
17	TXFIFO	R	0h	TXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred
16	RXFIFO	R	0h	RXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred

Table 28-12. RIS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R	0h	PBE15 event 0h = Interrupt did not occur 1h = Interrupt occurred
14	PBE14	R	0h	PBE14 event 0h = Interrupt did not occur 1h = Interrupt occurred
13	PBE13	R	0h	PBE13 event 0h = Interrupt did not occur 1h = Interrupt occurred
12	PBE12	R	0h	PBE12 event 0h = Interrupt did not occur 1h = Interrupt occurred
11	PBE11	R	0h	PBE11 event 0h = Interrupt did not occur 1h = Interrupt occurred
10	PBE10	R	0h	PBE10 event 0h = Interrupt did not occur 1h = Interrupt occurred
9	PBE9	R	0h	PBE9 event 0h = Interrupt did not occur 1h = Interrupt occurred
8	PBE8	R	0h	PBE8 event 0h = Interrupt did not occur 1h = Interrupt occurred
7	PBE7	R	0h	PBE7 event 0h = Interrupt did not occur 1h = Interrupt occurred
6	PBE6	R	0h	PBE6 event 0h = Interrupt did not occur 1h = Interrupt occurred
5	PBE5	R	0h	PBE5 event 0h = Interrupt did not occur 1h = Interrupt occurred
4	PBE4	R	0h	PBE4 event 0h = Interrupt did not occur 1h = Interrupt occurred
3	PBE3	R	0h	PBE3 event 0h = Interrupt did not occur 1h = Interrupt occurred
2	PBE2	R	0h	PBE2 event 0h = Interrupt did not occur 1h = Interrupt occurred
1	PBE1	R	0h	PBE1 event 0h = Interrupt did not occur 1h = Interrupt occurred
0	PBE0	R	0h	PBE0 event 0h = Interrupt did not occur 1h = Interrupt occurred

28.5.10 MIS0 Register (Offset = 4Ch) [Reset = 00000000h]

MIS0 is shown in Table 28-13.

Return to the Summary Table.

Masked interrupt status. This register is simply a bitwise AND of the contents of IMASK and RIS.*] registers. A flag set in this register can be cleared by writing 1 to the corresponding ICLR register bit.

Table 28-13. MIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R	0h	SYSTIM2 event 0h = Interrupt did not occur 1h = Interrupt occurred
30	SYSTIM1	R	0h	SYSTIM1 event 0h = Interrupt did not occur 1h = Interrupt occurred
29	SYSTIM0	R	0h	SYSTIM0 event 0h = Interrupt did not occur 1h = Interrupt occurred
28	MDMDONE	R	0h	MDMDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
27	MDMIN	R	0h	MDMIN event 0h = Interrupt did not occur 1h = Interrupt occurred
26	MDMOUT	R	0h	MDMOUT event 0h = Interrupt did not occur 1h = Interrupt occurred
25	MDMSOFT2	R	0h	MDMSOFT2 event 0h = Interrupt did not occur 1h = Interrupt occurred
24	MDMSOFT1	R	0h	MDMSOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
23	MDMSOFT0	R	0h	MDMSOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
22	RFEDONE	R	0h	RFEDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
21	RFESOFT1	R	0h	RFESOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
20	RFESOFT0	R	0h	RFESOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
19	LOCK	R	0h	LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
18	LOL	R	0h	LOSS_OF_LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
17	TXFIFO	R	0h	TXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred
16	RXFIFO	R	0h	RXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred

Table 28-13. MIS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R	0h	PBE15 event 0h = Interrupt did not occur 1h = Interrupt occurred
14	PBE14	R	0h	PBE14 event 0h = Interrupt did not occur 1h = Interrupt occurred
13	PBE13	R	0h	PBE13 event 0h = Interrupt did not occur 1h = Interrupt occurred
12	PBE12	R	0h	PBE12 event 0h = Interrupt did not occur 1h = Interrupt occurred
11	PBE11	R	0h	PBE11 event 0h = Interrupt did not occur 1h = Interrupt occurred
10	PBE10	R	0h	PBE10 event 0h = Interrupt did not occur 1h = Interrupt occurred
9	PBE9	R	0h	PBE9 event 0h = Interrupt did not occur 1h = Interrupt occurred
8	PBE8	R	0h	PBE8 event 0h = Interrupt did not occur 1h = Interrupt occurred
7	PBE7	R	0h	PBE7 event 0h = Interrupt did not occur 1h = Interrupt occurred
6	PBE6	R	0h	PBE6 event 0h = Interrupt did not occur 1h = Interrupt occurred
5	PBE5	R	0h	PBE5 event 0h = Interrupt did not occur 1h = Interrupt occurred
4	PBE4	R	0h	PBE4 event 0h = Interrupt did not occur 1h = Interrupt occurred
3	PBE3	R	0h	PBE3 event 0h = Interrupt did not occur 1h = Interrupt occurred
2	PBE2	R	0h	PBE2 event 0h = Interrupt did not occur 1h = Interrupt occurred
1	PBE1	R	0h	PBE1 event 0h = Interrupt did not occur 1h = Interrupt occurred
0	PBE0	R	0h	PBE0 event 0h = Interrupt did not occur 1h = Interrupt occurred

28.5.11 ISET0 Register (Offset = 50h) [Reset = 00000000h]

ISET0 is shown in Table 28-14.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 28-14. ISET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	W	0h	SYSTIM2 event 0h = Writing 0 has no effect 1h = Set Interrupt
30	SYSTIM1	W	0h	SYSTIM1 event 0h = Writing 0 has no effect 1h = Set Interrupt
29	SYSTIM0	W	0h	SYSTIM0 event 0h = Writing 0 has no effect 1h = Set Interrupt
28	MDMDONE	W	0h	MDMDONE event 0h = Writing 0 has no effect 1h = Set Interrupt
27	MDMIN	W	0h	MDMIN event 0h = Writing 0 has no effect 1h = Set Interrupt
26	MDMOUT	W	0h	MDMOUT event 0h = Writing 0 has no effect 1h = Set Interrupt
25	MDMSOFT2	W	0h	MDMSOFT2 event 0h = Writing 0 has no effect 1h = Set Interrupt
24	MDMSOFT1	W	0h	MDMSOFT1 event 0h = Writing 0 has no effect 1h = Set Interrupt
23	MDMSOFT0	W	0h	MDMSOFT0 event 0h = Writing 0 has no effect 1h = Set Interrupt
22	RFEDONE	W	0h	RFEDONE event 0h = Writing 0 has no effect 1h = Set Interrupt
21	RFESOFT1	W	0h	RFESOFT1 event 0h = Writing 0 has no effect 1h = Set Interrupt
20	RFESOFT0	W	0h	RFESOFT0 event 0h = Writing 0 has no effect 1h = Set Interrupt
19	LOCK	W	0h	LOCK event 0h = Writing 0 has no effect 1h = Set Interrupt
18	LOL	W	0h	LOSS_OF_LOCK event 0h = Writing 0 has no effect 1h = Set Interrupt
17	TXFIFO	W	0h	TXFIFO event 0h = Writing 0 has no effect 1h = Set Interrupt
16	RXFIFO	W	0h	RXFIFO event 0h = Writing 0 has no effect 1h = Set Interrupt

Table 28-14. ISET0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	W	0h	PBE15 event 0h = Writing 0 has no effect 1h = Set Interrupt
14	PBE14	W	0h	PBE14 event 0h = Writing 0 has no effect 1h = Set Interrupt
13	PBE13	W	0h	PBE13 event 0h = Writing 0 has no effect 1h = Set Interrupt
12	PBE12	W	0h	PBE12 event 0h = Writing 0 has no effect 1h = Set Interrupt
11	PBE11	W	0h	PBE11 event 0h = Writing 0 has no effect 1h = Set Interrupt
10	PBE10	W	0h	PBE10 event 0h = Writing 0 has no effect 1h = Set Interrupt
9	PBE9	W	0h	PBE9 event 0h = Writing 0 has no effect 1h = Set Interrupt
8	PBE8	W	0h	PBE8 event 0h = Writing 0 has no effect 1h = Set Interrupt
7	PBE7	W	0h	PBE7 event 0h = Writing 0 has no effect 1h = Set Interrupt
6	PBE6	W	0h	PBE6 event 0h = Writing 0 has no effect 1h = Set Interrupt
5	PBE5	W	0h	PBE5 event 0h = Writing 0 has no effect 1h = Set Interrupt
4	PBE4	W	0h	PBE4 event 0h = Writing 0 has no effect 1h = Set Interrupt
3	PBE3	W	0h	PBE3 event 0h = Writing 0 has no effect 1h = Set Interrupt
2	PBE2	W	0h	PBE2 event 0h = Writing 0 has no effect 1h = Set Interrupt
1	PBE1	W	0h	PBE1 event 0h = Writing 0 has no effect 1h = Set Interrupt
0	PBE0	W	0h	PBE0 event 0h = Writing 0 has no effect 1h = Set Interrupt

28.5.12 ICLR0 Register (Offset = 54h) [Reset = 00000000h]

ICLR0 is shown in Table 28-15.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 28-15. ICLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	W	0h	SYSTIM2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
30	SYSTIM1	W	0h	SYSTIM1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
29	SYSTIM0	W	0h	SYSTIM0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
28	MDMDONE	W	0h	MDMDONE event 0h = Writing 0 has no effect 1h = Clear Interrupt
27	MDMIN	W	0h	MDMIN event 0h = Writing 0 has no effect 1h = Clear Interrupt
26	MDMOUT	W	0h	MDMOUT event 0h = Writing 0 has no effect 1h = Clear Interrupt
25	MDMSOFT2	W	0h	MDMSOFT2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
24	MDMSOFT1	W	0h	MDMSOFT1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
23	MDMSOFT0	W	0h	MDMSOFT0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
22	RFEDONE	W	0h	RFEDONE event 0h = Writing 0 has no effect 1h = Clear Interrupt
21	RFESOFT1	W	0h	RFESOFT1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
20	RFESOFT0	W	0h	RFESOFT0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
19	LOCK	W	0h	LOCK event 0h = Writing 0 has no effect 1h = Clear Interrupt
18	LOL	W	0h	LOSS_OF_LOCK event 0h = Writing 0 has no effect 1h = Clear Interrupt
17	TXFIFO	W	0h	TXFIFO event 0h = Writing 0 has no effect 1h = Clear Interrupt
16	RXFIFO	W	0h	RXFIFO event 0h = Writing 0 has no effect 1h = Clear Interrupt

Table 28-15. ICLR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	W	0h	PBE15 event 0h = Writing 0 has no effect 1h = Clear Interrupt
14	PBE14	W	0h	PBE14 event 0h = Writing 0 has no effect 1h = Clear Interrupt
13	PBE13	W	0h	PBE13 event 0h = Writing 0 has no effect 1h = Clear Interrupt
12	PBE12	W	0h	PBE12 event 0h = Writing 0 has no effect 1h = Clear Interrupt
11	PBE11	W	0h	PBE11 event 0h = Writing 0 has no effect 1h = Clear Interrupt
10	PBE10	W	0h	PBE10 event 0h = Writing 0 has no effect 1h = Clear Interrupt
9	PBE9	W	0h	PBE9 event 0h = Writing 0 has no effect 1h = Clear Interrupt
8	PBE8	W	0h	PBE8 event 0h = Writing 0 has no effect 1h = Clear Interrupt
7	PBE7	W	0h	PBE7 event 0h = Writing 0 has no effect 1h = Clear Interrupt
6	PBE6	W	0h	PBE6 event 0h = Writing 0 has no effect 1h = Clear Interrupt
5	PBE5	W	0h	PBE5 event 0h = Writing 0 has no effect 1h = Clear Interrupt
4	PBE4	W	0h	PBE4 event 0h = Writing 0 has no effect 1h = Clear Interrupt
3	PBE3	W	0h	PBE3 event 0h = Writing 0 has no effect 1h = Clear Interrupt
2	PBE2	W	0h	PBE2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
1	PBE1	W	0h	PBE1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
0	PBE0	W	0h	PBE0 event 0h = Writing 0 has no effect 1h = Clear Interrupt

28.5.13 IMASK1 Register (Offset = 84h) [Reset = 00000000h]

IMASK1 is shown in Table 28-16.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 28-16. IMASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R/W	0h	SYSTIM2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
30	SYSTIM1	R/W	0h	SYSTIM1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
29	SYSTIM0	R/W	0h	SYSTIM0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
28	MDMDONE	R/W	0h	MDMDONE event 0h = Disable interrupt mask 1h = Enable interrupt mask
27	MDMIN	R/W	0h	MDMIN event 0h = Disable interrupt mask 1h = Enable interrupt mask
26	MDMOUT	R/W	0h	MDMOUT event 0h = Disable interrupt mask 1h = Enable interrupt mask
25	MDMSOFT2	R/W	0h	MDMSOFT2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
24	MDMSOFT1	R/W	0h	MDMSOFT1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
23	MDMSOFT0	R/W	0h	MDMSOFT0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
22	RFEDONE	R/W	0h	RFEDONE event 0h = Disable interrupt mask 1h = Enable interrupt mask
21	RFESOFT1	R/W	0h	RFESOFT1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
20	RFESOFT0	R/W	0h	RFESOFT0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
19	LOCK	R/W	0h	LOCK event 0h = Disable interrupt mask 1h = Enable interrupt mask
18	LOL	R/W	0h	LOSS_OF_LOCK event 0h = Disable interrupt mask 1h = Enable interrupt mask
17	TXFIFO	R/W	0h	TXFIFO event 0h = Disable interrupt mask 1h = Enable interrupt mask
16	RXFIFO	R/W	0h	RXFIFO event 0h = Disable interrupt mask 1h = Enable interrupt mask

Table 28-16. IMASK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R/W	0h	PBE15 event 0h = Disable interrupt mask 1h = Enable interrupt mask
14	PBE14	R/W	0h	PBE14 event 0h = Disable interrupt mask 1h = Enable interrupt mask
13	PBE13	R/W	0h	PBE13 event 0h = Disable interrupt mask 1h = Enable interrupt mask
12	PBE12	R/W	0h	PBE12 event 0h = Disable interrupt mask 1h = Enable interrupt mask
11	PBE11	R/W	0h	PBE11 event 0h = Disable interrupt mask 1h = Enable interrupt mask
10	PBE10	R/W	0h	PBE10 event 0h = Disable interrupt mask 1h = Enable interrupt mask
9	PBE9	R/W	0h	PBE9 event 0h = Disable interrupt mask 1h = Enable interrupt mask
8	PBE8	R/W	0h	PBE8 event 0h = Disable interrupt mask 1h = Enable interrupt mask
7	PBE7	R/W	0h	PBE7 event 0h = Disable interrupt mask 1h = Enable interrupt mask
6	PBE6	R/W	0h	PBE6 event 0h = Disable interrupt mask 1h = Enable interrupt mask
5	PBE5	R/W	0h	PBE5 event 0h = Disable interrupt mask 1h = Enable interrupt mask
4	PBE4	R/W	0h	PBE4 event 0h = Disable interrupt mask 1h = Enable interrupt mask
3	PBE3	R/W	0h	PBE3 event 0h = Disable interrupt mask 1h = Enable interrupt mask
2	PBE2	R/W	0h	PBE2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
1	PBE1	R/W	0h	PBE1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
0	PBE0	R/W	0h	PBE0 event 0h = Disable interrupt mask 1h = Enable interrupt mask

28.5.14 RIS1 Register (Offset = 88h) [Reset = 00000000h]

RIS1 is shown in Table 28-17.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS0 register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 28-17. RIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R	0h	SYSTIM2 event 0h = Interrupt did not occur 1h = Interrupt occurred
30	SYSTIM1	R	0h	SYSTIM1 event 0h = Interrupt did not occur 1h = Interrupt occurred
29	SYSTIM0	R	0h	SYSTIM0 event 0h = Interrupt did not occur 1h = Interrupt occurred
28	MDMDONE	R	0h	MDMDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
27	MDMIN	R	0h	MDMIN event 0h = Interrupt did not occur 1h = Interrupt occurred
26	MDMOUT	R	0h	MDMOUT event 0h = Interrupt did not occur 1h = Interrupt occurred
25	MDMSOFT2	R	0h	MDMSOFT2 event 0h = Interrupt did not occur 1h = Interrupt occurred
24	MDMSOFT1	R	0h	MDMSOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
23	MDMSOFT0	R	0h	MDMSOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
22	RFEDONE	R	0h	RFEDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
21	RFESOFT1	R	0h	RFESOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
20	RFESOFT0	R	0h	RFESOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
19	LOCK	R	0h	LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
18	LOL	R	0h	LOSS_OF_LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
17	TXFIFO	R	0h	TXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred
16	RXFIFO	R	0h	RXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred

Table 28-17. RIS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R	0h	PBE15 event 0h = Interrupt did not occur 1h = Interrupt occurred
14	PBE14	R	0h	PBE14 event 0h = Interrupt did not occur 1h = Interrupt occurred
13	PBE13	R	0h	PBE13 event 0h = Interrupt did not occur 1h = Interrupt occurred
12	PBE12	R	0h	PBE12 event 0h = Interrupt did not occur 1h = Interrupt occurred
11	PBE11	R	0h	PBE11 event 0h = Interrupt did not occur 1h = Interrupt occurred
10	PBE10	R	0h	PBE10 event 0h = Interrupt did not occur 1h = Interrupt occurred
9	PBE9	R	0h	PBE9 event 0h = Interrupt did not occur 1h = Interrupt occurred
8	PBE8	R	0h	PBE8 event 0h = Interrupt did not occur 1h = Interrupt occurred
7	PBE7	R	0h	PBE7 event 0h = Interrupt did not occur 1h = Interrupt occurred
6	PBE6	R	0h	PBE6 event 0h = Interrupt did not occur 1h = Interrupt occurred
5	PBE5	R	0h	PBE5 event 0h = Interrupt did not occur 1h = Interrupt occurred
4	PBE4	R	0h	PBE4 event 0h = Interrupt did not occur 1h = Interrupt occurred
3	PBE3	R	0h	PBE3 event 0h = Interrupt did not occur 1h = Interrupt occurred
2	PBE2	R	0h	PBE2 event 0h = Interrupt did not occur 1h = Interrupt occurred
1	PBE1	R	0h	PBE1 event 0h = Interrupt did not occur 1h = Interrupt occurred
0	PBE0	R	0h	PBE0 event 0h = Interrupt did not occur 1h = Interrupt occurred

28.5.15 MIS1 Register (Offset = 8Ch) [Reset = 00000000h]

MIS1 is shown in Table 28-18.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 28-18. MIS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R	0h	SYSTIM2 event 0h = Interrupt did not occur 1h = Interrupt occurred
30	SYSTIM1	R	0h	SYSTIM1 event 0h = Interrupt did not occur 1h = Interrupt occurred
29	SYSTIM0	R	0h	SYSTIM0 event 0h = Interrupt did not occur 1h = Interrupt occurred
28	MDMDONE	R	0h	MDMDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
27	MDMIN	R	0h	MDMIN event 0h = Interrupt did not occur 1h = Interrupt occurred
26	MDMOUT	R	0h	MDMOUT event 0h = Interrupt did not occur 1h = Interrupt occurred
25	MDMSOFT2	R	0h	MDMSOFT2 event 0h = Interrupt did not occur 1h = Interrupt occurred
24	MDMSOFT1	R	0h	MDMSOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
23	MDMSOFT0	R	0h	MDMSOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
22	RFEDONE	R	0h	RFEDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
21	RFESOFT1	R	0h	RFESOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
20	RFESOFT0	R	0h	RFESOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
19	LOCK	R	0h	LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
18	LOL	R	0h	LOSS_OF_LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
17	TXFIFO	R	0h	TXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred
16	RXFIFO	R	0h	RXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred

Table 28-18. MIS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R	0h	PBE15 event 0h = Interrupt did not occur 1h = Interrupt occurred
14	PBE14	R	0h	PBE14 event 0h = Interrupt did not occur 1h = Interrupt occurred
13	PBE13	R	0h	PBE13 event 0h = Interrupt did not occur 1h = Interrupt occurred
12	PBE12	R	0h	PBE12 event 0h = Interrupt did not occur 1h = Interrupt occurred
11	PBE11	R	0h	PBE11 event 0h = Interrupt did not occur 1h = Interrupt occurred
10	PBE10	R	0h	PBE10 event 0h = Interrupt did not occur 1h = Interrupt occurred
9	PBE9	R	0h	PBE9 event 0h = Interrupt did not occur 1h = Interrupt occurred
8	PBE8	R	0h	PBE8 event 0h = Interrupt did not occur 1h = Interrupt occurred
7	PBE7	R	0h	PBE7 event 0h = Interrupt did not occur 1h = Interrupt occurred
6	PBE6	R	0h	PBE6 event 0h = Interrupt did not occur 1h = Interrupt occurred
5	PBE5	R	0h	PBE5 event 0h = Interrupt did not occur 1h = Interrupt occurred
4	PBE4	R	0h	PBE4 event 0h = Interrupt did not occur 1h = Interrupt occurred
3	PBE3	R	0h	PBE3 event 0h = Interrupt did not occur 1h = Interrupt occurred
2	PBE2	R	0h	PBE2 event 0h = Interrupt did not occur 1h = Interrupt occurred
1	PBE1	R	0h	PBE1 event 0h = Interrupt did not occur 1h = Interrupt occurred
0	PBE0	R	0h	PBE0 event 0h = Interrupt did not occur 1h = Interrupt occurred

28.5.16 ISET1 Register (Offset = 90h) [Reset = 00000000h]

ISET1 is shown in Table 28-19.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 28-19. ISET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	W	0h	SYSTIM2 event 0h = Writing 0 has no effect 1h = Set Interrupt
30	SYSTIM1	W	0h	SYSTIM1 event 0h = Writing 0 has no effect 1h = Set Interrupt
29	SYSTIM0	W	0h	SYSTIM0 event 0h = Writing 0 has no effect 1h = Set Interrupt
28	MDMDONE	W	0h	MDMDONE event 0h = Writing 0 has no effect 1h = Set Interrupt
27	MDMIN	W	0h	MDMIN event 0h = Writing 0 has no effect 1h = Set Interrupt
26	MDMOUT	W	0h	MDMOUT event 0h = Writing 0 has no effect 1h = Set Interrupt
25	MDMSOFT2	W	0h	MDMSOFT2 event 0h = Writing 0 has no effect 1h = Set Interrupt
24	MDMSOFT1	W	0h	MDMSOFT1 event 0h = Writing 0 has no effect 1h = Set Interrupt
23	MDMSOFT0	W	0h	MDMSOFT0 event 0h = Writing 0 has no effect 1h = Set Interrupt
22	RFEDONE	W	0h	RFEDONE event 0h = Writing 0 has no effect 1h = Set Interrupt
21	RFESOFT1	W	0h	RFESOFT1 event 0h = Writing 0 has no effect 1h = Set Interrupt
20	RFESOFT0	W	0h	RFESOFT0 event 0h = Writing 0 has no effect 1h = Set Interrupt
19	LOCK	W	0h	LOCK event 0h = Writing 0 has no effect 1h = Set Interrupt
18	LOL	W	0h	LOSS_OF_LOCK event 0h = Writing 0 has no effect 1h = Set Interrupt
17	TXFIFO	W	0h	TXFIFO event 0h = Writing 0 has no effect 1h = Set Interrupt
16	RXFIFO	W	0h	RXFIFO event 0h = Writing 0 has no effect 1h = Set Interrupt

Table 28-19. ISET1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	W	0h	PBE15 event 0h = Writing 0 has no effect 1h = Set Interrupt
14	PBE14	W	0h	PBE14 event 0h = Writing 0 has no effect 1h = Set Interrupt
13	PBE13	W	0h	PBE13 event 0h = Writing 0 has no effect 1h = Set Interrupt
12	PBE12	W	0h	PBE12 event 0h = Writing 0 has no effect 1h = Set Interrupt
11	PBE11	W	0h	PBE11 event 0h = Writing 0 has no effect 1h = Set Interrupt
10	PBE10	W	0h	PBE10 event 0h = Writing 0 has no effect 1h = Set Interrupt
9	PBE9	W	0h	PBE9 event 0h = Writing 0 has no effect 1h = Set Interrupt
8	PBE8	W	0h	PBE8 event 0h = Writing 0 has no effect 1h = Set Interrupt
7	PBE7	W	0h	PBE7 event 0h = Writing 0 has no effect 1h = Set Interrupt
6	PBE6	W	0h	PBE6 event 0h = Writing 0 has no effect 1h = Set Interrupt
5	PBE5	W	0h	PBE5 event 0h = Writing 0 has no effect 1h = Set Interrupt
4	PBE4	W	0h	PBE4 event 0h = Writing 0 has no effect 1h = Set Interrupt
3	PBE3	W	0h	PBE3 event 0h = Writing 0 has no effect 1h = Set Interrupt
2	PBE2	W	0h	PBE2 event 0h = Writing 0 has no effect 1h = Set Interrupt
1	PBE1	W	0h	PBE1 event 0h = Writing 0 has no effect 1h = Set Interrupt
0	PBE0	W	0h	PBE0 event 0h = Writing 0 has no effect 1h = Set Interrupt

28.5.17 ICLR1 Register (Offset = 94h) [Reset = 00000000h]

ICLR1 is shown in Table 28-20.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 28-20. ICLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	SYSTIM2	W	0h	SYSTIM2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
29	SYSTIM1	W	0h	SYSTIM1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
28	SYSTIM0	W	0h	SYSTIM0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
27	MDMDONE	W	0h	MDMDONE event 0h = Writing 0 has no effect 1h = Clear Interrupt
26	MDMIN	W	0h	MDMIN event 0h = Writing 0 has no effect 1h = Clear Interrupt
25	MDMOUT	W	0h	MDMOUT event 0h = Writing 0 has no effect 1h = Clear Interrupt
24	MDMSOFT2	W	0h	MDMSOFT2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
23	MDMSOFT1	W	0h	MDMSOFT1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
22	MDMSOFT0	W	0h	MDMSOFT0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
21	RFEDONE	W	0h	RFEDONE event 0h = Writing 0 has no effect 1h = Clear Interrupt
20	RFESOFT1	W	0h	RFESOFT1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
19	RFESOFT0	W	0h	RFESOFT0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
18	LOCK	W	0h	LOCK event 0h = Writing 0 has no effect 1h = Clear Interrupt
17	LOL	W	0h	LOSS_OF_LOCK event 0h = Writing 0 has no effect 1h = Clear Interrupt
16	TXFIFO	W	0h	TXFIFO event 0h = Writing 0 has no effect 1h = Clear Interrupt
15	RXFIFO	W	0h	RXFIFO event 0h = Writing 0 has no effect 1h = Clear Interrupt

Table 28-20. ICLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	PBE15	W	0h	PBE15 event 0h = Writing 0 has no effect 1h = Clear Interrupt
13	PBE14	W	0h	PBE14 event 0h = Writing 0 has no effect 1h = Clear Interrupt
12	PBE13	W	0h	PBE13 event 0h = Writing 0 has no effect 1h = Clear Interrupt
11	PBE12	W	0h	PBE12 event 0h = Writing 0 has no effect 1h = Clear Interrupt
10	PBE11	W	0h	PBE11 event 0h = Writing 0 has no effect 1h = Clear Interrupt
9	PBE10	W	0h	PBE10 event 0h = Writing 0 has no effect 1h = Clear Interrupt
8	PBE9	W	0h	PBE9 event 0h = Writing 0 has no effect 1h = Clear Interrupt
7	PBE8	W	0h	PBE8 event 0h = Writing 0 has no effect 1h = Clear Interrupt
6	PBE6	W	0h	PBE6 event 0h = Writing 0 has no effect 1h = Clear Interrupt
5	PBE5	W	0h	PBE5 event 0h = Writing 0 has no effect 1h = Clear Interrupt
4	PBE4	W	0h	PBE4 event 0h = Writing 0 has no effect 1h = Clear Interrupt
3	PBE3	W	0h	PBE3 event 0h = Writing 0 has no effect 1h = Clear Interrupt
2	PBE2	W	0h	PBE2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
1	PBE1	W	0h	PBE1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
0	PBE0	W	0h	PBE0 event 0h = Writing 0 has no effect 1h = Clear Interrupt

28.5.18 IMASK2 Register (Offset = C4h) [Reset = 00000000h]

IMASK2 is shown in Table 28-21.

Return to the Summary Table.

Interrupt mask. This register selects interrupt sources which are allowed to pass from RIS to MIS when the corresponding bit-fields are set to 1.

Table 28-21. IMASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R/W	0h	SYSTIM2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
30	SYSTIM1	R/W	0h	SYSTIM1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
29	SYSTIM0	R/W	0h	SYSTIM0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
28	MDMDONE	R/W	0h	MDMDONE event 0h = Disable interrupt mask 1h = Enable interrupt mask
27	MDMIN	R/W	0h	MDMIN event 0h = Disable interrupt mask 1h = Enable interrupt mask
26	MDMOUT	R/W	0h	MDMOUT event 0h = Disable interrupt mask 1h = Enable interrupt mask
25	MDMSOFT2	R/W	0h	MDMSOFT2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
24	MDMSOFT1	R/W	0h	MDMSOFT1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
23	MDMSOFT0	R/W	0h	MDMSOFT0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
22	RFEDONE	R/W	0h	RFEDONE event 0h = Disable interrupt mask 1h = Enable interrupt mask
21	RFESOFT1	R/W	0h	RFESOFT1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
20	RFESOFT0	R/W	0h	RFESOFT0 event 0h = Disable interrupt mask 1h = Enable interrupt mask
19	LOCK	R/W	0h	LOCK event 0h = Disable interrupt mask 1h = Enable interrupt mask
18	LOL	R/W	0h	LOSS_OF_LOCK event 0h = Disable interrupt mask 1h = Enable interrupt mask
17	TXFIFO	R/W	0h	TXFIFO event 0h = Disable interrupt mask 1h = Enable interrupt mask
16	RXFIFO	R/W	0h	RXFIFO event 0h = Disable interrupt mask 1h = Enable interrupt mask

Table 28-21. IMASK2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R/W	0h	PBE15 event 0h = Disable interrupt mask 1h = Enable interrupt mask
14	PBE14	R/W	0h	PBE14 event 0h = Disable interrupt mask 1h = Enable interrupt mask
13	PBE13	R/W	0h	PBE13 event 0h = Disable interrupt mask 1h = Enable interrupt mask
12	PBE12	R/W	0h	PBE12 event 0h = Disable interrupt mask 1h = Enable interrupt mask
11	PBE11	R/W	0h	PBE11 event 0h = Disable interrupt mask 1h = Enable interrupt mask
10	PBE10	R/W	0h	PBE10 event 0h = Disable interrupt mask 1h = Enable interrupt mask
9	PBE9	R/W	0h	PBE9 event 0h = Disable interrupt mask 1h = Enable interrupt mask
8	PBE8	R/W	0h	PBE8 event 0h = Disable interrupt mask 1h = Enable interrupt mask
7	PBE7	R/W	0h	PBE7 event 0h = Disable interrupt mask 1h = Enable interrupt mask
6	PBE6	R/W	0h	PBE6 event 0h = Disable interrupt mask 1h = Enable interrupt mask
5	PBE5	R/W	0h	PBE5 event 0h = Disable interrupt mask 1h = Enable interrupt mask
4	PBE4	R/W	0h	PBE4 event 0h = Disable interrupt mask 1h = Enable interrupt mask
3	PBE3	R/W	0h	PBE3 event 0h = Disable interrupt mask 1h = Enable interrupt mask
2	PBE2	R/W	0h	PBE2 event 0h = Disable interrupt mask 1h = Enable interrupt mask
1	PBE1	R/W	0h	PBE1 event 0h = Disable interrupt mask 1h = Enable interrupt mask
0	PBE0	R/W	0h	PBE0 event 0h = Disable interrupt mask 1h = Enable interrupt mask

28.5.19 RIS2 Register (Offset = C8h) [Reset = 00000000h]

RIS2 is shown in Table 28-22.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS0 register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Table 28-22. RIS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R	0h	SYSTIM2 event 0h = Interrupt did not occur 1h = Interrupt occurred
30	SYSTIM1	R	0h	SYSTIM1 event 0h = Interrupt did not occur 1h = Interrupt occurred
29	SYSTIM0	R	0h	SYSTIM0 event 0h = Interrupt did not occur 1h = Interrupt occurred
28	MDMDONE	R	0h	MDMDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
27	MDMIN	R	0h	MDMIN event 0h = Interrupt did not occur 1h = Interrupt occurred
26	MDMOUT	R	0h	MDMOUT event 0h = Interrupt did not occur 1h = Interrupt occurred
25	MDMSOFT2	R	0h	MDMSOFT2 event 0h = Interrupt did not occur 1h = Interrupt occurred
24	MDMSOFT1	R	0h	MDMSOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
23	MDMSOFT0	R	0h	MDMSOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
22	RFEDONE	R	0h	RFEDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
21	RFESOFT1	R	0h	RFESOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
20	RFESOFT0	R	0h	RFESOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
19	LOCK	R	0h	LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
18	LOL	R	0h	LOSS_OF_LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
17	TXFIFO	R	0h	TXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred
16	RXFIFO	R	0h	RXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred

Table 28-22. RIS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R	0h	PBE15 event 0h = Interrupt did not occur 1h = Interrupt occurred
14	PBE14	R	0h	PBE14 event 0h = Interrupt did not occur 1h = Interrupt occurred
13	PBE13	R	0h	PBE13 event 0h = Interrupt did not occur 1h = Interrupt occurred
12	PBE12	R	0h	PBE12 event 0h = Interrupt did not occur 1h = Interrupt occurred
11	PBE11	R	0h	PBE11 event 0h = Interrupt did not occur 1h = Interrupt occurred
10	PBE10	R	0h	PBE10 event 0h = Interrupt did not occur 1h = Interrupt occurred
9	PBE9	R	0h	PBE9 event 0h = Interrupt did not occur 1h = Interrupt occurred
8	PBE8	R	0h	PBE8 event 0h = Interrupt did not occur 1h = Interrupt occurred
7	PBE7	R	0h	PBE7 event 0h = Interrupt did not occur 1h = Interrupt occurred
6	PBE6	R	0h	PBE6 event 0h = Interrupt did not occur 1h = Interrupt occurred
5	PBE5	R	0h	PBE5 event 0h = Interrupt did not occur 1h = Interrupt occurred
4	PBE4	R	0h	PBE4 event 0h = Interrupt did not occur 1h = Interrupt occurred
3	PBE3	R	0h	PBE3 event 0h = Interrupt did not occur 1h = Interrupt occurred
2	PBE2	R	0h	PBE2 event 0h = Interrupt did not occur 1h = Interrupt occurred
1	PBE1	R	0h	PBE1 event 0h = Interrupt did not occur 1h = Interrupt occurred
0	PBE0	R	0h	PBE0 event 0h = Interrupt did not occur 1h = Interrupt occurred

28.5.20 MIS2 Register (Offset = CCh) [Reset = 00000000h]

MIS2 is shown in Table 28-23.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Table 28-23. MIS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	R	0h	SYSTIM2 event 0h = Interrupt did not occur 1h = Interrupt occurred
30	SYSTIM1	R	0h	SYSTIM1 event 0h = Interrupt did not occur 1h = Interrupt occurred
29	SYSTIM0	R	0h	SYSTIM0 event 0h = Interrupt did not occur 1h = Interrupt occurred
28	MDMDONE	R	0h	MDMDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
27	MDMIN	R	0h	MDMIN event 0h = Interrupt did not occur 1h = Interrupt occurred
26	MDMOUT	R	0h	MDMOUT event 0h = Interrupt did not occur 1h = Interrupt occurred
25	MDMSOFT2	R	0h	MDMSOFT2 event 0h = Interrupt did not occur 1h = Interrupt occurred
24	MDMSOFT1	R	0h	MDMSOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
23	MDMSOFT0	R	0h	MDMSOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
22	RFEDONE	R	0h	RFEDONE event 0h = Interrupt did not occur 1h = Interrupt occurred
21	RFESOFT1	R	0h	RFESOFT1 event 0h = Interrupt did not occur 1h = Interrupt occurred
20	RFESOFT0	R	0h	RFESOFT0 event 0h = Interrupt did not occur 1h = Interrupt occurred
19	LOCK	R	0h	LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
18	LOL	R	0h	LOSS_OF_LOCK event 0h = Interrupt did not occur 1h = Interrupt occurred
17	TXFIFO	R	0h	TXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred
16	RXFIFO	R	0h	RXFIFO event 0h = Interrupt did not occur 1h = Interrupt occurred

Table 28-23. MIS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	R	0h	PBE15 event 0h = Interrupt did not occur 1h = Interrupt occurred
14	PBE14	R	0h	PBE14 event 0h = Interrupt did not occur 1h = Interrupt occurred
13	PBE13	R	0h	PBE13 event 0h = Interrupt did not occur 1h = Interrupt occurred
12	PBE12	R	0h	PBE12 event 0h = Interrupt did not occur 1h = Interrupt occurred
11	PBE11	R	0h	PBE11 event 0h = Interrupt did not occur 1h = Interrupt occurred
10	PBE10	R	0h	PBE10 event 0h = Interrupt did not occur 1h = Interrupt occurred
9	PBE9	R	0h	PBE9 event 0h = Interrupt did not occur 1h = Interrupt occurred
8	PBE8	R	0h	PBE8 event 0h = Interrupt did not occur 1h = Interrupt occurred
7	PBE7	R	0h	PBE7 event 0h = Interrupt did not occur 1h = Interrupt occurred
6	PBE6	R	0h	PBE6 event 0h = Interrupt did not occur 1h = Interrupt occurred
5	PBE5	R	0h	PBE5 event 0h = Interrupt did not occur 1h = Interrupt occurred
4	PBE4	R	0h	PBE4 event 0h = Interrupt did not occur 1h = Interrupt occurred
3	PBE3	R	0h	PBE3 event 0h = Interrupt did not occur 1h = Interrupt occurred
2	PBE2	R	0h	PBE2 event 0h = Interrupt did not occur 1h = Interrupt occurred
1	PBE1	R	0h	PBE1 event 0h = Interrupt did not occur 1h = Interrupt occurred
0	PBE0	R	0h	PBE0 event 0h = Interrupt did not occur 1h = Interrupt occurred

28.5.21 ISET2 Register (Offset = D0h) [Reset = 00000000h]

ISET2 is shown in Table 28-24.

Return to the Summary Table.

Interrupt set register. This register can used by software for diagnostics and safety checking purposes. Writing a 1 to a bit in this register will set the event and the corresponding RIS bit also gets set. If the corresponding IMASK bit is set, then the corresponding MIS register bit also gets set.

Table 28-24. ISET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SYSTIM2	W	0h	SYSTIM2 event 0h = Writing 0 has no effect 1h = Set Interrupt
30	SYSTIM1	W	0h	SYSTIM1 event 0h = Writing 0 has no effect 1h = Set Interrupt
29	SYSTIM0	W	0h	SYSTIM0 event 0h = Writing 0 has no effect 1h = Set Interrupt
28	MDMDONE	W	0h	MDMDONE event 0h = Writing 0 has no effect 1h = Set Interrupt
27	MDMIN	W	0h	MDMIN event 0h = Writing 0 has no effect 1h = Set Interrupt
26	MDMOUT	W	0h	MDMOUT event 0h = Writing 0 has no effect 1h = Set Interrupt
25	MDMSOFT2	W	0h	MDMSOFT2 event 0h = Writing 0 has no effect 1h = Set Interrupt
24	MDMSOFT1	W	0h	MDMSOFT1 event 0h = Writing 0 has no effect 1h = Set Interrupt
23	MDMSOFT0	W	0h	MDMSOFT0 event 0h = Writing 0 has no effect 1h = Set Interrupt
22	RFEDONE	W	0h	RFEDONE event 0h = Writing 0 has no effect 1h = Set Interrupt
21	RFESOFT1	W	0h	RFESOFT1 event 0h = Writing 0 has no effect 1h = Set Interrupt
20	RFESOFT0	W	0h	RFESOFT0 event 0h = Writing 0 has no effect 1h = Set Interrupt
19	LOCK	W	0h	LOCK event 0h = Writing 0 has no effect 1h = Set Interrupt
18	LOL	W	0h	LOSS_OF_LOCK event 0h = Writing 0 has no effect 1h = Set Interrupt
17	TXFIFO	W	0h	TXFIFO event 0h = Writing 0 has no effect 1h = Set Interrupt
16	RXFIFO	W	0h	RXFIFO event 0h = Writing 0 has no effect 1h = Set Interrupt

Table 28-24. ISET2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PBE15	W	0h	PBE15 event 0h = Writing 0 has no effect 1h = Set Interrupt
14	PBE14	W	0h	PBE14 event 0h = Writing 0 has no effect 1h = Set Interrupt
13	PBE13	W	0h	PBE13 event 0h = Writing 0 has no effect 1h = Set Interrupt
12	PBE12	W	0h	PBE12 event 0h = Writing 0 has no effect 1h = Set Interrupt
11	PBE11	W	0h	PBE11 event 0h = Writing 0 has no effect 1h = Set Interrupt
10	PBE10	W	0h	PBE10 event 0h = Writing 0 has no effect 1h = Set Interrupt
9	PBE9	W	0h	PBE9 event 0h = Writing 0 has no effect 1h = Set Interrupt
8	PBE8	W	0h	PBE8 event 0h = Writing 0 has no effect 1h = Set Interrupt
7	PBE7	W	0h	PBE7 event 0h = Writing 0 has no effect 1h = Set Interrupt
6	PBE6	W	0h	PBE6 event 0h = Writing 0 has no effect 1h = Set Interrupt
5	PBE5	W	0h	PBE5 event 0h = Writing 0 has no effect 1h = Set Interrupt
4	PBE4	W	0h	PBE4 event 0h = Writing 0 has no effect 1h = Set Interrupt
3	PBE3	W	0h	PBE3 event 0h = Writing 0 has no effect 1h = Set Interrupt
2	PBE2	W	0h	PBE2 event 0h = Writing 0 has no effect 1h = Set Interrupt
1	PBE1	W	0h	PBE1 event 0h = Writing 0 has no effect 1h = Set Interrupt
0	PBE0	W	0h	PBE0 event 0h = Writing 0 has no effect 1h = Set Interrupt

28.5.22 ICLR2 Register (Offset = D4h) [Reset = 00000000h]

ICLR2 is shown in Table 28-25.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Table 28-25. ICLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	SYSTIM2	W	0h	SYSTIM2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
29	SYSTIM1	W	0h	SYSTIM1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
28	SYSTIM0	W	0h	SYSTIM0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
27	MDMDONE	W	0h	MDMDONE event 0h = Writing 0 has no effect 1h = Clear Interrupt
26	MDMIN	W	0h	MDMIN event 0h = Writing 0 has no effect 1h = Clear Interrupt
25	MDMOUT	W	0h	MDMOUT event 0h = Writing 0 has no effect 1h = Clear Interrupt
24	MDMSOFT2	W	0h	MDMSOFT2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
23	MDMSOFT1	W	0h	MDMSOFT1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
22	MDMSOFT0	W	0h	MDMSOFT0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
21	RFEDONE	W	0h	RFEDONE event 0h = Writing 0 has no effect 1h = Clear Interrupt
20	RFESOFT1	W	0h	RFESOFT1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
19	RFESOFT0	W	0h	RFESOFT0 event 0h = Writing 0 has no effect 1h = Clear Interrupt
18	LOCK	W	0h	LOCK event 0h = Writing 0 has no effect 1h = Clear Interrupt
17	LOL	W	0h	LOSS_OF_LOCK event 0h = Writing 0 has no effect 1h = Clear Interrupt
16	TXFIFO	W	0h	TXFIFO event 0h = Writing 0 has no effect 1h = Clear Interrupt
15	RXFIFO	W	0h	RXFIFO event 0h = Writing 0 has no effect 1h = Clear Interrupt

Table 28-25. ICLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	PBE15	W	0h	PBE15 event 0h = Writing 0 has no effect 1h = Clear Interrupt
13	PBE14	W	0h	PBE14 event 0h = Writing 0 has no effect 1h = Clear Interrupt
12	PBE13	W	0h	PBE13 event 0h = Writing 0 has no effect 1h = Clear Interrupt
11	PBE12	W	0h	PBE12 event 0h = Writing 0 has no effect 1h = Clear Interrupt
10	PBE11	W	0h	PBE11 event 0h = Writing 0 has no effect 1h = Clear Interrupt
9	PBE10	W	0h	PBE10 event 0h = Writing 0 has no effect 1h = Clear Interrupt
8	PBE9	W	0h	PBE9 event 0h = Writing 0 has no effect 1h = Clear Interrupt
7	PBE8	W	0h	PBE8 event 0h = Writing 0 has no effect 1h = Clear Interrupt
6	PBE6	W	0h	PBE6 event 0h = Writing 0 has no effect 1h = Clear Interrupt
5	PBE5	W	0h	PBE5 event 0h = Writing 0 has no effect 1h = Clear Interrupt
4	PBE4	W	0h	PBE4 event 0h = Writing 0 has no effect 1h = Clear Interrupt
3	PBE3	W	0h	PBE3 event 0h = Writing 0 has no effect 1h = Clear Interrupt
2	PBE2	W	0h	PBE2 event 0h = Writing 0 has no effect 1h = Clear Interrupt
1	PBE1	W	0h	PBE1 event 0h = Writing 0 has no effect 1h = Clear Interrupt
0	PBE0	W	0h	PBE0 event 0h = Writing 0 has no effect 1h = Clear Interrupt

28.6 LRFDMDM32 Registers

Table 28-26 lists the memory-mapped registers for the LRFDMDM32 registers. All register offset addresses not listed in Table 28-26 should be considered as reserved locations and the register contents should not be modified.

Table 28-26. LRFDMDM32 Registers

Offset	Acronym	Register Name	Section
0h	FWSRC_ENABLE	Internal. Only to be used through TI provided API.	Section 28.6.1
4h	INIT	Internal. Only to be used through TI provided API.	Section 28.6.2
8h	DEMENABLE1_DEMENABLE0	Internal. Only to be used through TI provided API.	Section 28.6.3
Ch	DEMINIT1_DEMINIT0	Internal. Only to be used through TI provided API.	Section 28.6.4
10h	STRB1_STRB0	Internal. Only to be used through TI provided API.	Section 28.6.5
14h	EVT1_EVT0	Internal. Only to be used through TI provided API.	Section 28.6.6
18h	EVT2	Internal. Only to be used through TI provided API.	Section 28.6.7
1Ch	EVTMSK1_EVTMSK0	Internal. Only to be used through TI provided API.	Section 28.6.8
20h	EVTMSK2	Internal. Only to be used through TI provided API.	Section 28.6.9
24h	EVTCLR1_EVTCLR0	Internal. Only to be used through TI provided API.	Section 28.6.10
28h	EVTCLR2	Internal. Only to be used through TI provided API.	Section 28.6.11
2Ch	API_PDREQ	Internal. Only to be used through TI provided API.	Section 28.6.12
30h	CMDPAR1_CMDPAR0	Internal. Only to be used through TI provided API.	Section 28.6.13
34h	MSGBOX_CMDPAR2	Internal. Only to be used through TI provided API.	Section 28.6.14
38h	FIFOWR_FREQ	Internal. Only to be used through TI provided API.	Section 28.6.15
3Ch	FIFORD	Internal. Only to be used through TI provided API.	Section 28.6.16
40h	FIFORDCTRL_FIFOWRCTRL	Internal. Only to be used through TI provided API.	Section 28.6.17
44h	FIFOSTA_PBEDATOUT1	Internal. Only to be used through TI provided API.	Section 28.6.18
48h	RFEDATIN0_RFEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.6.19
4Ch	RFECMDIN_RFECMDOUT	Internal. Only to be used through TI provided API.	Section 28.6.20
50h	PBEDATIN0_PBEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.6.21
54h	PBECMDIN_PBECMDOUT	Internal. Only to be used through TI provided API.	Section 28.6.22
58h	PBEEVTMUX_LQIEST	Internal. Only to be used through TI provided API.	Section 28.6.23
5Ch	SYSTIMEVTMUX1_SYSTIMEVTMUX0	Internal. Only to be used through TI provided API.	Section 28.6.24
60h	MODPRECTRL_ADCDIGCONF	Internal. Only to be used through TI provided API.	Section 28.6.25
64h	MODSYMMAP1_MODSYMMAP0	Internal. Only to be used through TI provided API.	Section 28.6.26
68h	BAUD_MODSOFTTX	Internal. Only to be used through TI provided API.	Section 28.6.27
6Ch	MODMAIN_BAUDPRE	Internal. Only to be used through TI provided API.	Section 28.6.28
70h	DEMMISC1_DEMMISC0	Internal. Only to be used through TI provided API.	Section 28.6.29
74h	DEMMISC3_DEMMISC2	Internal. Only to be used through TI provided API.	Section 28.6.30
78h	DEMDSBU_DEMIQMC0	Internal. Only to be used through TI provided API.	Section 28.6.31
7Ch	DEMCODC0_DEMDSBU2	Internal. Only to be used through TI provided API.	Section 28.6.32
80h	DEMFEXB0_DEMFIDC0	Internal. Only to be used through TI provided API.	Section 28.6.33
84h	DEMMAFI0_DEMFIFE0	Internal. Only to be used through TI provided API.	Section 28.6.34
88h	DEMMAFI2_DEMMAFI1	Internal. Only to be used through TI provided API.	Section 28.6.35
8Ch	DEMC1BE1_DEMC1BE0	Internal. Only to be used through TI provided API.	Section 28.6.36
90h	SPARE0_DEMC1BE2	Internal. Only to be used through TI provided API.	Section 28.6.37
94h	SPARE2_SPARE1	Internal. Only to be used through TI provided API.	Section 28.6.38
98h	DEMSWQU0_SPARE3	Internal. Only to be used through TI provided API.	Section 28.6.39
9Ch	DEMC1BEREF1_DEMC1BEREF0	Internal. Only to be used through TI provided API.	Section 28.6.40

Table 28-26. LRFDMDM32 Registers (continued)

Offset	Acronym	Register Name	Section
A0h	DEMC1BEREF3_DEMC1BEREF2	Internal. Only to be used through TI provided API.	Section 28.6.41
A4h	MODPREAMBLE_MODCTRL	Internal. Only to be used through TI provided API.	Section 28.6.42
A8h	DEMFRAC1_DEMFRAC0	Internal. Only to be used through TI provided API.	Section 28.6.43
ACh	DEMFRAC3_DEMFRAC2	Internal. Only to be used through TI provided API.	Section 28.6.44
B0h	DEMCODC2_DEMCODC1	Internal. Only to be used through TI provided API.	Section 28.6.45
B4h	DEMFIDC2_DEMFIDC1	Internal. Only to be used through TI provided API.	Section 28.6.46
B8h	DEMMAFC0_DEMFIFE1	Internal. Only to be used through TI provided API.	Section 28.6.47
BCh	DEMSWIMBAL_DEMMAFI4	Internal. Only to be used through TI provided API.	Section 28.6.48
C0h	DEMDEBUG_DEMSOFTPDIFF	Internal. Only to be used through TI provided API.	Section 28.6.49
C4h	VITCOMPUTE_VITCTRL	Internal. Only to be used through TI provided API.	Section 28.6.50
C8h	VITSTATE_VITAPMRDBACK	Internal. Only to be used through TI provided API.	Section 28.6.51
CCh	VITBRMETRIC32_VITBRMETRIC10	Internal. Only to be used through TI provided API.	Section 28.6.52
D0h	VITBRMETRIC76_VITBRMETRIC54	Internal. Only to be used through TI provided API.	Section 28.6.53
D4h	DEMD2XB0_DEMDSXB0	Internal. Only to be used through TI provided API.	Section 28.6.54
F0h	TIMCTL	Internal. Only to be used through TI provided API.	Section 28.6.55
F4h	TIMPER_TIMINC	Internal. Only to be used through TI provided API.	Section 28.6.56
F8h	TIMCAPT_TIMCNT	Internal. Only to be used through TI provided API.	Section 28.6.57
FCh	COUNT1IN_TIMEBASE	Internal. Only to be used through TI provided API.	Section 28.6.58
100h	COUNT1RES	Internal. Only to be used through TI provided API.	Section 28.6.59
104h	BRMACC2_BRMACC1	Internal. Only to be used through TI provided API.	Section 28.6.60
108h	MCETRCSTAT_MCETRCCTRL	Internal. Only to be used through TI provided API.	Section 28.6.61
10Ch	MCETRCPAR0_MCETRCCMD	Internal. Only to be used through TI provided API.	Section 28.6.62
110h	RDCAPT0_MCETRCPAR1	Internal. Only to be used through TI provided API.	Section 28.6.63
114h	FECAPT0_RDCAPT1	Internal. Only to be used through TI provided API.	Section 28.6.64
118h	DSCAPT0_FECAPT1	Internal. Only to be used through TI provided API.	Section 28.6.65
11Ch	DSCAPT2_DSCAPT1	Internal. Only to be used through TI provided API.	Section 28.6.66
120h	DEMSWQU1_DSCAPT3	Internal. Only to be used through TI provided API.	Section 28.6.67
124h	GPOCTRL1_GPOCTRL0	Internal. Only to be used through TI provided API.	Section 28.6.68
128h	RFEMAXRSSI_RFERSSI	Internal. Only to be used through TI provided API.	Section 28.6.69
12Ch	SYNC0_RFEDBGAIN	Internal. Only to be used through TI provided API.	Section 28.6.70
130h	SYNC2_SYNC1	Internal. Only to be used through TI provided API.	Section 28.6.71
134h	SYNC3	Internal. Only to be used through TI provided API.	Section 28.6.72
138h	DEMHDIS0	Internal. Only to be used through TI provided API.	Section 28.6.73
13Ch	DEMCOHR1_DEMCOHR0	Internal. Only to be used through TI provided API.	Section 28.6.74
140h	DEMCOHR3_DEMCOHR2	Internal. Only to be used through TI provided API.	Section 28.6.75
144h	DEMCOHR5_DEMCOHR4	Internal. Only to be used through TI provided API.	Section 28.6.76
148h	DEMCOHR7_DEMCOHR6	Internal. Only to be used through TI provided API.	Section 28.6.77
14Ch	DEMCOHR9_DEMCOHR8	Internal. Only to be used through TI provided API.	Section 28.6.78
150h	BAUDCOMP	Internal. Only to be used through TI provided API.	Section 28.6.79
158h	DEMFB2P0_DEMCMIX2	Internal. Only to be used through TI provided API.	Section 28.6.80
15Ch	DEMFB2P2_DEMFB2P1	Internal. Only to be used through TI provided API.	Section 28.6.81
160h	DEMDSBU0	Internal. Only to be used through TI provided API.	Section 28.6.82
164h	DEMDSBU3_DEMDSBU1	Internal. Only to be used through TI provided API.	Section 28.6.83
168h	DEMPHAC1_DEMPHAC0	Internal. Only to be used through TI provided API.	Section 28.6.84
16Ch	DEMPHAC3_DEMPHAC2	Internal. Only to be used through TI provided API.	Section 28.6.85

Table 28-26. LRFDMDM32 Registers (continued)

Offset	Acronym	Register Name	Section
170h	DEMPHAC5_DEMPHAC4	Internal. Only to be used through TI provided API.	Section 28.6.86
174h	DEMPHAC7_DEMPHAC6	Internal. Only to be used through TI provided API.	Section 28.6.87
178h	DEMPHAC9_DEMPHAC8	Internal. Only to be used through TI provided API.	Section 28.6.88
17Ch	DEMC1BEREF5_DEMC1BEREF4	Internal. Only to be used through TI provided API.	Section 28.6.89
180h	DEMC1BEREF7_DEMC1BEREF6	Internal. Only to be used through TI provided API.	Section 28.6.90
184h	DEMC1BE4_DEMC1BE3	Internal. Only to be used through TI provided API.	Section 28.6.91
188h	DEMC1BE6_DEMC1BE5	Internal. Only to be used through TI provided API.	Section 28.6.92
18Ch	DEMC1BE8_DEMC1BE7	Internal. Only to be used through TI provided API.	Section 28.6.93
190h	DEMC1BE10_DEMC1BE9	Internal. Only to be used through TI provided API.	Section 28.6.94
194h	DEMC1BE12_DEMC1BE11	Internal. Only to be used through TI provided API.	Section 28.6.95
198h	DEMC1BE14_DEMC1BE13	Internal. Only to be used through TI provided API.	Section 28.6.96
19Ch	DEMC1BE15	Internal. Only to be used through TI provided API.	Section 28.6.97
1A4h	DEMC1BE20	Internal. Only to be used through TI provided API.	Section 28.6.98
1A8h	STRB2	Internal. Only to be used through TI provided API.	Section 28.6.99
1ACh	EVTMSK3_EVT3	Internal. Only to be used through TI provided API.	Section 28.6.100
1B0h	EVTCLR3	Internal. Only to be used through TI provided API.	Section 28.6.101

Complex bit access types are encoded to fit into small table cells. Table 28-27 shows the codes that are used for access types in this section.

Table 28-27. LRFDMDM32 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.6.1 FWSRC_ENABLE Register (Offset = 0h) [Reset = 00000000h]

FWSRC_ENABLE is shown in Table 28-28.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-28. FWSRC_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	DATARAM	R/W	0h	Internal. Only to be used through TI provided API.
17	FWRAM	R/W	0h	Internal. Only to be used through TI provided API.
16	BANK	R/W	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5	ADCDIG	R/W	0h	Internal. Only to be used through TI provided API.
4	DEMODULATOR	R/W	0h	Internal. Only to be used through TI provided API.
3	MODULATOR	R/W	0h	Internal. Only to be used through TI provided API.
2	TIMEBASE	R/W	0h	Internal. Only to be used through TI provided API.
1	TXRXFIFO	R/W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	R/W	0h	Internal. Only to be used through TI provided API.

28.6.2 INIT Register (Offset = 4h) [Reset = 00000000h]

INIT is shown in Table 28-29.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-29. INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	ADCDIG	W	0h	Internal. Only to be used through TI provided API.
4	DEMODULATOR	W	0h	Internal. Only to be used through TI provided API.
3	MODULATOR	W	0h	Internal. Only to be used through TI provided API.
2	TIMEBASE	W	0h	Internal. Only to be used through TI provided API.
1	TXRXFIFO	W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	W	0h	Internal. Only to be used through TI provided API.

28.6.3 DEMENABLE1_DEMENABLE0 Register (Offset = 8h) [Reset = 00000000h]

DEMENABLE1_DEMENABLE0 is shown in Table 28-30.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-30. DEMENABLE1_DEMENABLE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	VITE	R/W	0h	Internal. Only to be used through TI provided API.
28	MLSE	R/W	0h	Internal. Only to be used through TI provided API.
27	SOFD	R/W	0h	Internal. Only to be used through TI provided API.
26	SWQU	R/W	0h	Internal. Only to be used through TI provided API.
25	MAFC	R/W	0h	Internal. Only to be used through TI provided API.
24	MAFI	R/W	0h	Internal. Only to be used through TI provided API.
23	FIFE	R/W	0h	Internal. Only to be used through TI provided API.
22	PDIF	R/W	0h	Internal. Only to be used through TI provided API.
21	CA2P	R/W	0h	Internal. Only to be used through TI provided API.
20	C1BE	R/W	0h	Internal. Only to be used through TI provided API.
19	LQIE	R/W	0h	Internal. Only to be used through TI provided API.
18	F4BA	R/W	0h	Internal. Only to be used through TI provided API.
17	STIM	R/W	0h	Internal. Only to be used through TI provided API.
16	DSBU	R/W	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14	PHASECORR	R/W	0h	Internal. Only to be used through TI provided API.
13	COHR	R/W	0h	Internal. Only to be used through TI provided API.
12	SINF	R/W	0h	Internal. Only to be used through TI provided API.
11	PDIF2	R/W	0h	Internal. Only to be used through TI provided API.
10	HILBDISC	R/W	0h	Internal. Only to be used through TI provided API.
9	FB2PLL	R/W	0h	Internal. Only to be used through TI provided API.
8	FRAC	R/W	0h	Internal. Only to be used through TI provided API.
7	FIDC	R/W	0h	Internal. Only to be used through TI provided API.
6	CHFI	R/W	0h	Internal. Only to be used through TI provided API.
5	BDEC	R/W	0h	Internal. Only to be used through TI provided API.
4	IQMC	R/W	0h	Internal. Only to be used through TI provided API.
3	MGE1	R/W	0h	Internal. Only to be used through TI provided API.
2	MGE0	R/W	0h	Internal. Only to be used through TI provided API.
1	CODC	R/W	0h	Internal. Only to be used through TI provided API.
0	CMIX	R/W	0h	Internal. Only to be used through TI provided API.

28.6.4 DEMINIT1_DEMINIT0 Register (Offset = Ch) [Reset = 00000000h]

DEMINIT1_DEMINIT0 is shown in Table 28-31.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-31. DEMINIT1_DEMINIT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	VITE	W	0h	Internal. Only to be used through TI provided API.
28	MLSE	W	0h	Internal. Only to be used through TI provided API.
27	SOFD	W	0h	Internal. Only to be used through TI provided API.
26	SWQU	W	0h	Internal. Only to be used through TI provided API.
25	MAFC	W	0h	Internal. Only to be used through TI provided API.
24	MAFI	W	0h	Internal. Only to be used through TI provided API.
23	FIFE	W	0h	Internal. Only to be used through TI provided API.
22	PDIF	W	0h	Internal. Only to be used through TI provided API.
21	CA2P	W	0h	Internal. Only to be used through TI provided API.
20	C1BE	W	0h	Internal. Only to be used through TI provided API.
19	LQIE	W	0h	Internal. Only to be used through TI provided API.
18	F4BA	W	0h	Internal. Only to be used through TI provided API.
17	STIM	W	0h	Internal. Only to be used through TI provided API.
16	DSBU	W	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14	PHASECORR	W	0h	Internal. Only to be used through TI provided API.
13	COHR	W	0h	Internal. Only to be used through TI provided API.
12	SINF	W	0h	Internal. Only to be used through TI provided API.
11	PDIF2	W	0h	Internal. Only to be used through TI provided API.
10	HILBDISC	W	0h	Internal. Only to be used through TI provided API.
9	FB2PLL	W	0h	Internal. Only to be used through TI provided API.
8	FRAC	W	0h	Internal. Only to be used through TI provided API.
7	FIDC	W	0h	Internal. Only to be used through TI provided API.
6	CHFI	W	0h	Internal. Only to be used through TI provided API.
5	BDEC	W	0h	Internal. Only to be used through TI provided API.
4	IQMC	W	0h	Internal. Only to be used through TI provided API.
3	MGE1	W	0h	Internal. Only to be used through TI provided API.
2	MGE0	W	0h	Internal. Only to be used through TI provided API.
1	CODC	W	0h	Internal. Only to be used through TI provided API.
0	CMIX	W	0h	Internal. Only to be used through TI provided API.

28.6.5 STRB1_STRB0 Register (Offset = 10h) [Reset = 00000000h]

STRB1_STRB0 is shown in Table 28-32.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-32. STRB1_STRB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	S2RTRG	W	0h	Internal. Only to be used through TI provided API.
28	DMATRG	W	0h	Internal. Only to be used through TI provided API.
27	SYSTCAPT2	W	0h	Internal. Only to be used through TI provided API.
26	SYSTCAPT1	W	0h	Internal. Only to be used through TI provided API.
25	SYSTCAPT0	W	0h	Internal. Only to be used through TI provided API.
24	C1BEPEAKAB	W	0h	Internal. Only to be used through TI provided API.
23	C1BEPEAKC	W	0h	Internal. Only to be used through TI provided API.
22	C1BEPEAKB	W	0h	Internal. Only to be used through TI provided API.
21	C1BEPEAKA	W	0h	Internal. Only to be used through TI provided API.
20	C1BEADVANCE	W	0h	Internal. Only to be used through TI provided API.
19	C1BESTALL	W	0h	Internal. Only to be used through TI provided API.
18-17	C1BEROT	W	0h	Internal. Only to be used through TI provided API.
16	C1BECOPY	W	0h	Internal. Only to be used through TI provided API.
15	COHRIEEE	W	0h	Internal. Only to be used through TI provided API.
14	COHRFOFF	W	0h	Internal. Only to be used through TI provided API.
13	COHRSINGLE	W	0h	Internal. Only to be used through TI provided API.
12	RESERVED	R	0h	Reserved
11	TIMBADVANCE	W	0h	Internal. Only to be used through TI provided API.
10	TIMBSTALL	W	0h	Internal. Only to be used through TI provided API.
9	EVT5	W	0h	Internal. Only to be used through TI provided API.
8	EVT4	W	0h	Internal. Only to be used through TI provided API.
7	MLSETERM	W	0h	Internal. Only to be used through TI provided API.
6	EVT3	W	0h	Internal. Only to be used through TI provided API.
5	EVT2	W	0h	Internal. Only to be used through TI provided API.
4	EVT1	W	0h	Internal. Only to be used through TI provided API.
3	EVT0	W	0h	Internal. Only to be used through TI provided API.
2	TIMBALIGN	W	0h	Internal. Only to be used through TI provided API.
1	DSBURST	W	0h	Internal. Only to be used through TI provided API.
0	CMDDONE	W	0h	Internal. Only to be used through TI provided API.

28.6.6 EVT1_EVT0 Register (Offset = 14h) [Reset = 00000000h]

EVT1_EVT0 is shown in Table 28-33.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-33. EVT1_EVT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	COHRFSM	R	0h	Internal. Only to be used through TI provided API.
26	COHRBUF	R	0h	Internal. Only to be used through TI provided API.
25	COHRUPD	R	0h	Internal. Only to be used through TI provided API.
24	REFCLK	R	0h	Internal. Only to be used through TI provided API.
23	S2RSTOP	R	0h	Internal. Only to be used through TI provided API.
22	SWQUFALSESYNC	R	0h	Internal. Only to be used through TI provided API.
21	SWQUSYNCED	R	0h	Internal. Only to be used through TI provided API.
20	CLKENBAUDF	R	0h	Internal. Only to be used through TI provided API.
19	FIFORVALID	R	0h	Internal. Only to be used through TI provided API.
18	FIFOWREADY	R	0h	Internal. Only to be used through TI provided API.
17	CLKENBAUD	R	0h	Internal. Only to be used through TI provided API.
16	PREAMBLEDONE	R	0h	Internal. Only to be used through TI provided API.
15	PBEDAT	R	0h	Internal. Only to be used through TI provided API.
14	PBECMD	R	0h	Internal. Only to be used through TI provided API.
13	RFEDAT	R	0h	Internal. Only to be used through TI provided API.
12	BDEC	R	0h	Internal. Only to be used through TI provided API.
11	FRAC	R	0h	Internal. Only to be used through TI provided API.
10	SYSTIMEVT2	R	0h	Internal. Only to be used through TI provided API.
9	SYSTIMEVT1	R	0h	Internal. Only to be used through TI provided API.
8	SYSTIMEVT0	R	0h	Internal. Only to be used through TI provided API.
7	FIFOWR	R	0h	Internal. Only to be used through TI provided API.
6	COUNTER	R	0h	Internal. Only to be used through TI provided API.
5	RFECMD	R	0h	Internal. Only to be used through TI provided API.
4	FIFOOVFL	R	0h	Internal. Only to be used through TI provided API.
3	FIFOUNFL	R	0h	Internal. Only to be used through TI provided API.
2	CLKEN4BAUD	R	0h	Internal. Only to be used through TI provided API.
1	TIMER	R	0h	Internal. Only to be used through TI provided API.
0	MDMAPI	R	0h	Internal. Only to be used through TI provided API.

28.6.7 EVT2 Register (Offset = 18h) [Reset = 00000000h]

EVT2 is shown in Table 28-34.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-34. EVT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	GPI1	R	0h	Internal. Only to be used through TI provided API.
14	GPI0	R	0h	Internal. Only to be used through TI provided API.
13	RESERVED	R	0h	Reserved
12	FIDCESTRDY	R	0h	Internal. Only to be used through TI provided API.
11	C1BECMBANY	R	0h	Internal. Only to be used through TI provided API.
10	C1BECMBNEG	R	0h	Internal. Only to be used through TI provided API.
9	C1BECMBPOS	R	0h	Internal. Only to be used through TI provided API.
8	C1BECANY	R	0h	Internal. Only to be used through TI provided API.
7	C1BECNEG	R	0h	Internal. Only to be used through TI provided API.
6	C1BECPOS	R	0h	Internal. Only to be used through TI provided API.
5	C1BEBANY	R	0h	Internal. Only to be used through TI provided API.
4	C1BEBNEG	R	0h	Internal. Only to be used through TI provided API.
3	C1BEBPOS	R	0h	Internal. Only to be used through TI provided API.
2	C1BEAANY	R	0h	Internal. Only to be used through TI provided API.
1	C1BEANEG	R	0h	Internal. Only to be used through TI provided API.
0	C1BEAPOS	R	0h	Internal. Only to be used through TI provided API.

28.6.8 EVTMSK1_EVTMSK0 Register (Offset = 1Ch) [Reset = 00000000h]

EVTMSK1_EVTMSK0 is shown in Table 28-35.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-35. EVTMSK1_EVTMSK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	COHRFSM	R/W	0h	Internal. Only to be used through TI provided API.
26	COHRBUF	R/W	0h	Internal. Only to be used through TI provided API.
25	COHRUPD	R/W	0h	Internal. Only to be used through TI provided API.
24	REFCLK	R/W	0h	Internal. Only to be used through TI provided API.
23	S2RSTOP	R/W	0h	Internal. Only to be used through TI provided API.
22	SWQUFALSESYNC	R/W	0h	Internal. Only to be used through TI provided API.
21	SWQUSYNCED	R/W	0h	Internal. Only to be used through TI provided API.
20	CLKENBAUDF	R/W	0h	Internal. Only to be used through TI provided API.
19	FIFORVALID	R/W	0h	Internal. Only to be used through TI provided API.
18	FIFOWREADY	R/W	0h	Internal. Only to be used through TI provided API.
17	CLKENBAUD	R/W	0h	Internal. Only to be used through TI provided API.
16	PREAMBLEDONE	R/W	0h	Internal. Only to be used through TI provided API.
15	PBEDAT	R/W	0h	Internal. Only to be used through TI provided API.
14	PBECMD	R/W	0h	Internal. Only to be used through TI provided API.
13	RFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
12	BDEC	R/W	0h	Internal. Only to be used through TI provided API.
11	FRAC	R/W	0h	Internal. Only to be used through TI provided API.
10	SYSTIMEVT2	R/W	0h	Internal. Only to be used through TI provided API.
9	SYSTIMEVT1	R/W	0h	Internal. Only to be used through TI provided API.
8	SYSTIMEVT0	R/W	0h	Internal. Only to be used through TI provided API.
7	FIFOWR	R/W	0h	Internal. Only to be used through TI provided API.
6	COUNTER	R/W	0h	Internal. Only to be used through TI provided API.
5	RFECMD	R/W	0h	Internal. Only to be used through TI provided API.
4	FIFOOVFL	R/W	0h	Internal. Only to be used through TI provided API.
3	FIFOUNFL	R/W	0h	Internal. Only to be used through TI provided API.
2	CLKEN4BAUD	R/W	0h	Internal. Only to be used through TI provided API.
1	TIMER	R/W	0h	Internal. Only to be used through TI provided API.
0	MDMAPI	R/W	0h	Internal. Only to be used through TI provided API.

28.6.9 EVTMSK2 Register (Offset = 20h) [Reset = 00000000h]

EVTMSK2 is shown in Table 28-36.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-36. EVTMSK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	GPI1	R/W	0h	Internal. Only to be used through TI provided API.
14	GPI0	R/W	0h	Internal. Only to be used through TI provided API.
13	RESERVED	R	0h	Reserved
12	FIDCESTRDY	R/W	0h	Internal. Only to be used through TI provided API.
11	C1BECMBANY	R/W	0h	Internal. Only to be used through TI provided API.
10	C1BECMBNEG	R/W	0h	Internal. Only to be used through TI provided API.
9	C1BECMBPOS	R/W	0h	Internal. Only to be used through TI provided API.
8	C1BECANY	R/W	0h	Internal. Only to be used through TI provided API.
7	C1BECNEG	R/W	0h	Internal. Only to be used through TI provided API.
6	C1BECPOS	R/W	0h	Internal. Only to be used through TI provided API.
5	C1BEBANY	R/W	0h	Internal. Only to be used through TI provided API.
4	C1BEBNEG	R/W	0h	Internal. Only to be used through TI provided API.
3	C1BEBPOS	R/W	0h	Internal. Only to be used through TI provided API.
2	C1BEAANY	R/W	0h	Internal. Only to be used through TI provided API.
1	C1BEANEG	R/W	0h	Internal. Only to be used through TI provided API.
0	C1BEAPOS	R/W	0h	Internal. Only to be used through TI provided API.

28.6.10 EVTCLR1_EVTCLR0 Register (Offset = 24h) [Reset = 00000000h]

EVTCLR1_EVTCLR0 is shown in Table 28-37.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-37. EVTCLR1_EVTCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	COHRFSM	W	0h	Internal. Only to be used through TI provided API.
26	COHRBUF	W	0h	Internal. Only to be used through TI provided API.
25	COHRUPD	W	0h	Internal. Only to be used through TI provided API.
24	REFCLK	W	0h	Internal. Only to be used through TI provided API.
23	S2RSTOP	W	0h	Internal. Only to be used through TI provided API.
22	SWQUFALSESYNC	W	0h	Internal. Only to be used through TI provided API.
21	SWQUSYNCED	W	0h	Internal. Only to be used through TI provided API.
20	CLKENBAUDF	W	0h	Internal. Only to be used through TI provided API.
19	FIFORVALID	W	0h	Internal. Only to be used through TI provided API.
18	FIFOWREADY	W	0h	Internal. Only to be used through TI provided API.
17	CLKENBAUD	W	0h	Internal. Only to be used through TI provided API.
16	PREAMBLEDONE	W	0h	Internal. Only to be used through TI provided API.
15	PBEDAT	W	0h	Internal. Only to be used through TI provided API.
14	PBECMD	W	0h	Internal. Only to be used through TI provided API.
13	RFEDAT	W	0h	Internal. Only to be used through TI provided API.
12	BDEC	W	0h	Internal. Only to be used through TI provided API.
11	FRAC	W	0h	Internal. Only to be used through TI provided API.
10	SYSTIMEVT2	W	0h	Internal. Only to be used through TI provided API.
9	SYSTIMEVT1	W	0h	Internal. Only to be used through TI provided API.
8	SYSTIMEVT0	W	0h	Internal. Only to be used through TI provided API.
7	FIFOWR	W	0h	Internal. Only to be used through TI provided API.
6	COUNTER	W	0h	Internal. Only to be used through TI provided API.
5	RFECMD	W	0h	Internal. Only to be used through TI provided API.
4	FIFOOVFL	W	0h	Internal. Only to be used through TI provided API.
3	FIFOUNFL	W	0h	Internal. Only to be used through TI provided API.
2	CLKEN4BAUD	W	0h	Internal. Only to be used through TI provided API.
1	TIMER	W	0h	Internal. Only to be used through TI provided API.
0	MDMAPI	W	0h	Internal. Only to be used through TI provided API.

28.6.11 EVTCLR2 Register (Offset = 28h) [Reset = 00000000h]

EVTCLR2 is shown in Table 28-38.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-38. EVTCLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	GPI1	W	0h	Internal. Only to be used through TI provided API.
14	GPI0	W	0h	Internal. Only to be used through TI provided API.
13	RESERVED	R	0h	Reserved
12	FIDCESTRDY	W	0h	Internal. Only to be used through TI provided API.
11	C1BECMBANY	W	0h	Internal. Only to be used through TI provided API.
10	C1BECMBNEG	W	0h	Internal. Only to be used through TI provided API.
9	C1BECMBPOS	W	0h	Internal. Only to be used through TI provided API.
8	C1BECANY	W	0h	Internal. Only to be used through TI provided API.
7	C1BECNEG	W	0h	Internal. Only to be used through TI provided API.
6	C1BECPOS	W	0h	Internal. Only to be used through TI provided API.
5	C1BEBANY	W	0h	Internal. Only to be used through TI provided API.
4	C1BEBNEG	W	0h	Internal. Only to be used through TI provided API.
3	C1BEBPOS	W	0h	Internal. Only to be used through TI provided API.
2	C1BEAANY	W	0h	Internal. Only to be used through TI provided API.
1	C1BEANEG	W	0h	Internal. Only to be used through TI provided API.
0	C1BEAPOS	W	0h	Internal. Only to be used through TI provided API.

28.6.12 API_PDREQ Register (Offset = 2Ch) [Reset = 00000000h]

API_PDREQ is shown in Table 28-39.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-39. API_PDREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	PROTOCOLID	R	0h	Internal. Only to be used through TI provided API.
19-16	MDMCMD	R	0h	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	TOPSMPDREQ	R/W	0h	Internal. Only to be used through TI provided API.

28.6.13 CMDPAR1_CMDPAR0 Register (Offset = 30h) [Reset = 00000000h]

CMDPAR1_CMDPAR0 is shown in Table 28-40.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-40. CMDPAR1_CMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMDPAR1_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	CMDPAR0_VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.14 MSGBOX_CMDPAR2 Register (Offset = 34h) [Reset = 00000000h]

MSGBOX_CMDPAR2 is shown in Table 28-41.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-41. MSGBOX_CMDPAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MSGBOX_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CMDPAR2_VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.15 FIFOWR_FREQ Register (Offset = 38h) [Reset = 00000000h]

FIFOWR_FREQ is shown in Table 28-42.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-42. FIFOWR_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAYLOADIN	R/W	0h	Internal. Only to be used through TI provided API.
15-0	OFFSET	R/W	0h	Internal. Only to be used through TI provided API.

28.6.16 FIFORD Register (Offset = 3Ch) [Reset = 00000000h]

FIFORD is shown in Table 28-43.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-43. FIFORD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PAYLOADOUT	R	0h	Internal. Only to be used through TI provided API.

28.6.17 FIFORDCTRL_FIFOWRCTRL Register (Offset = 40h) [Reset = 00000000h]

FIFORDCTRL_FIFOWRCTRL is shown in Table 28-44.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-44. FIFORDCTRL_FIFOWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-20	FIFORDPORT	R/W	0h	Internal. Only to be used through TI provided API.
19-16	WORDSZRD	R/W	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5-4	FIFOWRPORT	R/W	0h	Internal. Only to be used through TI provided API.
3-0	WORDSZWR	R/W	0h	Internal. Only to be used through TI provided API.

28.6.18 FIFOSTA_PBEDATOUT1 Register (Offset = 44h) [Reset = 00000000h]

FIFOSTA_PBEDATOUT1 is shown in Table 28-45.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-45. FIFOSTA_PBEDATOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	OVERFLOW	R	0h	Internal. Only to be used through TI provided API.
20	ALMOSTFULL	R	0h	Internal. Only to be used through TI provided API.
19	ALMOSTEMPTY	R	0h	Internal. Only to be used through TI provided API.
18	UNDERFLOW	R	0h	Internal. Only to be used through TI provided API.
17	RXVALID	R	0h	Internal. Only to be used through TI provided API.
16	TXREADY	R	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.19 RFEDATIN0_RFEDATOUT0 Register (Offset = 48h) [Reset = 00000000h]

RFEDATIN0_RFEDATOUT0 is shown in Table 28-46.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-46. RFEDATIN0_RFEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RFEDATIN0_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	RFEDATOUT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.20 RFECMDIN_RFECMDOUT Register (Offset = 4Ch) [Reset = 00000000h]

RFECMDIN_RFECMDOUT is shown in Table 28-47.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-47. RFECMDIN_RFECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RFECMDIN_VAL	R	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	RFECMDOUT_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.21 PBEDATIN0_PBEDATOUT0 Register (Offset = 50h) [Reset = 00000000h]

PBEDATIN0_PBEDATOUT0 is shown in Table 28-48.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-48. PBEDATIN0_PBEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PBEDATIN0_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	PBEDATOUT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.22 PBECMDIN_PBECMDOUT Register (Offset = 54h) [Reset = 00000000h]

PBECMDIN_PBECMDOUT is shown in Table 28-49.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-49. PBECMDIN_PBECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	PBECMDIN_VAL	R	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	PBECMDOUT_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.23 PBEEVTMUX_LQIEST Register (Offset = 58h) [Reset = 00000000h]

PBEEVTMUX_LQIEST is shown in Table 28-50.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-50. PBEEVTMUX_LQIEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-16	SEL	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.24 SYSTIMEVTMUX1_SYSTIMEVTMUX0 Register (Offset = 5Ch) [Reset = 00000000h]

SYSTIMEVTMUX1_SYSTIMEVTMUX0 is shown in Table 28-51.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-51. SYSTIMEVTMUX1_SYSTIMEVTMUX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-16	SEL2	R/W	0h	Internal. Only to be used through TI provided API.
15-12	RESERVED	R	0h	Reserved
11-6	SEL1	R/W	0h	Internal. Only to be used through TI provided API.
5-0	SEL0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.25 MODPRECTRL_ADCDIGCONF Register (Offset = 60h) [Reset = 00000000h]

MODPRECTRL_ADCDIGCONF is shown in Table 28-52.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-52. MODPRECTRL_ADCDIGCONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	REPS	R/W	0h	Internal. Only to be used through TI provided API.
19-16	SIZE	R/W	0h	Internal. Only to be used through TI provided API.
15-2	RESERVED	R	0h	Reserved
1	QBRANCHEN	R/W	0h	Internal. Only to be used through TI provided API.
0	IBRANCHEN	R/W	0h	Internal. Only to be used through TI provided API.

28.6.26 MODSYMMAP1_MODSYMMAP0 Register (Offset = 64h) [Reset = 00000000h]

MODSYMMAP1_MODSYMMAP0 is shown in Table 28-53.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-53. MODSYMMAP1_MODSYMMAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	SYM7	R/W	0h	Internal. Only to be used through TI provided API.
27-24	SYM6	R/W	0h	Internal. Only to be used through TI provided API.
23-20	SYM5	R/W	0h	Internal. Only to be used through TI provided API.
19-16	SYM4	R/W	0h	Internal. Only to be used through TI provided API.
15-12	SYM3	R/W	0h	Internal. Only to be used through TI provided API.
11-8	SYM2	R/W	0h	Internal. Only to be used through TI provided API.
7-4	SYM1	R/W	0h	Internal. Only to be used through TI provided API.
3-0	SYM0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.27 BAUD_MODSOFTTX Register (Offset = 68h) [Reset = 00000000h]

BAUD_MODSOFTTX is shown in Table 28-54.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-54. BAUD_MODSOFTTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RATEWORD	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	SOFTSYMBOL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.28 MODMAIN_BAUDPRE Register (Offset = 6Ch) [Reset = 00000000h]

MODMAIN_BAUDPRE is shown in Table 28-55.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-55. MODMAIN_BAUDPRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-18	FECSELECT	R/W	0h	Internal. Only to be used through TI provided API.
17-16	MODLEVELS	R/W	0h	Internal. Only to be used through TI provided API.
15-13	ALIGNVALUE	R/W	0h	Internal. Only to be used through TI provided API.
12-8	EXTRATEWORD	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PRESCALER	R/W	0h	Internal. Only to be used through TI provided API.

28.6.29 DEMMISC1_DEMMISC0 Register (Offset = 70h) [Reset = 00000000h]

DEMMISC1_DEMMISC0 is shown in Table 28-56.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-56. DEMMISC1_DEMMISC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	CDCTGAINMA	R/W	0h	Internal. Only to be used through TI provided API.
23-21	CDCTGAINEX	R/W	0h	Internal. Only to be used through TI provided API.
20	CDCCOLRST	R/W	0h	Internal. Only to be used through TI provided API.
19-18	MGE1SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
17-16	CHFIBW	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12-10	CMIXNFINE	R/W	0h	Internal. Only to be used through TI provided API.
9-0	CMIXN	R/W	0h	Internal. Only to be used through TI provided API.

28.6.30 DEMMISC3_DEMMISC2 Register (Offset = 74h) [Reset = 00000000h]

DEMMISC3_DEMMISC2 is shown in Table 28-57.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-57. DEMMISC3_DEMMISC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CDCOVERRIDE	R/W	0h	Internal. Only to be used through TI provided API.
30-29	BDE2DVGA	R/W	0h	Internal. Only to be used through TI provided API.
28	BDE1FILTMODE	R/W	0h	Internal. Only to be used through TI provided API.
27-26	LQIPERIOD	R/W	0h	Internal. Only to be used through TI provided API.
25-24	BDE1DVGA	R/W	0h	Internal. Only to be used through TI provided API.
23	BDE1NUMSTAGES	R/W	0h	Internal. Only to be used through TI provided API.
22-21	PDIFDECIM	R/W	0h	Internal. Only to be used through TI provided API.
20-16	BDE2DECRATIO	R/W	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14	MLSERUN	R/W	0h	Internal. Only to be used through TI provided API.
13-12	MAFCGAIN	R/W	0h	Internal. Only to be used through TI provided API.
11	STIMBYPASS	R/W	0h	Internal. Only to be used through TI provided API.
10	STIMESTONLY	R/W	0h	Internal. Only to be used through TI provided API.
9-7	STIMTEAPERIOD	R/W	0h	Internal. Only to be used through TI provided API.
6-4	STIMTEAGAIN	R/W	0h	Internal. Only to be used through TI provided API.
3	PDIFLINPREDEN	R/W	0h	Internal. Only to be used through TI provided API.
2	PDIFDESPECK	R/W	0h	Internal. Only to be used through TI provided API.
1	PDIFIQCONJEN	R/W	0h	Internal. Only to be used through TI provided API.
0	PDIFLIMITRANGE	R/W	0h	Internal. Only to be used through TI provided API.

28.6.31 DEMDSBU_DEMIQMC0 Register (Offset = 78h) [Reset = 00000000h]

DEMDSBU_DEMIQMC0 is shown in Table 28-58.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-58. DEMDSBU_DEMIQMC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24-16	DSBUDELAY	R/W	0h	Internal. Only to be used through TI provided API.
15-8	GAINFACTOR	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PHASEFACTOR	R/W	0h	Internal. Only to be used through TI provided API.

28.6.32 DEMCODC0_DEMDSBU2 Register (Offset = 7Ch) [Reset = 00000000h]

DEMCODC0_DEMDSBU2 is shown in Table 28-59.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-59. DEMCODC0_DEMDSBU2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	ESTSEL	R/W	0h	Internal. Only to be used through TI provided API.
26-25	COMPSEL	R/W	0h	Internal. Only to be used through TI provided API.
24	IIRUSEINITIAL	R/W	0h	Internal. Only to be used through TI provided API.
23-21	IIRGAIN	R/W	0h	Internal. Only to be used through TI provided API.
20	IIREN	R/W	0h	Internal. Only to be used through TI provided API.
19	ACCMODE	R/W	0h	Internal. Only to be used through TI provided API.
18-17	ACCPERIOD	R/W	0h	Internal. Only to be used through TI provided API.
16	ACCEN	R/W	0h	Internal. Only to be used through TI provided API.
15-9	RESERVED	R	0h	Reserved
8-0	DSBUAVGLENGTH	R/W	0h	Internal. Only to be used through TI provided API.

28.6.33 DEMFEXB0_DEMFIDC0 Register (Offset = 80h) [Reset = 00000000h]

DEMFEXB0_DEMFIDC0 is shown in Table 28-60.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-60. DEMFEXB0_DEMFIDC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	OUT2PASSTHROUGH	R/W	0h	Internal. Only to be used through TI provided API.
28-27	OUT2SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
26	OUT1PASSTHROUGH	R/W	0h	Internal. Only to be used through TI provided API.
25-24	OUT1SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
23-22	B4SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
21-20	B3SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
19-18	B2SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
17-16	B1SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5-4	COMPSEL	R/W	0h	Internal. Only to be used through TI provided API.
3-2	ACCPERIOD	R/W	0h	Internal. Only to be used through TI provided API.
1	ACCMODE	R/W	0h	Internal. Only to be used through TI provided API.
0	ACCEN	R/W	0h	Internal. Only to be used through TI provided API.

28.6.34 DEMMAFI0_DEMFIFE0 Register (Offset = 84h) [Reset = 00000000h]

DEMMAFI0_DEMFIFE0 is shown in Table 28-61.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-61. DEMMAFI0_DEMFIFE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	C1C7	R/W	0h	Internal. Only to be used through TI provided API.
23-16	C0C8	R/W	0h	Internal. Only to be used through TI provided API.
15-12	RESERVED	R	0h	Reserved
11	FINEFOESEL	R/W	0h	Internal. Only to be used through TI provided API.
10-9	FOCFFSEL	R/W	0h	Internal. Only to be used through TI provided API.
8	ACCCNTMODE	R/W	0h	Internal. Only to be used through TI provided API.
7-6	ACCPERIOD	R/W	0h	Internal. Only to be used through TI provided API.
5	ACCEN	R/W	0h	Internal. Only to be used through TI provided API.
4	IIRUSEINITIAL	R/W	0h	Internal. Only to be used through TI provided API.
3-1	IIRGAIN	R/W	0h	Internal. Only to be used through TI provided API.
0	IIREN	R/W	0h	Internal. Only to be used through TI provided API.

28.6.35 DEMMAFI2_DEMMAFI1 Register (Offset = 88h) [Reset = 00000000h]

DEMMAFI2_DEMMAFI1 is shown in Table 28-62.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-62. DEMMAFI2_DEMMAFI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24-16	C4	R/W	0h	Internal. Only to be used through TI provided API.
15-8	C3C5	R/W	0h	Internal. Only to be used through TI provided API.
7-0	C2C6	R/W	0h	Internal. Only to be used through TI provided API.

28.6.36 DEMC1BE1_DEMC1BE0 Register (Offset = 8Ch) [Reset = 00000000h]

DEMC1BE1_DEMC1BE0 is shown in Table 28-63.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-63. DEMC1BE1_DEMC1BE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	THRESHOLDB	R/W	0h	Internal. Only to be used through TI provided API.
23-16	THRESHOLDA	R/W	0h	Internal. Only to be used through TI provided API.
15-11	MASKB	R/W	0h	Internal. Only to be used through TI provided API.
10-6	MASKA	R/W	0h	Internal. Only to be used through TI provided API.
5-4	CASCCONF	R/W	0h	Internal. Only to be used through TI provided API.
3-0	COPYCONF	R/W	0h	Internal. Only to be used through TI provided API.

28.6.37 SPARE0_DEMC1BE2 Register (Offset = 90h) [Reset = 00000000h]

SPARE0_DEMC1BE2 is shown in Table 28-64.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-64. SPARE0_DEMC1BE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-11	RESERVED	R	0h	Reserved
10	PARLOADCONF	R/W	0h	Internal. Only to be used through TI provided API.
9-8	PEAKCONF	R/W	0h	Internal. Only to be used through TI provided API.
7-0	THRESHOLDC	R/W	0h	Internal. Only to be used through TI provided API.

28.6.38 SPARE2_SPARE1 Register (Offset = 94h) [Reset = 00000000h]

SPARE2_SPARE1 is shown in Table 28-65.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-65. SPARE2_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SPARE2_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	SPARE1_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.39 DEMSWQU0_SPARE3 Register (Offset = 98h) [Reset = 00000000h]

DEMSWQU0_SPARE3 is shown in Table 28-66.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-66. DEMSWQU0_SPARE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	SYNCMODE	R/W	0h	Internal. Only to be used through TI provided API.
22	AUTOMAFC	R/W	0h	Internal. Only to be used through TI provided API.
21	RUN	R/W	0h	Internal. Only to be used through TI provided API.
20-16	REFLEN	R/W	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.40 DEMC1BEREF1_DEMC1BEREF0 Register (Offset = 9Ch) [Reset = 00000000h]

DEMC1BEREF1_DEMC1BEREF0 is shown in Table 28-67.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-67. DEMC1BEREF1_DEMC1BEREF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CAR31C16	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CAR15C0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.41 DEMC1BEREF3_DEMC1BEREF2 Register (Offset = A0h) [Reset = 00000000h]

DEMC1BEREF3_DEMC1BEREF2 is shown in Table 28-68.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-68. DEMC1BEREF3_DEMC1BEREF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CBR31C16	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CBR15C0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.42 MODPREAMBLE_MODCTRL Register (Offset = A4h) [Reset = 00000000h]

MODPREAMBLE_MODCTRL is shown in Table 28-69.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-69. MODPREAMBLE_MODCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WORD	R/W	0h	Internal. Only to be used through TI provided API.
15-12	RESERVED	R	0h	Reserved
11	DSBUSEL	R/W	0h	Internal. Only to be used through TI provided API.
10	HDISMODE	R/W	0h	Internal. Only to be used through TI provided API.
9	PARBITQUALEN	R/W	0h	Internal. Only to be used through TI provided API.
8-7	STIMMODE	R/W	0h	Internal. Only to be used through TI provided API.
6	C1BEMODE	R/W	0h	Internal. Only to be used through TI provided API.
5	SOFTPDIFFMODE	R/W	0h	Internal. Only to be used through TI provided API.
4	SOFTTXENABLE	R/W	0h	Internal. Only to be used through TI provided API.
3	FECENABLE	R/W	0h	Internal. Only to be used through TI provided API.
2	FEC5TERMINATE	R/W	0h	Internal. Only to be used through TI provided API.
1	TONEINSERT	R/W	0h	Internal. Only to be used through TI provided API.
0	PREAMBLEINSERT	R/W	0h	Internal. Only to be used through TI provided API.

28.6.43 DEMFRAC1_DEMFRAC0 Register (Offset = A8h) [Reset = 00000000h]

DEMFRAC1_DEMFRAC0 is shown in Table 28-70.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-70. DEMFRAC1_DEMFRAC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	P27C16	R/W	0h	Internal. Only to be used through TI provided API.
15-0	P15C0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.44 DEMFRAC3_DEMFRAC2 Register (Offset = ACh) [Reset = 00000000h]

DEMFRAC3_DEMFRAC2 is shown in Table 28-71.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-71. DEMFRAC3_DEMFRAC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	Q27C16	R/W	0h	Internal. Only to be used through TI provided API.
15-0	Q15C0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.45 DEMCODC2_DEMCODC1 Register (Offset = B0h) [Reset = 00000000h]

DEMCODC2_DEMCODC1 is shown in Table 28-72.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-72. DEMCODC2_DEMCODC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-16	COMPQVAL	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12-0	COMPIVAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.46 DEMFIDC2_DEMFIDC1 Register (Offset = B4h) [Reset = 00000000h]

DEMFIDC2_DEMFIDC1 is shown in Table 28-73.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-73. DEMFIDC2_DEMFIDC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-16	COMPQVAL	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12-0	COMPIVAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.47 DEMMAFC0_DEMFIFE1 Register (Offset = B8h) [Reset = 00000000h]

DEMMAFC0_DEMFIFE1 is shown in Table 28-74.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-74. DEMMAFC0_DEMFIFE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	COMPVAL	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	FOCFBREGVAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.48 DEMSWIMBAL_DEMMAFI4 Register (Offset = BCh) [Reset = 00000000h]

DEMSWIMBAL_DEMMAFI4 is shown in Table 28-75.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-75. DEMSWIMBAL_DEMMAFI4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	IMBALB	R/W	0h	Internal. Only to be used through TI provided API.
23-16	IMBALA	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	TERMVAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.49 DEMDEBUG_DEMSOFTPDIFF Register (Offset = C0h) [Reset = 00000000h]

DEMDEBUG_DEMSOFTPDIFF is shown in Table 28-76.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-76. DEMDEBUG_DEMSOFTPDIFF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-25	LOOPBACKPIN	R/W	0h	Internal. Only to be used through TI provided API.
24	DECSTAGETRIGGER	R/W	0h	Internal. Only to be used through TI provided API.
23-21	DECSTAGEDEBUG	R/W	0h	Internal. Only to be used through TI provided API.
20	FRONTENDTRIGGER	R/W	0h	Internal. Only to be used through TI provided API.
19-17	FRONTENDDEBUG	R/W	0h	Internal. Only to be used through TI provided API.
16	LOOPBACKMODE	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.50 VITCOMPUTE_VITCTRL Register (Offset = C4h) [Reset = 00000000h]

VITCOMPUTE_VITCTRL is shown in Table 28-77.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-77. VITCOMPUTE_VITCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	START	W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-6	METRSEL	R/W	0h	Internal. Only to be used through TI provided API.
5-2	APMRDBACKSEL	R/W	0h	Internal. Only to be used through TI provided API.
1	ACSITERATIONS	R/W	0h	Internal. Only to be used through TI provided API.
0	METRICS	R/W	0h	Internal. Only to be used through TI provided API.

28.6.51 VITSTATE_VITAPMRDBACK Register (Offset = C8h) [Reset = 00000000h]

VITSTATE_VITAPMRDBACK is shown in Table 28-78.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-78. VITSTATE_VITAPMRDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	VITSTATE_VALUE	R	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	VITAPMRDBACK_VALUE	R	0h	Internal. Only to be used through TI provided API.

28.6.52 VITBRMETRIC32_VITBRMETRIC10 Register (Offset = CCh) [Reset = 00000000h]

VITBRMETRIC32_VITBRMETRIC10 is shown in Table 28-79.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-79. VITBRMETRIC32_VITBRMETRIC10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MET3	R/W	0h	Internal. Only to be used through TI provided API.
23-16	MET2	R/W	0h	Internal. Only to be used through TI provided API.
15-8	MET1	R/W	0h	Internal. Only to be used through TI provided API.
7-0	MET0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.53 VITBRMETRIC76_VITBRMETRIC54 Register (Offset = D0h) [Reset = 00000000h]

VITBRMETRIC76_VITBRMETRIC54 is shown in Table 28-80.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-80. VITBRMETRIC76_VITBRMETRIC54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MET7	R/W	0h	Internal. Only to be used through TI provided API.
23-16	MET6	R/W	0h	Internal. Only to be used through TI provided API.
15-8	MET5	R/W	0h	Internal. Only to be used through TI provided API.
7-0	MET4	R/W	0h	Internal. Only to be used through TI provided API.

28.6.54 DEMD2XB0_DEMDSXB0 Register (Offset = D4h) [Reset = 00000000h]

DEMD2XB0_DEMDSXB0 is shown in Table 28-81.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-81. DEMD2XB0_DEMDSXB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-26	DEMD2XB0_B3SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
25	DEMD2XB0_OUT2PASSTHROUGH	R/W	0h	Internal. Only to be used through TI provided API.
24	DEMD2XB0_OUT1PASSTHROUGH	R/W	0h	Internal. Only to be used through TI provided API.
23-22	DEMD2XB0_OUTSRCSEL2	R/W	0h	Internal. Only to be used through TI provided API.
21-20	DEMD2XB0_OUTSRCSEL1	R/W	0h	Internal. Only to be used through TI provided API.
19-18	DEMD2XB0_B2SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
17-16	DEMD2XB0_B1SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5	DEMDSXB0_OUT2PASSTHROUGH	R/W	0h	Internal. Only to be used through TI provided API.
4	DEMDSXB0_OUT1PASSTHROUGH	R/W	0h	Internal. Only to be used through TI provided API.
3	DEMDSXB0_OUTSRCSEL2	R/W	0h	Internal. Only to be used through TI provided API.
2	DEMDSXB0_OUTSRCSEL1	R/W	0h	Internal. Only to be used through TI provided API.
1	DEMDSXB0_B2SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.
0	DEMDSXB0_B1SRCSEL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.55 TIMCTL Register (Offset = F0h) [Reset = 00000000h]

TIMCTL is shown in Table 28-82.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-82. TIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	CPTSRC	R/W	0h	Internal. Only to be used through TI provided API.
23	CPTCTL	R/W	0h	Internal. Only to be used through TI provided API.
22-21	CNTRSRC	R/W	0h	Internal. Only to be used through TI provided API.
20	CNTRCLR	R/W	0h	Internal. Only to be used through TI provided API.
19	CNTRCTL	R/W	0h	Internal. Only to be used through TI provided API.
18-17	TIMSRC	R/W	0h	Internal. Only to be used through TI provided API.
16	TIMCTL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

28.6.56 TIMPER_TIMINC Register (Offset = F4h) [Reset = 00000000h]

TIMPER_TIMINC is shown in Table 28-83.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-83. TIMPER_TIMINC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TIMPER_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	TIMINC_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.57 TIMCAPT_TIMCNT Register (Offset = F8h) [Reset = 00000000h]

TIMCAPT_TIMCNT is shown in Table 28-84.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-84. TIMCAPT_TIMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VALUE	R	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.58 COUNT1IN_TIMEBASE Register (Offset = FCh) [Reset = 00000000h]

COUNT1IN_TIMEBASE is shown in Table 28-85.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-85. COUNT1IN_TIMEBASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	FLUSH	W	0h	Internal. Only to be used through TI provided API.

28.6.59 COUNT1RES Register (Offset = 100h) [Reset = 00000000h]

COUNT1RES is shown in Table 28-86.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-86. COUNT1RES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.60 BRMACC2_BRMACC1 Register (Offset = 104h) [Reset = 00000000h]

BRMACC2_BRMACC1 is shown in Table 28-87.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-87. BRMACC2_BRMACC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	METRIC11	R	0h	Internal. Only to be used through TI provided API.
23-16	METRIC10	R	0h	Internal. Only to be used through TI provided API.
15-8	METRIC01	R	0h	Internal. Only to be used through TI provided API.
7-0	METRIC00	R	0h	Internal. Only to be used through TI provided API.

28.6.61 MCETRCSTAT_MCETRCCTRL Register (Offset = 108h) [Reset = 00000000h]

MCETRCSTAT_MCETRCCTRL is shown in Table 28-88.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-88. MCETRCSTAT_MCETRCCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	BUSY	R	0h	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	SEND	W	0h	Internal. Only to be used through TI provided API.

28.6.62 MCETRCPAR0_MCETRCCMD Register (Offset = 10Ch) [Reset = 00000000h]

MCETRCPAR0_MCETRCCMD is shown in Table 28-89.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-89. MCETRCPAR0_MCETRCCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-8	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.

28.6.63 RDCAPT0_MCETRCPAR1 Register (Offset = 110h) [Reset = 00000000h]

RDCAPT0_MCETRCPAR1 is shown in Table 28-90.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-90. RDCAPT0_MCETRCPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	CHFI	W	0h	Internal. Only to be used through TI provided API.
20	BDE2	W	0h	Internal. Only to be used through TI provided API.
19	FIDC	W	0h	Internal. Only to be used through TI provided API.
18	FRAC	W	0h	Internal. Only to be used through TI provided API.
17	MGEX	W	0h	Internal. Only to be used through TI provided API.
16	CODC	W	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.64 FECAPT0_RDCAPT1 Register (Offset = 114h) [Reset = 00000000h]

FECAPT0_RDCAPT1 is shown in Table 28-91.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-91. FECAPT0_RDCAPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-14	RESERVED	R	0h	Reserved
13	COHRX	W	0h	Internal. Only to be used through TI provided API.
12	C1BEX3	W	0h	Internal. Only to be used through TI provided API.
11	C1BEX2	W	0h	Internal. Only to be used through TI provided API.
10	C1BEX1	W	0h	Internal. Only to be used through TI provided API.
9	C1BEX0	W	0h	Internal. Only to be used through TI provided API.
8	SOFD	W	0h	Internal. Only to be used through TI provided API.
7	LQIE	W	0h	Internal. Only to be used through TI provided API.
6	STIM	W	0h	Internal. Only to be used through TI provided API.
6	RESERVED	R	0h	Reserved
5	FIFE	W	0h	Internal. Only to be used through TI provided API.
4	PDIF	W	0h	Internal. Only to be used through TI provided API.
3	CA2P	W	0h	Internal. Only to be used through TI provided API.
2	MAFI	W	0h	Internal. Only to be used through TI provided API.
1	DSBU	W	0h	Internal. Only to be used through TI provided API.
0	MLSEBIT	W	0h	Internal. Only to be used through TI provided API.

28.6.65 DSCAPT0_FECAPT1 Register (Offset = 118h) [Reset = 00000000h]

DSCAPT0_FECAPT1 is shown in Table 28-92.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-92. DSCAPT0_FECAPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	DSCAPT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12-0	FECAPT1_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.66 DSCAPT2_DSCAPT1 Register (Offset = 11Ch) [Reset = 00000000h]

DSCAPT2_DSCAPT1 is shown in Table 28-93.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-93. DSCAPT2_DSCAPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	DSCAPT2_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	DSCAPT1_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.67 DEMSWQU1_DSCAPT3 Register (Offset = 120h) [Reset = 00000000h]

DEMSWQU1_DSCAPT3 is shown in Table 28-94.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-94. DEMSWQU1_DSCAPT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-18	MAFCCOMPVAL	R	0h	Internal. Only to be used through TI provided API.
17	SWSEL	R	0h	Internal. Only to be used through TI provided API.
16	SYNCED	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.68 GPOCTRL1_GPOCTRL0 Register (Offset = 124h) [Reset = 00000000h]

GPOCTRL1_GPOCTRL0 is shown in Table 28-95.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-95. GPOCTRL1_GPOCTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	HWCLKSTRETCH	R/W	0h	Internal. Only to be used through TI provided API.
29-27	HWCLKMUX1	R/W	0h	Internal. Only to be used through TI provided API.
26-24	HWCLKMUX0	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SW	R/W	0h	Internal. Only to be used through TI provided API.
15-14	GPO7	R/W	0h	Internal. Only to be used through TI provided API.
13-12	GPO6	R/W	0h	Internal. Only to be used through TI provided API.
11-10	GPO5	R/W	0h	Internal. Only to be used through TI provided API.
9-8	GPO4	R/W	0h	Internal. Only to be used through TI provided API.
7-6	GPO3	R/W	0h	Internal. Only to be used through TI provided API.
5-4	GPO2	R/W	0h	Internal. Only to be used through TI provided API.
3-2	GPO1	R/W	0h	Internal. Only to be used through TI provided API.
1-0	GPO0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.69 RFEMAXRSSI_RFERSSI Register (Offset = 128h) [Reset = 00000000h]

RFEMAXRSSI_RFERSSI is shown in Table 28-96.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-96. RFEMAXRSSI_RFERSSI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	RFEMAXRSSI_VAL	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	RFERSSI_VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.70 SYNC0_RFEDBGAIN Register (Offset = 12Ch) [Reset = 00000000h]

SYNC0_RFEDBGAIN is shown in Table 28-97.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-97. SYNC0_RFEDBGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SWA15C0	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.71 SYNC2_SYNC1 Register (Offset = 130h) [Reset = 00000000h]

SYNC2_SYNC1 is shown in Table 28-98.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-98. SYNC2_SYNC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SWB15C0	R	0h	Internal. Only to be used through TI provided API.
15-0	SWA31C16	R	0h	Internal. Only to be used through TI provided API.

28.6.72 SYNC3 Register (Offset = 134h) [Reset = 00000000h]

SYNC3 is shown in Table 28-99.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-99. SYNC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	SWB31C16	R	0h	Internal. Only to be used through TI provided API.

28.6.73 DEMHDIS0 Register (Offset = 138h) [Reset = 00000000h]

DEMHDIS0 is shown in Table 28-100.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-100. DEMHDIS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

28.6.74 DEMCOHR1_DEMCOHR0 Register (Offset = 13Ch) [Reset = 00000000h]

DEMCOHR1_DEMCOHR0 is shown in Table 28-101.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-101. DEMCOHR1_DEMCOHR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BETA	R/W	0h	Internal. Only to be used through TI provided API.
23-16	ALPHA	R/W	0h	Internal. Only to be used through TI provided API.
15-14	RESERVED	R	0h	Reserved
13-5	NCOLIMIT	R/W	0h	Internal. Only to be used through TI provided API.
4-2	IIRBW	R/W	0h	Internal. Only to be used through TI provided API.
1-0	IIRGAIN	R/W	0h	Internal. Only to be used through TI provided API.

28.6.75 DEMCOHR3_DEMCOHR2 Register (Offset = 140h) [Reset = 00000000h]

DEMCOHR3_DEMCOHR2 is shown in Table 28-102.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-102. DEMCOHR3_DEMCOHR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	REF150	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-5	REFROT	R/W	0h	Internal. Only to be used through TI provided API.
4-0	REFLEN	R/W	0h	Internal. Only to be used through TI provided API.

28.6.76 DEMCOHR5_DEMCOHR4 Register (Offset = 144h) [Reset = 00000000h]

DEMCOHR5_DEMCOHR4 is shown in Table 28-103.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-103. DEMCOHR5_DEMCOHR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	REF3116	R/W	0h	Internal. Only to be used through TI provided API.

28.6.77 DEMCOHR7_DEMCOHR6 Register (Offset = 148h) [Reset = 00000000h]

DEMCOHR7_DEMCOHR6 is shown in Table 28-104.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-104. DEMCOHR7_DEMCOHR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	DEMCOHR7_VAL	R	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5-0	DEMCOHR6_VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.78 DEMCOHR9_DEMCOHR8 Register (Offset = 14Ch) [Reset = 00000000h]

DEMCOHR9_DEMCOHR8 is shown in Table 28-105.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-105. DEMCOHR9_DEMCOHR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-16	DEMCOHR9_VAL	R	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5-0	DEMCOHR8_VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.79 BAUDCOMP Register (Offset = 150h) [Reset = 00000000h]

BAUDCOMP is shown in Table 28-106.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-106. BAUDCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	SCALEVAL	R/W	0h	Internal. Only to be used through TI provided API.

28.6.80 DEMFB2P0_DEMCMIX2 Register (Offset = 158h) [Reset = 00000000h]

DEMFB2P0_DEMCMIX2 is shown in Table 28-107.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-107. DEMFB2P0_DEMCMIX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BETA	R/W	0h	Internal. Only to be used through TI provided API.
23-16	ALPHA	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12-0	N	R/W	0h	Internal. Only to be used through TI provided API.

28.6.81 DEMFB2P2_DEMFB2P1 Register (Offset = 15Ch) [Reset = 00000000h]

DEMFB2P2_DEMFB2P1 is shown in Table 28-108.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-108. DEMFB2P2_DEMFB2P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-16	RBP	R	0h	Internal. Only to be used through TI provided API.
15	FB2POPEN	R/W	0h	Internal. Only to be used through TI provided API.
14-13	HDISPRS	R/W	0h	Internal. Only to be used through TI provided API.
12-11	IIRGAIN	R/W	0h	Internal. Only to be used through TI provided API.
10-8	IIRBW	R/W	0h	Internal. Only to be used through TI provided API.
7-0	FB2PLLLIMIT	R/W	0h	Internal. Only to be used through TI provided API.

28.6.82 DEMDSBU0 Register (Offset = 160h) [Reset = 00000000h]

DEMDSBU0 is shown in Table 28-109.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-109. DEMDSBU0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24-16	RDPOUT	R	1FFh	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

28.6.83 DEMDSBU3_DEMDSBU1 Register (Offset = 164h) [Reset = 00000000h]

DEMDSBU3_DEMDSBU1 is shown in Table 28-110.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-110. DEMDSBU3_DEMDSBU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24-16	WRPOUT	R	0h	Internal. Only to be used through TI provided API.
15-0	AVGVAL	R	0h	Internal. Only to be used through TI provided API.

28.6.84 DEMPHAC1_DEMPHAC0 Register (Offset = 168h) [Reset = 00000000h]

DEMPHAC1_DEMPHAC0 is shown in Table 28-111.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-111. DEMPHAC1_DEMPHAC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	PHACTRLEN	R/W	0h	Internal. Only to be used through TI provided API.
25-23	PHACSYMLEN	R/W	0h	Internal. Only to be used through TI provided API.
22-16	PHASEINCR	R/W	0h	Internal. Only to be used through TI provided API.
15-8	REFB	R/W	0h	Internal. Only to be used through TI provided API.
7-0	REFA	R/W	0h	Internal. Only to be used through TI provided API.

28.6.85 DEMPHAC3_DEMPHAC2 Register (Offset = 16Ch) [Reset = 00000000h]

DEMPHAC3_DEMPHAC2 is shown in Table 28-112.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-112. DEMPHAC3_DEMPHAC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	IIRBW	R/W	0h	Internal. Only to be used through TI provided API.
15-8	ALPHA	R/W	0h	Internal. Only to be used through TI provided API.
7-0	BETA	R/W	0h	Internal. Only to be used through TI provided API.

28.6.86 DEMPHAC5_DEMPHAC4 Register (Offset = 170h) [Reset = 00000000h]

DEMPHAC5_DEMPHAC4 is shown in Table 28-113.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-113. DEMPHAC5_DEMPHAC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TR3116	R/W	0h	Internal. Only to be used through TI provided API.
15-0	TR150	R/W	0h	Internal. Only to be used through TI provided API.

28.6.87 DEMPHAC7_DEMPHAC6 Register (Offset = 174h) [Reset = 00000000h]

DEMPHAC7_DEMPHAC6 is shown in Table 28-114.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-114. DEMPHAC7_DEMPHAC6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TR6348	R/W	0h	Internal. Only to be used through TI provided API.
15-0	TR4732	R/W	0h	Internal. Only to be used through TI provided API.

28.6.88 DEMPHAC9_DEMPHAC8 Register (Offset = 178h) [Reset = 00000000h]

DEMPHAC9_DEMPHAC8 is shown in Table 28-115.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-115. DEMPHAC9_DEMPHAC8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	METRIC11	R	0h	Internal. Only to be used through TI provided API.
23-16	METRIC10	R	0h	Internal. Only to be used through TI provided API.
15-8	METRIC01	R	0h	Internal. Only to be used through TI provided API.
7-0	METRIC00	R	0h	Internal. Only to be used through TI provided API.

28.6.89 DEMC1BEREF5_DEMC1BEREF4 Register (Offset = 17Ch) [Reset = 00000000h]

DEMC1BEREF5_DEMC1BEREF4 is shown in Table 28-116.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-116. DEMC1BEREF5_DEMC1BEREF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CDR31C16	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CDR15C0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.90 DEMC1BEREF7_DEMC1BEREF6 Register (Offset = 180h) [Reset = 00000000h]

DEMC1BEREF7_DEMC1BEREF6 is shown in Table 28-117.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-117. DEMC1BEREF7_DEMC1BEREF6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CER31C16	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CER15C0	R/W	0h	Internal. Only to be used through TI provided API.

28.6.91 DEMC1BE4_DEMC1BE3 Register (Offset = 184h) [Reset = 00000000h]

DEMC1BE4_DEMC1BE3 is shown in Table 28-118.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-118. DEMC1BE4_DEMC1BE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CORRVALUEB	R	0h	Internal. Only to be used through TI provided API.
15-0	CORRVALUEA	R	0h	Internal. Only to be used through TI provided API.

28.6.92 DEMC1BE6_DEMC1BE5 Register (Offset = 188h) [Reset = 00000000h]

DEMC1BE6_DEMC1BE5 is shown in Table 28-119.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-119. DEMC1BE6_DEMC1BE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	CORRVALUEC	R	0h	Internal. Only to be used through TI provided API.

28.6.93 DEMC1BE8_DEMC1BE7 Register (Offset = 18Ch) [Reset = 00000000h]

DEMC1BE8_DEMC1BE7 is shown in Table 28-120.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-120. DEMC1BE8_DEMC1BE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	DEMC1BE8_VAL	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	DEMC1BE7_VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.94 DEMC1BE10_DEMC1BE9 Register (Offset = 190h) [Reset = 00000000h]

DEMC1BE10_DEMC1BE9 is shown in Table 28-121.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-121. DEMC1BE10_DEMC1BE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PEAKCONFG	R/W	0h	Internal. Only to be used through TI provided API.
30-29	PEAKCONFCF	R/W	0h	Internal. Only to be used through TI provided API.
28-24	MASKE	R/W	0h	Internal. Only to be used through TI provided API.
23-19	MASKD	R/W	0h	Internal. Only to be used through TI provided API.
18-16	CASCCONF	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.6.95 DEMC1BE12_DEMC1BE11 Register (Offset = 194h) [Reset = 00000000h]

DEMC1BE12_DEMC1BE11 is shown in Table 28-122.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-122. DEMC1BE12_DEMC1BE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	THRESHOLDG	R/W	0h	Internal. Only to be used through TI provided API.
23-16	THRESHOLDF	R/W	0h	Internal. Only to be used through TI provided API.
15-8	THRESHOLDE	R/W	0h	Internal. Only to be used through TI provided API.
7-0	THRESHOLDD	R/W	0h	Internal. Only to be used through TI provided API.

28.6.96 DEMC1BE14_DEMC1BE13 Register (Offset = 198h) [Reset = 00000000h]

DEMC1BE14_DEMC1BE13 is shown in Table 28-123.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-123. DEMC1BE14_DEMC1BE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CORRVALUEE	R	0h	Internal. Only to be used through TI provided API.
15-0	CORRVALUED	R	0h	Internal. Only to be used through TI provided API.

28.6.97 DEMC1BE15 Register (Offset = 19Ch) [Reset = 00000000h]

DEMC1BE15 is shown in Table 28-124.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-124. DEMC1BE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CORRVALUEF	R	0h	Internal. Only to be used through TI provided API.

28.6.98 DEMC1BE20 Register (Offset = 1A4h) [Reset = 00000000h]

DEMC1BE20 is shown in Table 28-125.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-125. DEMC1BE20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CORRVALUEG	R	0h	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

28.6.99 STRB2 Register (Offset = 1A8h) [Reset = 00000000h]

STRB2 is shown in Table 28-126.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-126. STRB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	C1BECOPY2	W	0h	Internal. Only to be used through TI provided API.
20	C1BEPEAKG	W	0h	Internal. Only to be used through TI provided API.
19	C1BEPEAKDE	W	0h	Internal. Only to be used through TI provided API.
18	C1BEPEAKF	W	0h	Internal. Only to be used through TI provided API.
17	C1BEPEAKE	W	0h	Internal. Only to be used through TI provided API.
16	C1BEPEAKD	W	0h	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

28.6.100 EVTMSK3_EVT3 Register (Offset = 1ACh) [Reset = 00000000h]

EVTMSK3_EVT3 is shown in Table 28-127.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-127. EVTMSK3_EVT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EVTMSK3_C1BEDLOADED	R/W	0h	Internal. Only to be used through TI provided API.
30	EVTMSK3_C1BEGANY	R/W	0h	Internal. Only to be used through TI provided API.
29	EVTMSK3_C1BEGNEG	R/W	0h	Internal. Only to be used through TI provided API.
28	EVTMSK3_C1BEGPOS	R/W	0h	Internal. Only to be used through TI provided API.
27	EVTMSK3_C1BECMBDEANY	R/W	0h	Internal. Only to be used through TI provided API.
26	EVTMSK3_C1BECMBDENEG	R/W	0h	Internal. Only to be used through TI provided API.
25	EVTMSK3_C1BECMBDEPOS	R/W	0h	Internal. Only to be used through TI provided API.
24	EVTMSK3_C1BEFANY	R/W	0h	Internal. Only to be used through TI provided API.
23	EVTMSK3_C1BEFNEG	R/W	0h	Internal. Only to be used through TI provided API.
22	EVTMSK3_C1BEFPOS	R/W	0h	Internal. Only to be used through TI provided API.
21	EVTMSK3_C1BEEANY	R/W	0h	Internal. Only to be used through TI provided API.
20	EVTMSK3_C1BEENEG	R/W	0h	Internal. Only to be used through TI provided API.
19	EVTMSK3_C1BEEPOS	R/W	0h	Internal. Only to be used through TI provided API.
18	EVTMSK3_C1BEDANY	R/W	0h	Internal. Only to be used through TI provided API.
17	EVTMSK3_C1BEDNEG	R/W	0h	Internal. Only to be used through TI provided API.
16	EVTMSK3_C1BEDPOS	R/W	0h	Internal. Only to be used through TI provided API.
15	EVT3_C1BEDLOADED	R	0h	Internal. Only to be used through TI provided API.
14	EVT3_C1BEGANY	R	0h	Internal. Only to be used through TI provided API.
13	EVT3_C1BEGNEG	R	0h	Internal. Only to be used through TI provided API.
12	EVT3_C1BEGPOS	R	0h	Internal. Only to be used through TI provided API.
11	EVT3_C1BECMBDEANY	R	0h	Internal. Only to be used through TI provided API.
10	EVT3_C1BECMBDENEG	R	0h	Internal. Only to be used through TI provided API.
9	EVT3_C1BECMBDEPOS	R	0h	Internal. Only to be used through TI provided API.
8	EVT3_C1BEFANY	R	0h	Internal. Only to be used through TI provided API.
7	EVT3_C1BEFNEG	R	0h	Internal. Only to be used through TI provided API.
6	EVT3_C1BEFPOS	R	0h	Internal. Only to be used through TI provided API.
5	EVT3_C1BEEANY	R	0h	Internal. Only to be used through TI provided API.
4	EVT3_C1BEENEG	R	0h	Internal. Only to be used through TI provided API.
3	EVT3_C1BEEPOS	R	0h	Internal. Only to be used through TI provided API.
2	EVT3_C1BEDANY	R	0h	Internal. Only to be used through TI provided API.
1	EVT3_C1BEDNEG	R	0h	Internal. Only to be used through TI provided API.
0	EVT3_C1BEDPOS	R	0h	Internal. Only to be used through TI provided API.

28.6.101 EVTCLR3 Register (Offset = 1B0h) [Reset = 00000000h]

EVTCLR3 is shown in Table 28-128.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-128. EVTCLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	C1BEDLOADED	W	0h	Internal. Only to be used through TI provided API.
14	C1BEGANY	W	0h	Internal. Only to be used through TI provided API.
13	C1BEGNEG	W	0h	Internal. Only to be used through TI provided API.
12	C1BEGPOS	W	0h	Internal. Only to be used through TI provided API.
11	C1BECMBDEANY	W	0h	Internal. Only to be used through TI provided API.
10	C1BECMBDENEG	W	0h	Internal. Only to be used through TI provided API.
9	C1BECMBDEPOS	W	0h	Internal. Only to be used through TI provided API.
8	C1BEFANY	W	0h	Internal. Only to be used through TI provided API.
7	C1BEFNEG	W	0h	Internal. Only to be used through TI provided API.
6	C1BEFPOS	W	0h	Internal. Only to be used through TI provided API.
5	C1BEEANY	W	0h	Internal. Only to be used through TI provided API.
4	C1BEENEG	W	0h	Internal. Only to be used through TI provided API.
3	C1BEEPOS	W	0h	Internal. Only to be used through TI provided API.
2	C1BEDANY	W	0h	Internal. Only to be used through TI provided API.
1	C1BEDNEG	W	0h	Internal. Only to be used through TI provided API.
0	C1BEDPOS	W	0h	Internal. Only to be used through TI provided API.

28.7 LRFDPBE Registers

Table 28-129 lists the memory-mapped registers for the LRFDPBE registers. All register offset addresses not listed in Table 28-129 should be considered as reserved locations and the register contents should not be modified.

Table 28-129. LRFDPBE Registers

Offset	Acronym	Register Name	Section
0h	ENABLE	Internal. Only to be used through TI provided API.	Section 28.7.1
4h	FWSRC	Internal. Only to be used through TI provided API.	Section 28.7.2
8h	INIT	Internal. Only to be used through TI provided API.	Section 28.7.3
Ch	STROBES0	Internal. Only to be used through TI provided API.	Section 28.7.4
10h	IRQ	Internal. Only to be used through TI provided API.	Section 28.7.5
14h	EVT0	Internal. Only to be used through TI provided API.	Section 28.7.6
18h	EVT1	Internal. Only to be used through TI provided API.	Section 28.7.7
1Ch	EVTMSK0	Internal. Only to be used through TI provided API.	Section 28.7.8
20h	EVTMSK1	Internal. Only to be used through TI provided API.	Section 28.7.9
24h	EVTCLR0	Internal. Only to be used through TI provided API.	Section 28.7.10
28h	EVTCLR1	Internal. Only to be used through TI provided API.	Section 28.7.11
2Ch	PDREQ	Internal. Only to be used through TI provided API.	Section 28.7.12
30h	API	Internal. Only to be used through TI provided API.	Section 28.7.13
34h	MCEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.7.14
38h	MCEDATIN0	Internal. Only to be used through TI provided API.	Section 28.7.15
3Ch	MCECMDOUT	Internal. Only to be used through TI provided API.	Section 28.7.16
40h	MCECMDIN	Internal. Only to be used through TI provided API.	Section 28.7.17
44h	MDMAPI	Internal. Only to be used through TI provided API.	Section 28.7.18
48h	MDMMSGBOX	Internal. Only to be used through TI provided API.	Section 28.7.19
4Ch	FREQ	Internal. Only to be used through TI provided API.	Section 28.7.20
50h	MDMLQI	Internal. Only to be used through TI provided API.	Section 28.7.21
54h	RFEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.7.22
58h	RFEDATIN0	Internal. Only to be used through TI provided API.	Section 28.7.23
5Ch	RFECMDOUT	Internal. Only to be used through TI provided API.	Section 28.7.24
60h	RFECMDIN	Internal. Only to be used through TI provided API.	Section 28.7.25
64h	RFEAPI	Internal. Only to be used through TI provided API.	Section 28.7.26
68h	RFECMDPAR0	Internal. Only to be used through TI provided API.	Section 28.7.27
6Ch	RFECMDPAR1	Internal. Only to be used through TI provided API.	Section 28.7.28
70h	RFEMSGBOX	Internal. Only to be used through TI provided API.	Section 28.7.29
74h	RFERSSI	Internal. Only to be used through TI provided API.	Section 28.7.30
78h	RFERSSIMAX	Internal. Only to be used through TI provided API.	Section 28.7.31
7Ch	RFERFGAIN	Internal. Only to be used through TI provided API.	Section 28.7.32
80h	MDMSYNCAL	Internal. Only to be used through TI provided API.	Section 28.7.33
84h	MDMSYNCAH	Internal. Only to be used through TI provided API.	Section 28.7.34
88h	MDMSYNCBL	Internal. Only to be used through TI provided API.	Section 28.7.35
8Ch	MDMSYNCBH	Internal. Only to be used through TI provided API.	Section 28.7.36
90h	MDMCMDPAR0	Internal. Only to be used through TI provided API.	Section 28.7.37
94h	MDMCMDPAR1	Internal. Only to be used through TI provided API.	Section 28.7.38
98h	MDMCMDPAR2	Internal. Only to be used through TI provided API.	Section 28.7.39
9Ch	RFEDATIN1	Internal. Only to be used through TI provided API.	Section 28.7.40

Table 28-129. LRFDPBE Registers (continued)

Offset	Acronym	Register Name	Section
A0h	POLY0L	Internal. Only to be used through TI provided API.	Section 28.7.41
A4h	POLY0H	Internal. Only to be used through TI provided API.	Section 28.7.42
A8h	POLY1L	Internal. Only to be used through TI provided API.	Section 28.7.43
ACh	POLY1H	Internal. Only to be used through TI provided API.	Section 28.7.44
B0h	PHACFG	Internal. Only to be used through TI provided API.	Section 28.7.45
B4h	FCFG0	Internal. Only to be used through TI provided API.	Section 28.7.46
B8h	FCFG1	Internal. Only to be used through TI provided API.	Section 28.7.47
BCh	FCFG2	Internal. Only to be used through TI provided API.	Section 28.7.48
C0h	FCFG3	Internal. Only to be used through TI provided API.	Section 28.7.49
C4h	FCFG4	Internal. Only to be used through TI provided API.	Section 28.7.50
C8h	FCFG5	Internal. Only to be used through TI provided API.	Section 28.7.51
CCh	RXFWBTHRS	Internal. Only to be used through TI provided API.	Section 28.7.52
D0h	RXFRBTHRS	Internal. Only to be used through TI provided API.	Section 28.7.53
D4h	TXFWBTHRS	Internal. Only to be used through TI provided API.	Section 28.7.54
D8h	TXFRBTHRS	Internal. Only to be used through TI provided API.	Section 28.7.55
DCh	TIMCTL	Internal. Only to be used through TI provided API.	Section 28.7.56
E0h	TIMPRE	Internal. Only to be used through TI provided API.	Section 28.7.57
E4h	TIMPER0	Internal. Only to be used through TI provided API.	Section 28.7.58
E8h	TIMPER1	Internal. Only to be used through TI provided API.	Section 28.7.59
ECh	TIMCAPT0	Internal. Only to be used through TI provided API.	Section 28.7.60
F0h	TIMCAPT1	Internal. Only to be used through TI provided API.	Section 28.7.61
F4h	TRCCTL	Internal. Only to be used through TI provided API.	Section 28.7.62
F8h	TRCSTAT	Internal. Only to be used through TI provided API.	Section 28.7.63
FCh	TRCCMD	Internal. Only to be used through TI provided API.	Section 28.7.64
100h	TRCPAR0	Internal. Only to be used through TI provided API.	Section 28.7.65
104h	TRCPAR1	Internal. Only to be used through TI provided API.	Section 28.7.66
108h	GPOCTRL	Internal. Only to be used through TI provided API.	Section 28.7.67
10Ch	MDMFWR	Internal. Only to be used through TI provided API.	Section 28.7.68
110h	MDMFRD	Internal. Only to be used through TI provided API.	Section 28.7.69
114h	MDMFWRCTL	Internal. Only to be used through TI provided API.	Section 28.7.70
118h	MDMFRDCTL	Internal. Only to be used through TI provided API.	Section 28.7.71
11Ch	MDMFCFG	Internal. Only to be used through TI provided API.	Section 28.7.72
120h	MDMFSTA	Internal. Only to be used through TI provided API.	Section 28.7.73
124h	PHASTA	Internal. Only to be used through TI provided API.	Section 28.7.74
128h	LFSR0L	Internal. Only to be used through TI provided API.	Section 28.7.75
12Ch	LFSR0H	Internal. Only to be used through TI provided API.	Section 28.7.76
130h	LFSR0BRL	Internal. Only to be used through TI provided API.	Section 28.7.77
134h	LFSR0BRH	Internal. Only to be used through TI provided API.	Section 28.7.78
138h	LFSR1L	Internal. Only to be used through TI provided API.	Section 28.7.79
13Ch	LFSR1H	Internal. Only to be used through TI provided API.	Section 28.7.80
140h	LFSR1BRL	Internal. Only to be used through TI provided API.	Section 28.7.81
144h	LFSR1BRH	Internal. Only to be used through TI provided API.	Section 28.7.82
148h	LFSR0INL	Internal. Only to be used through TI provided API.	Section 28.7.83
14Ch	LFSR0N	Internal. Only to be used through TI provided API.	Section 28.7.84
150h	LFSR0INM	Internal. Only to be used through TI provided API.	Section 28.7.85

Table 28-129. LRFDPBE Registers (continued)

Offset	Acronym	Register Name	Section
154h	PHAOUT0	Internal. Only to be used through TI provided API.	Section 28.7.86
158h	LFSR1INL	Internal. Only to be used through TI provided API.	Section 28.7.87
15Ch	LFSR1N	Internal. Only to be used through TI provided API.	Section 28.7.88
160h	LFSR1INM	Internal. Only to be used through TI provided API.	Section 28.7.89
164h	PHAOUT0BR	Internal. Only to be used through TI provided API.	Section 28.7.90
168h	DIVIDENDL	Internal. Only to be used through TI provided API.	Section 28.7.91
16Ch	DIVIDENDH	Internal. Only to be used through TI provided API.	Section 28.7.92
170h	DIVISORL	Internal. Only to be used through TI provided API.	Section 28.7.93
174h	DIVISORH	Internal. Only to be used through TI provided API.	Section 28.7.94
178h	QUOTIENTL	Internal. Only to be used through TI provided API.	Section 28.7.95
17Ch	QUOTIENTH	Internal. Only to be used through TI provided API.	Section 28.7.96
180h	SYSTIM0L	Internal. Only to be used through TI provided API.	Section 28.7.97
184h	SYSTIM0H	Internal. Only to be used through TI provided API.	Section 28.7.98
188h	SYSTIM1L	Internal. Only to be used through TI provided API.	Section 28.7.99
18Ch	SYSTIM1H	Internal. Only to be used through TI provided API.	Section 28.7.100
190h	SYSTIM2L	Internal. Only to be used through TI provided API.	Section 28.7.101
194h	SYSTIM2H	Internal. Only to be used through TI provided API.	Section 28.7.102
198h	GPI	Internal. Only to be used through TI provided API.	Section 28.7.103
19Ch	DIVSTA	Internal. Only to be used through TI provided API.	Section 28.7.104
1A0h	FCMD	Internal. Only to be used through TI provided API.	Section 28.7.105
1A4h	FSTAT	Internal. Only to be used through TI provided API.	Section 28.7.106
1A8h	RXFWP	Internal. Only to be used through TI provided API.	Section 28.7.107
1ACh	RXFRP	Internal. Only to be used through TI provided API.	Section 28.7.108
1B0h	RXFSWP	Internal. Only to be used through TI provided API.	Section 28.7.109
1B4h	RXFSRP	Internal. Only to be used through TI provided API.	Section 28.7.110
1B8h	TXFWP	Internal. Only to be used through TI provided API.	Section 28.7.111
1BCh	TXFRP	Internal. Only to be used through TI provided API.	Section 28.7.112
1C0h	TXFSWP	Internal. Only to be used through TI provided API.	Section 28.7.113
1C4h	TXFSRP	Internal. Only to be used through TI provided API.	Section 28.7.114
1C8h	RXFWRITABLE	Internal. Only to be used through TI provided API.	Section 28.7.115
1CCh	RXFREADABLE	Internal. Only to be used through TI provided API.	Section 28.7.116
1D0h	TXFWRITABLE	Internal. Only to be used through TI provided API.	Section 28.7.117
1D4h	TXFREADABLE	Internal. Only to be used through TI provided API.	Section 28.7.118
1D8h	RXFBRD	Internal. Only to be used through TI provided API.	Section 28.7.119
1DCh	RXFBWR	Internal. Only to be used through TI provided API.	Section 28.7.120
1E0h	TXFBRD	Internal. Only to be used through TI provided API.	Section 28.7.121
1E4h	TXFBWR	Internal. Only to be used through TI provided API.	Section 28.7.122
1E8h	RXFHRD	Internal. Only to be used through TI provided API.	Section 28.7.123
1ECh	RXFHWR	Internal. Only to be used through TI provided API.	Section 28.7.124
1F0h	TXFHRD	Internal. Only to be used through TI provided API.	Section 28.7.125
1F4h	TXFHWR	Internal. Only to be used through TI provided API.	Section 28.7.126
1F8h	MCEDATIN1	Internal. Only to be used through TI provided API.	Section 28.7.127

Complex bit access types are encoded to fit into small table cells. Table 28-130 shows the codes that are used for access types in this section.

Table 28-130. LRFDPBE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.7.1 ENABLE Register (Offset = 0h) [Reset = 00000000h]

ENABLE is shown in Table 28-131.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-131. ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	MDMF	R/W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	R/W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	R/W	0h	Internal. Only to be used through TI provided API.

28.7.2 FWSRC Register (Offset = 4h) [Reset = 00000000h]

FWSRC is shown in Table 28-132.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-132. FWSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	DATARAM	R/W	0h	Internal. Only to be used through TI provided API.
1	FWRAM	R/W	0h	Internal. Only to be used through TI provided API.
0	BANK	R/W	0h	Internal. Only to be used through TI provided API.

28.7.3 INIT Register (Offset = 8h) [Reset = 00000000h]

INIT is shown in Table 28-133.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-133. INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RFE	W	0h	Internal. Only to be used through TI provided API.
3	MDM	W	0h	Internal. Only to be used through TI provided API.
2	MDMF	W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	W	0h	Internal. Only to be used through TI provided API.

28.7.4 STROBES0 Register (Offset = Ch) [Reset = 00000000h]

STROBES0 is shown in Table 28-134.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-134. STROBES0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	TIMCAPT1	W	0h	Internal. Only to be used through TI provided API.
5	TIMCAPT0	W	0h	Internal. Only to be used through TI provided API.
4	S2RTRIG	W	0h	Internal. Only to be used through TI provided API.
3	DMATRIG	W	0h	Internal. Only to be used through TI provided API.
2	SYSTCAPT2	W	0h	Internal. Only to be used through TI provided API.
1	SYSTCAPT1	W	0h	Internal. Only to be used through TI provided API.
0	SYSTCAPT0	W	0h	Internal. Only to be used through TI provided API.

28.7.5 IRQ Register (Offset = 10h) [Reset = 00000000h]

IRQ is shown in Table 28-135.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-135. IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SOFT15	W	0h	Internal. Only to be used through TI provided API.
14	SOFT14	W	0h	Internal. Only to be used through TI provided API.
13	SOFT13	W	0h	Internal. Only to be used through TI provided API.
12	SOFT12	W	0h	Internal. Only to be used through TI provided API.
11	SOFT11	W	0h	Internal. Only to be used through TI provided API.
10	SOFT10	W	0h	Internal. Only to be used through TI provided API.
9	SOFT9	W	0h	Internal. Only to be used through TI provided API.
8	SOFT8	W	0h	Internal. Only to be used through TI provided API.
7	SOFT7	W	0h	Internal. Only to be used through TI provided API.
6	SOFT6	W	0h	Internal. Only to be used through TI provided API.
5	SOFT5	W	0h	Internal. Only to be used through TI provided API.
4	SOFT4	W	0h	Internal. Only to be used through TI provided API.
3	SOFT3	W	0h	Internal. Only to be used through TI provided API.
2	SOFT2	W	0h	Internal. Only to be used through TI provided API.
1	SOFT1	W	0h	Internal. Only to be used through TI provided API.
0	SOFT0	W	0h	Internal. Only to be used through TI provided API.

28.7.6 EVT0 Register (Offset = 14h) [Reset = 00000000h]

EVT0 is shown in Table 28-136.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-136. EVT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	MDMFAEMPTY	R	0h	Internal. Only to be used through TI provided API.
14	S2RSTOP	R	0h	Internal. Only to be used through TI provided API.
13	FIFOERR	R	0h	Internal. Only to be used through TI provided API.
12	MDMFAFULL	R	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP2	R	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP1	R	0h	Internal. Only to be used through TI provided API.
9	SYSTCMP0	R	0h	Internal. Only to be used through TI provided API.
8	MDMMSGBOX	R	0h	Internal. Only to be used through TI provided API.
7	RFEMSGBOX	R	0h	Internal. Only to be used through TI provided API.
6	RFEDAT	R	0h	Internal. Only to be used through TI provided API.
5	RFECMD	R	0h	Internal. Only to be used through TI provided API.
4	MDMDAT	R	0h	Internal. Only to be used through TI provided API.
3	MDMCMD	R	0h	Internal. Only to be used through TI provided API.
2	TIMER1	R	0h	Internal. Only to be used through TI provided API.
1	TIMER0	R	0h	Internal. Only to be used through TI provided API.
0	PBEAPI	R	0h	Internal. Only to be used through TI provided API.

28.7.7 EVT1 Register (Offset = 18h) [Reset = 00000000h]

EVT1 is shown in Table 28-137.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-137. EVT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	TXRDBTHR	R	0h	Internal. Only to be used through TI provided API.
11	TXWRBTHR	R	0h	Internal. Only to be used through TI provided API.
10	RXRDBTHR	R	0h	Internal. Only to be used through TI provided API.
9	RXWRBTHR	R	0h	Internal. Only to be used through TI provided API.
8	MDMPROG	R	0h	Internal. Only to be used through TI provided API.
7	PBEGPI7	R	0h	Internal. Only to be used through TI provided API.
6	PBEGPI6	R	0h	Internal. Only to be used through TI provided API.
5	PBEGPI5	R	0h	Internal. Only to be used through TI provided API.
4	PBEGPI4	R	0h	Internal. Only to be used through TI provided API.
3	PBEGPI3	R	0h	Internal. Only to be used through TI provided API.
2	PBEGPI2	R	0h	Internal. Only to be used through TI provided API.
1	PBEGPI1	R	0h	Internal. Only to be used through TI provided API.
0	PBEGPI0	R	0h	Internal. Only to be used through TI provided API.

28.7.8 EVTMSK0 Register (Offset = 1Ch) [Reset = 00000000h]

EVTMSK0 is shown in Table 28-138.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-138. EVTMSK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	MDMFAEMPTY	R/W	0h	Internal. Only to be used through TI provided API.
14	S2RSTOP	R/W	0h	Internal. Only to be used through TI provided API.
13	FIFOERR	R/W	0h	Internal. Only to be used through TI provided API.
12	MDMFAFULL	R/W	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP2	R/W	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP1	R/W	0h	Internal. Only to be used through TI provided API.
9	SYSTCMP0	R/W	0h	Internal. Only to be used through TI provided API.
8	MDMMSGBOX	R/W	0h	Internal. Only to be used through TI provided API.
7	RFEMSGBOX	R/W	0h	Internal. Only to be used through TI provided API.
6	RFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
5	RFECMD	R/W	0h	Internal. Only to be used through TI provided API.
4	MDMDAT	R/W	0h	Internal. Only to be used through TI provided API.
3	MDMCMD	R/W	0h	Internal. Only to be used through TI provided API.
2	TIMER1	R/W	0h	Internal. Only to be used through TI provided API.
1	TIMER0	R/W	0h	Internal. Only to be used through TI provided API.
0	PBEAPI	R/W	0h	Internal. Only to be used through TI provided API.

28.7.9 EVTMSK1 Register (Offset = 20h) [Reset = 00000000h]

EVTMSK1 is shown in Table 28-139.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-139. EVTMSK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	TXRDBTHR	R/W	0h	Internal. Only to be used through TI provided API.
11	TXWRBTHR	R/W	0h	Internal. Only to be used through TI provided API.
10	RXRDBTHR	R/W	0h	Internal. Only to be used through TI provided API.
9	RXWRBTHR	R/W	0h	Internal. Only to be used through TI provided API.
8	MDMPROG	R/W	0h	Internal. Only to be used through TI provided API.
7	PBEGPI7	R/W	0h	Internal. Only to be used through TI provided API.
6	PBEGPI6	R/W	0h	Internal. Only to be used through TI provided API.
5	PBEGPI5	R/W	0h	Internal. Only to be used through TI provided API.
4	PBEGPI4	R/W	0h	Internal. Only to be used through TI provided API.
3	PBEGPI3	R/W	0h	Internal. Only to be used through TI provided API.
2	PBEGPI2	R/W	0h	Internal. Only to be used through TI provided API.
1	PBEGPI1	R/W	0h	Internal. Only to be used through TI provided API.
0	PBEGPI0	R/W	0h	Internal. Only to be used through TI provided API.

28.7.10 EVTCLR0 Register (Offset = 24h) [Reset = 00000000h]

EVTCLR0 is shown in Table 28-140.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-140. EVTCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	MDMFAEMPTY	W	0h	Internal. Only to be used through TI provided API.
14	S2RSTOP	W	0h	Internal. Only to be used through TI provided API.
13	FIFOERR	W	0h	Internal. Only to be used through TI provided API.
12	MDMFAFULL	W	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP2	W	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP1	W	0h	Internal. Only to be used through TI provided API.
9	SYSTCMP0	W	0h	Internal. Only to be used through TI provided API.
8	MDMMSGBOX	W	0h	Internal. Only to be used through TI provided API.
7	RFEMSGBOX	W	0h	Internal. Only to be used through TI provided API.
6	RFEDAT	W	0h	Internal. Only to be used through TI provided API.
5	RFECMD	W	0h	Internal. Only to be used through TI provided API.
4	MDMDAT	W	0h	Internal. Only to be used through TI provided API.
3	MDMCMD	W	0h	Internal. Only to be used through TI provided API.
2	TIMER1	W	0h	Internal. Only to be used through TI provided API.
1	TIMER0	W	0h	Internal. Only to be used through TI provided API.
0	PBEAPI	W	0h	Internal. Only to be used through TI provided API.

28.7.11 EVTCLR1 Register (Offset = 28h) [Reset = 00000000h]

EVTCLR1 is shown in Table 28-141.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-141. EVTCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	TXRDBTHR	W	0h	Internal. Only to be used through TI provided API.
11	TXWRBTHR	W	0h	Internal. Only to be used through TI provided API.
10	RXRDBTHR	W	0h	Internal. Only to be used through TI provided API.
9	RXWRBTHR	W	0h	Internal. Only to be used through TI provided API.
8	MDMPROG	W	0h	Internal. Only to be used through TI provided API.
7	PBEGPI7	W	0h	Internal. Only to be used through TI provided API.
6	PBEGPI6	W	0h	Internal. Only to be used through TI provided API.
5	PBEGPI5	W	0h	Internal. Only to be used through TI provided API.
4	PBEGPI4	W	0h	Internal. Only to be used through TI provided API.
3	PBEGPI3	W	0h	Internal. Only to be used through TI provided API.
2	PBEGPI2	W	0h	Internal. Only to be used through TI provided API.
1	PBEGPI1	W	0h	Internal. Only to be used through TI provided API.
0	PBEGPI0	W	0h	Internal. Only to be used through TI provided API.

28.7.12 PDREQ Register (Offset = 2Ch) [Reset = 00000000h]

PDREQ is shown in Table 28-142.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-142. PDREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TOPSMPDREQ	R/W	0h	Internal. Only to be used through TI provided API.

28.7.13 API Register (Offset = 30h) [Reset = 00000000h]

API is shown in Table 28-143.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-143. API Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	PBECMD	R/W	0h	Internal. Only to be used through TI provided API.

28.7.14 MCEDATOUT0 Register (Offset = 34h) [Reset = 00000000h]

MCEDATOUT0 is shown in Table 28-144.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-144. MCEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.15 MCEDATIN0 Register (Offset = 38h) [Reset = 00000000h]

MCEDATIN0 is shown in Table 28-145.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-145. MCEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.16 MCECMDOUT Register (Offset = 3Ch) [Reset = 00000000h]

MCECMDOUT is shown in Table 28-146.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-146. MCECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.17 MCECMDIN Register (Offset = 40h) [Reset = 00000000h]

MCECMDIN is shown in Table 28-147.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-147. MCECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.18 MDMAPI Register (Offset = 44h) [Reset = 00000000h]

MDMAPI is shown in Table 28-148.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-148. MDMAPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	PROTOCOLID	R/W	0h	Internal. Only to be used through TI provided API.
3-0	MDMCMD	R/W	0h	Internal. Only to be used through TI provided API.

28.7.19 MDMMSGBOX Register (Offset = 48h) [Reset = 00000000h]

MDMMSGBOX is shown in Table 28-149.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-149. MDMMSGBOX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

28.7.20 FREQ Register (Offset = 4Ch) [Reset = 00000000h]

FREQ is shown in Table 28-150.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-150. FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	OFFSET	R	0h	Internal. Only to be used through TI provided API.

28.7.21 MDMLQI Register (Offset = 50h) [Reset = 00000000h]

MDMLQI is shown in Table 28-151.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-151. MDMLQI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.22 RFEDATOUT0 Register (Offset = 54h) [Reset = 00000000h]

RFEDATOUT0 is shown in Table 28-152.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-152. RFEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.23 RFEDATIN0 Register (Offset = 58h) [Reset = 00000000h]

RFEDATIN0 is shown in Table 28-153.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-153. RFEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.24 RFECMDOUT Register (Offset = 5Ch) [Reset = 00000000h]

RFECMDOUT is shown in Table 28-154.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-154. RFECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.25 RFECMDIN Register (Offset = 60h) [Reset = 00000000h]

RFECMDIN is shown in Table 28-155.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-155. RFECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.26 RFEAPI Register (Offset = 64h) [Reset = 00000000h]

RFEAPI is shown in Table 28-156.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-156. RFEAPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	PROTOCOLID	R/W	0h	Internal. Only to be used through TI provided API.
3-0	RFECMD	R/W	0h	Internal. Only to be used through TI provided API.

28.7.27 RFECMDPAR0 Register (Offset = 68h) [Reset = 00000000h]

RFECMDPAR0 is shown in Table 28-157.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-157. RFECMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.28 RFECMDPAR1 Register (Offset = 6Ch) [Reset = 00000000h]

RFECMDPAR1 is shown in Table 28-158.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-158. RFECMDPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.29 RFEMSGBOX Register (Offset = 70h) [Reset = 00000000h]

RFEMSGBOX is shown in Table 28-159.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-159. RFEMSGBOX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.30 RFERSSI Register (Offset = 74h) [Reset = 00000000h]

RFERSSI is shown in Table 28-160.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-160. RFERSSI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.31 RFERSSIMAX Register (Offset = 78h) [Reset = 00000000h]

RFERSSIMAX is shown in Table 28-161.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-161. RFERSSIMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.32 RFERFGAIN Register (Offset = 7Ch) [Reset = 00000000h]

RFERFGAIN is shown in Table 28-162.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-162. RFERFGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DBGAIN	R	0h	Internal. Only to be used through TI provided API.

28.7.33 MDMSYNCAL Register (Offset = 80h) [Reset = 00000000h]

MDMSYNCAL is shown in Table 28-163.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-163. MDMSYNCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	SWALSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.34 MDMSYNCAH Register (Offset = 84h) [Reset = 00000000h]

MDMSYNCAH is shown in Table 28-164.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-164. MDMSYNCAH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	SWAMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.35 MDMSYNCBL Register (Offset = 88h) [Reset = 00000000h]

MDMSYNCBL is shown in Table 28-165.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-165. MDMSYNCBL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	SWBLSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.36 MDMSYNCBH Register (Offset = 8Ch) [Reset = 00000000h]

MDMSYNCBH is shown in Table 28-166.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-166. MDMSYNCBH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	SWBMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.37 MDMCMDPAR0 Register (Offset = 90h) [Reset = 00000000h]

MDMCMDPAR0 is shown in Table 28-167.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-167. MDMCMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.38 MDMCMDPAR1 Register (Offset = 94h) [Reset = 00000000h]

MDMCMDPAR1 is shown in Table 28-168.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-168. MDMCMDPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.39 MDMCMDPAR2 Register (Offset = 98h) [Reset = 00000000h]

MDMCMDPAR2 is shown in Table 28-169.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-169. MDMCMDPAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.40 RFEDATIN1 Register (Offset = 9Ch) [Reset = 00000000h]

RFEDATIN1 is shown in Table 28-170.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-170. RFEDATIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.41 POLY0L Register (Offset = A0h) [Reset = 00000000h]

POLY0L is shown in Table 28-171.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-171. POLY0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.42 POLY0H Register (Offset = A4h) [Reset = 00000000h]

POLY0H is shown in Table 28-172.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-172. POLY0H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.43 POLY1L Register (Offset = A8h) [Reset = 00000000h]

POLY1L is shown in Table 28-173.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-173. POLY1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.44 POLY1H Register (Offset = ACh) [Reset = 00000000h]

POLY1H is shown in Table 28-174.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-174. POLY1H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.45 PHACFG Register (Offset = B0h) [Reset = 00000000h]

PHACFG is shown in Table 28-175.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-175. PHACFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-1	MODE1	R/W	0h	Internal. Only to be used through TI provided API.
0	MODE0	R/W	0h	Internal. Only to be used through TI provided API.

28.7.46 FCFG0 Register (Offset = B4h) [Reset = 00000000h]

FCFG0 is shown in Table 28-176.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-176. FCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	TXIRQMET	R/W	0h	Internal. Only to be used through TI provided API.
6	RXIRQMET	R/W	0h	Internal. Only to be used through TI provided API.
5	TXACOM	R/W	1h	Internal. Only to be used through TI provided API.
4	TXADEAL	R/W	0h	Internal. Only to be used through TI provided API.
3-2	RESERVED	R	0h	Reserved
1	RXACOM	R/W	0h	Internal. Only to be used through TI provided API.
0	RXADEAL	R/W	1h	Internal. Only to be used through TI provided API.

28.7.47 FCFG1 Register (Offset = B8h) [Reset = 00000000h]

FCFG1 is shown in Table 28-177.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-177. FCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	TXSTRT	R/W	0h	Internal. Only to be used through TI provided API.

28.7.48 FCFG2 Register (Offset = BCh) [Reset = 00000000h]

FCFG2 is shown in Table 28-178.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-178. FCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	TXHSIZE	R/W	0h	Internal. Only to be used through TI provided API.
7-0	TXSIZE	R/W	0h	Internal. Only to be used through TI provided API.

28.7.49 FCFG3 Register (Offset = C0h) [Reset = 00000000h]

FCFG3 is shown in Table 28-179.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-179. FCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	RXSTRT	R/W	0h	Internal. Only to be used through TI provided API.

28.7.50 FCFG4 Register (Offset = C4h) [Reset = 00000000h]

FCFG4 is shown in Table 28-180.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-180. FCFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	RXHSIZE	R/W	0h	Internal. Only to be used through TI provided API.
7-0	RXSIZE	R/W	0h	Internal. Only to be used through TI provided API.

28.7.51 FCFG5 Register (Offset = C8h) [Reset = 00000000h]

FCFG5 is shown in Table 28-181.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-181. FCFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-6	DMASREQ	R/W	0h	Internal. Only to be used through TI provided API.
5	RESERVED	R	0h	Reserved
4-0	DMAREQ	R/W	0h	Internal. Only to be used through TI provided API.

28.7.52 RXFWBTHRS Register (Offset = CCh) [Reset = 00000000h]

RXFWBTHRS is shown in Table 28-182.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-182. RXFWBTHRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R/W	0h	Internal. Only to be used through TI provided API.

28.7.53 RXFRBTHRS Register (Offset = D0h) [Reset = 00000000h]

RXFRBTHRS is shown in Table 28-183.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-183. RXFRBTHRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R/W	0h	Internal. Only to be used through TI provided API.

28.7.54 TXFWBTHRS Register (Offset = D4h) [Reset = 00000000h]

TXFWBTHRS is shown in Table 28-184.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-184. TXFWBTHRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R/W	0h	Internal. Only to be used through TI provided API.

28.7.55 TXFRBTHRS Register (Offset = D8h) [Reset = 00000000h]

TXFRBTHRS is shown in Table 28-185.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-185. TXFRBTHRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R/W	0h	Internal. Only to be used through TI provided API.

28.7.56 TIMCTL Register (Offset = DCh) [Reset = 00000000h]

TIMCTL is shown in Table 28-186.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-186. TIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-11	CPTSRC1	R/W	0h	Internal. Only to be used through TI provided API.
10	ENCPT1	R/W	0h	Internal. Only to be used through TI provided API.
9	SRC1	R/W	0h	Internal. Only to be used through TI provided API.
8	EN1	R/W	0h	Internal. Only to be used through TI provided API.
7-3	CPTSRC0	R/W	0h	Internal. Only to be used through TI provided API.
2	ENCPT0	R/W	0h	Internal. Only to be used through TI provided API.
1	SRC0	R/W	0h	Internal. Only to be used through TI provided API.
0	EN0	R/W	0h	Internal. Only to be used through TI provided API.

28.7.57 TIMPRE Register (Offset = E0h) [Reset = 00000000h]

TIMPRE is shown in Table 28-187.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-187. TIMPRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	PRE1	R/W	0h	Internal. Only to be used through TI provided API.
7-6	RESERVED	R	0h	Reserved
5-0	PRE0	R/W	0h	Internal. Only to be used through TI provided API.

28.7.58 TIMPER0 Register (Offset = E4h) [Reset = 00000000h]

TIMPER0 is shown in Table 28-188.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-188. TIMPER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.59 TIMPER1 Register (Offset = E8h) [Reset = 00000000h]

TIMPER1 is shown in Table 28-189.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-189. TIMPER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.60 TIMCAPT0 Register (Offset = ECh) [Reset = 00000000h]

TIMCAPT0 is shown in Table 28-190.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-190. TIMCAPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

28.7.61 TIMCAPT1 Register (Offset = F0h) [Reset = 00000000h]

TIMCAPT1 is shown in Table 28-191.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-191. TIMCAPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

28.7.62 TRCCTL Register (Offset = F4h) [Reset = 00000000h]

TRCCTL is shown in Table 28-192.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-192. TRCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SEND	W	0h	Internal. Only to be used through TI provided API.

28.7.63 TRCSTAT Register (Offset = F8h) [Reset = 00000000h]

TRCSTAT is shown in Table 28-193.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-193. TRCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BUSY	R	0h	Internal. Only to be used through TI provided API.

28.7.64 TRCCMD Register (Offset = FCh) [Reset = 00000000h]

TRCCMD is shown in Table 28-194.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-194. TRCCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-8	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.65 TRCPAR0 Register (Offset = 100h) [Reset = 00000000h]

TRCPAR0 is shown in Table 28-195.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-195. TRCPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.66 TRCPAR1 Register (Offset = 104h) [Reset = 00000000h]

TRCPAR1 is shown in Table 28-196.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-196. TRCPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.67 GPOCTRL Register (Offset = 108h) [Reset = 00000000h]

GPOCTRL is shown in Table 28-197.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-197. GPOCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	GPO7	R/W	0h	Internal. Only to be used through TI provided API.
6	GPO6	R/W	0h	Internal. Only to be used through TI provided API.
5	GPO5	R/W	0h	Internal. Only to be used through TI provided API.
4	GPO4	R/W	0h	Internal. Only to be used through TI provided API.
3	GPO3	R/W	0h	Internal. Only to be used through TI provided API.
2	GPO2	R/W	0h	Internal. Only to be used through TI provided API.
1	GPO1	R/W	0h	Internal. Only to be used through TI provided API.
0	GPO0	R/W	0h	Internal. Only to be used through TI provided API.

28.7.68 MDMFWR Register (Offset = 10Ch) [Reset = 00000000h]

MDMFWR is shown in Table 28-198.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-198. MDMFWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PAYLOADIN	R/W	0h	Internal. Only to be used through TI provided API.

28.7.69 MDMFRD Register (Offset = 110h) [Reset = 00000000h]

MDMFRD is shown in Table 28-199.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-199. MDMFRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PAYLOADOUT	R	0h	Internal. Only to be used through TI provided API.

28.7.70 MDMFWRCTL Register (Offset = 114h) [Reset = 00000000h]

MDMFWRCTL is shown in Table 28-200.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-200. MDMFWRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	WORDSZWR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.71 MDMFRDCTL Register (Offset = 118h) [Reset = 00000000h]

MDMFRDCTL is shown in Table 28-201.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-201. MDMFRDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	WORDSZRD	R/W	0h	Internal. Only to be used through TI provided API.

28.7.72 MDMFCFG Register (Offset = 11Ch) [Reset = 00000000h]

MDMFCFG is shown in Table 28-202.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-202. MDMFCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	AFULLTHR	R/W	0h	Internal. Only to be used through TI provided API.
7-0	AEMPTYTHR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.73 MDMFSTA Register (Offset = 120h) [Reset = 00000000h]

MDMFSTA is shown in Table 28-203.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-203. MDMFSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	OVFL	R	0h	Internal. Only to be used through TI provided API.
4	ALMOSTFULL	R	0h	Internal. Only to be used through TI provided API.
3	ALMOSTEMPTY	R	0h	Internal. Only to be used through TI provided API.
2	UNFL	R	0h	Internal. Only to be used through TI provided API.
1	RXVALID	R	0h	Internal. Only to be used through TI provided API.
0	TXREADY	R	0h	Internal. Only to be used through TI provided API.

28.7.74 PHASTA Register (Offset = 124h) [Reset = 00000000h]

PHASTA is shown in Table 28-204.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-204. PHASTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	BUSY	R	0h	Internal. Only to be used through TI provided API.

28.7.75 LFSR0L Register (Offset = 128h) [Reset = 00000000h]

LFSR0L is shown in Table 28-205.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-205. LFSR0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.76 LFSR0H Register (Offset = 12Ch) [Reset = 00000000h]

LFSR0H is shown in Table 28-206.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-206. LFSR0H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.77 LFSR0BRL Register (Offset = 130h) [Reset = 00000000h]

LFSR0BRL is shown in Table 28-207.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-207. LFSR0BRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.78 LFSR0BRH Register (Offset = 134h) [Reset = 00000000h]

LFSR0BRH is shown in Table 28-208.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-208. LFSR0BRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.79 LFSR1L Register (Offset = 138h) [Reset = 00000000h]

LFSR1L is shown in Table 28-209.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-209. LFSR1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.80 LFSR1H Register (Offset = 13Ch) [Reset = 00000000h]

LFSR1H is shown in Table 28-210.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-210. LFSR1H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.81 LFSR1BRL Register (Offset = 140h) [Reset = 00000000h]

LFSR1BRL is shown in Table 28-211.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-211. LFSR1BRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.82 LFSR1BRH Register (Offset = 144h) [Reset = 00000000h]

LFSR1BRH is shown in Table 28-212.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-212. LFSR1BRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	FFFFh	Internal. Only to be used through TI provided API.

28.7.83 LFSR0INL Register (Offset = 148h) [Reset = 00000000h]

LFSR0INL is shown in Table 28-213.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-213. LFSR0INL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.7.84 LFSR0N Register (Offset = 14Ch) [Reset = 00000000h]

LFSR0N is shown in Table 28-214.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-214. LFSR0N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	SIZE	R/W	0h	Internal. Only to be used through TI provided API.

28.7.85 LFSR0INM Register (Offset = 150h) [Reset = 00000000h]

LFSR0INM is shown in Table 28-215.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-215. LFSR0INM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.7.86 PHAOUT0 Register (Offset = 154h) [Reset = 00000000h]

PHAOUT0 is shown in Table 28-216.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-216. PHAOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.7.87 LFSR1INL Register (Offset = 158h) [Reset = 00000000h]

LFSR1INL is shown in Table 28-217.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-217. LFSR1INL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.7.88 LFSR1N Register (Offset = 15Ch) [Reset = 00000000h]

LFSR1N is shown in Table 28-218.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-218. LFSR1N Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	SIZE	R/W	0h	Internal. Only to be used through TI provided API.

28.7.89 LFSR1INM Register (Offset = 160h) [Reset = 00000000h]

LFSR1INM is shown in Table 28-219.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-219. LFSR1INM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.7.90 PHAOUT0BR Register (Offset = 164h) [Reset = 00000000h]

PHAOUT0BR is shown in Table 28-220.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-220. PHAOUT0BR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.7.91 DIVIDENDL Register (Offset = 168h) [Reset = 00000000h]

DIVIDENDL is shown in Table 28-221.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-221. DIVIDENDL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	W	0h	Internal. Only to be used through TI provided API.

28.7.92 DIVIDENDH Register (Offset = 16Ch) [Reset = 00000000h]

DIVIDENDH is shown in Table 28-222.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-222. DIVIDENDH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	W	0h	Internal. Only to be used through TI provided API.

28.7.93 DIVISORL Register (Offset = 170h) [Reset = 00000000h]

DIVISORL is shown in Table 28-223.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-223. DIVISORL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.94 DIVISORH Register (Offset = 174h) [Reset = 00000000h]

DIVISORH is shown in Table 28-224.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-224. DIVISORH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.7.95 QUOTIENTL Register (Offset = 178h) [Reset = 00000000h]

QUOTIENTL is shown in Table 28-225.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-225. QUOTIENTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R	0h	Internal. Only to be used through TI provided API.

28.7.96 QUOTIENTH Register (Offset = 17Ch) [Reset = 00000000h]

QUOTIENTH is shown in Table 28-226.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-226. QUOTIENTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R	0h	Internal. Only to be used through TI provided API.

28.7.97 SYSTIM0L Register (Offset = 180h) [Reset = 00000000h]

SYSTIM0L is shown in Table 28-227.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-227. SYSTIM0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R	0h	Internal. Only to be used through TI provided API.

28.7.98 SYSTIM0H Register (Offset = 184h) [Reset = 00000000h]

SYSTIM0H is shown in Table 28-228.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-228. SYSTIM0H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R	0h	Internal. Only to be used through TI provided API.

28.7.99 SYSTIM1L Register (Offset = 188h) [Reset = 00000000h]

SYSTIM1L is shown in Table 28-229.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-229. SYSTIM1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R	0h	Internal. Only to be used through TI provided API.

28.7.100 SYSTIM1H Register (Offset = 18Ch) [Reset = 00000000h]

SYSTIM1H is shown in Table 28-230.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-230. SYSTIM1H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R	0h	Internal. Only to be used through TI provided API.

28.7.101 SYSTIM2L Register (Offset = 190h) [Reset = 00000000h]

SYSTIM2L is shown in Table 28-231.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-231. SYSTIM2L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R	0h	Internal. Only to be used through TI provided API.

28.7.102 SYSTIM2H Register (Offset = 194h) [Reset = 00000000h]

SYSTIM2H is shown in Table 28-232.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-232. SYSTIM2H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R	0h	Internal. Only to be used through TI provided API.

28.7.103 GPI Register (Offset = 198h) [Reset = 00000000h]

GPI is shown in Table 28-233.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-233. GPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	GPI7	R	0h	Internal. Only to be used through TI provided API.
6	GPI6	R	0h	Internal. Only to be used through TI provided API.
5	GPI5	R	0h	Internal. Only to be used through TI provided API.
4	GPI4	R	0h	Internal. Only to be used through TI provided API.
3	GPI3	R	0h	Internal. Only to be used through TI provided API.
2	GPI2	R	0h	Internal. Only to be used through TI provided API.
1	GPI1	R	0h	Internal. Only to be used through TI provided API.
0	GPI0	R	0h	Internal. Only to be used through TI provided API.

28.7.104 DIVSTA Register (Offset = 19Ch) [Reset = 00000000h]

DIVSTA is shown in Table 28-234.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-234. DIVSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STAT	R	0h	Internal. Only to be used through TI provided API.

28.7.105 FCMD Register (Offset = 1A0h) [Reset = 00000000h]

FCMD is shown in Table 28-235.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-235. FCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	W	0h	Internal. Only to be used through TI provided API.

28.7.106 FSTAT Register (Offset = 1A4h) [Reset = 00000000h]

FSTAT is shown in Table 28-236.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-236. FSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	TXUNFL	R	0h	Internal. Only to be used through TI provided API.
10	TXOVFL	R	0h	Internal. Only to be used through TI provided API.
9	TXEMPTY	R	0h	Internal. Only to be used through TI provided API.
8	TXFULL	R	0h	Internal. Only to be used through TI provided API.
7-4	RESERVED	R	0h	Reserved
3	RXUNFL	R	0h	Internal. Only to be used through TI provided API.
2	RXOVFL	R	0h	Internal. Only to be used through TI provided API.
1	RXEMPTY	R	0h	Internal. Only to be used through TI provided API.
0	RXFULL	R	0h	Internal. Only to be used through TI provided API.

28.7.107 RXFWP Register (Offset = 1A8h) [Reset = 00000000h]

RXFWP is shown in Table 28-237.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-237. RXFWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.108 RXFRP Register (Offset = 1ACh) [Reset = 00000000h]

RXFRP is shown in Table 28-238.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-238. RXFRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.109 RXFSWP Register (Offset = 1B0h) [Reset = 00000000h]

RXFSWP is shown in Table 28-239.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-239. RXFSWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.110 RXFSRP Register (Offset = 1B4h) [Reset = 00000000h]

RXFSRP is shown in Table 28-240.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-240. RXFSRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.111 TXFWP Register (Offset = 1B8h) [Reset = 00000000h]

TXFWP is shown in Table 28-241.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-241. TXFWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.112 TXFRP Register (Offset = 1BCh) [Reset = 00000000h]

TXFRP is shown in Table 28-242.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-242. TXFRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.113 TXFSWP Register (Offset = 1C0h) [Reset = 00000000h]

TXFSWP is shown in Table 28-243.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-243. TXFSWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.114 TXFSRP Register (Offset = 1C4h) [Reset = 00000000h]

TXFSRP is shown in Table 28-244.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-244. TXFSRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.7.115 RXFWRITABLE Register (Offset = 1C8h) [Reset = 00000000h]

RXFWRITABLE is shown in Table 28-245.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-245. RXFWRITABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R	0h	Internal. Only to be used through TI provided API.

28.7.116 RXFREADABLE Register (Offset = 1CCh) [Reset = 00000000h]

RXFREADABLE is shown in Table 28-246.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-246. RXFREADABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R	0h	Internal. Only to be used through TI provided API.

28.7.117 TXFWRITABLE Register (Offset = 1D0h) [Reset = 00000000h]

TXFWRITABLE is shown in Table 28-247.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-247. TXFWRITABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R	0h	Internal. Only to be used through TI provided API.

28.7.118 TXFREADABLE Register (Offset = 1D4h) [Reset = 00000000h]

TXFREADABLE is shown in Table 28-248.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-248. TXFREADABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BYTES	R	0h	Internal. Only to be used through TI provided API.

28.7.119 RXFBRD Register (Offset = 1D8h) [Reset = 00000000h]

RXFBRD is shown in Table 28-249.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-249. RXFBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	R	0h	Internal. Only to be used through TI provided API.

28.7.120 RXFBWR Register (Offset = 1DCh) [Reset = 00000000h]

RXFBWR is shown in Table 28-250.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-250. RXFBWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	W	0h	Internal. Only to be used through TI provided API.

28.7.121 TXFBRD Register (Offset = 1E0h) [Reset = 00000000h]

TXFBRD is shown in Table 28-251.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-251. TXFBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	R	0h	Internal. Only to be used through TI provided API.

28.7.122 TXFBWR Register (Offset = 1E4h) [Reset = 00000000h]

TXFBWR is shown in Table 28-252.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-252. TXFBWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	W	0h	Internal. Only to be used through TI provided API.

28.7.123 RXFHRD Register (Offset = 1E8h) [Reset = 00000000h]

RXFHRD is shown in Table 28-253.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-253. RXFHRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	Internal. Only to be used through TI provided API.

28.7.124 RXFHWR Register (Offset = 1ECh) [Reset = 00000000h]

RXFHWR is shown in Table 28-254.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-254. RXFHWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	W	0h	Internal. Only to be used through TI provided API.

28.7.125 TXFHRD Register (Offset = 1F0h) [Reset = 00000000h]

TXFHRD is shown in Table 28-255.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-255. TXFHRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	Internal. Only to be used through TI provided API.

28.7.126 TXFHWR Register (Offset = 1F4h) [Reset = 00000000h]

TXFHWR is shown in Table 28-256.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-256. TXFHWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	W	0h	Internal. Only to be used through TI provided API.

28.7.127 MCEDATIN1 Register (Offset = 1F8h) [Reset = 00000000h]

MCEDATIN1 is shown in Table 28-257.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-257. MCEDATIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8 LRFDPBE32 Registers

Table 28-258 lists the memory-mapped registers for the LRFDPBE32 registers. All register offset addresses not listed in Table 28-258 should be considered as reserved locations and the register contents should not be modified.

Table 28-258. LRFDPBE32 Registers

Offset	Acronym	Register Name	Section
0h	FWSRC_ENABLE	Internal. Only to be used through TI provided API.	Section 28.8.1
4h	STROBES0_INIT	Internal. Only to be used through TI provided API.	Section 28.8.2
8h	EVT0_IRQ	Internal. Only to be used through TI provided API.	Section 28.8.3
Ch	EVTMSK0_EVT1	Internal. Only to be used through TI provided API.	Section 28.8.4
10h	EVTCLR0_EVTMSK1	Internal. Only to be used through TI provided API.	Section 28.8.5
14h	PDREQ_EVTCLR1	Internal. Only to be used through TI provided API.	Section 28.8.6
18h	MCEDATOUT0_API	Internal. Only to be used through TI provided API.	Section 28.8.7
1Ch	MCECMDOUT_MCEDATIN0	Internal. Only to be used through TI provided API.	Section 28.8.8
20h	MDMAPI_MCECMDIN	Internal. Only to be used through TI provided API.	Section 28.8.9
24h	FREQ_MDMMSGBOX	Internal. Only to be used through TI provided API.	Section 28.8.10
28h	RFEDATOUT0_MDMLQI	Internal. Only to be used through TI provided API.	Section 28.8.11
2Ch	RFECMDOUT_RFEDATIN0	Internal. Only to be used through TI provided API.	Section 28.8.12
30h	RFEAPI_RFECMDIN	Internal. Only to be used through TI provided API.	Section 28.8.13
34h	RFECMDPAR1_RFECMDPAR0	Internal. Only to be used through TI provided API.	Section 28.8.14
38h	RFERSSI_RFEMSGBOX	Internal. Only to be used through TI provided API.	Section 28.8.15
3Ch	RFERFGAIN_RFERSSIMAX	Internal. Only to be used through TI provided API.	Section 28.8.16
40h	MDMSYNCA	Internal. Only to be used through TI provided API.	Section 28.8.17
44h	MDMSYNCB	Internal. Only to be used through TI provided API.	Section 28.8.18
48h	MDMCMDPAR1_MDMCMDPAR0	Internal. Only to be used through TI provided API.	Section 28.8.19
4Ch	RFEDATIN1_MDMCMDPAR2	Internal. Only to be used through TI provided API.	Section 28.8.20
50h	POLY0	Internal. Only to be used through TI provided API.	Section 28.8.21
54h	POLY1	Internal. Only to be used through TI provided API.	Section 28.8.22
58h	FCFG0_PHACFG	Internal. Only to be used through TI provided API.	Section 28.8.23
5Ch	FCFG2_FCFG1	Internal. Only to be used through TI provided API.	Section 28.8.24
60h	FCFG4_FCFG3	Internal. Only to be used through TI provided API.	Section 28.8.25
64h	RXFWBTHRS_FCFG5	Internal. Only to be used through TI provided API.	Section 28.8.26
68h	TXFWBTHRS_RXFRBTHRS	Internal. Only to be used through TI provided API.	Section 28.8.27
6Ch	TIMCTL_TXFRBTHRS	Internal. Only to be used through TI provided API.	Section 28.8.28
70h	TIMPER0_TIMPRE	Internal. Only to be used through TI provided API.	Section 28.8.29
74h	TIMCAPT0_TIMPER1	Internal. Only to be used through TI provided API.	Section 28.8.30
78h	TRCCTL_TIMCAPT1	Internal. Only to be used through TI provided API.	Section 28.8.31
7Ch	TRCCMD_TRCSTAT	Internal. Only to be used through TI provided API.	Section 28.8.32
80h	TRCPAR1_TRCPAR0	Internal. Only to be used through TI provided API.	Section 28.8.33
84h	MDMFWR_GPOCTRL	Internal. Only to be used through TI provided API.	Section 28.8.34
88h	MDMFWRCTL_MDMFRD	Internal. Only to be used through TI provided API.	Section 28.8.35
8Ch	MDMFCFG_MDMFRDCTL	Internal. Only to be used through TI provided API.	Section 28.8.36
90h	PHASTA_MDMFSTA	Internal. Only to be used through TI provided API.	Section 28.8.37
94h	LFSR0	Internal. Only to be used through TI provided API.	Section 28.8.38
98h	LFSR0BR	Internal. Only to be used through TI provided API.	Section 28.8.39
9Ch	LFSR1	Internal. Only to be used through TI provided API.	Section 28.8.40

Table 28-258. LRFDPBE32 Registers (continued)

Offset	Acronym	Register Name	Section
A0h	LFSR1BR	Internal. Only to be used through TI provided API.	Section 28.8.41
A4h	LFSR0N_LFSR0INL	Internal. Only to be used through TI provided API.	Section 28.8.42
A8h	PHAOUT0_LFSR0INM	Internal. Only to be used through TI provided API.	Section 28.8.43
ACh	LFSR1N_LFSR1INL	Internal. Only to be used through TI provided API.	Section 28.8.44
B0h	PHAOUT0BR_LFSR1INM	Internal. Only to be used through TI provided API.	Section 28.8.45
B4h	DIVIDEND	Internal. Only to be used through TI provided API.	Section 28.8.46
B8h	DIVISOR	Internal. Only to be used through TI provided API.	Section 28.8.47
BCh	QUOTIENT	Internal. Only to be used through TI provided API.	Section 28.8.48
C0h	SYSTIM0	Internal. Only to be used through TI provided API.	Section 28.8.49
C4h	SYSTIM1	Internal. Only to be used through TI provided API.	Section 28.8.50
C8h	SYSTIM2	Internal. Only to be used through TI provided API.	Section 28.8.51
CCh	DIVSTA_GPI	Internal. Only to be used through TI provided API.	Section 28.8.52
D0h	FSTAT_FCMD	Internal. Only to be used through TI provided API.	Section 28.8.53
D4h	RXFRP_RXFWP	Internal. Only to be used through TI provided API.	Section 28.8.54
D8h	RXFSRP_RXFSWP	Internal. Only to be used through TI provided API.	Section 28.8.55
DCh	TXFRP_TXFWP	Internal. Only to be used through TI provided API.	Section 28.8.56
E0h	TXFSRP_TXFSWP	Internal. Only to be used through TI provided API.	Section 28.8.57
E4h	RXFREADABLE_RXFWRITABLE	Internal. Only to be used through TI provided API.	Section 28.8.58
E8h	TXFREADABLE_TXFWRITABLE	Internal. Only to be used through TI provided API.	Section 28.8.59
ECh	RXFBWR_RXFBRD	Internal. Only to be used through TI provided API.	Section 28.8.60
F0h	TXFBWR_TXFBRD	Internal. Only to be used through TI provided API.	Section 28.8.61
F4h	RXFHWR_RXFHRD	Internal. Only to be used through TI provided API.	Section 28.8.62
F8h	TXFHWR_TXFHRD	Internal. Only to be used through TI provided API.	Section 28.8.63
FCh	MCEDATIN1	Internal. Only to be used through TI provided API.	Section 28.8.64

Complex bit access types are encoded to fit into small table cells. Table 28-259 shows the codes that are used for access types in this section.

Table 28-259. LRFDPBE32 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.8.1 FWSRC_ENABLE Register (Offset = 0h) [Reset = 00000000h]

FWSRC_ENABLE is shown in Table 28-260.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-260. FWSRC_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	DATARAM	R/W	0h	Internal. Only to be used through TI provided API.
17	FWRAM	R/W	0h	Internal. Only to be used through TI provided API.
16	BANK	R/W	0h	Internal. Only to be used through TI provided API.
15-3	RESERVED	R	0h	Reserved
2	MDMF	R/W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	R/W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	R/W	0h	Internal. Only to be used through TI provided API.

28.8.2 STROBES0_INIT Register (Offset = 4h) [Reset = 00000000h]

STROBES0_INIT is shown in Table 28-261.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-261. STROBES0_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22	TIMCAPT1	W	0h	Internal. Only to be used through TI provided API.
21	TIMCAPT0	W	0h	Internal. Only to be used through TI provided API.
20	S2RTRIG	W	0h	Internal. Only to be used through TI provided API.
19	DMATRIG	W	0h	Internal. Only to be used through TI provided API.
18	SYSTCAPT2	W	0h	Internal. Only to be used through TI provided API.
17	SYSTCAPT1	W	0h	Internal. Only to be used through TI provided API.
16	SYSTCAPT0	W	0h	Internal. Only to be used through TI provided API.
15-5	RESERVED	R	0h	Reserved
4	RFE	W	0h	Internal. Only to be used through TI provided API.
3	MDM	W	0h	Internal. Only to be used through TI provided API.
2	MDMF	W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	W	0h	Internal. Only to be used through TI provided API.

28.8.3 EVT0_IRQ Register (Offset = 8h) [Reset = 00000000h]

EVT0_IRQ is shown in Table 28-262.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-262. EVT0_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MDMFAEMPTY	R	0h	Internal. Only to be used through TI provided API.
30	S2RSTOP	R	0h	Internal. Only to be used through TI provided API.
29	FIFOERR	R	0h	Internal. Only to be used through TI provided API.
28	MDMFAFULL	R	0h	Internal. Only to be used through TI provided API.
27	SYSTCMP2	R	0h	Internal. Only to be used through TI provided API.
26	SYSTCMP1	R	0h	Internal. Only to be used through TI provided API.
25	SYSTCMP0	R	0h	Internal. Only to be used through TI provided API.
24	MDMMSGBOX	R	0h	Internal. Only to be used through TI provided API.
23	RFEMSGBOX	R	0h	Internal. Only to be used through TI provided API.
22	RFEDAT	R	0h	Internal. Only to be used through TI provided API.
21	RFECMD	R	0h	Internal. Only to be used through TI provided API.
20	MDMDAT	R	0h	Internal. Only to be used through TI provided API.
19	MDMCMD	R	0h	Internal. Only to be used through TI provided API.
18	TIMER1	R	0h	Internal. Only to be used through TI provided API.
17	TIMER0	R	0h	Internal. Only to be used through TI provided API.
16	PBEAPI	R	0h	Internal. Only to be used through TI provided API.
15	SOFT15	W	0h	Internal. Only to be used through TI provided API.
14	SOFT14	W	0h	Internal. Only to be used through TI provided API.
13	SOFT13	W	0h	Internal. Only to be used through TI provided API.
12	SOFT12	W	0h	Internal. Only to be used through TI provided API.
11	SOFT11	W	0h	Internal. Only to be used through TI provided API.
10	SOFT10	W	0h	Internal. Only to be used through TI provided API.
9	SOFT9	W	0h	Internal. Only to be used through TI provided API.
8	SOFT8	W	0h	Internal. Only to be used through TI provided API.
7	SOFT7	W	0h	Internal. Only to be used through TI provided API.
6	SOFT6	W	0h	Internal. Only to be used through TI provided API.
5	SOFT5	W	0h	Internal. Only to be used through TI provided API.
4	SOFT4	W	0h	Internal. Only to be used through TI provided API.
3	SOFT3	W	0h	Internal. Only to be used through TI provided API.
2	SOFT2	W	0h	Internal. Only to be used through TI provided API.
1	SOFT1	W	0h	Internal. Only to be used through TI provided API.
0	SOFT0	W	0h	Internal. Only to be used through TI provided API.
9-0	RESERVED	R	0h	Reserved

28.8.4 EVTMSK0_EVT1 Register (Offset = Ch) [Reset = 00000000h]

EVTMSK0_EVT1 is shown in Table 28-263.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-263. EVTMSK0_EVT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MDMFAEMPTY	R/W	0h	Internal. Only to be used through TI provided API.
30	S2RSTOP	R/W	0h	Internal. Only to be used through TI provided API.
29	FIFOERR	R/W	0h	Internal. Only to be used through TI provided API.
28	MDMFAFULL	R/W	0h	Internal. Only to be used through TI provided API.
27	SYSTCMP2	R/W	0h	Internal. Only to be used through TI provided API.
26	SYSTCMP1	R/W	0h	Internal. Only to be used through TI provided API.
25	SYSTCMP0	R/W	0h	Internal. Only to be used through TI provided API.
24	MDMMSGBOX	R/W	0h	Internal. Only to be used through TI provided API.
23	RFEMSGBOX	R/W	0h	Internal. Only to be used through TI provided API.
22	RFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
21	RFECMD	R/W	0h	Internal. Only to be used through TI provided API.
20	MDMDAT	R/W	0h	Internal. Only to be used through TI provided API.
19	MDMCMD	R/W	0h	Internal. Only to be used through TI provided API.
18	TIMER1	R/W	0h	Internal. Only to be used through TI provided API.
17	TIMER0	R/W	0h	Internal. Only to be used through TI provided API.
16	PBEAPI	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12	TXRDBTHR	R	0h	Internal. Only to be used through TI provided API.
11	TXWRBTHR	R	0h	Internal. Only to be used through TI provided API.
10	RXRDBTHR	R	0h	Internal. Only to be used through TI provided API.
9	RXWRBTHR	R	0h	Internal. Only to be used through TI provided API.
8	MDMPROG	R	0h	Internal. Only to be used through TI provided API.
7	PBEGPI7	R	0h	Internal. Only to be used through TI provided API.
6	PBEGPI6	R	0h	Internal. Only to be used through TI provided API.
5	PBEGPI5	R	0h	Internal. Only to be used through TI provided API.
4	PBEGPI4	R	0h	Internal. Only to be used through TI provided API.
3	PBEGPI3	R	0h	Internal. Only to be used through TI provided API.
2	PBEGPI2	R	0h	Internal. Only to be used through TI provided API.
1	PBEGPI1	R	0h	Internal. Only to be used through TI provided API.
0	PBEGPI0	R	0h	Internal. Only to be used through TI provided API.

28.8.5 EVTCLR0_EVTMSK1 Register (Offset = 10h) [Reset = 00000000h]

EVTCLR0_EVTMSK1 is shown in Table 28-264.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-264. EVTCLR0_EVTMSK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MDMFAEMPTY	W	0h	Internal. Only to be used through TI provided API.
30	S2RSTOP	W	0h	Internal. Only to be used through TI provided API.
29	FIFOERR	W	0h	Internal. Only to be used through TI provided API.
28	MDMFAFULL	W	0h	Internal. Only to be used through TI provided API.
27	SYSTCMP2	W	0h	Internal. Only to be used through TI provided API.
26	SYSTCMP1	W	0h	Internal. Only to be used through TI provided API.
25	SYSTCMP0	W	0h	Internal. Only to be used through TI provided API.
24	MDMMSGBOX	W	0h	Internal. Only to be used through TI provided API.
23	RFEMSGBOX	W	0h	Internal. Only to be used through TI provided API.
22	RFEDAT	W	0h	Internal. Only to be used through TI provided API.
21	RFECMD	W	0h	Internal. Only to be used through TI provided API.
20	MDMDAT	W	0h	Internal. Only to be used through TI provided API.
19	MDMCMD	W	0h	Internal. Only to be used through TI provided API.
18	TIMER1	W	0h	Internal. Only to be used through TI provided API.
17	TIMER0	W	0h	Internal. Only to be used through TI provided API.
16	PBEAPI	W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12	TXRDBTHR	R/W	0h	Internal. Only to be used through TI provided API.
11	TXWRBTHR	R/W	0h	Internal. Only to be used through TI provided API.
10	RXRDBTHR	R/W	0h	Internal. Only to be used through TI provided API.
9	RXWRBTHR	R/W	0h	Internal. Only to be used through TI provided API.
8	MDMPROG	R/W	0h	Internal. Only to be used through TI provided API.
7	PBEGPI7	R/W	0h	Internal. Only to be used through TI provided API.
6	PBEGPI6	R/W	0h	Internal. Only to be used through TI provided API.
5	PBEGPI5	R/W	0h	Internal. Only to be used through TI provided API.
4	PBEGPI4	R/W	0h	Internal. Only to be used through TI provided API.
3	PBEGPI3	R/W	0h	Internal. Only to be used through TI provided API.
2	PBEGPI2	R/W	0h	Internal. Only to be used through TI provided API.
1	PBEGPI1	R/W	0h	Internal. Only to be used through TI provided API.
0	PBEGPI0	R/W	0h	Internal. Only to be used through TI provided API.

28.8.6 PDREQ_EVTCLR1 Register (Offset = 14h) [Reset = 00000000h]

PDREQ_EVTCLR1 is shown in Table 28-265.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-265. PDREQ_EVTCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	TOPSMPDREQ	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12	TXRDBTHR	W	0h	Internal. Only to be used through TI provided API.
11	TXWRBTHR	W	0h	Internal. Only to be used through TI provided API.
10	RXRDBTHR	W	0h	Internal. Only to be used through TI provided API.
9	RXWRBTHR	W	0h	Internal. Only to be used through TI provided API.
8	MDMPROG	W	0h	Internal. Only to be used through TI provided API.
7	PBEGPI7	W	0h	Internal. Only to be used through TI provided API.
6	PBEGPI6	W	0h	Internal. Only to be used through TI provided API.
6	RESERVED	R	0h	Reserved
5	PBEGPI5	W	0h	Internal. Only to be used through TI provided API.
4	PBEGPI4	W	0h	Internal. Only to be used through TI provided API.
3	PBEGPI3	W	0h	Internal. Only to be used through TI provided API.
2	PBEGPI2	W	0h	Internal. Only to be used through TI provided API.
1	PBEGPI1	W	0h	Internal. Only to be used through TI provided API.
0	PBEGPI0	W	0h	Internal. Only to be used through TI provided API.

28.8.7 MCEDATOUT0_API Register (Offset = 18h) [Reset = 00000000h]

MCEDATOUT0_API is shown in Table 28-266.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-266. MCEDATOUT0_API Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-5	RESERVED	R	0h	Reserved
4-0	PBECMD	R/W	0h	Internal. Only to be used through TI provided API.

28.8.8 MCECMDOUT_MCEDATIN0 Register (Offset = 1Ch) [Reset = 00000000h]

MCECMDOUT_MCEDATIN0 is shown in Table 28-267.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-267. MCECMDOUT_MCEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	MCECMDOUT_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	MCEDATIN0_VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.9 MDMAPI_MCECMDIN Register (Offset = 20h) [Reset = 00000000h]

MDMAPI_MCECMDIN is shown in Table 28-268.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-268. MDMAPI_MCECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	PROTOCOLID	R/W	0h	Internal. Only to be used through TI provided API.
19-16	MDMCMD	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.10 FREQ_MDMMSGBOX Register (Offset = 24h) [Reset = 00000000h]

FREQ_MDMMSGBOX is shown in Table 28-269.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-269. FREQ_MDMMSGBOX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OFFSET	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

28.8.11 RFEDATOUT0_MDMLQI Register (Offset = 28h) [Reset = 00000000h]

RFEDATOUT0_MDMLQI is shown in Table 28-270.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-270. RFEDATOUT0_MDMLQI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RFEDATOUT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	MDMLQI_VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.12 RFECMDOUT_RFEDATIN0 Register (Offset = 2Ch) [Reset = 00000000h]

RFECMDOUT_RFEDATIN0 is shown in Table 28-271.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-271. RFECMDOUT_RFEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	RFECMDOUT_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	RFEDATIN0_VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.13 RFEAPI_RFECMDIN Register (Offset = 30h) [Reset = 00000000h]

RFEAPI_RFECMDIN is shown in Table 28-272.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-272. RFEAPI_RFECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	PROTOCOLID	R/W	0h	Internal. Only to be used through TI provided API.
19-16	RFECMD	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.14 RFECMDPAR1_RFECMDPAR0 Register (Offset = 34h) [Reset = 00000000h]

RFECMDPAR1_RFECMDPAR0 is shown in Table 28-273.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-273. RFECMDPAR1_RFECMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RFECMDPAR1_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	RFECMDPAR0_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.15 RFERSSI_RFEMSGBOX Register (Offset = 38h) [Reset = 00000000h]

RFERSSI_RFEMSGBOX is shown in Table 28-274.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-274. RFERSSI_RFEMSGBOX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	RFERSSI_VAL	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	RFEMSGBOX_VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.16 RFERFGAIN_RFERSSIMAX Register (Offset = 3Ch) [Reset = 00000000h]

RFERFGAIN_RFERSSIMAX is shown in Table 28-275.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-275. RFERFGAIN_RFERSSIMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	DBGAIN	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.17 MDMSYNCA Register (Offset = 40h) [Reset = 00000000h]

MDMSYNCA is shown in Table 28-276.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-276. MDMSYNCA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SWA	R/W	0h	Internal. Only to be used through TI provided API.

28.8.18 MDMSYNCB Register (Offset = 44h) [Reset = 00000000h]

MDMSYNCB is shown in Table 28-277.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-277. MDMSYNCB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SWB	R/W	0h	Internal. Only to be used through TI provided API.

28.8.19 MDMCMDPAR1_MDMCMDPAR0 Register (Offset = 48h) [Reset = 00000000h]

MDMCMDPAR1_MDMCMDPAR0 is shown in Table 28-278.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-278. MDMCMDPAR1_MDMCMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MDMCMDPAR1_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	MDMCMDPAR0_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.20 RFEDATIN1_MDMCMDPAR2 Register (Offset = 4Ch) [Reset = 00000000h]

RFEDATIN1_MDMCMDPAR2 is shown in Table 28-279.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-279. RFEDATIN1_MDMCMDPAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RFEDATIN1_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	MDMCMDPAR2_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.21 POLY0 Register (Offset = 50h) [Reset = 00000000h]

POLY0 is shown in Table 28-280.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-280. POLY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.22 POLY1 Register (Offset = 54h) [Reset = 00000000h]

POLY1 is shown in Table 28-281.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-281. POLY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.23 FCFG0_PHACFG Register (Offset = 58h) [Reset = 00000000h]

FCFG0_PHACFG is shown in Table 28-282.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-282. FCFG0_PHACFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	TXIRQMET	R/W	0h	Internal. Only to be used through TI provided API.
22	RXIRQMET	R/W	0h	Internal. Only to be used through TI provided API.
21	TXACOM	R/W	1h	Internal. Only to be used through TI provided API.
20	TXADEAL	R/W	0h	Internal. Only to be used through TI provided API.
19-18	RESERVED	R	0h	Reserved
17	RXACOM	R/W	0h	Internal. Only to be used through TI provided API.
16	RXADEAL	R/W	1h	Internal. Only to be used through TI provided API.
15-3	RESERVED	R	0h	Reserved
2-1	MODE1	R/W	0h	Internal. Only to be used through TI provided API.
0	MODE0	R/W	0h	Internal. Only to be used through TI provided API.

28.8.24 FCFG2_FCFG1 Register (Offset = 5Ch) [Reset = 00000000h]

FCFG2_FCFG1 is shown in Table 28-283.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-283. FCFG2_FCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	TXHSIZE	R/W	0h	Internal. Only to be used through TI provided API.
23-16	TXSIZE	R/W	0h	Internal. Only to be used through TI provided API.
15-9	RESERVED	R	0h	Reserved
8-0	TXSTRT	R/W	0h	Internal. Only to be used through TI provided API.

28.8.25 FCFG4_FCFG3 Register (Offset = 60h) [Reset = 00000000h]

FCFG4_FCFG3 is shown in Table 28-284.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-284. FCFG4_FCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-24	RXHSIZE	R/W	0h	Internal. Only to be used through TI provided API.
23-16	RXSIZE	R/W	0h	Internal. Only to be used through TI provided API.
15-9	RESERVED	R	0h	Reserved
8-0	RXSTRT	R/W	0h	Internal. Only to be used through TI provided API.

28.8.26 RXFWBTHRS_FCFG5 Register (Offset = 64h) [Reset = 00000000h]

RXFWBTHRS_FCFG5 is shown in Table 28-285.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-285. RXFWBTHRS_FCFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	BYTES	R/W	0h	Internal. Only to be used through TI provided API.
15-9	RESERVED	R	0h	Reserved
8-6	DMASREQ	R/W	0h	Internal. Only to be used through TI provided API.
5	RESERVED	R	0h	Reserved
4-0	DMAREQ	R/W	0h	Internal. Only to be used through TI provided API.

28.8.27 TXFWBTHRS_RXFRBTHRS Register (Offset = 68h) [Reset = 00000000h]

TXFWBTHRS_RXFRBTHRS is shown in Table 28-286.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-286. TXFWBTHRS_RXFRBTHRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	TXFWBTHRS_BYTES	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	RXFRBTHRS_BYTES	R/W	0h	Internal. Only to be used through TI provided API.

28.8.28 TIMCTL_TXFRBTHRS Register (Offset = 6Ch) [Reset = 00000000h]

TIMCTL_TXFRBTHRS is shown in Table 28-287.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-287. TIMCTL_TXFRBTHRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	CPTSRC1	R/W	0h	Internal. Only to be used through TI provided API.
26	ENCPT1	R/W	0h	Internal. Only to be used through TI provided API.
25	SRC1	R/W	0h	Internal. Only to be used through TI provided API.
24	EN1	R/W	0h	Internal. Only to be used through TI provided API.
23-19	CPTSRC0	R/W	0h	Internal. Only to be used through TI provided API.
18	ENCPT0	R/W	0h	Internal. Only to be used through TI provided API.
17	SRC0	R/W	0h	Internal. Only to be used through TI provided API.
16	EN0	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	BYTES	R/W	0h	Internal. Only to be used through TI provided API.

28.8.29 TIMPER0_TIMPRE Register (Offset = 70h) [Reset = 00000000h]

TIMPER0_TIMPRE is shown in Table 28-288.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-288. TIMPER0_TIMPRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-14	RESERVED	R	0h	Reserved
13-8	PRE1	R/W	0h	Internal. Only to be used through TI provided API.
7-6	RESERVED	R	0h	Reserved
5-0	PRE0	R/W	0h	Internal. Only to be used through TI provided API.

28.8.30 TIMCAPT0_TIMPER1 Register (Offset = 74h) [Reset = 00000000h]

TIMCAPT0_TIMPER1 is shown in Table 28-289.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-289. TIMCAPT0_TIMPER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VALUE	R	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.31 TRCCTL_TIMCAPT1 Register (Offset = 78h) [Reset = 00000000h]

TRCCTL_TIMCAPT1 is shown in Table 28-290.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-290. TRCCTL_TIMCAPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	SEND	W	0h	Internal. Only to be used through TI provided API.
15-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

28.8.32 TRCCMD_TRCSTAT Register (Offset = 7Ch) [Reset = 00000000h]

TRCCMD_TRCSTAT is shown in Table 28-291.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-291. TRCCMD_TRCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.
23-16	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	BUSY	R	0h	Internal. Only to be used through TI provided API.

28.8.33 TRCPAR1_TRCPAR0 Register (Offset = 80h) [Reset = 00000000h]

TRCPAR1_TRCPAR0 is shown in Table 28-292.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-292. TRCPAR1_TRCPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TRCPAR1_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	TRCPAR0_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.34 MDMFWR_GPOCTRL Register (Offset = 84h) [Reset = 00000000h]

MDMFWR_GPOCTRL is shown in Table 28-293.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-293. MDMFWR_GPOCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAYLOADIN	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7	GPO7	R/W	0h	Internal. Only to be used through TI provided API.
6	GPO6	R/W	0h	Internal. Only to be used through TI provided API.
5	GPO5	R/W	0h	Internal. Only to be used through TI provided API.
4	GPO4	R/W	0h	Internal. Only to be used through TI provided API.
3	GPO3	R/W	0h	Internal. Only to be used through TI provided API.
2	GPO2	R/W	0h	Internal. Only to be used through TI provided API.
1	GPO1	R/W	0h	Internal. Only to be used through TI provided API.
0	GPO0	R/W	0h	Internal. Only to be used through TI provided API.

28.8.35 MDMFWRCTL_MDMFRD Register (Offset = 88h) [Reset = 00000000h]

MDMFWRCTL_MDMFRD is shown in Table 28-294.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-294. MDMFWRCTL_MDMFRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	WORDSZWR	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAYLOADOUT	R	0h	Internal. Only to be used through TI provided API.

28.8.36 MDMFCFG_MDMFRDCTL Register (Offset = 8Ch) [Reset = 00000000h]

MDMFCFG_MDMFRDCTL is shown in Table 28-295.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-295. MDMFCFG_MDMFRDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	AFULLTHR	R/W	0h	Internal. Only to be used through TI provided API.
23-16	AEMPTYTHR	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	WORDSZRD	R/W	0h	Internal. Only to be used through TI provided API.

28.8.37 PHASTA_MDMFSTA Register (Offset = 90h) [Reset = 00000000h]

PHASTA_MDMFSTA is shown in Table 28-296.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-296. PHASTA_MDMFSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	BUSY	R	0h	Internal. Only to be used through TI provided API.
15-6	RESERVED	R	0h	Reserved
5	OVFL	R	0h	Internal. Only to be used through TI provided API.
4	ALMOSTFULL	R	0h	Internal. Only to be used through TI provided API.
3	ALMOSTEMPTY	R	0h	Internal. Only to be used through TI provided API.
2	UNFL	R	0h	Internal. Only to be used through TI provided API.
1	RXVALID	R	0h	Internal. Only to be used through TI provided API.
0	TXREADY	R	0h	Internal. Only to be used through TI provided API.

28.8.38 LFSR0 Register (Offset = 94h) [Reset = 00000000h]

LFSR0 is shown in Table 28-297.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-297. LFSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Internal. Only to be used through TI provided API.

28.8.39 LFSR0BR Register (Offset = 98h) [Reset = 00000000h]

LFSR0BR is shown in Table 28-298.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-298. LFSR0BR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Internal. Only to be used through TI provided API.

28.8.40 LFSR1 Register (Offset = 9Ch) [Reset = 00000000h]

LFSR1 is shown in Table 28-299.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-299. LFSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Internal. Only to be used through TI provided API.

28.8.41 LFSR1BR Register (Offset = A0h) [Reset = 00000000h]

LFSR1BR is shown in Table 28-300.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-300. LFSR1BR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Internal. Only to be used through TI provided API.

28.8.42 LFSR0N_LFSR0INL Register (Offset = A4h) [Reset = 00000000h]

LFSR0N_LFSR0INL is shown in Table 28-301.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-301. LFSR0N_LFSR0INL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	SIZE	R/W	0h	Internal. Only to be used through TI provided API.
15-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.8.43 PHAOUT0_LFSR0INM Register (Offset = A8h) [Reset = 00000000h]

PHAOUT0_LFSR0INM is shown in Table 28-302.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-302. PHAOUT0_LFSR0INM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHAOUT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	LFSR0INM_VAL	W	0h	Internal. Only to be used through TI provided API.

28.8.44 LFSR1N_LFSR1INL Register (Offset = ACh) [Reset = 00000000h]

LFSR1N_LFSR1INL is shown in Table 28-303.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-303. LFSR1N_LFSR1INL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	SIZE	R/W	0h	Internal. Only to be used through TI provided API.
15-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.8.45 PHAOUT0BR_LFSR1INM Register (Offset = B0h) [Reset = 00000000h]

PHAOUT0BR_LFSR1INM is shown in Table 28-304.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-304. PHAOUT0BR_LFSR1INM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHAOUT0BR_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	LFSR1INM_VAL	W	0h	Internal. Only to be used through TI provided API.

28.8.46 DIVIDEND Register (Offset = B4h) [Reset = 00000000h]

DIVIDEND is shown in Table 28-305.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-305. DIVIDEND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.8.47 DIVISOR Register (Offset = B8h) [Reset = 00000000h]

DIVISOR is shown in Table 28-306.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-306. DIVISOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.8.48 QUOTIENT Register (Offset = BCh) [Reset = 00000000h]

QUOTIENT is shown in Table 28-307.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-307. QUOTIENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.49 SYSTIM0 Register (Offset = C0h) [Reset = 00000000h]

SYSTIM0 is shown in Table 28-308.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-308. SYSTIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.50 SYSTIM1 Register (Offset = C4h) [Reset = 00000000h]

SYSTIM1 is shown in Table 28-309.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-309. SYSTIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.51 SYSTIM2 Register (Offset = C8h) [Reset = 00000000h]

SYSTIM2 is shown in Table 28-310.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-310. SYSTIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.8.52 DIVSTA_GPI Register (Offset = CCh) [Reset = 00000000h]

DIVSTA_GPI is shown in Table 28-311.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-311. DIVSTA_GPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	STAT	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7	GPI7	R	0h	Internal. Only to be used through TI provided API.
6	GPI6	R	0h	Internal. Only to be used through TI provided API.
5	GPI5	R	0h	Internal. Only to be used through TI provided API.
4	GPI4	R	0h	Internal. Only to be used through TI provided API.
3	GPI3	R	0h	Internal. Only to be used through TI provided API.
2	GPI2	R	0h	Internal. Only to be used through TI provided API.
1	GPI1	R	0h	Internal. Only to be used through TI provided API.
0	GPI0	R	0h	Internal. Only to be used through TI provided API.

28.8.53 FSTAT_FCMD Register (Offset = D0h) [Reset = 00000000h]

FSTAT_FCMD is shown in Table 28-312.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-312. FSTAT_FCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	TXUNFL	R	0h	Internal. Only to be used through TI provided API.
26	TXOVFL	R	0h	Internal. Only to be used through TI provided API.
25	TXEMPTY	R	0h	Internal. Only to be used through TI provided API.
24	TXFULL	R	0h	Internal. Only to be used through TI provided API.
23-20	RESERVED	R	0h	Reserved
19	RXUNFL	R	0h	Internal. Only to be used through TI provided API.
18	RXOVFL	R	0h	Internal. Only to be used through TI provided API.
17	RXEMPTY	R	0h	Internal. Only to be used through TI provided API.
16	RXFULL	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	DATA	W	0h	Internal. Only to be used through TI provided API.

28.8.54 RXFRP_RXFWP Register (Offset = D4h) [Reset = 00000000h]

RXFRP_RXFWP is shown in Table 28-313.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-313. RXFRP_RXFWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	RXFRP_PTR	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	RXFWP_PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.8.55 RXFSRP_RXFSWP Register (Offset = D8h) [Reset = 00000000h]

RXFSRP_RXFSWP is shown in Table 28-314.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-314. RXFSRP_RXFSWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	RXFSRP_PTR	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	RXFSWP_PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.8.56 TXFRP_TXFWP Register (Offset = DCh) [Reset = 00000000h]

TXFRP_TXFWP is shown in Table 28-315.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-315. TXFRP_TXFWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	TXFRP_PTR	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	TXFWP_PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.8.57 TXFSRP_TXFSWP Register (Offset = E0h) [Reset = 00000000h]

TXFSRP_TXFSWP is shown in Table 28-316.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-316. TXFSRP_TXFSWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	TXFSRP_PTR	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	TXFSWP_PTR	R/W	0h	Internal. Only to be used through TI provided API.

28.8.58 RXFREADABLE_RXFWRITABLE Register (Offset = E4h) [Reset = 00000000h]

RXFREADABLE_RXFWRITABLE is shown in Table 28-317.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-317. RXFREADABLE_RXFWRITABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	RXFREADABLE_BYTES	R	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	RXFWRITABLE_BYTES	R	0h	Internal. Only to be used through TI provided API.

28.8.59 TXFREADABLE_TXFWRITABLE Register (Offset = E8h) [Reset = 00000000h]

TXFREADABLE_TXFWRITABLE is shown in Table 28-318.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-318. TXFREADABLE_TXFWRITABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-16	TXFREADABLE_BYTES	R	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-0	TXFWRITABLE_BYTES	R	0h	Internal. Only to be used through TI provided API.

28.8.60 RXFBWR_RXFBRD Register (Offset = ECh) [Reset = 00000000h]

RXFBWR_RXFBRD is shown in Table 28-319.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-319. RXFBWR_RXFBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	RXFBWR_DATA	W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	RXFBRD_DATA	R	0h	Internal. Only to be used through TI provided API.

28.8.61 TXFBWR_TXFBRD Register (Offset = F0h) [Reset = 00000000h]

TXFBWR_TXFBRD is shown in Table 28-320.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-320. TXFBWR_TXFBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	TXFBWR_DATA	W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	TXFBRD_DATA	R	0h	Internal. Only to be used through TI provided API.

28.8.62 RXFHWR_RXFHRD Register (Offset = F4h) [Reset = 00000000h]

RXFHWR_RXFHRD is shown in Table 28-321.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-321. RXFHWR_RXFHRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RXFHWR_DATA	W	0h	Internal. Only to be used through TI provided API.
15-0	RXFHRD_DATA	R	0h	Internal. Only to be used through TI provided API.

28.8.63 TXFHWR_TXFHRD Register (Offset = F8h) [Reset = 00000000h]

TXFHWR_TXFHRD is shown in Table 28-322.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-322. TXFHWR_TXFHRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TXFHWR_DATA	W	0h	Internal. Only to be used through TI provided API.
15-0	TXFHRD_DATA	R	0h	Internal. Only to be used through TI provided API.

28.8.64 MCEDATIN1 Register (Offset = FCh) [Reset = 00000000h]

MCEDATIN1 is shown in Table 28-323.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-323. MCEDATIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9 LRFDRFE Registers

Table 28-324 lists the memory-mapped registers for the LRFDRFE registers. All register offset addresses not listed in Table 28-324 should be considered as reserved locations and the register contents should not be modified.

Table 28-324. LRFDRFE Registers

Offset	Acronym	Register Name	Section
0h	ENABLE	Internal. Only to be used through TI provided API.	Section 28.9.1
4h	FWSRC	Internal. Only to be used through TI provided API.	Section 28.9.2
8h	INIT	Internal. Only to be used through TI provided API.	Section 28.9.3
Ch	PDREQ	Internal. Only to be used through TI provided API.	Section 28.9.4
10h	EVT0	Internal. Only to be used through TI provided API.	Section 28.9.5
14h	EVT1	Internal. Only to be used through TI provided API.	Section 28.9.6
18h	EVTMSK0	Internal. Only to be used through TI provided API.	Section 28.9.7
1Ch	EVTMSK1	Internal. Only to be used through TI provided API.	Section 28.9.8
20h	EVTCLR0	Internal. Only to be used through TI provided API.	Section 28.9.9
24h	EVTCLR1	Internal. Only to be used through TI provided API.	Section 28.9.10
28h	HFXTSTAT	Internal. Only to be used through TI provided API.	Section 28.9.11
30h	RFSTATE	Internal. Only to be used through TI provided API.	Section 28.9.12
38h	SPIN	Internal. Only to be used through TI provided API.	Section 28.9.13
48h	API	Internal. Only to be used through TI provided API.	Section 28.9.14
4Ch	CMDPAR0	Internal. Only to be used through TI provided API.	Section 28.9.15
50h	CMDPAR1	Internal. Only to be used through TI provided API.	Section 28.9.16
54h	MSGBOX	Internal. Only to be used through TI provided API.	Section 28.9.17
58h	MCEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.9.18
5Ch	MCEDATIN0	Internal. Only to be used through TI provided API.	Section 28.9.19
60h	MCECMDOUT	Internal. Only to be used through TI provided API.	Section 28.9.20
64h	MCECMDIN	Internal. Only to be used through TI provided API.	Section 28.9.21
68h	PBEDATOUT1	Internal. Only to be used through TI provided API.	Section 28.9.22
6Ch	PBEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.9.23
70h	PBEDATIN0	Internal. Only to be used through TI provided API.	Section 28.9.24
74h	PBECMDOUT	Internal. Only to be used through TI provided API.	Section 28.9.25
78h	PBECMDIN	Internal. Only to be used through TI provided API.	Section 28.9.26
7Ch	STRB	Internal. Only to be used through TI provided API.	Section 28.9.27
84h	MAGNTHRCFG	Internal. Only to be used through TI provided API.	Section 28.9.28
88h	MAGNTHR	Internal. Only to be used through TI provided API.	Section 28.9.29
8Ch	RSSIOFFSET	Internal. Only to be used through TI provided API.	Section 28.9.30
90h	GAINCTL	Internal. Only to be used through TI provided API.	Section 28.9.31
94h	MAGNCTL0	Internal. Only to be used through TI provided API.	Section 28.9.32
98h	MAGNCTL1	Internal. Only to be used through TI provided API.	Section 28.9.33
9Ch	SPARE0	Internal. Only to be used through TI provided API.	Section 28.9.34
A0h	SPARE1	Internal. Only to be used through TI provided API.	Section 28.9.35
A4h	SPARE2	Internal. Only to be used through TI provided API.	Section 28.9.36
A8h	SPARE3	Internal. Only to be used through TI provided API.	Section 28.9.37
ACh	SPARE4	Internal. Only to be used through TI provided API.	Section 28.9.38
B0h	SPARE5	Internal. Only to be used through TI provided API.	Section 28.9.39
B4h	LNA	Internal. Only to be used through TI provided API.	Section 28.9.40

Table 28-324. LRFDRFE Registers (continued)

Offset	Acronym	Register Name	Section
B8h	IFAMPRFLDO	Internal. Only to be used through TI provided API.	Section 28.9.41
BCh	PA0	Internal. Only to be used through TI provided API.	Section 28.9.42
C0h	ULNA	Internal. Only to be used through TI provided API.	Section 28.9.43
C4h	IFADC0	Internal. Only to be used through TI provided API.	Section 28.9.44
C8h	IFADC1	Internal. Only to be used through TI provided API.	Section 28.9.45
CCh	IFADCLF	Internal. Only to be used through TI provided API.	Section 28.9.46
D0h	IFADCQUANT	Internal. Only to be used through TI provided API.	Section 28.9.47
D4h	IFADCALDO	Internal. Only to be used through TI provided API.	Section 28.9.48
D8h	IFADCDLDO	Internal. Only to be used through TI provided API.	Section 28.9.49
DCh	IFADCTST	Internal. Only to be used through TI provided API.	Section 28.9.50
E0h	ATSTREFL	Internal. Only to be used through TI provided API.	Section 28.9.51
E4h	ATSTREFH	Internal. Only to be used through TI provided API.	Section 28.9.52
E8h	DCO	Internal. Only to be used through TI provided API.	Section 28.9.53
ECh	DIV	Internal. Only to be used through TI provided API.	Section 28.9.54
F0h	DIVLDO	Internal. Only to be used through TI provided API.	Section 28.9.55
F4h	TDCLDO	Internal. Only to be used through TI provided API.	Section 28.9.56
F8h	DCOLDO0	Internal. Only to be used through TI provided API.	Section 28.9.57
FCh	DCOLDO1	Internal. Only to be used through TI provided API.	Section 28.9.58
100h	PRE0	Internal. Only to be used through TI provided API.	Section 28.9.59
104h	PRE1	Internal. Only to be used through TI provided API.	Section 28.9.60
108h	PRE2	Internal. Only to be used through TI provided API.	Section 28.9.61
10Ch	PRE3	Internal. Only to be used through TI provided API.	Section 28.9.62
110h	CAL0	Internal. Only to be used through TI provided API.	Section 28.9.63
114h	CAL1	Internal. Only to be used through TI provided API.	Section 28.9.64
118h	CAL2	Internal. Only to be used through TI provided API.	Section 28.9.65
11Ch	CAL3	Internal. Only to be used through TI provided API.	Section 28.9.66
120h	MISC0	Internal. Only to be used through TI provided API.	Section 28.9.67
124h	MISC1	Internal. Only to be used through TI provided API.	Section 28.9.68
128h	LF0	Internal. Only to be used through TI provided API.	Section 28.9.69
12Ch	LF1	Internal. Only to be used through TI provided API.	Section 28.9.70
130h	PHEDISC	Internal. Only to be used through TI provided API.	Section 28.9.71
134h	PHINIT	Internal. Only to be used through TI provided API.	Section 28.9.72
138h	PLLMON0	Internal. Only to be used through TI provided API.	Section 28.9.73
13Ch	PLLMON1	Internal. Only to be used through TI provided API.	Section 28.9.74
140h	MOD0	Internal. Only to be used through TI provided API.	Section 28.9.75
144h	MOD1	Internal. Only to be used through TI provided API.	Section 28.9.76
148h	DTX0	Internal. Only to be used through TI provided API.	Section 28.9.77
14Ch	DTX1	Internal. Only to be used through TI provided API.	Section 28.9.78
150h	DTX2	Internal. Only to be used through TI provided API.	Section 28.9.79
154h	DTX3	Internal. Only to be used through TI provided API.	Section 28.9.80
158h	DTX4	Internal. Only to be used through TI provided API.	Section 28.9.81
15Ch	DTX5	Internal. Only to be used through TI provided API.	Section 28.9.82
160h	DTX6	Internal. Only to be used through TI provided API.	Section 28.9.83
164h	DTX7	Internal. Only to be used through TI provided API.	Section 28.9.84
168h	DTX8	Internal. Only to be used through TI provided API.	Section 28.9.85

Table 28-324. LRFDRFE Registers (continued)

Offset	Acronym	Register Name	Section
16Ch	DTX9	Internal. Only to be used through TI provided API.	Section 28.9.86
170h	DTX10	Internal. Only to be used through TI provided API.	Section 28.9.87
174h	DTX11	Internal. Only to be used through TI provided API.	Section 28.9.88
178h	PLLM0L	Internal. Only to be used through TI provided API.	Section 28.9.89
17Ch	PLLM0H	Internal. Only to be used through TI provided API.	Section 28.9.90
180h	PLLM1L	Internal. Only to be used through TI provided API.	Section 28.9.91
184h	PLLM1H	Internal. Only to be used through TI provided API.	Section 28.9.92
188h	CALMCRS	Internal. Only to be used through TI provided API.	Section 28.9.93
18Ch	CALMMID	Internal. Only to be used through TI provided API.	Section 28.9.94
190h	REFDIV	Internal. Only to be used through TI provided API.	Section 28.9.95
198h	DLOCTL0	Internal. Only to be used through TI provided API.	Section 28.9.96
1A0h	DLOCTL1	Internal. Only to be used through TI provided API.	Section 28.9.97
1A8h	DCOOVR0	Internal. Only to be used through TI provided API.	Section 28.9.98
1ACh	DCOOVR1	Internal. Only to be used through TI provided API.	Section 28.9.99
1B0h	DTST	Internal. Only to be used through TI provided API.	Section 28.9.100
1B4h	DLOEV	Internal. Only to be used through TI provided API.	Section 28.9.101
1B8h	DTSTRD	Internal. Only to be used through TI provided API.	Section 28.9.102
1C0h	FDCOSPANLSB	Internal. Only to be used through TI provided API.	Section 28.9.103
1C4h	FDCOSPANMSB	Internal. Only to be used through TI provided API.	Section 28.9.104
1C8h	TDCCAL	Internal. Only to be used through TI provided API.	Section 28.9.105
1CCh	TDCCALLOW	Internal. Only to be used through TI provided API.	Section 28.9.106
1D0h	TDCCALHIGH	Internal. Only to be used through TI provided API.	Section 28.9.107
1D4h	TDCODET	Internal. Only to be used through TI provided API.	Section 28.9.108
1D8h	CALRES	Internal. Only to be used through TI provided API.	Section 28.9.109
1DCh	GPI	Internal. Only to be used through TI provided API.	Section 28.9.110
1E0h	MATHACCELIN	Internal. Only to be used through TI provided API.	Section 28.9.111
1E4h	LIN2LOGOUT	Internal. Only to be used through TI provided API.	Section 28.9.112
1E8h	DIVBY3OUT	Internal. Only to be used through TI provided API.	Section 28.9.113
1ECh	TIMCTL	Internal. Only to be used through TI provided API.	Section 28.9.114
1F0h	TIMINC	Internal. Only to be used through TI provided API.	Section 28.9.115
1F4h	TIMPER	Internal. Only to be used through TI provided API.	Section 28.9.116
1F8h	TIMCNT	Internal. Only to be used through TI provided API.	Section 28.9.117
1FCh	TIMCAPT	Internal. Only to be used through TI provided API.	Section 28.9.118
200h	TRCCTRL	Internal. Only to be used through TI provided API.	Section 28.9.119
204h	TRCSTAT	Internal. Only to be used through TI provided API.	Section 28.9.120
208h	TRCCMD	Internal. Only to be used through TI provided API.	Section 28.9.121
20Ch	TRCPAR0	Internal. Only to be used through TI provided API.	Section 28.9.122
210h	TRCPAR1	Internal. Only to be used through TI provided API.	Section 28.9.123
214h	GPOCTL	Internal. Only to be used through TI provided API.	Section 28.9.124
218h	ANAISOCTL	Internal. Only to be used through TI provided API.	Section 28.9.125
21Ch	DIVCTL	Internal. Only to be used through TI provided API.	Section 28.9.126
220h	RXCTRL	Internal. Only to be used through TI provided API.	Section 28.9.127
224h	MAGNACC0	Internal. Only to be used through TI provided API.	Section 28.9.128
228h	MAGNACC1	Internal. Only to be used through TI provided API.	Section 28.9.129
22Ch	RSSI	Internal. Only to be used through TI provided API.	Section 28.9.130

Table 28-324. LRFDRFE Registers (continued)

Offset	Acronym	Register Name	Section
230h	RSSIMAX	Internal. Only to be used through TI provided API.	Section 28.9.131
234h	RFGAIN	Internal. Only to be used through TI provided API.	Section 28.9.132
238h	IFADCSTAT	Internal. Only to be used through TI provided API.	Section 28.9.133
23Ch	DIVSTA	Internal. Only to be used through TI provided API.	Section 28.9.134
240h	DIVIDENDL	Internal. Only to be used through TI provided API.	Section 28.9.135
244h	DIVIDENDH	Internal. Only to be used through TI provided API.	Section 28.9.136
248h	DIVISORL	Internal. Only to be used through TI provided API.	Section 28.9.137
24Ch	DIVISORH	Internal. Only to be used through TI provided API.	Section 28.9.138
250h	QUOTIENTL	Internal. Only to be used through TI provided API.	Section 28.9.139
254h	QUOTIENTH	Internal. Only to be used through TI provided API.	Section 28.9.140
258h	PRODUCTL	Internal. Only to be used through TI provided API.	Section 28.9.141
25Ch	PRODUCTH	Internal. Only to be used through TI provided API.	Section 28.9.142
260h	MULTSTA	Internal. Only to be used through TI provided API.	Section 28.9.143
268h	MULTCFG	Internal. Only to be used through TI provided API.	Section 28.9.144
26Ch	PA1	Internal. Only to be used through TI provided API.	Section 28.9.145
270h	PA2	Internal. Only to be used through TI provided API.	Section 28.9.146

Complex bit access types are encoded to fit into small table cells. Table 28-325 shows the codes that are used for access types in this section.

Table 28-325. LRFDRFE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.9.1 ENABLE Register (Offset = 0h) [Reset = 00000000h]

ENABLE is shown in Table 28-326.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-326. ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	ACC1	R/W	0h	Internal. Only to be used through TI provided API.
2	ACC0	R/W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	R/W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	R/W	0h	Internal. Only to be used through TI provided API.

28.9.2 FWSRC Register (Offset = 4h) [Reset = 00000000h]

FWSRC is shown in Table 28-327.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-327. FWSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	DATARAM	R/W	0h	Internal. Only to be used through TI provided API.
1	FWRAM	R/W	0h	Internal. Only to be used through TI provided API.
0	BANK	R/W	0h	Internal. Only to be used through TI provided API.

28.9.3 INIT Register (Offset = 8h) [Reset = 00000000h]

INIT is shown in Table 28-328.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-328. INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	ACC1	W	0h	Internal. Only to be used through TI provided API.
2	ACC0	W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	W	0h	Internal. Only to be used through TI provided API.

28.9.4 PDREQ Register (Offset = Ch) [Reset = 00000000h]

PDREQ is shown in Table 28-329.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-329. PDREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TOPSMPDREQ	R/W	0h	Internal. Only to be used through TI provided API.

28.9.5 EVT0 Register (Offset = 10h) [Reset = 00000000h]

EVT0 is shown in Table 28-330.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-330. EVT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MAGNTHR	R	0h	Internal. Only to be used through TI provided API.
13	S2RSTOP	R	0h	Internal. Only to be used through TI provided API.
12	SYSTCMP2	R	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP1	R	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP0	R	0h	Internal. Only to be used through TI provided API.
9	PBERFEDAT	R	0h	Internal. Only to be used through TI provided API.
8	MDMRFEDAT	R	0h	Internal. Only to be used through TI provided API.
7	DLO	R	0h	Internal. Only to be used through TI provided API.
6	PBECMD	R	0h	Internal. Only to be used through TI provided API.
5	COUNTER	R	0h	Internal. Only to be used through TI provided API.
4	MDMCMD	R	0h	Internal. Only to be used through TI provided API.
3	ACC1	R	0h	Internal. Only to be used through TI provided API.
2	ACC0	R	0h	Internal. Only to be used through TI provided API.
1	TIMER	R	0h	Internal. Only to be used through TI provided API.
0	RFEAPI	R	0h	Internal. Only to be used through TI provided API.

28.9.6 EVT1 Register (Offset = 14h) [Reset = 00000000h]

EVT1 is shown in Table 28-331.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-331. EVT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	PREREFCLK	R	0h	Internal. Only to be used through TI provided API.
12	REFCLK	R	0h	Internal. Only to be used through TI provided API.
11	FBLWTHR	R	0h	Internal. Only to be used through TI provided API.
10	FABVTHR	R	0h	Internal. Only to be used through TI provided API.
9	LOCK	R	0h	Internal. Only to be used through TI provided API.
8	LOL	R	0h	Internal. Only to be used through TI provided API.
7	GPI7	R	0h	Internal. Only to be used through TI provided API.
6	GPI6	R	0h	Internal. Only to be used through TI provided API.
5	GPI5	R	0h	Internal. Only to be used through TI provided API.
4	GPI4	R	0h	Internal. Only to be used through TI provided API.
3	GPI3	R	0h	Internal. Only to be used through TI provided API.
2	GPI2	R	0h	Internal. Only to be used through TI provided API.
1	GPI1	R	0h	Internal. Only to be used through TI provided API.
0	GPI0	R	0h	Internal. Only to be used through TI provided API.

28.9.7 EVTMSK0 Register (Offset = 18h) [Reset = 00000000h]

EVTMSK0 is shown in Table 28-332.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-332. EVTMSK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MAGNTHR	R/W	0h	Internal. Only to be used through TI provided API.
13	S2RSTOP	R/W	0h	Internal. Only to be used through TI provided API.
12	SYSTCMP2	R/W	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP1	R/W	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP0	R/W	0h	Internal. Only to be used through TI provided API.
9	PBERFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
8	MDMRFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
7	DLO	R/W	0h	Internal. Only to be used through TI provided API.
6	PBECMD	R/W	0h	Internal. Only to be used through TI provided API.
5	COUNTER	R/W	0h	Internal. Only to be used through TI provided API.
4	MDMCMD	R/W	0h	Internal. Only to be used through TI provided API.
3	ACC1	R/W	0h	Internal. Only to be used through TI provided API.
2	ACC0	R/W	0h	Internal. Only to be used through TI provided API.
1	TIMER	R/W	0h	Internal. Only to be used through TI provided API.
0	RFEAPI	R/W	0h	Internal. Only to be used through TI provided API.

28.9.8 EVTMSK1 Register (Offset = 1Ch) [Reset = 00000000h]

EVTMSK1 is shown in Table 28-333.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-333. EVTMSK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	PREREFCLK	R/W	0h	Internal. Only to be used through TI provided API.
12	REFCLK	R/W	0h	Internal. Only to be used through TI provided API.
11	FBLWTHR	R/W	0h	Internal. Only to be used through TI provided API.
10	FABVTHR	R/W	0h	Internal. Only to be used through TI provided API.
9	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
8	LOL	R/W	0h	Internal. Only to be used through TI provided API.
7	GPI7	R/W	0h	Internal. Only to be used through TI provided API.
6	GPI6	R/W	0h	Internal. Only to be used through TI provided API.
5	GPI5	R/W	0h	Internal. Only to be used through TI provided API.
4	GPI4	R/W	0h	Internal. Only to be used through TI provided API.
3	GPI3	R/W	0h	Internal. Only to be used through TI provided API.
2	GPI2	R/W	0h	Internal. Only to be used through TI provided API.
1	GPI1	R/W	0h	Internal. Only to be used through TI provided API.
0	GPI0	R/W	0h	Internal. Only to be used through TI provided API.

28.9.9 EVTCLR0 Register (Offset = 20h) [Reset = 00000000h]

EVTCLR0 is shown in Table 28-334.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-334. EVTCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MAGNTHR	W	0h	Internal. Only to be used through TI provided API.
13	S2RSTOP	W	0h	Internal. Only to be used through TI provided API.
12	SYSTCMP2	W	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP1	W	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP0	W	0h	Internal. Only to be used through TI provided API.
9	PBERFEDAT	W	0h	Internal. Only to be used through TI provided API.
8	MDMRFEDAT	W	0h	Internal. Only to be used through TI provided API.
7	DLO	W	0h	Internal. Only to be used through TI provided API.
6	PBECMD	W	0h	Internal. Only to be used through TI provided API.
5	COUNTER	W	0h	Internal. Only to be used through TI provided API.
4	MDMCMD	W	0h	Internal. Only to be used through TI provided API.
3	ACC1	W	0h	Internal. Only to be used through TI provided API.
2	ACC0	W	0h	Internal. Only to be used through TI provided API.
1	TIMER	W	0h	Internal. Only to be used through TI provided API.
0	RFEAPI	W	0h	Internal. Only to be used through TI provided API.

28.9.10 EVTCLR1 Register (Offset = 24h) [Reset = 00000000h]

EVTCLR1 is shown in Table 28-335.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-335. EVTCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	PREREFCLK	W	0h	Internal. Only to be used through TI provided API.
12	REFCLK	W	0h	Internal. Only to be used through TI provided API.
11	FBLWTHR	W	0h	Internal. Only to be used through TI provided API.
10	FABVTHR	W	0h	Internal. Only to be used through TI provided API.
9	LOCK	W	0h	Internal. Only to be used through TI provided API.
8	LOL	W	0h	Internal. Only to be used through TI provided API.
7	GPI7	W	0h	Internal. Only to be used through TI provided API.
6	GPI6	W	0h	Internal. Only to be used through TI provided API.
5	GPI5	W	0h	Internal. Only to be used through TI provided API.
4	GPI4	W	0h	Internal. Only to be used through TI provided API.
3	GPI3	W	0h	Internal. Only to be used through TI provided API.
2	GPI2	W	0h	Internal. Only to be used through TI provided API.
1	GPI1	W	0h	Internal. Only to be used through TI provided API.
0	GPI0	W	0h	Internal. Only to be used through TI provided API.

28.9.11 HFXTSTAT Register (Offset = 28h) [Reset = 00000000h]

HFXTSTAT is shown in Table 28-336.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-336. HFXTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STAT	R	0h	Internal. Only to be used through TI provided API.

28.9.12 RFSTATE Register (Offset = 30h) [Reset = 00000000h]

RFSTATE is shown in Table 28-337.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-337. RFSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.13 SPIN Register (Offset = 38h) [Reset = 00000000h]

SPIN is shown in Table 28-338.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-338. SPIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	OPT	R	0h	Internal. Only to be used through TI provided API.

28.9.14 API Register (Offset = 48h) [Reset = 00000000h]

API is shown in Table 28-339.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-339. API Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	PROTOCOLID	R	0h	Internal. Only to be used through TI provided API.
3-0	RFECMD	R	0h	Internal. Only to be used through TI provided API.

28.9.15 CMDPAR0 Register (Offset = 4Ch) [Reset = 00000000h]

CMDPAR0 is shown in Table 28-340.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-340. CMDPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.16 CMDPAR1 Register (Offset = 50h) [Reset = 00000000h]

CMDPAR1 is shown in Table 28-341.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-341. CMDPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.17 MSGBOX Register (Offset = 54h) [Reset = 00000000h]

MSGBOX is shown in Table 28-342.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-342. MSGBOX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.18 MCEDATOUT0 Register (Offset = 58h) [Reset = 00000000h]

MCEDATOUT0 is shown in Table 28-343.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-343. MCEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.19 MCEDATIN0 Register (Offset = 5Ch) [Reset = 00000000h]

MCEDATIN0 is shown in Table 28-344.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-344. MCEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.20 MCECMDOUT Register (Offset = 60h) [Reset = 00000000h]

MCECMDOUT is shown in Table 28-345.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-345. MCECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.21 MCECMDIN Register (Offset = 64h) [Reset = 00000000h]

MCECMDIN is shown in Table 28-346.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-346. MCECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.22 PBEDATOUT1 Register (Offset = 68h) [Reset = 00000000h]

PBEDATOUT1 is shown in Table 28-347.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-347. PBEDATOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.23 PBEDATOUT0 Register (Offset = 6Ch) [Reset = 00000000h]

PBEDATOUT0 is shown in Table 28-348.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-348. PBEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.24 PBEDATIN0 Register (Offset = 70h) [Reset = 00000000h]

PBEDATIN0 is shown in Table 28-349.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-349. PBEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.25 PBECMDOUT Register (Offset = 74h) [Reset = 00000000h]

PBECMDOUT is shown in Table 28-350.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-350. PBECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.26 PBECMDIN Register (Offset = 78h) [Reset = 00000000h]

PBECMDIN is shown in Table 28-351.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-351. PBECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.27 STRB Register (Offset = 7Ch) [Reset = 00000000h]

STRB is shown in Table 28-352.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-352. STRB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	S2RTRG	W	0h	Internal. Only to be used through TI provided API.
6	DMATRG	W	0h	Internal. Only to be used through TI provided API.
5	SYSTCPT2	W	0h	Internal. Only to be used through TI provided API.
4	SYSTCPT1	W	0h	Internal. Only to be used through TI provided API.
3	SYSTCPT0	W	0h	Internal. Only to be used through TI provided API.
2	EVT1	W	0h	Internal. Only to be used through TI provided API.
1	EVT0	W	0h	Internal. Only to be used through TI provided API.
0	CMDDONE	W	0h	Internal. Only to be used through TI provided API.

28.9.28 MAGNTHRCFG Register (Offset = 84h) [Reset = 00000000h]

MAGNTHRCFG is shown in Table 28-353.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-353. MAGNTHRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	SEL	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.29 MAGNTHR Register (Offset = 88h) [Reset = 00000000h]

MAGNTHR is shown in Table 28-354.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-354. MAGNTHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.30 RSSIOFFSET Register (Offset = 8Ch) [Reset = 00000000h]

RSSIOFFSET is shown in Table 28-355.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-355. RSSIOFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.31 GAINCTL Register (Offset = 90h) [Reset = 00000000h]

GAINCTL is shown in Table 28-356.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-356. GAINCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	BDE2DVGA	R/W	0h	Internal. Only to be used through TI provided API.
1-0	BDE1DVGA	R/W	0h	Internal. Only to be used through TI provided API.

28.9.32 MAGNCTL0 Register (Offset = 94h) [Reset = 00000000h]

MAGNCTL0 is shown in Table 28-357.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-357. MAGNCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	PERMODE	R/W	0h	Internal. Only to be used through TI provided API.
11-8	SCL	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PER	R/W	0h	Internal. Only to be used through TI provided API.

28.9.33 MAGNCTL1 Register (Offset = 98h) [Reset = 00000000h]

MAGNCTL1 is shown in Table 28-358.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-358. MAGNCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	PERMODE	R/W	0h	Internal. Only to be used through TI provided API.
11-8	SCL	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PER	R/W	0h	Internal. Only to be used through TI provided API.

28.9.34 SPARE0 Register (Offset = 9Ch) [Reset = 00000000h]

SPARE0 is shown in Table 28-359.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-359. SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.35 SPARE1 Register (Offset = A0h) [Reset = 00000000h]

SPARE1 is shown in Table 28-360.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-360. SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.36 SPARE2 Register (Offset = A4h) [Reset = 00000000h]

SPARE2 is shown in Table 28-361.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-361. SPARE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.37 SPARE3 Register (Offset = A8h) [Reset = 00000000h]

SPARE3 is shown in Table 28-362.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-362. SPARE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.38 SPARE4 Register (Offset = ACh) [Reset = 00000000h]

SPARE4 is shown in Table 28-363.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-363. SPARE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.39 SPARE5 Register (Offset = B0h) [Reset = 00000000h]

SPARE5 is shown in Table 28-364.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-364. SPARE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.40 LNA Register (Offset = B4h) [Reset = 00000000h]

LNA is shown in Table 28-365.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-365. LNA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-13	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
12	PA20DBMATSTSEL	R/W	0h	Internal. Only to be used through TI provided API.
11	PA20DBMATST	R/W	0h	Internal. Only to be used through TI provided API.
10	MIXATST	R/W	0h	Internal. Only to be used through TI provided API.
9	LDOITST	R/W	0h	Internal. Only to be used through TI provided API.
8	LDOATST	R/W	0h	Internal. Only to be used through TI provided API.
7-4	TRIM	R/W	0h	Internal. Only to be used through TI provided API.
3	MIXCAP	R/W	0h	Internal. Only to be used through TI provided API.
2-1	IB	R/W	0h	Internal. Only to be used through TI provided API.
0	EN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.41 IFAMPRFLDO Register (Offset = B8h) [Reset = 00000000h]

IFAMPRFLDO is shown in Table 28-366.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-366. IFAMPRFLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-9	TRIM	R/W	0h	Internal. Only to be used through TI provided API.
8	EN	R/W	0h	Internal. Only to be used through TI provided API.
7-4	AAFCAP	R/W	0h	Internal. Only to be used through TI provided API.
3-1	IFAMPIB	R/W	0h	Internal. Only to be used through TI provided API.
0	IFAMP	R/W	0h	Internal. Only to be used through TI provided API.

28.9.42 PA0 Register (Offset = BCh) [Reset = 00000000h]

PA0 is shown in Table 28-367.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-367. PA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	SPARE14	R/W	0h	Internal. Only to be used through TI provided API.
13	BIASSEL	R/W	0h	Internal. Only to be used through TI provided API.
12	PA20DBMESDCTL	R/W	0h	Internal. Only to be used through TI provided API.
11-9	VCADJSCND	R/W	0h	Internal. Only to be used through TI provided API.
8-6	VCADJFRST	R/W	0h	Internal. Only to be used through TI provided API.
5-4	RC	R/W	0h	Internal. Only to be used through TI provided API.
3-2	SPARE2	R/W	0h	Internal. Only to be used through TI provided API.
1	RAMP	R/W	0h	Internal. Only to be used through TI provided API.
0	EN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.43 ULNA Register (Offset = C0h) [Reset = 00000000h]

ULNA is shown in Table 28-368.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-368. ULNA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	SPARE	R/W	0h	Internal. Only to be used through TI provided API.

28.9.44 IFADC0 Register (Offset = C4h) [Reset = 00000000h]

IFADC0 is shown in Table 28-369.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-369. IFADC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	EXTCLK	R/W	0h	Internal. Only to be used through TI provided API.
14-12	DITHERTRIM	R/W	0h	Internal. Only to be used through TI provided API.
11-10	DITHEREN	R/W	0h	Internal. Only to be used through TI provided API.
9	ADCIEN	R/W	0h	Internal. Only to be used through TI provided API.
8	ADCQEN	R/W	0h	Internal. Only to be used through TI provided API.
7-4	INT2ADJ	R/W	0h	Internal. Only to be used through TI provided API.
3-2	AAFCAP	R/W	0h	Internal. Only to be used through TI provided API.
1-0	RESERVED	R	0h	Internal. Only to be used through TI provided API.

28.9.45 IFADC1 Register (Offset = C8h) [Reset = 00000000h]

IFADC1 is shown in Table 28-370.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-370. IFADC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NRZ	R/W	0h	Internal. Only to be used through TI provided API.
14-9	TRIM	R/W	0h	Internal. Only to be used through TI provided API.
8	RESERVED	R	0h	Internal. Only to be used through TI provided API.
7	RSTN	R/W	0h	Internal. Only to be used through TI provided API.
6	CLKGEN	R/W	0h	Internal. Only to be used through TI provided API.
5	ADCDIGCLK	R/W	0h	Internal. Only to be used through TI provided API.
4	ADCLFSROUT	R/W	0h	Internal. Only to be used through TI provided API.
3-1	LPFTSTMODE	R/W	0h	Internal. Only to be used through TI provided API.
0	INVCLKOUT	R/W	0h	Internal. Only to be used through TI provided API.

28.9.46 IFADCLF Register (Offset = CCh) [Reset = 00000000h]

IFADCLF is shown in Table 28-371.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-371. IFADCLF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	FF3	R/W	0h	Internal. Only to be used through TI provided API.
11-8	FF2	R/W	0h	Internal. Only to be used through TI provided API.
7-4	FF1	R/W	0h	Internal. Only to be used through TI provided API.
3-0	INT3	R/W	0h	Internal. Only to be used through TI provided API.

28.9.47 IFADCQUANT Register (Offset = D0h) [Reset = 00000000h]

IFADCQUANT is shown in Table 28-372.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-372. IFADCQUANT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	CLKDLYTRIM	R/W	0h	Internal. Only to be used through TI provided API.
13-9	DBGCALVALIN	R/W	0h	Internal. Only to be used through TI provided API.
8	DBGCALLEG	R/W	0h	Internal. Only to be used through TI provided API.
7-6	DBGCALMQ	R/W	0h	Internal. Only to be used through TI provided API.
5-4	DBGCALMI	R/W	0h	Internal. Only to be used through TI provided API.
3	AUTOCAL	R/W	0h	Internal. Only to be used through TI provided API.
2-0	QUANTTHR	R/W	0h	Internal. Only to be used through TI provided API.

28.9.48 IFADCALDO Register (Offset = D4h) [Reset = 00000000h]

IFADCALDO is shown in Table 28-373.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-373. IFADCALDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	ATESTVSSANA	R/W	0h	Internal. Only to be used through TI provided API.
14	RESERVED	R	0h	Internal. Only to be used through TI provided API.
13-8	TRIMOUT	R/W	0h	Internal. Only to be used through TI provided API.
7	DUMMY	R/W	0h	Internal. Only to be used through TI provided API.
6	ATESTERRAMP	R/W	0h	Internal. Only to be used through TI provided API.
5	ATESTINPUTREF	R/W	0h	Internal. Only to be used through TI provided API.
4	ATESTOUT	R/W	0h	Internal. Only to be used through TI provided API.
3	ITEST	R/W	0h	Internal. Only to be used through TI provided API.
2	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
1	CLAMP	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.49 IFADCDLDO Register (Offset = D8h) [Reset = 00000000h]

IFADCDLDO is shown in Table 28-374.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-374. IFADCDLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	RESERVED	R	0h	Internal. Only to be used through TI provided API.
13-8	TRIMOUT	R/W	0h	Internal. Only to be used through TI provided API.
7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6	ATESTERRAMP	R/W	0h	Internal. Only to be used through TI provided API.
5	ATESTFB	R/W	0h	Internal. Only to be used through TI provided API.
4	ATESTOUT	R/W	0h	Internal. Only to be used through TI provided API.
3	ITEST	R/W	0h	Internal. Only to be used through TI provided API.
2	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
1	CLAMP	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.50 IFADCTST Register (Offset = DCh) [Reset = 00000000h]

IFADCTST is shown in Table 28-375.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-375. IFADCTST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	EXTCURR	R/W	0h	Internal. Only to be used through TI provided API.
6	QCALDBIQ	R/W	0h	Internal. Only to be used through TI provided API.
5	QCALDBC	R/W	0h	Internal. Only to be used through TI provided API.
4-0	SEL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.51 ATSTREFL Register (Offset = E0h) [Reset = 00000000h]

ATSTREFL is shown in Table 28-376.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-376. ATSTREFL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	MUXLSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.52 ATSTREFH Register (Offset = E4h) [Reset = 00000000h]

ATSTREFH is shown in Table 28-377.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-377. ATSTREFH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	VREFBPDIS	R/W	0h	Internal. Only to be used through TI provided API.
14-10	IREFTRIM	R/W	0h	Internal. Only to be used through TI provided API.
9	BIAS	R/W	0h	Internal. Only to be used through TI provided API.
8	OUTPUT1	R/W	0h	Internal. Only to be used through TI provided API.
7	OUTPUT2	R/W	0h	Internal. Only to be used through TI provided API.
6-0	MUXMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.53 DCO Register (Offset = E8h) [Reset = 00000000h]

DCO is shown in Table 28-378.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-378. DCO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-9	MTDCSPARE	R/W	0h	Internal. Only to be used through TI provided API.
8-7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6-3	TAILRESTRIM	R/W	0h	Internal. Only to be used through TI provided API.
2	RTRIMCAP	R/W	0h	Internal. Only to be used through TI provided API.
1	CNRCAP	R/W	0h	Internal. Only to be used through TI provided API.
0	CRSCAPCM	R/W	0h	Internal. Only to be used through TI provided API.

28.9.54 DIV Register (Offset = ECh) [Reset = 00000000h]

DIV is shown in Table 28-379.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-379. DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	PDET	R/W	0h	Internal. Only to be used through TI provided API.
14-12	NMIREFTRIM	R/W	0h	Internal. Only to be used through TI provided API.
11-9	PMIREFTRIM	R/W	0h	Internal. Only to be used through TI provided API.
8	TXBBOOST	R/W	0h	Internal. Only to be used through TI provided API.
7	S1GFRC	R/W	0h	Internal. Only to be used through TI provided API.
6-5	BUFGAIN	R/W	0h	Internal. Only to be used through TI provided API.
4	BIAS	R/W	0h	Internal. Only to be used through TI provided API.
3	OUT	R/W	0h	Internal. Only to be used through TI provided API.
2-0	RATIO	R/W	0h	Internal. Only to be used through TI provided API.

28.9.55 DIVLDO Register (Offset = F0h) [Reset = 00000000h]

DIVLDO is shown in Table 28-380.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-380. DIVLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	ITESTCTL	R/W	0h	Internal. Only to be used through TI provided API.
14-8	VOUTTRIM	R/W	0h	Internal. Only to be used through TI provided API.
7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6-4	TMUX	R/W	0h	Internal. Only to be used through TI provided API.
3	PDSEL	R/W	0h	Internal. Only to be used through TI provided API.
2	MODE	R/W	0h	Internal. Only to be used through TI provided API.
1	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.56 TDCLDO Register (Offset = F4h) [Reset = 00000000h]

TDCLDO is shown in Table 28-381.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-381. TDCLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	ITESTCTL	R/W	0h	Internal. Only to be used through TI provided API.
14-8	VOUTTRIM	R/W	0h	Internal. Only to be used through TI provided API.
7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6-4	TMUX	R/W	0h	Internal. Only to be used through TI provided API.
3	PDSEL	R/W	0h	Internal. Only to be used through TI provided API.
2	MODE	R/W	0h	Internal. Only to be used through TI provided API.
1	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.57 DCOLDO0 Register (Offset = F8h) [Reset = 00000000h]

DCOLDO0 is shown in Table 28-382.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-382. DCOLDO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	ITST	R/W	0h	Internal. Only to be used through TI provided API.
13-8	SECONDTRIM	R/W	0h	Internal. Only to be used through TI provided API.
7-4	FIRSTTRIM	R/W	0h	Internal. Only to be used through TI provided API.
3	PDN	R/W	0h	Internal. Only to be used through TI provided API.
2	BYPFIRST	R/W	0h	Internal. Only to be used through TI provided API.
1	BYPBOTH	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.58 DCOLDO1 Register (Offset = FCh) [Reset = 00000000h]

DCOLDO1 is shown in Table 28-383.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-383. DCOLDO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	REFSRC	R/W	0h	Internal. Only to be used through TI provided API.
9-8	DIVATST	R/W	0h	Internal. Only to be used through TI provided API.
7	PERFM	R/W	0h	Internal. Only to be used through TI provided API.
6	CHRGFILT	R/W	0h	Internal. Only to be used through TI provided API.
5-0	ATST	R/W	0h	Internal. Only to be used through TI provided API.

28.9.59 PRE0 Register (Offset = 100h) [Reset = 00000000h]

PRE0 is shown in Table 28-384.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-384. PRE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	SPARE14	R/W	0h	Internal. Only to be used through TI provided API.
13-8	PLLDIV1	R/W	0h	Internal. Only to be used through TI provided API.
7-6	SPARE6	R/W	0h	Internal. Only to be used through TI provided API.
5-0	PLLDIV0	R/W	0h	Internal. Only to be used through TI provided API.

28.9.60 PRE1 Register (Offset = 104h) [Reset = 00000000h]

PRE1 is shown in Table 28-385.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-385. PRE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	IIRBW	R/W	0h	Internal. Only to be used through TI provided API.
13	IIRORD	R/W	0h	Internal. Only to be used through TI provided API.
12-8	IIRDIV	R/W	0h	Internal. Only to be used through TI provided API.
7	RESERVED	R	0h	Reserved
6	CALHSDDC	R/W	0h	Internal. Only to be used through TI provided API.
5-0	HSDDC	R/W	0h	Internal. Only to be used through TI provided API.

28.9.61 PRE2 Register (Offset = 108h) [Reset = 00000000h]

PRE2 is shown in Table 28-386.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-386. PRE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	MIDCALDIVLSB	R/W	0h	Internal. Only to be used through TI provided API.
11-6	CRSCALDIV	R/W	0h	Internal. Only to be used through TI provided API.
5-0	FSMDIV	R/W	0h	Internal. Only to be used through TI provided API.

28.9.62 PRE3 Register (Offset = 10Ch) [Reset = 00000000h]

PRE3 is shown in Table 28-387.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-387. PRE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-5	FINECALDIV	R/W	0h	Internal. Only to be used through TI provided API.
4-0	MIDCALDIVMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.63 CAL0 Register (Offset = 110h) [Reset = 00000000h]

CAL0 is shown in Table 28-388.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-388. CAL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SPARE15	R/W	0h	Internal. Only to be used through TI provided API.
14-8	FCSTART	R/W	0h	Internal. Only to be used through TI provided API.
7	CRS	R/W	0h	Internal. Only to be used through TI provided API.
6	MID	R/W	0h	Internal. Only to be used through TI provided API.
5	KTDC	R/W	0h	Internal. Only to be used through TI provided API.
4	KDCO	R/W	0h	Internal. Only to be used through TI provided API.
3-2	TDCAVG	R/W	0h	Internal. Only to be used through TI provided API.
1-0	TDC_SPARE	R/W	0h	Internal. Only to be used through TI provided API.

28.9.64 CAL1 Register (Offset = 114h) [Reset = 00000000h]

CAL1 is shown in Table 28-389.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-389. CAL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SPARE15	R/W	0h	Internal. Only to be used through TI provided API.
14-8	FCTOP	R/W	0h	Internal. Only to be used through TI provided API.
7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6-0	FCBOT	R/W	0h	Internal. Only to be used through TI provided API.

28.9.65 CAL2 Register (Offset = 118h) [Reset = 00000000h]

CAL2 is shown in Table 28-390.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-390. CAL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	KTDCINV	R/W	0h	Internal. Only to be used through TI provided API.

28.9.66 CAL3 Register (Offset = 11Ch) [Reset = 00000000h]

CAL3 is shown in Table 28-391.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-391. CAL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DTXGAIN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.67 MISC0 Register (Offset = 120h) [Reset = 00000000h]

MISC0 is shown in Table 28-392.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-392. MISC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	TDCCALENHCTL	R/W	0h	Internal. Only to be used through TI provided API.
14	TDCCALENHCFG	R/W	0h	Internal. Only to be used through TI provided API.
13	PHCPT	R/W	0h	Internal. Only to be used through TI provided API.
12	TDCCALCORR	R/W	0h	Internal. Only to be used through TI provided API.
11	TDCMSBCORR	R/W	0h	Internal. Only to be used through TI provided API.
10	SDMDEM	R/W	0h	Internal. Only to be used through TI provided API.
9-8	DLYSDM	R/W	0h	Internal. Only to be used through TI provided API.
7	CKVDENFRC	R/W	0h	Internal. Only to be used through TI provided API.
6	DLYPHVALID	R/W	0h	Internal. Only to be used through TI provided API.
5-4	DLYCANCRS	R/W	0h	Internal. Only to be used through TI provided API.
3-2	DLYCANFINE	R/W	0h	Internal. Only to be used through TI provided API.
1-0	DLYADD	R/W	0h	Internal. Only to be used through TI provided API.

28.9.68 MISC1 Register (Offset = 124h) [Reset = 00000000h]

MISC1 is shown in Table 28-393.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-393. MISC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	FCDEMCLK	R/W	0h	Internal. Only to be used through TI provided API.
13-12	FCDEMUPD	R/W	0h	Internal. Only to be used through TI provided API.
11-6	TDCINL	R/W	0h	Internal. Only to be used through TI provided API.
5	TDCINLCTL	R/W	0h	Internal. Only to be used through TI provided API.
4	PHINIT	R/W	0h	Internal. Only to be used through TI provided API.
3	SDMOOVRCTL	R/W	0h	Internal. Only to be used through TI provided API.
2-0	SDMOOVR	R/W	0h	Internal. Only to be used through TI provided API.

28.9.69 LF0 Register (Offset = 128h) [Reset = 00000000h]

LF0 is shown in Table 28-394.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-394. LF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	KIPREC	R/W	0h	Internal. Only to be used through TI provided API.
11-0	KI	R/W	0h	Internal. Only to be used through TI provided API.

28.9.70 LF1 Register (Offset = 12Ch) [Reset = 00000000h]

LF1 is shown in Table 28-395.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-395. LF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-0	KP	R/W	0h	Internal. Only to be used through TI provided API.

28.9.71 PHEDISC Register (Offset = 130h) [Reset = 00000000h]

PHEDISC is shown in Table 28-396.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-396. PHEDISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-10	CNT	R/W	0h	Internal. Only to be used through TI provided API.
9-0	THR	R/W	0h	Internal. Only to be used through TI provided API.

28.9.72 PHINIT Register (Offset = 134h) [Reset = 00000000h]

PHINIT is shown in Table 28-397.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-397. PHINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	OFF	R/W	0h	Internal. Only to be used through TI provided API.

28.9.73 PLLMON0 Register (Offset = 138h) [Reset = 00000000h]

PLLMON0 is shown in Table 28-398.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-398. PLLMON0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-14	PHELOLCNT	R/W	0h	Internal. Only to be used through TI provided API.
13-8	PHELOLTHR	R/W	0h	Internal. Only to be used through TI provided API.
7	RESERVED	R	0h	Reserved
6-0	FCTHR	R/W	0h	Internal. Only to be used through TI provided API.

28.9.74 PLLMON1 Register (Offset = 13Ch) [Reset = 00000000h]

PLLMON1 is shown in Table 28-399.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-399. PLLMON1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-8	PHELOCKCNT	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PHELOCKTHR	R/W	0h	Internal. Only to be used through TI provided API.

28.9.75 MOD0 Register (Offset = 140h) [Reset = 00000000h]

MOD0 is shown in Table 28-400.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-400. MOD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-11	SCHEME	R/W	0h	Internal. Only to be used through TI provided API.
10-8	SYMSHP	R/W	0h	Internal. Only to be used through TI provided API.
7-6	CANPTHGAIN	R/W	0h	Internal. Only to be used through TI provided API.
5-4	SHPGAIN	R/W	0h	Internal. Only to be used through TI provided API.
3-2	INTPFACT	R/W	0h	Internal. Only to be used through TI provided API.
1-0	RESERVED	R	0h	Reserved

28.9.76 MOD1 Register (Offset = 144h) [Reset = 00000000h]

MOD1 is shown in Table 28-401.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-401. MOD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	FOFF	R/W	0h	Internal. Only to be used through TI provided API.

28.9.77 DTX0 Register (Offset = 148h) [Reset = 00000000h]

DTX0 is shown in Table 28-402.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-402. DTX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP1	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP0	R/W	0h	Internal. Only to be used through TI provided API.

28.9.78 DTX1 Register (Offset = 14Ch) [Reset = 00000000h]

DTX1 is shown in Table 28-403.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-403. DTX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP3	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP2	R/W	0h	Internal. Only to be used through TI provided API.

28.9.79 DTX2 Register (Offset = 150h) [Reset = 00000000h]

DTX2 is shown in Table 28-404.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-404. DTX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP5	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP4	R/W	0h	Internal. Only to be used through TI provided API.

28.9.80 DTX3 Register (Offset = 154h) [Reset = 00000000h]

DTX3 is shown in Table 28-405.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-405. DTX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP7	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP6	R/W	0h	Internal. Only to be used through TI provided API.

28.9.81 DTX4 Register (Offset = 158h) [Reset = 00000000h]

DTX4 is shown in Table 28-406.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-406. DTX4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP9	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP8	R/W	0h	Internal. Only to be used through TI provided API.

28.9.82 DTX5 Register (Offset = 15Ch) [Reset = 00000000h]

DTX5 is shown in Table 28-407.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-407. DTX5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP11	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP10	R/W	0h	Internal. Only to be used through TI provided API.

28.9.83 DTX6 Register (Offset = 160h) [Reset = 00000000h]

DTX6 is shown in Table 28-408.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-408. DTX6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP13	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP12	R/W	0h	Internal. Only to be used through TI provided API.

28.9.84 DTX7 Register (Offset = 164h) [Reset = 00000000h]

DTX7 is shown in Table 28-409.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-409. DTX7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP15	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP14	R/W	0h	Internal. Only to be used through TI provided API.

28.9.85 DTX8 Register (Offset = 168h) [Reset = 00000000h]

DTX8 is shown in Table 28-410.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-410. DTX8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP17	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP16	R/W	0h	Internal. Only to be used through TI provided API.

28.9.86 DTX9 Register (Offset = 16Ch) [Reset = 00000000h]

DTX9 is shown in Table 28-411.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-411. DTX9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP19	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP18	R/W	0h	Internal. Only to be used through TI provided API.

28.9.87 DTX10 Register (Offset = 170h) [Reset = 00000000h]

DTX10 is shown in Table 28-412.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-412. DTX10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP21	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP20	R/W	0h	Internal. Only to be used through TI provided API.

28.9.88 DTX11 Register (Offset = 174h) [Reset = 00000000h]

DTX11 is shown in Table 28-413.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-413. DTX11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	SHP23	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP22	R/W	0h	Internal. Only to be used through TI provided API.

28.9.89 PLLM0L Register (Offset = 178h) [Reset = 00000000h]

PLLM0L is shown in Table 28-414.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-414. PLLM0L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	VALLSB	R/W	0h	Internal. Only to be used through TI provided API.
1-0	SPARE0	R/W	0h	Internal. Only to be used through TI provided API.

28.9.90 PLLM0H Register (Offset = 17Ch) [Reset = 00000000h]

PLLM0H is shown in Table 28-415.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-415. PLLM0H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.91 PLLM1L Register (Offset = 180h) [Reset = 00000000h]

PLLM1L is shown in Table 28-416.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-416. PLLM1L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-2	VALLSB	R/W	0h	Internal. Only to be used through TI provided API.
1-0	SPARE0	R/W	0h	Internal. Only to be used through TI provided API.

28.9.92 PLLM1H Register (Offset = 184h) [Reset = 00000000h]

PLLM1H is shown in Table 28-417.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-417. PLLM1H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.93 CALMCRS Register (Offset = 188h) [Reset = 00000000h]

CALMCRS is shown in Table 28-418.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-418. CALMCRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.94 CALMMID Register (Offset = 18Ch) [Reset = 00000000h]

CALMMID is shown in Table 28-419.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-419. CALMMID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.95 REFDIV Register (Offset = 190h) [Reset = 00000000h]

REFDIV is shown in Table 28-420.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-420. REFDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LOAD	R/W	0h	Internal. Only to be used through TI provided API.

28.9.96 DLOCTL0 Register (Offset = 198h) [Reset = 00000000h]

DLOCTL0 is shown in Table 28-421.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-421. DLOCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	TDCSTOP	R/W	0h	Internal. Only to be used through TI provided API.
7	DTSTXTAL	R/W	0h	Internal. Only to be used through TI provided API.
6-4	LOOPUPD	R/W	0h	Internal. Only to be used through TI provided API.
3	PH3	R/W	0h	Internal. Only to be used through TI provided API.
2	PH2	R/W	0h	Internal. Only to be used through TI provided API.
1	LOOPMODE	R/W	0h	Internal. Only to be used through TI provided API.
0	RSTN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.97 DLOCTL1 Register (Offset = 1A0h) [Reset = 00000000h]

DLOCTL1 is shown in Table 28-422.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-422. DLOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	DCO	R/W	0h	Internal. Only to be used through TI provided API.
14-11	RESERVED	R	0h	Reserved
10	LFSYNCATGRSHFT	R/W	0h	Internal. Only to be used through TI provided API.
9	LFSYNCATPEAK	R/W	0h	Internal. Only to be used through TI provided API.
8	PHEADJ	R/W	0h	Internal. Only to be used through TI provided API.
7	FCDEM	R/W	0h	Internal. Only to be used through TI provided API.
6	DTSTCKVD	R/W	0h	Internal. Only to be used through TI provided API.
5	PHEDISC	R/W	0h	Internal. Only to be used through TI provided API.
4	PLLMON	R/W	0h	Internal. Only to be used through TI provided API.
3	IIR	R/W	0h	Internal. Only to be used through TI provided API.
2	MOD	R/W	0h	Internal. Only to be used through TI provided API.
1	MODINIT	R/W	0h	Internal. Only to be used through TI provided API.
0	MTDCRSTN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.98 DCOOVR0 Register (Offset = 1A8h) [Reset = 00000000h]

DCOOVR0 is shown in Table 28-423.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-423. DCOOVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	MIDCODE	R/W	0h	Internal. Only to be used through TI provided API.
7-4	CRSCODE	R/W	0h	Internal. Only to be used through TI provided API.
3	FINECTL	R/W	0h	Internal. Only to be used through TI provided API.
2	SDMICTL	R/W	0h	Internal. Only to be used through TI provided API.
1	MIDCTL	R/W	0h	Internal. Only to be used through TI provided API.
0	CRSCTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.99 DCOOVR1 Register (Offset = 1ACh) [Reset = 00000000h]

DCOOVR1 is shown in Table 28-424.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-424. DCOOVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-8	FINECODE	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SDMICODE	R/W	0h	Internal. Only to be used through TI provided API.

28.9.100 DTST Register (Offset = 1B0h) [Reset = 00000000h]

DTST is shown in Table 28-425.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-425. DTST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14-11	SPARE11	R/W	0h	Internal. Only to be used through TI provided API.
10-8	VARTGLDLY	R/W	0h	Internal. Only to be used through TI provided API.
7	REFTGLDLY	R/W	0h	Internal. Only to be used through TI provided API.
6	TRNSEQ	R/W	0h	Internal. Only to be used through TI provided API.
5	SPARE5	R/W	0h	Internal. Only to be used through TI provided API.
4-0	SIG	R/W	0h	Internal. Only to be used through TI provided API.

28.9.101 DLOEV Register (Offset = 1B4h) [Reset = 00000000h]

DLOEV is shown in Table 28-426.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-426. DLOEV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	LOCK	R	0h	Internal. Only to be used through TI provided API.
6	LOL	R	0h	Internal. Only to be used through TI provided API.
5	FCABVTHR	R	0h	Internal. Only to be used through TI provided API.
4	FCBLWTHR	R	0h	Internal. Only to be used through TI provided API.
3-0	STATE	R	0h	Internal. Only to be used through TI provided API.

28.9.102 DTSTRD Register (Offset = 1B8h) [Reset = 00000000h]

DTSTRD is shown in Table 28-427.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-427. DTSTRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	Internal. Only to be used through TI provided API.

28.9.103 FDCOSPANLSB Register (Offset = 1C0h) [Reset = 00000000h]

FDCOSPANLSB is shown in Table 28-428.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-428. FDCOSPANLSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.104 FDCOSPANMSB Register (Offset = 1C4h) [Reset = 00000000h]

FDCOSPANMSB is shown in Table 28-429.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-429. FDCOSPANMSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.105 TDCCAL Register (Offset = 1C8h) [Reset = 00000000h]

TDCCAL is shown in Table 28-430.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-430. TDCCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.106 TDCCALLOW Register (Offset = 1CCh) [Reset = 00000000h]

TDCCALLOW is shown in Table 28-431.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-431. TDCCALLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.107 TDCCALHIGH Register (Offset = 1D0h) [Reset = 00000000h]

TDCCALHIGH is shown in Table 28-432.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-432. TDCCALHIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.108 TDCODET Register (Offset = 1D4h) [Reset = 00000000h]

TDCODET is shown in Table 28-433.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-433. TDCODET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	FLAGS	R	0h	Internal. Only to be used through TI provided API.

28.9.109 CALRES Register (Offset = 1D8h) [Reset = 00000000h]

CALRES is shown in Table 28-434.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-434. CALRES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-4	MIDCODE	R	0h	Internal. Only to be used through TI provided API.
3-0	CRSCODE	R	0h	Internal. Only to be used through TI provided API.

28.9.110 GPI Register (Offset = 1DCh) [Reset = 00000000h]

GPI is shown in Table 28-435.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-435. GPI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	GPI7	R	0h	Internal. Only to be used through TI provided API.
6	GPI6	R	0h	Internal. Only to be used through TI provided API.
5	GPI5	R	0h	Internal. Only to be used through TI provided API.
4	GPI4	R	0h	Internal. Only to be used through TI provided API.
3	GPI3	R	0h	Internal. Only to be used through TI provided API.
2	GPI2	R	0h	Internal. Only to be used through TI provided API.
1	GPI1	R	0h	Internal. Only to be used through TI provided API.
0	GPI0	R	0h	Internal. Only to be used through TI provided API.

28.9.111 MATHACCELIN Register (Offset = 1E0h) [Reset = 00000000h]

MATHACCELIN is shown in Table 28-436.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-436. MATHACCELIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.112 LIN2LOGOUT Register (Offset = 1E4h) [Reset = 00000000h]

LIN2LOGOUT is shown in Table 28-437.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-437. LIN2LOGOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-0	LOGVAL	R	0h	Internal. Only to be used through TI provided API.

28.9.113 DIVBY3OUT Register (Offset = 1E8h) [Reset = 00000000h]

DIVBY3OUT is shown in Table 28-438.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-438. DIVBY3OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	DIV3	R	0h	Internal. Only to be used through TI provided API.

28.9.114 TIMCTL Register (Offset = 1ECh) [Reset = 00000000h]

TIMCTL is shown in Table 28-439.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-439. TIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	CPTSRC	R/W	0h	Internal. Only to be used through TI provided API.
7	CPTCTL	R/W	0h	Internal. Only to be used through TI provided API.
6-5	CNTRSRC	R/W	0h	Internal. Only to be used through TI provided API.
4	CNTRCLR	R/W	0h	Internal. Only to be used through TI provided API.
3	CNTRCTL	R/W	0h	Internal. Only to be used through TI provided API.
2-1	TIMSRC	R/W	0h	Internal. Only to be used through TI provided API.
0	TIMCTL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.115 TIMINC Register (Offset = 1F0h) [Reset = 00000000h]

TIMINC is shown in Table 28-440.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-440. TIMINC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.116 TIMPER Register (Offset = 1F4h) [Reset = 00000000h]

TIMPER is shown in Table 28-441.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-441. TIMPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.117 TIMCNT Register (Offset = 1F8h) [Reset = 00000000h]

TIMCNT is shown in Table 28-442.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-442. TIMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.118 TIMCAPT Register (Offset = 1FCh) [Reset = 00000000h]

TIMCAPT is shown in Table 28-443.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-443. TIMCAPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALUE	R	0h	Internal. Only to be used through TI provided API.

28.9.119 TRCCTRL Register (Offset = 200h) [Reset = 00000000h]

TRCCTRL is shown in Table 28-444.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-444. TRCCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SEND	W	0h	Internal. Only to be used through TI provided API.

28.9.120 TRCSTAT Register (Offset = 204h) [Reset = 00000000h]

TRCSTAT is shown in Table 28-445.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-445. TRCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	BUSY	R	0h	Internal. Only to be used through TI provided API.

28.9.121 TRCCMD Register (Offset = 208h) [Reset = 00000000h]

TRCCMD is shown in Table 28-446.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-446. TRCCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-8	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.

28.9.122 TRCPAR0 Register (Offset = 20Ch) [Reset = 00000000h]

TRCPAR0 is shown in Table 28-447.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-447. TRCPAR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.123 TRCPAR1 Register (Offset = 210h) [Reset = 00000000h]

TRCPAR1 is shown in Table 28-448.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-448. TRCPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.124 GPOCTL Register (Offset = 214h) [Reset = 00000000h]

GPOCTL is shown in Table 28-449.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-449. GPOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SEL7	R/W	0h	Internal. Only to be used through TI provided API.
14	SEL6	R/W	0h	Internal. Only to be used through TI provided API.
13	SEL5	R/W	0h	Internal. Only to be used through TI provided API.
12	SEL4	R/W	0h	Internal. Only to be used through TI provided API.
11	SEL3	R/W	0h	Internal. Only to be used through TI provided API.
10	SEL2	R/W	0h	Internal. Only to be used through TI provided API.
9	SEL1	R/W	0h	Internal. Only to be used through TI provided API.
8	SEL0	R/W	0h	Internal. Only to be used through TI provided API.
7	GPO7	R/W	0h	Internal. Only to be used through TI provided API.
6	GPO6	R/W	0h	Internal. Only to be used through TI provided API.
5	GPO5	R/W	0h	Internal. Only to be used through TI provided API.
4	GPO4	R/W	0h	Internal. Only to be used through TI provided API.
3	GPO3	R/W	0h	Internal. Only to be used through TI provided API.
2	GPO2	R/W	0h	Internal. Only to be used through TI provided API.
1	GPO1	R/W	0h	Internal. Only to be used through TI provided API.
0	GPO0	R/W	0h	Internal. Only to be used through TI provided API.

28.9.125 ANAISOCTL Register (Offset = 218h) [Reset = 00000000h]

ANAISOCTL is shown in Table 28-450.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-450. ANAISOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	ADCDIGRSTN	R/W	0h	Internal. Only to be used through TI provided API.
3	IFADC2SVTISO	R/W	0h	Internal. Only to be used through TI provided API.
2	DIV2IFADCISO	R/W	0h	Internal. Only to be used through TI provided API.
1	MTDC2SVTISO	R/W	0h	Internal. Only to be used through TI provided API.
0	DIV2MTDCISO	R/W	0h	Internal. Only to be used through TI provided API.

28.9.126 DIVCTL Register (Offset = 21Ch) [Reset = 00000000h]

DIVCTL is shown in Table 28-451.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-451. DIVCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	DIV2PH180	R/W	0h	Internal. Only to be used through TI provided API.
14	DIV2PH0	R/W	0h	Internal. Only to be used through TI provided API.
13	DIV2PH270	R/W	0h	Internal. Only to be used through TI provided API.
12	DIV2PH90	R/W	0h	Internal. Only to be used through TI provided API.
11	SPARE11	R/W	0h	Internal. Only to be used through TI provided API.
10	S1G20DBMMUX	R/W	0h	Internal. Only to be used through TI provided API.
9	ADCDIV	R/W	0h	Internal. Only to be used through TI provided API.
8	ENSYNTH	R/W	0h	Internal. Only to be used through TI provided API.
7	TXPH18020DBMDIV	R/W	0h	Internal. Only to be used through TI provided API.
6	TXPH020DBMDIV	R/W	0h	Internal. Only to be used through TI provided API.
5	TXPH180DIV	R/W	0h	Internal. Only to be used through TI provided API.
4	TXPH0DIV	R/W	0h	Internal. Only to be used through TI provided API.
3	RXPH90DIV	R/W	0h	Internal. Only to be used through TI provided API.
2	RXPH0DIV	R/W	0h	Internal. Only to be used through TI provided API.
1	Spare1	R/W	0h	Internal. Only to be used through TI provided API.
0	EN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.127 RXCTRL Register (Offset = 220h) [Reset = 00000000h]

RXCTRL is shown in Table 28-452.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-452. RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
11-9	ATTN	R/W	0h	Internal. Only to be used through TI provided API.
8-4	IFAMPGC	R/W	0h	Internal. Only to be used through TI provided API.
3-0	LNAGAIN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.128 MAGNACC0 Register (Offset = 224h) [Reset = 00000000h]

MAGNACC0 is shown in Table 28-453.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-453. MAGNACC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.129 MAGNACC1 Register (Offset = 228h) [Reset = 00000000h]

MAGNACC1 is shown in Table 28-454.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-454. MAGNACC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.9.130 RSSI Register (Offset = 22Ch) [Reset = 00000000h]

RSSI is shown in Table 28-455.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-455. RSSI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.131 RSSIMAX Register (Offset = 230h) [Reset = 00000000h]

RSSIMAX is shown in Table 28-456.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-456. RSSIMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.9.132 RFGAIN Register (Offset = 234h) [Reset = 00000000h]

RFGAIN is shown in Table 28-457.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-457. RFGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DBGAIN	R/W	0h	Internal. Only to be used through TI provided API.

28.9.133 IFADCSTAT Register (Offset = 238h) [Reset = 00000000h]

IFADCSTAT is shown in Table 28-458.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-458. IFADCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Internal. Only to be used through TI provided API.
6-2	QUANTCALVAL	R	0h	Internal. Only to be used through TI provided API.
1	QUANTCALDONE	R	0h	Internal. Only to be used through TI provided API.
0	RESERVED	R	0h	Internal. Only to be used through TI provided API.

28.9.134 DIVSTA Register (Offset = 23Ch) [Reset = 00000000h]

DIVSTA is shown in Table 28-459.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-459. DIVSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STAT	R	0h	Internal. Only to be used through TI provided API.

28.9.135 DIVIDENDL Register (Offset = 240h) [Reset = 00000000h]

DIVIDENDL is shown in Table 28-460.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-460. DIVIDENDL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	W	0h	Internal. Only to be used through TI provided API.

28.9.136 DIVIDENDH Register (Offset = 244h) [Reset = 00000000h]

DIVIDENDH is shown in Table 28-461.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-461. DIVIDENDH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	W	0h	Internal. Only to be used through TI provided API.

28.9.137 DIVISORL Register (Offset = 248h) [Reset = 00000000h]

DIVISORL is shown in Table 28-462.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-462. DIVISORL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.138 DIVISORH Register (Offset = 24Ch) [Reset = 00000000h]

DIVISORH is shown in Table 28-463.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-463. DIVISORH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R/W	0h	Internal. Only to be used through TI provided API.

28.9.139 QUOTIENTL Register (Offset = 250h) [Reset = 00000000h]

QUOTIENTL is shown in Table 28-464.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-464. QUOTIENTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R	0h	Internal. Only to be used through TI provided API.

28.9.140 QUOTIENTH Register (Offset = 254h) [Reset = 00000000h]

QUOTIENTH is shown in Table 28-465.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-465. QUOTIENTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R	0h	Internal. Only to be used through TI provided API.

28.9.141 PRODUCTL Register (Offset = 258h) [Reset = 00000000h]

PRODUCTL is shown in Table 28-466.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-466. PRODUCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALLSB	R	0h	Internal. Only to be used through TI provided API.

28.9.142 PRODUCTH Register (Offset = 25Ch) [Reset = 00000000h]

PRODUCTH is shown in Table 28-467.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-467. PRODUCTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VALMSB	R	0h	Internal. Only to be used through TI provided API.

28.9.143 MULTSTA Register (Offset = 260h) [Reset = 00000000h]

MULTSTA is shown in Table 28-468.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-468. MULTSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STAT	R	0h	Internal. Only to be used through TI provided API.

28.9.144 MULTCFG Register (Offset = 268h) [Reset = 00000000h]

MULTCFG is shown in Table 28-469.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-469. MULTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MODE	R/W	0h	Internal. Only to be used through TI provided API.

28.9.145 PA1 Register (Offset = 26Ch) [Reset = 00000000h]

PA1 is shown in Table 28-470.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-470. PA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-13	SPARE0	R/W	0h	Internal. Only to be used through TI provided API.
12-11	MODE	R/W	0h	Internal. Only to be used through TI provided API.
10-8	GAIN	R/W	0h	Internal. Only to be used through TI provided API.
7-2	IB	R/W	0h	Internal. Only to be used through TI provided API.
1-0	IBBOOST	R/W	0h	Internal. Only to be used through TI provided API.

28.9.146 PA2 Register (Offset = 270h) [Reset = 00000000h]

PA2 is shown in Table 28-471.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-471. PA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-5	SPARE5	R/W	0h	Internal. Only to be used through TI provided API.
4-0	TRIM	R/W	0h	Internal. Only to be used through TI provided API.

28.10 LRFDRFE32 Registers

Table 28-472 lists the memory-mapped registers for the LRFDRFE32 registers. All register offset addresses not listed in Table 28-472 should be considered as reserved locations and the register contents should not be modified.

Table 28-472. LRFDRFE32 Registers

Offset	Acronym	Register Name	Section
0h	FWSRC_ENABLE	Internal. Only to be used through TI provided API.	Section 28.10.1
4h	PDREQ_INIT	Internal. Only to be used through TI provided API.	Section 28.10.2
8h	EVT1_EVT0	Internal. Only to be used through TI provided API.	Section 28.10.3
Ch	EVTMSK1_EVTMSK0	Internal. Only to be used through TI provided API.	Section 28.10.4
10h	EVTCLR1_EVTCLR0	Internal. Only to be used through TI provided API.	Section 28.10.5
14h	HFXTSTAT	Internal. Only to be used through TI provided API.	Section 28.10.6
18h	RFSTATE	Internal. Only to be used through TI provided API.	Section 28.10.7
1Ch	SPIN	Internal. Only to be used through TI provided API.	Section 28.10.8
24h	CMDPAR0_API	Internal. Only to be used through TI provided API.	Section 28.10.9
28h	MSGBOX_CMDPAR1	Internal. Only to be used through TI provided API.	Section 28.10.10
2Ch	MCEDATIN0_MCEDATOUT0	Internal. Only to be used through TI provided API.	Section 28.10.11
30h	MCECMDIN_MCECMDOUT	Internal. Only to be used through TI provided API.	Section 28.10.12
34h	PBEDATOUT0_PBEDATOUT1	Internal. Only to be used through TI provided API.	Section 28.10.13
38h	PBECMDOUT_PBEDATIN0	Internal. Only to be used through TI provided API.	Section 28.10.14
3Ch	STRB_PBECMDIN	Internal. Only to be used through TI provided API.	Section 28.10.15
40h	MAGNTHRCFG	Internal. Only to be used through TI provided API.	Section 28.10.16
44h	RSSIOFFSET_MAGNTHR	Internal. Only to be used through TI provided API.	Section 28.10.17
48h	MAGNCTL0_GAINCTL	Internal. Only to be used through TI provided API.	Section 28.10.18
4Ch	SPARE0_MAGNCTL1	Internal. Only to be used through TI provided API.	Section 28.10.19
50h	SPARE2_SPARE1	Internal. Only to be used through TI provided API.	Section 28.10.20
54h	SPARE4_SPARE3	Internal. Only to be used through TI provided API.	Section 28.10.21
58h	LNA_SPARE5	Internal. Only to be used through TI provided API.	Section 28.10.22
5Ch	PA0_IFAMPRFLDO	Internal. Only to be used through TI provided API.	Section 28.10.23
60h	IFADC0_ULNA	Internal. Only to be used through TI provided API.	Section 28.10.24
64h	IFADCLF_IFADC1	Internal. Only to be used through TI provided API.	Section 28.10.25
68h	IFADCALDO_IFADCQUANT	Internal. Only to be used through TI provided API.	Section 28.10.26
6Ch	IFADCTST_IFADCDLDO	Internal. Only to be used through TI provided API.	Section 28.10.27
70h	ATSTREF	Internal. Only to be used through TI provided API.	Section 28.10.28
74h	DIV_DCO	Internal. Only to be used through TI provided API.	Section 28.10.29
78h	TDCLDO_DIVLDO	Internal. Only to be used through TI provided API.	Section 28.10.30
7Ch	DCOLDO1_DCOLDO0	Internal. Only to be used through TI provided API.	Section 28.10.31
80h	PRE1_PRE0	Internal. Only to be used through TI provided API.	Section 28.10.32
84h	PRE3_PRE2	Internal. Only to be used through TI provided API.	Section 28.10.33
88h	CAL1_CAL0	Internal. Only to be used through TI provided API.	Section 28.10.34
8Ch	CAL3_CAL2	Internal. Only to be used through TI provided API.	Section 28.10.35
90h	MISC1_MISC0	Internal. Only to be used through TI provided API.	Section 28.10.36
94h	LF1_LF0	Internal. Only to be used through TI provided API.	Section 28.10.37
98h	PHINIT_PHEDISC	Internal. Only to be used through TI provided API.	Section 28.10.38
9Ch	PLLMON1_PLLMON0	Internal. Only to be used through TI provided API.	Section 28.10.39
A0h	MOD1_MOD0	Internal. Only to be used through TI provided API.	Section 28.10.40

Table 28-472. LRFDRFE32 Registers (continued)

Offset	Acronym	Register Name	Section
A4h	DTX1_DTX0	Internal. Only to be used through TI provided API.	Section 28.10.41
A8h	DTX3_DTX2	Internal. Only to be used through TI provided API.	Section 28.10.42
ACh	DTX5_DTX4	Internal. Only to be used through TI provided API.	Section 28.10.43
B0h	DTX7_DTX6	Internal. Only to be used through TI provided API.	Section 28.10.44
B4h	DTX9_DTX8	Internal. Only to be used through TI provided API.	Section 28.10.45
B8h	DTX11_DTX10	Internal. Only to be used through TI provided API.	Section 28.10.46
BCh	PLLM0	Internal. Only to be used through TI provided API.	Section 28.10.47
C0h	PLLM1	Internal. Only to be used through TI provided API.	Section 28.10.48
C4h	CALMMID_CALMCRS	Internal. Only to be used through TI provided API.	Section 28.10.49
C8h	REFDIV	Internal. Only to be used through TI provided API.	Section 28.10.50
CCh	DLOCTL0	Internal. Only to be used through TI provided API.	Section 28.10.51
D0h	DLOCTL1	Internal. Only to be used through TI provided API.	Section 28.10.52
D4h	DCOOVR1_DCOOVR0	Internal. Only to be used through TI provided API.	Section 28.10.53
D8h	DLOEV_DTST	Internal. Only to be used through TI provided API.	Section 28.10.54
DCh	DTSTRD	Internal. Only to be used through TI provided API.	Section 28.10.55
E0h	FDCOSPANMSB_FDCOSPANLSB	Internal. Only to be used through TI provided API.	Section 28.10.56
E4h	TDCCALLOW_TDCCAL	Internal. Only to be used through TI provided API.	Section 28.10.57
E8h	TDCODET_TDCCALHIGH	Internal. Only to be used through TI provided API.	Section 28.10.58
ECh	GPI_CALRES	Internal. Only to be used through TI provided API.	Section 28.10.59
F0h	LIN2LOGOUT_MATHACCELIN	Internal. Only to be used through TI provided API.	Section 28.10.60
F4h	TIMCTL_DIVBY3OUT	Internal. Only to be used through TI provided API.	Section 28.10.61
F8h	TIMPER_TIMINC	Internal. Only to be used through TI provided API.	Section 28.10.62
FCh	TIMCAPT_TIMCNT	Internal. Only to be used through TI provided API.	Section 28.10.63
100h	TRCSTAT_TRCCTRL	Internal. Only to be used through TI provided API.	Section 28.10.64
104h	TRCPAR0_TRCCMD	Internal. Only to be used through TI provided API.	Section 28.10.65
108h	GPOCTL_TRCPAR1	Internal. Only to be used through TI provided API.	Section 28.10.66
10Ch	DIVCTL_ANAISOCTL	Internal. Only to be used through TI provided API.	Section 28.10.67
110h	MAGNACC0_RXCTRL	Internal. Only to be used through TI provided API.	Section 28.10.68
114h	RSSI_MAGNACC1	Internal. Only to be used through TI provided API.	Section 28.10.69
118h	RFGAIN_RSSIMAX	Internal. Only to be used through TI provided API.	Section 28.10.70
11Ch	DIVSTA_IFADCSTAT	Internal. Only to be used through TI provided API.	Section 28.10.71
120h	DIVIDEND	Internal. Only to be used through TI provided API.	Section 28.10.72
124h	DIVISOR	Internal. Only to be used through TI provided API.	Section 28.10.73
128h	QUOTIENT	Internal. Only to be used through TI provided API.	Section 28.10.74
12Ch	PRODUCT	Internal. Only to be used through TI provided API.	Section 28.10.75
130h	MULTSTA	Internal. Only to be used through TI provided API.	Section 28.10.76
134h	PA1_MULTCFG	Internal. Only to be used through TI provided API.	Section 28.10.77
138h	PA2	Internal. Only to be used through TI provided API.	Section 28.10.78

Complex bit access types are encoded to fit into small table cells. Table 28-473 shows the codes that are used for access types in this section.

Table 28-473. LRFDRFE32 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 28-473. LRFDRFE32 Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.10.1 FWSRC_ENABLE Register (Offset = 0h) [Reset = 00000000h]

FWSRC_ENABLE is shown in Table 28-474.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-474. FWSRC_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	DATARAM	R/W	0h	Internal. Only to be used through TI provided API.
17	FWRAM	R/W	0h	Internal. Only to be used through TI provided API.
16	BANK	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3	ACC1	R/W	0h	Internal. Only to be used through TI provided API.
2	ACC0	R/W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	R/W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	R/W	0h	Internal. Only to be used through TI provided API.

28.10.2 PDREQ_INIT Register (Offset = 4h) [Reset = 00000000h]

PDREQ_INIT is shown in Table 28-475.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-475. PDREQ_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	TOPSMPDREQ	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3	ACC1	W	0h	Internal. Only to be used through TI provided API.
2	ACC0	W	0h	Internal. Only to be used through TI provided API.
1	LOCTIM	W	0h	Internal. Only to be used through TI provided API.
0	TOPSM	W	0h	Internal. Only to be used through TI provided API.

28.10.3 EVT1_EVT0 Register (Offset = 8h) [Reset = 00000000h]

EVT1_EVT0 is shown in Table 28-476.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-476. EVT1_EVT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	PREREFCLK	R	0h	Internal. Only to be used through TI provided API.
28	REFCLK	R	0h	Internal. Only to be used through TI provided API.
27	FBLWTHR	R	0h	Internal. Only to be used through TI provided API.
26	FABVTHR	R	0h	Internal. Only to be used through TI provided API.
25	LOCK	R	0h	Internal. Only to be used through TI provided API.
24	LOL	R	0h	Internal. Only to be used through TI provided API.
23	GPI7	R	0h	Internal. Only to be used through TI provided API.
22	GPI6	R	0h	Internal. Only to be used through TI provided API.
21	GPI5	R	0h	Internal. Only to be used through TI provided API.
20	GPI4	R	0h	Internal. Only to be used through TI provided API.
19	GPI3	R	0h	Internal. Only to be used through TI provided API.
18	GPI2	R	0h	Internal. Only to be used through TI provided API.
17	GPI1	R	0h	Internal. Only to be used through TI provided API.
16	GPI0	R	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14	MAGNTHR	R	0h	Internal. Only to be used through TI provided API.
13	S2RSTOP	R	0h	Internal. Only to be used through TI provided API.
12	SYSTCMP2	R	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP1	R	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP0	R	0h	Internal. Only to be used through TI provided API.
9	PBERFEDAT	R	0h	Internal. Only to be used through TI provided API.
8	MDMRFEDAT	R	0h	Internal. Only to be used through TI provided API.
7	DLO	R	0h	Internal. Only to be used through TI provided API.
6	PBECMD	R	0h	Internal. Only to be used through TI provided API.
5	COUNTER	R	0h	Internal. Only to be used through TI provided API.
4	MDMCMD	R	0h	Internal. Only to be used through TI provided API.
3	ACC1	R	0h	Internal. Only to be used through TI provided API.
2	ACC0	R	0h	Internal. Only to be used through TI provided API.
1	TIMER	R	0h	Internal. Only to be used through TI provided API.
0	RFEAPI	R	0h	Internal. Only to be used through TI provided API.

28.10.4 EVTMSK1_EVTMSK0 Register (Offset = Ch) [Reset = 00000000h]

EVTMSK1_EVTMSK0 is shown in Table 28-477.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-477. EVTMSK1_EVTMSK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	PREREFCLK	R/W	0h	Internal. Only to be used through TI provided API.
28	REFCLK	R/W	0h	Internal. Only to be used through TI provided API.
27	FBLWTHR	R/W	0h	Internal. Only to be used through TI provided API.
26	FABVTHR	R/W	0h	Internal. Only to be used through TI provided API.
25	LOCK	R/W	0h	Internal. Only to be used through TI provided API.
24	LOL	R/W	0h	Internal. Only to be used through TI provided API.
23	GPI7	R/W	0h	Internal. Only to be used through TI provided API.
22	GPI6	R/W	0h	Internal. Only to be used through TI provided API.
21	GPI5	R/W	0h	Internal. Only to be used through TI provided API.
20	GPI4	R/W	0h	Internal. Only to be used through TI provided API.
19	GPI3	R/W	0h	Internal. Only to be used through TI provided API.
18	GPI2	R/W	0h	Internal. Only to be used through TI provided API.
17	GPI1	R/W	0h	Internal. Only to be used through TI provided API.
16	GPI0	R/W	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14	MAGNTHR	R/W	0h	Internal. Only to be used through TI provided API.
13	S2RSTOP	R/W	0h	Internal. Only to be used through TI provided API.
12	SYSTCMP2	R/W	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP1	R/W	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP0	R/W	0h	Internal. Only to be used through TI provided API.
9	PBERFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
8	MDMRFEDAT	R/W	0h	Internal. Only to be used through TI provided API.
7	DLO	R/W	0h	Internal. Only to be used through TI provided API.
6	PBECMD	R/W	0h	Internal. Only to be used through TI provided API.
5	COUNTER	R/W	0h	Internal. Only to be used through TI provided API.
4	MDMCMD	R/W	0h	Internal. Only to be used through TI provided API.
3	ACC1	R/W	0h	Internal. Only to be used through TI provided API.
2	ACC0	R/W	0h	Internal. Only to be used through TI provided API.
1	TIMER	R/W	0h	Internal. Only to be used through TI provided API.
0	RFEAPI	R/W	0h	Internal. Only to be used through TI provided API.

28.10.5 EVTCLR1_EVTCLR0 Register (Offset = 10h) [Reset = 00000000h]

EVTCLR1_EVTCLR0 is shown in Table 28-478.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-478. EVTCLR1_EVTCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	PREREFCLK	W	0h	Internal. Only to be used through TI provided API.
28	REFCLK	W	0h	Internal. Only to be used through TI provided API.
27	FBLWTHR	W	0h	Internal. Only to be used through TI provided API.
26	FABVTHR	W	0h	Internal. Only to be used through TI provided API.
25	LOCK	W	0h	Internal. Only to be used through TI provided API.
24	LOL	W	0h	Internal. Only to be used through TI provided API.
23	GPI7	W	0h	Internal. Only to be used through TI provided API.
22	GPI6	W	0h	Internal. Only to be used through TI provided API.
21	GPI5	W	0h	Internal. Only to be used through TI provided API.
20	GPI4	W	0h	Internal. Only to be used through TI provided API.
19	GPI3	W	0h	Internal. Only to be used through TI provided API.
18	GPI2	W	0h	Internal. Only to be used through TI provided API.
17	GPI1	W	0h	Internal. Only to be used through TI provided API.
16	GPI0	W	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14	MAGNTHR	W	0h	Internal. Only to be used through TI provided API.
13	S2RSTOP	W	0h	Internal. Only to be used through TI provided API.
12	SYSTCMP2	W	0h	Internal. Only to be used through TI provided API.
11	SYSTCMP1	W	0h	Internal. Only to be used through TI provided API.
10	SYSTCMP0	W	0h	Internal. Only to be used through TI provided API.
9	PBERFEDAT	W	0h	Internal. Only to be used through TI provided API.
8	MDMRFEDAT	W	0h	Internal. Only to be used through TI provided API.
7	DLO	W	0h	Internal. Only to be used through TI provided API.
6	PBECMD	W	0h	Internal. Only to be used through TI provided API.
5	COUNTER	W	0h	Internal. Only to be used through TI provided API.
4	MDMCMD	W	0h	Internal. Only to be used through TI provided API.
3	ACC1	W	0h	Internal. Only to be used through TI provided API.
2	ACC0	W	0h	Internal. Only to be used through TI provided API.
1	TIMER	W	0h	Internal. Only to be used through TI provided API.
0	RFEAPI	W	0h	Internal. Only to be used through TI provided API.

28.10.6 HFXTSTAT Register (Offset = 14h) [Reset = 00000000h]

HFXTSTAT is shown in Table 28-479.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-479. HFXTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STAT	R	0h	Internal. Only to be used through TI provided API.

28.10.7 RFSTATE Register (Offset = 18h) [Reset = 00000000h]

RFSTATE is shown in Table 28-480.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-480. RFSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.8 SPIN Register (Offset = 1Ch) [Reset = 00000000h]

SPIN is shown in Table 28-481.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-481. SPIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	OPT	R	0h	Internal. Only to be used through TI provided API.

28.10.9 CMDPAR0_API Register (Offset = 24h) [Reset = 00000000h]

CMDPAR0_API is shown in Table 28-482.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-482. CMDPAR0_API Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-4	PROTOCOLID	R	0h	Internal. Only to be used through TI provided API.
3-0	RFECMD	R	0h	Internal. Only to be used through TI provided API.

28.10.10 MSGBOX_CMDPAR1 Register (Offset = 28h) [Reset = 00000000h]

MSGBOX_CMDPAR1 is shown in Table 28-483.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-483. MSGBOX_CMDPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MSGBOX_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CMDPAR1_VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.11 MCEDATIN0_MCEDATOUT0 Register (Offset = 2Ch) [Reset = 00000000h]

MCEDATIN0_MCEDATOUT0 is shown in Table 28-484.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-484. MCEDATIN0_MCEDATOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MCEDATIN0_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	MCEDATOUT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.12 MCECMDIN_MCECMDOUT Register (Offset = 30h) [Reset = 00000000h]

MCECMDIN_MCECMDOUT is shown in Table 28-485.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-485. MCECMDIN_MCECMDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	MCECMDIN_VAL	R	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	MCECMDOUT_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.13 PBEDATOUT0_PBEDATOUT1 Register (Offset = 34h) [Reset = 00000000h]

PBEDATOUT0_PBEDATOUT1 is shown in Table 28-486.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-486. PBEDATOUT0_PBEDATOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PBEDATOUT0_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PBEDATOUT1_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.14 PBECMDOUT_PBEDATIN0 Register (Offset = 38h) [Reset = 00000000h]

PBECMDOUT_PBEDATIN0 is shown in Table 28-487.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-487. PBECMDOUT_PBEDATIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	PBECMDOUT_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PBEDATIN0_VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.15 STRB_PBECMDIN Register (Offset = 3Ch) [Reset = 00000000h]

STRB_PBECMDIN is shown in Table 28-488.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-488. STRB_PBECMDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	S2RTRG	W	0h	Internal. Only to be used through TI provided API.
22	DMATRG	W	0h	Internal. Only to be used through TI provided API.
21	SYSTCPT2	W	0h	Internal. Only to be used through TI provided API.
20	SYSTCPT1	W	0h	Internal. Only to be used through TI provided API.
19	SYSTCPT0	W	0h	Internal. Only to be used through TI provided API.
18	EVT1	W	0h	Internal. Only to be used through TI provided API.
17	EVT0	W	0h	Internal. Only to be used through TI provided API.
16	CMDDONE	W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.16 MAGNTHRCFG Register (Offset = 40h) [Reset = 00000000h]

MAGNTHRCFG is shown in Table 28-489.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-489. MAGNTHRCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	SEL	R/W	0h	Internal. Only to be used through TI provided API.
16	CTL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	RESERVED	R	0h	Reserved

28.10.17 RSSIOFFSET_MAGNTHR Register (Offset = 44h) [Reset = 00000000h]

RSSIOFFSET_MAGNTHR is shown in Table 28-490.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-490. RSSIOFFSET_MAGNTHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	RSSIOFFSET_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	MAGNTHR_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.18 MAGNCTL0_GAINCTL Register (Offset = 48h) [Reset = 00000000h]

MAGNCTL0_GAINCTL is shown in Table 28-491.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-491. MAGNCTL0_GAINCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	PERMODE	R/W	0h	Internal. Only to be used through TI provided API.
27-24	SCL	R/W	0h	Internal. Only to be used through TI provided API.
23-16	PER	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-2	BDE2DVGA	R/W	0h	Internal. Only to be used through TI provided API.
1-0	BDE1DVGA	R/W	0h	Internal. Only to be used through TI provided API.

28.10.19 SPARE0_MAGNCTL1 Register (Offset = 4Ch) [Reset = 00000000h]

SPARE0_MAGNCTL1 is shown in Table 28-492.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-492. SPARE0_MAGNCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12	PERMODE	R/W	0h	Internal. Only to be used through TI provided API.
11-8	SCL	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PER	R/W	0h	Internal. Only to be used through TI provided API.

28.10.20 SPARE2_SPARE1 Register (Offset = 50h) [Reset = 00000000h]

SPARE2_SPARE1 is shown in Table 28-493.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-493. SPARE2_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SPARE2_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	SPARE1_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.21 SPARE4_SPARE3 Register (Offset = 54h) [Reset = 00000000h]

SPARE4_SPARE3 is shown in Table 28-494.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-494. SPARE4_SPARE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SPARE4_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	SPARE3_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.22 LNA_SPARE5 Register (Offset = 58h) [Reset = 00000000h]

LNA_SPARE5 is shown in Table 28-495.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-495. LNA_SPARE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
28	PA20DBMATSTSEL	R/W	0h	Internal. Only to be used through TI provided API.
27	PA20DBMATST	R/W	0h	Internal. Only to be used through TI provided API.
26	MIXATST	R/W	0h	Internal. Only to be used through TI provided API.
25	LDOITST	R/W	0h	Internal. Only to be used through TI provided API.
24	LDOATST	R/W	0h	Internal. Only to be used through TI provided API.
23-20	TRIM	R/W	0h	Internal. Only to be used through TI provided API.
19	MIXCAP	R/W	0h	Internal. Only to be used through TI provided API.
18-17	IB	R/W	0h	Internal. Only to be used through TI provided API.
16	EN	R/W	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.23 PA0_IFAMPRFLDO Register (Offset = 5Ch) [Reset = 00000000h]

PA0_IFAMPRFLDO is shown in Table 28-496.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-496. PA0_IFAMPRFLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PA0_SPARE14	R/W	0h	Internal. Only to be used through TI provided API.
29	PA0_BIASSEL	R/W	0h	Internal. Only to be used through TI provided API.
28	PA0_PA20DBMESDCTL	R/W	0h	Internal. Only to be used through TI provided API.
27-25	PA0_VCADJSCND	R/W	0h	Internal. Only to be used through TI provided API.
24-22	PA0_VCADJFRST	R/W	0h	Internal. Only to be used through TI provided API.
21-20	PA0_RC	R/W	0h	Internal. Only to be used through TI provided API.
19-18	PA0_SPARE2	R/W	0h	Internal. Only to be used through TI provided API.
17	PA0_RAMP	R/W	0h	Internal. Only to be used through TI provided API.
16	PA0_EN	R/W	0h	Internal. Only to be used through TI provided API.
15-9	IFAMPRFLDO_TRIM	R/W	0h	Internal. Only to be used through TI provided API.
8	IFAMPRFLDO_EN	R/W	0h	Internal. Only to be used through TI provided API.
7-4	IFAMPRFLDO_AAFCAP	R/W	0h	Internal. Only to be used through TI provided API.
3-1	IFAMPRFLDO_IFAMPIB	R/W	0h	Internal. Only to be used through TI provided API.
0	IFAMPRFLDO_IFAMP	R/W	0h	Internal. Only to be used through TI provided API.

28.10.24 IFADC0_ULNA Register (Offset = 60h) [Reset = 00000000h]

IFADC0_ULNA is shown in Table 28-497.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-497. IFADC0_ULNA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXTCLK	R/W	0h	Internal. Only to be used through TI provided API.
30-28	DITHERTRIM	R/W	0h	Internal. Only to be used through TI provided API.
27-26	DITHEREN	R/W	0h	Internal. Only to be used through TI provided API.
25	ADCIEN	R/W	0h	Internal. Only to be used through TI provided API.
24	ADCQEN	R/W	0h	Internal. Only to be used through TI provided API.
23-20	INT2ADJ	R/W	0h	Internal. Only to be used through TI provided API.
19-18	AAFCAP	R/W	0h	Internal. Only to be used through TI provided API.
17-16	RESERVED	R	0h	Internal. Only to be used through TI provided API.
15-0	SPARE	R/W	0h	Internal. Only to be used through TI provided API.

28.10.25 IFADCLF_IFADC1 Register (Offset = 64h) [Reset = 00000000h]

IFADCLF_IFADC1 is shown in Table 28-498.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-498. IFADCLF_IFADC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	FF3	R/W	0h	Internal. Only to be used through TI provided API.
27-24	FF2	R/W	0h	Internal. Only to be used through TI provided API.
23-20	FF1	R/W	0h	Internal. Only to be used through TI provided API.
19-16	INT3	R/W	0h	Internal. Only to be used through TI provided API.
15	NRZ	R/W	0h	Internal. Only to be used through TI provided API.
14-9	TRIM	R/W	0h	Internal. Only to be used through TI provided API.
8	RESERVED	R	0h	Internal. Only to be used through TI provided API.
7	RSTN	R/W	0h	Internal. Only to be used through TI provided API.
6	CLKGEN	R/W	0h	Internal. Only to be used through TI provided API.
5	ADCDIGCLK	R/W	0h	Internal. Only to be used through TI provided API.
4	ADCLFSROUT	R/W	0h	Internal. Only to be used through TI provided API.
3-1	LPFTSTMODE	R/W	0h	Internal. Only to be used through TI provided API.
0	INVCLKOUT	R/W	0h	Internal. Only to be used through TI provided API.

28.10.26 IFADCALDO_IFADCQUANT Register (Offset = 68h) [Reset = 00000000h]

IFADCALDO_IFADCQUANT is shown in Table 28-499.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-499. IFADCALDO_IFADCQUANT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ATESTVSSANA	R/W	0h	Internal. Only to be used through TI provided API.
30	RESERVED	R	0h	Internal. Only to be used through TI provided API.
29-24	TRIMOUT	R/W	0h	Internal. Only to be used through TI provided API.
23	DUMMY	R/W	0h	Internal. Only to be used through TI provided API.
22	ATESTERRAMP	R/W	0h	Internal. Only to be used through TI provided API.
21	ATESTINPUTREF	R/W	0h	Internal. Only to be used through TI provided API.
20	ATESTOUT	R/W	0h	Internal. Only to be used through TI provided API.
19	ITEST	R/W	0h	Internal. Only to be used through TI provided API.
18	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
17	CLAMP	R/W	0h	Internal. Only to be used through TI provided API.
16	CTL	R/W	0h	Internal. Only to be used through TI provided API.
15-14	CLKDLYTRIM	R/W	0h	Internal. Only to be used through TI provided API.
13-9	DBGCALVALIN	R/W	0h	Internal. Only to be used through TI provided API.
8	DBGCALLEG	R/W	0h	Internal. Only to be used through TI provided API.
7-6	DBGCALMQ	R/W	0h	Internal. Only to be used through TI provided API.
5-4	DBGCALMI	R/W	0h	Internal. Only to be used through TI provided API.
3	AUTOCAL	R/W	0h	Internal. Only to be used through TI provided API.
2-0	QUANTTHR	R/W	0h	Internal. Only to be used through TI provided API.

28.10.27 IFADCTST_IFADCDLDO Register (Offset = 6Ch) [Reset = 00000000h]

IFADCTST_IFADCDLDO is shown in Table 28-500.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-500. IFADCTST_IFADCDLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	EXTCURR	R/W	0h	Internal. Only to be used through TI provided API.
22	QCALDBIQ	R/W	0h	Internal. Only to be used through TI provided API.
21	QCALDBC	R/W	0h	Internal. Only to be used through TI provided API.
20-16	SEL	R/W	0h	Internal. Only to be used through TI provided API.
15-14	RESERVED	R	0h	Internal. Only to be used through TI provided API.
13-8	TRIMOUT	R/W	0h	Internal. Only to be used through TI provided API.
7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6	ATESTERRAMP	R/W	0h	Internal. Only to be used through TI provided API.
5	ATESTFB	R/W	0h	Internal. Only to be used through TI provided API.
4	ATESTOUT	R/W	0h	Internal. Only to be used through TI provided API.
3	ITEST	R/W	0h	Internal. Only to be used through TI provided API.
2	BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
1	CLAMP	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.28 ATSTREF Register (Offset = 70h) [Reset = 00000000h]

ATSTREF is shown in Table 28-501.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-501. ATSTREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VREFBPDIS	R/W	0h	Internal. Only to be used through TI provided API.
30-26	IREFTRIM	R/W	0h	Internal. Only to be used through TI provided API.
25	BIAS	R/W	0h	Internal. Only to be used through TI provided API.
24	OUTPUT1	R/W	0h	Internal. Only to be used through TI provided API.
23	OUTPUT2	R/W	0h	Internal. Only to be used through TI provided API.
22-0	MUX	R/W	X	Internal. Only to be used through TI provided API.

28.10.29 DIV_DCO Register (Offset = 74h) [Reset = 00000000h]

DIV_DCO is shown in Table 28-502.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-502. DIV_DCO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PDET	R/W	0h	Internal. Only to be used through TI provided API.
30-28	NMIREFTRIM	R/W	0h	Internal. Only to be used through TI provided API.
27-25	PMIREFTRIM	R/W	0h	Internal. Only to be used through TI provided API.
24	TXBBOOST	R/W	0h	Internal. Only to be used through TI provided API.
23	S1GFRC	R/W	0h	Internal. Only to be used through TI provided API.
22-21	BUFGAIN	R/W	0h	Internal. Only to be used through TI provided API.
20	BIAS	R/W	0h	Internal. Only to be used through TI provided API.
19	OUT	R/W	0h	Internal. Only to be used through TI provided API.
18-16	RATIO	R/W	0h	Internal. Only to be used through TI provided API.
15-11	RESERVED	R	0h	Reserved
10-9	MTDCSPARE	R/W	0h	Internal. Only to be used through TI provided API.
8-7	SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6-3	TAILRESTRIM	R/W	0h	Internal. Only to be used through TI provided API.
2	RTRIMCAP	R/W	0h	Internal. Only to be used through TI provided API.
1	CNRCAP	R/W	0h	Internal. Only to be used through TI provided API.
0	CRSCAPCM	R/W	0h	Internal. Only to be used through TI provided API.

28.10.30 TDCLDO_DIVLDO Register (Offset = 78h) [Reset = 00000000h]

TDCLDO_DIVLDO is shown in Table 28-503.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-503. TDCLDO_DIVLDO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TDCLDO_ITESTCTL	R/W	0h	Internal. Only to be used through TI provided API.
30-24	TDCLDO_VOUTTRIM	R/W	0h	Internal. Only to be used through TI provided API.
23	TDCLDO_SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
22-20	TDCLDO_TMUX	R/W	0h	Internal. Only to be used through TI provided API.
19	TDCLDO_PDSEL	R/W	0h	Internal. Only to be used through TI provided API.
18	TDCLDO_MODE	R/W	0h	Internal. Only to be used through TI provided API.
17	TDCLDO_BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
16	TDCLDO_CTL	R/W	0h	Internal. Only to be used through TI provided API.
15	DIVLDO_ITESTCTL	R/W	0h	Internal. Only to be used through TI provided API.
14-8	DIVLDO_VOUTTRIM	R/W	0h	Internal. Only to be used through TI provided API.
7	DIVLDO_SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
6-4	DIVLDO_TMUX	R/W	0h	Internal. Only to be used through TI provided API.
3	DIVLDO_PDSEL	R/W	0h	Internal. Only to be used through TI provided API.
2	DIVLDO_MODE	R/W	0h	Internal. Only to be used through TI provided API.
1	DIVLDO_BYPASS	R/W	0h	Internal. Only to be used through TI provided API.
0	DIVLDO_CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.31 DCOLDO1_DCOLDO0 Register (Offset = 7Ch) [Reset = 00000000h]

DCOLDO1_DCOLDO0 is shown in Table 28-504.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-504. DCOLDO1_DCOLDO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	REFSRC	R/W	0h	Internal. Only to be used through TI provided API.
25-24	DIVATST	R/W	0h	Internal. Only to be used through TI provided API.
23	PERFM	R/W	0h	Internal. Only to be used through TI provided API.
22	CHRGFILT	R/W	0h	Internal. Only to be used through TI provided API.
21-16	ATST	R/W	0h	Internal. Only to be used through TI provided API.
15-14	ITST	R/W	0h	Internal. Only to be used through TI provided API.
13-8	SECONDTRIM	R/W	0h	Internal. Only to be used through TI provided API.
7-4	FIRSTTRIM	R/W	0h	Internal. Only to be used through TI provided API.
3	PDN	R/W	0h	Internal. Only to be used through TI provided API.
2	BYPFIRST	R/W	0h	Internal. Only to be used through TI provided API.
1	BYPBOTH	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.32 PRE1_PRE0 Register (Offset = 80h) [Reset = 00000000h]

PRE1_PRE0 is shown in Table 28-505.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-505. PRE1_PRE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	IIRBW	R/W	0h	Internal. Only to be used through TI provided API.
29	IIRORD	R/W	0h	Internal. Only to be used through TI provided API.
28-24	IIRDIV	R/W	0h	Internal. Only to be used through TI provided API.
23	RESERVED	R	0h	Reserved
22	CALHSDDC	R/W	0h	Internal. Only to be used through TI provided API.
21-16	HSDDC	R/W	0h	Internal. Only to be used through TI provided API.
15-14	SPARE14	R/W	0h	Internal. Only to be used through TI provided API.
13-8	PLLDIV1	R/W	0h	Internal. Only to be used through TI provided API.
7-6	SPARE6	R/W	0h	Internal. Only to be used through TI provided API.
5-0	PLLDIV0	R/W	0h	Internal. Only to be used through TI provided API.

28.10.33 PRE3_PRE2 Register (Offset = 84h) [Reset = 00000000h]

PRE3_PRE2 is shown in Table 28-506.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-506. PRE3_PRE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	FINECALDIV	R/W	0h	Internal. Only to be used through TI provided API.
20-16	MIDCALDIVMSB	R/W	0h	Internal. Only to be used through TI provided API.
15-12	MIDCALDIVLSB	R/W	0h	Internal. Only to be used through TI provided API.
11-6	CRSCALDIV	R/W	0h	Internal. Only to be used through TI provided API.
5-0	FSMDIV	R/W	0h	Internal. Only to be used through TI provided API.

28.10.34 CAL1_CAL0 Register (Offset = 88h) [Reset = 00000000h]

CAL1_CAL0 is shown in Table 28-507.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-507. CAL1_CAL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL1_SPARE15	R/W	0h	Internal. Only to be used through TI provided API.
30-24	CAL1_FCTOP	R/W	0h	Internal. Only to be used through TI provided API.
23	CAL1_SPARE7	R/W	0h	Internal. Only to be used through TI provided API.
22-16	CAL1_FCBOT	R/W	0h	Internal. Only to be used through TI provided API.
15	CAL0_SPARE15	R/W	0h	Internal. Only to be used through TI provided API.
14-8	CAL0_FCSTART	R/W	0h	Internal. Only to be used through TI provided API.
7	CAL0_CRS	R/W	0h	Internal. Only to be used through TI provided API.
6	CAL0_MID	R/W	0h	Internal. Only to be used through TI provided API.
5	CAL0_KTDC	R/W	0h	Internal. Only to be used through TI provided API.
4	CAL0_KDCO	R/W	0h	Internal. Only to be used through TI provided API.
3-2	CAL0_TDCAVG	R/W	0h	Internal. Only to be used through TI provided API.
1-0	CAL0_TDC_SPARE	R/W	0h	Internal. Only to be used through TI provided API.

28.10.35 CAL3_CAL2 Register (Offset = 8Ch) [Reset = 00000000h]

CAL3_CAL2 is shown in Table 28-508.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-508. CAL3_CAL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DTXGAIN	R/W	0h	Internal. Only to be used through TI provided API.
15-0	KTDCINV	R/W	0h	Internal. Only to be used through TI provided API.

28.10.36 MISC1_MISC0 Register (Offset = 90h) [Reset = 00000000h]

MISC1_MISC0 is shown in Table 28-509.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-509. MISC1_MISC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	FCDEMCLK	R/W	0h	Internal. Only to be used through TI provided API.
29-28	FCDEMUPD	R/W	0h	Internal. Only to be used through TI provided API.
27-22	TDCINL	R/W	0h	Internal. Only to be used through TI provided API.
21	TDCINLCTL	R/W	0h	Internal. Only to be used through TI provided API.
20	PHINIT	R/W	0h	Internal. Only to be used through TI provided API.
19	SDMOOVRCTL	R/W	0h	Internal. Only to be used through TI provided API.
18-16	SDMOOVR	R/W	0h	Internal. Only to be used through TI provided API.
15	TDCCALENHCTL	R/W	0h	Internal. Only to be used through TI provided API.
14	TDCCALENHCFG	R/W	0h	Internal. Only to be used through TI provided API.
13	PHCPT	R/W	0h	Internal. Only to be used through TI provided API.
12	TDCCALCORR	R/W	0h	Internal. Only to be used through TI provided API.
11	TDCMSBCORR	R/W	0h	Internal. Only to be used through TI provided API.
10	SDMDEM	R/W	0h	Internal. Only to be used through TI provided API.
9-8	DLYSDM	R/W	0h	Internal. Only to be used through TI provided API.
7	CKVDENFRC	R/W	0h	Internal. Only to be used through TI provided API.
6	DLYPHVALID	R/W	0h	Internal. Only to be used through TI provided API.
5-4	DLYCANCRS	R/W	0h	Internal. Only to be used through TI provided API.
3-2	DLYCANFINE	R/W	0h	Internal. Only to be used through TI provided API.
1-0	DLYADD	R/W	0h	Internal. Only to be used through TI provided API.

28.10.37 LF1_LF0 Register (Offset = 94h) [Reset = 00000000h]

LF1_LF0 is shown in Table 28-510.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-510. LF1_LF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	KP	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12	KIPREC	R/W	0h	Internal. Only to be used through TI provided API.
11-0	KI	R/W	0h	Internal. Only to be used through TI provided API.

28.10.38 PHINIT_PHEDISC Register (Offset = 98h) [Reset = 00000000h]

PHINIT_PHEDISC is shown in Table 28-511.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-511. PHINIT_PHEDISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	OFF	R/W	0h	Internal. Only to be used through TI provided API.
15-14	RESERVED	R	0h	Reserved
13-10	CNT	R/W	0h	Internal. Only to be used through TI provided API.
9-0	THR	R/W	0h	Internal. Only to be used through TI provided API.

28.10.39 PLLMON1_PLLMON0 Register (Offset = 9Ch) [Reset = 00000000h]

PLLMON1_PLLMON0 is shown in Table 28-512.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-512. PLLMON1_PLLMON0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	PHELOCKCNT	R/W	0h	Internal. Only to be used through TI provided API.
23-16	PHELOCKTHR	R/W	0h	Internal. Only to be used through TI provided API.
15-14	PHELOLCNT	R/W	0h	Internal. Only to be used through TI provided API.
13-8	PHELOLTHR	R/W	0h	Internal. Only to be used through TI provided API.
7	RESERVED	R	0h	Reserved
6-0	FCTHR	R/W	0h	Internal. Only to be used through TI provided API.

28.10.40 MOD1_MOD0 Register (Offset = A0h) [Reset = 00000000h]

MOD1_MOD0 is shown in Table 28-513.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-513. MOD1_MOD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	FOFF	R/W	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12-11	SCHEME	R/W	0h	Internal. Only to be used through TI provided API.
10-8	SYMSHP	R/W	0h	Internal. Only to be used through TI provided API.
7-6	CANPTHGAIN	R/W	0h	Internal. Only to be used through TI provided API.
5-4	SHPGAIN	R/W	0h	Internal. Only to be used through TI provided API.
3-2	INTPFACT	R/W	0h	Internal. Only to be used through TI provided API.
1-0	RESERVED	R	0h	Reserved

28.10.41 DTX1_DTX0 Register (Offset = A4h) [Reset = 00000000h]

DTX1_DTX0 is shown in Table 28-514.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-514. DTX1_DTX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHP3	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SHP2	R/W	0h	Internal. Only to be used through TI provided API.
15-8	SHP1	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP0	R/W	0h	Internal. Only to be used through TI provided API.

28.10.42 DTX3_DTX2 Register (Offset = A8h) [Reset = 00000000h]

DTX3_DTX2 is shown in Table 28-515.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-515. DTX3_DTX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHP7	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SHP6	R/W	0h	Internal. Only to be used through TI provided API.
15-8	SHP5	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP4	R/W	0h	Internal. Only to be used through TI provided API.

28.10.43 DTX5_DTX4 Register (Offset = ACh) [Reset = 00000000h]

DTX5_DTX4 is shown in Table 28-516.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-516. DTX5_DTX4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHP11	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SHP10	R/W	0h	Internal. Only to be used through TI provided API.
15-8	SHP9	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP8	R/W	0h	Internal. Only to be used through TI provided API.

28.10.44 DTX7_DTX6 Register (Offset = B0h) [Reset = 00000000h]

DTX7_DTX6 is shown in Table 28-517.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-517. DTX7_DTX6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHP15	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SHP14	R/W	0h	Internal. Only to be used through TI provided API.
15-8	SHP13	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP12	R/W	0h	Internal. Only to be used through TI provided API.

28.10.45 DTX9_DTX8 Register (Offset = B4h) [Reset = 00000000h]

DTX9_DTX8 is shown in Table 28-518.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-518. DTX9_DTX8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHP19	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SHP18	R/W	0h	Internal. Only to be used through TI provided API.
15-8	SHP17	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP16	R/W	0h	Internal. Only to be used through TI provided API.

28.10.46 DTX11_DTX10 Register (Offset = B8h) [Reset = 00000000h]

DTX11_DTX10 is shown in Table 28-519.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-519. DTX11_DTX10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SHP23	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SHP22	R/W	0h	Internal. Only to be used through TI provided API.
15-8	SHP21	R/W	0h	Internal. Only to be used through TI provided API.
7-0	SHP20	R/W	0h	Internal. Only to be used through TI provided API.

28.10.47 PLLM0 Register (Offset = BCh) [Reset = 00000000h]

PLLM0 is shown in Table 28-520.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-520. PLLM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	VAL	R/W	0h	Internal. Only to be used through TI provided API.
1-0	SPARE0	R/W	0h	Internal. Only to be used through TI provided API.

28.10.48 PLLM1 Register (Offset = C0h) [Reset = 00000000h]

PLLM1 is shown in Table 28-521.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-521. PLLM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	VAL	R/W	0h	Internal. Only to be used through TI provided API.
1-0	SPARE0	R/W	0h	Internal. Only to be used through TI provided API.

28.10.49 CALMMID_CALMCRS Register (Offset = C4h) [Reset = 00000000h]

CALMMID_CALMCRS is shown in Table 28-522.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-522. CALMMID_CALMCRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALMMID_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	CALMCRS_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.50 REFDIV Register (Offset = C8h) [Reset = 00000000h]

REFDIV is shown in Table 28-523.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-523. REFDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LOAD	R/W	0h	Internal. Only to be used through TI provided API.

28.10.51 DLOCTL0 Register (Offset = CCh) [Reset = 00000000h]

DLOCTL0 is shown in Table 28-524.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-524. DLOCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	TDCSTOP	R/W	0h	Internal. Only to be used through TI provided API.
7	DTSTXTAL	R/W	0h	Internal. Only to be used through TI provided API.
6-4	LOOPUPD	R/W	0h	Internal. Only to be used through TI provided API.
3	PH3	R/W	0h	Internal. Only to be used through TI provided API.
2	PH2	R/W	0h	Internal. Only to be used through TI provided API.
1	LOOPMODE	R/W	0h	Internal. Only to be used through TI provided API.
0	RSTN	R/W	0h	Internal. Only to be used through TI provided API.

28.10.52 DLOCTL1 Register (Offset = D0h) [Reset = 00000000h]

DLOCTL1 is shown in Table 28-525.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-525. DLOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	DCO	R/W	0h	Internal. Only to be used through TI provided API.
14-11	RESERVED	R	0h	Reserved
10	LFSYNCATGRSHFT	R/W	0h	Internal. Only to be used through TI provided API.
9	LFSYNCATPEAK	R/W	0h	Internal. Only to be used through TI provided API.
8	PHEADJ	R/W	0h	Internal. Only to be used through TI provided API.
7	FCDEM	R/W	0h	Internal. Only to be used through TI provided API.
6	DTSTCKVD	R/W	0h	Internal. Only to be used through TI provided API.
5	PHEDISC	R/W	0h	Internal. Only to be used through TI provided API.
4	PLLMON	R/W	0h	Internal. Only to be used through TI provided API.
3	IIR	R/W	0h	Internal. Only to be used through TI provided API.
2	MOD	R/W	0h	Internal. Only to be used through TI provided API.
1	MODINIT	R/W	0h	Internal. Only to be used through TI provided API.
0	MTDCRSTN	R/W	0h	Internal. Only to be used through TI provided API.

28.10.53 DCOOVR1_DCOOVR0 Register (Offset = D4h) [Reset = 00000000h]

DCOOVR1_DCOOVR0 is shown in Table 28-526.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-526. DCOOVR1_DCOOVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-24	FINECODE	R/W	0h	Internal. Only to be used through TI provided API.
23-16	SDMICODE	R/W	0h	Internal. Only to be used through TI provided API.
15-14	RESERVED	R	0h	Reserved
13-8	MIDCODE	R/W	0h	Internal. Only to be used through TI provided API.
7-4	CRSCODE	R/W	0h	Internal. Only to be used through TI provided API.
3	FINECTL	R/W	0h	Internal. Only to be used through TI provided API.
2	SDMICTL	R/W	0h	Internal. Only to be used through TI provided API.
1	MIDCTL	R/W	0h	Internal. Only to be used through TI provided API.
0	CRSCTL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.54 DLOEV_DTST Register (Offset = D8h) [Reset = 00000000h]

DLOEV_DTST is shown in Table 28-527.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-527. DLOEV_DTST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	LOCK	R	0h	Internal. Only to be used through TI provided API.
22	LOL	R	0h	Internal. Only to be used through TI provided API.
21	FCABVTHR	R	0h	Internal. Only to be used through TI provided API.
20	FCBLWTHR	R	0h	Internal. Only to be used through TI provided API.
19-16	STATE	R	0h	Internal. Only to be used through TI provided API.
15	RESERVED	R	0h	Reserved
14-11	SPARE11	R/W	0h	Internal. Only to be used through TI provided API.
10-8	VARTGLDLY	R/W	0h	Internal. Only to be used through TI provided API.
7	REFTGLDLY	R/W	0h	Internal. Only to be used through TI provided API.
6	TRNSEQ	R/W	0h	Internal. Only to be used through TI provided API.
5	SPARE5	R/W	0h	Internal. Only to be used through TI provided API.
4-0	SIG	R/W	0h	Internal. Only to be used through TI provided API.

28.10.55 DTSTRD Register (Offset = DCh) [Reset = 00000000h]

DTSTRD is shown in Table 28-528.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-528. DTSTRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	DATA	R	0h	Internal. Only to be used through TI provided API.

28.10.56 FDCOSPANMSB_FDCOSPANLSB Register (Offset = E0h) [Reset = 00000000h]

FDCOSPANMSB_FDCOSPANLSB is shown in Table 28-529.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-529. FDCOSPANMSB_FDCOSPANLSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	FDCOSPANMSB_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	FDCOSPANLSB_VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.57 TDCCALLOW_TDCCAL Register (Offset = E4h) [Reset = 00000000h]

TDCCALLOW_TDCCAL is shown in Table 28-530.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-530. TDCCALLOW_TDCCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TDCCALLOW_VAL	R	0h	Internal. Only to be used through TI provided API.
15-0	TDCCAL_VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.58 TDCODET_TDCCALHIGH Register (Offset = E8h) [Reset = 00000000h]

TDCODET_TDCCALHIGH is shown in Table 28-531.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-531. TDCODET_TDCCALHIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	FLAGS	R	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.59 GPI_CALRES Register (Offset = ECh) [Reset = 00000000h]

GPI_CALRES is shown in Table 28-532.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-532. GPI_CALRES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23	GPI7	R	0h	Internal. Only to be used through TI provided API.
22	GPI6	R	0h	Internal. Only to be used through TI provided API.
21	GPI5	R	0h	Internal. Only to be used through TI provided API.
20	GPI4	R	0h	Internal. Only to be used through TI provided API.
19	GPI3	R	0h	Internal. Only to be used through TI provided API.
18	GPI2	R	0h	Internal. Only to be used through TI provided API.
17	GPI1	R	0h	Internal. Only to be used through TI provided API.
16	GPI0	R	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-4	MIDCODE	R	0h	Internal. Only to be used through TI provided API.
3-0	CRSCODE	R	0h	Internal. Only to be used through TI provided API.

28.10.60 LIN2LOGOUT_MATHACCELIN Register (Offset = F0h) [Reset = 00000000h]

LIN2LOGOUT_MATHACCELIN is shown in Table 28-533.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-533. LIN2LOGOUT_MATHACCELIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-16	LOGVAL	R	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.61 TIMCTL_DIVBY3OUT Register (Offset = F4h) [Reset = 00000000h]

TIMCTL_DIVBY3OUT is shown in Table 28-534.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-534. TIMCTL_DIVBY3OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	CPTSRC	R/W	0h	Internal. Only to be used through TI provided API.
23	CPTCTL	R/W	0h	Internal. Only to be used through TI provided API.
22-21	CNTRSRC	R/W	0h	Internal. Only to be used through TI provided API.
20	CNTRCLR	R/W	0h	Internal. Only to be used through TI provided API.
19	CNTRCTL	R/W	0h	Internal. Only to be used through TI provided API.
18-17	TIMSRC	R/W	0h	Internal. Only to be used through TI provided API.
16	TIMCTL	R/W	0h	Internal. Only to be used through TI provided API.
15-4	RESERVED	R	0h	Reserved
3-0	DIV3	R	0h	Internal. Only to be used through TI provided API.

28.10.62 TIMPER_TIMINC Register (Offset = F8h) [Reset = 00000000h]

TIMPER_TIMINC is shown in Table 28-535.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-535. TIMPER_TIMINC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TIMPER_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	TIMINC_VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.63 TIMCAPT_TIMCNT Register (Offset = FCh) [Reset = 00000000h]

TIMCAPT_TIMCNT is shown in Table 28-536.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-536. TIMCAPT_TIMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VALUE	R	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.64 TRCSTAT_TRCCTRL Register (Offset = 100h) [Reset = 00000000h]

TRCSTAT_TRCCTRL is shown in Table 28-537.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-537. TRCSTAT_TRCCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	BUSY	R	0h	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	SEND	W	0h	Internal. Only to be used through TI provided API.

28.10.65 TRCPAR0_TRCCMD Register (Offset = 104h) [Reset = 00000000h]

TRCPAR0_TRCCMD is shown in Table 28-538.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-538. TRCPAR0_TRCCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-10	RESERVED	R	0h	Reserved
9-8	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.
7-0	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.

28.10.66 GPOCTL_TRCPAR1 Register (Offset = 108h) [Reset = 00000000h]

GPOCTL_TRCPAR1 is shown in Table 28-539.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-539. GPOCTL_TRCPAR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEL7	R/W	0h	Internal. Only to be used through TI provided API.
30	SEL6	R/W	0h	Internal. Only to be used through TI provided API.
29	SEL5	R/W	0h	Internal. Only to be used through TI provided API.
28	SEL4	R/W	0h	Internal. Only to be used through TI provided API.
27	SEL3	R/W	0h	Internal. Only to be used through TI provided API.
26	SEL2	R/W	0h	Internal. Only to be used through TI provided API.
25	SEL1	R/W	0h	Internal. Only to be used through TI provided API.
24	SEL0	R/W	0h	Internal. Only to be used through TI provided API.
23	GPO7	R/W	0h	Internal. Only to be used through TI provided API.
22	GPO6	R/W	0h	Internal. Only to be used through TI provided API.
21	GPO5	R/W	0h	Internal. Only to be used through TI provided API.
20	GPO4	R/W	0h	Internal. Only to be used through TI provided API.
19	GPO3	R/W	0h	Internal. Only to be used through TI provided API.
18	GPO2	R/W	0h	Internal. Only to be used through TI provided API.
17	GPO1	R/W	0h	Internal. Only to be used through TI provided API.
16	GPO0	R/W	0h	Internal. Only to be used through TI provided API.
15-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.67 DIVCTL_ANAISOCTL Register (Offset = 10Ch) [Reset = 00000000h]

DIVCTL_ANAISOCTL is shown in Table 28-540.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-540. DIVCTL_ANAISOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIV2PH180	R/W	0h	Internal. Only to be used through TI provided API.
30	DIV2PH0	R/W	0h	Internal. Only to be used through TI provided API.
29	DIV2PH270	R/W	0h	Internal. Only to be used through TI provided API.
28	DIV2PH90	R/W	0h	Internal. Only to be used through TI provided API.
27	SPARE11	R/W	0h	Internal. Only to be used through TI provided API.
26	S1G20DBMMUX	R/W	0h	Internal. Only to be used through TI provided API.
25	ADCDIV	R/W	0h	Internal. Only to be used through TI provided API.
24	ENSYNTH	R/W	0h	Internal. Only to be used through TI provided API.
23	TXPH18020DBMDIV	R/W	0h	Internal. Only to be used through TI provided API.
22	TXPH020DBMDIV	R/W	0h	Internal. Only to be used through TI provided API.
21	TXPH180DIV	R/W	0h	Internal. Only to be used through TI provided API.
20	TXPH0DIV	R/W	0h	Internal. Only to be used through TI provided API.
19	RXPH90DIV	R/W	0h	Internal. Only to be used through TI provided API.
18	RXPH0DIV	R/W	0h	Internal. Only to be used through TI provided API.
17	Spare1	R/W	0h	Internal. Only to be used through TI provided API.
16	EN	R/W	0h	Internal. Only to be used through TI provided API.
15-5	RESERVED	R	0h	Reserved
4	ADCDIGRSTN	R/W	0h	Internal. Only to be used through TI provided API.
3	IFADC2SVTISO	R/W	0h	Internal. Only to be used through TI provided API.
2	DIV2IFADCISO	R/W	0h	Internal. Only to be used through TI provided API.
1	MTDC2SVTISO	R/W	0h	Internal. Only to be used through TI provided API.
0	DIV2MTDCISO	R/W	0h	Internal. Only to be used through TI provided API.

28.10.68 MAGNACC0_RXCTRL Register (Offset = 110h) [Reset = 00000000h]

MAGNACC0_RXCTRL is shown in Table 28-541.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-541. MAGNACC0_RXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VAL	R	0h	Internal. Only to be used through TI provided API.
15-13	RESERVED	R	0h	Reserved
12	SPARE	R/W	0h	Internal. Only to be used through TI provided API.
11-9	ATTN	R/W	0h	Internal. Only to be used through TI provided API.
8-4	IFAMPGC	R/W	0h	Internal. Only to be used through TI provided API.
3-0	LNAGAIN	R/W	0h	Internal. Only to be used through TI provided API.

28.10.69 RSSI_MAGNACC1 Register (Offset = 114h) [Reset = 00000000h]

RSSI_MAGNACC1 is shown in Table 28-542.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-542. RSSI_MAGNACC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	RSSI_VAL	R/W	0h	Internal. Only to be used through TI provided API.
15-0	MAGNACC1_VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.70 RFGAIN_RSSIMAX Register (Offset = 118h) [Reset = 00000000h]

RFGAIN_RSSIMAX is shown in Table 28-543.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-543. RFGAIN_RSSIMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	DBGAIN	R/W	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.71 DIVSTA_IFADCSTAT Register (Offset = 11Ch) [Reset = 00000000h]

DIVSTA_IFADCSTAT is shown in Table 28-544.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-544. DIVSTA_IFADCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	STAT	R	0h	Internal. Only to be used through TI provided API.
15-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Internal. Only to be used through TI provided API.
6-2	QUANTCALVAL	R	0h	Internal. Only to be used through TI provided API.
1	QUANTCALDONE	R	0h	Internal. Only to be used through TI provided API.
0	RESERVED	R	0h	Internal. Only to be used through TI provided API.

28.10.72 DIVIDEND Register (Offset = 120h) [Reset = 00000000h]

DIVIDEND is shown in Table 28-545.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-545. DIVIDEND Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	W	0h	Internal. Only to be used through TI provided API.

28.10.73 DIVISOR Register (Offset = 124h) [Reset = 00000000h]

DIVISOR is shown in Table 28-546.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-546. DIVISOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Internal. Only to be used through TI provided API.

28.10.74 QUOTIENT Register (Offset = 128h) [Reset = 00000000h]

QUOTIENT is shown in Table 28-547.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-547. QUOTIENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.75 PRODUCT Register (Offset = 12Ch) [Reset = 00000000h]

PRODUCT is shown in Table 28-548.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-548. PRODUCT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Internal. Only to be used through TI provided API.

28.10.76 MULTSTA Register (Offset = 130h) [Reset = 00000000h]

MULTSTA is shown in Table 28-549.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-549. MULTSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	STAT	R	0h	Internal. Only to be used through TI provided API.

28.10.77 PA1_MULTCFG Register (Offset = 134h) [Reset = 00000000h]

PA1_MULTCFG is shown in Table 28-550.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-550. PA1_MULTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PA1_SPARE0	R/W	0h	Internal. Only to be used through TI provided API.
28-27	PA1_MODE	R/W	0h	Internal. Only to be used through TI provided API.
26-24	PA1_GAIN	R/W	0h	Internal. Only to be used through TI provided API.
23-18	PA1_IB	R/W	0h	Internal. Only to be used through TI provided API.
17-16	PA1_IBBOOST	R/W	0h	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	MULTCFG_MODE	R/W	0h	Internal. Only to be used through TI provided API.

28.10.78 PA2 Register (Offset = 138h) [Reset = 00000000h]

PA2 is shown in Table 28-551.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-551. PA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-5	SPARE5	R/W	0h	Internal. Only to be used through TI provided API.
4-0	TRIM	R/W	0h	Internal. Only to be used through TI provided API.

28.11 LRFDRXF Registers

Table 28-552 lists the memory-mapped registers for the LRFDRXF registers. All register offset addresses not listed in Table 28-552 should be considered as reserved locations and the register contents should not be modified.

Table 28-552. LRFDRXF Registers

Offset	Acronym	Register Name	Section
0h	RXD	Data to from RXFIFO	Section 28.11.1

Complex bit access types are encoded to fit into small table cells. Table 28-553 shows the codes that are used for access types in this section.

Table 28-553. LRFDRXF Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.11.1 RXD Register (Offset = 0h) [Reset = 00000000h]

RXD is shown in Table 28-554.

Return to the Summary Table.

RX FIFO data. When written the register data is pushed to the RX FIFO. When read, data is popped from the RX FIFO

Table 28-554. RXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	RX FIFO data. When written the register data is pushed to the RX FIFO. When read, data is popped from the RX FIFO. When writing or reading this register the access size will determine how many bytes are pushed to or popped from the FIFO. It is possible to push or pop 1,2 or 4 bytes depending on the access being done.

28.12 LRFDS2R Registers

Table 28-555 lists the memory-mapped registers for the LRFDS2R registers. All register offset addresses not listed in Table 28-555 should be considered as reserved locations and the register contents should not be modified.

Table 28-555. LRFDS2R Registers

Offset	Acronym	Register Name	Section
0h	CFG	Internal. Only to be used through TI provided API.	Section 28.12.1
4h	START	Internal. Only to be used through TI provided API.	Section 28.12.2
8h	STOP	Internal. Only to be used through TI provided API.	Section 28.12.3
Ch	STAT	Internal. Only to be used through TI provided API.	Section 28.12.4
10h	TRIG	Internal. Only to be used through TI provided API.	Section 28.12.5

Complex bit access types are encoded to fit into small table cells. Table 28-556 shows the codes that are used for access types in this section.

Table 28-556. LRFDS2R Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.12.1 CFG Register (Offset = 0h) [Reset = 00000000h]

CFG is shown in Table 28-557.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-557. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	LAST0	R/W	0h	Internal. Only to be used through TI provided API.
4-3	TRIGMODE	R/W	0h	Internal. Only to be used through TI provided API.
2-1	SEL	R/W	0h	Internal. Only to be used through TI provided API.
0	CTL	R/W	0h	Internal. Only to be used through TI provided API.

28.12.2 START Register (Offset = 4h) [Reset = 00000000h]

START is shown in Table 28-558.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-558. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ADDR	R/W	0h	Internal. Only to be used through TI provided API.

28.12.3 STOP Register (Offset = 8h) [Reset = 00000000h]

STOP is shown in Table 28-559.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-559. STOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ADDR	R/W	0h	Internal. Only to be used through TI provided API.

28.12.4 STAT Register (Offset = Ch) [Reset = 00000000h]

STAT is shown in Table 28-560.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-560. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	ADDRCNT	R	FFFh	Internal. Only to be used through TI provided API.
15-1	RESERVED	R	0h	Reserved
0	RUNNING	R	0h	Internal. Only to be used through TI provided API.

28.12.5 TRIG Register (Offset = 10h) [Reset = 00000000h]

TRIG is shown in Table 28-561.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-561. TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TRIG	W	0h	Internal. Only to be used through TI provided API.

28.13 LRFDTRC Registers

Table 28-562 lists the memory-mapped registers for the LRFDTRC registers. All register offset addresses not listed in Table 28-562 should be considered as reserved locations and the register contents should not be modified.

Table 28-562. LRFDTRC Registers

Offset	Acronym	Register Name	Section
0h	CFG	Internal. Only to be used through TI provided API.	Section 28.13.1
4h	CH1CMD	Internal. Only to be used through TI provided API.	Section 28.13.2
8h	CH2CMD	Internal. Only to be used through TI provided API.	Section 28.13.3
Ch	CH3CMD	Internal. Only to be used through TI provided API.	Section 28.13.4
14h	CH1PAR01	Internal. Only to be used through TI provided API.	Section 28.13.5
18h	CH2PAR01	Internal. Only to be used through TI provided API.	Section 28.13.6
1Ch	CH3PAR01	Internal. Only to be used through TI provided API.	Section 28.13.7
24h	CH1PAR23	Internal. Only to be used through TI provided API.	Section 28.13.8
28h	CH2PAR23	Internal. Only to be used through TI provided API.	Section 28.13.9
2Ch	CH3PAR23	Internal. Only to be used through TI provided API.	Section 28.13.10

Complex bit access types are encoded to fit into small table cells. Table 28-563 shows the codes that are used for access types in this section.

Table 28-563. LRFDTRC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.13.1 CFG Register (Offset = 0h) [Reset = 00000000h]

CFG is shown in Table 28-564.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-564. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-7	PRESCAL	R/W	0h	Internal. Only to be used through TI provided API.
6	TSCLR	W	0h	Internal. Only to be used through TI provided API.
5	TSEN	R/W	0h	Internal. Only to be used through TI provided API.
4-3	CH3EN	R/W	0h	Internal. Only to be used through TI provided API.
2-1	CH2EN	R/W	0h	Internal. Only to be used through TI provided API.
0	CH1EN	R/W	0h	Internal. Only to be used through TI provided API.

28.13.2 CH1CMD Register (Offset = 4h) [Reset = 00000000h]

CH1CMD is shown in Table 28-565.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-565. CH1CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
7-3	RESERVED	R	0h	Reserved
2-0	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.

28.13.3 CH2CMD Register (Offset = 8h) [Reset = 00000000h]

CH2CMD is shown in Table 28-566.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-566. CH2CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
7-3	RESERVED	R	0h	Reserved
2-0	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.

28.13.4 CH3CMD Register (Offset = Ch) [Reset = 00000000h]

CH3CMD is shown in Table 28-567.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-567. CH3CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PKTHDR	R/W	0h	Internal. Only to be used through TI provided API.
7-3	RESERVED	R	0h	Reserved
2-0	PARCNT	R/W	0h	Internal. Only to be used through TI provided API.

28.13.5 CH1PAR01 Register (Offset = 14h) [Reset = 00000000h]

CH1PAR01 is shown in Table 28-568.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-568. CH1PAR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR1	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR0	R/W	0h	Internal. Only to be used through TI provided API.

28.13.6 CH2PAR01 Register (Offset = 18h) [Reset = 00000000h]

CH2PAR01 is shown in Table 28-569.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-569. CH2PAR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR1	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR0	R/W	0h	Internal. Only to be used through TI provided API.

28.13.7 CH3PAR01 Register (Offset = 1Ch) [Reset = 00000000h]

CH3PAR01 is shown in Table 28-570.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-570. CH3PAR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR1	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR0	R/W	0h	Internal. Only to be used through TI provided API.

28.13.8 CH1PAR23 Register (Offset = 24h) [Reset = 00000000h]

CH1PAR23 is shown in Table 28-571.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-571. CH1PAR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR3	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR2	R/W	0h	Internal. Only to be used through TI provided API.

28.13.9 CH2PAR23 Register (Offset = 28h) [Reset = 00000000h]

CH2PAR23 is shown in Table 28-572.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-572. CH2PAR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR3	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR2	R/W	0h	Internal. Only to be used through TI provided API.

28.13.10 CH3PAR23 Register (Offset = 2Ch) [Reset = 00000000h]

CH3PAR23 is shown in Table 28-573.

Return to the Summary Table.

Internal. Only to be used through TI provided API.

Table 28-573. CH3PAR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PAR3	R/W	0h	Internal. Only to be used through TI provided API.
15-0	PAR2	R/W	0h	Internal. Only to be used through TI provided API.

28.14 LRFDTXF Registers

Table 28-574 lists the memory-mapped registers for the LRFDTXF registers. All register offset addresses not listed in Table 28-574 should be considered as reserved locations and the register contents should not be modified.

Table 28-574. LRFDTXF Registers

Offset	Acronym	Register Name	Section
0h	TXD	Data to from TXFIFO	Section 28.14.1

Complex bit access types are encoded to fit into small table cells. Table 28-575 shows the codes that are used for access types in this section.

Table 28-575. LRFDTXF Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

28.14.1 TXD Register (Offset = 0h) [Reset = 00000000h]

TXD is shown in Table 28-576.

Return to the Summary Table.

TX FIFO data. When written the register data is pushed to the TX FIFO. When read, data is popped from the TX FIFO

Table 28-576. TXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	TX FIFO data. When written the register data is pushed to the TX FIFO. When read, data is popped from the TX FIFO. When writing or reading this register the access size will determine how many bytes are pushed to or popped from the FIFO. It is possible to push or pop 1,2 or 4 bytes depending on the access being done.

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