GDO Pin Usage

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Keywords

- *CC1100*
- *CC1101*
- *CC1150*
- *CC2500*
- *CC2550*
- *GDO Pin*
- *RXFIFO_OVERFLOW*
- *TXFIFO_UNDERFLOW*

1 Introduction

CC1100, CC1101, and CC2500 have three digital output pins, GDO0, GDO1, and GDO2, which are general control pins configured using `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG`, and `IOCFG2.GDO2_CFG` respectively. There are several different signals that can be monitored on the GDO pins and hence be useful for the MCU controlling the radio. GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CSn is high. It is important to notice that the CC1150 and the CC2550 only have two digital output pins; GDO0 and GDO1.

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2 Abbreviations

CRC	Cyclic Redundancy Check
FIFO	First-In-First-Out
ISR	Interrupt Service Routine
MCU	Micro Controller Unit
SPI	Serial Peripheral Interface

3 IOCFGx = 0x06

This signal is probably the most useful signal related to the packet handler engine. The GDOx pin is asserted when a sync word has been sent / received, and de-asserted at the end of the packet. In RX, the pin will de-assert when address filtering or maximum length filtering leads to a packet being discarded or if the RX FIFO overflows. In TX, the pin will de-assert if the TX FIFO underflows.

3.1 TX when IOCFGx = 0x06

3.1.1 Error Free TX (IOCFGx = 0x06)

Assume transmitting the following packet: 0x06, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06. The radio is configured to use variable packet length mode (PKTCTRL0.LENGTH_CONFIG = 1), CRC insertion is enabled (PKTCTRL0.CRC_EN = 1), and the data rate is 250 kbps.

After the sync word is transmitted (1), 9 more bytes are sent: 1 length byte + 6 payload bytes + 2 CRC bytes. This takes (9 · 8) · (1 / 250000) = 288 [us]. In Figure 1, the GDOx signal is high for about 292 us. The difference between the theoretical value and the measure value is due to internal delays in the signal path. The radio will be in the state determined by MCSM1.TXOFF_MODE after GDOx is de-asserted (2).

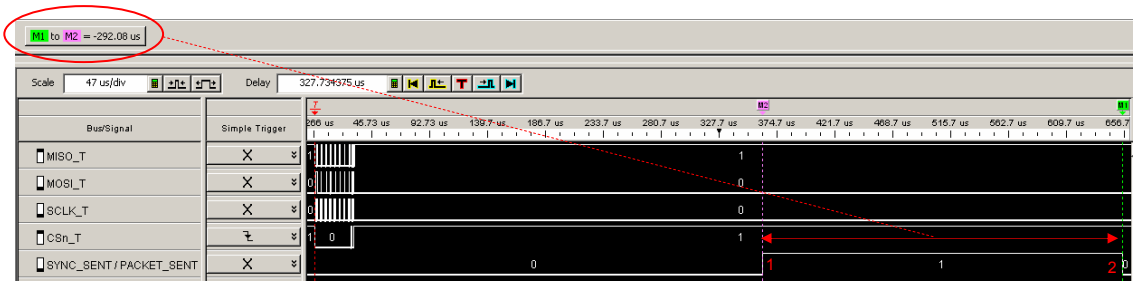

Figure 1. Error Free TX (IOCFGx = 0x06)

3.1.2 TXFIFO_UNDERFLOW (IOCFGx = 0x06)

Assume transmitting the following packet: 0x03, 0x01, 0x02. The radio is configured as described in 3.1.1.

Since variable packet length mode is used, transmitting this packet will make the radio enter the TXFIFO_UNDERFLOW state (the length byte is 3, but there are only two bytes in the payload; 0x01 and 0x02). This means that the GDOx signal will be de-asserted (2) after (3 · 8) · (1 / 250000) = 96 [us] ((1) shows sync transmitted). The only way to get out of TXFIFO_UNDERFLOW state is to issue a SFTX strobe. This will get the radio back to IDLE state, regardless of the MCSM1.TXOFF_MODE setting.

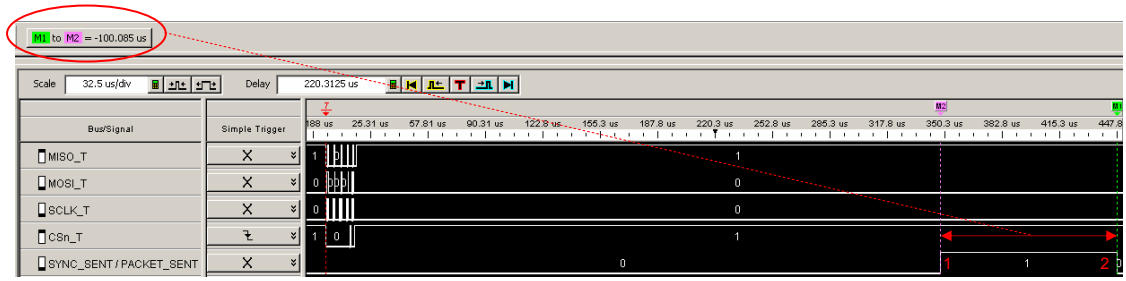

Figure 2. TXFIFO_UNDERFLOW (IOCFGx = 0x06)

3.2 RX when IOCFGx = 0x06

3.2.1 Error Free RX (IOCFGx = 0x06)

Assume receiving the packet transmitted in 3.1.1. As seen in Figure 3, the GDOx signal on the receiver (SYNC RECEIVED / PACKET RECEIVED) is asserted (3) and de-asserted (4) just after the GDOx signal on the transmitter (SYNC SENT / PACKET SENT) is asserted (1) and de-asserted (2). The radio will be in the state determined by MCSM1.RXOFF_MODE after GDOx is de-asserted.

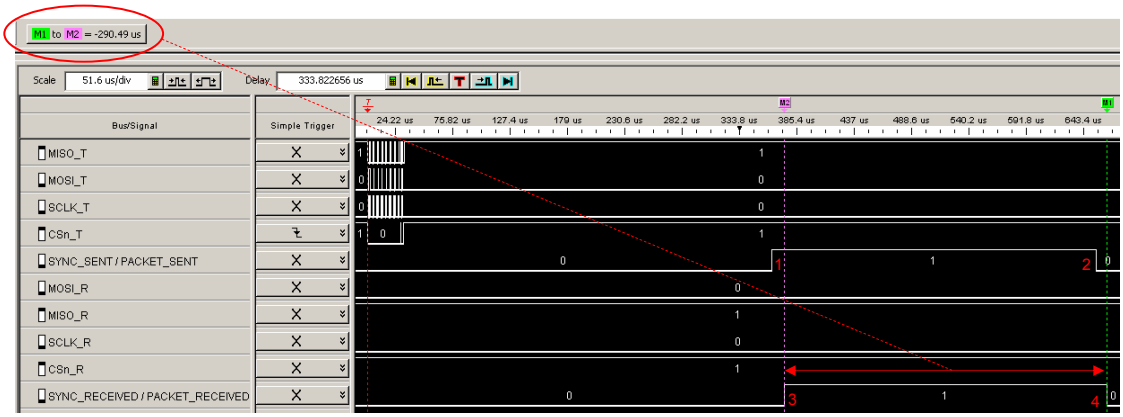

Figure 3. Error Free RX (IOCFGx = 0x06)

3.2.2 RXFIFO_OVERFLOW (IOCFGx = 0x06)

The transmitted packet is still the same as in 3.1.1, but the receiver has been configured to use fixed packet length mode (PKTCTRL0.LENGTH_CONFIG = 0) and the packet length is set to 70 (PKTLEN = 0x46). Sync word is received (3) immediately after the sync word has been transmitted (1). However, when the packet it sent (2), the receiver continues in RX state since it is configured to receive 70 bytes. After 2.15 ms the radio enters RXFIFO_OVERFLOW state (4). It only takes (64 · 8) · (1 / 250000) = 2.048 [ms] to fill up the RX FIFO, but due to some internal buffering, it takes some additional time before RXFIFO_OVERFLOW state is entered. The only way to get out of RXFIFO_UNDERFLOW state is to issue a SFRX strobe. This will get the radio back to IDLE state, regardless of the MCSM1.RXOFF_MODE setting.
Please see the Errata Note for a description of a bug related to the RXFIFO_OVERFLOW state.

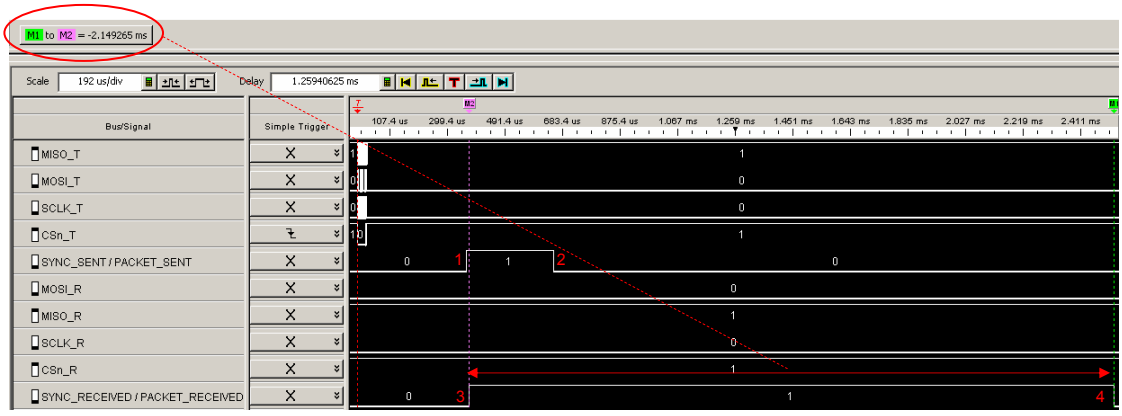

Figure 4. RXFIFO_OVERFLOW (IOCFGx = 0x06)

3.2.3 Address Filtering (IOCFGx = 0x06)

Assume transmitting the following packet: 0x0A, 0x07, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A (the radio settings are the same as in 3.1.1). The receiver have the same radio settings as the transmitter, but in addition it is configured to use address filtering (PKTCTRL1.ADR_CHK = 1 and ADDR = 0x06). When address filtering is enabled, the receiver will interpret the second byte received after the sync word as the address (if fixed packet length mode where used (PKTCTRL0.LENGTH_CONFIG = 0), it would interpret the first byte after sync as the address byte, since the packet would not have a length byte).

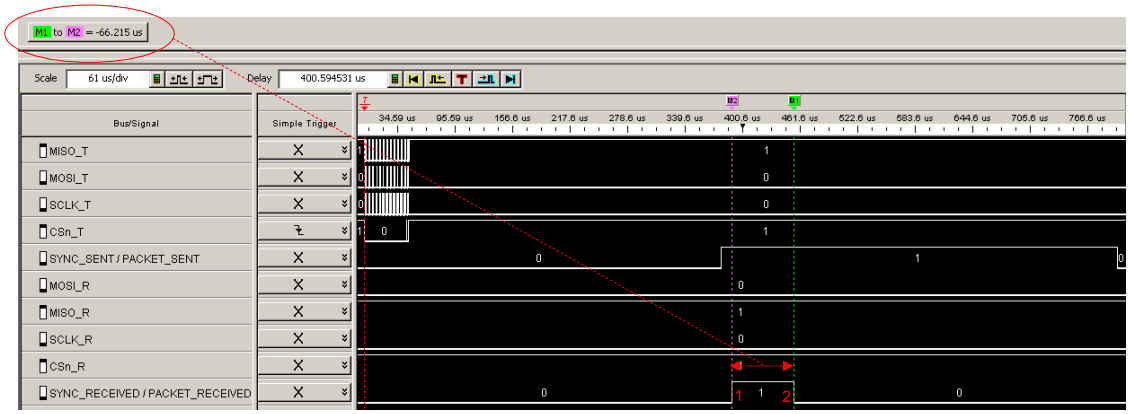

Figure 5. Address Filtering (IOCFGx = 0x06)

Since the receiver has the address 0x06 (ADDR = 0x06) and the second byte received after sync is 0x07, the packet will be discarded and GDOx will de-assert (2). Figure 5 shows that GDOx is de-asserted after 66 us (2 bytes must be received before the address is checked; $(2 \cdot 8) \cdot (1 / 250000) = 64$ [us] ((1) shows sync received). After GDOx is de-asserted, the radio will go back to RX state, regardless of the MCSM1.RXOFF_MODE setting.

3.2.4 Maximum Length Filtering (IOCFGx = 0x06)

If using maximum length filtering (PKTCTRL0.LENGTH_CONFIG = 1 and PKTLEN set to the maximum packet length the radio should accept) the GDOx signal will behave the same way as described in 3.2.3. However, the GDOx pin will be de-asserted (2) after 32 us (and not 64 us) since only the length byte has to be received before the filtering can take place. After the GDOx signal has been de-asserted, the radio will also in this case go back to RX state, regardless of the MCSM1.RXOFF_MODE setting. In Figure 6 ((1) is sync received), the transmitted packet is the same as the one described in 3.2.3. On the receiver, PKTLEN = 0x09 (with PKTLEN ≥ 0x0A, the packet would be received properly).

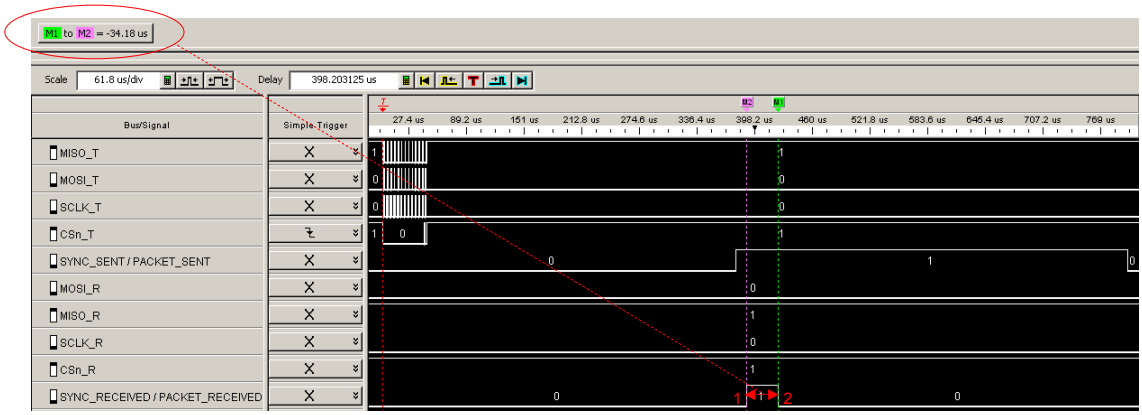

Figure 6. Maximum Length Filtering (IOCFGx = 0x06)

4 IOCFGx = 0x00

This signal is associated with the RX FIFO and is asserted when the RX FIFO is filled at or above the RX FIFO threshold and de-asserted when the RX FIFO is drained below the same threshold. This signal is not valid for CC1150 and CC2550.

Assume the same packet being transmitted as in 3.2.3. On the receiver, FIFOTHR.FIFO_THR = 0 (4 bytes in the RX FIFO) and append status is enabled (PKTCTRL1.APPEND_STATUS = 1). This means that a total of 13 bytes is put in the RX FIFO (1 length byte + 10 data bytes + 2 status bytes). It takes (4 · 8) · (1 / 250000) = 128 [us] after sync word is received (1) until the GDOx pin indicated that there are 4 bytes in the RX FIFO (2). When 10 bytes has been read from the RX FIFO (and there are 3 bytes left), the GDOx pin is de-asserted (3).

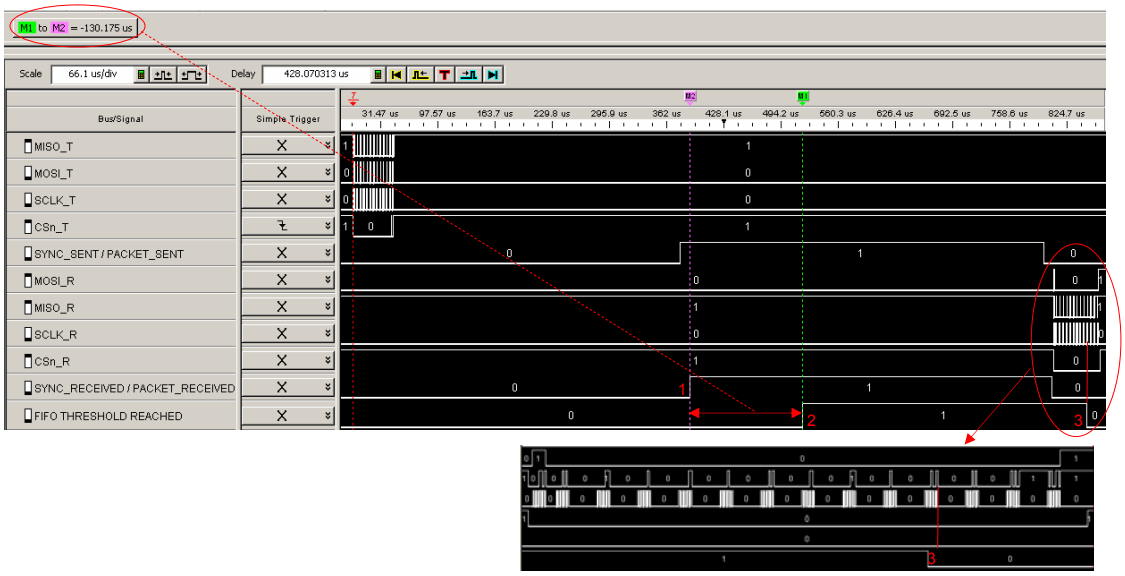

Figure 7. IOCFGx = 0x00

5 IOCFGx = 0x01

This signal is associated with the RX FIFO and is asserted when the RX FIFO is filled at or above RX FIFO threshold or the end of packet is reached. It de-asserts when the RX FIFO is empty. This signal is not valid for CC1150 and CC2550.

Assume transmitting the packet described in 3.2.3. After the sync word is received (1) it takes (4 · 8) · (1 / 250000) = 128 [us] before the RX FIFO threshold is reached (2) (see Figure 8).

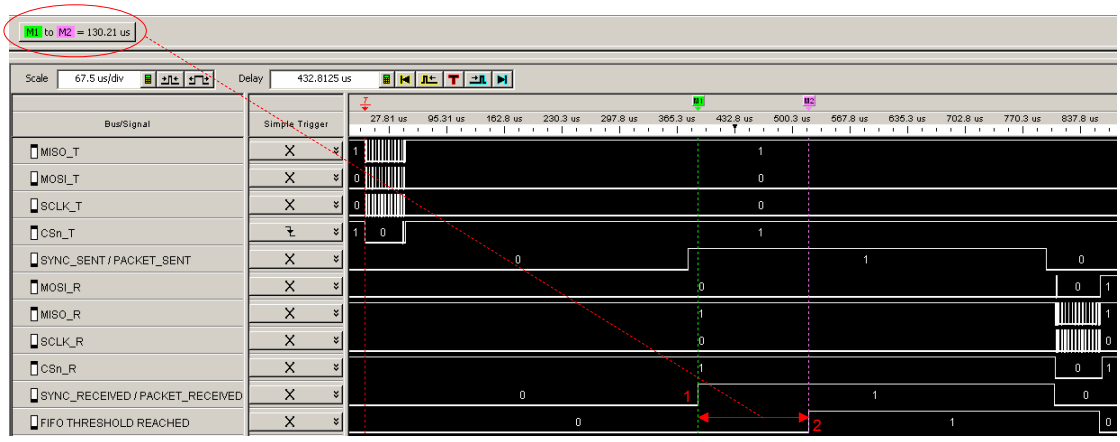

Figure 8. IOCFGx = 0x01 (RX FIFO Filled Above Threshold)

For the transmission showed in Figure 9, the RX FIFO threshold is changed to 16 (FIFOTHR.FIFO_THR = 3). Since only 13 bytes are to be received in the RX FIFO, the GDOx pin is not asserted before the whole packet has been received (1) (same time as the packet received signal is de-asserted (2)).

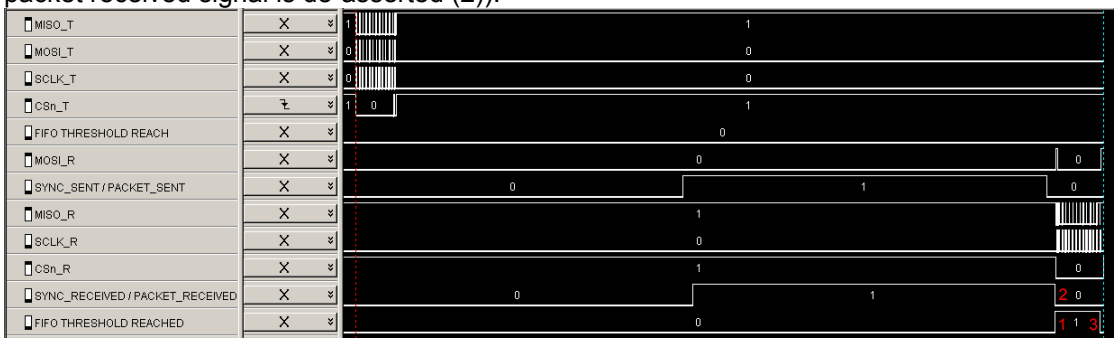

Figure 9. IOCFGx = 0x01 (End of Packet Reached)

The GDOx pin is de-asserted when the RX FIFO is empty (3). It is important to remember that due to a bug related to the RX FIFO one should never empty the RX FIFO before the last byte of the packet has been received (See Errata Notes for CC1100 [1], CC1101 [2], and CC2500 [3]).

6 IOCFGx = 0x02

This signal is associated with the TX FIFO; it is asserted when the TX FIFO is filled at or above the TX FIFO threshold and is de-asserted when the TX FIFO is below the same threshold. Assume writing 11 bytes to the TX FIFO. FIFOTHR.FIFO_THR = 14, meaning that there will be five bytes in the TX FIFO when the signal is asserted (1). The signal is de-asserted (2) when the number of bytes in the TX FIFO goes below five. To illustrate this, the TXBYTES register was read just after the signal was de-asserted and it shows that there are four bytes in the TX FIFO (3).

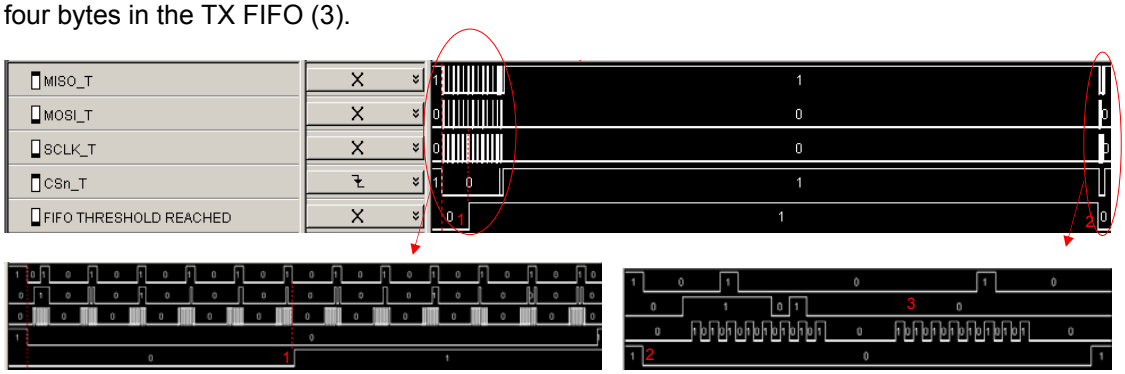

Figure 10. IOCFGx = 0x02

7 IOCFGx = 0x03

This signal is associated with the TX FIFO; it asserts when TX FIFO is full and de-asserts when the TX FIFO is drained below the TX FIFO threshold. If FIFOTHR.FIFO_THR = 0 (TX FIFO threshold = 61 bytes) and 64 bytes are written to the TX FIFO, the GDOx signal will behave as shown in Figure 11; It asserts after 64 bytes have been written to the TX FIFO (1) and de-asserts when there are less than 61 bytes left (2). Reading the TXBYTES register after the GDOx was de-asserted shows that there are 60 bytes left in the TX FIFO (3).

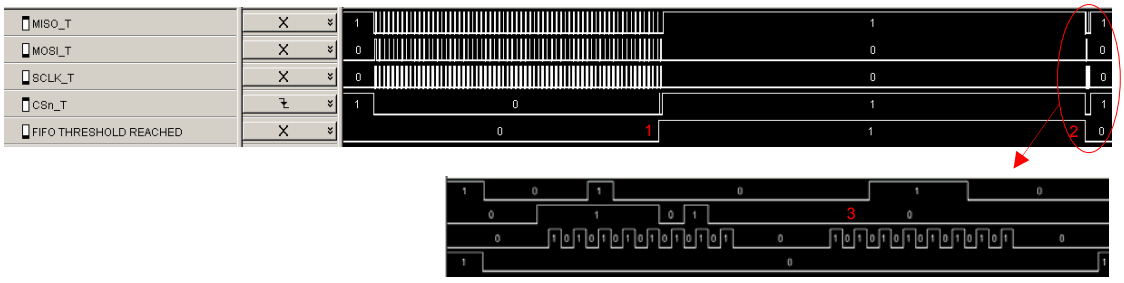

Figure 11. IOCFGx = 0x03

8 IOCFGx = 0x07

This signal is asserted when a packet has been received with CRC OK and is de-asserted when the first byte is read from the RX FIFO. The signal is not valid for CC1150 and CC2550. Note that on the CC2500, this signal is only valid when PKTCTRL0.CC2400_EN = 1. Figure 12 shows an 11 bytes long packet being transmitted. (1) shows sync sent and (2) shows packet sent. The GDOx signal is asserted (3) when the packet has been received (4) and is de-asserted after the first byte is read from the RX FIFO (5).

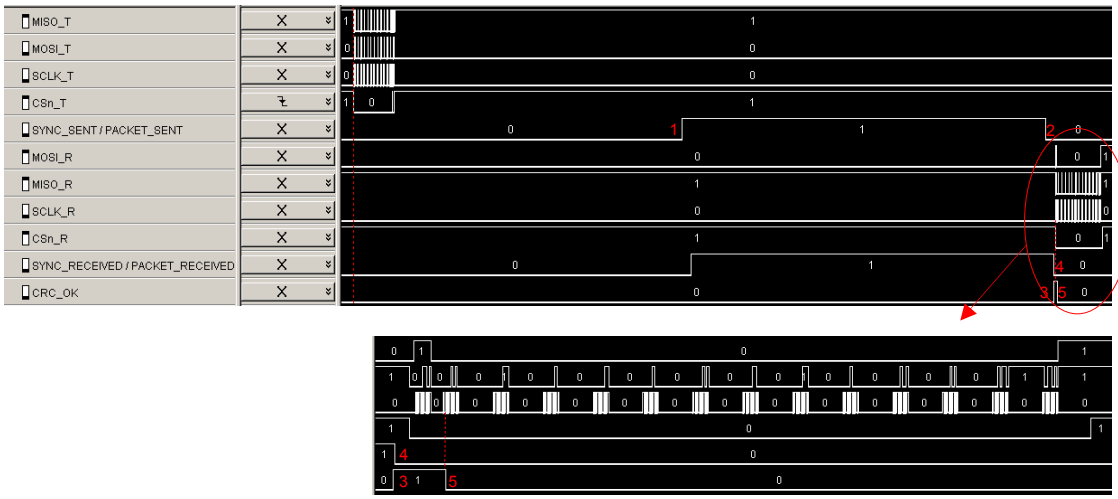

Figure 12. IOCFGx = 0x07

Assume the following scenario: The GDOx pin is used to generate an interrupt when a packet with CRC OK has been received. This means that if a faulty packet is being received, no interrupt is generated and hence the faulty packet will be in the RX FIFO, potentially causing the RX FIFO to overflow. A solution would be to use the CRC auto flush function (PKTCTRL1.CRC_AUTOFLUSH = 1), which will flush the entire RX FIFO if the CRC check fails. The problem is that for the CRC filtering to work, PKTCTRL0.CC2400_EN must be 0. This means that using this approach will only work on the CC1100 where this GDOx signal is valid for both PKTCTRL0.CC2400_EN = 0 and PKTCTRL0.CC2400_EN = 1. It is, however, still possible to use the CRC OK signal on the CC2500, but it should not be used as the single source of interrupt to an MCU. One way of using this signal is to use sync received / packet received (IOCFGx = 0x06) to generate an interrupt on falling edge and then, in the ISR, check if the GDOx pin, indicating CRC OK, is asserted or not. If the GDOx pin is not asserted, the received packet is faulty and the RX FIFO should be flushed by issuing an SFRX strobe. Remember that the SFRX strobe should only be issued when the radio is in RXFIFO_OVERFLOW state or when in IDLE state.

9 References

[1] CC1100 Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc1100.pdf)

[2] CC1101 Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc1101.pdf)

[3] CC2500 Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc2500.pdf)

10 General Information

10.1 Document History

Revision	Date	Description/Changes
SWRA121A	2007.10.22	Added reference table. Removed logo from header. Added CC1101
SWRA121	2006.12.18	Initial release.

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