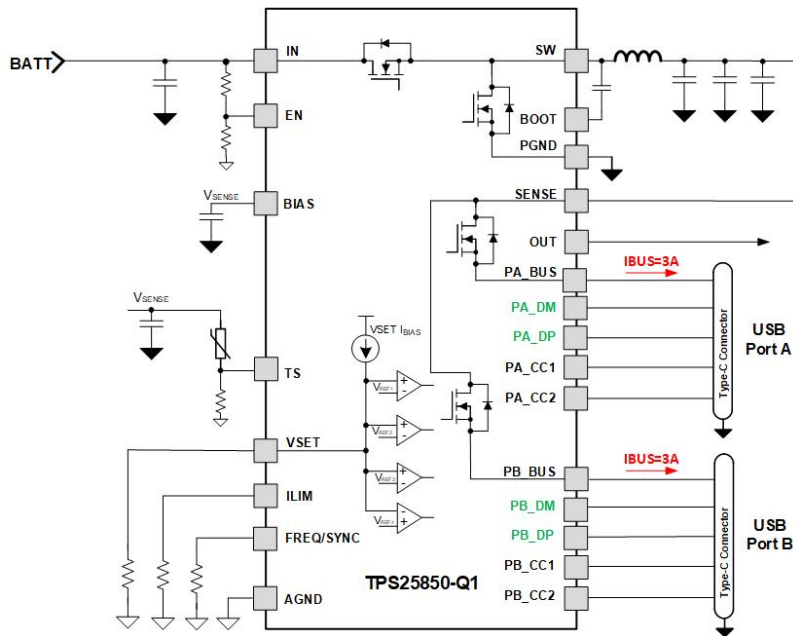


CISPR 25 Class 5 400-kHz-Rated 30-W Automotive Dual USB Type-C™ Charger Reference Design

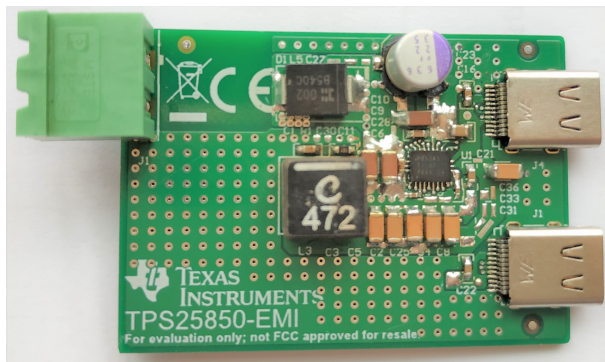


Description

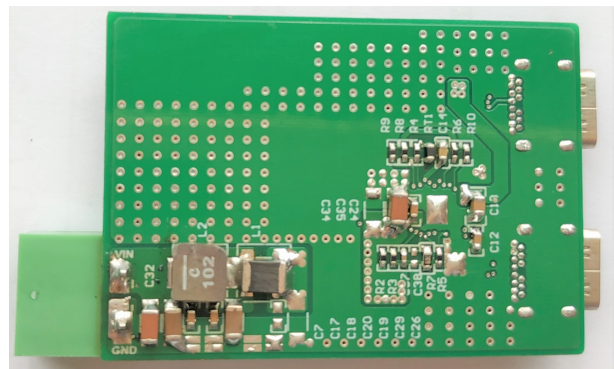
This reference design is an EMI-optimized design for automotive USB Type-C™ charger with dual 15-W output. The TPS25850-Q1 is used as a DC/DC regulator and port controller. The switching frequency is 400 kHz. The front-end filter is designed and PCB layout is optimized to pass stringent CISPR 25 Class 5 Conducted Electromagnetic Interference (EMI) standards. This reference design has already been tested to CISPR 25 Class 5 conducted EMI standards, which accelerates customer design time.



Block Diagram



Top



Bottom

1 Test Prerequisites

1.1 Design Requirements

Table 1-1. Design Requirements

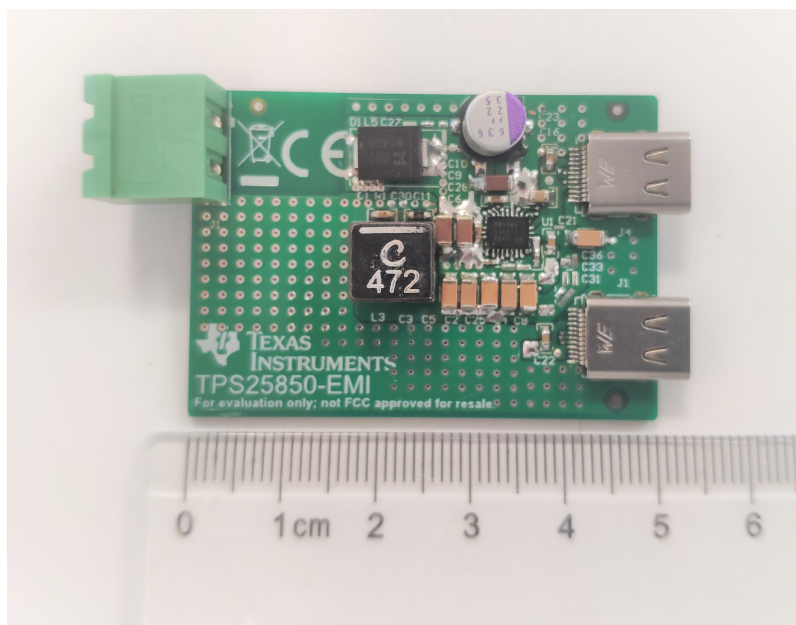
Parameter	Specifications
Input Voltage	13.5 Vdc
PA_BUS Output Voltage	5.17 Vdc
PA_BUS Maximum Output Current	3 A
PB_BUS Output Voltage	5.17 Vdc
PB_BUS Maximum Output Current	3 A
Switching Frequency	400 kHz

1.2 Required Equipment

- Multi-meter (current): Fluke 287C
- Multi-meter (voltage): Fluke 287C
- DC Source: Chroma 62006P-100-25
- E-Load: Chroma 63103A module
- Oscilloscope: Tektronix DPO4104B
- Electrical Thermography: Fluke TiS55
- Thermal Data Acquisition: Agilent 34970A

1.3 Dimensions

The dimension of this board is 50mm (length)*35mm (width)*10mm (height, ignore J1).


Figure 1-1. Dimension

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in the following figure.

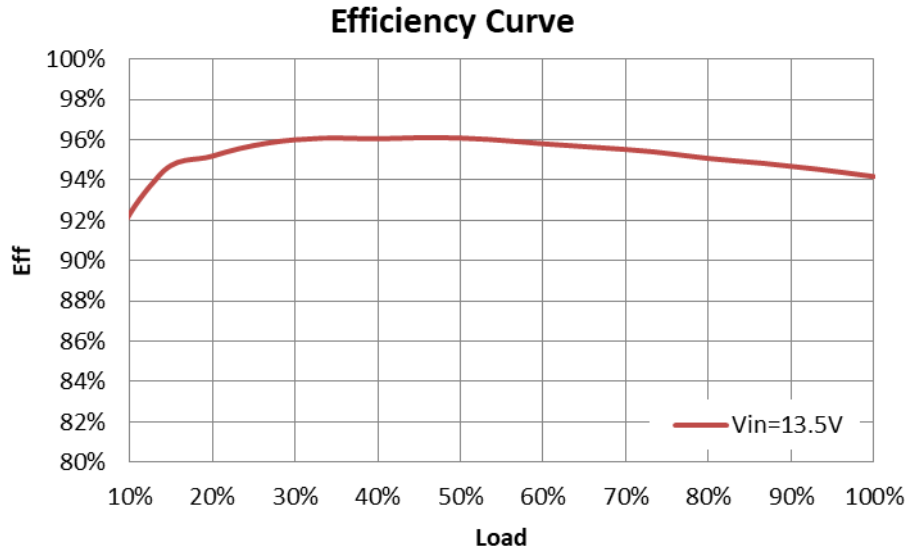


Figure 2-1. Efficiency graph

2.2 Efficiency Data

Efficiency data is shown in the following table.

VIN (V)	IIN (A)	VPA_BUS (V)	IPA_BUS (A)	VPB_BUS (V)	IPB_BUS (A)	Eff
13.497	0.013	5.1726	0	5.1728	0	0.00%
13.474	0.174	5.1749	0.2	5.1755	0.2	88.30%
13.464	0.327	5.1791	0.4	5.1802	0.4	94.12%
13.448	0.486	5.1841	0.6	5.1856	0.6	95.20%
13.432	0.645	5.1889	0.8	5.1909	0.8	95.85%
13.415	0.806	5.1935	1	5.1959	1	96.09%
13.407	0.969	5.1981	1.2	5.201	1.2	96.06%
13.381	1.133	5.2026	1.4	5.2061	1.4	96.12%
13.363	1.299	5.2071	1.6	5.2111	1.6	96.03%
13.346	1.468	5.2116	1.8	5.2167	1.8	95.81%
13.327	1.638	5.2161	2	5.221	2	95.62%
13.308	1.81	5.2204	2.2	5.2259	2.2	95.41%
13.289	1.986	5.2248	2.4	5.2308	2.4	95.08%
13.27	2.16	5.2243	2.6	5.2308	2.6	94.84%

VIN (V)	IIN (A)	VPA_BUS (V)	IPA_BUS (A)	VPB_BUS (V)	IPB_BUS (A)	Eff
13.249	2.336	5.2214	2.8	5.2285	2.8	94.54%
13.229	2.515	5.2185	3	5.2262	3	94.18%

2.3 Load Regulation

Load regulation is shown in the following figure.

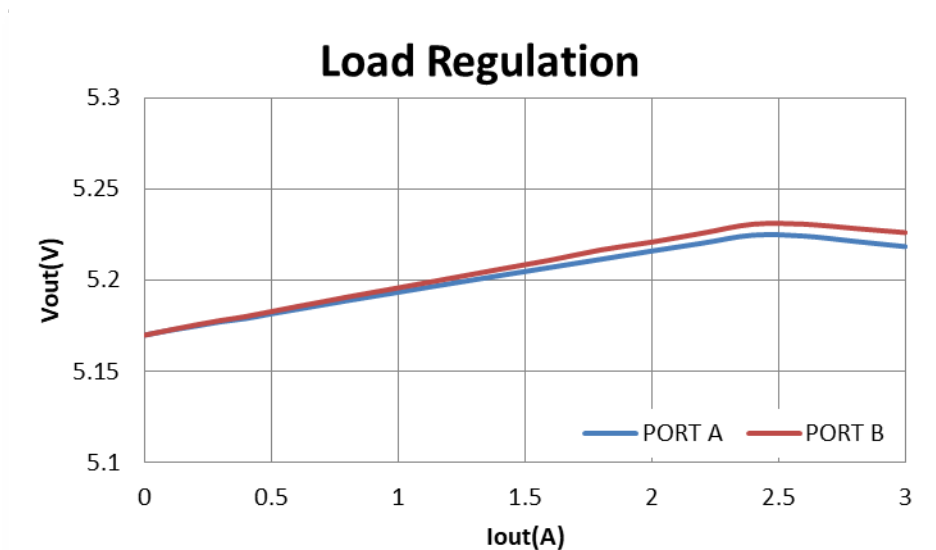


Figure 2-2. Load Regulation

2.4 Thermal Images

Thermal images are shown in the following figures. The ambient temperature is 25°C. The thermal image is taken at the steady state with 13.5 V in and all outputs at a full load of 5.17 V and 3 A.

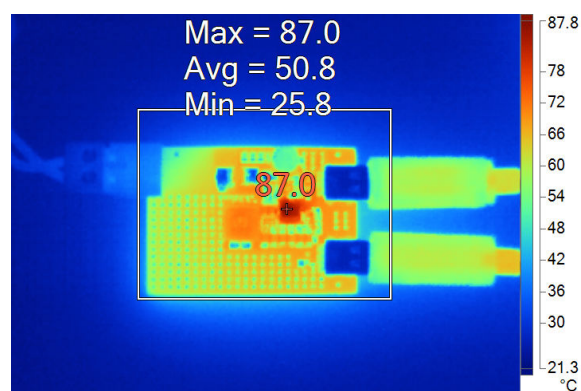


Figure 2-3. Top side

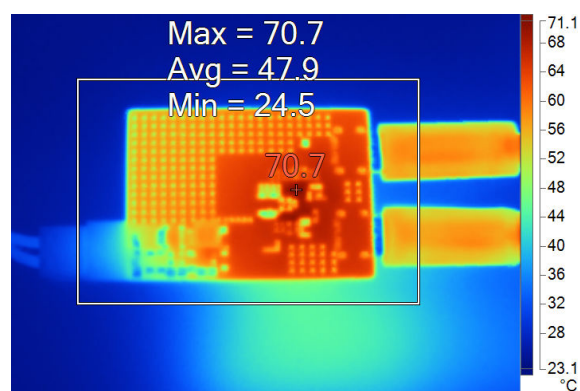
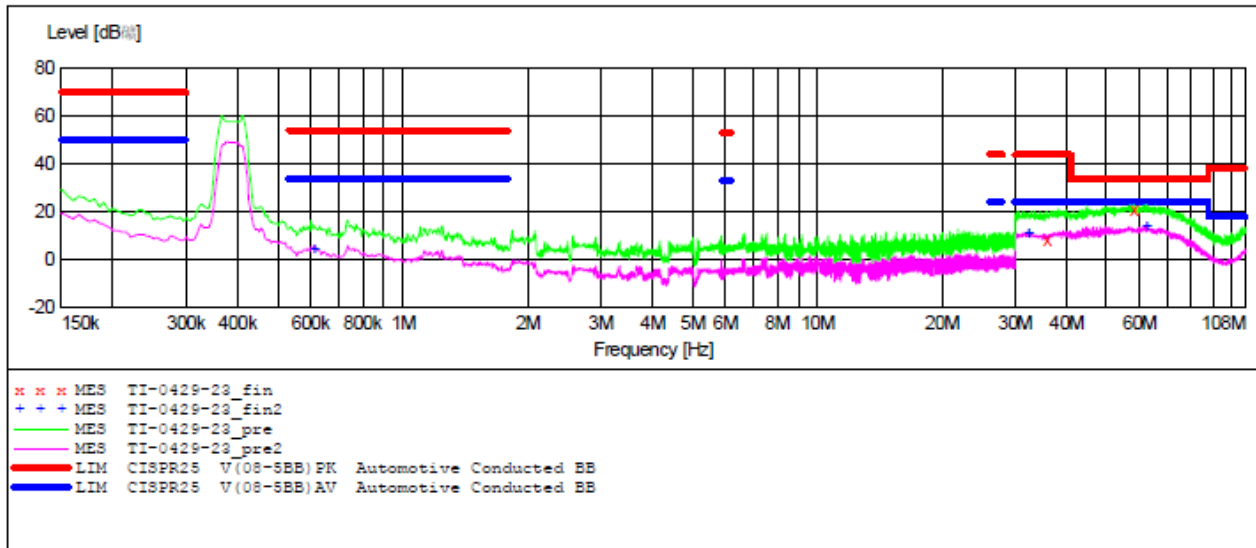


Figure 2-4. Bottom side

2.5 EMI

The conducted emissions are tested to the CISPR 25 class 5 standards. The CISPR 25 class 5 compliance was achieved without a common-mode choke or shielding. EMI is shown in the following figure.



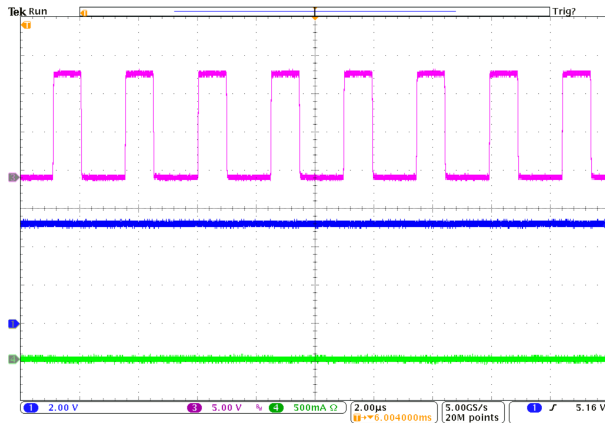
Green: Peak Detection Result
 Purple: Average Detection Result
 Red: CISPR 25 Class 5 Peak Limits
 Blue: CISPR 25 Class 5 Average Limits

Figure 2-5. EMI performance from 150kHz to 108MHz.

3 Waveforms

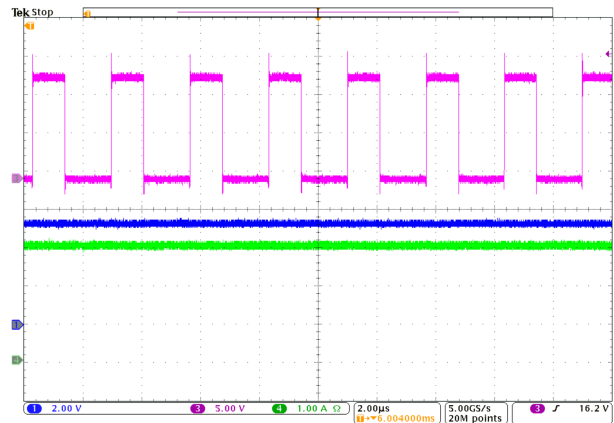
3.1 Switching

Switching behavior is shown in the following figures.



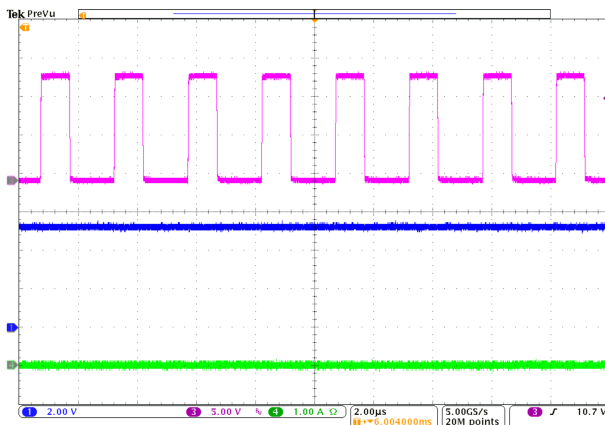
CH1: V_{PA_BUS} CH3: V_{SW} CH4: I_{PA_BUS}

Figure 3-1. PA_BUS 13.5V input, 5.17V no-load



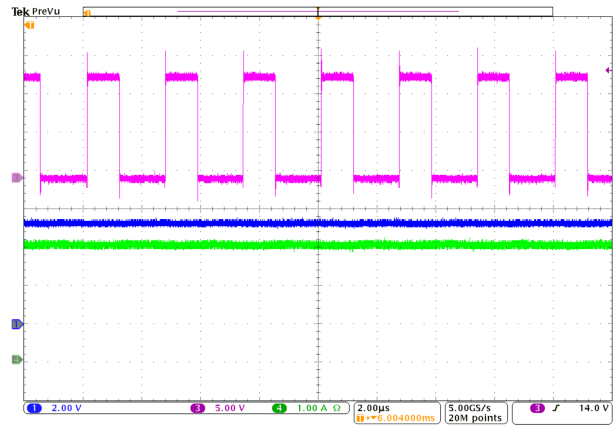
CH1: V_{PA_BUS} CH3: V_{SW} CH4: I_{PA_BUS}

Figure 3-2. PA_BUS 13.5V input, 5.17V 3A load



CH1: V_{PB_BUS} CH3: V_{SW} CH4: I_{PB_BUS}

Figure 3-3. PB_BUS 13.5V input, 5.17V no-load

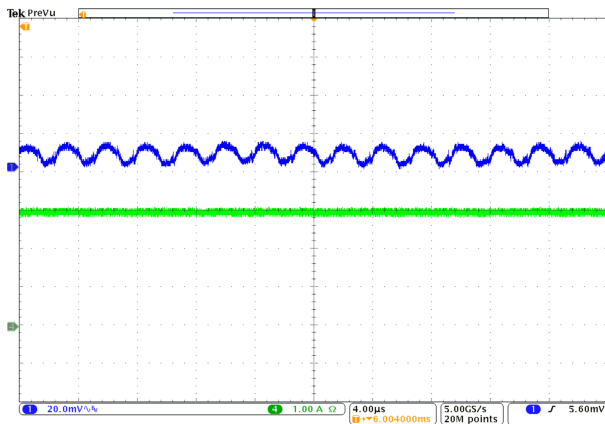


CH1: V_{PB_BUS} CH3: V_{SW} CH4: I_{PB_BUS}

Figure 3-4. PB_BUS 13.5V input, 5.17V 3A load

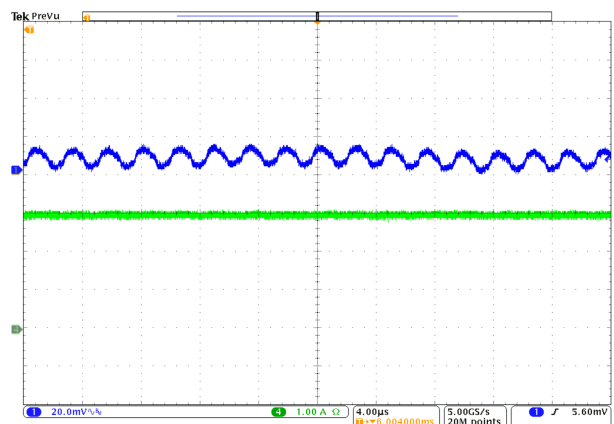
3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.



CH1: VPA_BUS, CH4: IPA_BUS

Figure 3-5. PA_BUS 13.5V input, 5.17V 3A load

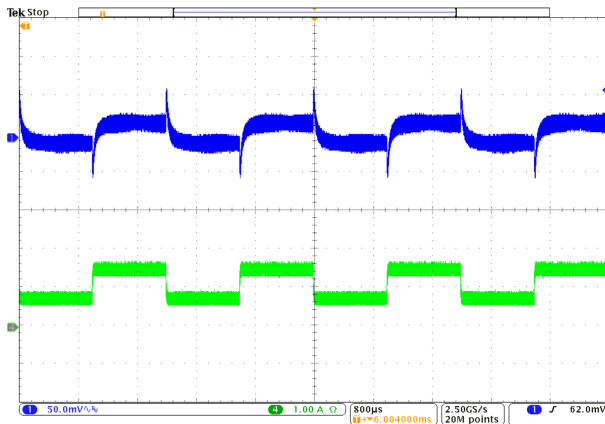


CH1: VPB_BUS, CH4: IPB_BUS

Figure 3-6. PB_BUS 13.5V input, 5.17V 3A load

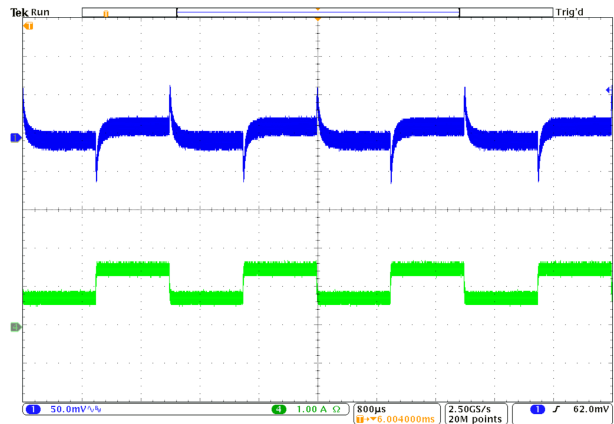
3.3 Load Transients

Load transient response is shown in the following figures.



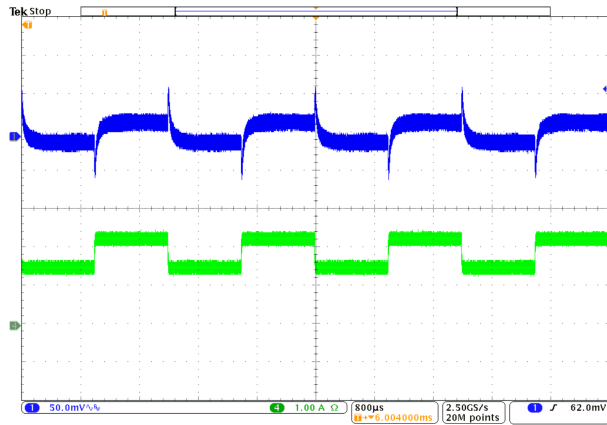
CH1: VPA_BUS, CH4: IPA_BUS

Figure 3-7. PA_BUS 13.5V input, 0.75A->1.5A



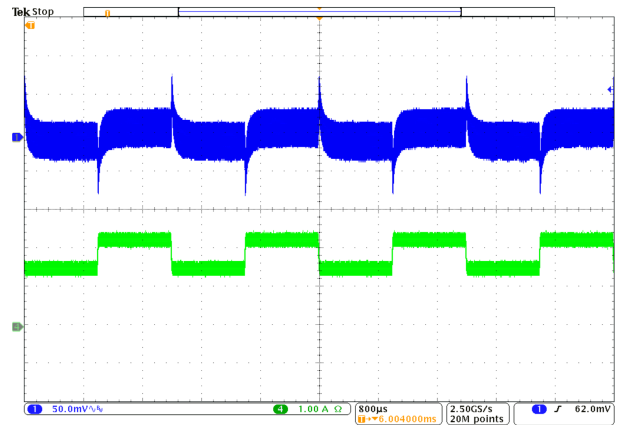
CH1: VPB_BUS, CH4: IPB_BUS

Figure 3-8. PB_BUS 13.5V input, 0.75A->1.5A



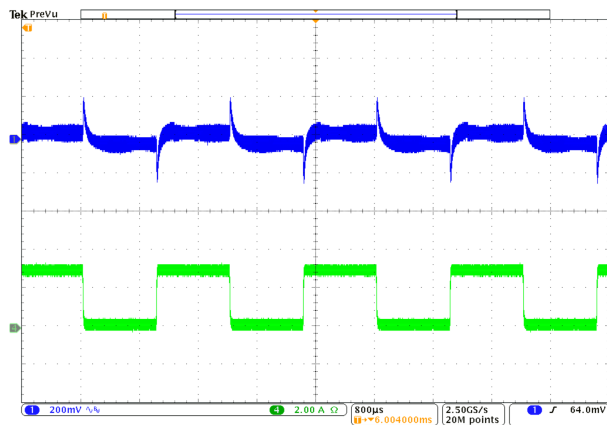
CH1: V_{PA_BUS} CH4: I_{PA_BUS}

Figure 3-9. PA_BUS 13.5V input, 1.5A->2.25A



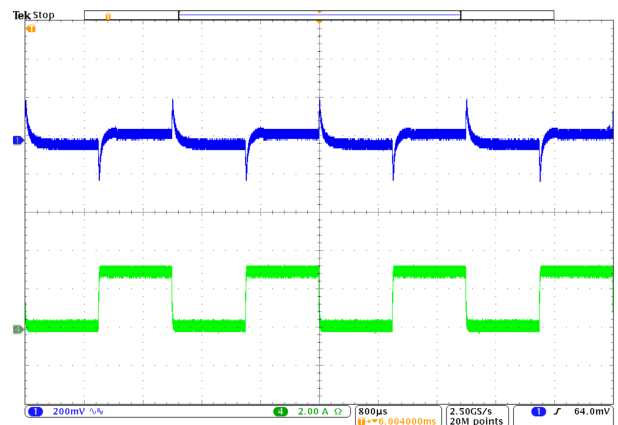
CH1: V_{PB_BUS} CH4: I_{PB_BUS}

Figure 3-10. PB_BUS 13.5V input, 1.5A->2.25A



CH1: V_{PA_BUS} CH4: I_{PA_BUS}

Figure 3-11. PA_BUS 13.5V input, 0.15A->3A



CH1: V_{PB_BUS} CH4: I_{PB_BUS}

Figure 3-12. PB_BUS 13.5V input, 0.15A->3A

3.4 Start-up Sequence

Start-up behavior is shown in the following figures.

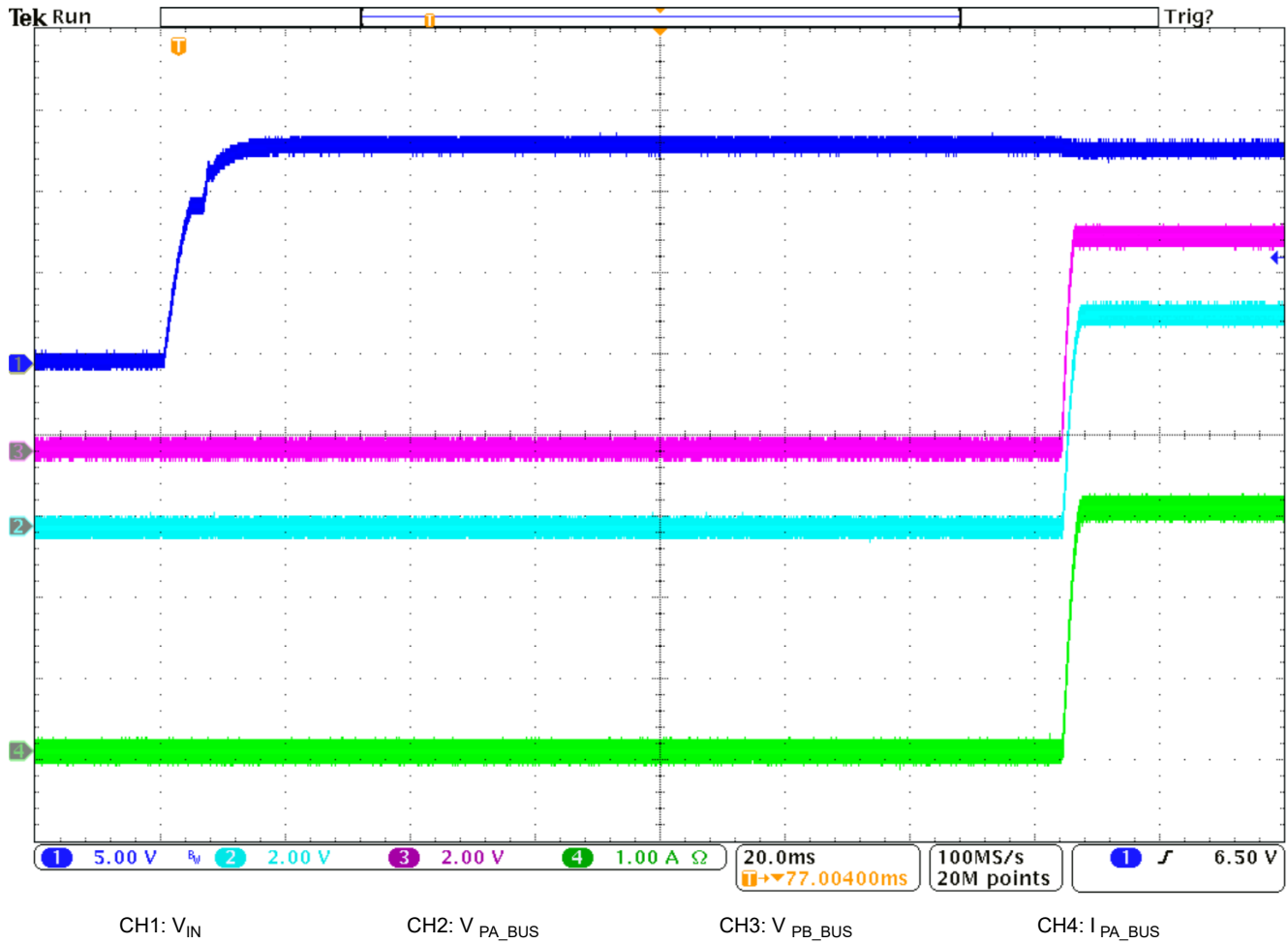


Figure 3-13. Power on

3.5 Undervoltage Protection

Undervoltage protection is shown in the following figures.

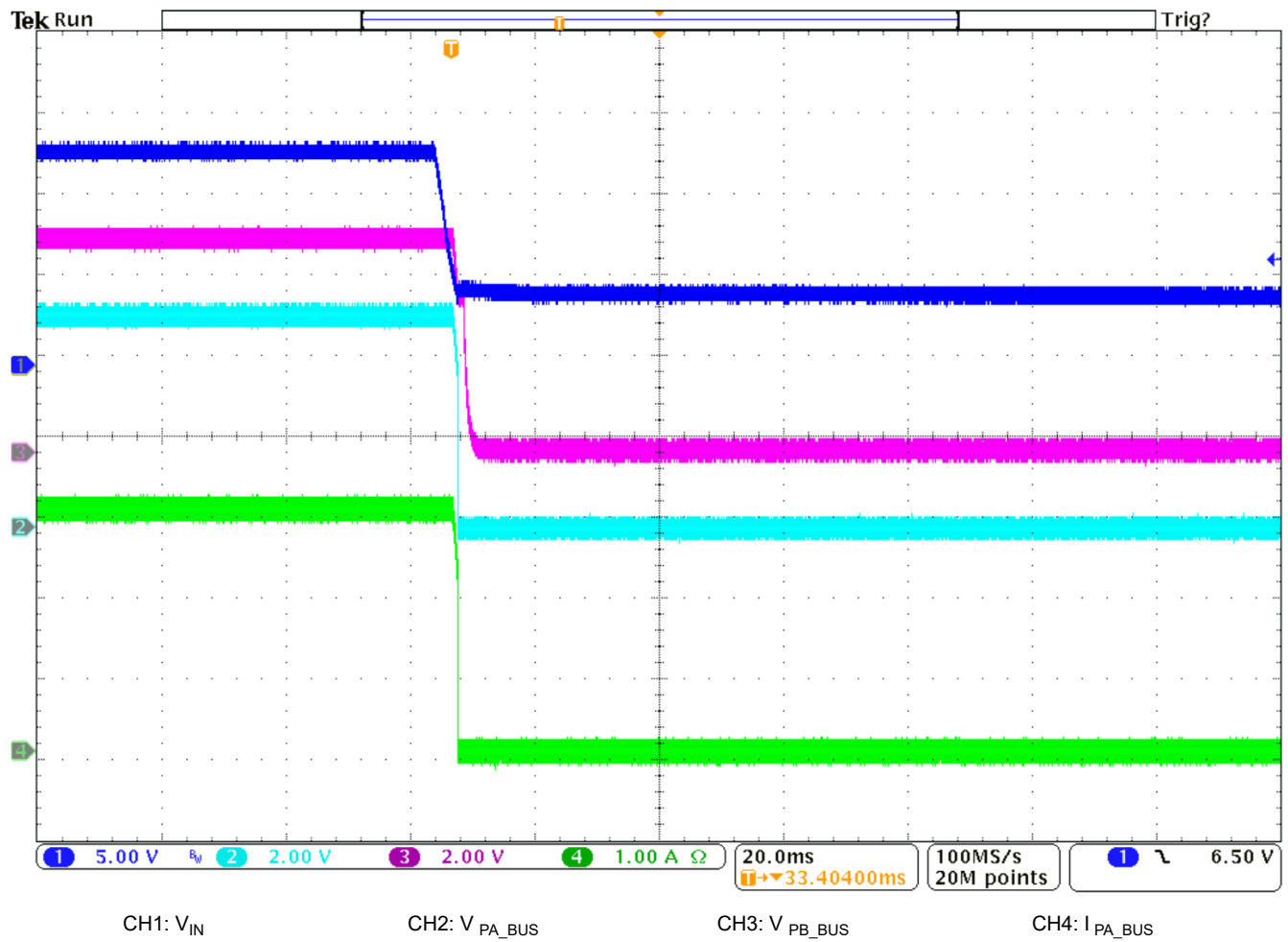


Figure 3-14. Power off

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