TI Designs
Interface to an EnDat 2.2 Position Encoder

TEXAS INSTRUMENTS

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Design Resources

|	
TIDA-00172	Tool Folder Containing Design Files
SN65HVD78	Product Folder
TPS54040A	Product Folder
TPS24750	Product Folder
LMZ14201	Product Folder
TLV70025/18	Product Folder
SN74AVC8T245	Product Folder

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Design Features

- Meets HEIDENHAIN EnDat 2.2 Clock Frequency of 16 MHz up to 20-m and 8 MHz up to 100-m Cable Length
- 3.3-V Supply RS-485 Transceiver with IEC-ESD
- Wide Input (17 to 30-V DC), High-Efficiency (>85%) DC/DC Power Supply for Encoder
- Configurable Encoder Supply Voltage 3.6 to 14 V, Default 8 V, 200 mA, Lowest Ripple (<20 mVpp)
- Encoder Power Supply Protected Against Overcurrent, Overpower, Overvoltage and Undervoltage
- Power Fault Feedback with Disconnect
- Option to Shutdown Encoder Power Supply in Case of Fault or to Save Power When No Encoder is Connected
- Configurable I/O Voltage 3.3-V, 2.5-V, or 1.8-V I/O Interface to Processors like Sitara AM4x for EnDat 2.2 Master
- Meets EMC-Immunity Requirements for ESD, EFT, and Surge According to IEC61800-3

Featured Applications

- Servo Drives, Position Control, AC Drives
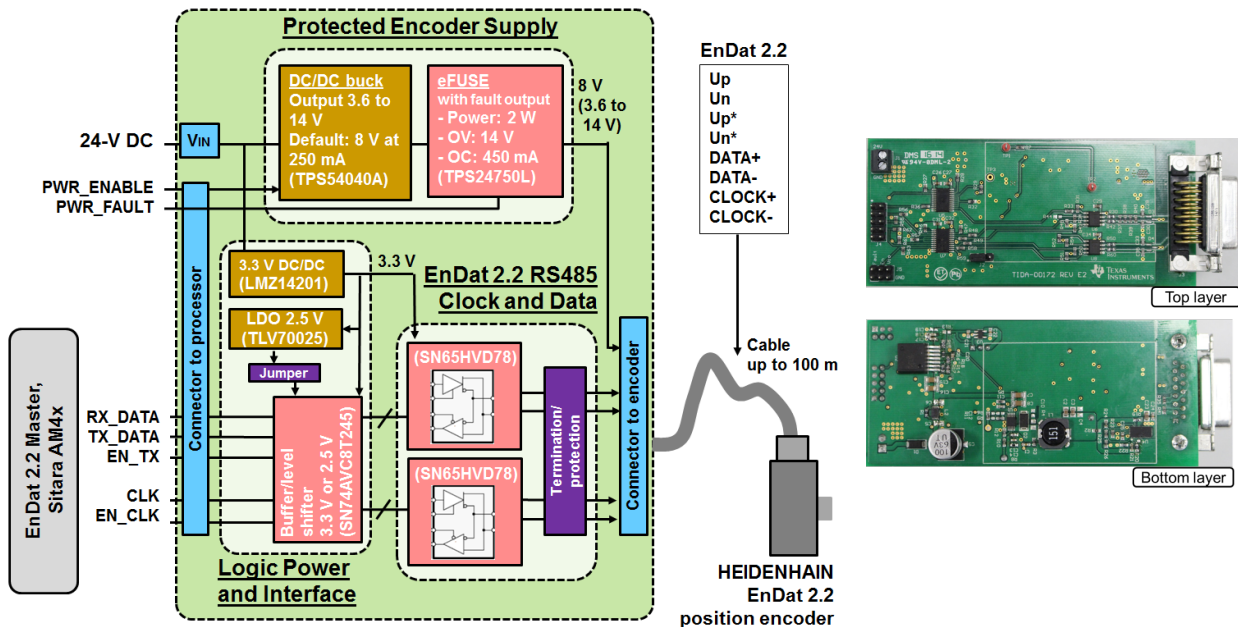
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1 System Description

Industrial drives, like servo drives, require accurate, high-reliable, and low-latency position feedback. A simplified system block diagram of a servo drive using an absolute position encoder with EnDat 2.2 bidirectional digital interface is shown in Figure 1.

The EnDat 2.2 interface from HEIDENHAIN is a digital, bidirectional interface standard for position or rotary encoders. The interface transmits position values or additional physical quantities and allows read out from and write to the encoder's internal memory. The type of data transmitted like absolute position, turns, temperature, parameters, diagnostics, and so on is selected through mode commands that the subsequent electronics, often referred to as EnDat 2.2 Master, sends to the encoder. The EnDat 2.2 interface is a pure serial digital interface based on RS-485 standard. The EnDat 2.2 interface is also suited for safety-related applications up to SIL 3.
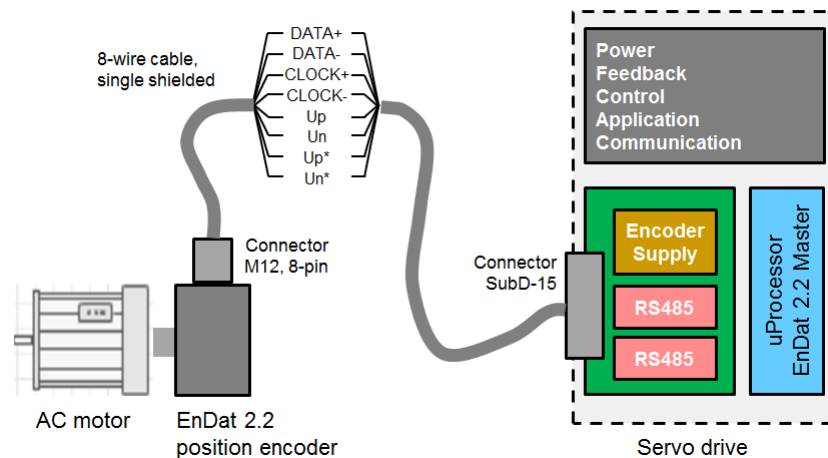

Figure 1. Industrial Servo Drive with Endat 2.2 Position Encoder Interface

The position encoder with EnDat 2.2 is connected to the subsequent electronics in the servo drive through a single, 8-wire shielded cable, as shown in Figure 1. The device only requires four signal lines. Two lines are for the bidirectional differential data (DATA+ and DATA-) and are transmitted in half-duplex mode. The other two lines are for the differential clock signal (CLOCK+ and CLOCK-). From the remaining wires, two wires are used for the encoder power supply. The other two wires are used for battery buffering or for parallel power supply lines to reduce the cable's losses.

EnDat 2.2 specifies a differential line transmitter and receiver according to EIA standard RS-485 for the differential signals CLOCK+, CLOCK-, DATA+, and DATA-. The clock frequency is variable. The maximum clock frequency depends on the cable length, as outlined in Figure 2.
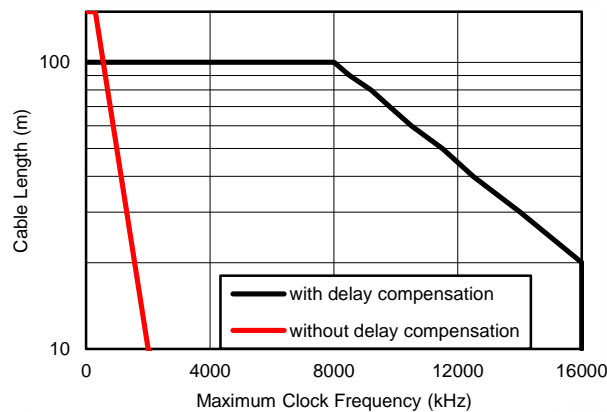

Figure 2. Maximum Clock Frequencies Versus Cable Length (Logarithmic Scale) for Endat 2.2

With propagation-delay compensation in the EnDat 2.2 Master, the clock frequency can be from 100 kHz up to 16 MHz, and up to 100 m cable length with 8 MHz. Use of HEIDENHAIN cables is required.

The data is transmitted and received synchronous to the clock signal, which is generated by the EnDat 2.2 Master. On the EnDat 2.2 Master, the transmit data changes on the falling edge clock edge. Without delay compensation on the Master, the receive data is latched on the rising clock edge. The clock remains high when there is neither data transmitted nor data received.

This TI design implements a hardware interface solution for the subsequent electronics typically implemented in the servo drive, to which the digital encoder is connected to. A simplified block diagram of the TI design is shown in Figure 3.

The major building blocks are the protected power supply for the encoder and the RS-485 transceivers including line termination and EMC protection. An auxiliary power supply and logic level interface with adjustable I/O voltage level is provided to connect to a subsequent microprocessor like Sitara, Delfino, Hercules, or FPGA, which would run the EnDat 2.2 master protocol stack.
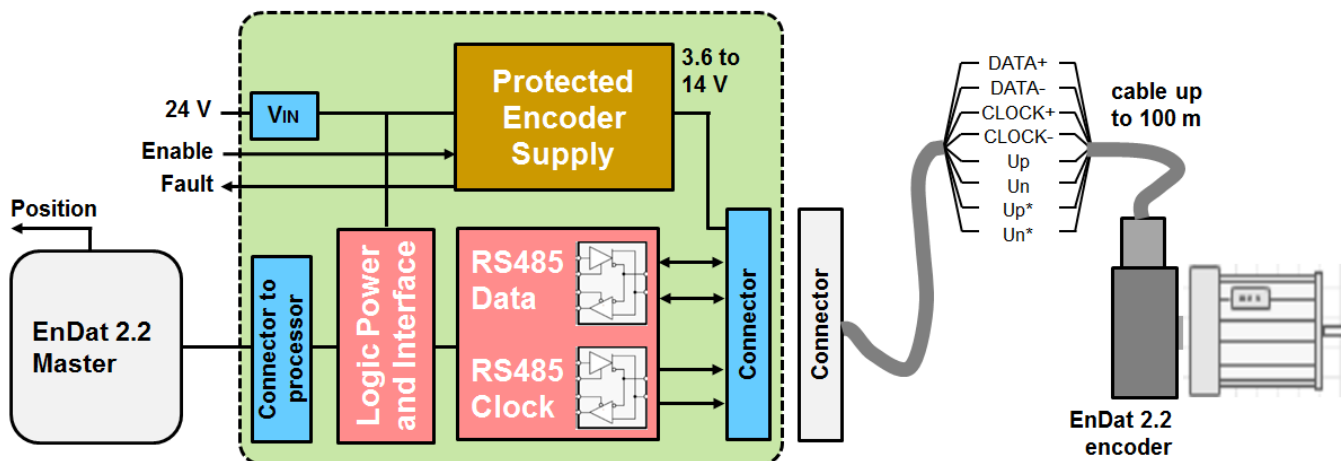

Figure 3. TIDA-00172 Simplified System Block Diagram

2 Design Features

A subsequent electronics as part of a servo drive, which interfaces to an EnDat 2.2 encoder, needs to be at least designed to meet these specifications:

- EnDat 2.2 RS-485 PHY
- EnDat 2.2 Master (communication protocol, not part of this TI design)
- EnDat 2.2 encoder power supply specification
- IEC 61800-3: EMC requirements and specific test methods applicable in adjustable speed, electrical power drive systems

2.1 RS-485 Communication Interface and Logic I/O

A simplified block diagram of the RS-485 communication and logic interface to an EnDat 2.2 master is shown in Figure 4. It consists of the RS-485 transceiver section for the EnDat 2.2 clock and data signals and an optional buffer and level shifter to support lower than 3.3-V I/O voltage level (for example, 2.5-V or 1.8-V I/O).
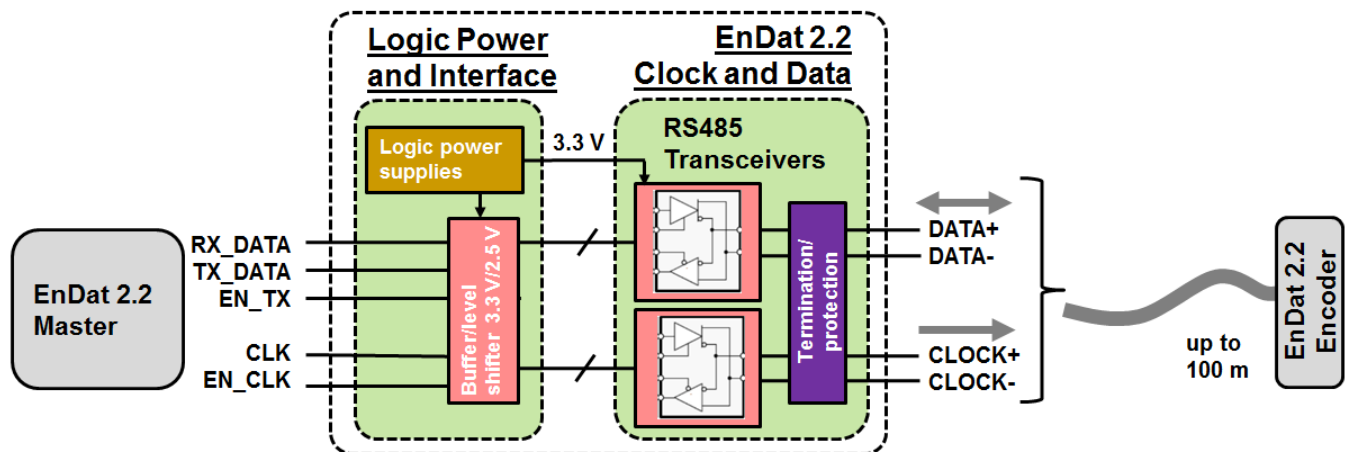

Figure 4. Block Diagram RS-485 and Logic Interface to EnDat 2.2 Master

RS-485 Transceivers

The differential DATA+ and DATA- signals are bidirectional half-duplex, and the RS-485 transceiver is configured in directional mode with DE and /RE signals connected together. The differential CLOCK+ and CLOCK- signals are unidirectional and are outputs of the subsequent electronics. The default state is HIGH. To support external fault conditions, the RS-485 clock transceiver can be disabled and put into an HIZ state. A logic level signal EN_TX_CLOCK is provided.

The minimum baud rate of the RS-485 transceiver should be at least 32 Mbps to support the 16-MHz clock frequency. The RS-485 transceiver should be capable of driving cable length up to 100 m at 8 MHz. The propagation delay of the driver and receiver should be low enough to support the 2-MHz clock frequency for EnDat 2.2 without delay compensation.

To minimize voltage rails, a 3.3-V supply RS-485 transceiver with 5-V tolerant I/O and low quiescence power has been selected. Due to 3.3-V I/O, the transceiver can connect directly to a processor.

Optional Buffer and Level Shifter

An optional voltage buffer and level shifter allows connection to other than 3.3-V I/O.

Table 1. RS-485 Communication and I/O Design Features

DESIGN FEATURES	ENDAT 2.2	TIDA-00172
Maximum clock frequency	16 MHz	25 MHz
Support 8-MHz clock frequency up to 100-m cable length	8 MHz at 100 m	8 MHz at 100 m
Safety option to disable (HIZ) both clock and data outputs	–	Yes
3.3-V supply voltage	–	Yes
Option to change digital I/O voltage from 3.3 V to 2.5 V or 1.8 V	–	Yes

2.2 Protected Encoder Power Supply

The protected encoder power supply is split into two functional blocks: A DC/DC buck converter and an eFUSE, as shown in Figure 5.
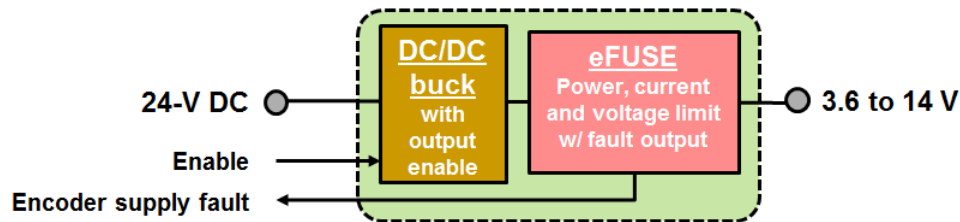

Figure 5. Block Diagram of the Protected Encoder Power Supply

The protected encoder power supply is designed to meet HEIDENHAIN's specification for EnDat 2.2 encoders. The 24-V input voltage is derived from an isolated 24-V power supply (PELV). Thanks to the eFUSE, the design can also be used in accordance with DIN EN 61010-1, where power must be supplied from a secondary circuit (in this design, the DC/DC buck converter), with current or power limitation as per DIN EN 61010-1:2011-07, section 9.4.

2.2.1 DC/DC Buck

The encoders require a stabilized DC voltage, which is measured at the encoder terminals. An EnDat 2.2 encoder is specified with an expanded power supply range from 3.6 to 14 V.

This expanded power supply range allows for design of the power supply at the subsequent electronics with enough headroom (for example, 8 V at 250 mA) without the need for correction depending on cable length. Monitoring the voltage at the encoder using sensor lines and adjusting the supply voltage through a controllable power supply (or sensor) is not necessary. For more details, please refer to Interfaces to HEIDENHAIN Encoders, pages 33-34.

The DC/DC supply specification is outlined in Table 2.

Table 2. Part I: Encoder Power Supply Generic Specification

ENCODER POWER SUPPLY PARAMETERS	ENDAT 2.2	TIDA-00172
Input voltage, nominal (range)[1]	–	24-V DC (17 to 30 V)
Output voltage range	3.6 to 14-V DC	3.6 to 14-V DC (default 8-V DC)
Output voltage accuracy	–	<±5%
Output voltage, low frequency ripple	<100 mVpp	<50 mVpp
Output voltage, high frequency interference	<250 mVpp with dU/dt >5V/us	<250 mVpp with dU/dt >5 V/us
Output current (nominal)	–	200 mA
Output voltage start-up time (0V à Up)	–	<30 ms
Efficiency at 8 V, 200 mA	–	>85% (including eFUSE)
DC/DC switching frequency[2]	–	700 kHz

[1] Assuming an isolated 24-V DC voltage (PELV).
[2] Adjustable through passive component change. Option to synchronize with external clock.

2.2.2 Power Limit and Trip with eFUSE

Additional safety features of the power supply include an enable pin to save power when no encoder is connected or to switch off the power supply in case of an external short.

Therefore, an eFUSE is added as part of the entire encoder power supply to electronically disconnect power from the encoder in case of a fault. Fault conditions are overvoltage, undervoltage, overpower, and overcurrent. A fault flag (Enc_PWR_Fault) is made available on the logic I/O connector to allow a host controller to recognize the fault condition and disable the power supply. The advantage of an eFUSE is that the eFUSE can be re-enabled by power-cycling. Therefore, eFUSEs can react on temporary faults like a short due to a defective cable without the need to send a technician. The additional protection features are specified in Table 3.

Table 3. Part II: Encoder Power Supply Protection Specification

ENCODER POWER SUPPLY PARAMETERS	TIDA-00172	COMMENT
Output voltage enable/disable pin	Yes	
eFUSE: Overpower trip limit	2 W	Adjustable, see Section 4.2.3
eFUSE: Inrush current limit	500 mA	Adjustable, see Section 4.2.3
eFUSE: Overvoltage trip limit	14 V	Adjustable, see Section 4.2.3
eFUSE: Undervoltage trip limit	4 V	Adjustable, see Section 4.2.3
eFUSE (turn-off time)	Approx. 1 ms	
eFUSE: Power fault pin (trip indication)	Yes	

2.2.3   EMC-Immunity Requirements According to IEC61800-3

IEC618000-3 specifies the EMC requirements for adjustable speed, electrical power drive systems. This TI design is intended for use in such drives. IEC618000-3, Table 4 specifies the minimum requirements for EMC, applicable for cases, cabinets, and connectors.

This design is assumed to be a part of a servo drive, and only the connector for the EnDat 2.2 encoder can be accessed. The assumption is that the connecter is tied to earth. According to IEC61800-3, the connector then falls under "Ports for process measurement and control lines, DC auxiliary supplies lower than 60 V". Since the encoder cable can be up to 100 m, EFT, surge, and conducted RF common mode apply per Table 4 for use in Environment 2.

Table 4. Extract of IEC61800-3 EMC Requirements for Second Environment

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Enclosure ports	ESD	IEC61000-4-2	±4 kV CD or 8 kV AD, if CD not possible	B
	Radiated RF	IEC61000-4-3	80 to 1000 MHz, 10 V / m, 80% AM (1 kHz) 1.4 to 2 GHz, 3 V / m, 80% AM (1 kHz) 2 to 2.7 GHz, 3 V / m, 80% AM (1 kHz)	A
Ports for control lines and DC auxiliary supplies <60 V	EFT	IEC61000-4-4	±2 kV / 5 kHz, capacitive clamp	B
	Surge 1,2/50 us, 8/20 us	IEC61000-4-5	±1 kV. Since shielded cable >20 m, direct coupling to shield (2 ohm / 500 A)	B
	Conducted RF	IEC61000-4-6	0.15 to 80 MHz, 10 V / m, 80% AM (1 kHz)	A

The performance (acceptance) criterion is defined in Table 5.

Table 5. Performance Qualifications

PERFORMANCE (PASS) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, a loss of functions is accepted, but not the destruction of hardware or software. After the test, the module shall continue to operate as intended automatically after a manual restart or power off/power on.

3 Block Diagram

The major building blocks are the protected encoder power supply and the RS-485 transceivers including line termination and EMC protection. A Sub-D 15-pin female connector with a shield is made available to connect an EnDat 2.2 position encoder with a corresponding Sub-D-15-to-M12 adapter cable from HEIDENHAIN. An auxiliary power supply and logic level interface with adjustable I/O voltage level has been added in order to connect to a microprocessor like Sitara, Delfino, Hercules, or FPGA to run the EnDat 2.2 Master protocol stack.
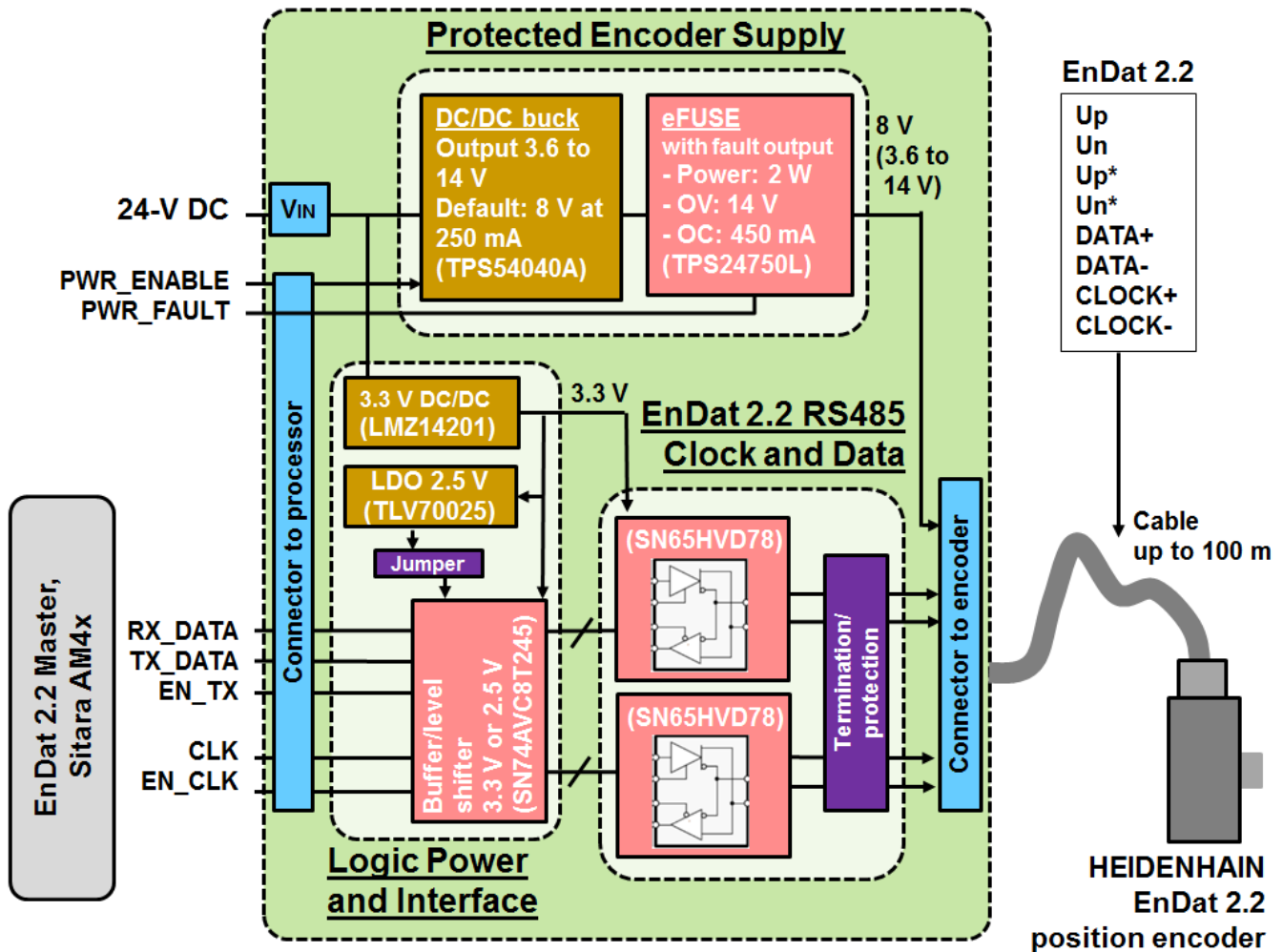
Figure 6. Block Diagram of TIDA-00172: Interface to Position Encoder with EnDat 2.2

4   Circuit Design and Component Selection

The following sections describe the components of this design and the criteria for why this components were chosen.

4.1   *EnDat 2.2 RS-485 Clock and Data and Logic Interface*

4.1.1   RS-485 Transceiver Circuits

When choosing the RS-485 device for EnDat 2.2, consider the relationship between baud rate and clock frequency. EnDat 2.2 is synchronous communication with the data shifted out at the falling clock edge. Each clock period equals two baud. The first half clock period equals a symbol as well as the second half period. The baud rate should be at least twice the clock rate. Therefore, an EnDat 2.2-compliant RS-485 transceiver needs to be specified for a minimum baud rate of 32 Mbps.

When EnDat 2.2 is implemented without delay compensation at a maximum clock of 2 MHz, the entire loop propagation delay (Master and Encoder) must not exceed 250 ns. Parameters with regards to RS-485 transceivers taken into consideration are listed in Table 6.

Table 6. RS-485 Parameters From Corresponding Data Sheets (SLLSE11, SLLS505)

PARAMETER	SN65HVD78	SN65HVD10
Supply voltage (recommended)	3.3 V	3.3 V
Baud rate (maximum)	50 Mbps	32 Mbps
Receiver propagation delay (maximum)	35 ns	25 ns
Driver propagation delay (maximum)	15 ns	16 ns
Receiver rise/fall time (maximum)	5 ns	5 ns
Driver rise/fall time (maximum)	6 ns	10 ns
Supply current (quiescent) driver and receiver enabled	0.95 mA (max)	15.5 mA (max)
IEC61000-4-2 ESD (absolute maximum ratings)	±12 kV (CD)	N/A
IEC61000-4-4 EFT (absolute maximum ratings)	±4 kV	±4 kV

With the information from Table 6, the RS-485 device was chosen to be the SN65HVD78. We also tested the design with SN65HVD10 as another option.

RS-485 Termination and Transient Protection

Instead of single 120 Ω/0.5 W resistors, the design uses four smaller resistors, each 1/8 W in parallel (470//470//470//510 Ω) to choose standard components and reduce cost. The line termination resistor is only needed on the half-duplex data signal transceivers. The clock is configured as transmitter only and is terminated at the encoder side. This configuration reduces current consumption of the RS-485 clock transceiver as the RS-485 clock transceiver only needs to drive the 120-Ω load, while the RS-485 data transceiver drives a 60-Ω load.

A pulse-proof resistor is added into the A and B bus lines if a transient voltage is higher than the specified maximum voltage of the transceiver bus terminals. See R30, R42, R50, and R60 in Figure 7 and Figure 8. These resistors limit the residual clamping current into the transceiver and prevent it from latching up. In data receive mode, due to the low input current of a typical 240 uA, the voltage drop across the 10-Ω resistors is negligible. In the clock and data transmit direction, the voltage drop across both 10-Ω resistors is around 15%, which results in a slightly lower transmit differential voltage.

To further improve immunity against common mode noise and only for clock frequencies of up to 8 MHz 330 pF, bypass capacitors are added from each differential RS-485 output A and B to GND. See C28, C30, C33 and C35 in Figure 7 and Figure 8.

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge.

For test purposes, a transient voltage suppressor (TVS) diode was added but not populated. Since the connector and corresponding cable are shielded, the surge pulse is applied to the cable shield only. The TVS diode would have been required only for equipment without a shielded cable. In that case, the surge would be coupled into all four differential signal lines with 160 Ω each source coupling impedance each to get 40 ohms.

Because ESDs and EFTs have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during the PCB design. A complete list of layout guidelines can be found in the SN65HVD78 data sheet. This design especially implements:

- V_{CC} and ground planes to provide low-inductance.
- 100-nF bypass capacitors as close as possible to the V_{CC} pins of the transceivers and other digital logic.
- At least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
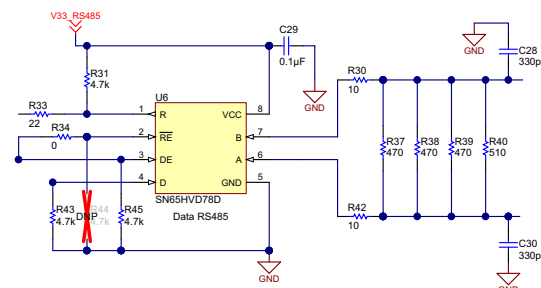
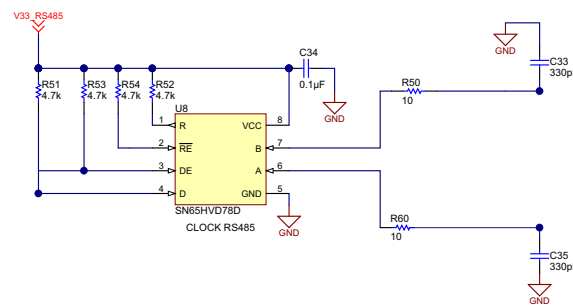**Figure 7. RS-485 Transceiver Configuration for EnDat DATA+/DATA-**

Figure 8. RS-485 Transceiver Configuration for EnDat CLOCK+/CLOCK-

4.1.2 Logic Interface to uP/FPGA

To support lower than 3.3-V I/O, this design uses the SN74AVC8T245 because SN74AVC8T245 can operate from 1.2 to 3.6 V. For ease of design and component purchase for the input, this design uses the 8-channel device. The 4-channel device SN74AVC8T245 could also have been used. SN74AVC8T245 would improve the BOM cost of the design. All signals not used were pulled down using a 4.7-kohm resistor to avoid any floating, undetermined input signals.

4.1.3 Logic Power Supply

The communication interface needs two voltage rails: a 3.3-V rail for the RS-485 transceivers and one side of the level shifter at 3.3 V as well as one voltage rail for the other side of the level shifter. This second rail can be 3.3 V, 2.5 V, or 1.8 V.

3.3-V DC/DC Buck

The voltage rail for the RS-485 and the level shifter is 3.3 V at 300 mA, coming from the 24-V bus (the voltage can be between 17 and 30 V). As this power supply does not need to be isolated, a buck (or step-down) topology is optimal. The specifications for this power supply are as follows:

- Input: 17 to 30 V, 24-V nominal
- V_{OUT}: 3.3 V at 300 mA
- Target switching frequency: Approximately 700 kHz
- Nonisolated

This design assumes the end application, the 3.3-V rail, will also be used to power other parts of the system (μC, FPGA, and so on). For this reason, good performance as well as high integration and ease of use are optimal characteristics for a device for power. This design uses a power module, which is a buck topology that integrates FET and inductor.

A TI power module presents several advantages. TI power modules are really easy to design with, saving time to market and development cost. TI power modules are tested for EMI and EMC, as well as the fact that the external components, usually found next to a controller (inductors, FETs, or diodes) are integrated, saving board space and cost of manufacturing.

With all these requirements in mind, the LMZ14201 fits the needs of the design. LMZ14201 is a buck topology, 6 to 42-V input, 0.8 to 6 V at 1-A output, and constant ON time power module. LMZ14201 required a few external components: a resistor divider to set the enable voltage, a resistor divider to set the output voltage, a resistor to set the ON time, one capacitor to set the soft start time, and input and output capacitors.
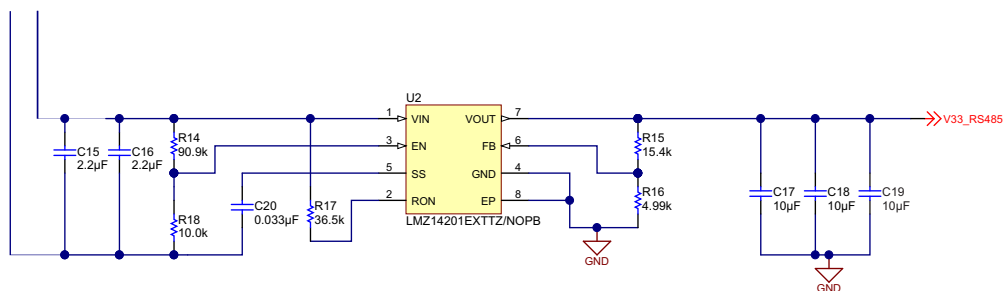

Figure 9. 3.3-V Logic Power Supply Schematic: Power Module LMZ14201

For the details on LMZ14201 and on how to calculate the external components around the LMZ14201, please have a look on the LMZ14201 data sheet and on the TIDA-00172 Design Calculator Excel sheet as depicted in Section 4.4.

For layout guidelines, please see page 16 of the LMZ14201 data sheet.

Level Shifter I/O Voltage Rail

The rail for the level shifter is 3.3 V, 2.5 V ,or 1.8 V at 100 mA. If the 3.3-V option is needed, this voltage can be the same as the voltage rail for the RS-485. If the 2.5-V or 1.8-V option is needed (communication with an FPGA, for example), the desired voltage can be generated by a low drop out (LDO) linear regulator. The specifications for this LDO are as follows:

- Input: 3.3 V
- V_{OUT}: 2.5 V/1.8 V at 100 mA. The 2.5-V option was chosen for this design
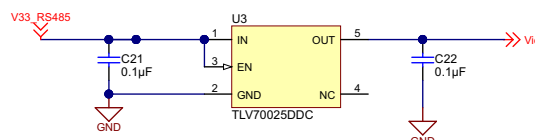- Drop out voltage: <0.7 V

Figure 10. Logic Power Supply Schematic: 2.5-V LDO

For the LDO, this design needs an easy-to-use, cost effective part. The TLV70025 fits the design needs. This design uses a 2 to 5.5-V input, 2.5-V at 200-mA LDO. The LDO only requires input and output capacitors. Please note that the TLV700XX family offers a wide range of voltage option, pin-to-pin compatible to each other: 1.2 V, 1.3 V, 1.5 V, 1.8 V, 1.9 V, 2.2 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.2 V, 3.3 V, and 3.6 V. For the details on the part, see the TLV700xx family data sheet.

4.2 *Protected Encoder Power Supply*

The Encoder requires a voltage between 3.6 and 14-V at 250 mA, coming from the 24-V bus (the voltage can be between 17 and 30 V). As this voltage conversion does not need to be isolated, a buck (step-down) topology is optimal. This voltage rail also requires some safety features: current limit during inrush, power limit, and overvoltage protection (OVP). These safety features are handled by an eFUSE.
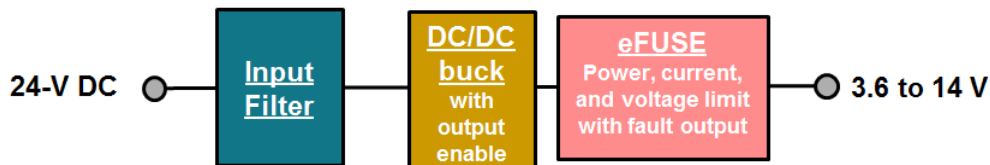
Figure 11. Protected Encoder Power Supply Block Diagram

4.2.1   Input Filter

Conducted EMI are generated by the normal operation of switching circuits. Large discontinuous currents are generated by the power switches turning ON and OFF. In a buck topology, these large discontinuous currents are present at the input side. The voltage ripple, created by these discontinuous currents, can be conducted to the rest of the system through physical contact of the conductor. Excessive input voltage ripples can disturb the normal operation of other parts of the system. To prevent this disruption, an input filter can be used to reduce the input voltage ripple and prevent compromising the operation of the complete system.

In this design, the input filter consists of a PI filter with the cutoff frequency around one-tenth of the switching frequency of the converters in order to have 40 dB of attenuation at the switching frequency.

The converters in this design have a switching frequency of 700 kHz, so for the input filter for this design is as follows:

$$F_C = \frac{1}{2 \times \pi \times \sqrt{L_C}}$$

where

- L is the range of 1 to 10 µH
- F_C at 70 kHz   (1)
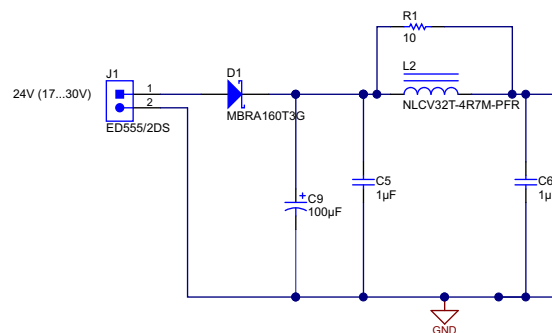
These settings give a capacitor value of 1 µF.

Figure 12. Input Filter

4.2.2 DC/DC Buck (TPS54040A)

The specifications for the encoder power supply are as follows:

- Input: 17 to 30 V, 24-V nominal
- V_{OUT}: 3.6 to 14 V at 250 mA. For this design, the output is set to 8 V at 250 mA
- Switching frequency: 700 kHz, adjustable with an option to synchronize to the external clock
- High efficiency: >85% at 8 V/200 mA output
- Nonisolated
- Output voltage ripple max: 50 mV
- Can be switched off (enable signal)

TPS54040A is a 3.5 to 42-V input, 0.8 to 39-V at 0.5-A output buck converter with integrated EFT. TPS54040A's frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. It can also be enabled or disabled. All these features make TPS54040A a good fit for the requirements of this design.
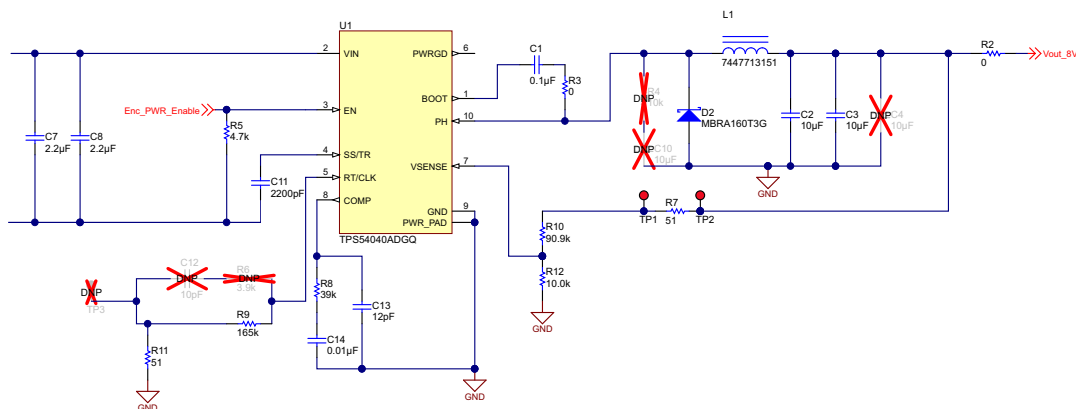
Figure 13. Protected Encoder Power Supply Schematic: DC/DC Converter TPS54040A

External Switching Frequency Option

When multiple power supplies are on a single board, multiple switching frequencies coexist. This switching creates undesirable subharmonic beat frequencies and EMI effects. The elusive noise problems caused by multiple switching frequencies can affect the performance of the controller. Therefore, synchronization of the switching frequencies, when applicable, can either improve performance or even be mandatory for stable operation.

For this design, the switching frequency is set at 700 kHz due to R9. In case a synchronization is required, the engineer can populate R6, C12, and TP3, and the external clock can be applied through TP3.

In case TPS54040A is synchronized to an external clock, the complete design should be calculated with the external clock frequency with the exception of the resistor, which sets the default switching frequency (R_{fset} in Figure 14, R9 in our design).The default switching frequency set by R9 should then be set to a frequency close to, but lower than the external clock (500 kHz in this case).
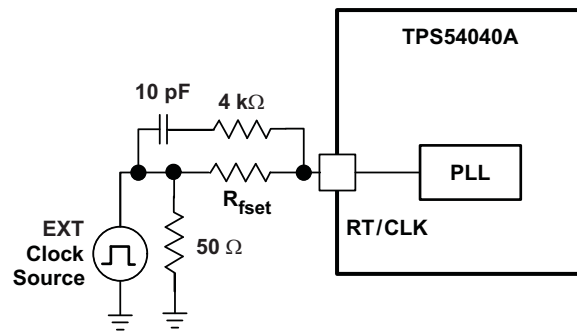
Figure 14. Synchronizing to a System Clock

For more details see page 21 to 23 of the TPS54040A data sheet.

On the schematic in Figure 14, some components are marked as do not populate (DNP).

TP3, R6, and C12 are needed for synchronization of the switching frequency to an external clock. The rest of the DNP components are placed to be able to improve the performance during the test of the board.

- **C4**: C2 and C3 are used as output capacitors. In case more capacitance is required, C4 can be populated. The C4 footprint can also be used to measure the output voltage generated by U1.

- **R3**: In case there is too much ringing on the switch node, one solution is to slightly slow the switching speed of the MOSFET. The slowdown can be achieved by adding a small resistor in series with the Bootstrap capacitor (approximately two ohms). See SLPA010 on how to use and calculate this Boot resistor.

- **R4, C10**: Another way of reducing the ringing and overshoot of the MOSFET is to add a snubber network. R4 and C10 are placed here in case of a snubber is being designed. See SLPA010 on how to use and calculate your snubber network.

Setting Output Voltage and Changing Parameters

For the details on the part and on how to calculate the external components around the TPS54040A, see the TPS54040A data sheet and the TIDA-00172 Design Calculator Excel sheet, shown in Section 4.4.

Please note that TPS54040A is pin-to-pin compatible with the TPS54140A, TPS54240, TPS54340, and TPS54540, which have the same specifications as TPS54040A with 1.5 A, 2.5 A, 3.5 A, and 5 A capability, respectively.

Please also note that TPS54040A is pin-to-pin compatible with TPS5401, which is a lower-cost version of TPS54040A with similar performance but less accurate output voltage and enabled threshold.

Layout Guideline

Please refer to page 38 of the TPS54040A data sheet.

4.2.3 eFUSE Protection

The specifications for the eFUSE are as follows:

- Current limit during inrush: 500 mA
- Power limit: 2 W
- Overvoltage protection (OVP): 14 V
- Undervoltage Lockout (UVLO): 4 V
- Latch or disconnect when a fault is detected
- Fault feedback

The TPS24750 is a 12-A eFUSE, 2.5 to 18-V bus operation with integrated MOSFET with 3 mΩ $R_{DS(on)}$. The TPS24750 has an OVP, a UVLO, a programmable current and power limit, and a programmable fault timer. The design uses this part as it fits the design requirements and contains an external sense resistor, allowing for a precise current-and-power limit event at low current.

In a traditional current limit use of the eFUSE, the voltage across the resistor (R_{IMON}, R22 in this design) between IMON and ground is proportional to the current through the sense resistor as well as scaling the current limit setting. In order to limit the power and not the current, this design adds a resistor (R_{POW}, R21 in TIDA-00172) between the V_{CC} and IMON pins of the TPS24750. The following equations are used to set the power limit at the level desired.

The first component to be calculated is the sense resistor (R_{SNS}, R19 in this design).

We start by setting the sense resistor to trigger the fast trip voltage threshold:

$$R_{SNS} = \frac{0.6}{I_{INRUSH}}$$

(2)

R_{IMON} is set at 6.75 kΩ. R_{PROG} is set (R23 in this design) to 5 Ω to disable the internal power limitation of the MOSFET.
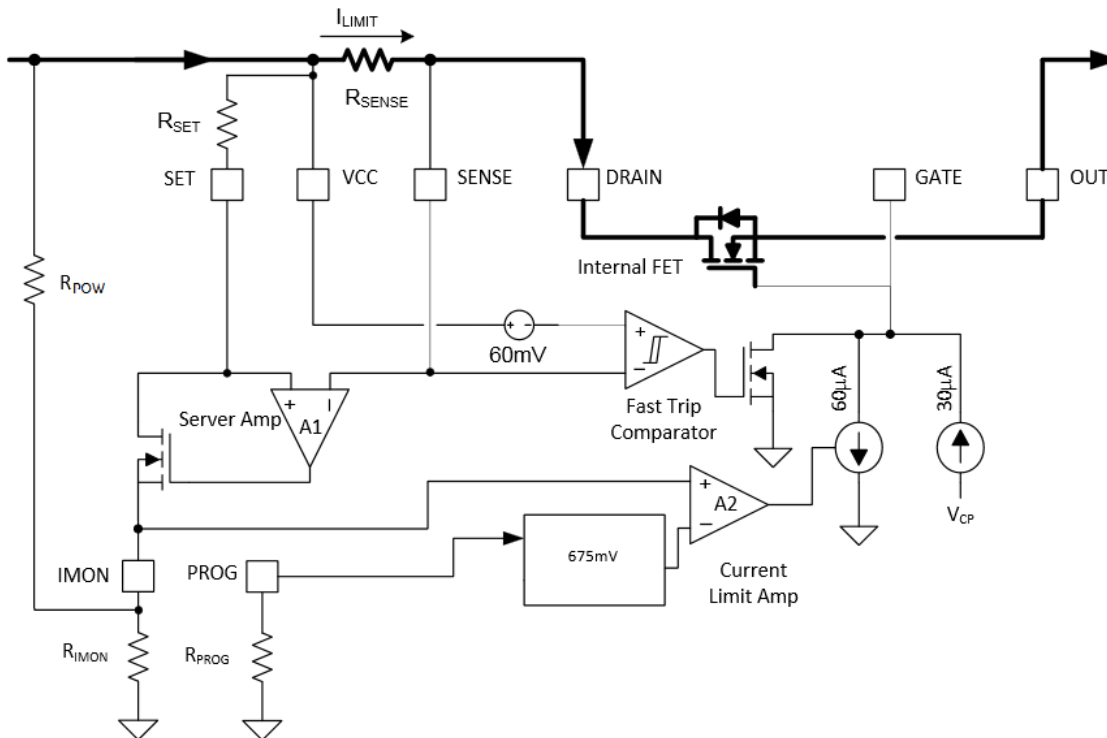
Figure 15. Partial Diagram of the TPS24750 with Selected External Components

From Figure 15:

$$I_{RIMON} = \frac{0.675}{R_{IMON}}$$

(3)

with I_{RIMON} the current through R_{IMON}, and

$$I_{RPOW} = \frac{V_{IN} - 0.675}{R_{POW}}$$

(4)

with I_{RPOW} the current through R_{POW}

$$I_{RSET} = I_{RIMON} - I_{RPOW}$$

(5)

with I_{RSET} the current through R_{SET}

$$I_{RSET} = \frac{0.675}{R_{IMON}} - \frac{V_{IN} - 0.675}{R_{POW}}$$

(6)

The amplifier A1 ensures that $V_{SE} = V_{SNS}$, with V_{SET} the voltage across R_{SET} and V_{SNS} the voltage across R_{SNS}.

So

$$I_{LIM} = \frac{I_{RSET} \times R_{SET}}{R_{SNS}}$$

(7)

Equation 7 and Equation 9 give

$$I_{LIM} = \frac{R_{SET}}{R_{SNS}} \times \left(\frac{0.675}{R_{RIMON}} - \frac{V_{IN} - 0.675}{R_{POW}} \right)$$

(8)

with

$$P_{LIM} = I_{LIM} \times V_{IN}$$

(9)
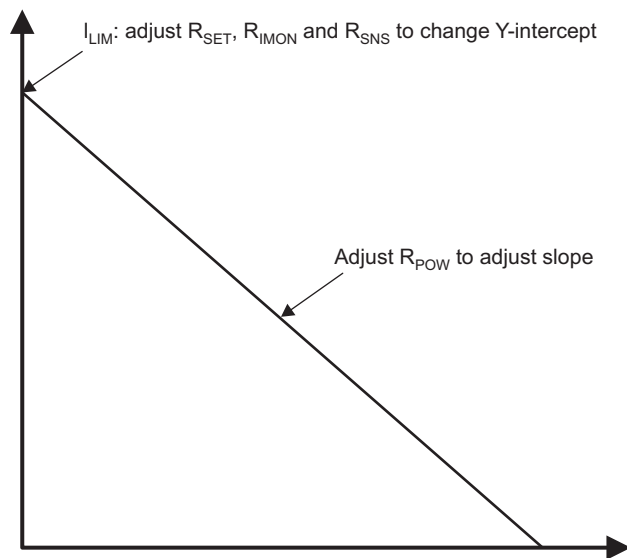
Figure 16. Power Limit Function of Input Voltage

By empirical result, the best settings are when Equation 11 and Equation 13 are fulfilled.

$$I_{LIM}\left(V_{IN} = 0.675\right) = 2 \times I_{LIM}\left(V_{IN} = V_{ENC}\right) \tag{10}$$

R_{POW} can now be calculated thanks to equations 9 and 11

$$R_{POW} = \frac{2 \times \left(V_{ENC} - 0.675\right) \times R_{IMON}}{0.675} \tag{11}$$

R_{SET} is then calculated thanks to Equation 9 and Equation 13

$$I_{LIM}\left(V_{IN} = V_{ENC}\right) \times V_{IN} = P_{LIM} \tag{12}$$

$$R_{SET} = \frac{P_{LIM} \times R_{SNS}}{V_{ENC} \times \left(\dfrac{0.675}{R_{RIMON}} - \dfrac{V_{ENC} - 0.675}{R_{POW}} \right)} \tag{13}$$

Finish by calculating the fault timer capacitor, as shown on page 9 of the data sheet.
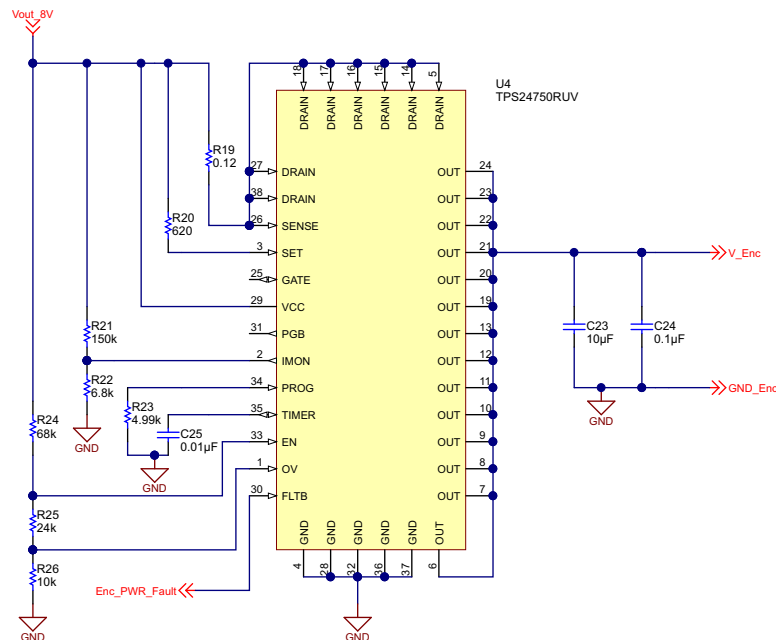
Figure 17. Protected Encoder Power Supply Schematic: eFUSE TPS24750

For the details on the part and on how to calculate the external components around the TPS24750, see the TPS24750 data sheet and on the Design Calculator Excel sheet, shown in Section 4.4.

Please note that the TPS2492 has a similar function and supports voltages between 9 and 80 V. The TPS2492 is available in a TSSOP package.

Layout Guideline

See page 31 of the TPS24750 data sheet.

4.3   *Connector to EnDat 2.2 Encoder and Master*

The connector to the EnDat 2.2 position encoder is connected to a SubD-15 female with the same pin-out that HEIDENHAIN equipment uses, such as PWM20. The pin-out of the EnDat 2.2 connector is shown in Section 5. The connector to the external processor or FPGA for the EnDat 2.2 Master has a 5 × 2 header with 2.54-mm spacing. The connector to control the encoder power supply has a 3 × 2 header with 2.54-mm spacing. Both connectors offer a configurable I/O voltage (V_{IO}), which is defaulted at 3.3 V but can be changed to 2.5 or 1.8 V. For details on the connector assignment, refer to Section 5.

4.4   *Design Support*

The TIDA-00172 Design Calculator Excel sheet was created to help design the power components presented in this Excel sheet. The Excel sheet includes the equation presented in this guide, as well as the equation presented in the data sheets.

This Excel sheet must be used in a sequential order from top to bottom.

This Design Calculator document contains three Excel sheets:

- Design: in this sheet, the designer enters his or her design values and choose the components he or she wants to use
- BOM and Schematic: this sheet recaps the components chosen in the design sheet and shows where to place the components in the schematic
- Components data: this sheet recaps some parameters of the TI components that are needed for the calculations on the design sheet

There are four different cases in this Excel document:

User input specifications
Calculated Component
User selected standart component
Calculated design parameter

Figure 18. Excel Document Color Code

- The yellow marked cells are the cases where the user will enter the different specifications of his or her design.
- The blue marked cells are the results of the equation needed to select a component.
- The green marked cells allow the user to choose the standard value the closest to the blue marked cells next to it.
- The red marked cells are design parameters that are calculated along the process (for example, the duty cycle or the current flowing in the inductor).

See Figure 19 for a short example.

Vencoder - TPS54040A						
power supply requirements	**Parameter**	**Value**	**Value chosen**	**Description**		
	vinstart (V)		10.00	Enable voltage		User input specifications
	vinstop (V)		9.00	Disable voltage		Calculated Component
	dVin (%)		1.00	input voltage ripple		User selected standart component
	dVopp (V)		0.10	output ripple voltage requirement		Calculated design parameter
	dVo (V)		0.10	output voltage transient requirement during step load changes		
	kind		0.30	inductor ripple constant (usually between 0.2 and 0.4)		
	ioh (A)		0.25	output current under heavy load		
	iol (A)		0.00	output current under light load		
	vfd (V)		0.50	forward voltage of schottky diode		
	vosc (V)		0.10	output voltage during short circuit		
power stage design	**Parameter**	**Value**	**Value chosen**	**Description**		
	R12 (kΩ)		10	low side feedback resistor for adjusting output voltage. Usually 10kΩ		User input specifications
eq1 in d/s	R10 (kΩ)	90.00	90.90	High side feedback resistor for adjusting output voltage		Calculated Component
	Dmax	0.47		maximum duty cycle		User selected standart component
	Dnom	0.33		nominal duty cycle		Calculated design parameter
	Dmin	0.27		minimum duty cycle		
eq28 in d/s	L1min (H)	139.7E-6	150.0E-6	calculated minimum inductor value		
	rdc actual (Ω)		0.110	actual DCR of output inductor		
eq29 in d/s	Iopp actual (A)	0.06		actual peak-to-peak output current ripple		
eq30 in d/s	Iind_rms (A)	0.20		RMS inductor current		

Figure 19. Extract of the TIDA-00172 Design Calculator Excel Sheet

In the extract in Figure 19, the designer fills the yellow cells according to the designer's specification. Once all the yellow cells are filled, the designer arrives to the first green case. The low side resistor is needed to set the output voltage of TPS54040A. This design recommends using 10 kΩ here.

Due to the 10 kΩ value and to some of the specification entered previously in the yellow cases, R10, the high side resistor, is needed to set the output voltage of the TPS54040A. Then the TPS5040A output voltage is calculated at 90 kΩ (in the blue case). The designer will then choose the closest standard value needed to implement in the design. This design uses 90.9 kΩ.

The next three cases are the maximum, nominal, and minimum duty cycle, calculated from the maximum, nominal, and minimum input voltage and output voltage set by the designer in previously filled yellow cases.

The designer then continues in a vertical sequence.

5 Getting Started

5.1 PCB Layout

A picture of the PCB top and bottom is shown in Figure 20. To minimize the PCB size, components are mounted on the top and bottom layers. All jumpers and connector to external components are mounted on the top layer.
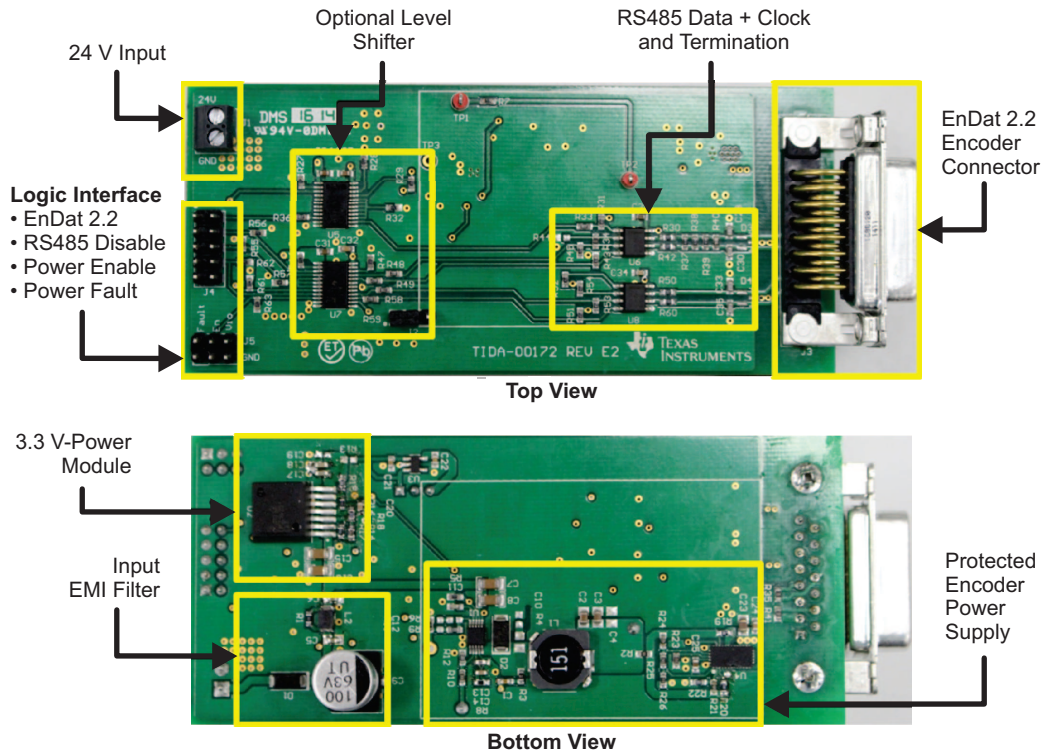

Figure 20. PCB Top and Bottom View with Functional Blocks

5.2 Connectors and Jumper Settings

The connector assignment and jumper settings are outlined in Table 7.

Table 7. Connector Assignments

CONNECTOR	PIN	SIGNAL	PIN	SIGNAL	DESCRIPTION
J4	1	GND	2	RCV_DATA (O)	EnDat 2.2 data receive
	3	GND	4	EN_TX_DATA (I)	EnDat 2.2 enable data transmit
	5	GND	6	TX_DATA (I)	EnDat 2.2 data transmit
	7	GND	8	TX_CLOCK (I)	EnDat 2.2 clock
	9	GND	10	EN_TX_CLOCK (I)	Enable clock transmit
J5	1	GND	2	Fault (O)	Encoder power supply fault indication
	3	GND	4	En (I)	Turn on encoder power supply
	5	GND	6	Vio (O)	GPIO voltage output

The Encoder Sub-D 15 connector is compatible with HEIDENHAIN SubD-15 (female) to the M12 (male) adapter cable. This design's default PCB configuration is Up* and Un*, which connects to Up and Un, respectively. If the connection not desired, remove the 0-ohm resistors (R35 and R41) on the bottom PCB close to the SubD-15 connector.

Table 8. Encoder SubD-15 Connector

CONNECTOR	PIN	DESCRIPTION (BLANK = NOT CONNECTED)
J3	1	
	2	Un (0v)
	3	
	4	Up (3.6 to 14 V)
	5	DATA+
	6	
	7	
	8	CLOCK+
	9	
	10	Sensor Un* (0V)
	11	
	12	Sensor Up*
	13	DATA-
	14	
	15	CLOCK-

Table 9. GPIO Voltage Selection

JUMPER	SETTING	DESCRIPTION
J2	1-2	Select 3.3-V I/O (default)
	2-3	Select 2.5-V I/O

6 Test Results

Testing was performed on the individual subsystems such as RS-485 and power supply. An application test was performed on the EnDat 2.2 position encoders. The RS-485 data and clock transceiver section was tested for maximum error-free data rate versus cable length, signal integrity (eye diagram, transceiver propagation delay) and power consumption. The protected encoder power supply was tested. Following that, performance tests were conducted using four different HEIDENHAIN EnDat 2.2 position encoders. An internal preliminary EnDat 2.2 Master software implementation on TI's Sitara AM4x Cortex A9 processor was used to conduct the application tests. Finally, the immunity of this design according to IEC61800-3, IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (Surge) was tested.

6.1 RS-485 Transceiver Performance

6.1.1 Test Setup

Figure 21 shows the setup of the RS-485 transceiver performance test and the test equipment used.
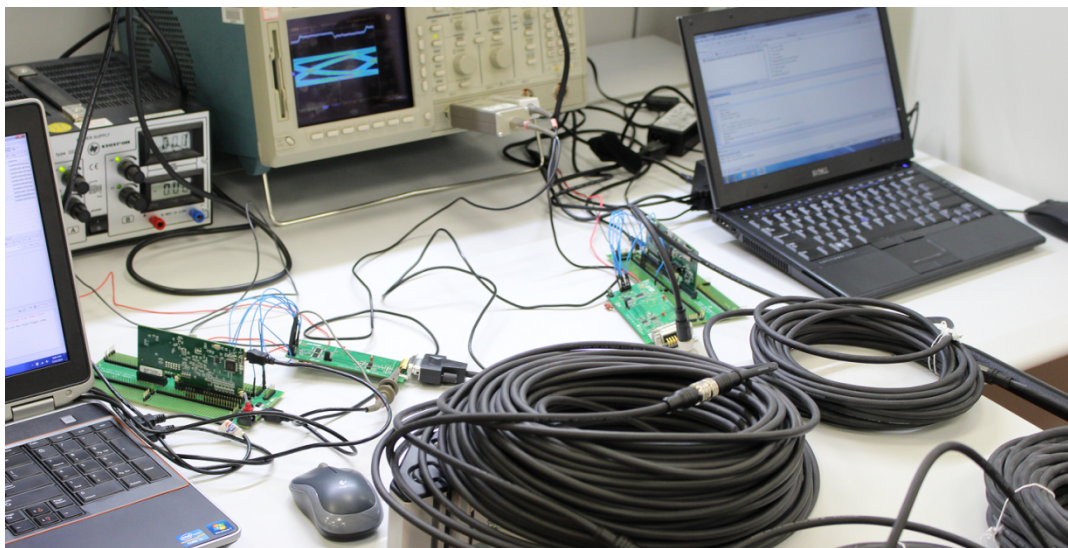
Figure 21. Picture of Test Setup for TIDA-00172 RS-485 Performance Tests

Table 10. Test Equipment

TEST EQUIPMENT	PART NUMBER
HEIDENHAIN shielded cables, PUR (4×0.14 mm^2, 4×0.34 mm^2), 10 m, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable 1m	524599-1
Random pattern generator and bit error analyzer (1 to 25 Mhz) via SPI	TMS320F28377D Experimenter Kit with internal TI test software
Oscilloscope	Tektronix TDS794D, P6330/P6339A diff/passive probes

The functional block diagram of the test setup is shown in Figure 22. The test used a TMS320F28377D MCU to implement a high-speed SPI master (with delay compensation) and another MCU to implement an SPI slave to control and analyze the synchronous data communication through the half-duplex interface. The master and slave were connected through HEIDENHAIN cables (4×0.14mm^2 for RS-485, 4×0.34mm^2 for supply lines) with 1 m, 9 m, 2×20 m, and 50 m, yielding a total length of 100 m. The SPI master was connected to the TIDA-00172. The SPI master clock was configurable from 1 MHz up to 50 MHz. The SPI slave was connected to a modified version of TIDA-00172 with only a 120-ohm termination. The RS-485 clock transceiver was configured in receive mode.
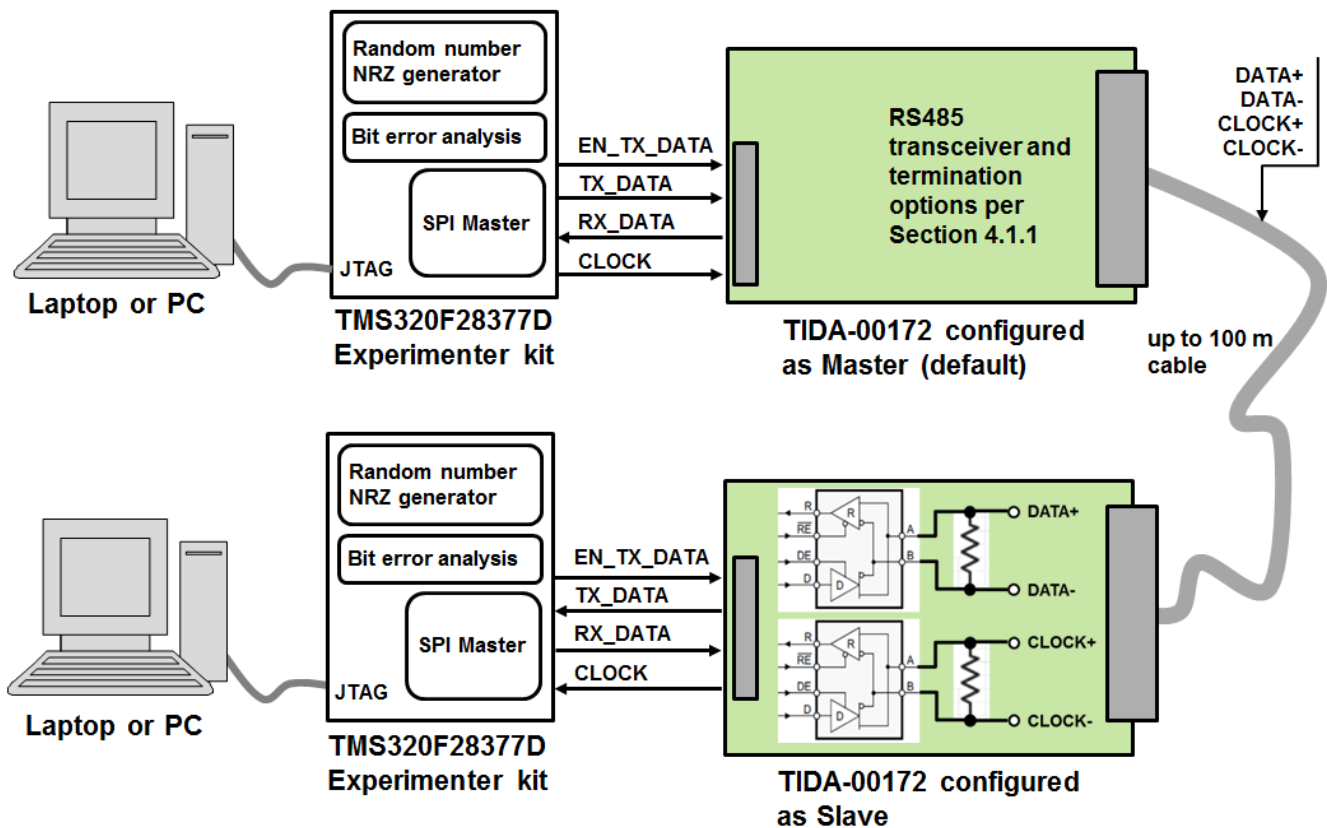
Figure 22. System Diagram of the Test Setup for TIDA-00172 RS-485 Performance Tests

The data communicated through the RS-485 half-duplex synchronous mode link was generated in software on TMS320F28337D MCU as well.

In test mode, "MAXCLOCK", a new data packet, was sent at an 8-kHz rate. Each packet was 48-bit, with the first 16-bit being the random number, the second word was the byte swapped random number, and the third word was the packet counter, as shown in Figure 23. The random number was generated using the C function rand(). Test mode "MAXCLOCK" was used for the maximum clock frequency versus cable length. To measure the maximum bit error-free data rate (clock rate) on either the received data on slave side or master side, the frame counter and the swapped random number were analyzed for bit errors, and an error counter was increased accordingly. If a single error occurred within 60 seconds, the test failed. This scenario should simulate a typical servo drive's inner current control loop (FOC) running at 8 kHz and requesting a new angle position through EnDat 2.2. A picture of the packet is shown in Figure 23.
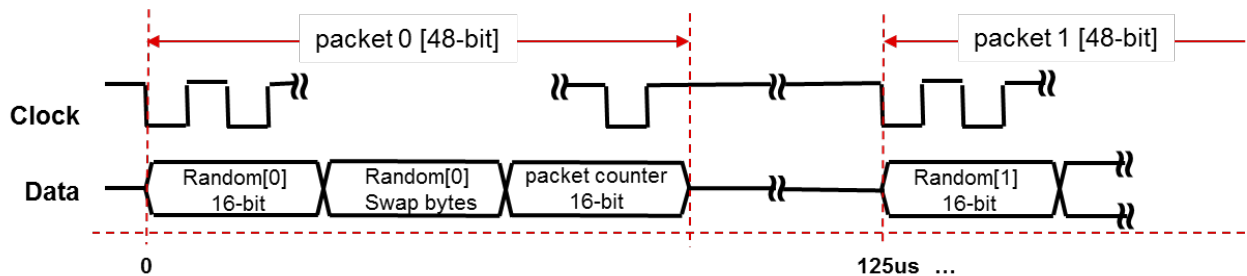
Figure 23. Test Pattern Transmitted Over RS-485 Link

In test mode EYEDIAGRAM, a 16-bit random number was generated and the 16-bit NRZ code was continuously sent to a configurable SPI master clock from 1 to 25 MHz. The SPI master clock was used to trigger the received data after the end of the cable on the slave side with a 120-ohm termination.

6.1.2   RS-485 Clock Frequencies Versus Cable Length

Figure 24 through Figure 27 show the maximum clock frequency versus cable length. The maximum clock frequency equals the synchronous data rate in half-duplex mode without any bit errors, as specified previously. Data was shifted out on the master side on the falling clock edge.

Remember that the maximum baud rate to which the RS-485 transceiver is specified must be twice the EnDat 2.2 clock rate, as EnDat transmits new data at the clock rate. Therefore, for a clock rate of 16 MHz, the minimum baud rate needs to be 32 Mbps. The maximum recommended baud rate of HVD78 and HVD10 is 50 Mbps and 32 Mbps, respectively. Therefore, testing was only performed up to the respective maximum clock rates, which were 25 MHz for HVD78 and 16 MHz for HVD10, respectively.

Figure 24 and Figure 25 compare the maximum clock (data) rates with zero bit error of the RS-485 transceivers SN65HVD10 versus SN65HVD78 in the default configuration without a bypass capacitor at the differential outputs to GND. The differential outputs to GND were measured at the slave and master receivers. See Section 6.1.1 for the test setup.
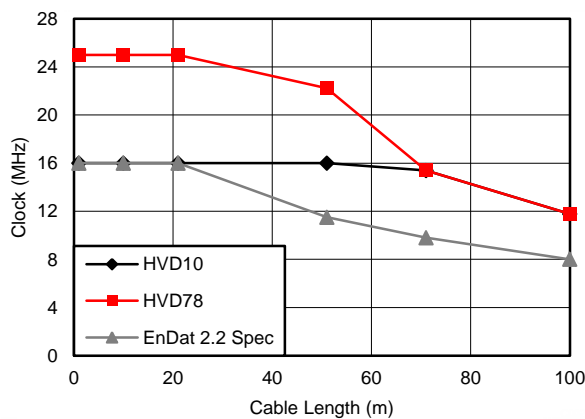
Figure 24. Maximum Clock Frequencies with Zero Bit Error for HVD78 or HVD10 Transmitter at Slave Receiver
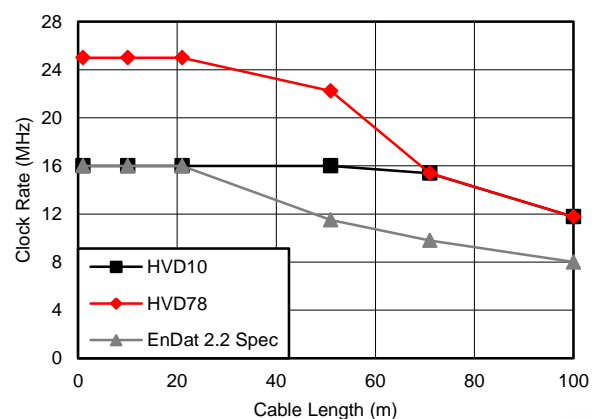
Figure 25. Maximum Frequencies with Zero Bit Error for HVD78 and HVD10 Transmitter at Master Receiver

Figure 26 and Figure 27 compare the maximum clock (data) with and without the 330-pF bypass capacitors (at terminals A, B to GND) on both differential signals, master clock, and master data RS-485 transceivers for HVD78. The bypass capacitors reduce the achievable data rate. As the rate was capped at 25 MHz (50 Mbps), the impact is only seen at higher attenuations where the rates were lower than the capped rate. The reference in the slave receive side was HVD78 without bypass caps and without TVS diodes.
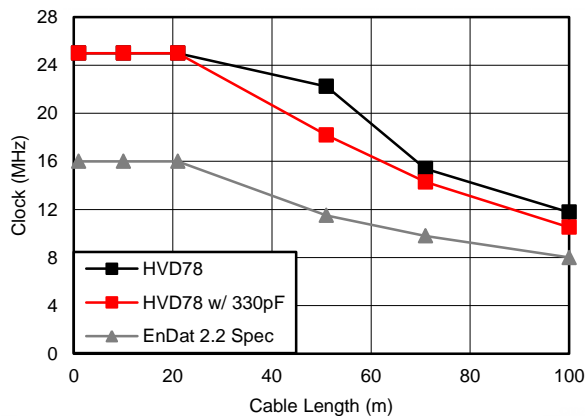
Figure 26. Maximum Clock Frequency with Zero Bit Error at Slave Received for HVD78 with and without 330-pF Bypass Caps at Master Transmitter
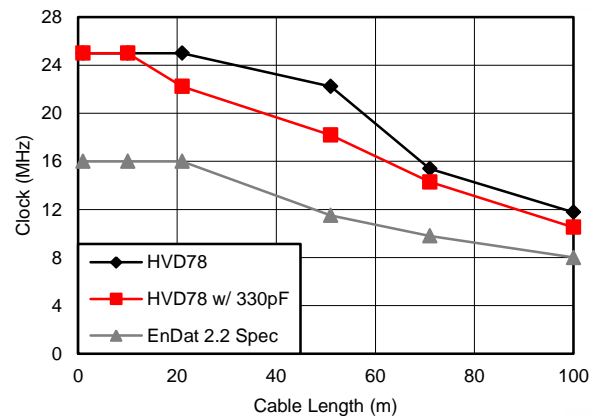
Figure 27. Maximum Clock Frequency with Zero Bit Error at Master Received for HVD78 with and without 330-pF Bypass Caps at Master Transmitter

6.1.3   RS-485 Eye Diagrams Versus Cable Length

The device under test was the master transceiver, RS-485. Figure 28 through Figure 33 show the eye diagrams using random NRZ data measured differentially with a 120-ohm termination at the cable end (slave receive side) with a differential Tektronix probe. The master transmitter clock rate was connected to channel 1 of the scope to trigger sampling of the differential data at the far cable end. The master clock was measured single-ended at the input of the master RS-485 clock transmitter and is shown as reference (Ch1, 5 V/div, 25 ns) on the scope plots also.

Measurements were conducted at cable length 100 m and 20 m with maximum data rates as well as with maximum rates as specified per EnDat 2.2 for both HVD78 and HVD10, as well as for HVD78 with bypass capacitors on the master differential clock and data outputs.

The jitter of the received differential data at the cable with a 120-ohm termination at the maximum EnDat 2.2 clock frequency is around 10% (0.9 UI-open). The steady state differential voltage is around ±1.2 V (2.4 Vpp). However, the rise or fall time from 10% to 90% is exactly one clock cycle. Taking into account that the receive data is sampled at the falling clock edge (in the 'middle' of the clock cycle), the effective worst case differential voltage is around ±0.8 V. Since EnDat 2.2 specifies the maximum clock frequency based on a 50% duty cycle, the maximum clock frequency is needed to be reduced by 10%.

Measurements at 100-m Cable Length
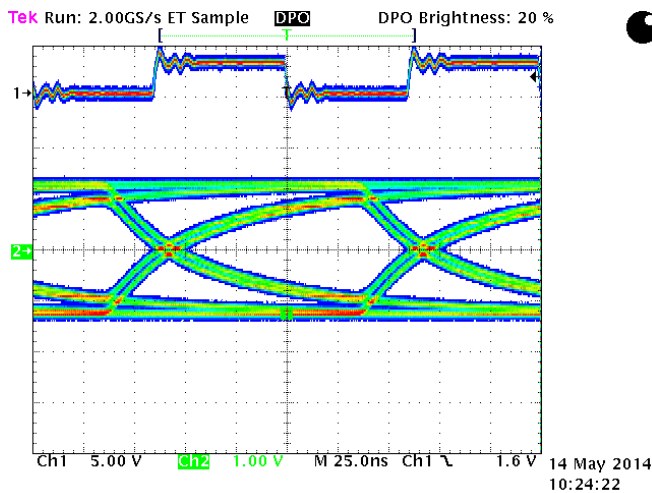
Figure 28. Eye Diagram HVD10, 100-m Cable, 8-MHz Data Rate
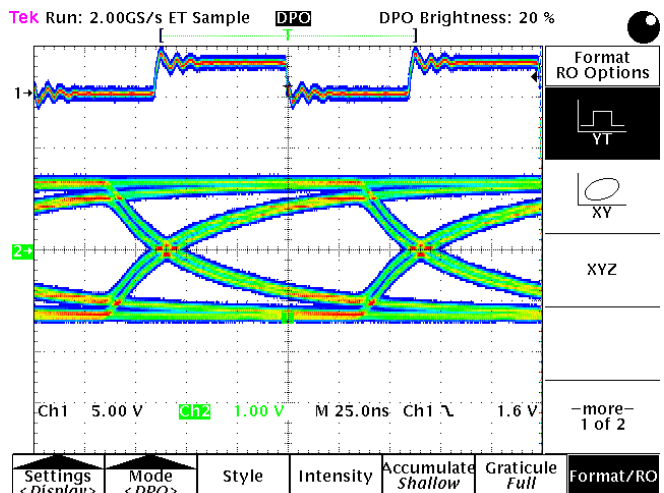
Figure 29. Eye Diagram HVD78, 100-m Cable, 8-MHz Data Rate
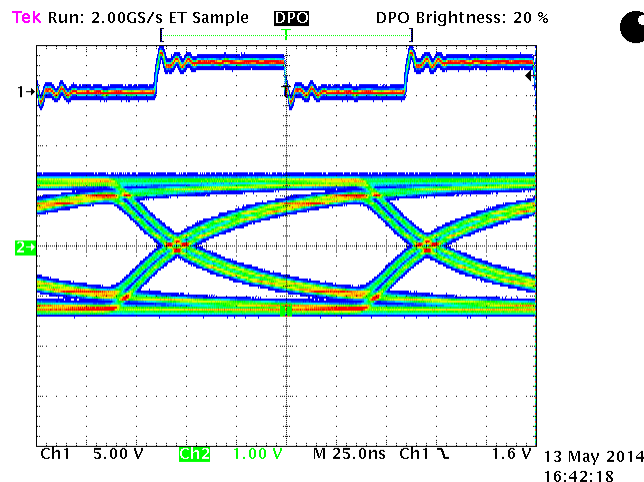
Figure 30. Eye Diagram HVD78 with 330-pF Bypass Caps at Master Transmit, 100-m Cable, 8-MHz Data Rate

Measurements at 20-m Cable Length
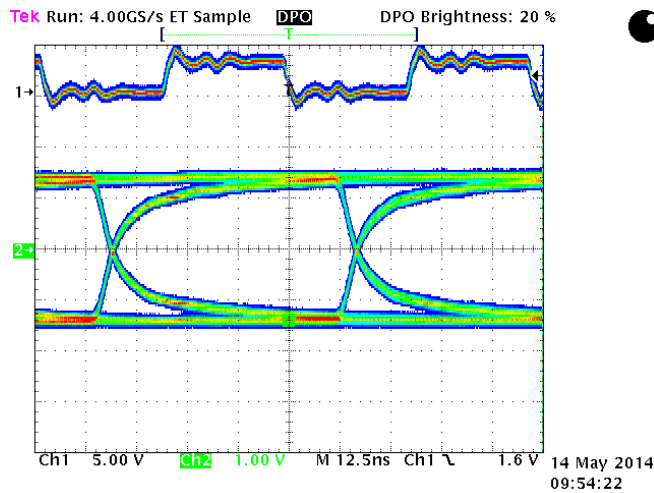
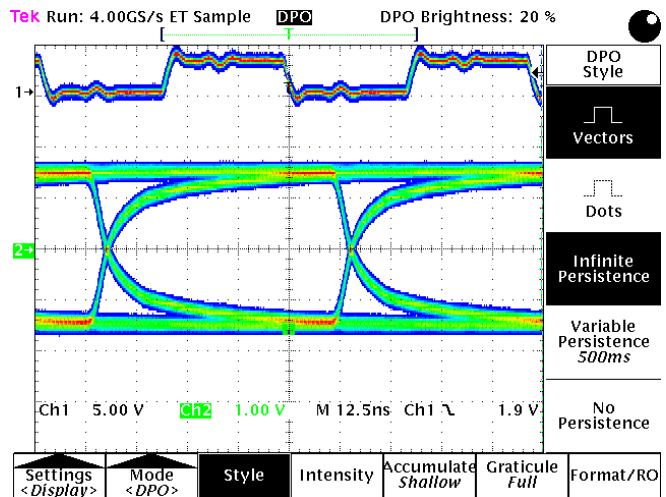**Figure 31. Eye Diagram HVD10, 20-m Cable, 16-MHz Data Rate**

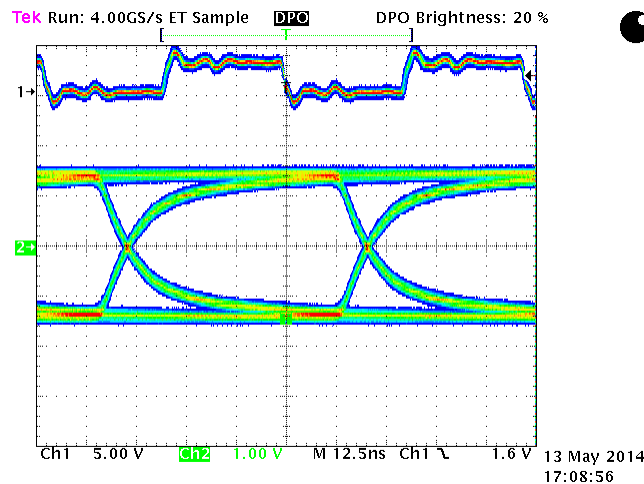**Figure 32. Eye Diagram HVD78, 20-m Cable, 16-MHz Data Rate**

Figure 33. Eye Diagram HVD78 with 330-pF Bypass Caps at Master Transmit, 20-m Cable, 16-MHz Data Rate

6.1.4   RS-485 Transceiver Propagation Delay and Common Mode

Figure 34 shows the transmit clock voltage levels measured single-ended versus GND at the EnDat 2.2 clock transmitter SN65HVD78 driver outputs A and B with a 20-m cable and a 120-ohm termination at the far end. The common-mode voltage of CLOCK+ (ch1: black) is around 1.8 V, with the upper voltage at 3 V and the lower voltage at 0.6 V. The common-mode voltage of CLOCK- (ch2: green) is around 2 V, with the upper voltage at 3.2 V and the lower voltage at 0.8 V. The differential voltage between those signals is around ±2.4 V. The differential signal using the MATH function on the scope is shown on M1 (purple) in Figure 34.

> **NOTE:** The 5-V/div scale is used for Math1.
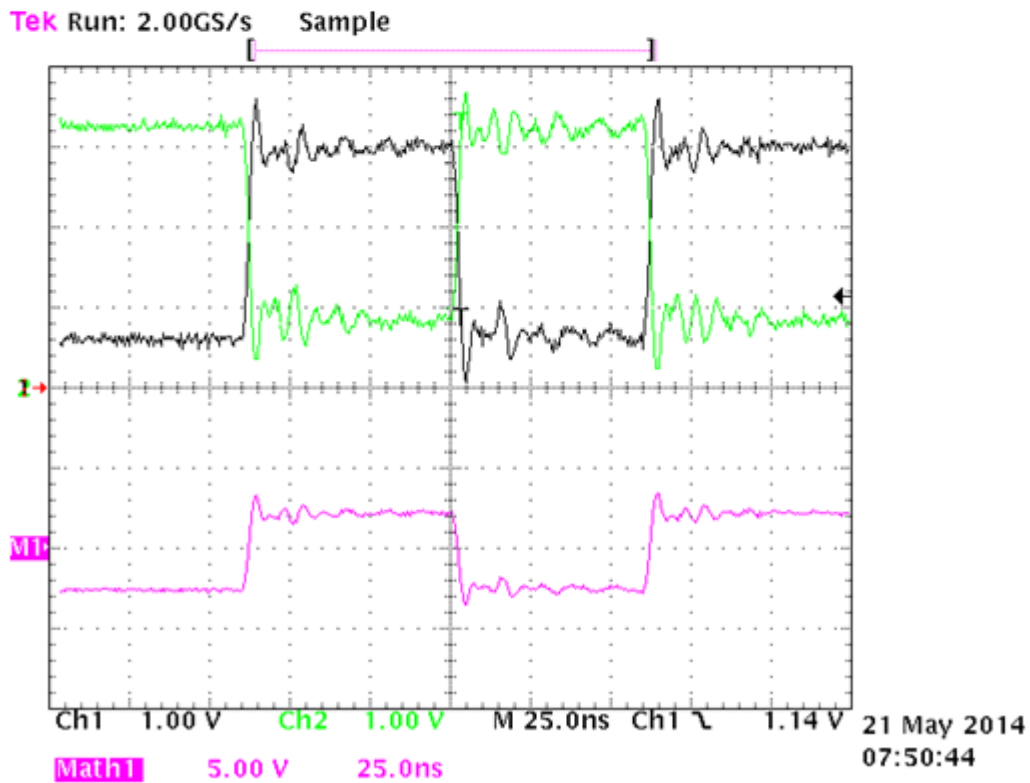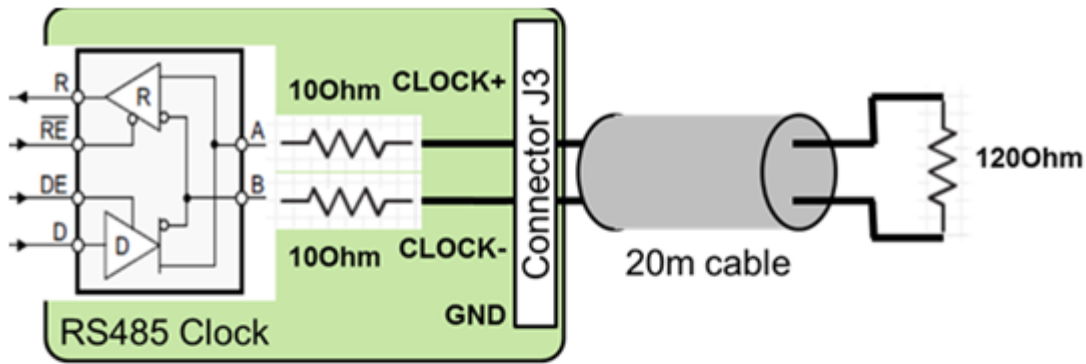
Figure 34. Voltage Versus GND Measured at the SN65HVD78 Differential Output A and B and the Differential Voltage (Ch1 to Ch2) per Signal (M1/Math1) in Data Transmit Mode

Another aspect to analyze is the RS-485 driver and receiver propagation delay, especially the configuration where no delay compensation is implemented. Refer to the red curve on Figure 2. The maximum frequency without delay compensation is 2 MHz. Therefore, the hardware must not contribute to more than 250 ns (border condition). The critical delay is the delay between the master clock and the receive data at the master. The following blocks contribute to this delay:

*   EnDat master serial port (transmit, receive)
*   If added: Buffer or level shifter (transmit, receive)
*   RS-485 master (driver, receiver)
*   Cable (two times the length) typically 5 ns/m in one direction
*   Encoder (slave receive to transmit delay, including RS-485)

With respect to the master implementation on this design, Figure 35 shows the rise and fall times of propagation delay of the SN65HVD78 RS-485 driver and receiver with 120-ohm termination. The driver-receiver pair is measured from logic input to differential output for the driver and in the opposite order for the receiver. There is a different time scale for driver and receiver measurement. The driver propagation delay measured is around 5 ns, and the receiver propagation delay is around 25 ns. The RS-485 master transceiver only contributes to 30 ns to the overall loop delay, which is well below the critical threshold for the configuration without delay compensation.
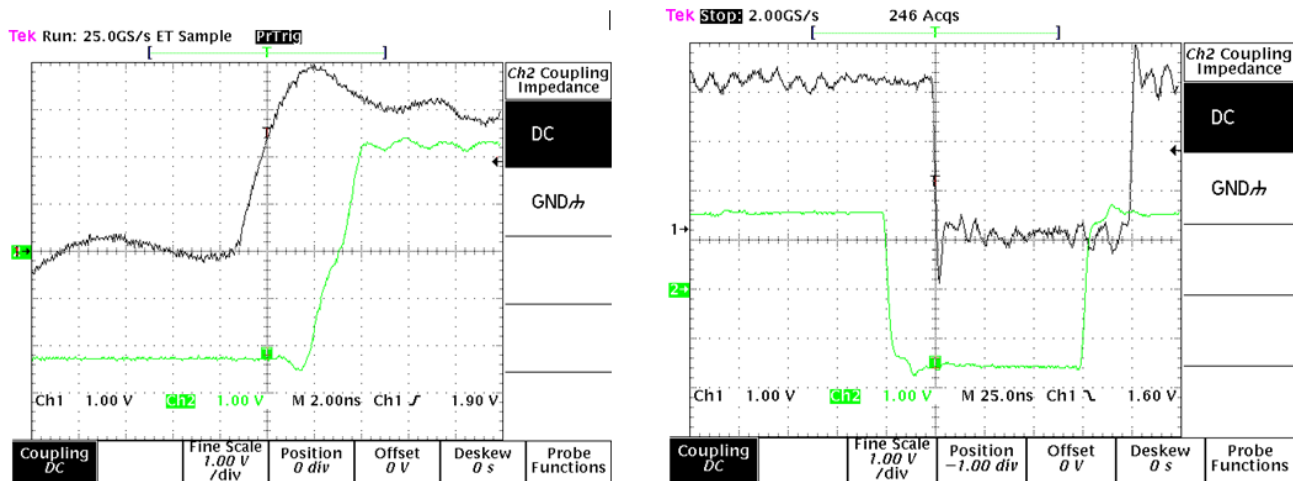
Figure 35. SN65HVD78 Propagation Delay (Driver, Left Figure; Receiver, Right Figure).
Ch1 (Back) = Logic Signal; Ch2 (Green) = Differential Signal

To estimate the cable delay, measurements were conducted with the HEIDENHAIN cable. Propagation times for an 8-MHz clock frequency are shown in Table 11.

Table 11. Encoder Cable Propagation Delay (Both Directions)

CABLE LENGTH	PROPAGATION DELAY, BOTH DIRECTIONS
21 m	210 ns
51 m	505 ns
71 m	715 ns
100 m	1005 ns

The cable propagation delay (around 5 m) will be already dominant versus the RS-485 transceiver. For an 8-MHz clock frequency, the entire loop delay will be approximately 1.1 us. At an 8-MHz clock, this delay equals nine clock periods. In other words, the data is delayed by 9-bits at the master receiver side.

6.1.5   Current Consumption at 3.3 V for RS-485 Transceivers and Level Shifters

In order to estimate the supply current on the 3.3-V rail, consumed by the two RS-485 transceivers and the optional logic level buffers, continuous random data was transmitted over a 20-m cable with a 120-ohm termination on the far end for both data and clock signals.

The effective load for the data transceiver was 60 ohms. The data transceiver was terminated on the master as well. Therefore, the total impedance is 60 ohms (120 ohm in parallel). The clock transceiver was terminated with 120 ohms. The drivers on both RS-485 transceivers were always enabled and active. The typical current consumption was measured from 1 MHz to 16 MHz, which equals the maximum clock frequency per EnDat 2.2.

The total current consumption of the system using 2 × SN65HVD78 and SN74AVC8T245 (per Figure 4) is around 11 mA lower than 2 × SN65HVD10, as expected from the data sheet numbers. Taking the 8-MHz clock (16 Mbps), a result of an average maximum supply current was found of around 26 mA for single SN65HVD78 and 30 mA for SN65HVD10, respectively. The lower current of the SN65HVD78 is due to its lower quiescent current (driver or receiver enabled). For current consumption details, please see the SN65HVD78 data sheet.
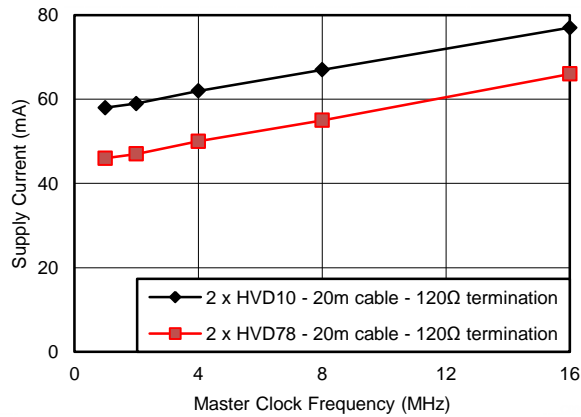

Figure 36. Supply Current (3.3-V Rail) for Subsystem 'RS-485 Transceiver and Logic Interface' Continuous Data Transmission

6.1.6 Encoder Supply Voltage Drop Across the Cable

As calculated in Section 2, an 8-V encoder supply voltage provides sufficient margin to meet EnDat 2.2 minimum supply voltage of 3.6 V. To verify, a test was conducted with a total of 100 m in HEIDENHAIN-shielded EnDat cables, PUR with 4 × 0.14 mm^2 gauge for the differential clock and data signals, and 4 × 0.34 mm^2 for supply and GND. The voltage was measured at the protected encoder output connector (SubD-15) and at the far end of the 100-m cable pending load current. The test used both available wires Up and Up*, as well as Un and Un*, which doubled the effective gauge and results, shown in Figure 37.
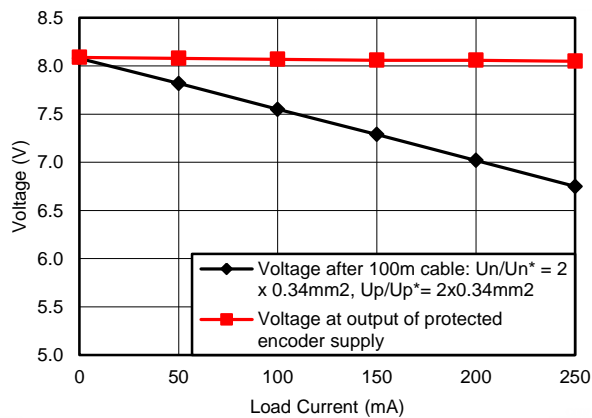
Figure 37. Encoder Supply Voltage Versus Load Current with 100-m Cable

Assuming an encoder with 100-mA average current consumption, the expected effective voltage at 100 m is 7.5 V (parallel supply wires). Therefore, the encoder easily meets the EnDat 2.2 specification (3.6 to 14 V). For more details, please refer to Interfaces to HEIDENHAIN Encoders, pages 33-34.

6.2 *Protected Encoder Power Supply Performance*

6.2.1 Output Ripple

The requirement for the output ripple is to have less than 50 mVpp of ripple on the output voltage at full load. As shown in Figure 38, there is less than 20 mVpp at 200 mA.
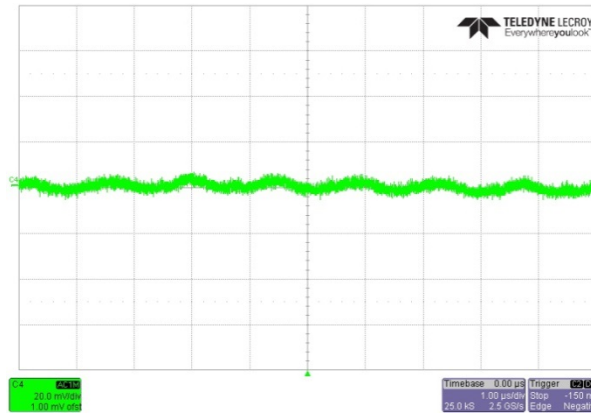

Figure 38. Input: 24 V, Output: 8 V at 200 mA

6.2.2 Output Voltage Characteristics

The requirements on the voltage accuracy need ±5% accuracy on the output voltage. this design uses a voltage between 7.6 and 8.4 V. Shown in Figure 39 and Figure 40, the design meets those specifications and line and load changes are met.
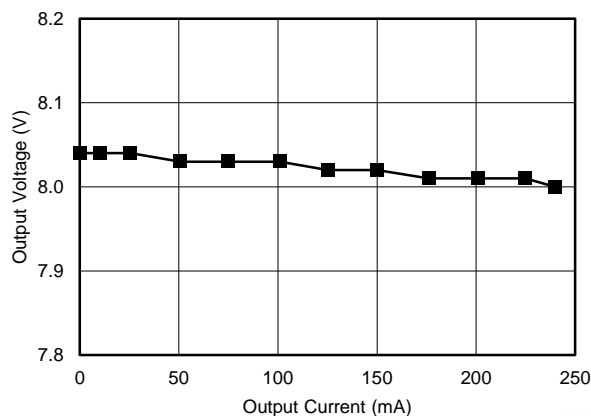
Figure 39. Output Voltage Versus Output Current
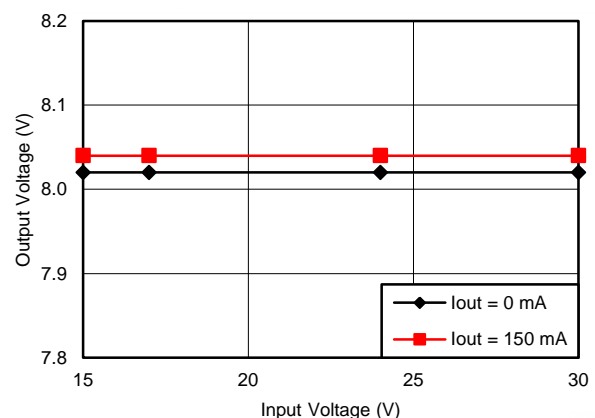
Figure 40. Output Voltage Versus Input Voltage

6.2.3 Efficiency

The efficiency was found by measuring the voltage and current through the input connector (J2) and the voltage and current through the encoder connector (J3).

This efficiency curve includes the input filter, the DC/DC converter (TPS54040A), and the eFUSE (TPS24750).
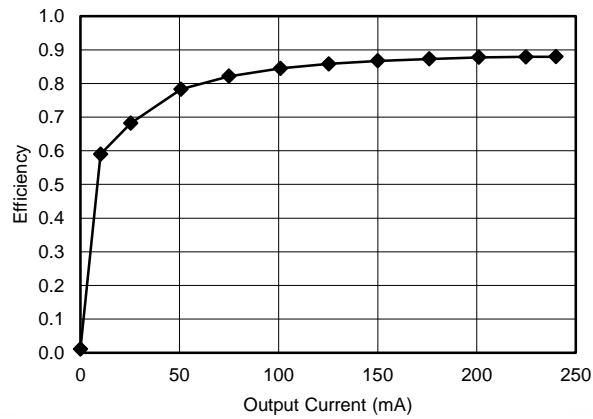
Figure 41. Efficiency

6.2.4   Thermal Image

As a result of the good efficiency, the board did not heat up very much. Figure 42 is the thermal picture done at 25°C room temperature, with a 24-V input and 8 V at 150-mA output.

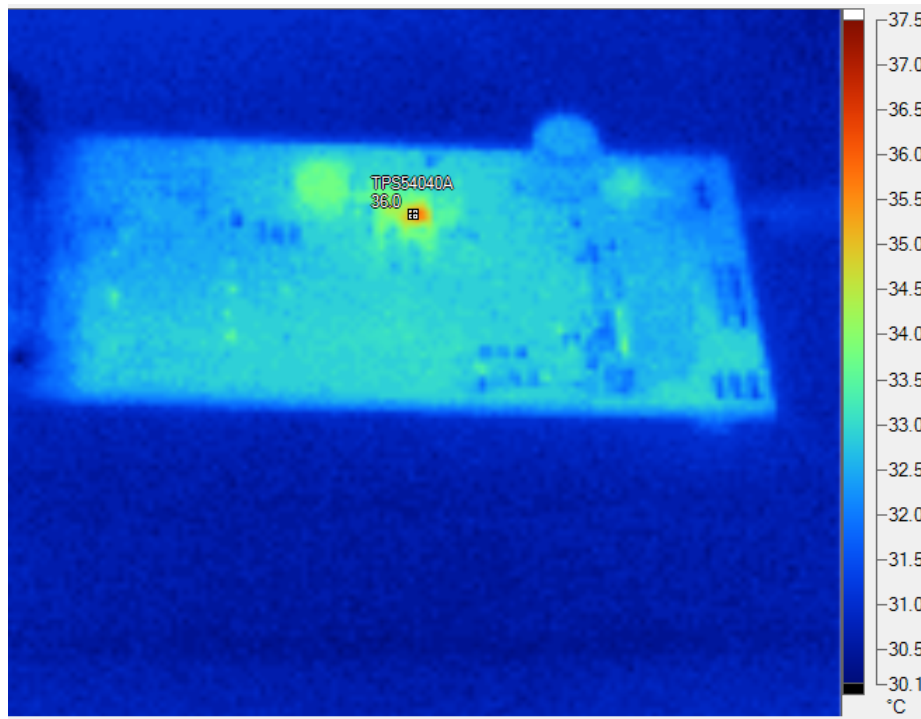The hottest point on the board is the TPS54040A at 36°C.

Figure 42. Thermal Picture

6.2.5   Start-Up

The start-up time of the output voltage at the encoder connector (J3) when enabled is around 2 ms, primarily due to the soft start implemented in TPS54040A. (This soft start can be changed.)

In Figure 43, the blue curve is the enable signal, and the red curve represents the output voltage at the encoder connector (J3).
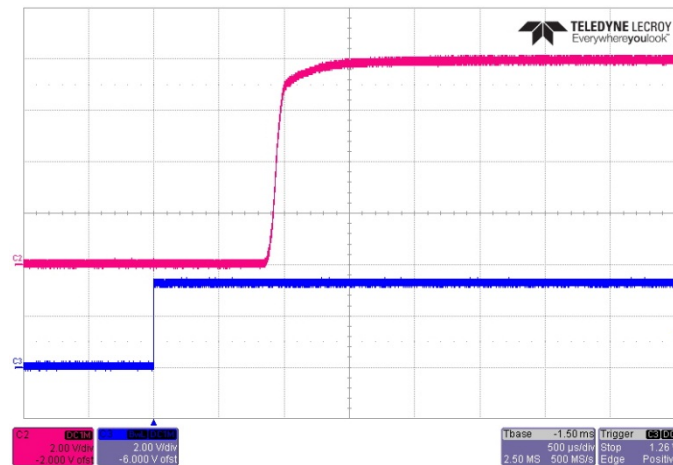
Figure 43. Output Voltage Ramp-Up (Red) with Enable Signal (Blue) Asserted (Input: 24 V, Output: 8 V at 150 mA)

6.2.6 Shutdown

The shutdown time of the output voltage at the encoder connector (J3) is around 1 ms, mainly due to the output capacitors. In Figure 44, the blue curve is the enable signal, and the red curve represents the output voltage at the encoder connector (J3).

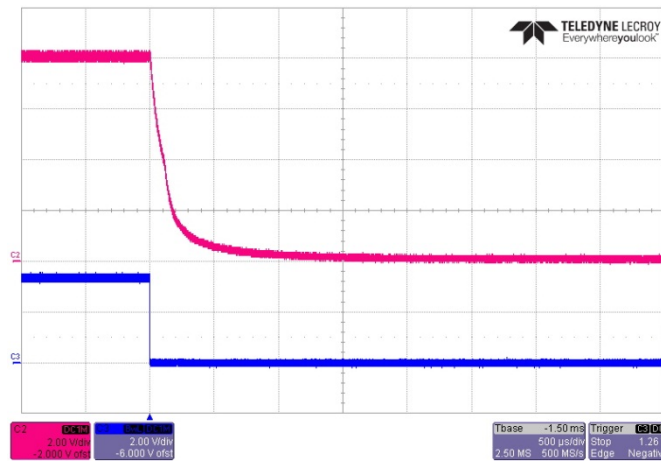**Figure 44. Output Voltage Ramp-down (Red) with Enable Signal (Blue) De-Asserted (Input: 24 V, Output: 8 V at 150 mA)**

6.2.7 Switch Node Waveforms

Figure 45 through Figure 48 are the switch node waveforms at full load and light load. These curves were measured across Diode D2.
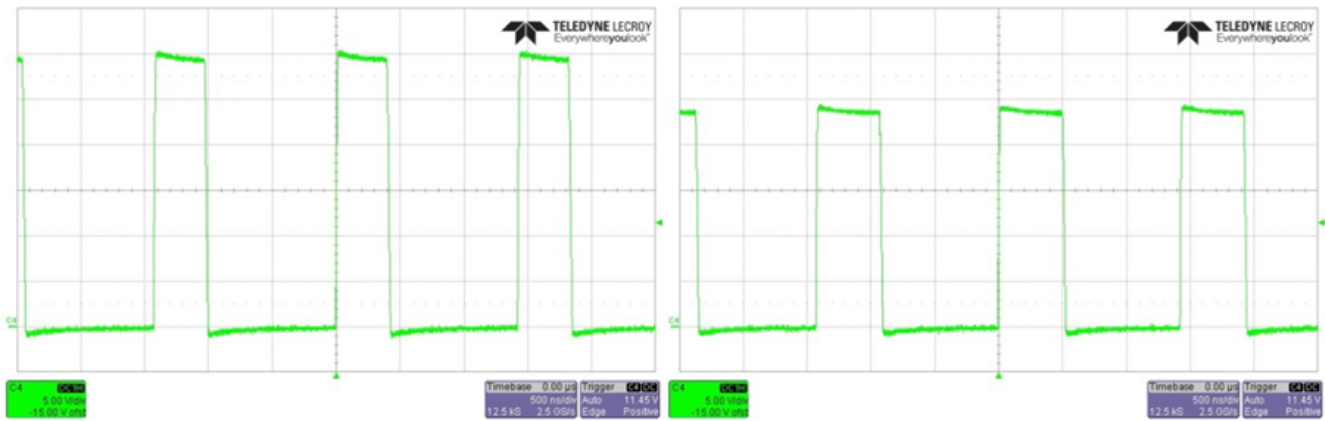
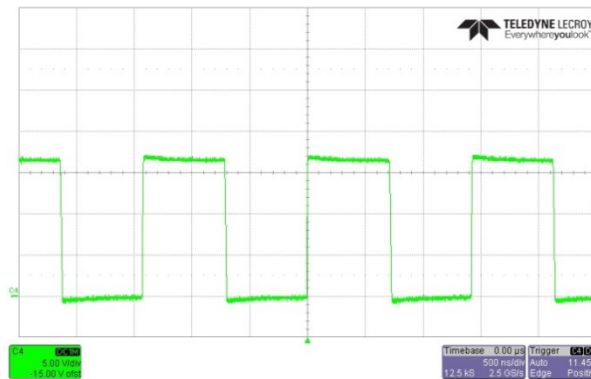**Figure 45. Output 8 V at 200 mA, Input voltage: 30 V (Left Figure), 24 V (Right Figure)**
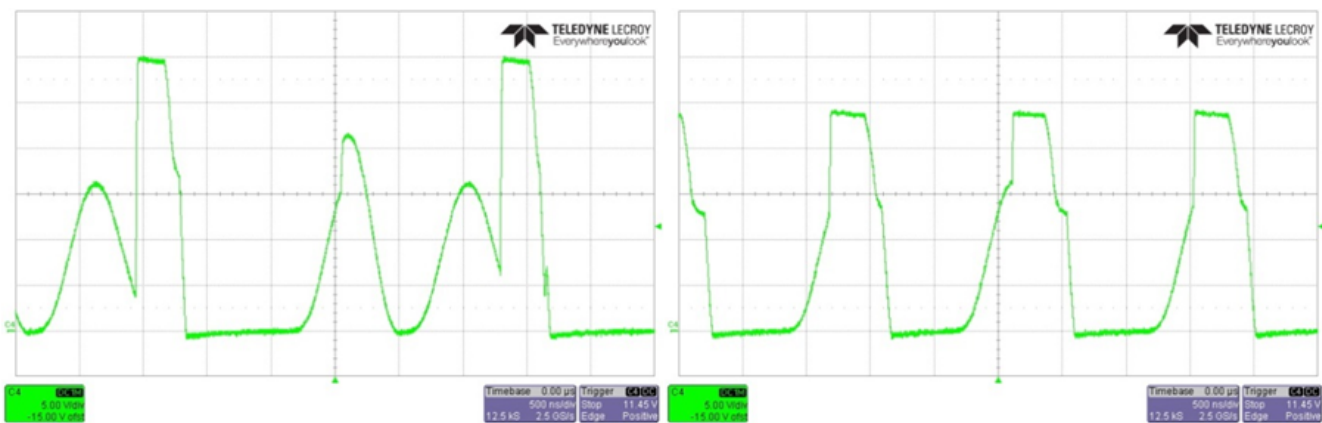

Figure 46. Output 8 V at 200 mA, Input voltage: 17 V

Figure 47. Output 8 V at 10 mA, Input Voltage: 30 V (Left Figure), 24 V (Right Figure)
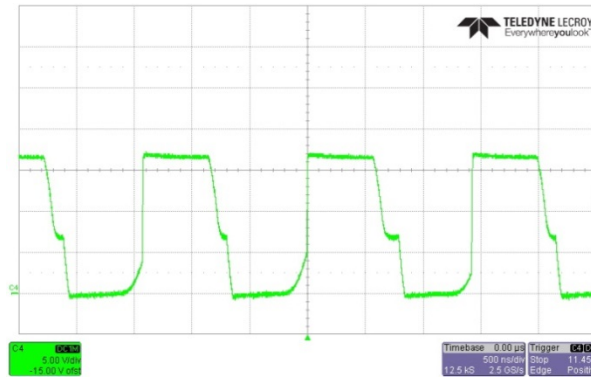
Figure 48. Output 8 V at 10 mA, Input Voltage: 17 V

6.2.8 Bode Plots

The bode plots in Figure 49 and Figure 50 verify that the loop is stable. The bode plots have been measured for the 24-V nominal input voltage as well as for a lower input voltage limit of 17 V and an upper limit of 30 V. The output voltage was 8 V as well. The design has enough of a phase and gain margin for the entire input voltage range, shown in Table 12.

Table 12. Phase and Gain Margin

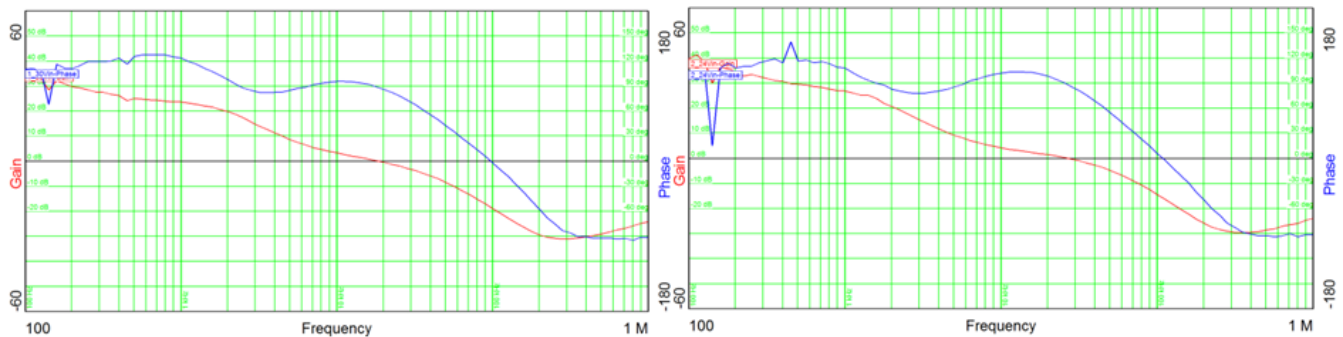| VOLTAGE	PHASE MARGIN	GAIN MARGIN
Input: 30 V, output: 8 V at 200 mA	86 degrees	−18 dB
Input: 24 V, output: 8 V at 200 mA	85 degrees	−15 dB
Input: 17 V, output: 8 V at 200 mA	85 degrees	−16 dB

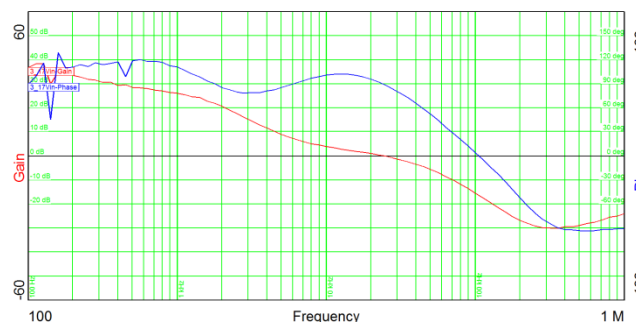**Figure 49. Bode Plot: Input Voltage: 30 V (Left Figure), 24 V (Right Figure)**

Figure 50. Bode Plot: Input Voltage: 17 V

6.2.9   Overpower Protection

This test used a 24-V input, 8-V output. The current was increased until the power protection was triggered. The power protection was triggered at 246 mA, meaning the power protection was triggered at 1.968 W.

In Figure 51, the blue waveform is the fault signal Enc_PWR_Fault on connector J5, and the red waveform is the output voltage at the encoder connector (J3).
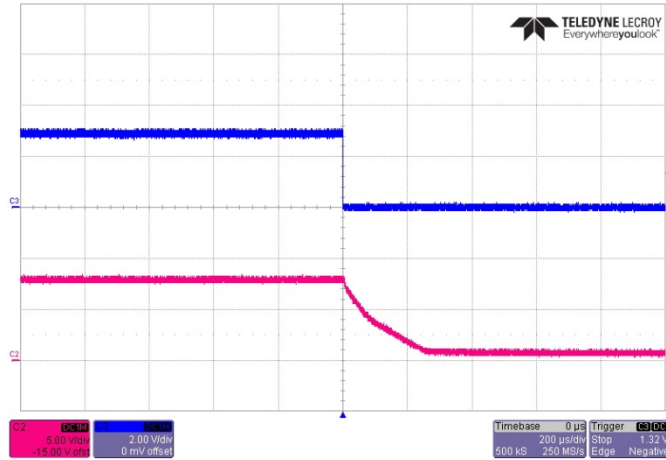

Figure 51. Output Voltage Shutdown (Red) During an Overpower Event (Power-Limit: 2 W, Input: 24 V, Output: 8 V)

6.3 System Performance with HEIDENHAIN Encoders

6.3.1 HEIDENHAIN Encoders Test Setup

In order to do a system test with the TIDA-00172 analog interface with EnDat 2.2 position encoder, a TI-internal EnDat 2.2 master implementation on Sitara™ AM4x Cortex A9 was used. The Sitara AM4x processors run at 1 GHz and feature a new generation of programmable real-time unit (PRU) subsystems that enable simultaneous industrial ethernet protocols and motor feedback protocols, such as EnDat. The TIDA-00172 design was connected to four of the AM4x GPIO ports of ICSS0_PRU0 for the four logic-level EnDat 2.2 signals.
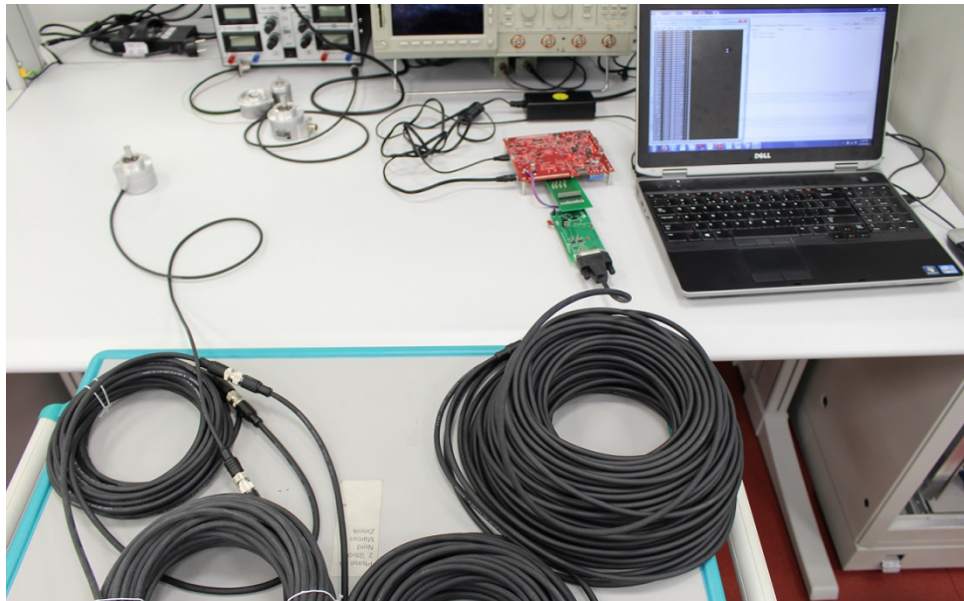

Figure 52. Setup for TIDA-00172 Test With HEIDENHAIN Encoders

Table 13. Test Equipment

TEST EQUIPMENT	PART NUMBER
HEIDENHAIN EnDat 2.2 position encoders	ROQ437, ROQ1035, ROC425, EQI1331
HEIDENHAIN shielded EnDat cables, PUR (4 × 0.14 mm^2, 4 × 0.34 mm^2), 10 m, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable 1m	524599-1
EnDat 2.2 master (internal evaluation TI software)	Sitara™ AM4x IDK EVM (internal TI)

6.3.2 HEIDENHAIN Encoders Test Results

The four HEIDENHAIN EnDat 2.2 encoders listed in Table 13 were measured to verify error-free communication at a maximum 8-MHz clock rate, which was the maximum specified clock frequency of these position encoders.

Internal evaluation software running the EnDat 2.2 master on the Sitara AM4x ICSS PRU0 peripheral was used.

A UART was implemented on Sitara AM4x to periodically transmit the number of position request, the turns, and position value, as well as the overall RX CRC count.
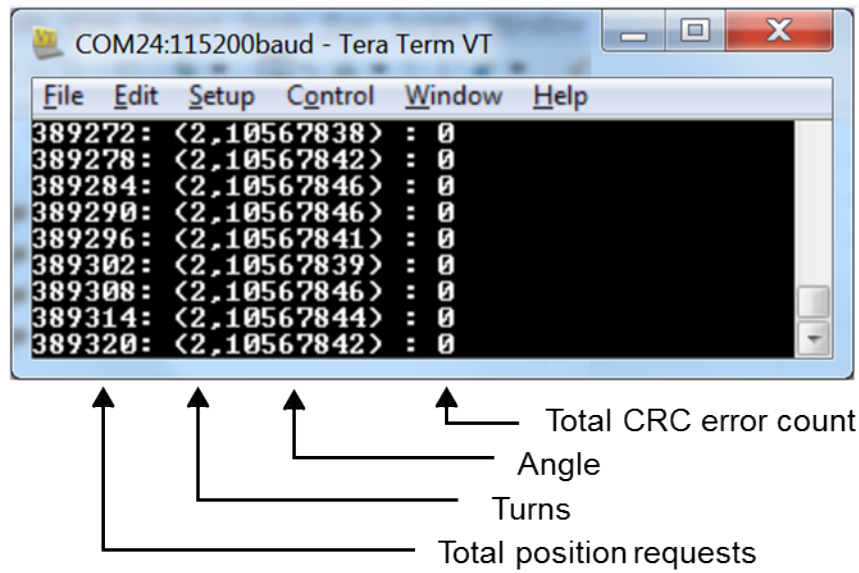
Figure 53. Sitara AM4x UART Output

An 8-MHz EnDat 2.2 clock frequency with error-free communication from 1-m up to 90-m cable length was successfully achieved. Only at 100 m did the master clock frequency have to be reduced to 4 MHz for ROQ437 and EQI1331 and 1 MHz with ROQ1035 and ROC425.
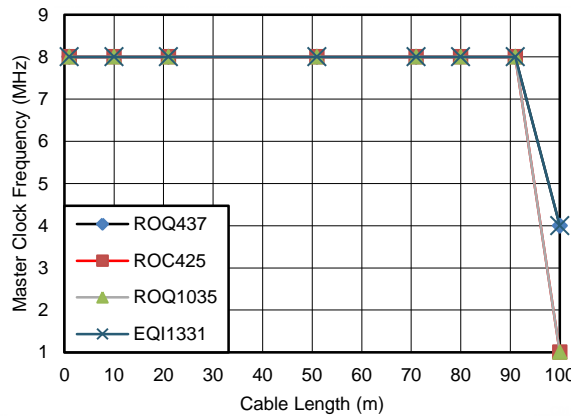

Figure 54. Master Clock Frequency With EnDat 2.2 Encoders with Zero CRC Errors

NOTE: The delay compensation with this initial software was yet not optimized for a cable length greater than 90 m. With a later software fix, 8 MHz at 100 m can be expected as well.

To verify the startup and shutdown of the encoder power supply, the voltage was measured at the encoder SubD-15 connector J3 pin 4 (signal Up) and pin 2 (signal Un/GND) with a 20-m cable and the HEIDENHAIN EnDat 2.2 encoder ROQ437 connected. The Enc_PWR_Enable signal, which enables and disables (or disconnects) the encoder supply voltage, was set and reset. The scope plot in Figure 55 shows the waveform with Enc_PWR_Enable on Ch1 and Up on Ch2. The startup and shutdown of the protected encoder supply with ROQ437 encoder connected is around 1.7 ms.
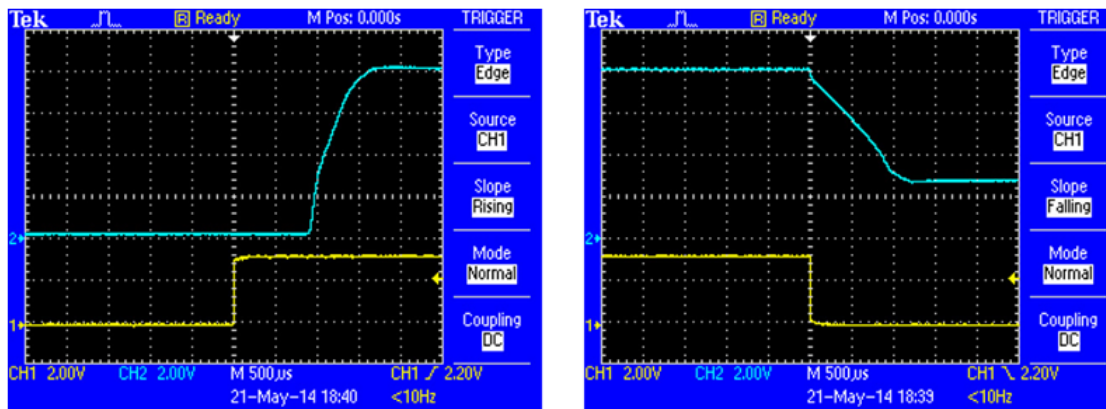
Figure 55. Encoder Power Supply Voltage Measured J3 Pin 4 (Up) at Start-Up (Left Figure) and Shutdown (Right Figure)

6.4 *EMC Test Results*

The design was tested according to IEC61800-3 for ESD, EFT, and Surge with reference to standard IEC61000-4-2, IEC61000-4-4, IEC61000-4-5, respectively.
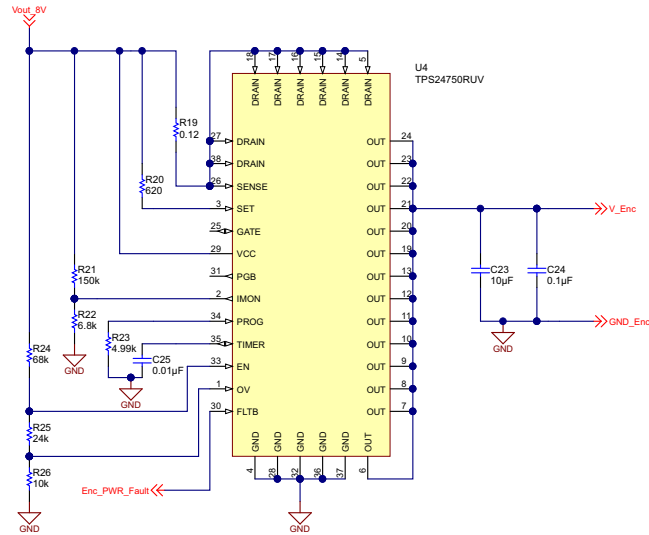
See EMC test results document at TIDA-00172.

7 Design Files

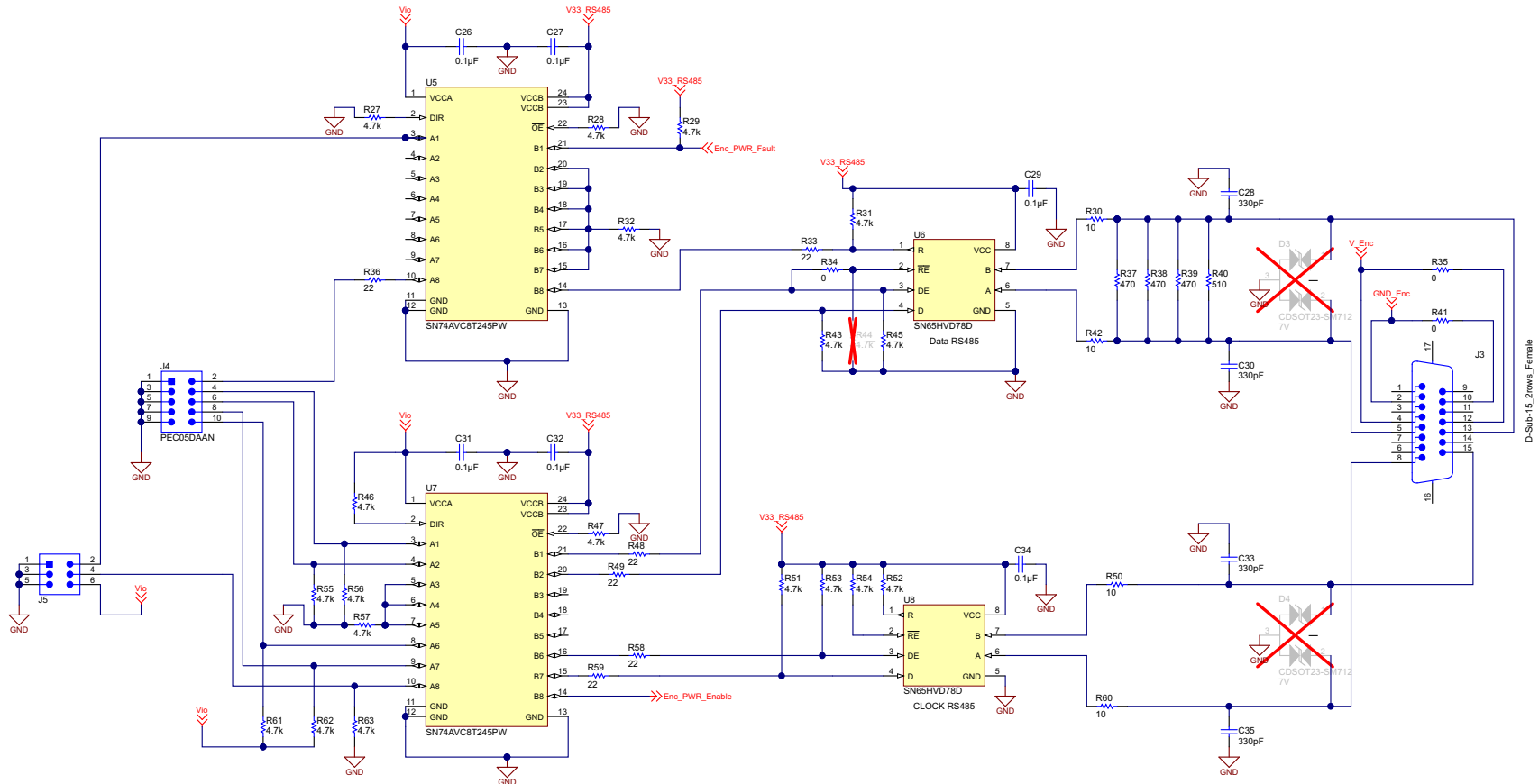## 7.1 Schematics

Figure 56. Power Supply

Figure 57. eFUSE

Figure 58. Signal Chain

7.2 Bill of Materials

Table 14. BOM

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QUANTITY
C1, C21, C22	CAP, CERM, 0.1 uF, 16 V, ±10%, X5R, 0603	MuRata	GRM188R61C104KA01D	3
C2, C3, C23	CAP, CERM, 10 uF, 25 V, ±10%, X5R, 0805	TDK	C2012X5R1E106K125AB	3
C5, C6	CAP, CERM, 1 uF, 50 V, ±10%, X7R, 0805	MuRata	GRM21BR71H105KA12L	2
C7, C8, C15, C16	CAP, CERM, 2.2 uF, 50 V, ±10%, X5R, 1206	MuRata	GRM31CR61H225KA88L	4
C9	CAP, AL, 100 uF, 63 V, ±20%, 0.35 ohm, SMD	Panasonic	EEE-FK1J101P	1
C11	CAP, CERM, 2200 pF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C222KA01D	1
C13	CAP, CERM, 12 pF, 50 V, ±5%, C0G/NP0, 0603	MuRata	GRM1885C1H120JA01D	1
C14, C25	CAP, CERM, 0.01 uF, 50 V, ±10%, X7R, 0603	MuRata	GRM188R71H103KA01D	2
C17, C18	CAP, CERM, 10 uF, 10 V, ±20%, X5R, 0603	TDK	C1608X5R1A106M	2
C20	CAP, CERM, 0.033 uF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
C24	CAP, CERM, 0.1 uF, 25 V, ±10%, X7R, 0603	TDK	C1608X7R1E104K	1
C26, C27, C29, C31, C32, C34	CAP, CERM, 0.1 uF, 25 V, ±10%, X5R, 0603	AVX	06033D104KAT2A	6
C28, C30, C33, C35	CAP, CERM, 330 pF, 50 V, ±10%, X7R, 0603	MuRata	GRM188R71H331KA01D	4
D1, D2	Diode, Schottky, 60 V, 1 A, SMA	ON Semiconductor	MBRA160T3G	2
J1	Terminal Block, 6 A, 3.5-mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	1
J2	Header, 100 mil, 3 × 1, Tin plated, TH	Sullins Connector Solutions	PEC03SAAN	1
J3	D-Sub-15, 17Pos, TH	Harting	09 66 252 6610	1
J4	Header, 100 mil, 5 × 2, Tin plated, TH	Sullins Connector Solutions	PEC05DAAN	1
J5	Header, 100 mil, 3 × 2, Tin, TH	Sullins Connector Solutions	PEC03DAAN	1
L1	Inductor, Shielded Drum Core, Ferrite, 150 uH, 0.7 A, 0.57 ohm, SMD	Wurth Elektronik eiSos	7447713151	1

Table 14. BOM (continued)

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QUANTITY
L2	Inductor, Wirewound, Ferrite, 4.7 uH, 0.9 A, 0.2 ohm, SMD	TDK	NLCV32T-4R7M-PFR	1
R1, R30, R42, R50, R60	RES, 10 ohm, 5%, 0.25 W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	5
R2, R3, R13, R34, R35, R41	RES, 0 ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	6
R5, R27, R28, R29, R31, R32, R43, R45, R46, R47, R51, R52, R53, R54, R55, R56, R57, R61, R62, R63	RES, 4.7 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06034K70JNEA	20
R7, R11	RES, 51 ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060351R0JNEA	2
R8	RES, 39 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060339K0JNEA	1
R9	RES, 165 k ohm, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603165KFKEA	1
R10, R14	RES, 90.9 k ohm, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060390K9FKEA	2
R12, R18	RES, 10.0 k ohm, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	2
R15	RES, 15.4 k ohm, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060315K4FKEA	1
R16, R23	RES, 4.99 k ohm, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K99FKEA	2
R17	RES, 36.5 k ohm, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060336K5FKEA	1
R19	RES, 0.12 ohm, 1%, 0.1 W, 0603	Panasonic	ERJ-3RSFR12V	1
R20	RES, 620 ohm, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07620RL	1
R21	RES, 150 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603150KJNEA	1
R22	RES, 6.8 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06036K80JNEA	1
R24	RES, 68 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060368K0JNEA	1
R25	RES, 24 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060324K0JNEA	1
R26	RES, 10 k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	1
R33, R36, R48, R49, R58, R59	RES, 22 ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060322R0JNEA	6
R37, R38, R39	RES, 470 ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603470RJNEA	3
R40	RES, 510 ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603510RJNEA	1
TP1, TP2	Test Point, Miniature, Red, TH	Keystone	5000	2
U1	0.5 A, 42 V Step Down DC/DC Converter with Eco-mode, DGQ0010D	Texas Instruments	TPS54040ADGQ	1
U2	1A SIMPLE SWITCHER® Power Module with 42-V Maximum Input Voltage for Military and Rugged Applications, 7-pin TO-PMOD	National Semiconductor	LMZ14201EXTTZ/NOPB	1
U3	200-mA, Low-IQ, LDO Regulator for Portable Devices, DDC0005A	Texas Instruments	TLV70025DDC	1

Table 14. BOM (continued)

| DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QUANTITY
U4	2.5 to 18-V Positive Voltage 10-A Integrated Hot-Swap Controller, RUV0036A	Texas Instruments	TPS24750RUV	1
U5, U7	8-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs, PW0024A	Texas Instruments	SN74AVC8T245PW	2
U6, U8	3.3-V Supply RS-485 with IEC ESD Protection, D0008A	Texas Instruments	SN65HVD78D	2

7.3   Assembly Drawings
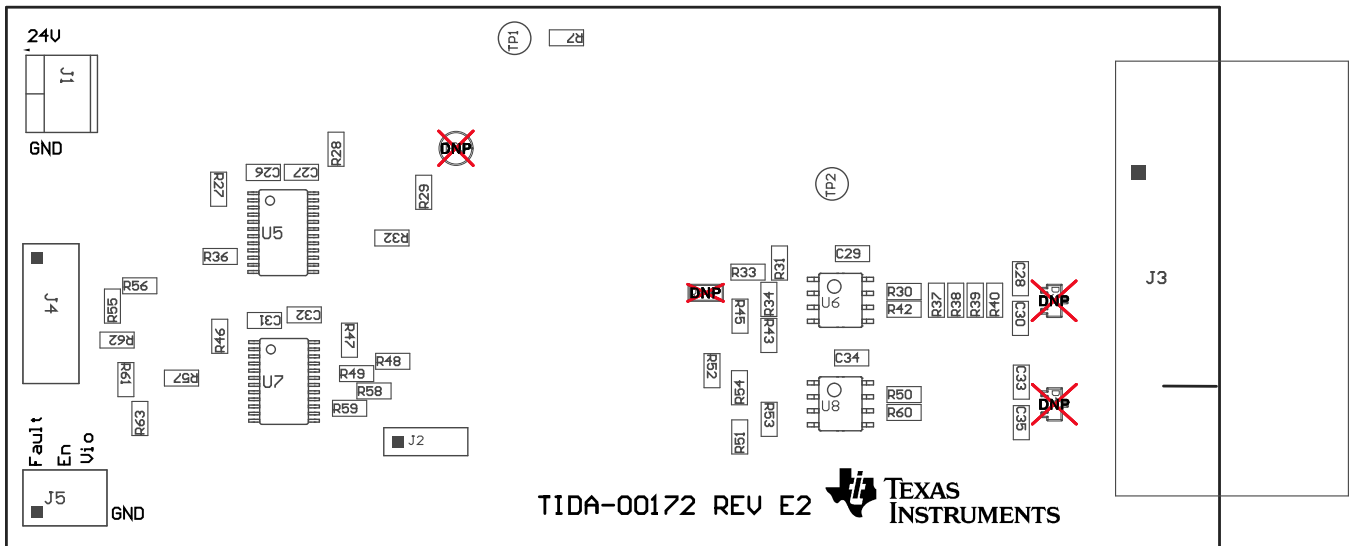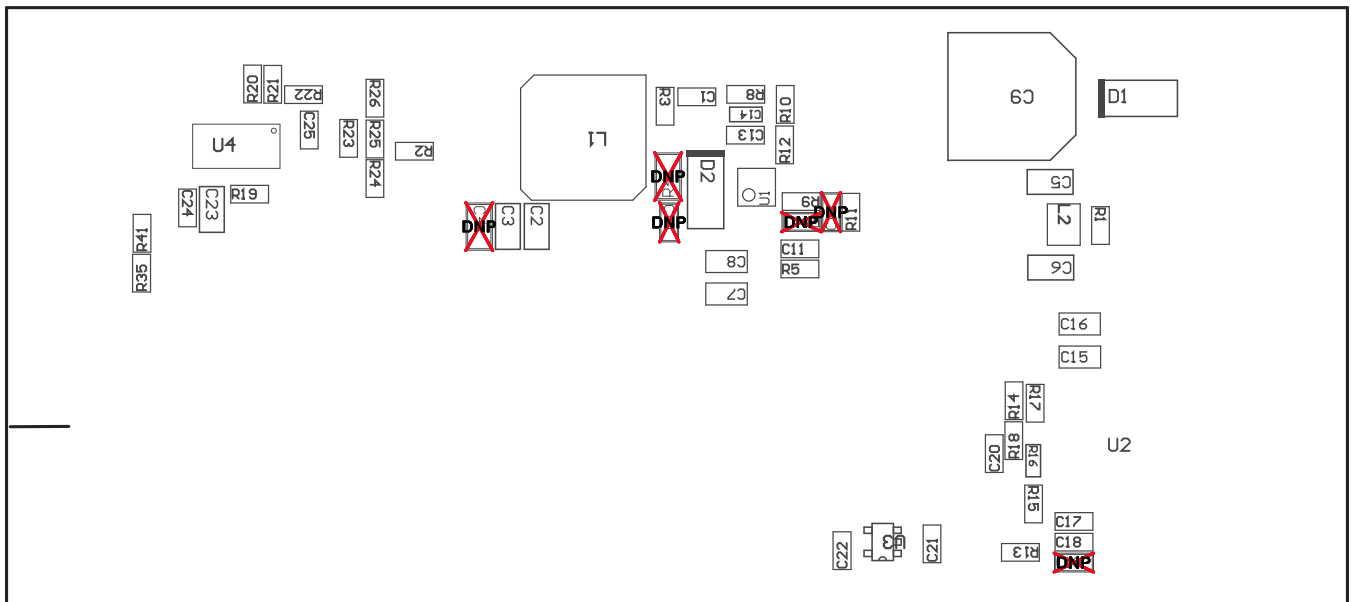

Figure 59. Top Assembly Drawing

Figure 60. Bottom Assembly Drawing
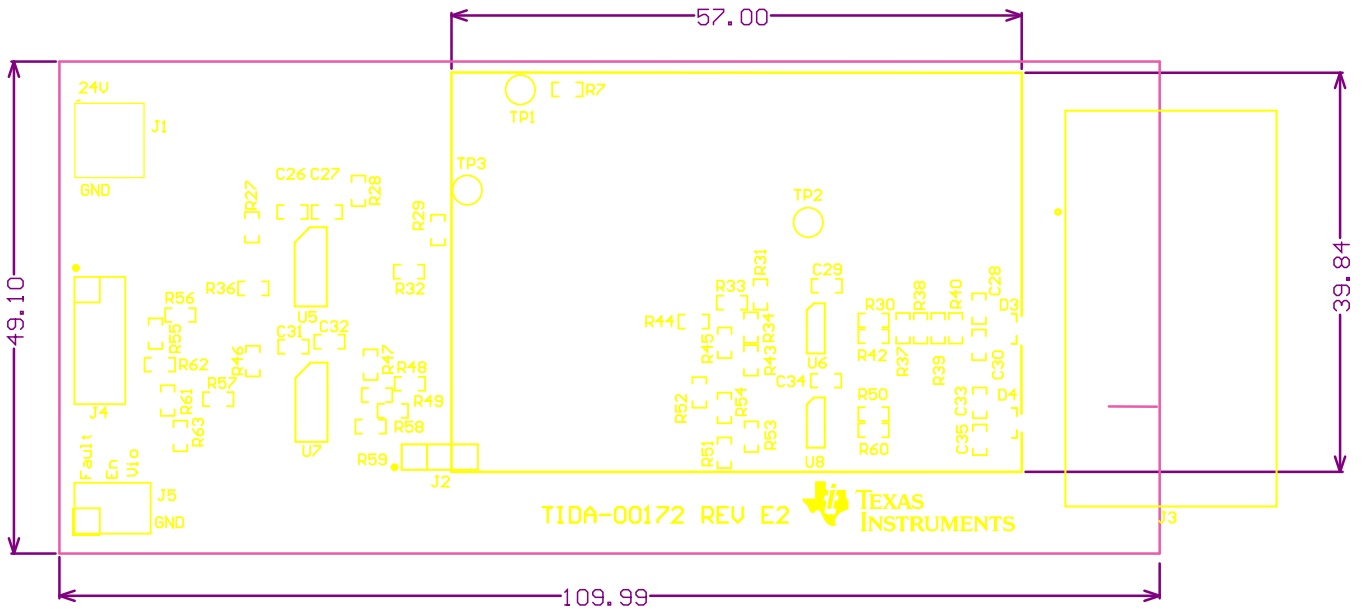
7.4 PCB Layer Plots
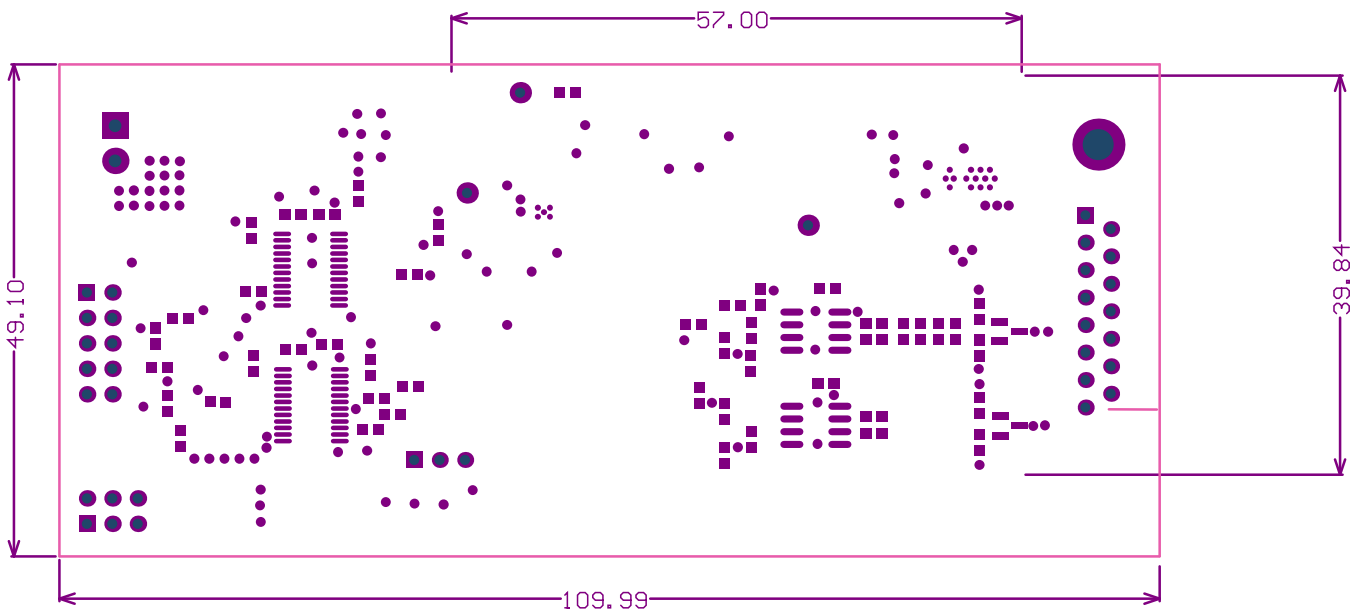

Figure 61. Top Overlay
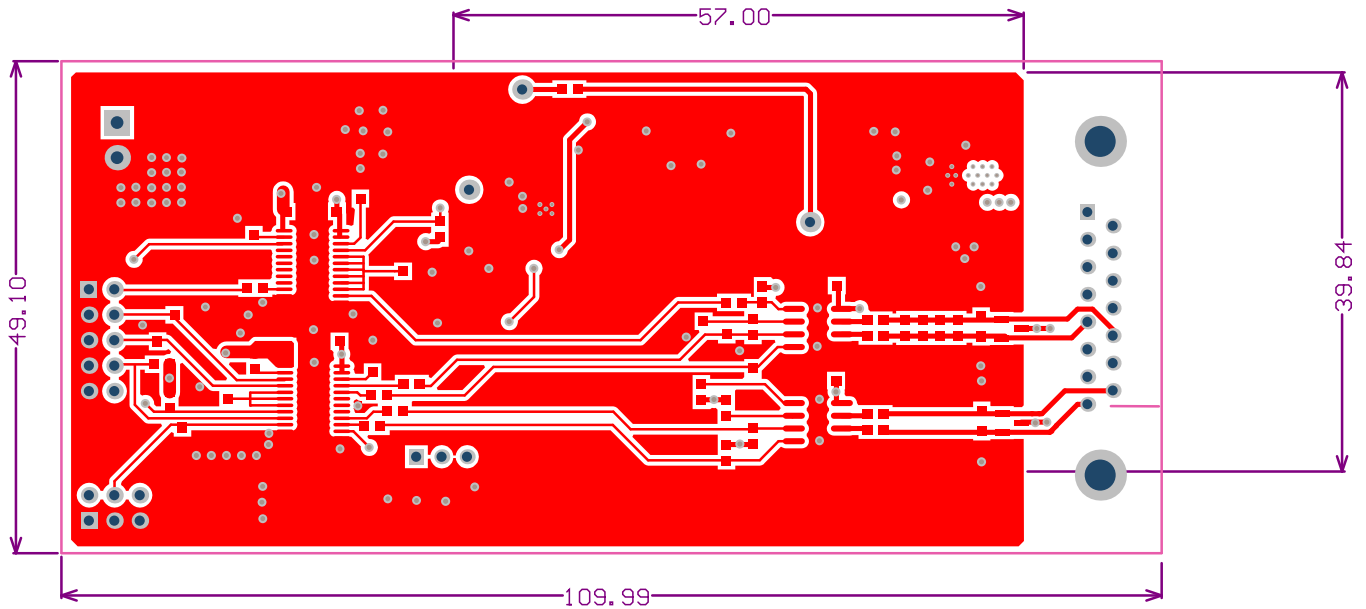

Figure 62. Top Solder Mask
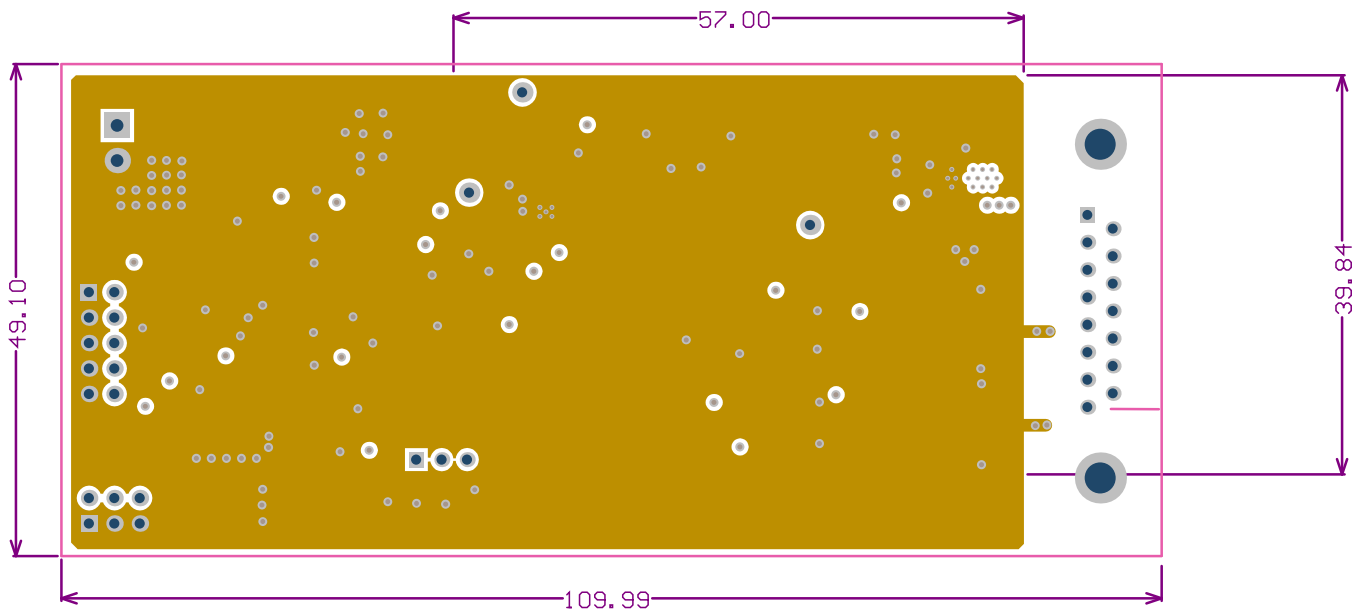
Figure 63. Layer 3: Top Layer

Figure 64. Mid Layer 1: GND
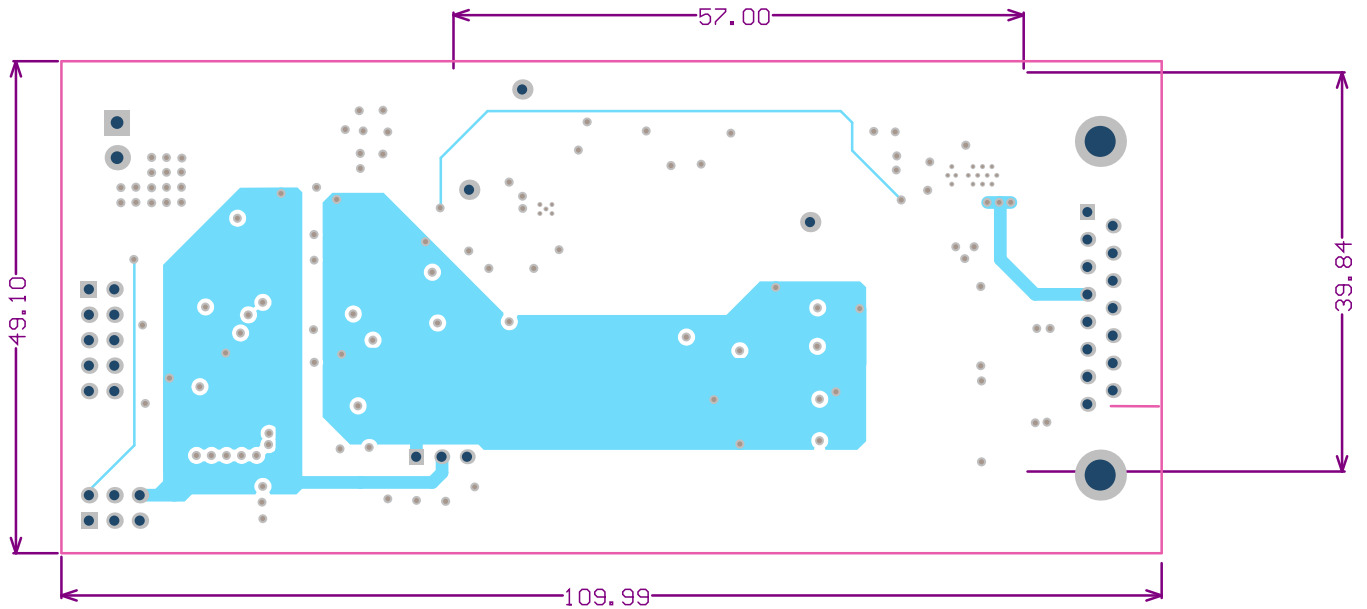
Figure 65. Mid Layer 2: V$_{CC}$
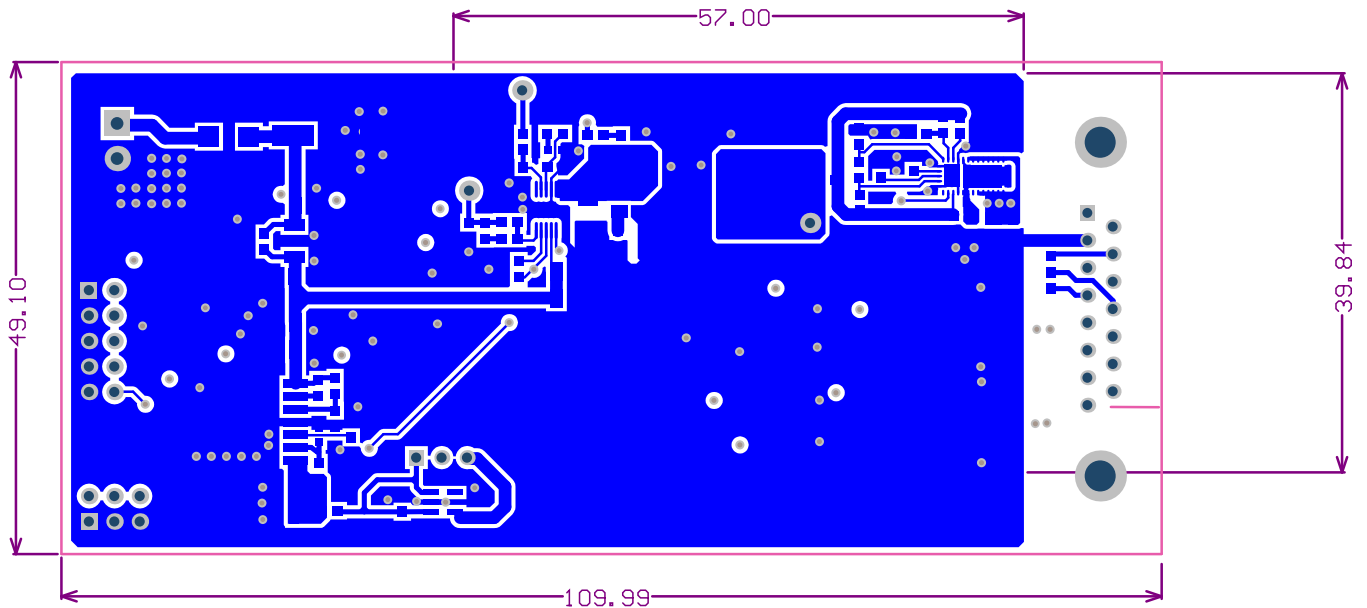
Figure 66. Bottom Layer
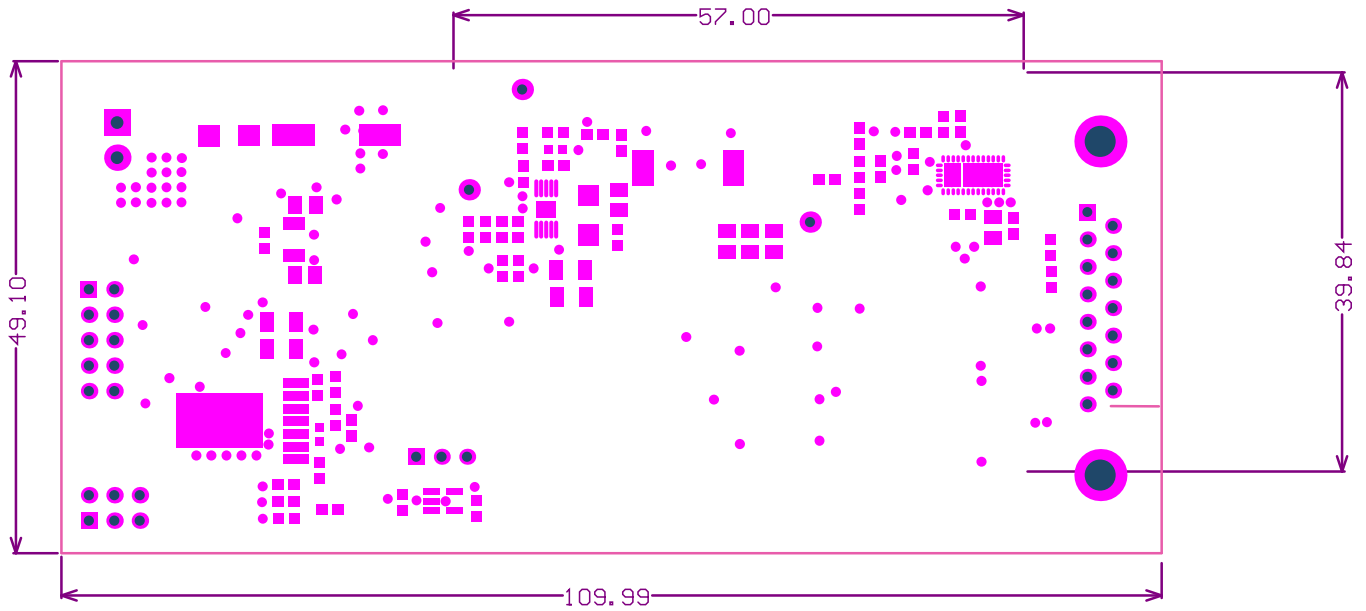
Figure 67. Bottom Solder Mask
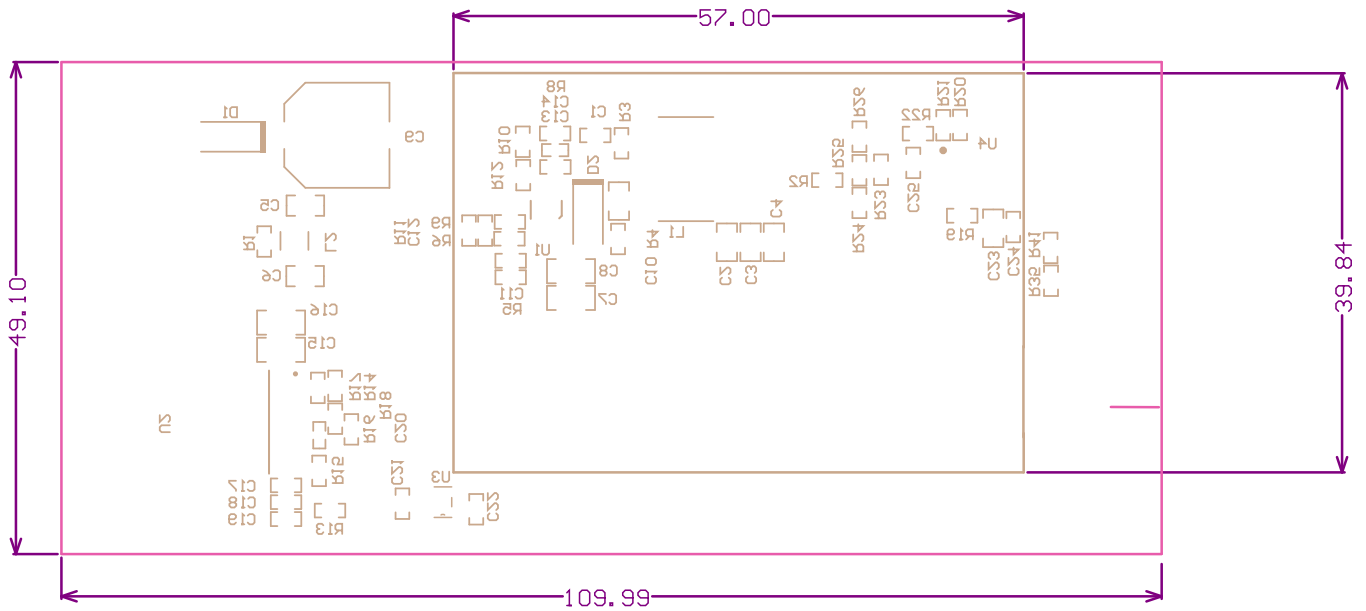
Figure 68. Bottom Overlay
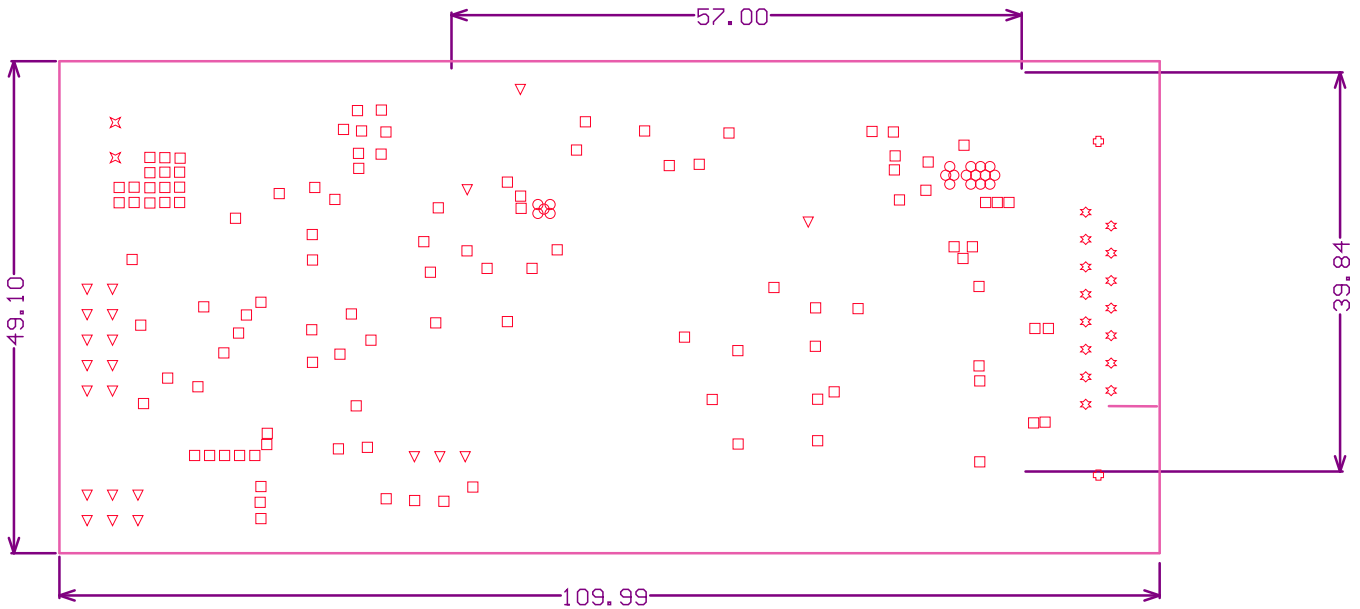
Figure 69. Drill Drawing

7.5   Layout Guidelines

100-nF bypass capacitors as close as possible connected to the V_{CC}-pin and GND-pin without any via to minimize inductance.

Keep the four termination resistors with effective 120 Ωs close to each other and close to SN65HVD78.

4k7 pull-up/pull-down resistors for enable lines to limit noise currents in theses lines during transient events.

Routed differential lines DATA+ and CLOCK− parallel and close to each other.

Pulse-proof resistors into the A and B bus lines to limit the residual clamping current into the transceiver during EFT or surge event.

Use solid V_{CC} (Mid Layer 2) and ground (Mid Layer 1) to provide low-inductance.

SN65HVD78

Figure 70. Layer 1: Top Layer, RS-485 Transceiver Section
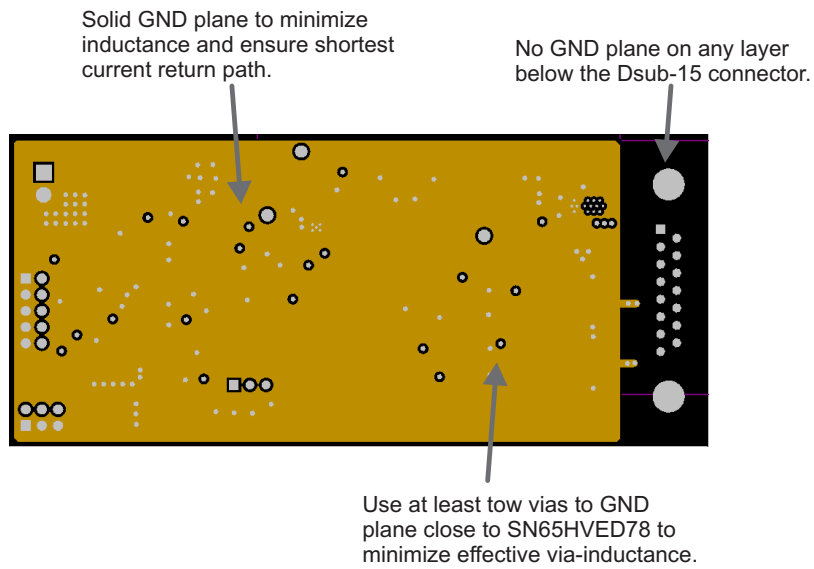
Figure 71. Layer 2: GND Layer
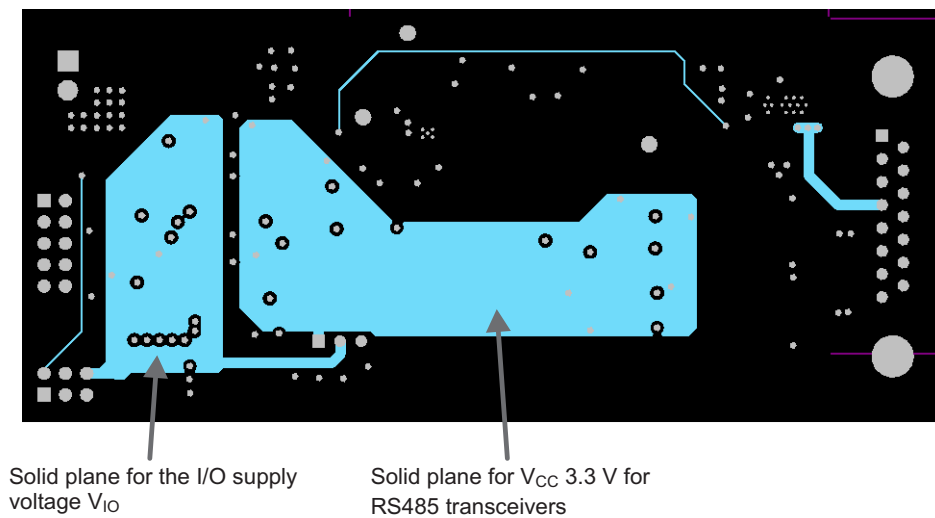
Figure 72. Layer 3: Supply Voltage Layer

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TPS24750 with vias for power dissipation through PCB.

TPS54040A: Since the PH-pin connection is the switching node, the catch diode and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized ro prevent excessive capacitive coupling.

TPS54040A: The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.

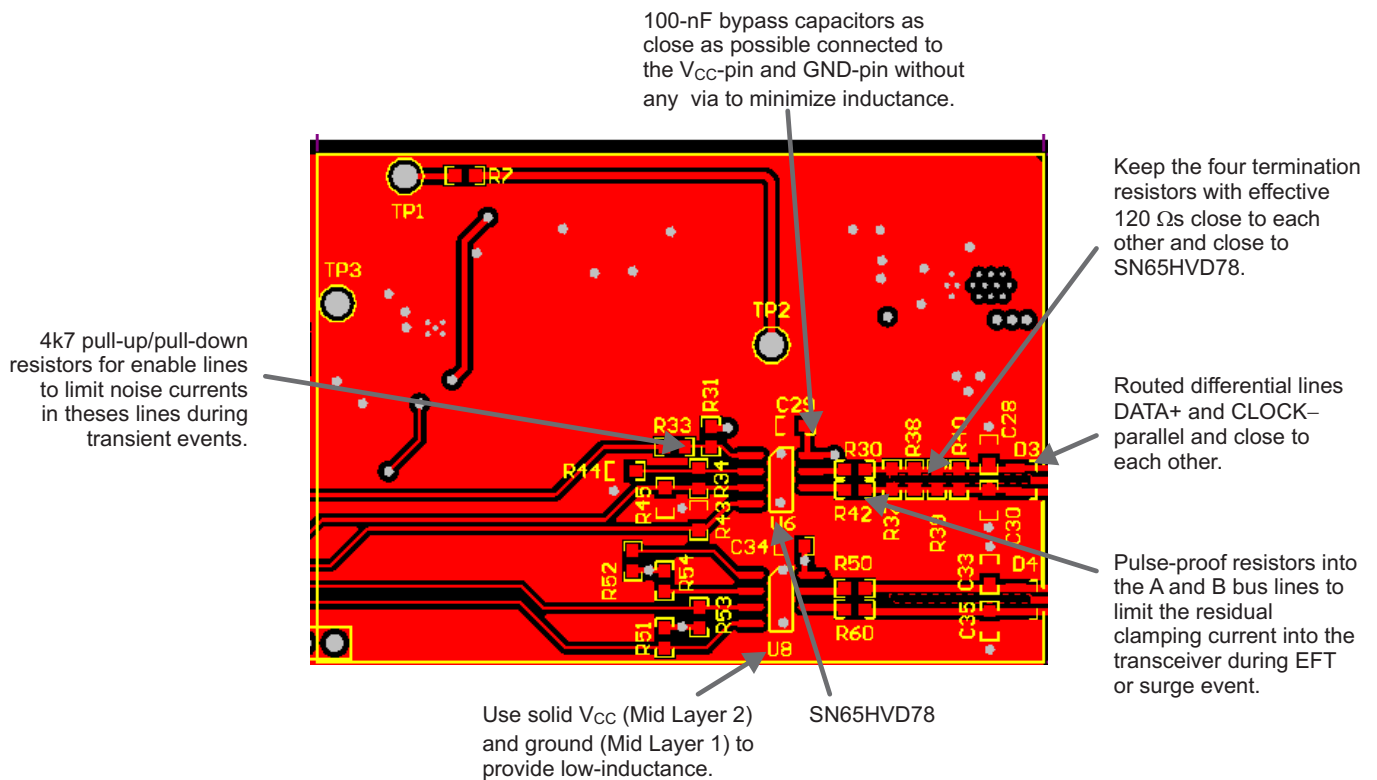TPS54040A: The GND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC.
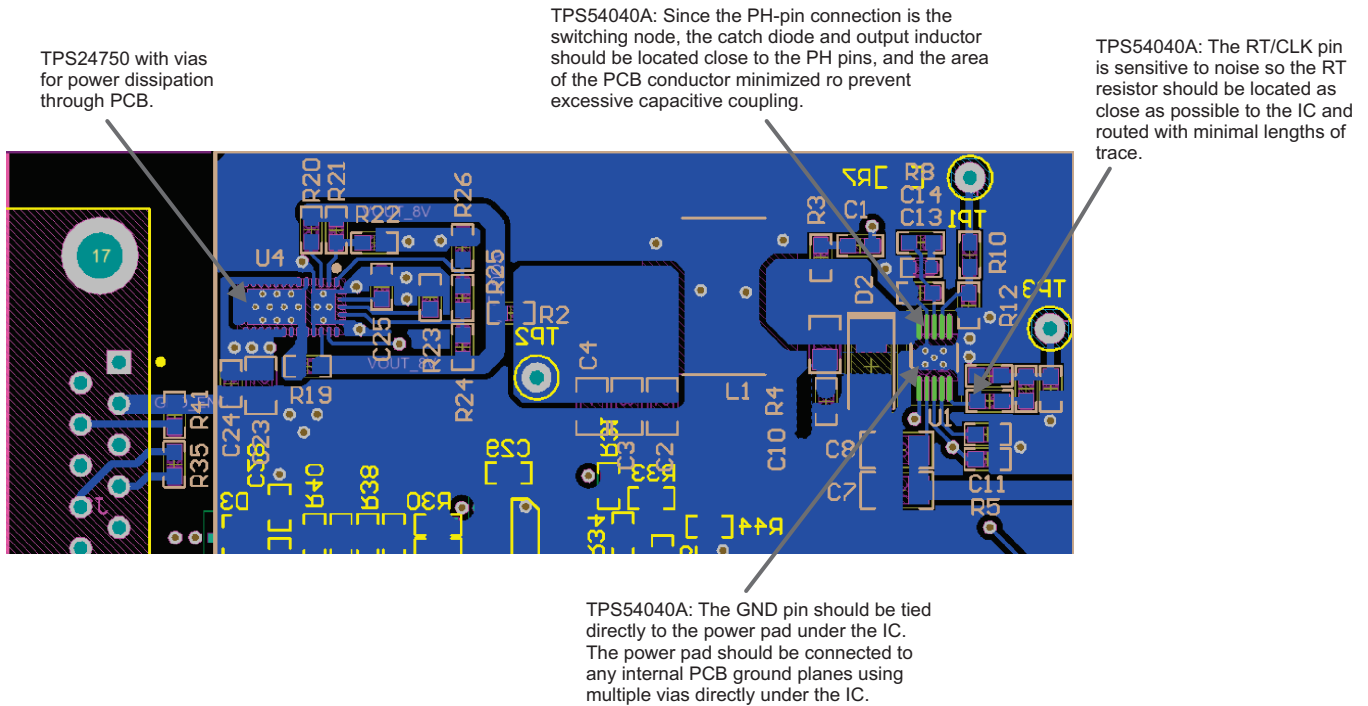
Figure 73. Layer 4: Bottom Layer, Protected Power Supply Section

NOTE: Layer 4 is flipped to have real view from bottom.

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00172.

7.7 Altium Files

To download the Altium database, see the design files at TIDA-00172.
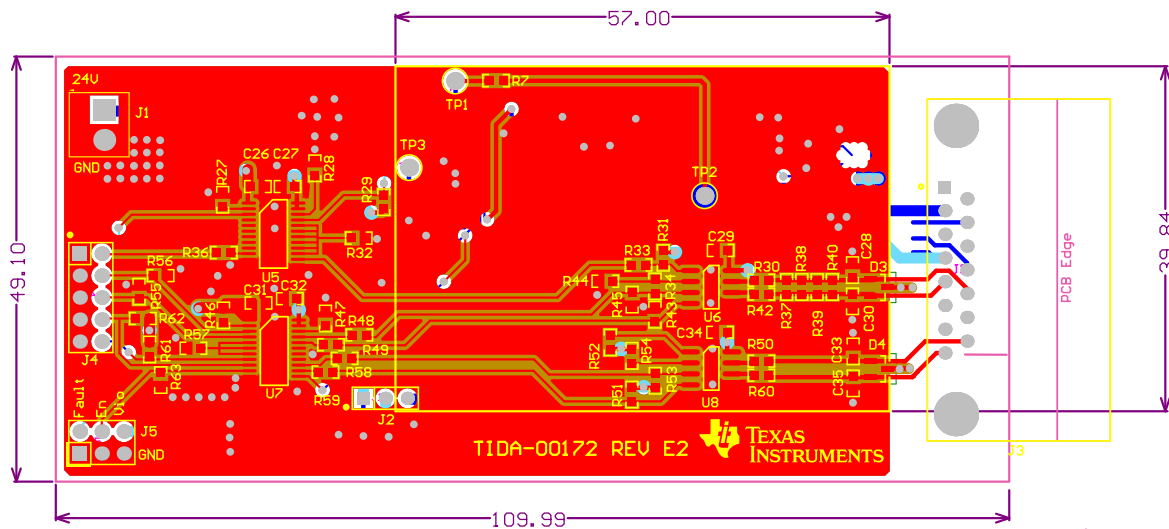
Figure 74. Multilayer Composite Print

8 References

For more information, please see the following references:

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5. RS-422 and RS-485 Application Report, *RS-422 and RS-485 Standards Overview and System Configurations*, (SLLA070).
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9 About the Author

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